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Nanofabrication approaches for Group IV Photonic MEMS devices

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Nanofabrication approaches for Group IV Photonic MEMS devices

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Abstract

Photonics has attracted a great deal of interest due to the rapid growth of the telecommunications industry. As silicon has been studied for decades in the semiconductor and microelectronics industry, the experience and infrastructure developed can be implemented in the fabrication of photonic devices. Therefore, the development of new materials and processes for this application is crucial. In this thesis, the materials and techniques used in the fabrication of suspended structures and photonic devices are studied.

Anisotropic etching is an essential technique necessary for the fabrication of photonic devices such as waveguides. The need for a reliable and repeatable etching process is discussed, along with the development of anisotropic etching recipes for silicon, silicon nitride and nano-crystalline diamond (NCD). The effect of etch roughness, along with the methods to reduce the roughness is also discussed, as well as the effect of various etch parameters on the etch rate and selectivity.

Waveguides fabricated in nano-crystalline diamond (NCD) on a silicon substrate with a propagation loss of 4.6 dB/mm has been demonstrated. The silicon substrate has to be undercut in order to isolate the mode in the NCD core, as the guiding layer (NCD) has a lower refractive index than silicon. In order to achieve this, the silicon was isotropically etched through an ICP-RIE process using SF_6.

SF_6 has been studied as an isotropic silicon etchant as a replacement for vapour phase etchants such as XeF_2. The etch rate is strongly dependent on the feature size, density and shape. This dependency is theoretically analysed, and supported experimentally. Also, the effect of this chemistry on photonic materials such as NCD, silicon nitride and silica, as well as on commonly used masking materials such as photoresists has been investigated.

Finally, a novel bonding process, which avoids the use of top down isotropic etching is presented. This can be beneficial as it enables the integration of various materials with silicon.

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Chapter 1

Introduction

1.1 Background and Motivation

Silicon has become a ubiquitous material in the electronics and photonics industry, and with the advent of integrated circuits (ICs), the processing techniques required for the fabrication of these devices have drawn considerable interest. The advent of VLSI (very large scale integration) and ULSI (ultra large scale integration) has necessitated the need for miniturisation, and therefore the development of specialised techniques. Complementary metal-oxide semiconductor (CMOS) is the state of the art processing technology which forms the cornerstone of the IC industry. The entire manufacturing process has been optimised for extremely large volume manufacturing, resulting in high yields and uniformity.

Silicon also possesses favourable optical properties as its band gap of approximately 1.1 eV ensures that the material is transparent in the wavelengths used for optical communications (between 1.3 and 1.6 μm). Silicon also has a high refractive index (3.4), which ensures high mode confinement, thereby enabling miniturisation. As a result, passive optical devices (such as waveguides) can be easily fabricated in silicon using the techniques developed for CMOS processing, thus utilising the existing manufacturing infrastructure. Various photonic components can be fabricated on a single chip, thereby forming photonic integrated circuits (PICs), which can be considered to be analogous to electronic ICs. Since PICs consist of many different individual components, it is very important that these components

are appropriately integrated with waveguides, since waveguides form the signal paths in the circuit. The interaction of the components can also be controlled via micro electro-mechanical systems (MEMS) actuation [1]. MEMS actuation has also been demonstrated in the realisation of switching arrays [2]. This requires the fabrication of suspended structures. Suspended waveguides can also increase the efficiency of chemical evanescent field sensing [3]. Hence, studying the methods and techniques used for the fabrication of these suspended structures is crucial.

In the work presented in this thesis, we present the design and fabrication of suspended structures, along with the development of the methods that are required to realise these devices. A suspended waveguide fabricated in nano-crystalline diamond (NCD) over silicon, using a novel fabrication process is demonstrated. We have also investigated in detail a related technique for the isotropic etching of silicon, which is required in the formation of membranes and overhanging structures. The effect of this etch on commonly used materials was also studied in order to understand its effect on these materials, and the results analysed. Finally, a unique bonding technique is presented, which can be used to fabricate suspended membranes.

1.2   Thesis Outline

The thesis is organised in chapters that are self-contained; the chapters that contain experimental work includes the necessary background required, experimental methods and results. Most of the SEM images in the thesis were acquired in the University of Manchester by Dr. Maziar Nezhad.

In Chapter 2, the theoretical background necessary for the understanding of the working of optical components such as waveguides is presented. Similarly, the basics of the fabrication techniques (such as lithography, dry and wet etching, and deposition) necessary for the fabrication of these devices is explored in Chapter 3.

The anisotropic etching of silicon, silicon nitride and NCD was studied in Chapter 4, with the focus being the fabrication of waveguides. It is important that the etch results in

vertical and smooth sidewalls in order to ensure that the losses are minimised. Engineering the etch is crucial, as the quality of the etch depends on various factors such as mask material, reactor size and material, pump capacity etc.

In Chapter 5, a hybrid group IV ridge waveguide platform is demonstrated, with potential application across the optical spectrum from ultraviolet to the far infrared wavelengths. The waveguides were fabricated by partial etching of sub-micron ridges in NCD grown on top of a silicon wafer. To create vertical confinement, the diamond film was locally undercut by exposing the chip to an isotropic fluorine plasma etch via etch holes surrounding the waveguides, resulting in a mechanically stable suspended air-clad waveguide platform. The optical simulations for this study were performed by Dr. Aly Abdou.

Chapter 6 consists of the study of the characteristics of isotropic etching of silicon in a purely inductively coupled SF_6 plasma. Since the etch results are strongly dependent on mask features, we investigated both large area and narrow trench etch characteristics. Circles of diameter 500 μm were used as a proxy for unpatterned surfaces and etched for different durations to establish the material etch rate and surface roughness.

In Chapter 7, we have investigated the effect of SF_6 plasma on various commonly used materials that are used along with silicon. The etch rates of silicon dielectric derivatives, SiO_2 and Si_xN_y, polymers (positive and negative photoresists and SU-8) , and nanocrystalline diamond (NCD) were studied. In particular, the effect of SF_6 on NCD has not been previously studied in depth, and therefore is of considerable interest.

In Chapter 8, the fabrication of a suspended membrane using a bonding process is described. This is an alternative method to the isotropic etch process that has been described earlier (in Chapter 5).

Finally, the conclusions are presented in Chapter 9, along with future vision and research considerations.

Chapter 2

Electromagnetic wave theory and background

2.1 Introduction

This chapter provides the theoretical background necessary for the work presented in this thesis. Here, a brief introduction to the fundamentals of electromagnetic theory along with a general background of photonic devices is given. The basic working principle as well as some of the commonly used configurations of dielectric waveguides is provided. The material properties of silicon, silica, silicon nitride, and diamond are also discussed. Both the waveguide configuration and the choice of material have an effect on the properties of the device, which are reviewed in this chapter. Finally, the common coupling techniques are discussed, as well as the numerical methods that are used to design photonic structures.

2.2 Maxwell's Equations

Maxwell's equations are a set of four equations that describe the behaviour of electromagnetic radiation. These equations were first proposed by James Maxwell in 1864 [4], and are commonly presented in the differential form as:

$$\nabla \times \mathbf{H} = \frac{\partial \mathbf{D}}{\partial t} + J, \tag{2.1}$$

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t}, \tag{2.2}$$

$$\nabla \cdot \mathbf{D} = \rho, \tag{2.3}$$

$$\nabla \cdot \mathbf{B} = 0. \tag{2.4}$$

$\mathbf{E}$ and $\mathbf{H}$ are the electric and magnetic field vectors respectively, $\mathbf{D}$ is the electric displacement, $\mathbf{B}$ is the magnetic flux density, J is the current density and ρ is the charge density.

Usually in photonics source free situations in dielectric materials are considered. Hence, we can set $\rho = J = 0$ [5]. Also, in isotropic and non-magnetic media the constitutive relations

$$\mathbf{D} = \varepsilon \mathbf{E} = \varepsilon_r \varepsilon_0 \mathbf{E}, \tag{2.5}$$

$$\mathbf{B} = \mu_0 \mathbf{H}, \tag{2.6}$$

are implicitly assumed. Applying these constraints to Equations 2.1-2.4, we get

$$\nabla \times \mathbf{E} = \frac{\partial}{\partial t} \mu_0 \mathbf{H}, \tag{2.7}$$

$$\nabla \times \mathbf{H} = \frac{\partial}{\partial t} \varepsilon \mathbf{E}, \tag{2.8}$$

$$\nabla \cdot \mathbf{E} = 0, \tag{2.9}$$

$$\nabla \cdot \mathbf{H} = 0. \tag{2.10}$$

Through the above equations and the application of the vector identity

$$\nabla \times \nabla \times \mathbf{A} = \nabla\left(\nabla \cdot \mathbf{A}\right) - \nabla^2\mathbf{A}, \tag{2.11}$$

we arrive at the Helmholtz equations.

$$\nabla^2\mathbf{E} = \mu\varepsilon\frac{\partial^2\mathbf{E}}{\partial t^2}, \tag{2.12}$$

$$\nabla^2\mathbf{B} = \mu\varepsilon\frac{\partial^2\mathbf{B}}{\partial t^2}. \tag{2.13}$$

In vacuum, $\varepsilon_r = \mu_r = 1$, and the speed of the wave is given by [6]

$$c = \frac{1}{\sqrt{\varepsilon_0\mu_0}}. \tag{2.14}$$

However, in dielectric media, the speed of the wave is slowed down by a factor equal to the refractive index of the material, n, where

$$n = \sqrt{\varepsilon_r\mu_r} = \sqrt{\varepsilon_r}. \tag{2.15}$$

An important property of an electromagnetic wave is the orientation of its field configurations, which is known as the polarisation of the wave. All electromagnetic waves can be represented as a superposition of different polarisation states [7]. The field components in the direction of propagation of the wave are used in order to categorise them. A Transverse Electric (TE) wave has no electric field in the direction of propagation and the Transverse Magnetic (TM) wave has no magnetic field in the direction of propagation. However, the field orientations cannot be sufficiently described through the transverse nature of the electric or the magnetic field. The direction of symmetry of the structure of interest should be considered in order to define the polarisation state. For example, co-axial structures such as optical fibres support Transverse Electromagnetic (TEM) modes, since they are symmetrical across the transverse plane.
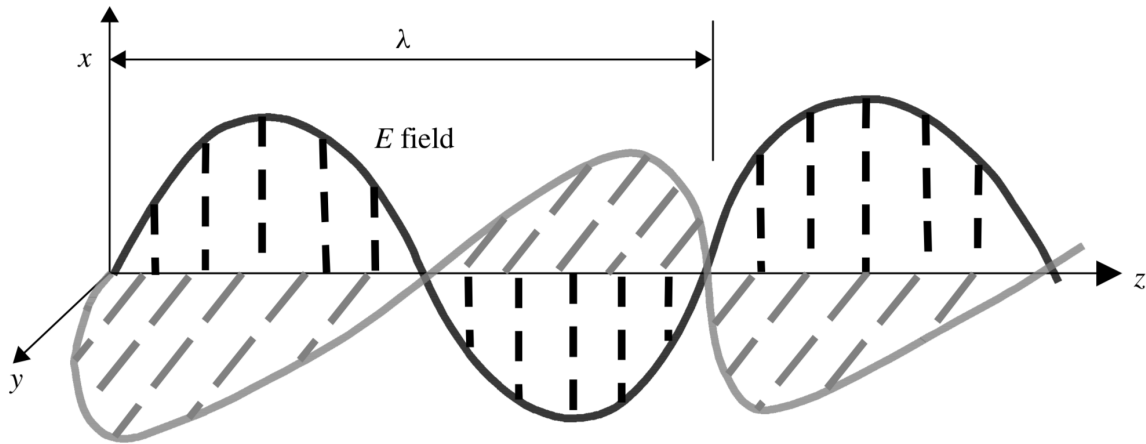
Fig. 2.1 A wave demonstrating transverse electric and magnetic fields (From [8]).

Electromagnetic waves also transmit energy, and the rate of energy transportation can be obtained from Maxwell's equations. The net power flow is given by Poynting's theorem

$$\oint_S (\mathbf{E} \times \mathbf{H}) . \partial S = -\frac{\partial}{\partial t} \int_v \left[\frac{1}{2} \varepsilon \mathbf{E}^2 + \frac{1}{2} \mu \mathbf{H}^2 \right] \partial v - \int_v \sigma \mathbf{E}^2 \partial v. \quad (2.16)$$

The quantity $\mathbf{E} \times \mathbf{H}$ on the left hand side of the equation is known as Poynting Vector, which represents the instantaneous power density associated with the electromagnetic field at any given point [9].

2.3   Waveguides

A waveguide is a structure that can confine and direct the path of an electromagnetic wave. The principle of confining light inside a photonic waveguide is the same as that of in step-index fibres, i.e total internal reflection [10]. A medium of refractive index n_{core} surrounded by a material with refractive indices $n_{cladding}$ confines light when $n_{core} > n_{cladding}$ (Figure 2.2).

When light enters a region of higher refractive index from a region of lower refractive index at an angle exceeding critical angle θ_c, the refracted fraction of the wave becomes
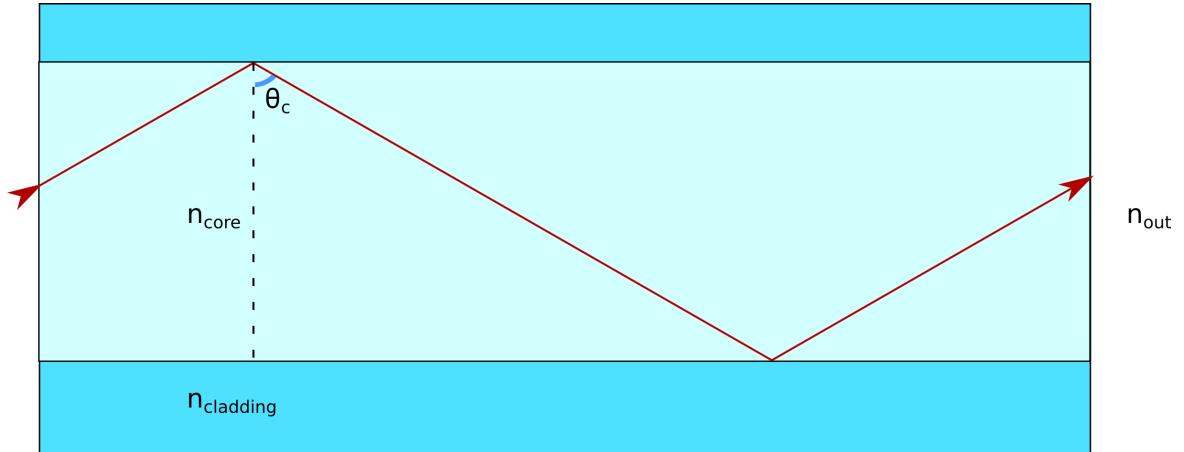
Fig. 2.2 A ray optics model demonstrating total internal reflection.

completely imaginary and all the power is carried by the reflected wave. The numerical aperture (*NA*) of the waveguide can be then defined as [11]:

$$NA = \sqrt{n_{core}^2 - n_{cladding}^2} = n_{out} sin(\theta_c). \tag{2.17}$$

In a dielectric waveguide, the power is carried in both the core and the cladding. This spacial distribution is often helpful while designing the waveguide structure. The confinement factor Γ is defined as the ratio of the power in the core to the total power.

$$\Gamma = \frac{\iint\limits_A |E(x,y)|^2 \, dxdy}{\iint\limits_\infty |E(x,y)|^2 \, dxdy}. \tag{2.18}$$

2.3.1 Modes in a Waveguide

The distribution of electric and magnetic fields inside the waveguide is given by the wave equations. In the case of a simple slab waveguide, Equations 2.12 and 2.13 become [12]

$$\frac{d^2 E_y}{dx^2} + (k^2 n^2 - \beta^2) E_y = 0, \tag{2.19}$$

$$\frac{d}{dx}\left(\frac{1}{n^2}\frac{dH_y}{dx}\right) + \left(k^2 - \frac{\beta^2}{n^2}\right)H_y = 0, \tag{2.20}$$

where β is called the propagation constant, and $k_0 = \frac{2\pi}{\lambda_0}$ is the free space wavenumber. Equation 2.19 gives the field distribution of the TE mode, and Equation 2.20 gives the field distribution of the TM mode.

(a) TE Mode   (b) TM Mode
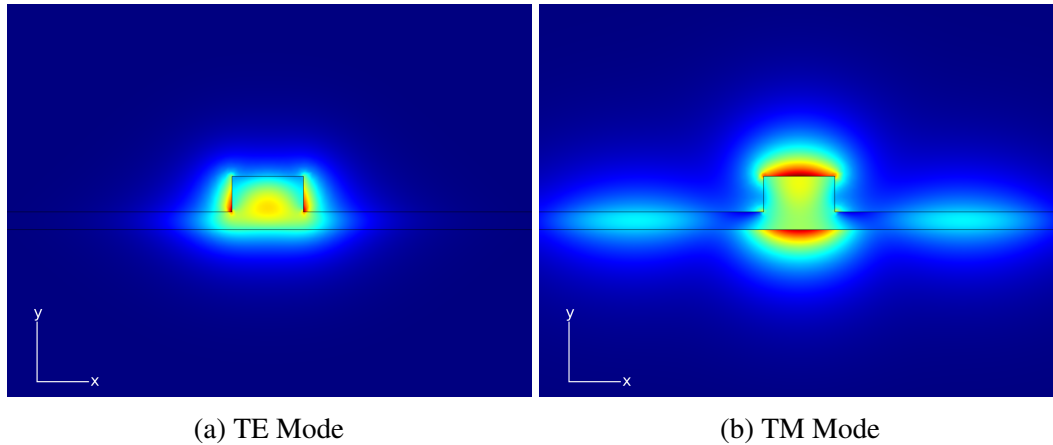
Fig. 2.3 Normalised electric field profiles in a rib waveguide.

Every value of β from Equation 2.19 and Equation 2.20 corresponds to a unique guided mode in the waveguide. The modal effective refractive index n_{eff} can be defined as

$$n_{eff} = \frac{\beta}{k_0}. \tag{2.21}$$

A similar technique cannot be used to analyse more complicated waveguide configurations (such as strip or rectangular waveguide structures). In these cases, numerical methods are used.

2.3.2 Waveguide Configurations

Dielectric waveguides can be fabricated in different configurations. Common configurations include slab waveguides, rib waveguides and strip waveguides.

Slab Waveguide

Slab waveguides are the simplest dielectric waveguide structures, consisting of a material of higher refractive index (which acts as the core) sandwiched between two layers of lower

refractive indices (which act as cladding) (Figure 2.4). Typically the thickness of the core is in the order of half a wavelength [13] for single mode operation.
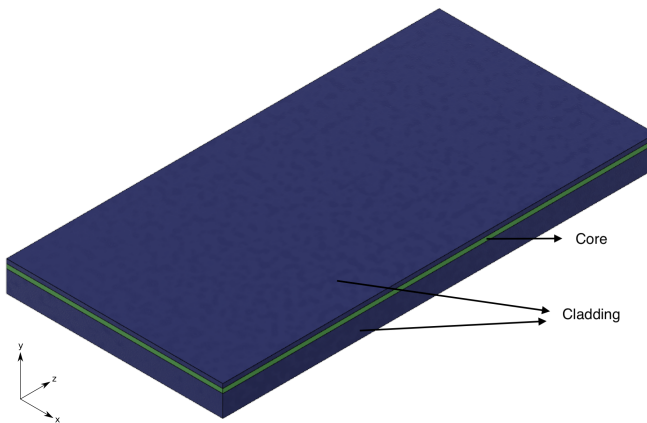
Fig. 2.4 A schematic depicting a slab waveguide. The core is shown in green and cladding in blue. The wave propagates along the z-axis.

Slab waveguides provide only lateral confinement, and therefore cannot provide horizontal confinement. Even though relatively complex integrated circuits have been demonstrated using slab waveguides [14] [15], most applications require confinement in two dimensions. This can be overcome using other waveguide designs.

Rib Waveguide

The rib waveguide structure (Figure 2.5) is formed by partially etching the guiding layer of a slab waveguide, forming an inverted 'T' profile. The central rib portion of this structure forms the main propagation area of the waveguide. This configuration is widely used as it is easily achievable on a Silicon-on-Insulator (SOI) platform using Complementary Metal-Oxide-Semiconductor (CMOS) fabrication techniques. The silicon dioxide (SiO_2) layer of the SOI platform acts as the lower cladding, and therefore should be thick enough to account for the spatial distribution of the evanescent field.
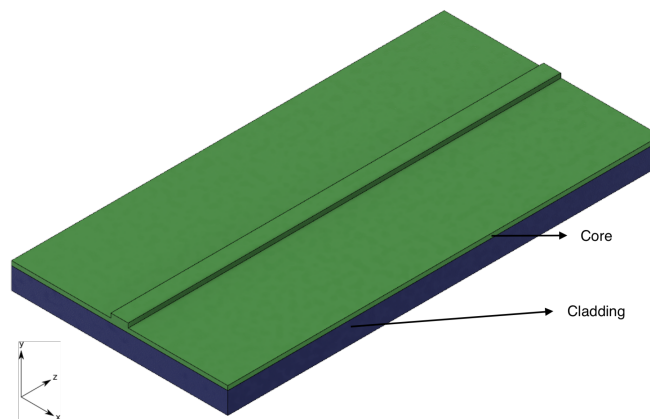
Fig. 2.5 A schematic depicting a rib waveguide. The core is shown in green and bottom cladding in blue. Air acts as the upper and horizontal cladding layer. The wave propagates along the z-axis.

A disadvantage of the rib waveguide configuration is that the etching process has to be carefully designed to achieve the exact rib height required as the partially etched part of the structure has no etch stop mechanism. However, this can be overlooked as rib waveguides generally exhibit very low propagation losses compared to strip waveguides of similar dimensions [16].

Strip Waveguide

A strip waveguide is basically a thin strip of the core on top of the bottom cladding material (Figure 2.6). As with the rib waveguide configuration, the bottom cladding should be thick enough to isolate the evanescent mode from the handle material. There are a couple of distinguishing characteristics that strip waveguides exhibit compared to rib waveguides: the higher confinement due to the vertical edges of the waveguide affects the single mode condition (and therefore the waveguide dimensions) and the scattering losses tend to be higher as the mode interaction with the sidewalls is increased. Therefore, strip waveguides are more sensitive to sidewall roughness than rib waveguides [5] [17] [18].
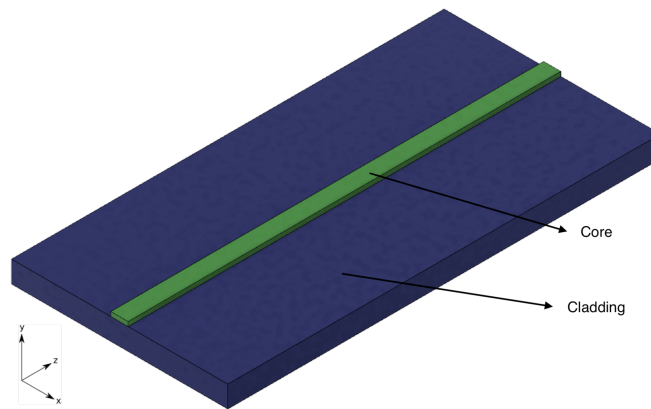
Fig. 2.6 A schematic depicting a strip waveguide. The core is shown in green and bottom cladding in blue. Air acts as the upper and horizontal cladding layer. The wave propagates along the z-axis.

2.4 Optical Materials

Silicon is a widely used material in photonics because of its abundance in nature and as it offers the ability to fabricate devices using CMOS related fabrication techniques and infrastructure [19] [20], along with its other advantages. Silicon fabrication is a mature technology as it has been the material of choice for the manufacture of transistors. It is transparent in the commonly used telecommunication spectrum (roughly between 1.3 μm and 1.6 μm), and since it has a high refractive index (3.4), it leads to high mode confinement and therefore reduction in the size of components [21]. Waveguide bends can designed to have small radii since silicon offers very high index contrast with materials like silicon dioxide and air. As it is a semiconductor, it has very low conductivity, though dopants such as boron and phosphorus can be added to increase it. Certain considerations have to be made while designing and fabricating silicon devices as they tend to be very sensitive to geometric variations and temperature perturbations because of their high refractive index and high thermo-optic coefficient [22]. Also, since silicon is an indirect band gap material, it

requires integration of other materials as sources. For example, several active devices have been demonstrated using III-V based sources and detectors [23] [24] [25].

Silicon dioxide or silica (SiO_2) is a very popular material in optical communication as it is used in optical fibres. Silica can be grown on silicon thermally, and it can be used as a mask material, as a structural material or as an optical material. As a masking material, it is commonly used as an etch mask for dry silicon etching. Optically, it can be used either as a core or a cladding material, owing to its refractive index of around 1.46. With the popularity of silicon on insulator (SOI) wafers, it is a very attractive platform for the realisation of a wide range of photonic devices. Doping of silicon and silicon dioxide can be used to alter the properties of the films, allowing for greater flexibility. Through metallisation and dry and wet etching techniques MEMS devices with electrostatic actuation can be fabricated on this platform.

Silicon nitride (Si_3N_4) is another material that can be integrated with silicon, as it can be grown relatively easily on silicon and because of its mechanical, elastic and dielectric properties [26] [27]. Hence, it can be often used for fabricating suspended structures. It is also commonly used as an optical material, as waveguides with very low propagation losses have been demonstrated [28]. As with SiO_2 it can be used as a masking material for silicon processing. Reducing film stress is especially important for creating suspended membranes and other structures. Hence nonstoichiometric silicon nitride films (Si_xN_y) are deposited through Low Pressure Chemical Vapour Deposition (LPCVD) and Plasma Enhanced Chemical Vapour Deposition (PECVD), and this is referred to as low-stress nitride. It is deposited by decreasing the $NH_3 : SiH_2$ ratio [29], leading to higher levels of Si.

Diamond is attracting interest as an optical material recently [30], because of its low absorption, high refractive index, high thermal conductivity, high density and large Young's modulus [31]. Synthetic diamond can be differentiated by its grain size: single crystal diamond, micro crystalline diamond, and nanocrystalline diamond.

2.5   Losses in Waveguides

Waves propagating in waveguides will experience losses as they travel. Attenuation can occur through scattering, absorption or radiation. The power transmitted in a waveguide is P_z at point "z" on the waveguide, and it can be calculated by:

$$P_z = P_0 e^{-\alpha z}, \tag{2.22}$$

where P_0 is the initial power, and α is the attenuation coefficient. The loss is also often described in decibels.

$$\alpha_{dB} = -10 log \left(\frac{P_z}{P_0} \right) /L \approx 4.343\alpha. \tag{2.23}$$

2.5.1   Scattering Losses

Scattering in waveguides primarily occurs due to roughness on the surface of the waveguide structure. This is known as interface scattering. However, scattering also can occur due to imperfections in the waveguide material like impurities, crystalline defects and grain boundaries, and this is called volume scattering. This is a function of the number and size of defects in the bulk material, and can be ignored in materials like silicon, but it can lead to significant losses in novel materials like nanocrystalline diamond.

The interface scattering is usually a main contributor to the propagation loss in a waveguide, especially in higher order modes. This can be reduced through improvements to the fabrication process, though it cannot be completely eliminated. As the mode interaction with the sidewalls is significant in quasi-TE modes, reduction in sidewall roughness becomes very important. The influence of sidewall roughness and waveguide dimensions on propagation loss has been established [17] [32]. Therefore, the lithography and etching steps of the process have to be carefully designed to ensure smooth and vertical sidewalls. The use of electron beam lithography helps in defining the waveguide patterns in the resist more precisely, leading to reduction in imperfections before the etch process. The etch mechanism

and the etch chemistry have to be carefully chosen in order to ensure not only smooth and vertical sidewalls, but also increase etch selectivity.

2.5.2   Absorption Losses

Absorption is a significant source of losses in dielectric materials, and can be classified into band edge absorption and free carrier absorption. Band edge absorption (also known as interband absorption) occurs when photons with energy greater than the material band gap energy get absorbed, therefore raising the electrons from the valence band to the conduction band. Therefore, waveguide materials must be chosen such that the band edge is lower than the wavelength. For example, silicon cannot be used as a waveguide material for wavelengths shorter than 1.1 μm, as silicon is highly absorptive in that region [8]. Band edge absorption is especially strong in direct band gap semiconductors.

Free carrier absorption is the phenomenon which occurs when the energy from the photon is transferred to an electron in the conduction band, or a hole in the valence band. This leads to increase in its energy, and therefore increase in loss. In silicon waveguides, free carrier density is often changed in order to affect its refractive index.

2.5.3   Radiation Losses

Radiation is another source of losses in optical waveguides, caused by modal energy lost to the surrounding material. This type of loss is generally negligible in straight, non-leaky waveguides, operating far from the cut-off region. In multi-mode waveguides, it is possible for energy to be coupled between propagation modes [33]. This leads to increased losses, as higher order modes tend to have higher radiation losses. In devices fabricated on the SOI platform, it is important that the buried oxide layer is thick enough to ensure that the mode does not leak into the silicon handle layer (Figure 2.7). This thickness depends on the wavelength being used as well as the waveguide dimensions, as smaller core dimensions lead to a greater fraction of the mode propagating in the cladding region. Figure 2.7 shows the minimum buried oxide thickness required to reduce radiation losses.
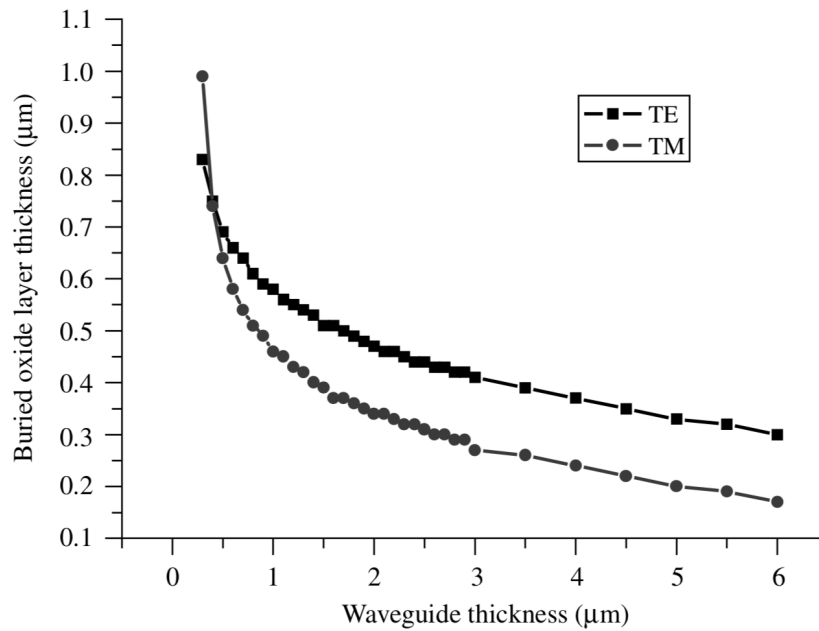
Fig. 2.7 Buried oxide layer thickness vs slab waveguide thickness to achieve less than 0.001 dB/cm loss at 1550 nm [8]. The various data points have been connected to provide a guide to the eye.

Another reason for radiation losses is because of turns or bends in the waveguide structures. In a bend, the wave has to propagate a longer distance on the outside compared to the inside, implying that velocity must be higher on the outside. This indicates that the refractive index on the outside of the bend is greater, attracting the mode towards it, and power starts leaking away from the core. Therefore, the bend radii must be designed to avoid this type of loss.

2.6 Dispersion

Generally, pulses are used in optical communication, and these pulses have a finite duration and can contain different frequencies making up the pulse. Dispersion refers to the phenomenon where different parts of the propagating wave travel at different velocities, and thus experience a spreading effect known as pulse broadening.

Dispersion in waveguides can be classified into the following categories:

1. Material Dispersion: It is important to discuss two quantities known as phase velocity and group velocity before material dispersion is defined. The phase velocity (V_{ph}) is the velocity with which phase fronts propagate in the material, and can be related to the wavenumber (k) and the angular frequency (ω) as [34]:

$$V_{ph} = \frac{\omega}{k}. \tag{2.24}$$

The group velocity in a medium is mathematically defined as the inverse of the derivative of the wavenumber with respect to the angular frequency [35]:

$$V_g = \left(\frac{\partial k}{\partial \omega} \right)^{-1} = \frac{c}{n_g(\omega)}, \tag{2.25}$$

where $n(\omega)$ is the refractive index, and the term group index (n_g) can be defined as

$$n_g = n(\omega) + \omega \frac{\partial n}{\partial \omega}. \tag{2.26}$$

Material dispersion occurs due to the wavelength dependence of the phase velocity and the group velocity in a given medium. The refractive index of a material is dependent on the wavelength, and this phenomenon is due to material dispersion.

2. Waveguide Dispersion: Since the propagation constant (β) of the waveguide is a function of the wavelength, the phase velocity also changes with the wavelength. This leads to waveguide dispersion.

3. Intermodal Dispersion: Intermodal dispersion takes place in multimode waveguides as different modes travel with different velocities, with the lower order modes travelling at higher velocities. This can be overcome by designing the waveguides to operate in a single mode condition.

4. Birefringence: Birefringence describes the effect in which different polarisations in a material or structure travel at different velocities, i.e. possess different refractive indices.

Waveguides that have been designed to reduce birefringence have been demonstrated
[36].

2.7   Numerical Methods

Analytical methods can be used to provide solutions for devices that have simple config-
urations, such as metallic waveguides. However, they cannot be used in the case of 2D
dielectric waveguides, as they tend to be inaccurate. Historically "trial and error" methods
have been used for this application. This has been primarily replaced by numerical methods,
with the advent of fast computers. Numerical methods are generally solved through partial
differential equations or integral equations, and though they usually provide approximate
solutions, they are accurate enough for engineering needs [9]. The most commonly used
numerical techniques are:

- Finite element method: This technique involves the solution of partial differential
  equations and was developed in the mid-20th century to be used in the field of structural
  engineering [37] [38]. Basically, it divides the domain into smaller and simpler
  elements, and solves the equations in these elements.

  This method provides the solutions through four steps:

  - Forming the elements

  - Approximating the field values to be constant inside the element, and defining
    the necessary equations

  - Assembling the elements of the domain

  - Solving the equations

  The main advantage of using the finite element method, is that the elements can be
  irregularly shaped and arranged, as opposed to the finite difference method which
  generally requires the elements to be arranged in grids.

- Finite difference method: The finite difference method is a numerical method which provides solutions for problems that are defined by a partial differential equation in a domain with boundary and/or initial conditions. The domain is initially divided into a grid of nodes. Then, the partial differential equations are approximated on the grid nodes through difference equations, and finally these equations are solved.

  Finite Difference Time Domain (FDTD) is a technique developed by Kane Yee [39], and it approximates the equations in a grid in the time and spatial domains. FDTD divides the region into cubes known as "Yee Cells", in which the edges represent the electric fields, and the faces represent the magnetic fields. In this way, the field values of one are used to calculate the values for the next cell. FDTD is widely used because of its ease of use, and the various scripts available freely. However, it can be challenging to mesh irregular or curved surfaces, which increases the complexity.

- Method of moments: This technique solves the Maxwell's equations in their integral form by dividing the domain into equal elements. The values are evaluated inside the elements, and the overall system is the weighted sum of the individual elements.

- Eigenmode expansion method: The eigenmode expansion method provides solutions by dividing the device cross-section into a number of layers, and decomposing the fields in each layer into local eigenmodes [40]. Since the layers are divided in a single axis, the number of elements is far lesser than finite difference or finite element methods, therefore reducing the computation time greatly. Since this technique assumes that the structure is infinite in each layer, complex structures cannot be designed accurately.

2.8   Coupling

Apart from photonic circuits that have an internally integrated source and photodetector, light needs to be coupled in and out of the circuit. The light is carried via optical fibres (in a Gaussian-like mode), and this needs to be injected into and out of the chip. This leads to a major problem, as the optical fibres are much larger than the designed waveguide

dimensions; the standard mode size of telecommunication fibres is 10.4 μm at 1550 nm, while waveguide dimensions are usually submicron. This problem is illustrated in Figure 2.8. If interfaced directly, losses often can be greater than 30 dB [41]. Therefore, an efficient method of power transfer must be used in order to minimize losses. In order to achieve good efficiency, the modes of the fibre and the waveguide must closely match in both the real space (spatial dimension) as well as the k-space (direction and magnitude of the propagation vector). Also, coupling efficiency is bidirectional, i.e the efficiency of coupling from the fibre to the waveguide is the same as from the waveguide to the fibre, assuming that there are no strong non linear effects.
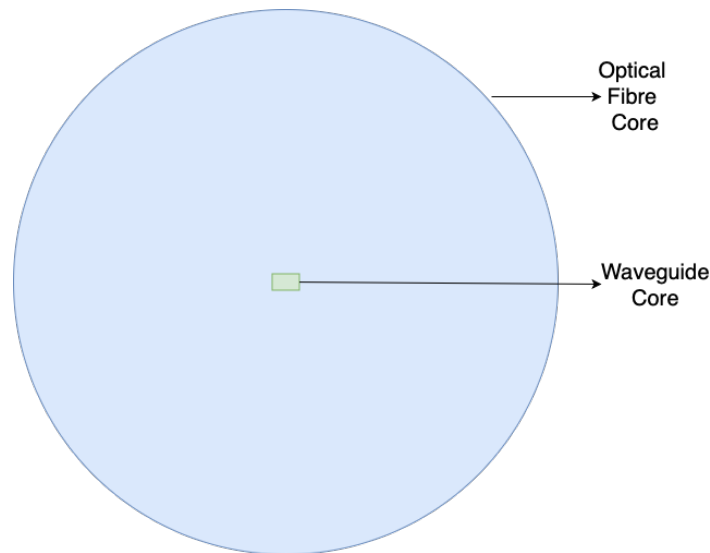
Fig. 2.8 Comparision of optical fibre dimensions and a waveguide core of 300 nm × 500 nm.

Most of the commonly used coupling techniques can be classified into in-plane or out-of-plane coupling.

2.8.1   In-plane Couplers

In-plane or edge coupling techniques are usually the simplest and the most widely used methods. One of the edge coupling methods is end-fire coupling, which uses a lens to focus the light into the waveguide edge. Since the fibre field is Gaussian, the intensity distribution at the point r, defined axially is given by,

$$I = I_0 e^{-\frac{r^2}{\sigma^2}}, \tag{2.27}$$

where σ is the $1/e$ width. To ensure optimal coupling, the lens setup must be adjusted such that the focused mode matches the dimensions of the waveguide as closely as possible.
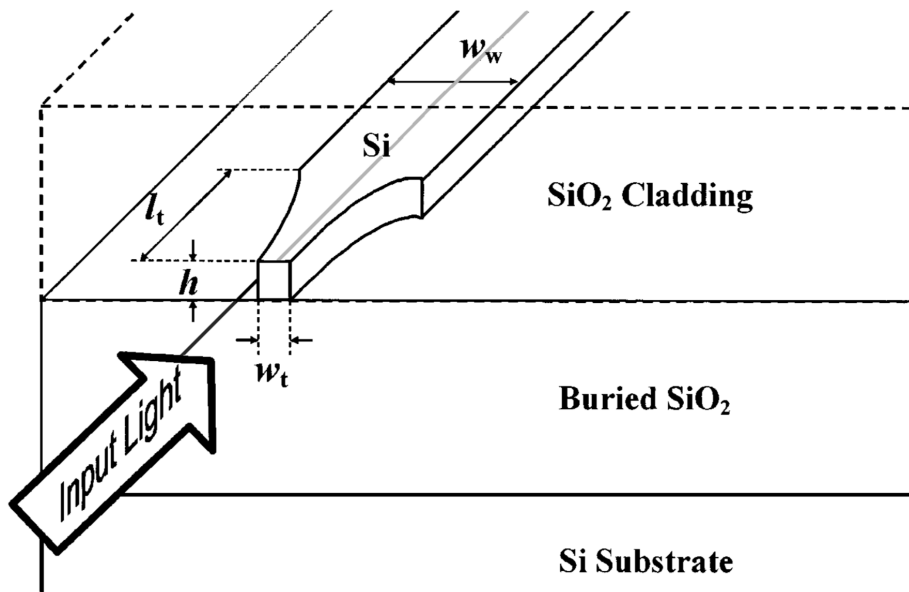
Fig. 2.9 Inverse taper coupling [32].

Butt-coupling is another form of edge coupling. It is a particularly attractive method, as it offers a very cost effective and simple solution with good coupling efficiency. In order to achieve good efficiency, the mode size of the waveguide must be increased to match the fibre mode. This can be achieved through adiabatic tapers, which involves slowly expanding the mode size by modifying the dimensions of the waveguide core. Nano-inverse tapers can be used to increase the core size to match the fibre mode size in the horizontal direction, providing good coupling efficiency. This can be improved using 3-D tapers, but this increases the fabrication difficulty. Alternatively, inverse tapers provide a good compromise between efficiency and fabrication complexity. This structure consists of a taper which is narrowed adiabatically, and surrounded by a polymer [42] or silicon oxynitride [32] overlayer, which

is designed to match the fibre mode dimensions more closely. As a consequence, the mode is 'squeezed out' of the core and spreads into the overlay material (Figure 2.9).

The coupling efficiency can be calculated through the overlap integral [43]:

$$\eta = \eta_F \frac{\left| \int E_{fibre}(x,y) E^*_{waveguide}(x,y) dS \right|^2}{\int \left| E_{fibre}(x,y) \right|^2 dS \int \left| E_{waveguide}(x,y) \right|^2 dS},$$ (2.28)

where η_F is the transmission coefficient for normal incidence, and E_{fibre} and $E_{waveguide}$ are the transverse components of the fibre and waveguide electric fields respectively.

Edge coupling techniques offer numerous reasons for choosing them as the design of choice:

- Broadband operation

- Ease of fabrication

- High coupling efficiency

- Non-sensitivity to polarization

However, there are drawbacks that have to be considered:

- Very sensitive to alignment

- Larger footprint on the chip

- Not compatible with wafer scale fabrication

- Requires additional dicing and/or polishing steps

2.8.2 Out-of-plane Couplers

Out-of-plane or grating couplers have been developed to overcome the limitations of in-plane couplers [44]. They offer a flexible device design, and low insertion losses of around 1 *dB* have been reported [45] [46]. The basic grating structure usually consists of a grid of

uniformly distributed gratings (smaller than the wavelength of the incident light) in the device layer therefore creating modulation in refractive index (Figure 2.10).
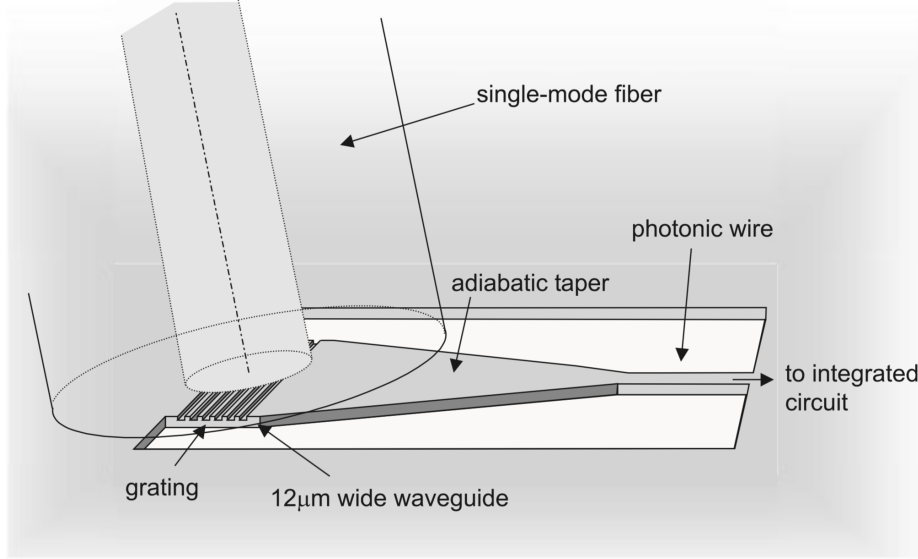
Fig. 2.10 A figure showing the coupling between an optical fibre and a grating coupler [25].

The period between the gratings is designed to aid constructive interference at the required wavelength leading to a coherent phase front, which is known as the Bragg condition. As a result, grating couplers are generally highly wavelength dependent. The Bragg relation is given by [47]:

$$\frac{2 \times n_{clad}}{\lambda} \times cos(\theta_{out}) = \frac{2 \times n_{eff}}{\lambda} \times cos(\theta_{in}) + \frac{2 \times q}{\Lambda}, \qquad (2.29)$$

where n_{clad} is the refractive index of the superstrate, λ is the wavelength, θ_{out} is the angle of the tilt of the output light (where $\theta = 0$ is the direction of waveguide propagation), n_{eff} is the weighted average of the refractive index in the etched and unetched areas, θ_{in} is the angle into the waveguide, q is the order of diffraction and Λ is the grating period.

The above equation describes an infinitely long grating. In reality, every grating scatters a part of the light, and the rest propagates in the waveguide, exponential losing or gaining power depending on if it is an output or input coupler, respectively. For an air clad fibre coupling setup, the period for second order diffraction is given by:

$$\Lambda = \frac{\lambda}{n_{eff} - sin(\theta_{out})}. \tag{2.30}$$

2.9 Summary and Perspective

The fundamentals of electromagnetic wave theory along with design considerations required for the study were detailed in this chapter. The basic theory behind wave propagation has been described along with the commonly used waveguide configurations along with material choices for devices and coupling. Effects that govern the design of optical structures such as losses and dispersion have also been outlined. The concepts introduced in this chapter provide the essential background necessary for designing photonic devices, such as the waveguides in Chapter 5. Also, understanding factors that increase losses such as surface roughness help in formulating the recipes developed in Chapter 4. In the next chapter, the basic techniques necessary for the fabrication of nanophotonic structures have been described.

Chapter 3

Fabrication

3.1 Introduction

The fabrication of nanophotonic devices involves the use of processes such as lithography, etching and material deposition. An overview of these fabrication techniques have been detailed in this chapter along with their advantages and disadvantages. Most of the processes described are fairly commonly used in modern device fabrication.

3.2 Sample Preparation

The surface of the samples must be prepared for the fabrication steps, to reduce device failure rates. The main step in the surface preparation process is the cleaning of contaminants. The most common contaminants are atmospheric dust, particles because of dicing or cleaving, polymer residue from etching, photoresist residue, and oil or solvent residue. The commonly used process is the standard degrease which consists of:

- 5 minutes soak in methanol (with ultrasonic agitation)

- 5 minutes soak in acetone (with ultrasonic agitation)

- 2 to 5 minutes soak in isopropanol (with ultrasonic agitation)

- 2 minutes rinse in flowing de-ionised (DI) water

- N_2 blow dry

A quick dip (around 30 seconds) in hydrofluoric acid is also performed if a thin film of silicon dioxide has been formed. This process can be used in conjunction with an O_2 dry plasma etch for a duration of 5 to 10 minutes. This is also known as "ashing" and helps in removing polymer and photoresist residue that might be left over. The organic impurities that might be present are removed in the degrease process where the acetone removes the impurities and the isopropanol removes the contaminated acetone.

Other cleaning processes like RCA and piranha etch are used in different situations. The RCA cleaning process is a series of steps consisting of general cleaning, particle removal, oxide removal, metal contamination removal, and finally drying of the substrate. Improper cleaning can lead to problems during oxidation, photolithography or deposition processes leading to yield loss. It can also lead to adhesion problems, which leads to the photoresist peeling from the substrate. The clean substrates are baked at above 150 ^0C for at least 5 minutes to assist in the desorption of H_2O. This is known as the dehydration bake, and immediately following this, adhesion promoters can be used. On silicon substrates, these materials form bonds with the surface and produce a polar association to the photoresist. A commonly used adhesion promoter is hexamethyldisilazine $((CH_3)_3SiNHSi(CH_3)_3)$ or HMDS.

3.3   Photolithography

Photolithography is a process used to define patterns on to the substrate (illustrated in Figure 3.1). It is an indirect method of pattern transfer, and therefore the pattern needs to be initially transferred to an intermediate material (photoresist) and then transferred to the substrate through other methods. It uses Ultra Violet (UV) light to illuminate the photoresist (which is photo-sensitive) through a photomask consisting of the required pattern. The photomask is
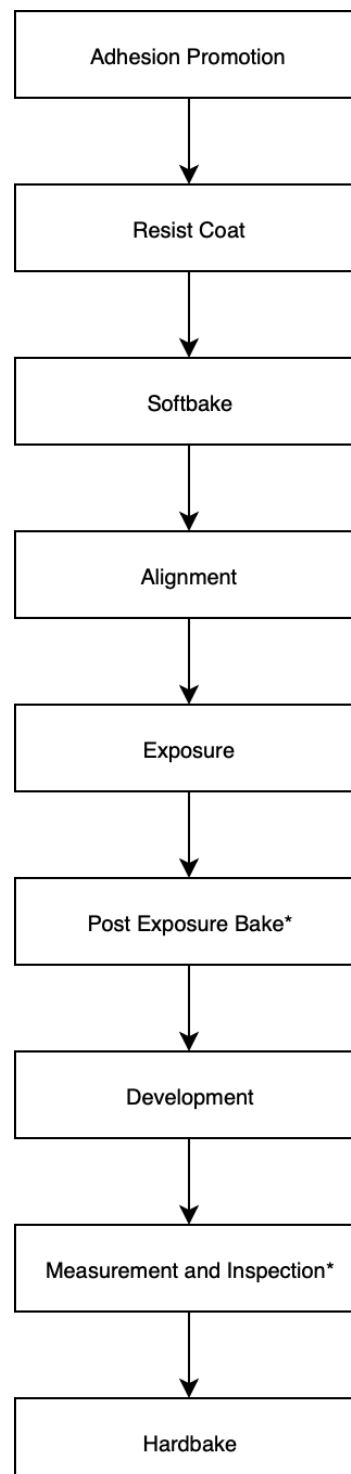
Fig. 3.1 Steps in the photolithography process. The steps marked with asterisks are optional.

usually constructed using a quartz plate patterned using chromium. A few factors have to be considered during the design of the photomask.

- The minimum feature size should be larger than the tool and photoresist capability.

- Designs should account for user and process error.

- The photomask layout should account for tool limitations (such as range of motion of the objectives, maximum and minimum mask size, layout of vacuum lines etc.)

- The substrate material, crystalline orientation and the size of the edge bead must be considered.

- Process limitations such as non uniform etch rates, loading effects and critical dimensions should be considered.

The absorption spectrum of photoresists is designed to match the emission spectrum of the lamp used. The exposure does depend on different factors like resist type, resist thickness, substrate material, etc. Optical lithography can be broadly classified into contact lithography, proximity lithography and projection lithography.

3.3.1   Contact Lithography

Contact lithography is a process which uses a tool known as a mask aligner which is used to align and expose the samples (Figure 3.2). It uses a mask consisting of the pattern that needs to be transferred. The tool can be generally be used in two contact modes (hard contact and soft contact) or proximity mode. In the hard contact mode, the sample and the mask are brought together with force, which ensures that the mask and wafers are as close together as possible. Therefore, this method achieves the best resolution. The main drawback of this method is its sensitivity to resist edge beads and the degradation of the photomask. It can also cause cracking of the resist, if the film is brittle. The soft contact mode can overcome some of these drawbacks as this mode brings the sample and the mask together, but without excessive force. However, the compromise is lower resolution compared to the hard contact

mode. In the proximity mode, the substrate is not in contact with the mask during exposure (Figure 3.3). This is the preferred method of operation when the feature sizes are large or if the resolution is not very important. Contact aligners provide alignment capabilities where the mask and the substrate can be aligned through the use of alignment marks. After the alignment, the mask and substrate are illuminated with light ranging from extreme UV (10-124 nm) to near UV (350-440 nm). Typically, a Hg lamp source is used as the source, and it consists of the g,h and i lines. The energy dose in J/cm^2 is calculated by multiplying the lamp intensity in W/cm^2 with the exposure time in seconds. Generally, contact lithography is not capable of very high resolution , but is the process of choice for processing thicker film resists. It is also favoured in experimental setups as it is relatively cost effective.
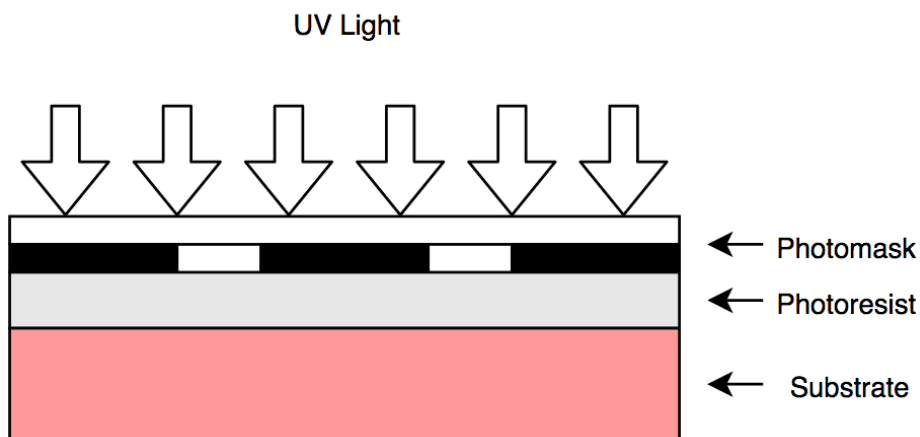
Fig. 3.2 A schematic of the contact lithography process.

3.3.2 Projection Lithography

In projection based lithography systems, a lens is used to focus the pattern of the photomask onto the substrate, and therefore contact between the mask and the substrate does not take place (Figure 3.4). They are popular for use in wafer scale fabrication techniques. There are different types of projection based systems developed including projection scanners, stepper systems (1:1, 5:1 or 10:1), step and scan systems and double sided mask aligners

UV Light
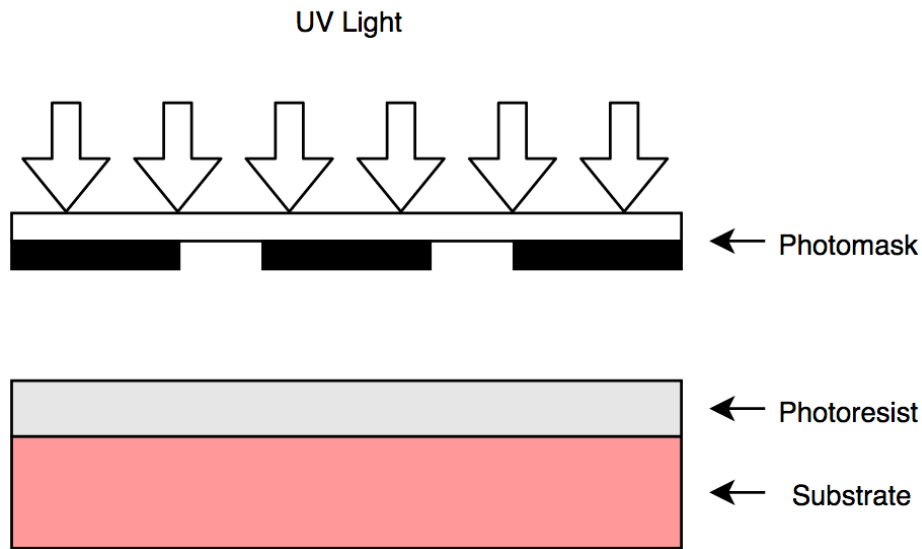
Fig. 3.3 A schematic of the proximity lithography process.

[48]. Steppers are one of most widely used projection lithography systems and they use a reticle to expose a single die at a time. The mask and the projection system then moves to the next die and repeats the exposure. In this way, the entire wafer is covered by a repeating pattern. Steppers using reduction lenses are generally favoured as they offer higher alignment accuracies and improved resolution.

3.3.3 Electron Beam Lithography

Electron Beam (or E-Beam) Lithography is a lithography technique which uses a beam of electrons to form the necessary patterns, compared with optical lithography which uses light. Since electrons have very short wavelengths, very high resolutions can be achieved, often in the range of 10 nm. This energised beam of electrons (usually between 5 KeV and 100 KeV) generated through a thermionic or field-emission cathode is focused over a resist material, and the resist is made soluble or insoluble depending on the tone of the resist. Since the beam size is small, negative tone resists are often preferred to pattern features like waveguides. Some of the commonly used electron beam resists are poly methyl methacrylate (PMMA), hydrogen silsesquioxane (HSQ), Ma-N 24xx series and ZEP series. E-Beam lithography offers many advantages over conventional optical lithography, principally the extremely
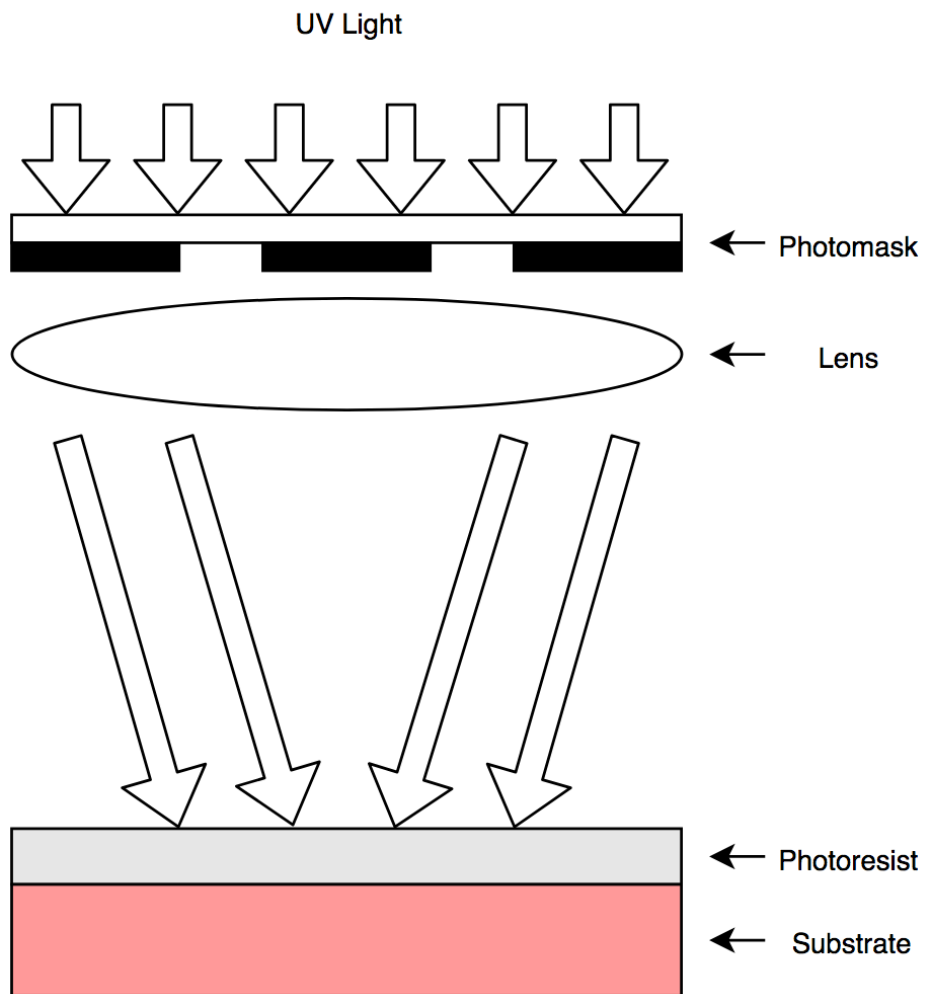
Fig. 3.4 A schematic of the projection lithography process.

small feature sizes that can be defined. It also removes the requirement of physical masks. The dosage and pattern control is also greater than optical lithography. However, certain considerations have to be made before choosing this technique:

- Because of electron scattering, the resolution is limited.

- The process is conducted in vacuum, increasing the complexity.

- This technique is considerably slower than optical lithography.

- Higher setup cost.

- Alignment errors while defining larger patterns.

The thickness of the resist film also plays an important role in the resolution. The electron beam can be broadened in the film because of electron scattering. For electron energy less than 50 KeV and resist thickness more than 0.25 μm, the following expression can be used to approximate the beam broadening [49]:

$$\sigma_f = \left(\frac{9.64t}{E}\right)^{1.75},$$

(3.1)

where σ_f is the standard deviation of beam broadening in μm, t is the resist film thickness in μm and E is the energy in KeV. Therefore, higher resolution can be achieved by reducing the film thickness and increasing the energy.

3.3.4 Photoresists

The pattern on the photomask is transferred to the substrate via the photoresist, which works through a photochemical reaction. The photoresist is made up of three parts: the resin (which is the base), the photoactive polymer (whose solubility is altered through photons) and a solvent. The smallest dimension that can be transferred is given by its resolution [50]:

$$Resolution = \frac{k_1 \lambda}{NA},$$

(3.2)

where λ is the wavelength used, *NA* is the numerical aperture of the lens and k_1 is the proportionality constant (whose theoretical limit is 0.25). Therefore, reducing the wavelength greatly helps in improving the resolution. The photoresist used is designed to be used with certain wavelengths that are widely used: 436 *nm* (which is the g-line of an *Hg* lamp), 365 *nm* (which is the i-line of a *Hg* lamp), 248 *nm* (generated through a *KrF* excimer laser) and 193 *nm* (generated through an *ArF* excimer laser). Generally resists designed to work with a mercury lamp source are novolak based with a diazoquinone sensitizer [50].

Resists are categorized into:

1. Positive resists: They develop in the regions that are exposed, and the unexposed regions remain on the substrate. Positive resists form an indene carboxylic acid during exposure and are soluble in aqueous alkaline solutions. They do not cross link on exposure, and are prone to reflow at high temperatures.

2. Negative resists: They behave in the opposite manner to positive resists, i.e the exposed regions cross-link and remain on the substrate, while the regions not exposed wash away in the developer. They are thermally very stable due to cross-linking and retain the resist profile even at high temperatures.

3. Image reversal resists: They are resists that can be used in either positive or negative tone. In the positive mode, they work as a positive resist, but in the image reversal mode, they are subjected to an image reversal bake followed by a flood exposure. In this mode, the degree of cross-linking is low, and high temperatures would lead to resist reflow [51].

The photoresist can be applied in three main ways: spray coating, dip coating and spin coating. Spin coating is the most widely used method, and deserves a brief overview of the process.

In this method, liquid photoresist is dispensed onto the substrate(either when it is stationary or already spinning). The spinning of the substrate creates centrifugal forces, producing a thin and uniform of photoresist on top of the surface.The thickness of the resist is dependent

on the substrate size, material, spin speed and viscosity. The exact modeling of the spin coating process is hard to model as the photoresist volume lost not only depends on the centrifugal forces but also the evaporation of the solvents in the material. The resist thickness can be expressed using the equation:

$$t = \frac{ks^2}{\sqrt{\omega}},$$ (3.3)

where t is the film thickness, k is a constant related to viscosity, s is the solids content in the solution and ω is the angular velocity.

Spin coating has a few advantages over other resist dispersion techniques such as good uniformity and short coating time. However, it also has drawbacks, with one of the biggest being the formation of the so called "edge bead", which is a pronounced edge formed at the edge of the sample. This can cause problems during contact exposure of the resist. This can be reduced or eliminated altogether by using edge bead removal (EBR) solvents (if using a circular substrate), by increasing the spin speed for a shorter duration or coating the sample using multiple steps with higher spin speeds.

3.3.5   Baking Steps During Photolithography

Soft Baking

The photoresist films after spin coating still have a considerable amount of solvents present. A baking step known as "soft baking" is performed in order to reduce the solvent content. This is important for a few reasons like improving adhesion, reducing dark erosion during development, avoiding mask contamination due to resist sticking, etc. The softbake has to be performed at the right temperature for the required amount of time, both of which are dependent on factors like resist type, film thickness and substrate material. If the softbake is not hot enough or long enough, the solvents will still be present in the film, whereas if it is too hot or too long, it will lead to resist decomposition leading to lithography issues. During the softbake, the water concentration of the resist film (which is required for resist development and to improve the resist profile) is reduced greatly. In order to offset this, water

has to diffuse from the atmosphere into the resist film. Hence, a delay after the softbake is recommended to facilitate rehydration [52].

Post Exposure Baking

Following the exposure of the photoresist, performing a post exposure bake (PEB) can be beneficial in certain situations. It can used to complete the exposure process of chemically amplified resists, cross-link negative resists, reduce mechanical stress in resist film and reduce the effects of standing waves during long exposures.

Hard Baking

Finally, following the resist development the resist can be baked at a higher temperature to change the properties of the patterned film. This is called "hard baking", and it can increase the resilience of the film (physically and chemically). Hardbaking generally improves the resist adhesion to the substrate, increase the etch resistance and might cause resist reflow. It might also embrittle the resist and introduce crack in the film. This can be reduced by slowing down the cooling process post bake. Hard baking at a high temperature for a longer duration also makes resist removal difficult due to thermal cross-linking [53].

3.3.6   Resist Removal

Removal of photoresists can depend on the resist composition, baking parameters and other processes that the resist film might have gone through. Though acetone is often used to remove photoresist residue, it is not very well suited for this purpose, as the high vapour pressure of acetone results in fast drying and form striations. NMP (1-Methyl 2-pyrrolidon) and DMSO (Dimethyl sulfoxide) are ideal resist strippers for most applications.

If positive resists have been exposed to temperatures greater than 150 $^{\circ}C$, thermally activated cross-linking occurs, making removal of the film very difficult. In such cases, oxygen plasma etching might be necessary for complete resist removal.

3.4   Etching

The term "etching" describes the selective removal of material through physical or chemical processes. It is generally used to remove material not protected with a hard mask (like photoresist), and therefore pattern the material. However, it is also sometimes used to remove an entire unrequired layer of material. Materials can be etched either through dry or wet etching techniques, the choice of which is dependent on the material to be etched and other factors like the degree of anisotropicity desired, the mask material etc.

Though low loss waveguides fabricated using wet etching [16] have been demonstrated, dry etching is usually preferred for fabricating devices having submicron dimensions whereas wet chemical etching is generally favoured for removing unpatterned material, shaping 3D microstructure, surface cleaning and removing surface damage [48].

The performance of an etch process can be measured qualitatively and quantitatively through parameters such as etch rate, uniformity, selectivity and directionality. In this section, these parameters are discussed, and are applicable more to elemental semiconductors. Etch rate, which is the measure of how fast the material is being removed, is one of the main parameters to be considered for selecting the appropriate process or techniques as other parameters like selectivity and uniformity often dependent on it. Etch uniformity is an important factor to be monitored especially during wafer-scale fabrication of devices, as different areas of the material can be etched at different rates.

Usually, a high degree of selectivity is preferred, so that the etchant removes the unprotected material faster than the mask material. The etch rates of all the materials of the device have to been determined before designing and implementing an etch process.

3.4.1   Wet Etching

Wet etching is a process in which liquid etchants are used to remove material. It usually involves multiple chemical reactions, and can be broken down into three steps:

1. Diffusion of the etchant to the etch site.

2. Chemical reaction between the etchant and the material to be removed.

3. Diffusion of the byproducts in the etchant away from the etch site.

Because of this etch mechanism, wet etchants generally perform better when stirred during the process, as fresh etchant is brought close to the etch site while the byproduct are taken away.

Wet etching generally tends to be a highly isotropic process even in the presence of a mask, as the etchant can enter under the mask. Hence wet etching is not a favorable method when etching thick films or when defining patterns that have very low horizontal tolerances. However, anisotropic profiles can be achieved depending on the etchants used and the crystalline axis of the substrate, in which case Miller indices become very important.

One of the major advantages of wet etching is its very high selectivity over mask materials [54]. Wet etching also tends to have a much higher etch rate than dry etching techniques. However, wet etching is not suitable for all etching applications, as it is associated with drawbacks like operator safety and the dependency on crystalline structure. One of the major disadvantages of wet etching is that the capillary forces associated with the liquid etchants can be damaging to free standing structures like MEMS devices or overhanging membranes [55].

Potassium hydroxide, tetramethylammonium hydroxide (TMAH), ethylenediamine pyro-catechol and HNA (hydrofluoric acid, nitric acid and acetic acid) are widely used etchants of silicon commercially [55][56][57].

There are various ways in which wet etch processes can be affected. This can be due to

- Changes to the setup such as temperature [54], reduction in etchant volume [58], etch duration etc.

- Variations in material such as impurities, film stress [59] etc.

- Layout of the material like crystalline orientation and loading [54].

Wet Etching of Silicon Dioxide

Hydrofluoric Acid (HF) based etchants are primarily used to etch silicon dioxide. As pure HF has a boiling point of 19.5 ^0C [54], and it is completely soluble below its boiling point,

HF is supplied at up to 49% concentration. This reduces the vapour pressure, allowing it to be stored at room temperature. Concentrated *HF* etches silicon dioxide extremely aggressively. It also leads to resist delamination. Therefore is used only for etching unpatterned sacrificial layers, and diluted HF (below 3:1) is generally preferred for etching patterned oxide. The more commonly used etchant is 5:1 Buffered Oxide Etch (BOE), which is a mixture of 5 parts of ammonium fluoride to one part of 49% HF. This formulation of etchant does not affect the resist adhesion, and the etch rate remains relatively unaffected even after use [54]. The overall equation in BOE is:

$$SiO_2 + 4\,HF + 2\,NH_4F \rightarrow (NH_4)_2\,SiF_6 + 2\,H_2O \tag{3.4}$$
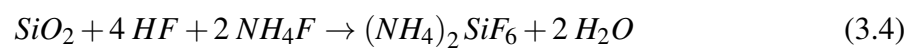
Wet Isotropic Etching of Silicon

One of the most commonly used isotropic silicon wet etchant is a mixture of hydrofluoric, nitric and acetic acids, also known as HNA. It is etched in a two step process, with the nitric acid oxidising the silicon, the hydrofluoric acid etching the oxide and the acetic acid acting as a buffering agent [54].

$$18\,HF + 4\,HNO_3 + 3\,Si \rightarrow 3\,H_2SiF_{6(aq)} + 4\,NO_{(g)} + 8\,H_2O \tag{3.5}$$
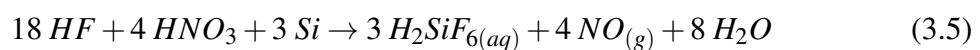
For this process, silicon nitride is the masking material of choice, as silica is aggressively etched in HNA. Hence, this method cannot be used in fabricating devices with silica or patterned using materials like HSQ.

Wet Anisotropic Etching of Silicon

Potassium hydroxide (*KOH*) is the most commonly used silicon etchant for isotropic or orientation dependent etching (ODE) of silicon. In this etching technique, the Miller index of the single crystal silicon becomes very important as the etch rate is very heavily dependent on it (Figure 3.5). For example, of the three most commonly used crystalline orientation of silicon available commercially (<100>,<110> and <111>), the <111> plane is etched

much slower than the other two orientations. This is explained by the fact that the <111> orientation has a higher bond density, but this explanation does not hold true for the etch rate ration between <100> and <110> planes [60]. In order to improve the etch uniformity, isopropyl alcohol (IPA) is added. However, this has an adverse effect on the etch rate [58], but it has been found that the etch rate ratio between the <110> and <111> planes improves. The overall chemical reaction is [58]:

$$Si + 2\,OH^- + 2\,H_2O \rightarrow SiO_2(OH)_2^{2-} + 2\,H_{2(g)} \tag{3.6}$$
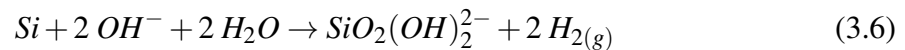
At 85 ^0C an etch ratio of 400:200:1 has been found between the <110>,<100> and <111> planes [60].
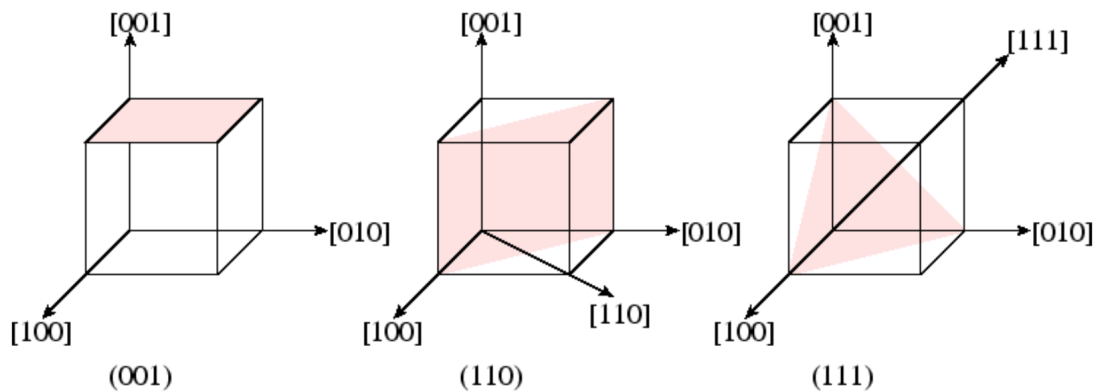
Fig. 3.5 The crystalline structure of silicon along with the Miller indices.

3.4.2   Dry Etching

In dry etching, a plasma or a suitable gas (or a mixture of gases) is used to remove the required material. The etching mechanism can involve a physical etch, the chemical effect of plasma or the etch gas or a combination of the two.

In a physical etch, the etching takes place directly through non-reactive beams that is incident on the material. The kinetic energy of the beams transfer their momentum to the substrate, but no chemical reaction occurs. Ion Beam Etching or IBE is one of the more

popularly used physical etching techniques and argon (which is a noble gas) is widely used as the etchant. Physical etches generally suffer from low selectivity, as the beam affects the whole surface almost evenly.

Chemical etching can be done in vapour phase (which involves no plasma) or plasma phase (which is more commonly used). In plasma etching, neutral chemical species are generated in the plasma, and they attack the substrate chemically to form volatile products.

Reactive Ion Etching or RIE is an etching method that uses both physical and chemical etching mechanisms, with the ions physically attacking the open surface, and thereby allowing chemical reactions to happen at the surface. It also utilises the formation and the subsequent removal of passivating polymers on the surface, which plays an important role in the anisotropic nature of the etch.

Dry etching techniques were primarily developed to remove photoresist and other polymers in the 1960's, and the technique was further developed in the 1970's for the anisotropic etching of materials like silicon [61].

Dry etching has an advantage when defining precise patterns, as highly anisotropic profiles can be achieved compared to wet etching techniques. A technique known as Bosch etching is commonly used in order to achieve very anisotropy, thereby enabling deep etching of patterned silicon. This has been discussed further in Chapter 4. Dry etching also provides a huge level of flexibility as the degree of anisotropicity (Figure 3.6), and hence the profile (undercut vs. overcut) can be tuned by altering various process parameters. Another benefit of dry etching is the small volume of the etching gases that is required compared to the volume of the etchant required during wet etching [62].

Silicon, silica and silicon nitride are commonly etched using fluorine-based chemical etches [8]. Due to the mechanism of the etch, the variable conditions of the etch like power, pressure, gas flow rates, electrode materials and temperature play a big part in the quality of the etch. The properties of the material being etched (such as microloading, masking material and film stress) are also of significance.
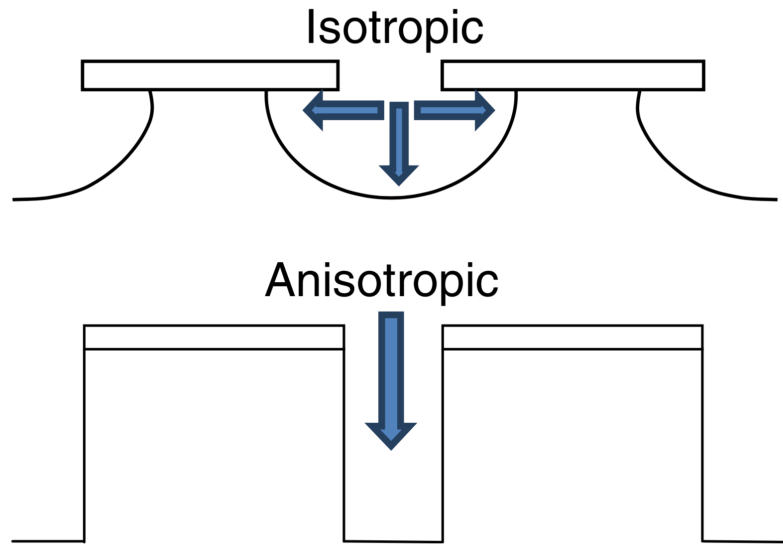
Fig. 3.6 Isotropic vs anisotropic etch profiles [63].

Vapour Phase Etching

The common etching technique used to remove sacrificial layers, to form membranes or to release MEMS structures is wet etching. This is a very sensitive process, especially as the wet etchants have to be rinsed away after the etch and capillary forces are formed during drying. These problems can be eliminated through vapour phase etching, which is a technique in which the etching of the material takes place in the vapour state of the etchant. The mechanism of the etch is similar to wet etching and can be used to replace it therefore overcoming the problems associated with it as mentioned earlier.

As in the case with wet etching, the etch is completely chemical in nature and without a physical component. Therefore, it results in isotropic etch profiles. As the etch occurs in the vapour state and the etchants react with the substrate readily, the etch takes place without a plasma. Due to its advantages over wet etching, it is widely used for MEMS device fabrication.

Vapour phase etching of silicon can be performed using chemicals like xenon difluoride (XeF_2), bromine trifluoride (BrF_3) and chlorine trifluoride (ClF_3)[64] [65]. Since its synthesis in 1962 [66] [67] [68] , and subsequent development as an isotropic etchant [69],

XeF_2 has been widely used as a vapour phase etchant, as it is highly selective to silicon with respect to aluminium, photoresist and silica. Similarly, silica has been selectively etched using a similar process using HF vapour.

XeF_2 is fairly easy to use, as it is a white solid at room temperature and pressure, vapourising at pressures below 4 Torr. Due to microloading factors, the etch rate is highly dependent on feature size. One unintended consequence of using the XeF_2 etch is that it reacts with moisture, forming HF, which in turn etches SiO_2 [48]. This may lead to selectivity issues when using a silica mask . It also requires specialised equipment and it is not integrated into conventional CMOS processes. Furthermore, both the equipment required for the etch and the chemical itself are niche and somewhat expensive, making the process less economically viable.

The chemical reaction for the etch is [70]:

$$2XeF_2 \rightarrow 2Xe + SiF_4 \qquad (3.7)$$

XeF_2 vapour phase etching is also associated with a few disadvantages. The biggest disadvantage is that it has no etch stop mechanism. Since the XeF_2 etching is not dependent on the crystalline orientation of the substrate, the etch will not stop at a plane that etches slower (as it does in KOH wet etching for example). Also, since the etch is vapour based, it is associated with the usual safety hazards that vapour fumes possess. Similar to the XeF_2 based silicon etch, silica can be etched in HF vapour. The same advantages are applicable to this method as well.

Plasma Etching

Plasma is generated when one or more gases are held at a low set pressure, and an electrical source is used to ionize the gases. The electric power drives the chemical reactions, and replaces high temperature or very reactive chemicals. A stable plasma is obtained by ionizing the particles in the gas mixture, and forming a "soup" of ions, electrons and free radicals. The role of the plasma in this etching technique is to provide the highly reactive etchants. The radicals formed in this process react with the material of the substrate, and etching

takes place (Figure 3.7(b)). The byproducts produced are then pumped away. Plasma can be formed using either DC or AC power sources. A major problem with using a DC source is that it cannot be used to etch insulating substrates, as charges do not get dissipated, leading to unstable plasma. This is overcome by using an AC power source. Generally, Radio Frequency (RF) power sources operating at 13.56 MHz are used to ionise the etch gases inside a vacuum chamber. This frequency is used as it has been set aside as one of the Industrial, Scientific and Medical (ISM) bands. However, other frequencies are used for different applications.

Since the mass of an ion is vastly higher than the mass of an electron, it cannot react to the change in polarity above its plasma frequency. This leads to a build up of negative charge near the electrodes, causing the plasma in this area to be extinguished and the formation of a dark region commonly called the sheath [8].

The plasma etch takes place in six major steps [48]:

1. Generation of reactive species

2. Diffusion to the surface

3. Adsorption on the surface

4. Chemical reaction

5. Desorption of byproducts

6. Diffusion into bulk gas

Gases rich in fluorine like CF_4, SF_6 and CHF_3 are used to etch silicon, silica and silicon nitride. Organic polymers like photoresist are etched in oxygen plasma, where oxygen atoms reach with the carbon and hydrogen atoms present in the polymers. Therefore, plasma etching is commonly used in the removal of photoresists after etching or metal deposition. In this context, plasma etching is often referred to as "ashing".
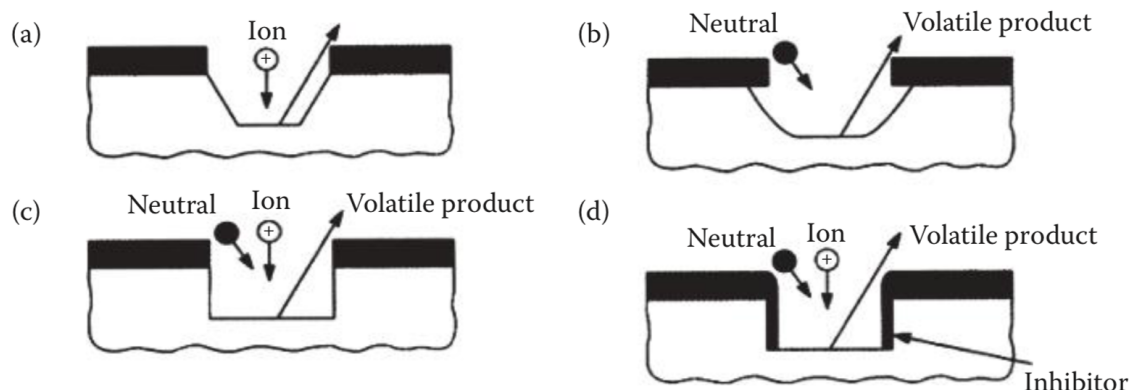
Fig. 3.7 Dry etching techniques. (a) Physical etching, (b) Plasma etching, (c) and (d) Reactive ion etching [48].

The advantage of plasma etching over other dry etching techniques is that as the etching is almost completely chemical, there is very little unintended surface damage, leading to very high selectivity.

Plasma etching is carried out in plasma chambers, generally constructed in stainless steel and containing two parallel plate electrodes (Figure 3.8). The necessary etch gases are allowed to flow into the chamber at the designed set flow rate. The chamber is also actively pumped, and the balance between the gas flow rate and the pump rate is used to maintain the chamber at the required pressure. An electrical voltage is applied between the electrodes leading to the formation of plasma. Different gas mixtures produce different plasma glow colours. The gas flow rate, the chamber pressure and the power can be all changed to alter the etch characteristics.

Reactive Ion Etching

Reactive Ion Etching (RIE) is a plasma etching technique which combines the chemical nature of plasma etching and the physical nature of ion based etching, in order to remove material from the substrate. Energetic ions and free radicals bombard the surface simultaneously, and it has been demonstrated that the etch rate in this technique exceeds the etch rate of ions and

ETCH GASES

ELECTRODES

SUBSTRATE

PLASMA

RF

TO PUMP
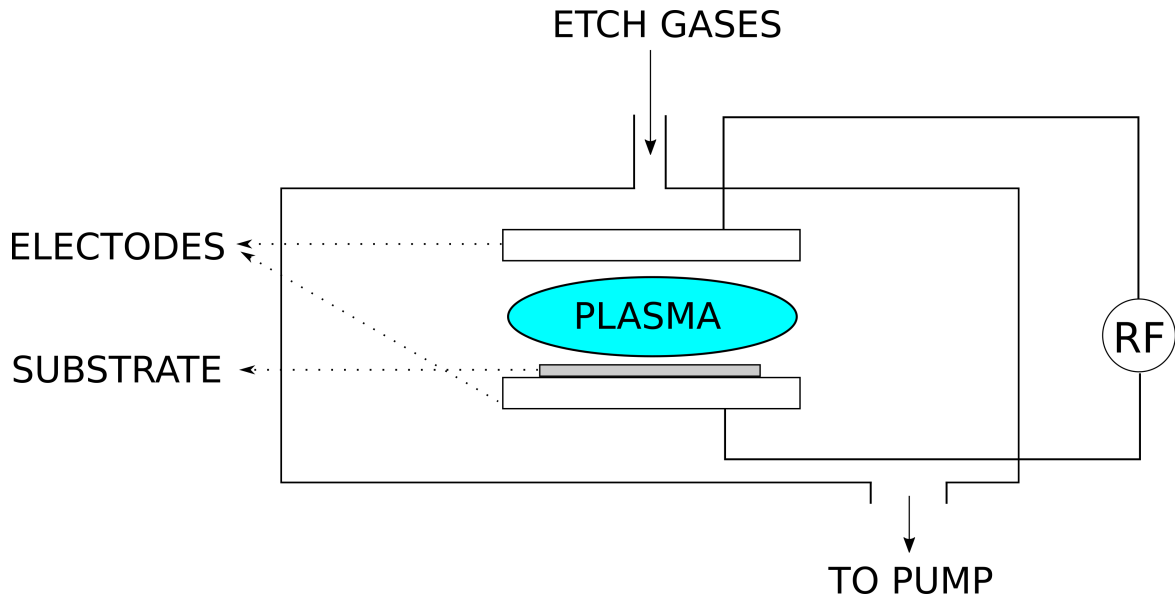
Fig. 3.8 A schematic layout of a plasma etching system.

radicals on their own [50] (Figure 3.7(c) and (d)). As a result, it is possible to etch materials independent of their crystalline orientation.

The RIE etching setup is slightly different compared to the plasma etch chambers. The wafer is placed on an electrode that is smaller than the other electrode, and is powered using an AC source generally operating in the RF region of the spectrum. As a result of the uneven electrode sizes, a potential difference is established between the electrodes. This causes the ions to be driven towards the electrode, therefore leading to a directionality to the etch.

One of the major advantages of using RIE is that the etch can be engineered to be anisotropic, leading to very vertical sidewalls. This is an important technique used in micro and nanofabrication to produce small features. It is also important that the etches do not take place in the horizontal direction. The choice of etch gases and parameters like chamber pressure, temperature, gas flow etc. are all important factors that determine the verticality of the etch. Another important feature of RIE is polymer deposition. This is formed during the etch, and helps in protecting the sidewalls from being attacked chemically by the etchants, leading to more vertical etch profiles.

One of the simplest and commonly used configurations of RIE systems is the Capacitively Coupled Plasma (CCP) RIE method. In a CCP-RIE etcher, gas is fed into an etch chamber,

and an RF voltage is applied between two parallel electrodes. This ionises the gases in the chamber, and the plasma generated is used for chemically etching the material (Figure 3.9). Due to the higher electron mobility (compared to the ion mobility), the low electrode becomes negatively charged, and this in turn leads to the formation of the positively charged sheath above it. The acceleration of the ions in the chamber towards the negative electrode is proportional to the potential build up in the electrode (known as the DC bias). This provides the kinetic energy to the ions, and is the source of the physical component of the etch.The RF power has the largest influence on the DC bias, though it is also affected by factors like chamber pressure, gas composition and gas flow. Since the DC bias is linked to the RF lower source, the impact of the ion based etching cannot be controlled independently.

Fig. 3.9 A schematic layout of a CCP-RIE reactor.

Another type of reactive ion etching is known as Inductively Coupled Plasma (ICP) RIE. In this method, the ionisation of the gas takes place separately and away from the

substrate. The system is powered by two RF sources, where one is used to generate the plasma (inductively) and the other is connected to the electrode for ion acceleration (providing the DC bias) (Figure 3.10). The powered coils surrounding the chamber result in a changing magnetic field, leading to an induced electric field inside the chamber. Due to the discrepancy in the momentums of electrons and ions, collisions occur, causing further ionization. The entire system therefore can be thought of as a combination of two separate units: one to control the number of ions generated, and the other to control the momentum of the ions. The possibility of generating a high density plasma without very high ion energy is an attractive proposition, as lower ion energy improves the physical etch selectivity and also reduces the damage to the substrate caused by ion bombardment. However, this can lead to lower etch rates and reduced anisotropy. High density plasma fixes this issue, as the etch rate increases due to the amount of highly reactive species present in the chamber. The anisotropy is increased owing to the fact that ICP-RIE systems can be operated at much lower pressure compared to CCP-RIE systems.

The electron density and the gas dissociation factor in CCP-RIE systems are lower than Induction Coupled Plasma (ICP) RIE systems. They also generally operate at a higher chamber pressure which results in scattering, and ultimately less vertical etch profiles. At the usual RF powers used in this method (between 100 W and 3000 W), re-sputtering due to micro masking is also a major concern, and can lead to micrograss [71].

Physical Etching

Physical etching uses ions from inert gases (like *Ar*), which are accelerated in an electric field towards the substrate, therefore leading to etching (Figure 3.7). As this technique is impact dependent and the surface bond energies are very small compared to ion energies, it is nonselective [48]. Though it is slower than chemical dry etching, it can be a very useful method to etch materials without chemical etchants. Ion beam etching (IBE) and sputter etching are two of the commonly used physical etching techniques.
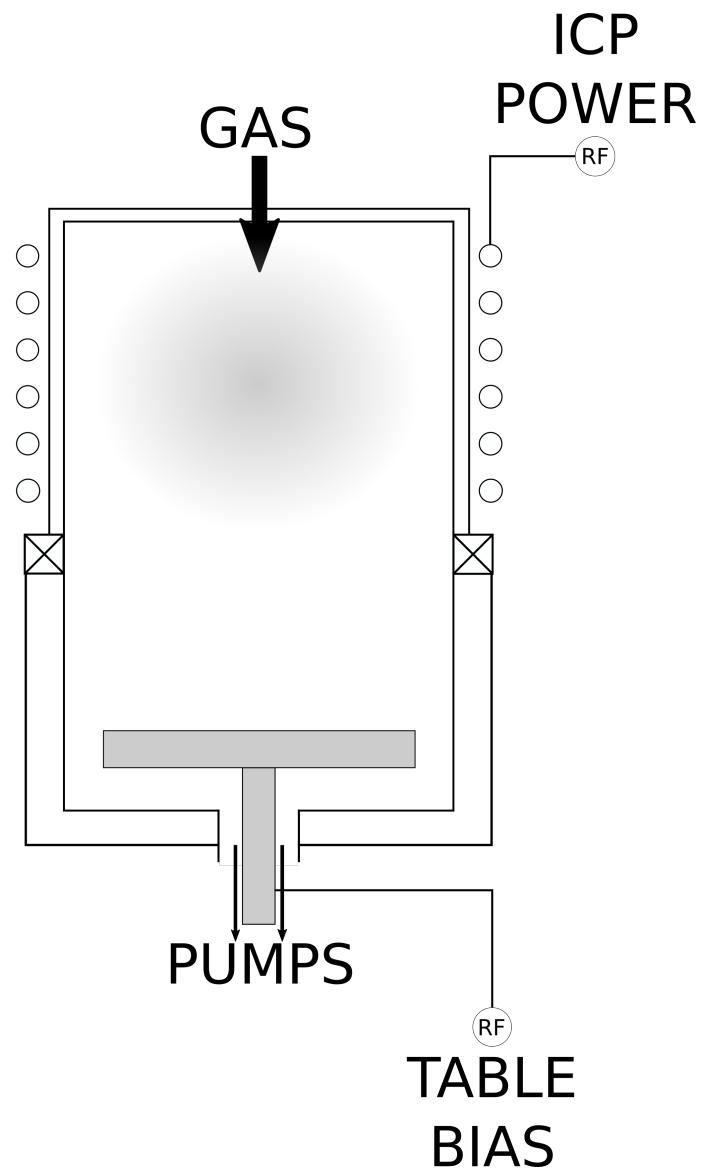
Fig. 3.10 A schematic layout of an ICP-RIE reactor.

Sputtering etches the substrate material by bombarding its surface with highly energised ions or neutrals. These particles transfer their energy to the substrate atoms through scattering, leading to their removal. Sputter etching also is characterised by threshold energy, below which etching does not take place. As different materials sputter at different rates, etching of non atomic substrates often leads to change in material structure near the surface [50].

Ion beam etching is a method of etching, where the plasma is created remotely, and accelerated towards the substrate which is placed on a third electrode. It can be operated through a DC or RF power source, as the charges from the substrate can be extracted using an auxiliary thermionic cathode, hence allowing etching of even insulators.

Physical etching is not always the favourable method for etching patterns, as it tends to form facets, ditches and hourglass shaped trenches [48]. Damage to the substrate and redeposition of the etched material can be potential issues.

Dry Etching Parameters

Anisotropy in the context of etching is the preferential removal of material in one direction. In wet etching, anisotropy is achieved as a result of difference in etch rates due to the crystalline orientation, However, in dry etching anisotropy is achieved because of preferential etching in the vertical direction due to ion bombardment or formation of inhibitors on the sidewalls to protect them. The degree of anisotropy can be defined as [72]:

$$A = 1 - \frac{H}{V}, \tag{3.8}$$

where H is the etch depth in the horizontal direction and V is the etch in the vertical direction. Therefore, perfectly anisotropic etches have $A = 1$, where as completely isotropic etches have $A = 0$.

Uniformity is the measure of etch rates across the entire substrate. It is preferable to have very low variance across the surface, especially if the processes are performed wafer

scale. Various plasma parameters like RF power, pressure and flow rates can alter the uniformity. The degree of uniformity can be calculated using:

$$U = \frac{E_{max} - E_{min}}{E_{max} + E_{min}}, \tag{3.9}$$

where U is the uniformity, and E_{max} and E_{min} are the maximum and minimum etch rates respectively.

Selectivity is the ratio of the etch rate of the material to be etched to the etch rate of the masking material. The selectivity can be mathematically defined as:

$$S = \frac{E_S}{E_M}, \tag{3.10}$$

where S is the selectivity, E_S is the etch rate of the substrate or the material of interest and E_M is the etch rate of the masking material. Most etching process are designed to be as selective as possible by choosing the etch mechanism, etch chemistry and masking material appropriately. Purely chemical etches are generally highly selective, where as physical etching processes are least selective. Selectivity in RIE processes is dependent on the degree of ion bombardment.

Microloading is an effect which is caused due to the dependency of the etch rate on the area of open substrate in a particular region. Regions with large open spaces use up the etchants faster than regions with smaller open areas. If the reactive species in the plasma are not brought to the area fast enough, the etch rate will be decreased in the areas with large features. The flow rate of the etchant gases has a big impact on this effect [73].

Aspect Ratio Dependent Etching is similar to microloading in that larger features are etched faster than smaller features. This mechanism is due to the difference in the way ions and radicals etch the substrate material at the bottom of a trench. As a result of this effect, over time the bottom of trenches can become non-uniform.

Micro-masking is a phenomenon that occurs in etches that have a physical component. The ions used in the etch also sputter the material surrounding the substrate, leading to their redeposition on top of the surface of the samples. This leads to areas in the surface being masked by these particles, leading to the formation of grass or other needle like features.

Etch profile is the shape of the sidewalls during anisotropic etch processes. Since processes like RIE depend on various etch mechanisms, it is generally very difficult to engineer a perfectly anisotropic etch profile.

3.5 Deposition Techniques

Thin films can be deposited on the substrate through different material additive techniques. Two families of deposition are of particular importance: Physical Vapour Deposition (PVD) and Chemical Vapour Deposition (CVD). PVD processes are methods in which films are deposited through fluxes of individual neutral or ionic species [50], where as in CVD techniques film deposition occurs through the means of chemical reactions. Some of the PVD techniques are evaporation, sputtering and molecular beam epitaxy, and CVD methods include plasma enhanced CVD, low pressure CVD and atomic layer deposition.

Generally, the process of most PVD techniques can be broken down into three mechanisms [48]:

- Formation of vapour in the target material.

- Transport of the vapour from the source to the substrate.

- Condensation of the vapour on the surface.

3.5.1 Thermal Evaporation

Thermal evaporation is a technique which is based on sublimating the target material (mostly metals) onto the substrate in a vacuum chamber through heating. The process takes place

inside a vacuum chamber as the evaporation point is much lower in vacuum than atmospheric pressure, and also prevents oxidation of the target material. In high vacuum, the collisions between the gas particles and the evaporated material happen less frequently resulting in higher mean free path. The ratio of particles scattered by collision to the atoms of the residual gas (N/N_0) is [48]:

$$\frac{N}{N_0} \propto 1 - e^{\frac{d}{\lambda}}, \tag{3.11}$$

where d is the distance between the source and substrate and λ is the mean free path.

The necessity of performing this process in good vacuum is shown in Table 3.1.

Pressure ($Torr$)	Mean Free Path (cm)	Impingement Rate ($s^{-1}.cm^{-2}$)
10^1	0.5	3.8×10^{18}
10^{-4}	51	3.8×10^{16}
10^{-5}	510	3.8×10^{15}
10^{-7}	5.1×10^4	3.8×10^{13}
10^{-9}	5.1×10^6	3.8×10^{11}

Table 3.1 Kinetic data for air vs pressure [48].

The heating can be done through different methods:

- Resistive heating is a process in which the target material is placed in a crucible (generally made up of a material with a very high evaporation temperature like tungsten) or formed into a filament and current it applied to it (Figure 3.11). This heats up the target, and leads to vapourisation. Since the amount of evaporant is restricted by the crucible or filament size, the thickness that can be deposited is limited.

- In electron beam evaporation, a high intensity electron beam is used to melt and evaporate the target material which is placed in a water-cooled crucible. Using a magnetic field, the electron beam can be deflected accurately. Though the tool is more complex and the process might lead to surface damage, it results in a higher deposition rate as well as better quality films.

- RF induction evaporation is a technique in which a radio frequency coil is used to induce a field, leading to the evaporation of the target material.

- Laser ablation uses a focused laser beam to heat and melt the target.

Evaporation is a widely used technique since it offers a few key advantages like high rate of deposition, simple setup, high levels of purity and minimal surface impact (apart from electron beam evaporation). However, the deposited films might have high levels of tensile stress. Also, the directional nature of deposition leads to difficulty achieving a continuous film over patterned substrates. This can however be a favourable feature for processes like lift-off lithography.
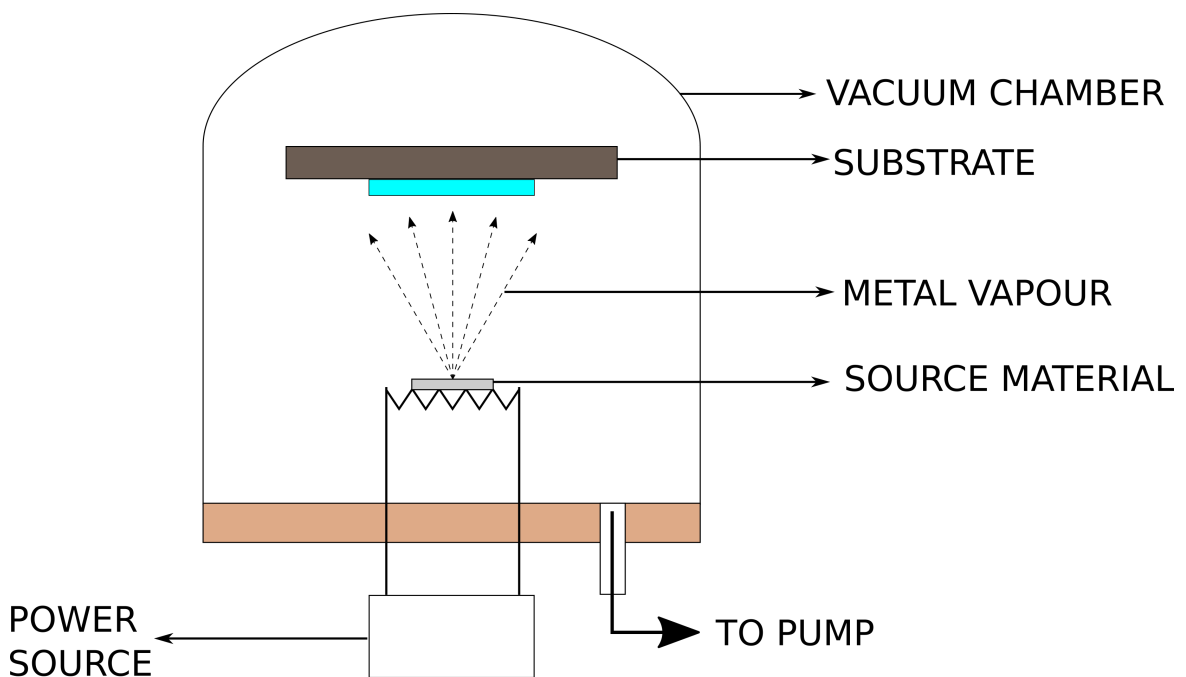
Fig. 3.11 Schematic of a thermal evaporator.

3.5.2   Sputtering

Sputtering is a PVD deposition technique in which the target material is bombarded with high energy particles (generally inert gases like *Ar*) generated in a plasma (Figure 3.13). Since

DC systems do not efficiently work with dielectric materials, RF plasma sputter deposition systems are preferred. The surface particles of the target material (generally negatively charged) are ejected due to kinetic energy provided by the ions, and are deposited onto the substrate.
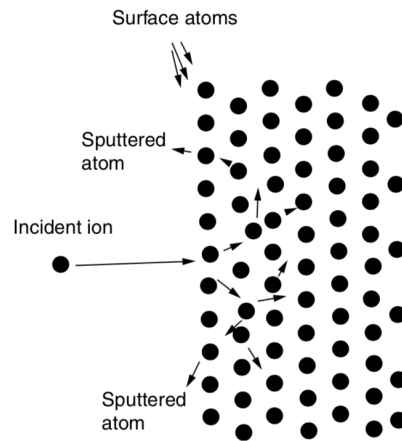
Fig. 3.12 Mechanism of physical sputtering [48].

The incident ion collides with the particles in the lattice structure of the target, leading to a cascade of collisions, and therefore a target particle receives enough energy to overcome the binding energy (Figure 3.12). The amount of material sputtered from the target can be calculated using [48]:

$$W = \frac{kVi}{P_T d},$$
(3.12)

where W is the amount of material, k is the proportionality constant, V is the voltage, i is the discharge current, P_T is the total gas pressure, and d is the distance between the target and substrate.

The deposition rate depends on sputter yield, which is defined as the average number of atoms ejected per ion. The factors affecting sputtering yield are shown in Table 3.2. It is also

Factor		Effect on sputter yield
Target material	Binding energy	Higher binding energy increases yield
	Atomic number	Higher atomic number decreases yield
Sputtering gas	Atomic number	Higher atomic number increases yield
	Incident energy	Higher energy increases yield
Angle of incidence		Yield is maximum at a glancing angle of 20^0 to 30^0

Table 3.2 Dependence of sputtering yield on various factors [48].
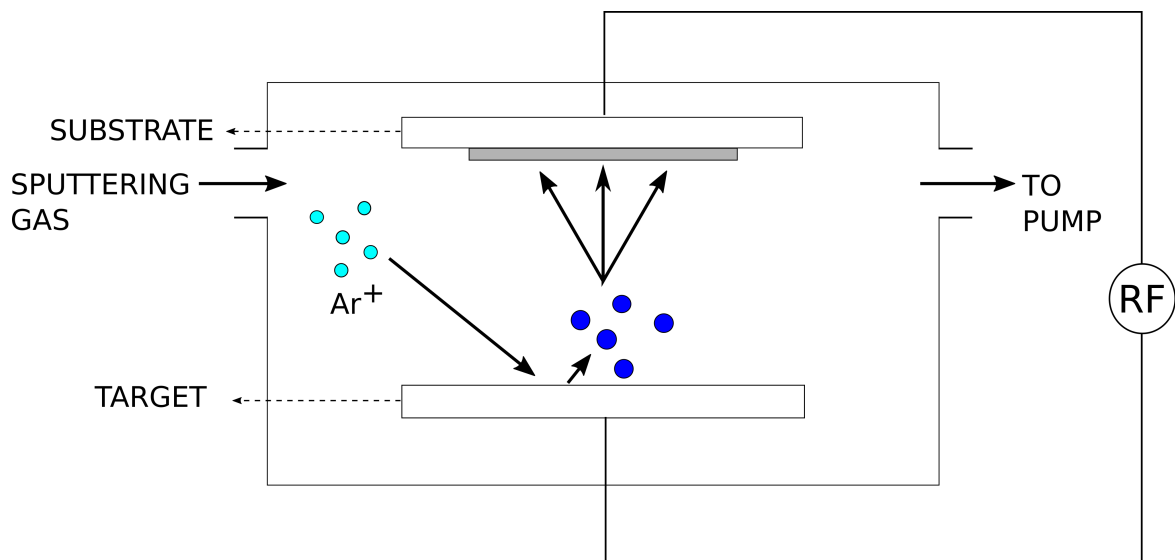
Fig. 3.13 Schematic of a sputter deposition system.

seen from the table that the sputter yield is a function of the angle of ion incidence (Figure 3.14).
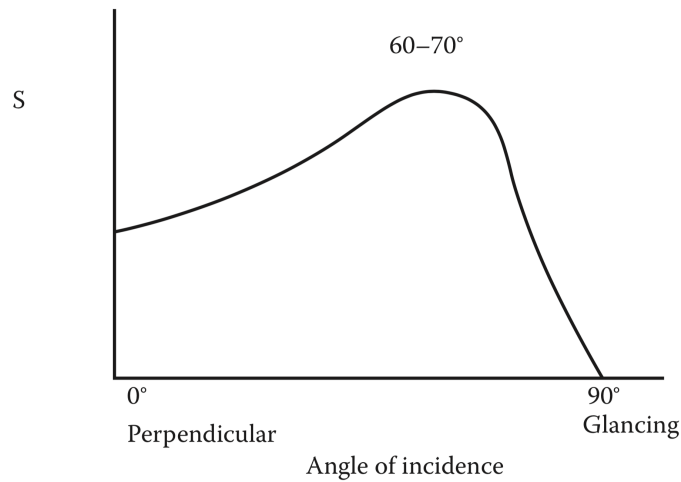
Fig. 3.14 Sputter yield vs angle of incidence [48].

Sputtering is the process of choice for depositing dielectric materials which cannot be evaporated. It also generally provides better adhesion, step coverage and capability of depositing a very wide array of materials including compounds. As with thermal evaporation, the step coverage might be a favourable or unfavourable consequence.

3.6   Metrology and Inspection

In order to ensure that the devices are fabricated as designed, it is important to monitor the results of the fabrication processes constantly. Substrate cleanliness, thin film thicknesses, etch depth, surface roughness and photoresist profile have to be measured to verify that they fall under limits. This is achieved through metrology tools.

The most commonly used metrology method is optical microscopy, which is used to inspect substrate surfaces and thin films for defects, impurities, residues and particles. They can typically resolve features below 1 μm with magnifications ranging from 5 X to 1000 X.

The thickness of thin films can be interrogated using ellipsometry. This technique uses the change in polarization of light after interaction with the films on top of the substrate. If

the optical properties of the film or stack of films are known, the thickness can be determined by fitting the measured readings with existing models of the materials.

Scanning electron microscopy (SEM) is an imaging technique that uses the interaction of electrons with the substrate in order to image it. The surface is bombarded with a beam of electrons, causing an ejection of secondary electrons from the sample. The secondary electron current is recorded, therefore forming an image of the surface. A key advantage of this imaging technique is its ability to resolve extremely small features, often with magnifications up to 300,000 X. However, imaging dielectric materials can be challenging due to the surface electrical charges not dissipating. This can be overcome by coating the surface with a thin metal layer like gold.

The topography of a surface can be mapped through atomic force microscopy (AFM). In this technique, a cantilever with a tip at the end is scanned over the surface, and the deflection of the tip due to its interaction with the surface is measured. This information can be used to form an image of the surface with nanometric precision. Because of its ability to resolve extremely small features, AFM is useful for the measurement of surface roughness. Since AFM is a non destructive technique, it can be used to characterise etch parameters such as etch roughness and etch depth before further processing steps. It also has an advantage over SEM as the substrate material has no effect on AFM. There are a couple of drawbacks that have to be considered before choosing this technique: the scan area is generally limited, and the surface has to be relatively flat.

3.7   Summary and Perspective

In this chapter, a general overview of some of the fabrication fundamentals has been provided. It is important to understand the advantages and limitations of these processes before choosing them for the fabrication of photonic devices. For example, E-beam lithography is preferable for defining photonic waveguides due to its excellent resolution. Also, some of the processes (such as metal deposition) might not be directly employed in the fabrication of these devices, but rather used indirectly (as an etch mask for example). The basic working principle of

the fabrication processes is also important to understand, as changing individual parameters can lead to different results. Finally, the basics of dry etching (along with the introduction of etching concepts such as selectivity) have been discussed before the study of anisotropic (Chapter 4) and isotropic etching (Chapters 5 and 6).

Chapter 4

Anisotropic etching

Developing a reliable anisotropic etching process is essential for the fabrication of photonic structures, such as waveguides. It is also invaluable in the fabrication of small and intricate structures, which are necessary for advanced micromaching [71]. The quality of the etch is crucial during the fabrication of waveguides, as it can lead to increased losses due to roughness introduced from the etching processes [74]. The other important parameters affecting the operation of waveguides are the etch rate and anisotropy.

A rib waveguide structure was simulated in COMSOL with a rib width of 280 nm, rib height of 260 nm and etch depth of 100 nm. The structure is represented in Fig 4.1a, and has an effective index of 2.6263 at 1550 nm. If the etch rate is slower than expected, the etch depth will be lower, and is presented in Fig 4.1b with an etch depth of 50 nm. This changes the mode shape and increases the effective index to 2.8225. If the etch rate is faster than anticipated, the etch depth will be higher as shown in Fig 4.1c. The mode shape is again affected, and the effective index decreases to 2.3579. The degree of anisotropy also changes the behavior of the waveguide. A waveguide with a positively sloped sidewalls is shown in Fig 4.1d, and the effect of the non-anisotropy of the etch is immediately evident in the mode shape. The effective index also increases slightly, to 2.6694. Therefore, it is highly desirable to engineer an etching process that is repeatable and resulting in smooth and vertical etches.

(a) Designed structure

(b) Slower etch rate

(c) Faster etch rate

(d) Sloped sidewalls
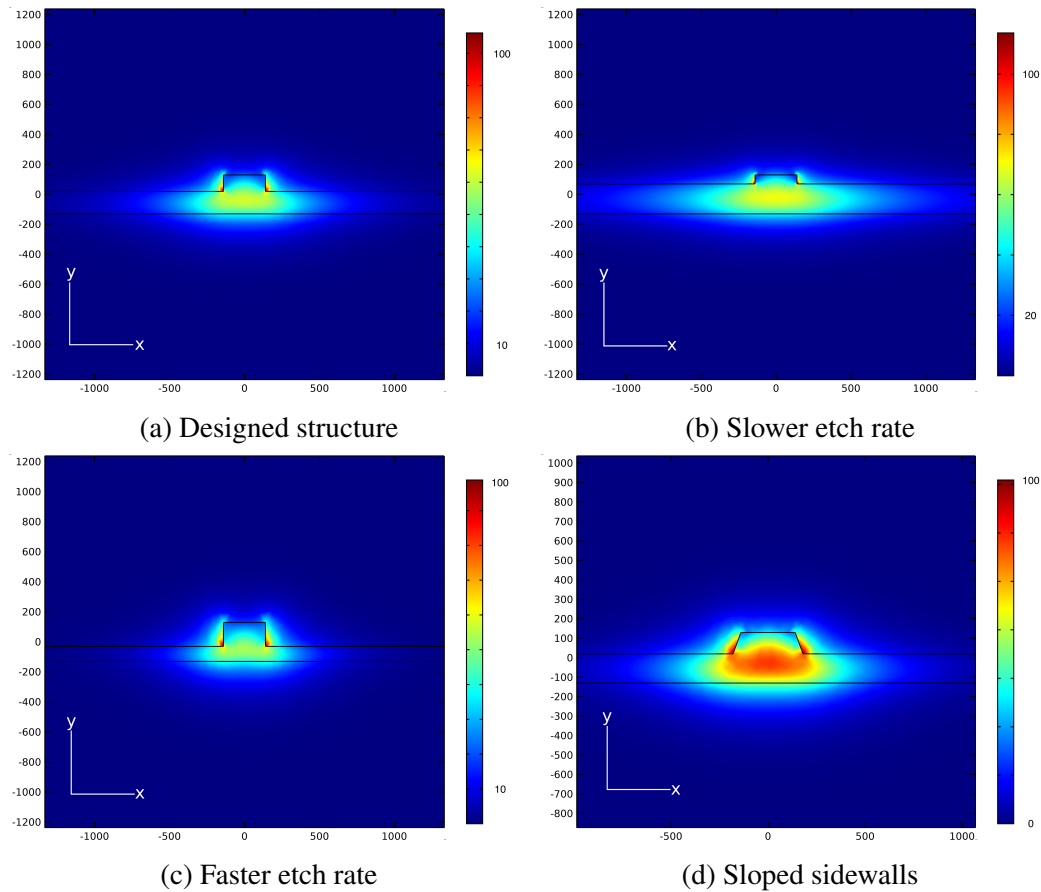
Fig. 4.1 Difference in mode shape due to undesirable etch characteristics. The sidewall profile, the etch depth and the waveguide width all have significant effects on the mode profile as well as the effective refractive index. The intensity bar depicts the normalised E-field intensity norm (V/m).

Dry etching is a widely used technique in achieving these etches as it offers a great deal of flexibility over the anisotropy, etch rate and the roughness. Dry etching also generally tends to be a cleaner process and offers better compatibility with other vacuum processes [71].

As with wet etching, the chemistry and the etching process parameters play a very important role in the quality of the etch. The choice of the etchants depends on the material that is to be etched. Anisotropic etching has been widely studied for commonly used optical materials, and waveguides fabricated using silicon nitride [75], diamond [76][77] and polymers [78] have been demonstrated. In this chapter, anisotropic etching of these materials will be studied and experimental findings reported.

4.1   Etch Mechanisms

As mentioned in the earlier chapter, anisotropy in the context of dry etching is different than with wet etching, as it is not related to the crystal orientation. Instead, it is defined using the angle of the etched sidewalls, with complete anisotropy implying perfectly vertical walls, and isotropy corresponding to rounded off sidewalls due to equal vertical and horizontal etching. In general, anisotropic dry etching is caused due to the directional ions accelerated in the etch chamber towards the substrate. There are two types of such etching mechanisms [71]:

1. Ion-induced RIE: This refers to the mechanism where the etching of the substrate does not occur spontaneously. Instead, the etching occurs due to the modification of the substrate surface caused by the ions, enabling the chemical reaction with the radicals. The polymer etch in an oxygen plasma is an example of this mechanism.

2. Ion-inhibitor RIE: In this technique, the substrate is etched spontaneously in the etchant, therefore requiring the deposition of a protective barrier layer to stop the sidewalls from being attacked [79]. Due to the directionality of the incident ions, the inhibiting layer of the sidewalls are not exposed to the bombardment. However, the layer covering the horizontal surfaces of the substrate are physically etched by the ions, exposing them to the etchant, and therefore achieving anisotropy. The inhibiting layer that

is deposited is very thin, enabling the etching to occur even at lower energy levels. This has the additional advantage of increasing the selectivity of the etch as well as decreasing the surface damage [71]. Anisotropic etching of silicon can be performed using this technique, for example using etch gases that react with silicon to form silicon oxyhalogens (which forms the etch barrier layer). Another example of this etch mechanism is the cryogenic etching of silicon.

4.2   Etch Tools

All the anisotropic etches reported in this chapter were performed in the PlasmaPod RIE system manufactured by JLS Designs Limited, United Kingdom. It is a table top system, with an aluminium chamber roughly 5 litres in volume. The aluminium electrode is 125 mm in diameter and is water cooled (connected to an external chiller with temperature control). Both the chamber and the electrodes are hard anodized to prevent corrosion. The RF generator powering the system operates at the industry standard frequency of 13.56 MHz, with a maximum power of 300 Watts. The chamber pressure is measured through a capacitance manometer gauge, with a maximum error of 0.25% of the reading value. The system has input for 3 mass flow controlled gas lines with isolation valves, along with a separate line for the nitrogen vent gas. The chamber is connected to a vacuum pump, with a pneumatically controlled isolation valve in between them. Apart from the valve, the chamber lid is also controlled pneumatically, with both connected to a compressed air line operating at 80 psi.

Due to the size of the chamber and pumping limitations, published recipes for other systems often cannot be used. Therefore, developing a recipe suitable for the system becomes necessary. The material of the chamber and electrode have a considerable effect on the characteristics of the etch. Hence, considerations have to be made regarding the etch chemistry. Since the chamber and electrode of our system are constructed using aluminium, it presents a unique set of issues [79]:

- Consumption of Cl atoms due to the aluminium surface, therefore resulting in depletion of the reactant.

- Increase in F atom density.

- Formation of non-volatile AlF_3 particles due to SF_x^+ ions sputtering the Al surface.

4.3   Reactor Preparation

The condition of the etching chamber might affect the etching characteristics drastically. Therefore, it is important to prepare the chamber such that the results can be repeatable. Generally, the surface of the electrode must be cleaned in between runs using isopropanol to remove any particles or remnants of vacuum grease. The surface of the chamber changes during the course of an etch due to the formation of polymer films. In order to make the process repeatable, the chamber can be initially cleaned through oxygen plasma to remove these films. Following this, the necessary etch recipe is run, without a substrate present, in order to "condition" the chamber. The conditioning process coats the walls of the chamber and ensures that the radicals get consumed at the same rate during repeated runs of etches. Another issue is the presence of water vapour in the chamber, which can alter the etch chemistry and the result [71]. This generally occurs when the chamber is exposed to the air during the loading and unloading of substrates. It can be mitigated by the use of load locks. When that is not possible, the duration that the chamber is opened should be minimized. Finally, nitrogen and oxygen molecules can be introduced into the chamber via leaks in the gas seals and gas lines. Flooding the chamber with the etch gas mixture for a set duration before igniting the plasma helps to pump out these molecules out of the chamber.

4.4   Anisotropic Silicon Etching

Due to its widespread use in the semiconductor and photonic industry, the anisotropic etching of silicon has been thoroughly studied. High aspect ratio and anisotropy are particularly important during the etch. Commercially, gases containing bromine and chlorine are used for the anisotropic etch [80]. However, owing to their corrosive and toxic nature, fluorinated gases such as SF_6 are being used increasingly. Since etching in a pure SF_6 plasma results in

an isotropic etch profile, addition of other gases resulting in anisotropic etch mixtures (eg. $CHF_3 : SF_6 : O_2$) are used [72].

An alternative method to change the nature of the SF_6 etch is a process known as cryogenic etching. In this method, O_2 is added to SF_6 as a catalyst for passivation [81]. At temperatures below $-85°C$, a thin layer of SiO_xF_y is created [82], and this layer acts as an etch barrier on the sidewalls, leading to anisotropy. The SiO_xF_y layer evaporates when the reactor is brought back to room temperature, leading to a clean and smooth etch.

In the two processes mentioned above, the etching and creation of the passivation layer occur simultaneously. It is also possible to achieve anisotropy through consecutive steps of isotropic etching and passivation [83][84]. This process is known as the Bosch process, and is performed in an ICP-RIE reactor. In the etch step, a low pressure SF_6 plasma is generated, leading to the fluorine radicals in the plasma reacting with the silicon substrate to form SiF (which is volatile). In the passivation step, C_4F_8 molecules react to form a protective layer of polymer in the etched trench. The ions in the subsequent etch step remove the layer from the horizontal surface of the trench due to the physical aspect of the etch. The degree of anisotropy can be changed by altering the ratio of etch vs. passivation. This cycle can be repeated for the necessary number of times to achieve the required etch depth. One drawback of the Bosch process is the formation of "scalloped" sidewalls, which is caused by the isotropic nature of each etch step.

Both the cryogenic silicon etch and the Bosch etch require specialized equipment, especially the former, since temperature control of the substrate is essential. Anisotropic etching in the fluorine based gas mixtures alleviates these issues, since the etch can be performed in a standard RIE system, and, since the etch and passivation occurs concurrently, scallops are not formed on the sidewalls.

4.4.1 Purpose of Etch Gases

A fluorine based process was chosen for the silicon anisotropic etch in our case. As mentioned above, a widely used gas mixture for this etch is a combination of CHF_3, SF_6 and O_2.
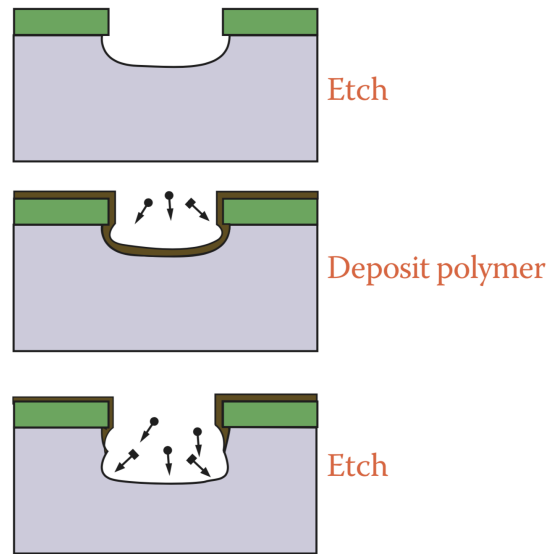
Fig. 4.2 A schematic depicting the etching principle of the Bosch process.

Different ratios of these gases yields different results, as each of these gases serves a different purpose.

1. SF_6: Of the many commercially used etchants, SF_6 is a gas that is particularly fluorine-rich. The fluorine atoms are very reactive towards silicon [54], forming SiF_4. Fluorine-based plasma reacts with silicon spontaneously, and does not require ion bombardment [48]. The reaction rate with crystalline silicon is given by the following equation [85][86]:

$$Rate(/min) = 2.9 \times 10^{12} T^{\frac{1}{2}} N_F e^{\frac{-E_F}{RT}}, \qquad (4.1)$$

where T is the substrate temperature in Kelvin, N_F is the F-atom density, R is the gas constant and E_F is the activation energy. Molecular fluorine is not a suitable silicon etchant as it is hazardous and leads to surface roughness [54].

2. O_2 : The addition of oxygen to SF_6 makes the etch anisotropic in nature [87], due to the formation of the passivating layer of $Si_xO_yF_z$ [71]. However, this mixture also gives rise to rough surfaces and forms "Black silicon" (further discussed in the next section)

[72]. Due to polymers being readily attacked in oxygen plasma, the etch selectivity can also be affected.

3. CHF_3: This is a widely used etchant for both silicon nitride and silicon dioxide. It is a source of both fluorine and carbon atoms, and the etch is ionic in nature [2]. Adding CHF_3 to a $SF_6 : O_2$ plasma removes the passivating layer from the horizontal surface through ion bombardment, and forms CO_xF_y or SO_xF_y [71]. The amount of CHF_3 in the mixture is a crucial parameter as it often determines the quality of the etch. If the flow rate is too low, the surface roughness remains high. On the other hand, if the flow rate it too high, the degree of anisotropy is affected.

The overall etch characteristics is a function of the gas flow rates, RF power and chamber pressure. Once the quality of the etch is satisfactory, the etch time can be determined from the etch rate obtained and the etch depth required. In the JLS PlasmaPod system, the flow rates have to constrained due to the chamber size, the maximum flow rate and the chamber pressure. The maximum values for the flow rate of SF_6 is 26 sccm, CHF_3 is 50 sccm and O_2 is 99 sccm. However, it is not possible to maintain low chamber operational pressure (< 30 mT) at higher gas flow rates due to the pumping limitations.

4.4.2   Black Silicon Method

Due to the many process variables involved in the anisotropic etch (such as individual flow rates, gas mix ratio, chamber pressure, substrate temperature and RF power), it is extremely challenging to arrive at an optimal recipe by just varying all the process parameters. A method known as the "Black Silicon Method" has been proposed by Jansen et. al. [79] in order to simplify the process of "engineering" the anisotropic etch.

This method uses the formation of micro-grass on the substrate surface in order to find the etching parameters that yield a smooth and vertical etch profile. In the etch chemistry we have used, the ratio between the etching fluorine radicals and passivating oxygen radicals is crucial. At a particular ratio, a balance is achieved between the etching and passivation mechanisms, resulting in anisotropy. At this moment, particles such as native oxide and

dust act as micromasks. Due to the anisotropic nature of the etch, these particles give rise to spikes which are covered by a SO_xF_y layer [79]. When etched for longer durations, the spikes get longer, eventually exceeding the wavelength of light. This is the reason the entire surface of the substrate turns black, and is termed as "Black Silicon".

This process is carried out in three steps [88]:

1. A piece of silicon is placed in the etching chamber and the power and pressure are adjusted according to the tool and process preference for a stable SF_6/O_2 plasma. Roughly 1 μm of silicon is etched, and the surface is inspected to check for black silicon. If the surface is not black, the process is repeated with increased oxygen flow. This sequence is continued until the surface is black. Care has to be taken not too increase the oxygen flow beyond requirement, as this results in a positively tapered profile.

2. Once the silicon surface turns black, a small quantity of CHF_3 is introduced to the gas mixture, and the etching repeated. The substrate is once again inspected to check the nature of the surface. This process is repeated by increasing the CHF_3 flow until the surface is clean and devoid of black silicon. The increase of the CHF_3 flow rate must also be performed slowly, as excess CHF_3 leads to isotropic profiles due to the CF_x species scavenging the oxygen radicals.

3. The patterned substrate is now etched using the established recipe. The etched profile is checked for anisotropy, and small adjustments made if necessary. A more isotropic profile can be obtained by increasing the SF_6 content. The angle of the profile can also be manipulated, with oxygen making the profile positively sloped, and CHF_3 making it negatively sloped. Increase in pressure or decrease in power will result in more positively sloped tapers.

It is important to keep the surface temperature stable ($< 20°C$) and the chamber condition constant during the process.

Since our devices were designed to be fabricated chip-scale, the above process had to be modified slightly. The piece of silicon used for step 1 was chosen to be 1 $cm \times$ 1 cm.

Larger substrate surfaces did not result in black silicon due to insufficient flow rates. Once the optimal etching recipe was established for the chip, the recipe had to be modified further. Since this would be the anisotropic etch recipe of choice for silicon, it had to be designed to overcome the issues of loading. Introducing a 4" silicon wafer as a carrier would increase the etchable area, reducing the loading effect by consuming more of the reactants. Once a suitable etching recipe which resulted in anisotropic profiles was found for the $1\ cm \times 1\ cm$ chip, the parameters were tweaked until the same results were obtained with the wafer present.

4.4.3   Experimental

The primary application of the anisotropic etches being studied is in the fabrication of waveguides. As explained earlier, the important parameters being degree of anisotropy and sidewall roughness. The etch depth for single mode silicon waveguides is generally in the range of a few hundred nanometers (< 600) for both rib waveguides and strip waveguides. Therefore, the etch depth was targeted to be in that range. Longer etches can sometimes be beneficial to characterise the etch quality, as the roughness and etch profiles will be more pronounced. During these longer etches, mask resilience and selectivity become very important.

Sample Preparation

As mentioned in the earlier section, the aim of this experiment is to determine an optimal RIE recipe for chip-scale silicon etching. Therefore, there are a few design details that have to be considered. In order to alleviate the effect of loading, all the etches would be designed considering a 4" silicon wafer carrier. All the chips were diced from bare silicon wafers from the same batch, following which, they were cleaned using the standard degrease process detailed in Chapter 3. This eliminates most particles and organic residue from the surface that might affect the etch quality. This was followed by a dip in HF in order to remove any native oxide from the surface.

Mask Selection

It is generally preferable that the mask material chosen has very little or no influence on the plasma chemistry, and therefore the etch result [88]. This is not entirely possible in practise, as intricate patterns have to be defined through e-beam lithography using e-beam resists. Most resists are affected in oxygen and fluorine based plasmas. Therefore, the mask selectivity and other factors such as loading have to be given consideration. Another property that has to be considered is mask conductivity. Insulating masks might be negatively charged due to charge accumulation, therefore resulting in strong local fields which in turn deflect the incoming directional ions. This effect is known as "Ion Bowing" and causes undercuts below the mask [89][90].

Initially, we used different photoresists as etch masks (AZ 1505 positive resist and AZ nLOF-2020 negative resist). This process had the problem of mask erosion on the edges, therefore transferring the profile to the silicon layer (Fig 4.3). An alternate method is using a metal mask (eg. chromium) deposited using thermal evaporation or sputtering and patterned through lift-off lithography or metal etching. Metal masks generally have excellent selectivity and can be used to achieve deep trenches. However, the process of patterning the metal layer introduces edge roughness. This makes the qualitative analysis of the etch quality difficult. Therefore, once the initial recipe was determined, further etches were performed with MaN-2403, patterned through e-beam lithography as the mask material. Series of lines of width 800 nm, length 200 μm and thickness 300 nm were used for this experiment. As seen in Fig 4.4, the sidewall profile and smoothness ensures that the etch profile obtained is due to the etching process, and not transferred via lithography. Also, this choice of mask material is beneficial, as it replicates the mask and etch behavior during waveguide etching.

SF_6 (*sccm*)	O_2 (*sccm*)	RF Power (*W*)	Pressure (*mTorr*)	Time (*min*)
14	10	100	50	5

Table 4.1 Black silicon initial parameters
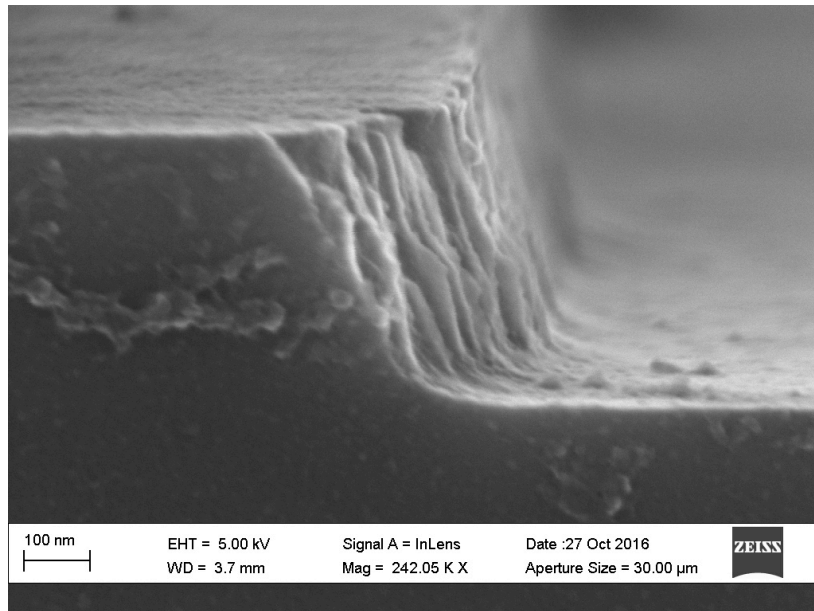
(a) Resist edge slope and roughness.
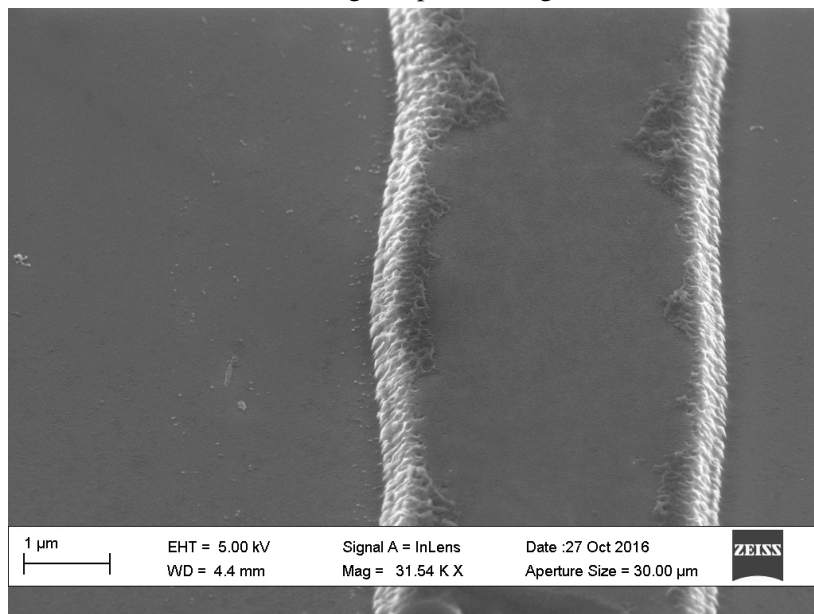
(b) Etch profile due to mask erosion.

Fig. 4.3 Photoresist masks for etch characterisation. The edge roughness of the mask can be seen.
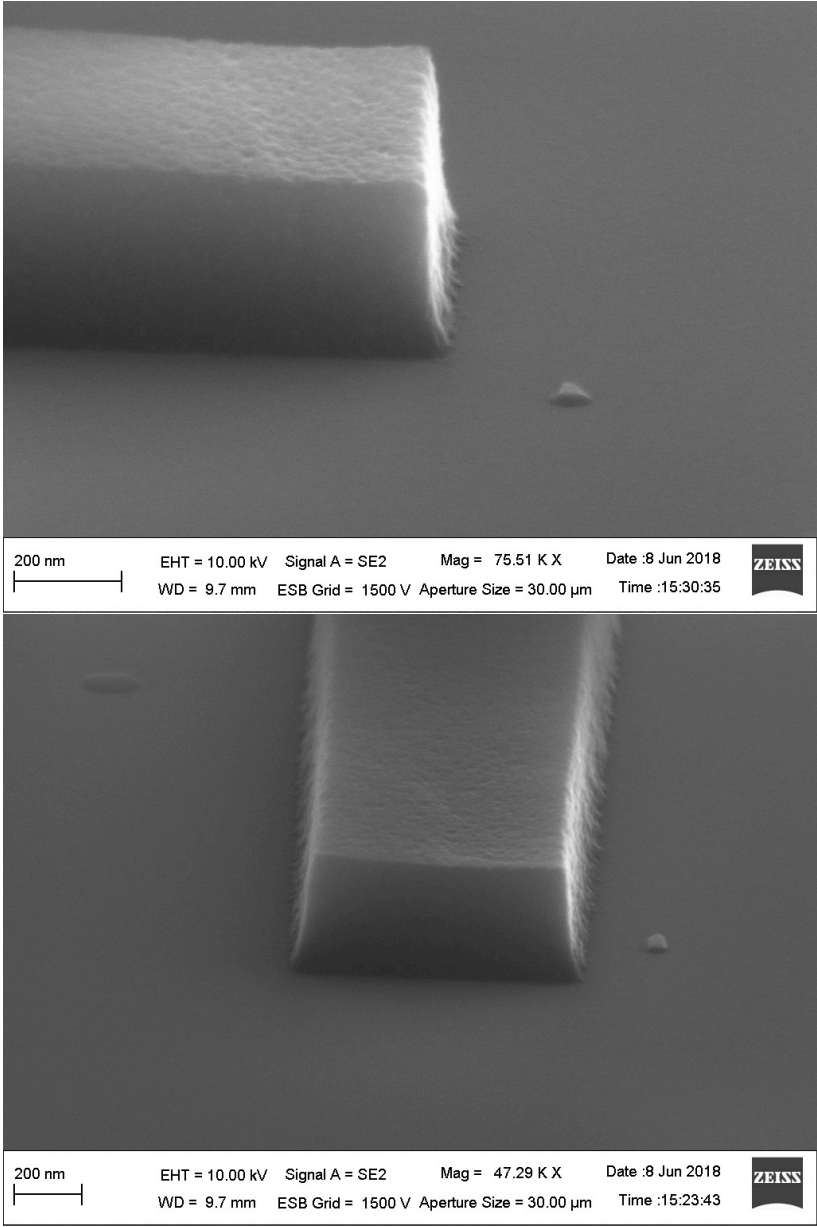
Fig. 4.4 MaN E-beam resist profile. The well defined edges as well as the smoothness makes this an ideal mask choice for etch characterisation.

Formation of Black Silicon

Initially, a silicon sample patterned with a series of lines was etched for 2 minutes to determine the approximate etch rate, which was found to be around 200 nm/min. Following this, an unpatterned piece of 1 $cm \times$ 1 cm silicon was placed on a 4" silicon wafer in order to form black silicon. The initial etch parameters values were chosen such that all of them could be reduced or increased later.

SF_6 (sccm)	O_2 (sccm)	RF Power (W)	Pressure ($mTorr$)	Time (min)
14	2	100	50	5

Table 4.2 Black silicon recipe
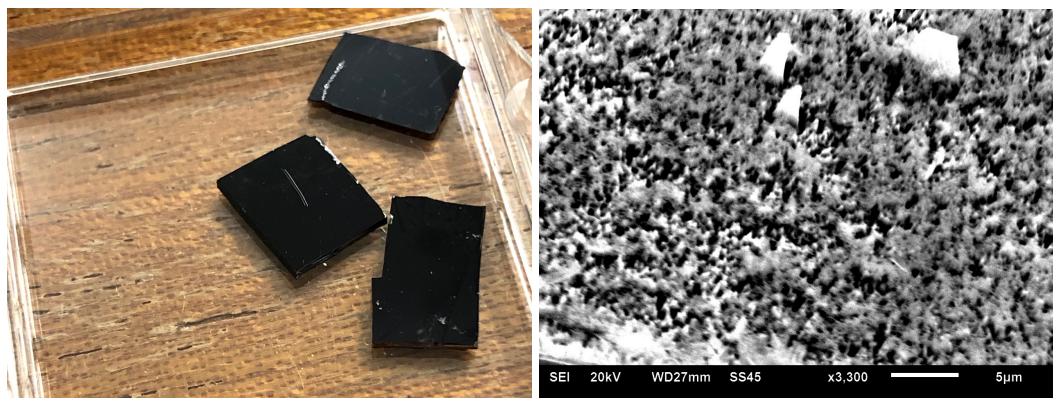
(a) Optical Microscope image of black silicon.   (b) SEM image of black silicon.

Fig. 4.5 Formation of black silicon.

The colour of the chip after the etch was pale blue. The flow rate then was adjusted to the maximum value in order to obtain black silicon, but without success (Table 4.1). The chip finally turned black by removing the silicon carrier wafer (reducing the loading effect) (Fig 4.5), and slowly reducing the oxygen flow rate.

CHF_3 was slowly added to the recipe presented in Table 4.2 until the black silicon completely disappeared, and the chip appeared smooth visually (Table 4.3).

SF_6 (*sccm*)	O_2 (*sccm*)	CHF_3 (*sccm*)	RF Power (*W*)	Pressure (*mTorr*)	Time (*min*)
14	2	6	100	50	5

Table 4.3 Black silicon method - smooth surface

Modification of the recipe

Once the etch recipe that yields black silicon was found, a silicon chip patterned with thermally evaporated chromium was used to determine its anisotropicity. CHF_3 was slowly introduced in the mixture in order to etch the passivating layer from the horizontal surfaces. Fig 4.6a had a CHF_3 flow rate of 2 sccm and Fig 4.6b was etched with a flow rate of 5 sccm. The decrease in the amount of the passivating film can be noticed, and the difference was evident through naked eye inspection as well. A smooth surface with vertical sidewalls (Fig 4.7) was obtained using the recipe presented in Table 4.3.

Recipe	SF_6 (*sccm*)	O_2 (*sccm*)	CHF_3 (*sccm*)	RF (*W*)	Pressure (*mT*)	Time (*s*)
1	18	2	2	100	30	60
2	18	2	4	100	30	60
3	18	2	6	100	30	60
4	18	4	2	100	30	60
5	18	4	4	100	30	60
6	18	4	6	100	30	60
7	18	6	2	100	30	60
8	18	6	6	100	30	60

Table 4.4 Black silicon method - Varying flow rates

Though the above etch recipe results are favourable, it had to be further studied and modified if required, as this was performed without the presence of a silicon carrier wafer. The wafer would consume the reactants at a faster rate, therefore changing the balance between the gas flow rates. At this stage of the experiment, the samples used were patterned with MaN-2403. In order to compensate for the increased consumption of the fluorine radicals by the added silicon area, increased SF_6 flow rates were tried, and the optimal value
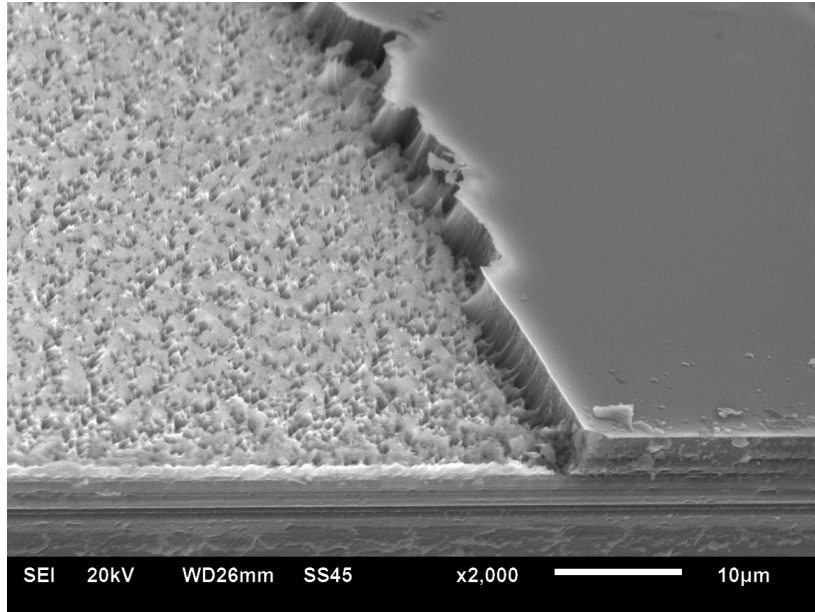
(a) $CHF_3 = 2sccm$.
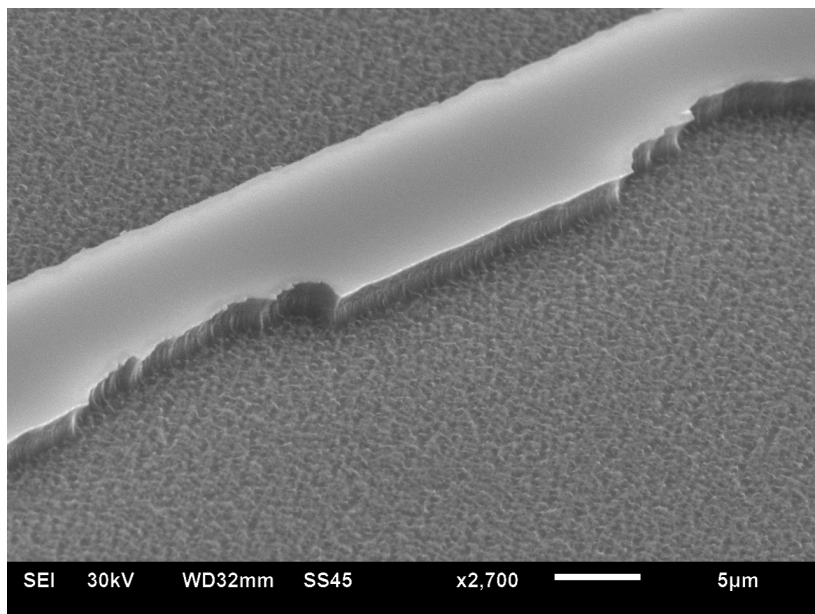
(b) $CHF_3 = 5sccm$.

Fig. 4.6 Addition of CHF_3 to black silicon.
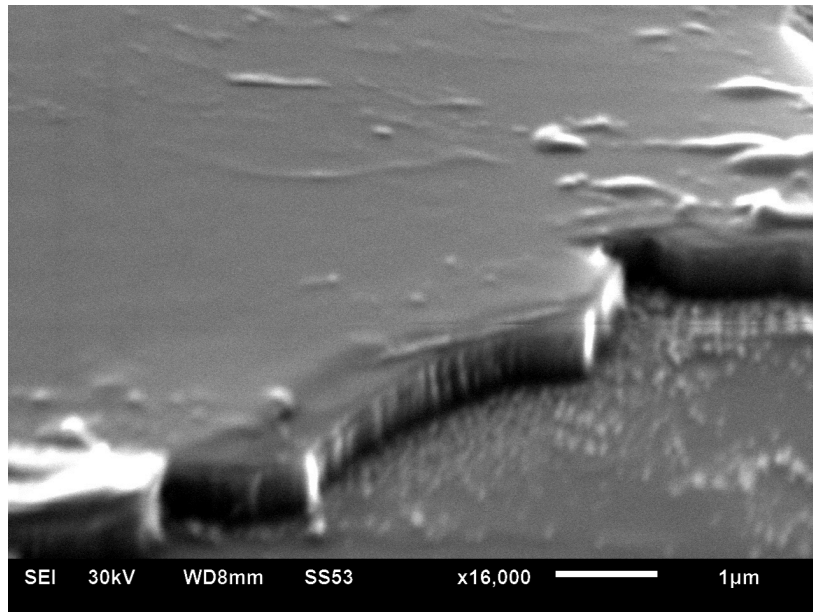
Fig. 4.7 Optimal etch recipe without silicon carrier wafer.

was found to be 18 sccm. Using this as a starting point, the other parameters were varied as shown below in Table 4.4.

Recipe	SF_6 (*sccm*)	O_2 (*sccm*)	CHF_3 (*sccm*)	RF (*W*)	Pressure (*mT*)	Time (*s*)
9	18	4	2	100	60	60
10	18	4	2	100	90	60
11	18	4	2	200	30	30
12	18	4	2	100	60	30
13	18	4	2	200	90	30

Table 4.5 Black silicon method - Varying pressure and power

The etch results of the recipes can be seen in Figure 4.8. The recipe with the best etch profile (Recipe 4, Figure 4.8d) was chosen, and the power and pressure was varied. The etch times for the recipes with increased pressure was reduced to 30 seconds to ensure that the mask survives the etch. The results are presented in Table 4.5.

(a) Recipe 1.

(b) Recipe 2.

(c) Recipe 3.

(d) Recipe 4.

(e) Recipe 5.

(f) Recipe 6.

(g) Recipe 7.

(h) Recipe 8.
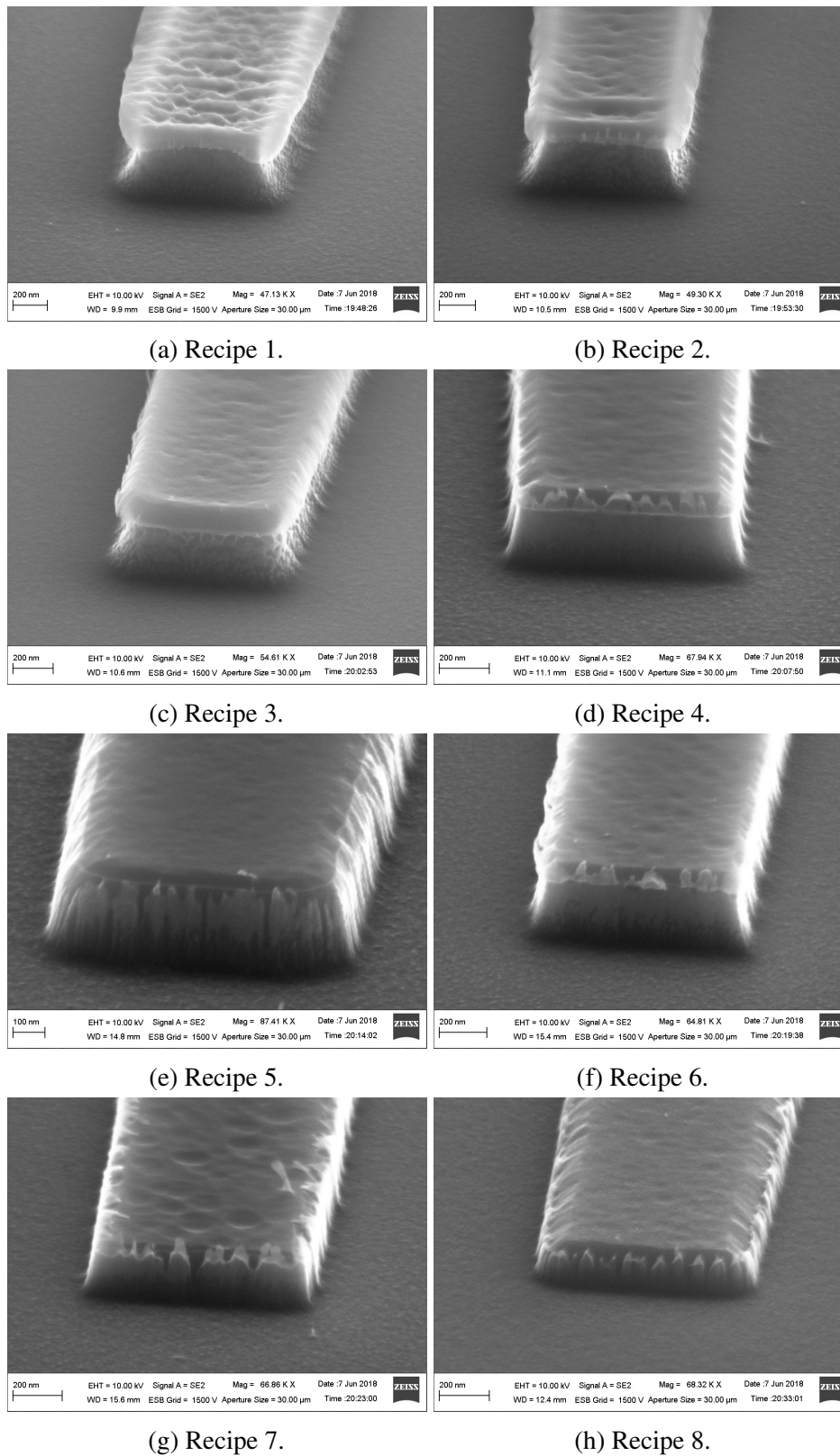
Fig. 4.8 Etch profiles obtained using the black silicon method (with silicon carrier wafer). The effect of CHF_3 addition on the sidewall profile can be seen. The effect of increased O_2 on the mask degradation is also clearly evident.

(a) Recipe 14.

(b) Recipe 15.

(c) Recipe 16.

(d) Recipe 17.

(e) Recipe 18.
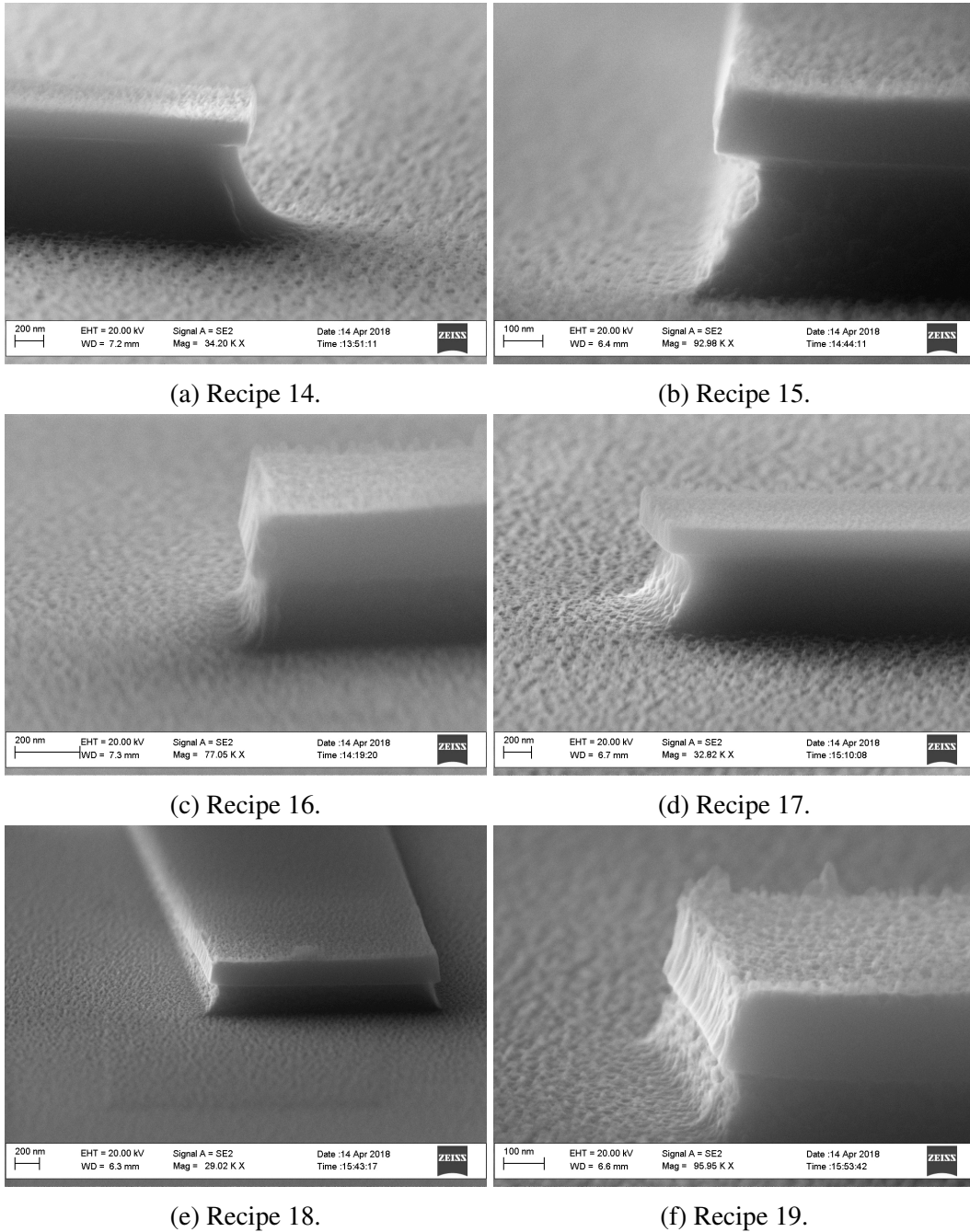
(f) Recipe 19.

Fig. 4.9 Etch profiles obtained without O_2 (without silicon carrier wafer). The effect of increased CHF_3 on the sidewall profile can be seen. The best results were obtained with the highest value of CHF_3 (Recipe 16 and 19).

Etching with other mixtures
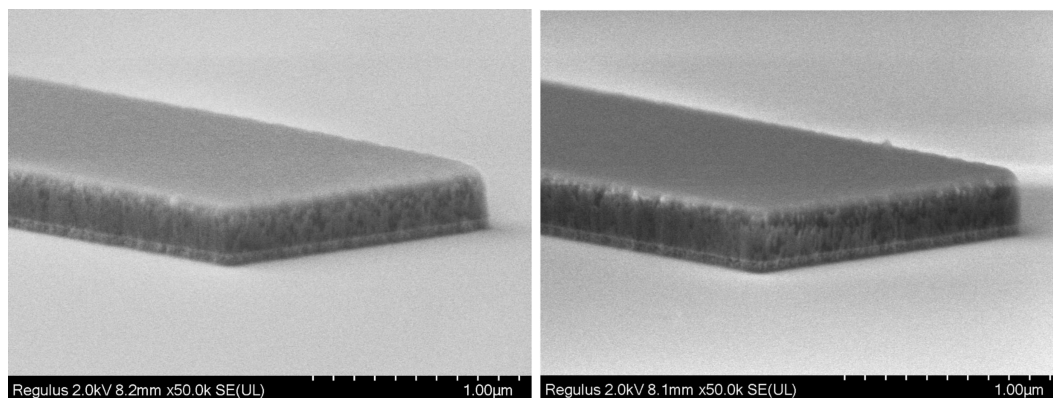
(a) Recipe 16.

(b) Recipe 19.

Fig. 4.10 Etch profiles obtained without O_2 (with silicon carrier wafer).
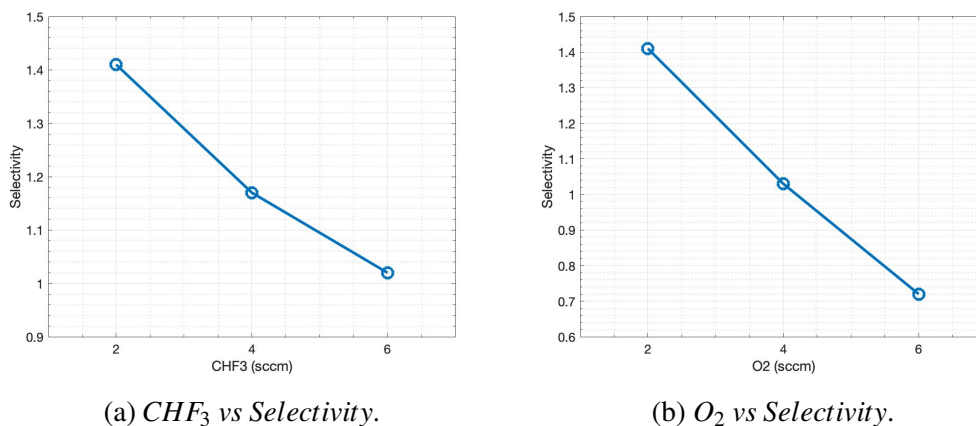
(a) *CHF$_3$ vs Selectivity*.

(b) *O_2 vs Selectivity*.

Fig. 4.11 The effect of gas flow rates on selectivity (black silicon method).

Since mask selectivity plays a very important role in the choice of recipe, alternate etch chemistries have to be considered. Anisotropic etching of silicon has been reported using both $SF_6 : O_2$ [91][92] and $SF_6 : CHF_3$ [93] gas mixtures. The former method results in excellent etch control, profile and offers very high selectivity to SiO_2. However, performing an etch using a photoresist mask is challenging due to the high amounts of fluorine as well as oxygen radicals in the plasma. This would attack the photoresist, therefore reducing

the selectivity. In this section, the $SF_6 : CHF_3$ gas mixture as an anisotropic etch process was investigated. As this recipe does not contain oxygen, the resilience of a resist mask is expected to be better than the $SF_6 : O_2$ mixture. The CHF_3 and SF_6 flow rates were varied with the power and pressure kept constant, in order to determine the effect of the gas ratio. The recipes are presented in Table 4.6, and the profiles can be seen in Figure 4.9. All the recipes were initially performed without a silicon carrier wafer in order to qualitatively assess the etch. The etching time was kept low in order to minimize the amount of resist removed during the etch.

Recipe	SF_6 (*sccm*)	CHF_3 (*sccm*)	RF (*W*)	Pressure (*mT*)	Time (*s*)
14	5	2	100	30	30
15	5	10	100	30	30
16	5	18	100	30	30
17	10	2	100	30	30
18	10	10	100	30	30
19	10	18	100	30	30

Table 4.6 Etching recipes without oxygen
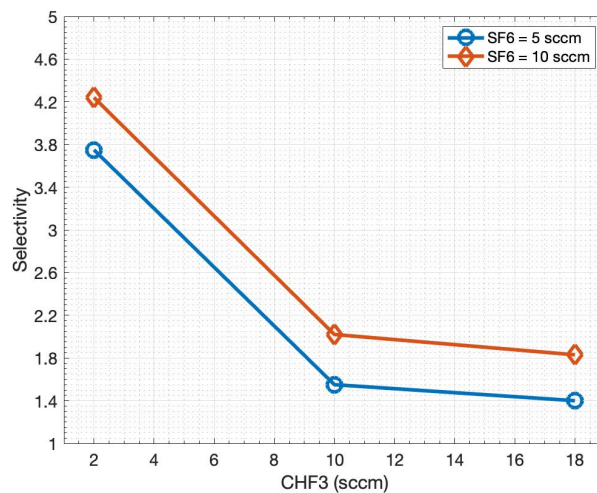
Fig. 4.12 The effect of CHF_3 flow rate on selectivity (No O_2).

The etches were then repeated in the presence of a 4" silicon wafer, and the results analysed.

4.4.4 Results and Discussion
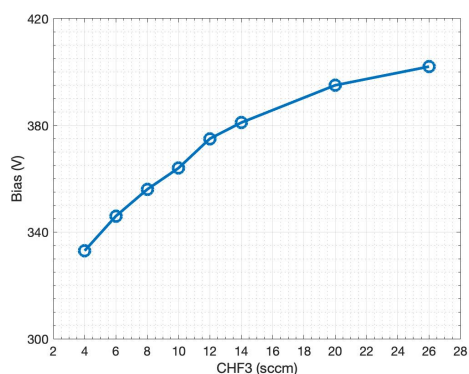
(a) *CHF$_3$ vs Bias*.
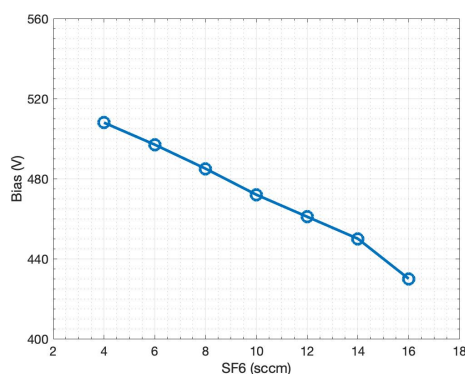
(b) *SF$_6$ vs Bias*.
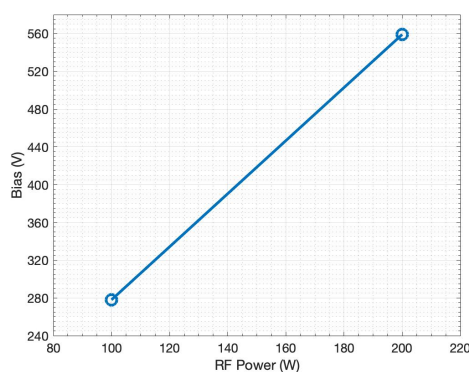
(c) *Power vs Bias*.
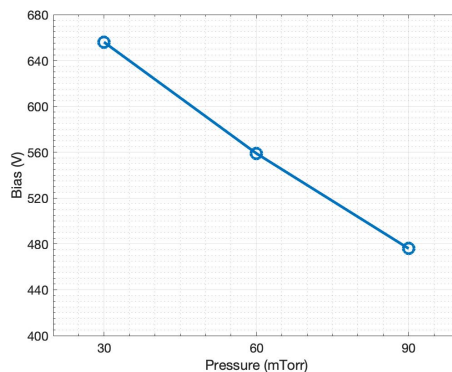
(d) *Pressure vs Bias*.

Fig. 4.13 The effect of etch parameters on Bias voltage.

The effect of the individual gases on the self bias, etch rate and selectivity can be qualitatively analysed. We have quantified selectivity using the equation presented in the previous chapter. Though the etch profile can also be analysed through parameters such as the degree of anisotropy, it can easily be investigated visually, thereby avoiding any measurement artifacts. SF_6 was usually unaltered once a suitable flow rate was found, as it is the main etching gas and the flow rates of the other gases can be varied to change the gas mixture ratio.

Recipe	Selectivity	Profile
1	1.41	Slightly isotropic
2	1.17	Slightly isotropic
3	1.02	Tapered sidewalls
4	1.03	Fairly vertical
5	1.01	Tapered
6	0.98	Tapered
7	0.72	Tapered
8	0.62	Tapered

Table 4.7 Black silicon method - selectivity and profile

The etch rate was found to be inversely related to the CHF_3 flow (Fig 4.14a). It was also found to affect the selectivity adversely (Fig 4.11a). Since CHF_3 is ionic in nature, increase in the CHF_3 flow rate corresponds to an increase in the bias voltage as well (Fig 4.13a). The addition of O_2 was found to decrease both the selectivity as well as the etch rate (Fig 4.11b and Fig 4.14b). The decrease in selectivity is due to the fact that O_2 is known to aggressively attack photoresists and other polymers.
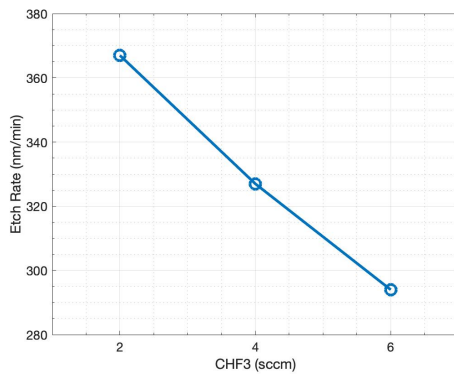
(a) CHF_3 vs Etch rate
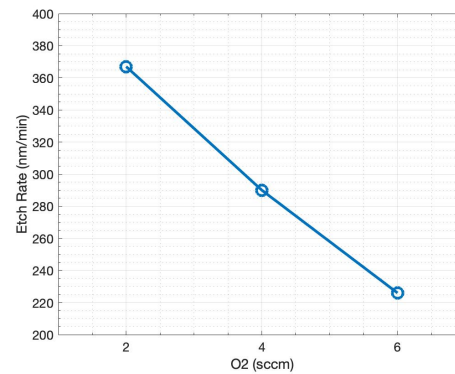
(b) O_2 vs Etch rate

Fig. 4.14 The effect of gas flow rates on etch rate (black silicon method).

As mentioned earlier, the selectivity and the etch profile are the parameters of interest in the study along with the etch roughness. Table 4.7 presents the results from the experiments performed.

The recipes with the increased RF power were deemed not suitable due to very low selectivity. Increased pressure led to more isotropic and negatively sloped profiles. Recipe 4 presents the best anisotropic recipe due to its selectivity, etch profile and roughness. It can be used to etch waveguides using an E-beam or photomask of reasonable thickness.

The results of the study conducted without O_2 is presented in Table 4.8. As with the other study, the addition of CHF_3 reduces the selectivity considerably (Fig 4.12).

When the etches were repeated with the silicon wafer presented, Recipe 16 and Recipe 19 yielded the best profiles (Figure 4.10). However, the selectivity was reduced greatly (Recipe 16 = 0.46, Recipe 19 = 0.57).

Recipe	Selectivity	Profile
14	3.75	Isotropic
15	1.55	Tapered
16	1.40	Fairly vertical
17	4.24	Isotropic
18	2.02	Tapered
19	1.83	Fairly Vertical

Table 4.8 Etching without oxygen - selectivity and profile

4.5   Anisotropic Silicon Nitride Etching

Silicon nitride is widely used not only as a masking layer [94] but also as a device layer due to its optical and mechanical properties [95][75]. As it has a high refractive index, it offers greater flexibility in the design and fabrication of waveguides. In these applications, accurate patterning of the layer becomes important. Silicon nitride can be wet etched using phosphoric acid [54]. However, this process has the traditional problems associated with wet etching, such as poor etch control and possible damage to thin membranes. As a result, a suitable dry etching process is preferable. As a compound of silicon, it can be etched using fluorine atoms. Due to the weaker $Si-N$ bond, it etches faster than silica [71]. The overall chemical reaction is [54]

Recipe	CHF_3 (*sccm*)	O_2 (*sccm*)	RF (*W*)	Pressure (*mT*)	Time (*s*)
1	20	0	100	40	60
2	20	1	100	40	60
3	20	2	100	40	60
4	20	3	100	40	60
5	40	0	100	40	60
6	40	2	100	40	60
7	40	4	100	40	60
8	40	6	100	40	60

Table 4.9 Initial nitride etching recipes

$$Si_3N_4 + 12\,F \rightarrow 3\,SiF_4 + 2\,N_2 \tag{4.2}$$
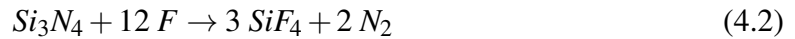
Various gases that are fluorine rich have been studied for the anisotropic etching of silicon nitride, including CF_4, CHF_3, NF_3 and SiF_4 [96]. In order for the etch to be anisotropic, an ionic etching process is required. This has the drawback of poor selectivity with silicon and mask materials such as resists. Using a chemistry containing CHF_3 [97] increases selectivity with silicon, as it contains both reactive species as well as polymer forming precursors [98]. A mixture of CHF_3 : O_2 is sometimes used in order to avoid excess polymer deposition [63]. This causes the etch mechanism to change. When etching silicon nitride with just CHF_3, the main species responsible for the etching are the CHF_3 and CHF_2 radicals. With the addition of O_2, other species are generated including atomic oxygen and fluorine, leading to a reduction in selectivity. If an isotropic etch is desired, using a gas that provides atomic fluorine (such as SF_6) can be used instead. The etch rate of silicon nitride is highly dependent on the deposition method used, with PECVD nitride etching faster than CVD nitride.

As with the anisotropic etching of silicon, the main focus of the study is to arrive at an etching recipe that yields good selectivity, etch profile and smoothness.
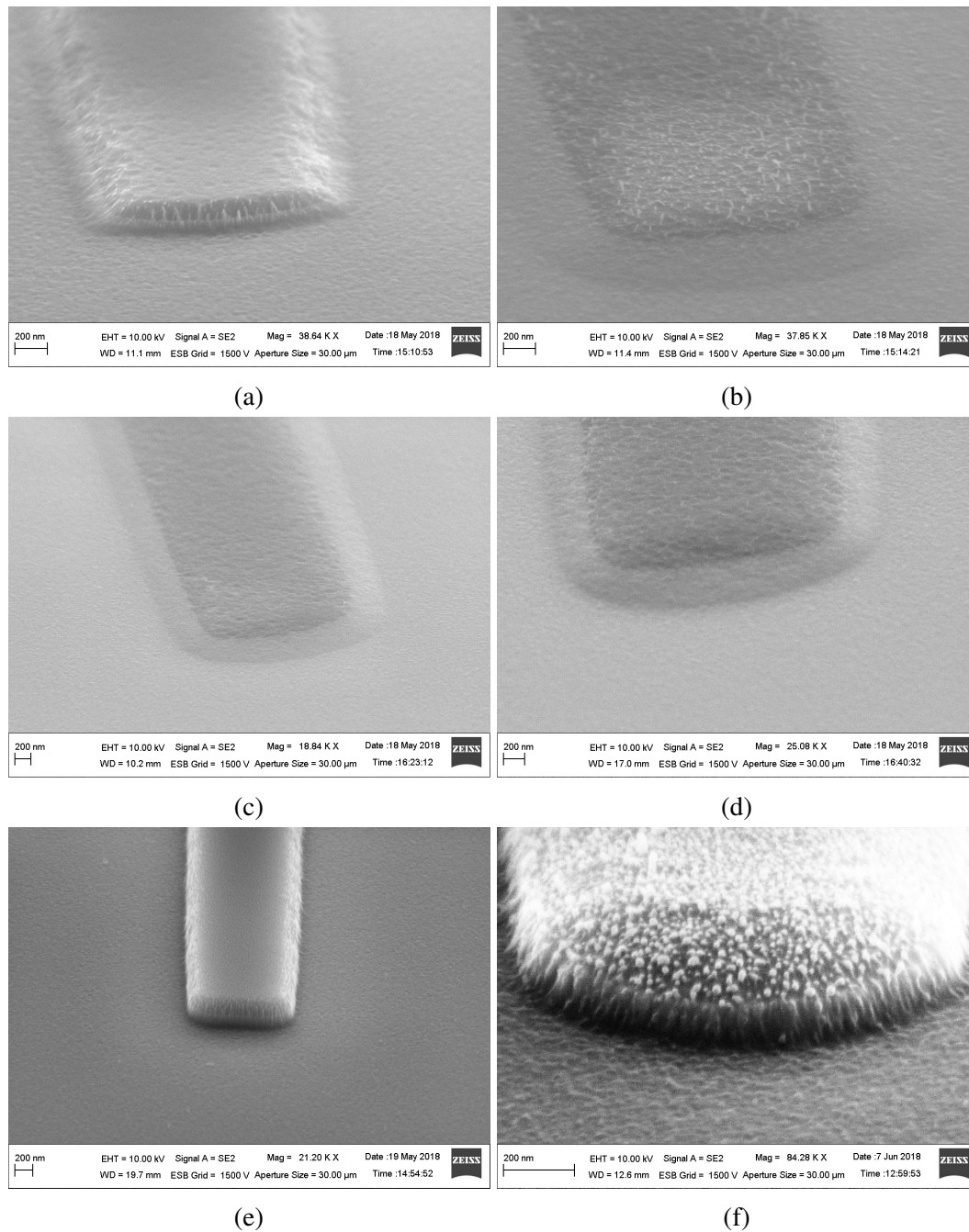
Fig. 4.15 Nitride etch profiles showing extremely sloped sidewalls, with the highest flow rate of CHF_3 and lowest flow rate of O_2 yielding the best results (Figure 4.15e).

(a) Recipe 5.

(b) Recipe 9.

(c) Recipe 10.

(d) Recipe 11.

(e) Recipe 12.

(f) Recipe 13.
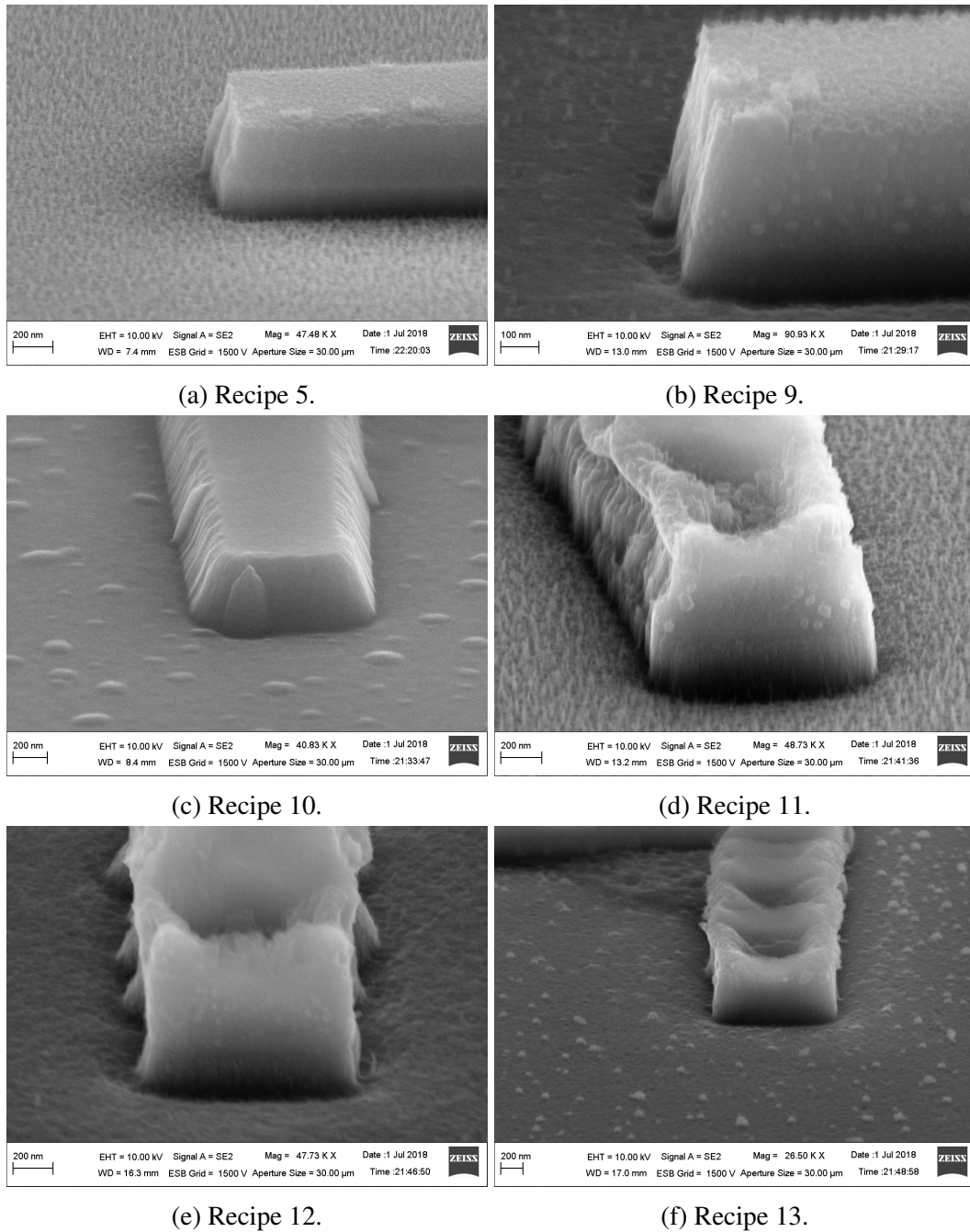
Fig. 4.16 Nitride etch profiles (with resist mask present). The increased pressure leads to decreased anisotropy. The effect of increased power on mask degradation and trenching is also clearly visible.

Recipe	CHF_3 (*sccm*)	O_2 (*sccm*)	RF (*W*)	Pressure (*mT*)	Time (*s*)
9	40	0	100	70	300
10	40	0	100	100	300
11	40	0	200	40	180
12	40	0	200	70	180
13	40	0	200	100	180

Table 4.10 Modified nitride etching recipes

4.5.1   Sample Preparation and Mask Selection

The silicon nitride used in this study was deposited using LPCVD. After the nitride was deposited, the thickness of the film was measured using ellipsometry on different spots on the wafer to ensure uniformity. The film was found to be around 510 *nm* thick. They were cleaned and diced as described in the previous section. The mask chosen, again, was MaN-2403 patterned through E-Beam lithography.

4.5.2   Experimental

The choice of material for the carrier wafer plays an important role, as both silicon as well as silicon dioxide (glass) wafers can be used. This is due to the fact that both silicon and silicon dioxide are etched in fluorine plasma, and therefore contribute to the loading effect.

CHF_3 (*sccm*)	O_2 (*sccm*)	RF (*W*)	Pressure (*mT*)
40	0	100	40

Table 4.11 Optimal nitride etching recipe

Initially the flow rate of CHF_3 was fixed such that the chamber pressure could be maintained at a reasonably low value (40 mTorr) along with a 30% O_2 flow. The sample was placed on a 4" silicon wafer carrier, and the etches were performed for 1 minute so that the risk of complete mask erosion is reduced. The CHF_3 flow rate was varied between 10 sccm to 20 sccm, and the O_2 flow rate was varied between 3 sccm and 9 sccm. The RF power was kept constant at 100 W. These tests were conducted in order to roughly estimate the ideal etch

parameters. Most of the etches yielded extremely sloped profiles and were highly unusable (Figure 4.15). The most promising result was found to be the recipe containing the highest flow rate of CHF_3 (20 sccm) and lowest flow rate of O_2 (3 sccm) (Figure 4.15e). This recipe was repeated again on a glass substrate, in order to determine the best carrier wafer material for the etch. Since the profiles achieved were comparable, and the selectivity was higher, glass was chosen as the wafer carrier material. The etch recipes are presented in Table 4.9.

The etch profiles from these recipes were analysed, and it was found that recipe 5 produced the best profile. The power and pressure values were varied in order to tune the etch further (Table 4.10). The etch times were also increased in order to assess the etch profile better.

4.5.3   Results and Discussion
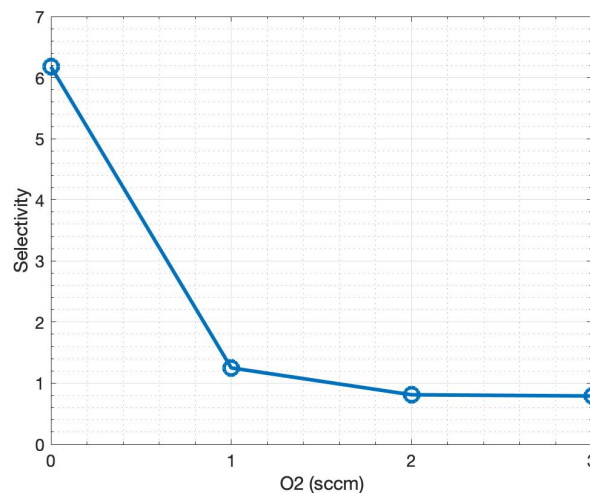
Fig. 4.17 The effect of O_2 flow rate on selectivity.

The optimal anisotropic silicon nitride etching recipe is presented in Table 4.11.

The high flow rate of CHF_3 makes this etch ionic and therefore highly anisotropic. The absence of O_2 increases selectivity greatly. Fig 4.17 illustrates the reduction of selectivity with the increase in O_2. The polymers that might have built up during the etch can be removed using an O_2-plasma clean after the process. Changes to the pressure at lower values

had little impact over the selectivity and etch profile. However, at 100 mT, the etch profile became tapered. Since the etch is ionic, higher power values are preferred; therefore the minimum power value was set at 100 W. Increasing the power to 200 W had an adverse effect on the E-Beam resist mask, due to the resist instability. The etches also exhibit some trenching adjacent to the sidewalls. This is likely due to the charge build up in the resist and nitride layers [89][90].

4.6 Anisotropic Nano-Crystalline Diamond (NCD) Etching

In Chapter 5, the design and fabrication of air-clad NCD waveguides is reported, along with the use of the material in optical applications. The anisotropic etching of NCD reported in this section was developed in order to etch the rib waveguide structures in Chapter 5. Dry etching of diamond has been well studied using different etch chemistries as well as different techniques. For example, narrow features have been etching using a mixture of Ar and O_2 [99], and a mixture of CF_4 and O_2 has been used in order to achieve smooth and selective etching [99]. However, a pure O_2 plasma is more commonly used as the etchant [76][100]. Here, we study the anisotropic etching of NCD using O_2-RIE.

4.6.1 Experimental

Since O_2 plasma etches diamond, using a conventional polymer resist mask would reduce the selectivity drastically. Therefore, Hydrogen Silsesquioxane (HSQ) was chosen as the mask material. HSQ is a negative tone resist that can be patterned through E-Beam lithography. This ensures that the feature size requirement of waveguides can be easily met. HSQ is a spin-on-glass material, which behaves similar to silica after exposure. As the etch rate of silica is negligible in oxygen plasma, the etch selectivity is extremely favourable.

The waveguide dimensions, growth of the NCD and sample preparation is mentioned in Chapter 5. An O_2 flow rate of 30 sccm was chosen as the starting point for the recipe. It is desirable to have a low chamber pressure, since anisotropy is inversely related to it. Due to

O_2 (*sccm*)	RF (*W*)	Pressure (*mT*)	Time (*s*)
30	100	65	180

Table 4.12 Optimal NCD etching recipe
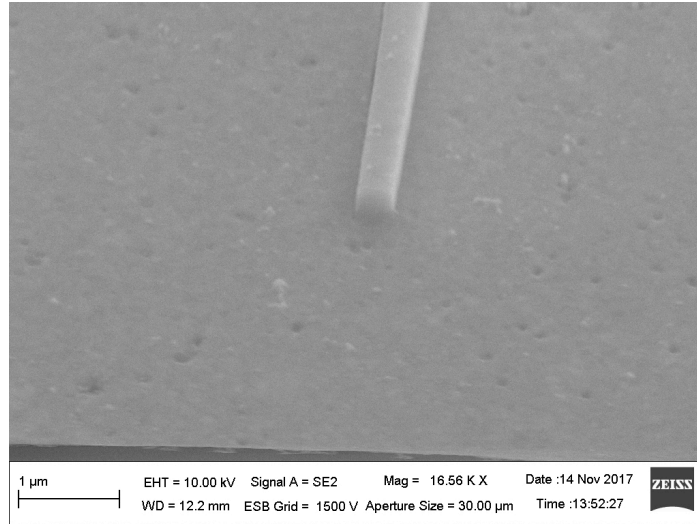
Fig. 4.18 Completed NCD waveguide.

the tool limitations such as chamber size and pump capacity, the lowest chamber pressure at 30 sccm was found to be 65 mTorr. The power was kept at 100 W in order to minimise the surface and mask damage. The etch recipe used is presented in Table 4.12.

4.6.2 Results and Discussion

The waveguide structure after the etch and HSQ removal is shown in Figure 4.18. The etch profile can be seen in Figure 4.19 , where the structure is partially covered by HSQ. The taper from the mask is not transferred to the diamond layer due to the excellent selectivity of the process. The etch rate of the process was found to be around 60 *nm/min*.
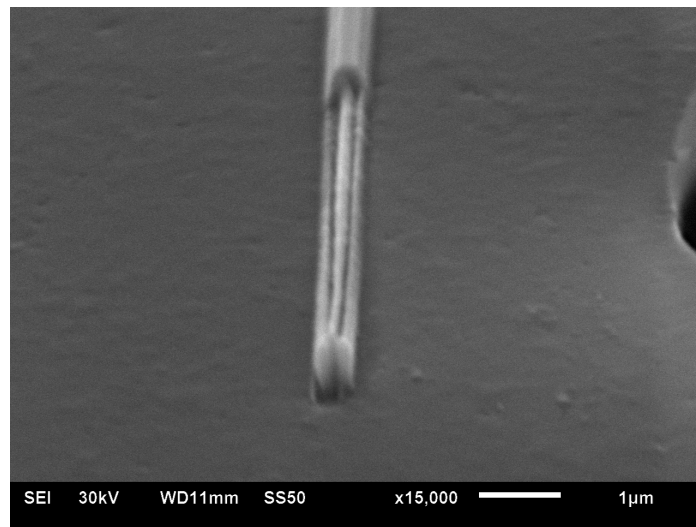
Fig. 4.19 NCD etch (with partial HSQ mask present).

4.7   Summary and Perspective

As mentioned earlier in this chapter, anisotropic etching forms an integral part of the photonic fabrication process. In this chapter we have introduced the basic concepts involved in anisotropic etching. We have also discussed the methods of engineering anisotropic etching recipes for silicon, silicon nitride and diamond, which are the optical materials of interest in this thesis. The anisotropic etching of silicon using two different gas mixtures have been studied in depth, and it was found that the $SF_6 : CHF_3$ mixture provided good results for shallow etches, but it is not preferable for performing longer etches due to its low selectivity. The $SF_6 : CHF_3$ improves the selectivity greatly, and is the better choice. The anisotropic etching of silicon nitride was also investigated, and it was found that the anisotropy can be controlled by altering the RF power. However, excessive power led to severe resist damage as well as trenching. The NCD etching recipe described in this chapter was used in the fabrication of the waveguides mentioned in Chapter 5.

Chapter 5

Air-clad suspended nanocrystalline diamond ridge waveguides [1]

5.1 Introduction

Integrated photonic chip production has developed into a mature technology, with silicon and III-V semiconductor platforms being the dominant materials and the telecommunications spectral window being the main focus of photonic chip research. Expanding this research into other parts of the optical spectrum requires new materials and architectures, mainly due to the absorption bands of the aforesaid materials. In particular, the use of the silicon-on-insulator platform at middle and long infrared wavelengths is limited by the spectral transmission windows of both the buried oxide and silicon device layers in the Silicon-on-Insulator platform.

Diamond is a wide bandgap material with a much larger optical transmission window compared to silicon and III-V materials [101] and is therefore an excellent candidate for photonic chips operating in the UV, visible and infrared spectral regions. Due to its high refractive index (2.39), it allows for the fabrication of sub-micron optical waveguides in integrated photonic chips. Many instances of photonic integrated circuits have been demon-

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[1]The work presented in this chapter has been published as a journal article titled "Air-clad suspended nanocrystalline diamond ridge waveguides" in Optics Express [77].

strated using bonded and thinned single crystal diamond layers [102][103][104]. While the optical quality of the diamond thin films used in this approach is very good, the required bond and layer transfer processes add additional layers of complexity to the fabrication process. In addition, large area single crystals of diamond are expensive and relatively difficult to obtain. As an alternative, polycrystalline diamond thin films can be readily grown on a variety of large area substrates (such as silicon and oxide wafers [105][106]) by chemical vapor deposition (CVD) on a substrate seeded with diamond nanocrystals. Polycrystalline diamond films with nanoscale grain sizes (nanocrystalline diamond (NCD)) inherit a great deal of the optical, mechanical and thermal properties of single crystal diamond and can be used in place of single crystal diamond thin films in numerous applications. Such films can be grown with controlled film stress using a variety of techniques, as reviewed in [107]. Several instances of integrated photonic components have been demonstrated using NCD grown on lower refractive index substrates or buried layers to create vertical confinement [30][108][109]. While this is perfectly acceptable for operation in the visible and near IR, it prohibits operation at longer wavelengths due to absorption in the lower index cladding. One approach for addressing this issue is to create undercut air-clad suspended waveguides, so that the effect of the cladding is completely removed. While such structures have been demonstrated in several instances using silicon waveguides [110][111], this is not generally the case for diamond and nanocrystalline diamond waveguides, even though suspended diamond waveguides can have a much wider transmission spectrum compared to silicon, thereby increasing the range of possible applications of such integrated photonic chips (e.g., far infra-red gas sensing). One relevant example of a suspended nanocrystalline diamond waveguide is reported in [112], where suspended air-clad rib waveguides guide light into suspended 2-D photonic crystals. The suspended structures are supported by 70 *nm* nano-tethers to minimize scattering losses from the tether points. While this approach offers a novel solution for creating NCD waveguides, the structural dependence on the fragile nano-tethers can compromise mechanical stability and robustness. In addition, due to their small size, patterning the 70 *nm* nano-tethers cannot be done without electron beam lithography. Finally, the architecture in [112] does not seem to offer a route for electrothermal on-chip

tuning, which would be a requirement for creating tunable nanophotonic devices such as ring resonators.
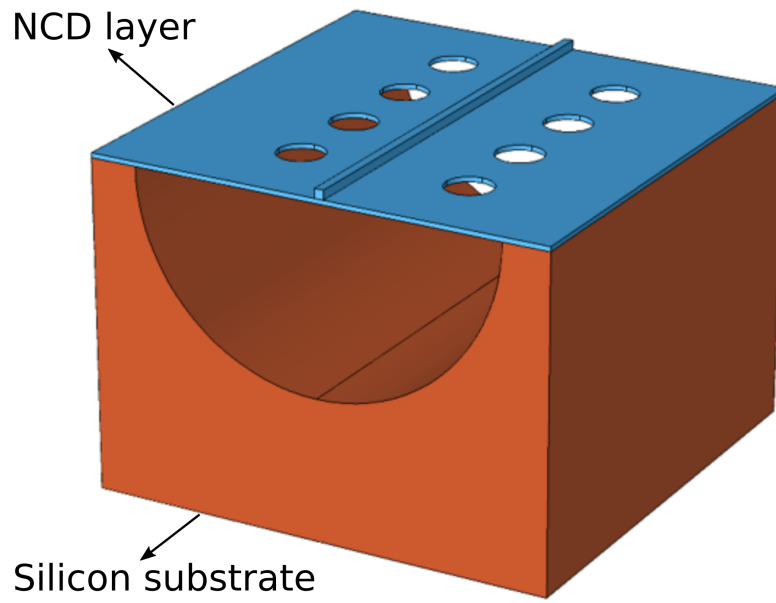
Fig. 5.1 Schematic of the proposed structure depicting the suspended diamond membrane (shown in blue) and the underlying silicon layer (shown in red).

As an alternate route, here we report a hybrid group IV waveguide platform consisting of suspended diamond ridge waveguides fabricated from NCD thin films grown directly on silicon substrates (Figure 5.1). This architecture not only creates the necessary vertical and lateral confinement needed to create a confined mode, it also offers a path for complete utilization of the wide optical transmission window of diamond, while being mechanically robust. The support membrane can also be utilized to add metal heatpads for electrothermal tuning. Finally, even though the waveguides here are written using e-beam lithography (for patterning flexibility), this is not an absolute necessity and all the features can be, in principle, patterned using optical lithography. . In the first part of the paper we present the architecture and associated waveguide simulations and design steps. Then we present details of the fabrication process and finally present optical measurements on these suspended waveguides, followed by a discussion on future potential applications of this waveguide platform.

5.2   Design

Since the NCD layer is grown on silicon substrates, the platform will not inherently possess
vertical confinement, due to the considerably larger refractive index of silicon (3.47). While
this can be remedied by using a lower index interlayer (such as an oxide layer a few microns
thick), we have chosen an alternative route, namely creating a suspended rib waveguide
with air cladding above and below it (Figure 5.1). As mentioned, this architecture has the
advantage of being limited only by the diamond transmission window. In addition, since
an appreciable portion of the optical mode lies in the air cladding, it offers a convenient
platform for sensing applications, in particular gas sensing. Given this architecture, all the
optical simulations have been carried out for a suspended air-clad ridge waveguide, under
the assumption that the void is large enough to optically isolate the diamond layer from the
silicon substrate. The 1550 *nm* telecommunications wavelength was chosen for the design,
due to the technological relevance of this wavelength and availability of test equipment,
however the same approach can be easily adapted to longer wavelengths.

The test wafer consisted of a polished 520 *nm* NCD layer grown on silicon, on which
partially etched waveguide ridges were created. The major constraint in designing the
waveguide structure is the ridge etch depth. A shallow etch will result in a weakly confined
optical mode, which will limit the bend radius. On the other hand, a deep etch will result in a
very thin support membrane, thereby compromising the structural integrity of the device.

Bend losses were calculated using a finite element solver (COMSOL) and an exact
mapping of Cartesian to curvilinear coordinates [113]. From this, we deduced that an
etch depth of 350 *nm*, corresponding to a 170 *nm* support membrane will provide a good
compromise between optical confinement and mechanical integrity, while ensuring single
mode quasi-TE operation. The quasi-TE mode distribution is depicted in the inset of Fig.
1(b).

Inverse taper edge-couplers were designed for coupling light in and out of the waveguides.
The edge-coupler was chosen due to the broadband nature of the coupling and fabrication
simplicity. Assuming a single etch depth throughout the chip, the coupling efficiency between
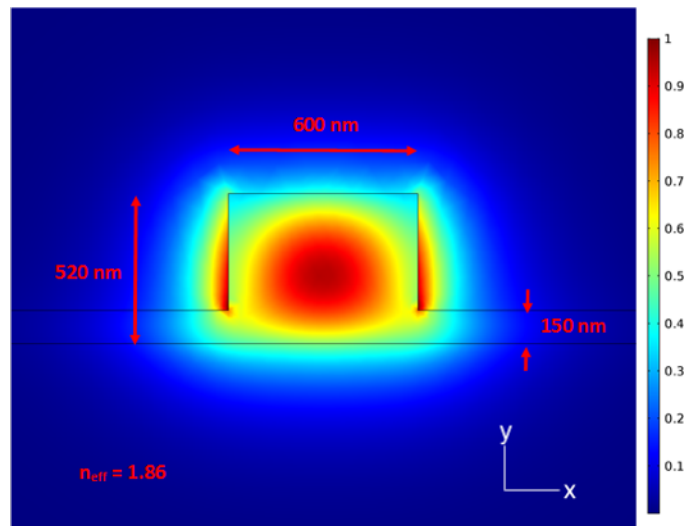
(a) Designed dimensions of the structure.
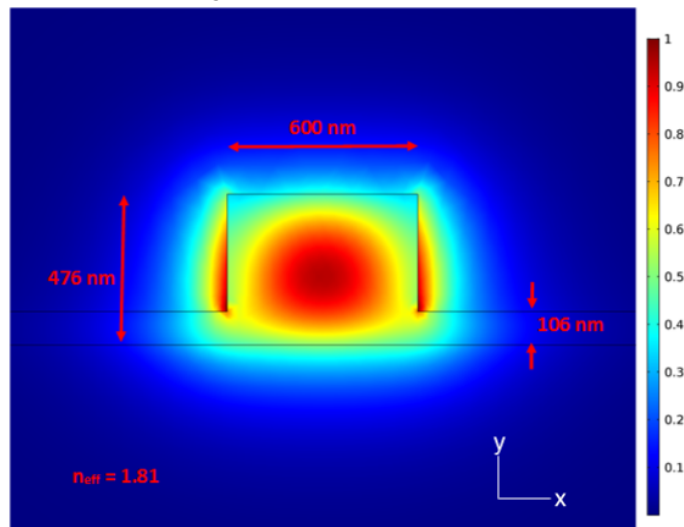
(b) Fabricated dimensions of the structure.

Fig. 5.2 Dimensions of the NCD waveguide (the gradient bar shows the normalised E-field norm (V/m)).

a flat single mode fiber facet and the taper was simulated, resulting in a calculated optimized coupling of 83% for a 300 nm wide inverse taper coupler.

5.3   Fabrication

The NCD was grown on a 500 μm thick, highly doped silicon wafer, as reported in [114].First, a mono-dispersed nanodiamond solution was applied in an ultra-sonic bath for 10 minutes to seed the silicon wafer. A 600 nm thick layer of diamond was grown on top of the silicon surface through CVD (CH_4 at 5 sccm; H_2 at 475 sccm; Pressure = 40 Torr; Power = 3500 W; Time: 298 minutes; Temperature = 842° C). The film was grown with an initial 5 min incubation period of 25 sccm CH_4 to establish the seeds before reducing to 5 sccm for the remainder of growth. The film was then thinned down to 520 nm through chemical mechanical polishing (using colloidal silica fluid, Logitech SF1) to achieve an RMS surface roughness value below 2 nm. An array of L-shaped suspended diamond ridge waveguides of lengths ranging from 1.524 to 4.524 mm was chosen for the study. The waveguides were fabricated via electron beam lithography, optical lithography and dry etching steps. First, the ridge was patterned using hydrogen silsesquioxane (HSQ) using electron beam lithography (Vistec EBPG5200, 100 kV) (Figure 5.3). The diamond film was then etched anisotropically down to 170 nm in order to form the ridge waveguide using reactive ion etching (RIE) with O_2 at 30 sccm, pressure = 65 mTorr and RF power = 100 W. This recipe provided the desired vertical side walls and had an etch rate of about 60 nm/min. The HSQ mask was removed using a hydrofluoric acid dip and a 40 nm thick chromium mask was then deposited on top of the partially etched diamond film. Optical lithography and a chromium wet etch (CR-7) were used to pattern the etch holes (3.3 μm diameter each) in the chromium mask. This pattern was transferred to the diamond film through a second anisotropic etching step using the same oxygen RIE parameters, after which the entire chromium film was removed using CR-7.

All wet processing steps were performed before undercutting the diamond film, to reduce the chances of damaging the undercut structures. Finally, the silicon substrate was isotropically dry etched through the diamond holes using a pure SF_6 ICP-RIE etch step
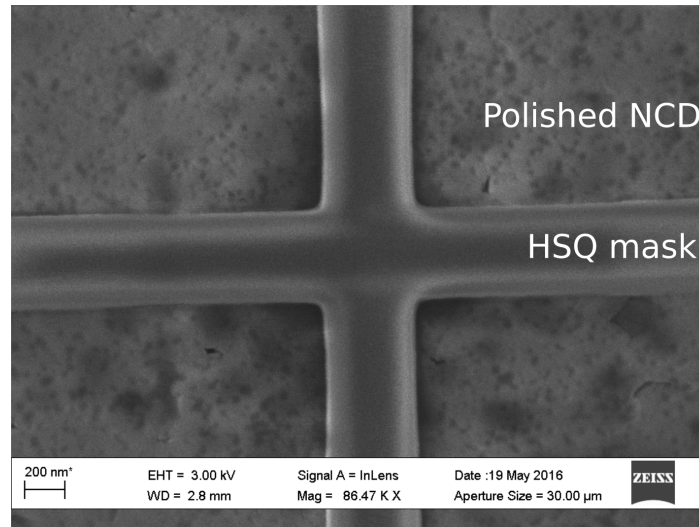
Fig. 5.3 SEM image of NCD surface after e-beam lithography of HSQ etch mask.

(50 sccm SF_6, 30 mTorr, 1500 W ICP power, 0 RF power). While the etch rate of the isotropic silicon undercut step is quite high (approximately 4 $\mu m/min$ for an unpatterned silicon surface), this was considerably reduced due to the limiting effect of the small holes in the diamond film. As a result, a 60 minute etch step was required for complete removal of the silicon from beneath the waveguide ridge (Figure 5.4), resulting in a 20 μm radius half-cylinder trench (measurement based on the optical image in Figure 5.6). Note that the trenches flare out at the start and end of the waveguides, due to the larger etch rate at these locations. Thin film thickness measurements on the diamond film revealed that it had been etched down at a rate of 1 nm/min in the SF_6 ICP plasma. As a result, the diamond support membrane and the top of the ridge had also been etched down 60 nm in the process of isotropic silicon removal. The lateral dimensions of the waveguides were not affected, which suggests a vertical physical etch component to the nominally isotropic SF6 etch. While this phenomenon did not substantially affect the waveguide mode, it is still preferable to avoid or minimize it if possible, since it contributed to increased surface roughness on the top of the diamond waveguide ridge. This can be achieved by using larger etch holes (to shorten the overall undercut time) or by using a non-plasma isotropic silicon etch process such as XeF_2 to avoid any unintended reactive ion acceleration due to residual charges. Another side effect of the lengthy isotropic etch step was to create a larger than intended undercut on the

edge of the chips, where the input and output tapers were situated. This is due to the fact that the etch rate of the unmasked silicon on the chip edges is much faster compared to etching through the holes in the diamond film. Due to this and the thinning of the support NCD membrane (in the SF_6 etch step), the edges of the diamond membrane exhibited a noticeable sag (Figure 5.5 and Figure 5.6) which was different across the waveguides, depending on the position of the waveguides on the chip. This causes a drop in the edge coupling efficiency and is a motivating factor for moving towards other light coupling mechanisms such as grating coupling, since a grating coupler fabricated on a suspended membrane would be supported on all sides, thus drastically reducing the membrane sag.
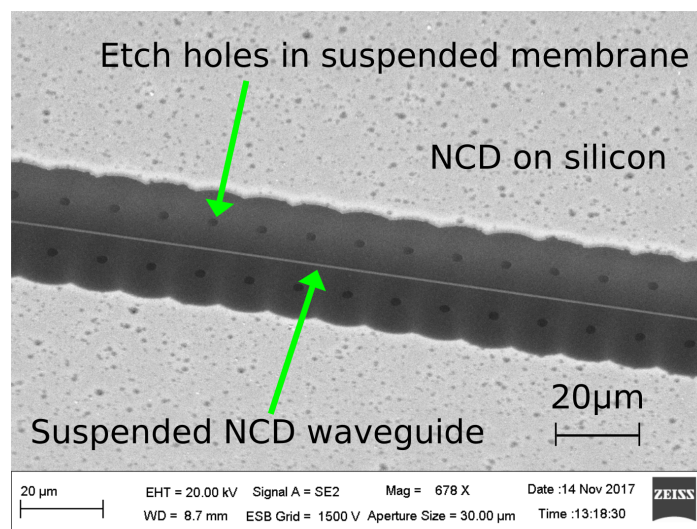
Fig. 5.4 SEM image of the undercut waveguide and membrane.

5.4   Optical Measurements

Polarized light from a tunable telecommunications laser was injected into the L-shaped waveguides using a lensed fiber. The original objective was to use the cutback method for loss measurements but the unexpected non-constant coupling between waveguides due to the varying membrane sag and the large amount of scatter from the waveguides prompted us to instead use the scattered light for quantifying the waveguide losses. The scattered light was
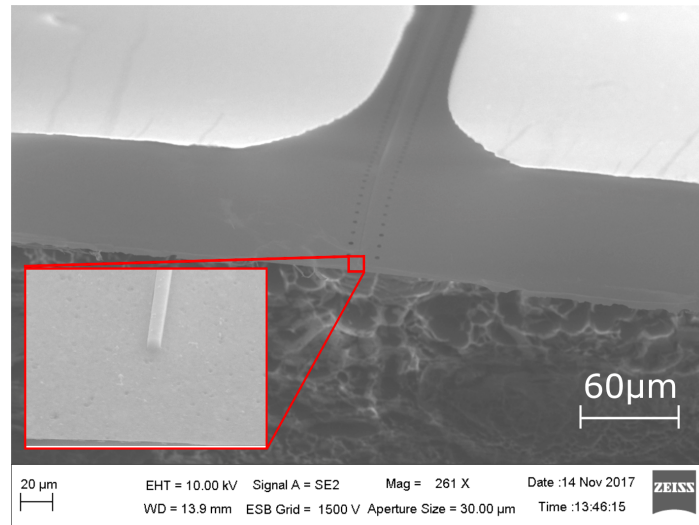
Fig. 5.5 SEM image of the input waveguide taper showing membrane sag.

collected using a near-infrared camera (Xenics Xeva 640) viewing the chip from the top (Fig. 3(a)). The obtained images were then processed to extract the optical losses by calculating the power drop along a horizontal or vertical segments of four different waveguides, under the assumption of uniform roughness scattering, and then fitting the results to an exponentially decaying function $P(L) = P(0)e^{-\alpha L}$ where $P(L)$ is the relative scattered power at the end of the segment and $P(0)$ is the relative power at the beginning of the segment (Fig. 3(b)). The bend sections were not included in the calculations. Scattered power at each point along the waveguide was estimated by integration across the waveguide width. An average loss coefficient of $4.67 \pm 0.47\ dB/mm$ has been extracted from the measurements listed in Table 5.1 with good fit (R^2 value above 0.9). It is of interest to note that while these loss numbers are higher than reported values for single crystal diamond waveguides, they are in the vicinity or smaller than other reported NCD waveguides [109][112][115]. This is likely due to the improved overall qualities of our NCD films that were grown and polished using the techniques outlined in [114]. For comparison, even though the surface roughness of the diamond film used in [112] is reported to be much lower than our etched final waveguide roughness (1.6 nm vs 27 nm), their losses are in the same range ($5 - 7\ dB/mm$). This may be due to the larger granularity in their diamond film (based on the SEM view of the diamond film.)
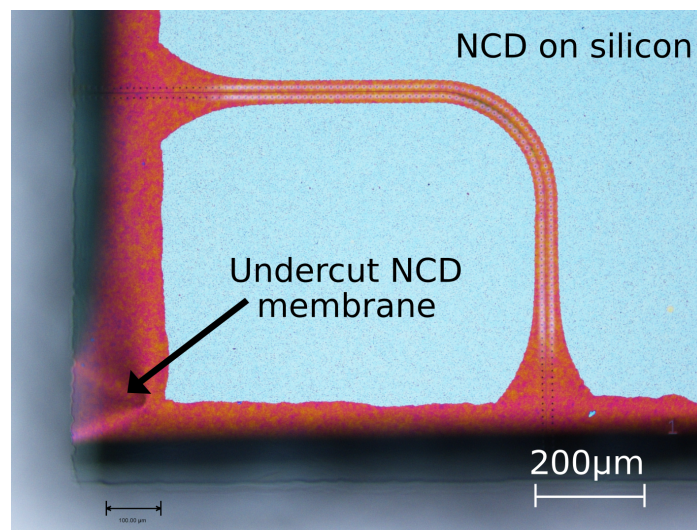
Fig. 5.6 Optical image of an undercut waveguide showing the sagging edges on the chip (the membrane wrinkle can be seen in the bottom left of the image).

Sample	L (μm)	P(L)/P(O)	R^2	Loss (dB/mm)
1	600	0.35	0.96	8.35
2	1000	0.52	0.92	3.41
3	1000	0.53	0.92	3.12
4	1050	0.53	0.93	3.50
5	1134	0.26	0.96	5.36
6	1150	0.31	0.94	3.93
7	1668	0.17	0.95	5.03

Table 5.1 Average loss measurements of various waveguides' segments

Since the losses of optical grade single-crystal and polycrystalline diamond [116] are much smaller than the values obtained through the loss measurement, other loss mechanisms need to be considered. The SEM image of the surface of the diamond film before etching (Figure 5.3) shows some dark spots that may indicate foreign particles in the diamond film, possibly from the silica-based polishing fluid. AFM imaging of the final waveguides shows a large amount of roughness on the top surface, as indicated in Figure 5.7.The presence of the silica polishing material in conjunction with the SF_6 etch step may be a contributor to this roughness (acting as nanoscale mask points) and it is likely that this roughness is the main source of optical losses in the NCD waveguides. This is supported by the considerable

amount of scattered light in the IR images. It should be noted that none of these issues are inherent to NCD films and they can be addressed with appropriate adjustments to the growth and polishing steps.

σ = 27.08nm
L$_c$ = 350nm
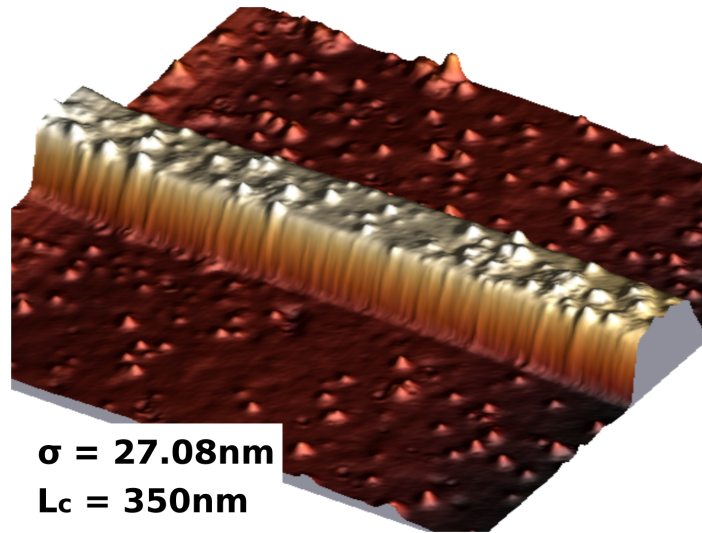
Fig. 5.7 AFM image of waveguide ridge with roughness measurements.

To analyse the effect and contribution of the roughness on the waveguide performance, we attempted to estimate the predicted losses using a scattering model. The total waveguide propagation loss is given as $\alpha = \alpha_{bulk} + \alpha_{rs}$ where α_{rs} is the scattering due to rough waveguide surfaces and other effects. Since the NCD film is grown on a polished silicon surface and the roughness of the sidewall is much smaller than the top, only the roughness on the top surface was considered. Some additional loss due to scattering from voids between the nanocrystalline grains may be present, however for a first order estimate this again was considered negligible compared to the large waveguide surface roughness. The absorption coefficient of bulk diamond at 1.55 μm is approximately 0.01 dB/mm [116]. α_{rs} was estimated using the roughness scattering formula for the TE_0 slab mode, developed by Payne and Lacey [117]. The model relates the optical scattering loss from rough surfaces to the RMS roughness σ according to the equations:
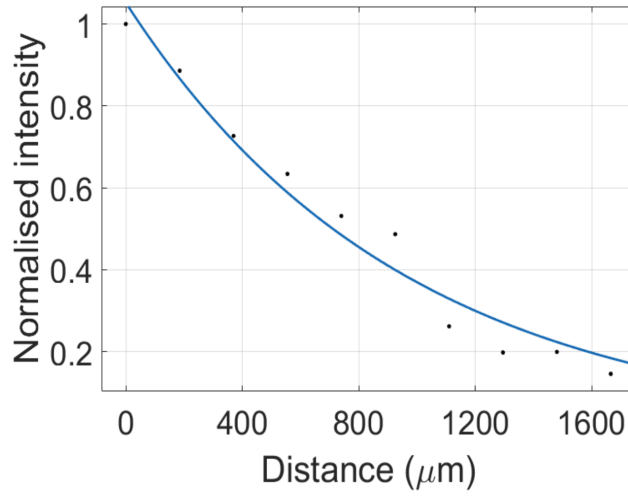
Fig. 5.8 Example of power decay measurement fitting ($R^2 = 0.96$).

$$\alpha_{rs} = \frac{\sigma^2}{\sqrt{2}k_0 d^4 n_1} \cdot g \cdot f(\chi, \gamma), \tag{5.1}$$

$$g = \frac{U^2 V^2}{1 + W}, \tag{5.2}$$

$$f(\chi, \gamma) = \chi \sqrt{\frac{\sqrt{((1+\chi^2))^2 + 2\chi^2 \gamma^2} + 1 - \chi^2}{(1+\chi^2)^2 + 2\chi^2 \gamma^2}}, \tag{5.3}$$

$$\chi = W \frac{L_c}{d}, \tag{5.4}$$

$$\gamma = \sqrt{\frac{2n_2^2}{n_e^2 - n_2^2}}, \tag{5.5}$$

$$U^2 = k_0^2 d^2 (n_1^2 - n_e^2), \tag{5.6}$$

$$V^2 = k_0^2 d^2 (n_1^2 - n_2^2), \tag{5.7}$$

$$W^2 = k_0^2 d^2 (n_e^2 - n_2^2), \tag{5.8}$$

where n_1, n_2 and n_e are the core, cladding and effective indices, k_0 is the free space wave number, d is half the slab thickness and L_c is the roughness correlation length. $f(\chi, \gamma)$ is the roughness spectral density function and g accounts for the effect of the waveguide structure and refractive indices. From the AFM measurement, the top surface σ and L_c are estimated to be 27 *nm* and 350 *nm*. These were calculated from the standard deviation and Fourier spectrum of the roughness scans, respectively. Using these parameters, the estimated waveguide loss is 4.7 *dB/mm*, which is reasonably close to the measured values. Additional scattering from sidewall roughness and occasional defects, contamination and voids in the film may appreciably increase this value (e.g., for waveguide 1 in Table 5.1). Based on this analysis, it is reasonable to expect that improvements in the fabrication process which target the roughness of the top waveguide surface will result in a marked improvement of the waveguide loss characteristics. In particular, using the roughness parameters of the original unprocessed film ($\sigma = 2$ *nm* and $Lc = 60$ *nm*), the predicted scattering loss is 0.11 *dB/mm*, which will be a drastic improvement in loss performance. Potential improvements can be effected by using a chemical gas etch step (such as XeF_2) for undercutting the silicon layer, increasing the size of the etch holes and by allowing the e-beam resist to remain on the top of the waveguide ridge until after the undercut is finished.

5.5　Summary and Perspective

In this chapter we have demonstrated an air-clad suspended NCD platform using the SF_6 ICP etching process. This architecture utilises the excellent optical and mechanical properties of NCD, and provides an attractive alternative to commonly used optical materials. The ridge waveguides were optically characterised at 1550 *nm*, and yielded an average loss of 4.67 *dB/mm*. However, this platform can be easily scaled to operate over a wide section of the optical spectrum, covering the UV to the far-infrared and therefore can have a large range of
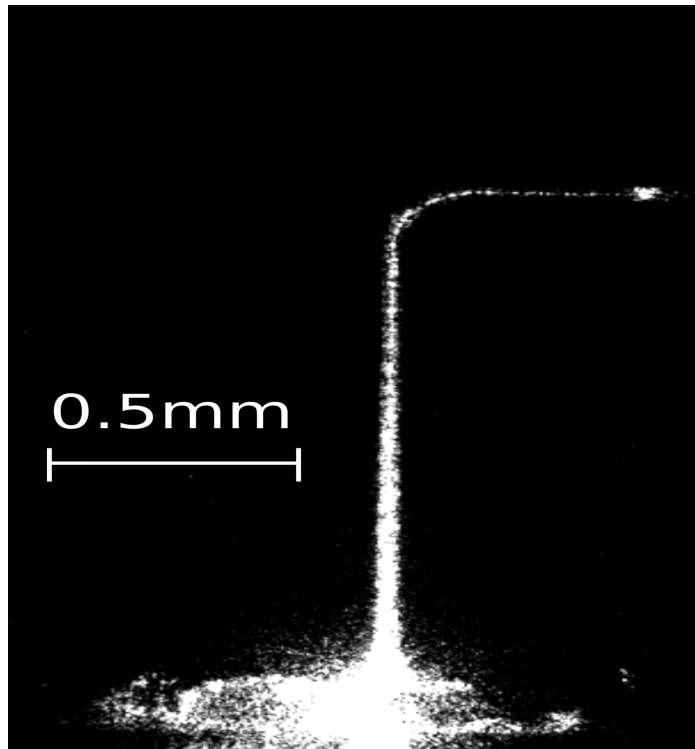
Fig. 5.9 IR image of the scattered light at 1.55 μm.

applications ranging from visible light integrated photonics to far-infrared optical sensing. The performance of this device can be further improved by reducing the surface roughness of the NCD film, by increasing the size of the etch holes, and by allowing the E-beam resist mask to remain on the top of the waveguide ridge until the undercut etch is completed.

Chapter 6

Isotropic silicon etch characteristics in a purely inductively coupled SF$_6$ plasma [1]

6.1 Introduction

6.1.1 Semiconductor Etching

Etching is an integral component of micro and nano-fabrication processing, therefore attracting considerable attention in the semiconductor industry. As the scope of etching can be vast, ranging from the removal of entire layers from wafers to the etching of sub-micron features with high precision, developing an etching technique that is appropriate for the application is crucial. Dry etching methods, especially, have been extensively studied because of the rapidly reducing node sizes of semiconductor components. Initially developed to remove organic residue and for "ashing" photoresists[118], dry etching techniques such as Reactive Ion Etching (RIE) can be used to achieve very high selectivity (provided that the etching chemistry and the process parameters are well chosen). Such techniques can also be engineered to achieve the desired level of anisotropy, therefore enabling the fabrication of high aspect ratio trenches [118] and pillars [119].

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[1] The work presented in this chapter has been submitted for publishing in the Journal of Vacuum Science and Technology A as "Isotropic silicon etch characteristics in a purely inductively coupled SF$_6$ plasma" by P. Panduranga, A. Abdou, Z. Ren, R. H. Pedersen and M. P. Nezhad.

Isotropic etches, essential for removing sacrificial layers, releasing MEMS structures and isolating membranes, have been conventionally realised through wet etching techniques, using chemicals such as HNO_3:H_2O:NH_4F or KOH [54] (to etch silicon) and HF (to etch silica). However, this approach can lead to problems, as the surface tension of the wet etchants can damage delicate structures and membranes. Alternatively, vapour phase etching can be used to overcome the problems associated with wet etching. As in the case with wet etching, the etch is completely chemical in nature, and without a physical component, usually resulting in isotropic etch profiles. As the etching occurs in the vapour state, and the etchants react with the substrate readily, the etch takes place without the need to generate a plasma. Vapour phase etching of silicon can be performed using chemicals like xenon difluoride (XeF_2), bromine trifluoride (BrF_3) and chlorine trifluoride (ClF_3)[64] [65]. Since its synthesis in 1962 [66] [67] [68] , and subsequent development as an isotropic etchant [69], XeF_2 has been widely used as a vapour phase etchant, as it is highly selective to silicon with respect to aluminium, photoresist and silica. Similarly, silica has been selectively etched using a similar process using HF vapour.

One unintended consequence of using the XeF_2 etch is that it reacts with moisture, forming HF, which in turn etches SiO_2 [48]. This may lead to selectivity issues when using a silica mask . It also requires specialised equipment and it is not integrated into conventional CMOS processes. Furthermore, both the equipment required for the etch and the chemical itself are niche and somewhat expensive, making the process less economically viable. To remedy this, alternative approaches using plasma etching have been explored, as described in the next section.

6.1.2   The SF$_6$ Isotropic ICP Etch

It has been well established that silicon readily etches in fluorine-based gases and plasmas [120], with chemical etching in these materials leading to large undercuts [71]. The exact chemical reaction that takes place during the etching process of silicon with fluorinated plasma is still not completely understood, and is the subject of some debate [121] [122]. As the F atoms are formed in the plasma by electron impact dissociations, they react

with the surface silicon to form SiF_4. However, significant amounts of SiF_2 and SiF_3 are produced as primary and subsequent etch products. Though several fluorinated gases such as tetrafluoromethane (CF_4), fluoroform (CHF_3), nitrogen trifluoride (NF_3), boron trifluoride (BF_3), etc., have been used, sulfur hexafluoride (SF_6) is particularly useful, owing to its superior etch rate and inert nature [85]. SF_6 also does not contain carbon and hydrogen atoms, therefore having the advantage of not producing hydrocarbon by-products. Plasma etch parameters can be adjusted to ensure a high degree of isotropy, along with other desirable properties such as selectivity. The choice between the two commonly used RIE techniques - Capacitively Coupled Plasma (CCP) and Inductively Coupled Plasma (ICP), usually depends on the application, and can result in vastly different etch outcomes. In a CCP-RIE etcher, gas is fed into an etch chamber and an RF voltage is applied between two parallel electrodes, which ionises the gases in the chamber, and the plasma generated is used for chemically etching the material. Due to the higher electron mobility (compared to the ion mobility), the low electrode becomes negatively charged, and this in turn leads to the formation of the positively charged sheath above it. The acceleration of the ions in the chamber towards the negative electrode is proportional to the potential build up in the electrode (known as the DC bias). This provides the kinetic energy to the ions, and is the source of the physical component of the etch. The RF power has the largest influence on the DC bias, though it is also affected by factors like chamber pressure, gas composition and gas flow. Since the DC bias is linked to the RF lower source, the impact of the ion based etching cannot be controlled independently. The electron density and the gas dissociation factor in CCP-RIE systems are also lower than Induction Coupled Plasma (ICP) RIE systems [63]. In contrast, in an ICP-RIE system, the ionisation of the gas takes place separately and away from the substrate. The system is powered by two RF sources, where one is used to generate the plasma (inductively) and the other is connected to the electrode for ion acceleration (providing the DC bias). The powered coils surrounding the chamber result in a changing magnetic field, leading to an induced electric field inside the chamber. The entire system therefore can be thought of as a combination of two separate units: one to control the number of ions generated, and the other to control the momentum of the ions. The possibility of generating a high

density plasma without very high ion energy is an attractive proposition, as lower ion energy improves the physical etch selectivity and also reduces the damage to the substrate caused by ion bombardment.

SF_6 plasma etching in an ICP-RIE reactor is an attractive method for the isotropic etching of silicon due to the higher density of radicals, as the radicals are responsible for the bulk of the etch. This particular etch is one part of the two step etching process known as the Bosch process, which involves consecutive steps of isotropic etching and passivation [84] [83]. The Bosch process was developed to combine the advantages of the pure SF_6 ICP etch (high etch rates) while also achieving anisotropy and vertical sidewalls. In contrast, we investigate the utility and the characteristics of the ICP SF_6 etch in the isotropic etching of silicon.

6.1.3   Isotropic Etching in Photonic Device Fabrication

Etching, in general, plays a very important role in the fabrication of photonic devices. For example, anisotropic etching is crucial in creating the vertical and smooth sidewalls of waveguide structures [28] [74]. Wet isotropic etching has been used not only to remove entire layers, but also for the controlled removal of material. For example, HCl has been used to etch InP in the fabrication of photonic lasers [123][124], and HF has been used as a wet etchant for the controlled removal of silica during the fabrication of pedestal waveguides [125]. As mentioned earlier, XeF_2 is a popular dry isotropic silicon etchant, and has been used for the fabrication of silica micro-toroid resonators [126]. We have earlier demonstrated the use of SF_6 isotropic etching to form suspended nano-crystalline diamond waveguides [77].

Though isotropic etching in SF_6 and a comparison of different fluorine based etchants and their etch rates [85] have been reported, isotropic etching of patterned substrates have not been well studied. The aim of this study is not to determine the effects of different etching parameters, but rather to better understand the etch characteristics, having arrived at a suitable recipe. Earlier studies have presented the ideal etching parameters for achieving the highest etch rates for bulk crystalline silicon substrates (unpatterned). We have found the behaviour

of these etches is radically different for patterned substrates, with strong dependency on the
pattern features and the substrate size.

6.2   Experimental

Sample	Etch Depth (nm)	Time (min)	Etch Rate(nm/min)
Circle 1	4399	2	2199
Circle 2	9085	4	2271
Circle 3	12474	6	2079
Circle 4	18141	8	2267
Circle 5	21461	10	2146
Circle 6	37111	15	2474

Table 6.1 Etch rates of the 500 μm circles

In order to quantify the etch itself, parameters such as etch rate, surface roughness and
anisotropy have to be considered. Anisotropy, which is the preferential removal of material
in a specific direction, becomes a critical parameter, especially in the context of anisotropic
etching of patterns. In *KOH* wet etching, anisotropy is achieved as a result of difference in
etch rates due to the crystalline orientation, However, in dry etching, anisotropy is achieved
because of preferential etching in the vertical direction due to ion bombardment or formation
of inhibitors on the sidewalls to protect them. The penetration of the etchants as well as
the mass removal of the etched byproducts also has an affect on the anisotropy. Since the
focus of this study is the isotropic etching of silicon, it is important to define an appropriate
quantitative metric for isotropy. The degree of isotropy (I) can be defined as:

$$I = \frac{H}{V},\tag{6.1}$$

where H is the etch depth in the horizontal direction and V is the etch in the vertical direction
(Figure 6.1). Therefore, completely isotropic etches have I=1, and completely vertical etches
have I=0.
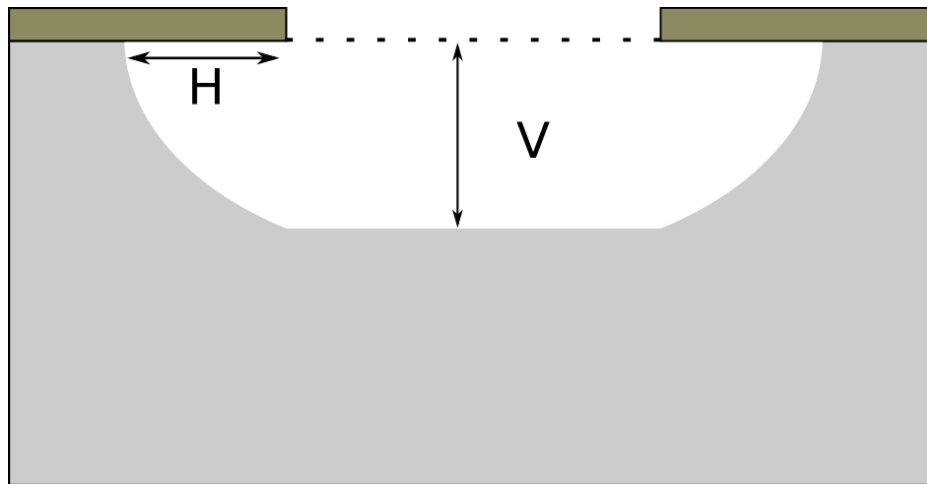
Fig. 6.1 A schematic of the definition of isotropy used, showing the location of the *H* and *V* measurements.

6.2.1   Sample Preparation

Thermally oxidised 4" silicon wafers with the oxide thickness of 290 *nm* were used to prepare the samples for this study. They were then diced into squares of approximately 1 *cm* × 1 *cm*. All the samples were cleaned using the standard degrease cleaning process which consists of 5 minutes of ultrasonic agitation in methanol, acetone and isopropanol, followed by rinsing in flowing D.I water for 2 minutes. The samples were then dried using a nitrogen gun. The final step was a 10 minute dehydration bake at 250°*C* in order to remove all the moisture from the substrate.

A 100 *nm* thick layer of chromium was deposited on the samples through sputtering (Figure 6.2), as the oxide layer cannot be used as the only mask for this study, since the *SF*$_6$ plasma may etch the oxide layer. The reason for choosing chromium-on-oxide over chromium as the mask material was that we found that the chromium layer on its own tends to sag or collapse during long isotropic etches (Figure 6.3). The samples (1 *cm* × 1 *cm* chips) were then spin coated with AZ-1505 photoresist and patterned using optical lithography using two sets of patterns. Pattern 1 consists of 8 circles of diameter 500 *μm* arranged diagonally across the chip with a 990 *μm* gap separating them. Pattern 2 consists of 4 sets of lines, 1 *cm* in length. Each set is made up of individual lines ranging from 8 *μm* to 28 *μm*, the lines separated by a distance of 200 *μm*. The patterns were then transferred to the chromium layer
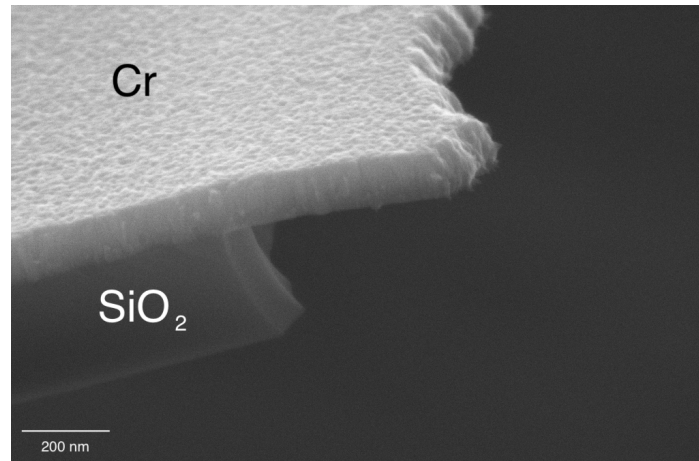
Fig. 6.2 The suspended edge of the chromium on silica mask, after isotropic removal of the underlying silicon in the SF_6 plasma. The undercut of the silica layer is due to the wet buffered oxide etching during the mask patterning step.
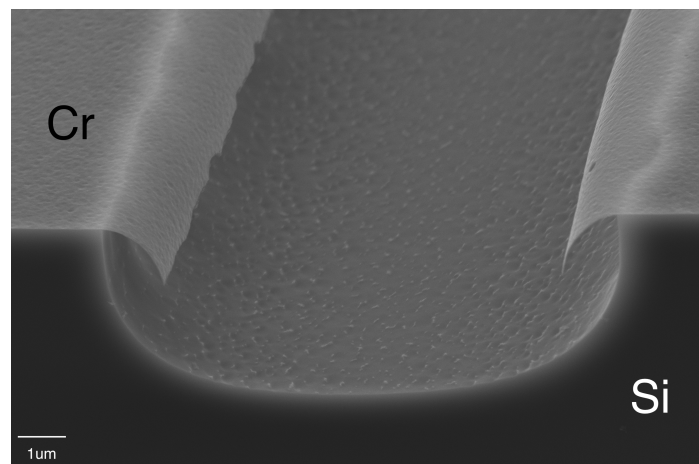
Fig. 6.3 Sag of the unsupported chromium mask layer during undercut.

using a commercially available etchant (CR-7). Finally, Buffered Oxide Etchant (BOE) was used to etch the oxide layer in order to reveal the silicon layer underneath.

6.2.2   Experimental Setup

The study was conducted in three parts:

- Part 1: This was conducted to measure the etch rate of the process in large area circles without the constraints of aspect ratio, micro masking and other etching phenomena that are dependent on the features, sample size, etc. Due to the relatively large size of

the circles (500 μm), the etch rate and roughness at the centre of the features can be approximately viewed as the etch rate of bulk silicon. All the samples were placed in similar areas of the chamber on a 4" silicon carrier wafer to ensure that the loading effect is mitigated.

- Part 2: This part of the study was designed to investigate the effect of feature size on the etch. Samples patterned with the series of lines were chosen for this experiment, and were etched for times ranging from 30 seconds to 15 minutes, resulting in semi-circular or semi-ovoid channels (Figure 6.4). As in part 1, the chips were placed in the same part of the chamber on a 4" silicon carrier wafer.

- Part 3: This was conducted to obtain the etch rate of the process without the balancing effect of the carrier wafer. Samples patterned with the circles were placed directly on a stainless steel carrier, and etched without the presence of the silicon wafer. The reduced area of exposed silicon has a considerable effect on the etch rates.

Sample	Time (min)	RMS Roughness (nm)
Circle 1	2	22.04
Circle 2	4	8.39
Circle 3	6	15.25
Circle 4	8	13.01
Circle 5	10	24.64
Circle 6	15	25.26

Table 6.2 Surface Roughness vs Time

All of the samples were etched using the same recipe in the same ICP-RIE system, an Oxford Instruments PlasmaPro 100 Cobra[300]. The chamber pressure was set to 30 mT, and the substrate temperature to $20^{\circ}C$. The ICP power was 2000 W with a bias of 0 V. Finally, the SF_6 flow rate was set to 50 sccm. The samples were fixed to the surface using Teflon tape on the edges.

The width and depth of all the features were measured before the isotropic etch using a Bruker Dektak profilometer. After the etches were performed, the chromium and the oxide
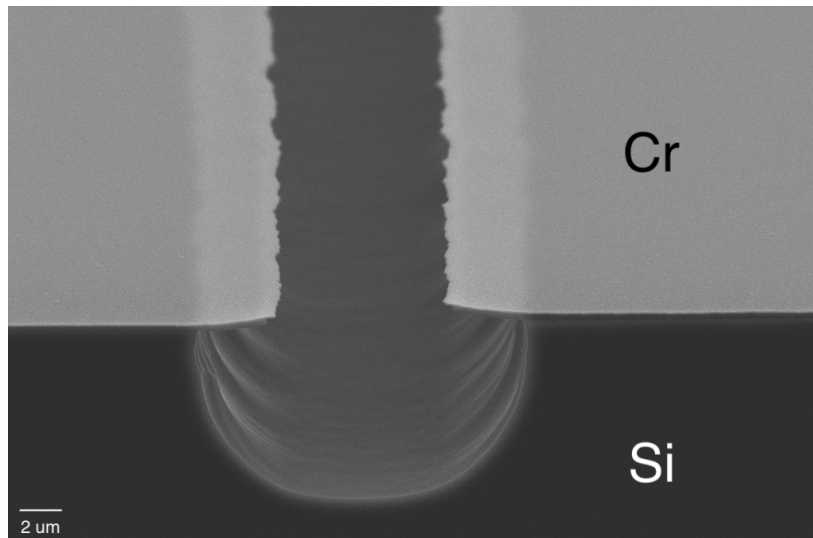
(a) 8 μm line (Chromium on silica mask).
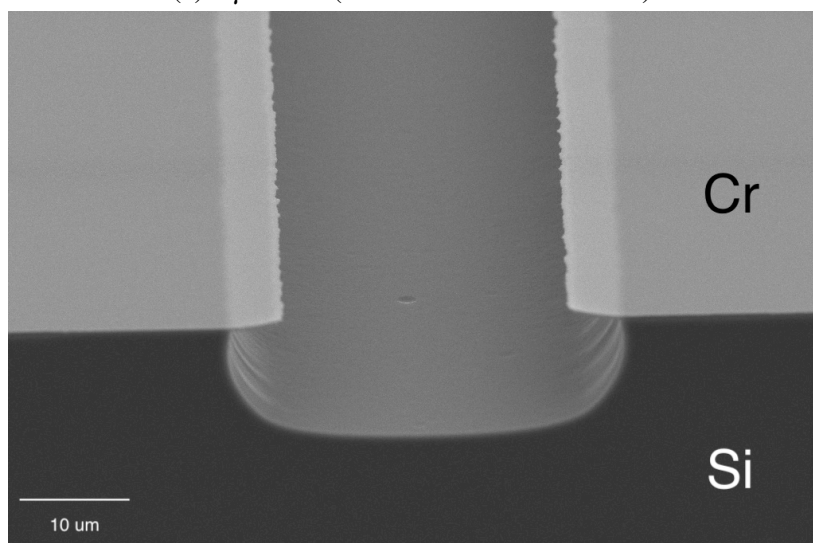
(b) 28 μm line (Chromium on silica mask).

Fig. 6.4 SEM images of the 8 μm and 28 μm lines after the isotropic etch (5 mins).
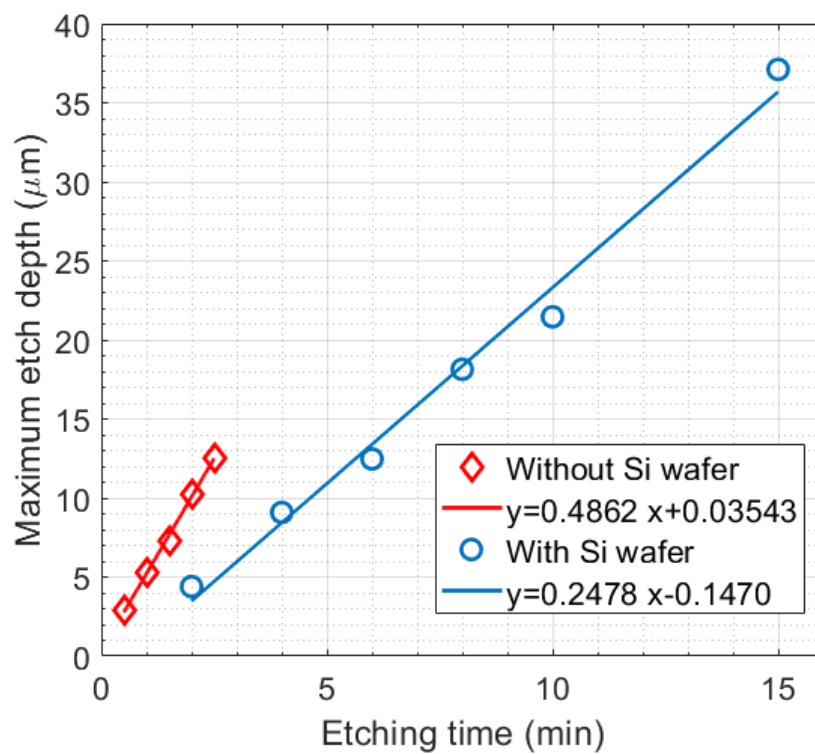
Fig. 6.5 Etch depth vs etch time with and without silicon carrier. It is clearly evident from the slope of the lines that the etch rate is much higher when the process is performed without the presence of the silicon wafer.

layers were completely stripped to reveal the entire silicon layer. The features were measure once again to obtain the post etch dimensions. The surface roughness measurements reported were conducted using a Veeco Atomic Force Microscope.

6.3   Results and Analysis

The results from Part 1 of the study are tabulated in Table 6.1 and illustrated in Figure 6.5. The etch rates are found to be in the range of 2.07 $\mu m/min$ to 2.47 $\mu m/min$. This is similar to etch rates achieved through the conventional dry isotropic etching of silicon i.e, the vapour phase etching using XeF_2 [70]. Though higher etch rates around 10 $\mu m/min$ have been reported [48], the typical etch rates range from 1 $\mu m/min$ to 3 $\mu m/min$ [70].

The surface roughness of the etch is presented in Table 6.2. It is evident that against the baseline roughness of the silicon (< 1 nm), the roughness initially rises. However, from the initial high, it slowly reduces with time, reaching its minimum value at 4 minutes, before increasing again. From the AFM scans of the etch (Figure 6.6), it can be seen that the initial roughness is evenly spread features with small amplitude. As the etch time increases, areas of these features consolidate into larger and smoother "scallops" of larger amplitude. The roughness associated with this etch is expected, due to its chemical nature, and can be undesirable in an optical context, for example leading to scattering.

Figure 6.5 also presents the etch rate obtained without the balancing effect of the carrier wafer. It is immediately clear that the etch rate without the presence of a silicon wafer is much higher than seen in Part 1. This is due to the decrease in the exposed silicon area. Though this offers higher etch rates, the presence of the wafer will ensure that the etch process is well defined and controllable, as the features on the chips will have a smaller overall impact on the etch.

In Part 2 of the study, the focus is on the effect of the feature geometry on parameters such as lag, aspect ratio dependent etching and isotropy. The vertical etch rates are presented in Figure 6.7, and the etch depth in the centre of the feature is shown in Figure 6.8. The etch rates range from 1.3 $\mu m/min$ to 2.6 $\mu m/min$, and it is clearly evident that the etch rate

(a) 2 minutes.

(b) 4 minutes.

(c) 6 minutes.

(d) 8 minutes.

(e) 10 minutes.

(f) 15 minutes.
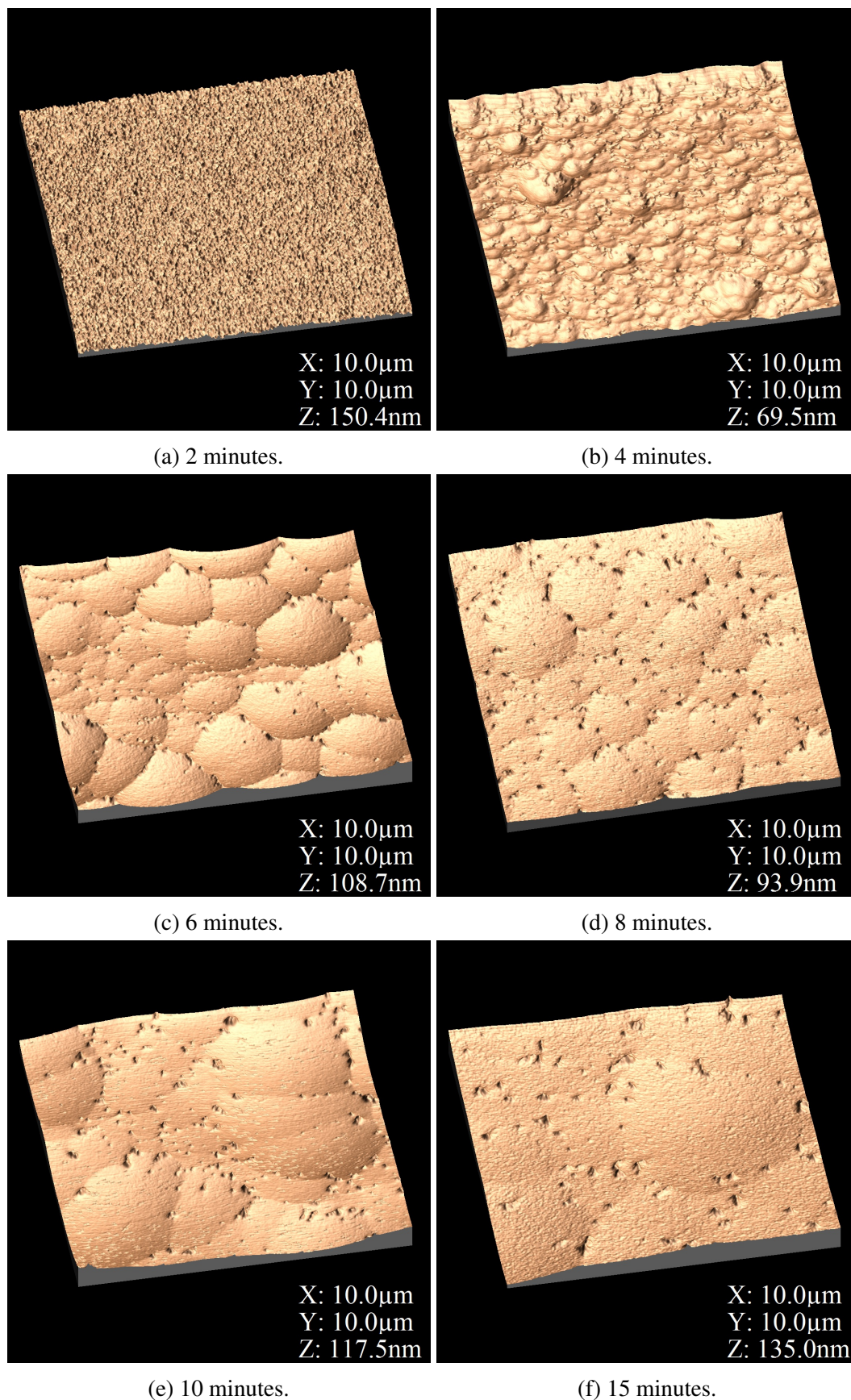
Fig. 6.6 AFM scans of the surface roughness for different etch times. The initial roughness is evenly spread with low amplitude. As the etch time increases, the features coalesce and form larger "scallops".
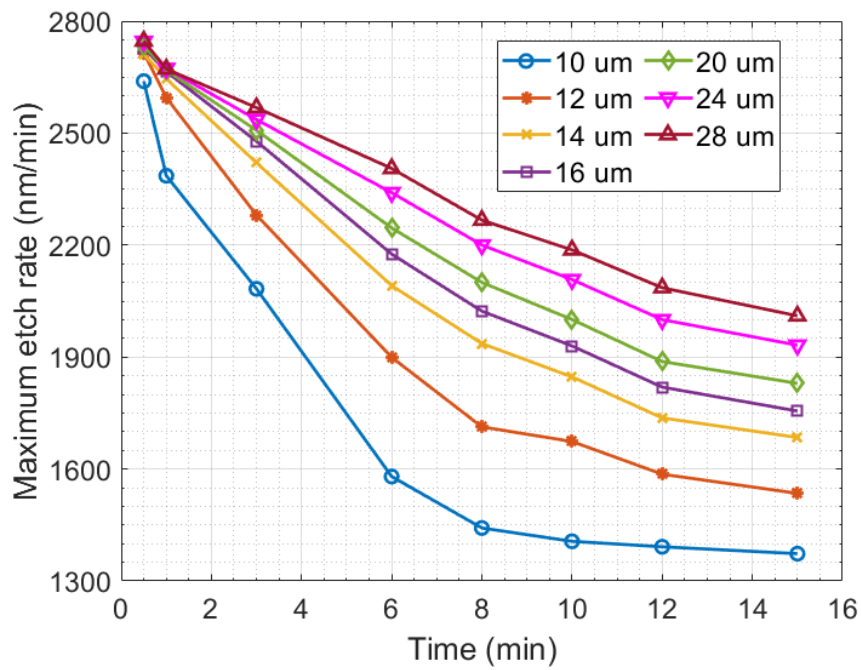
Fig. 6.7 Maximum etch rate vs etch time for pattern set 2.
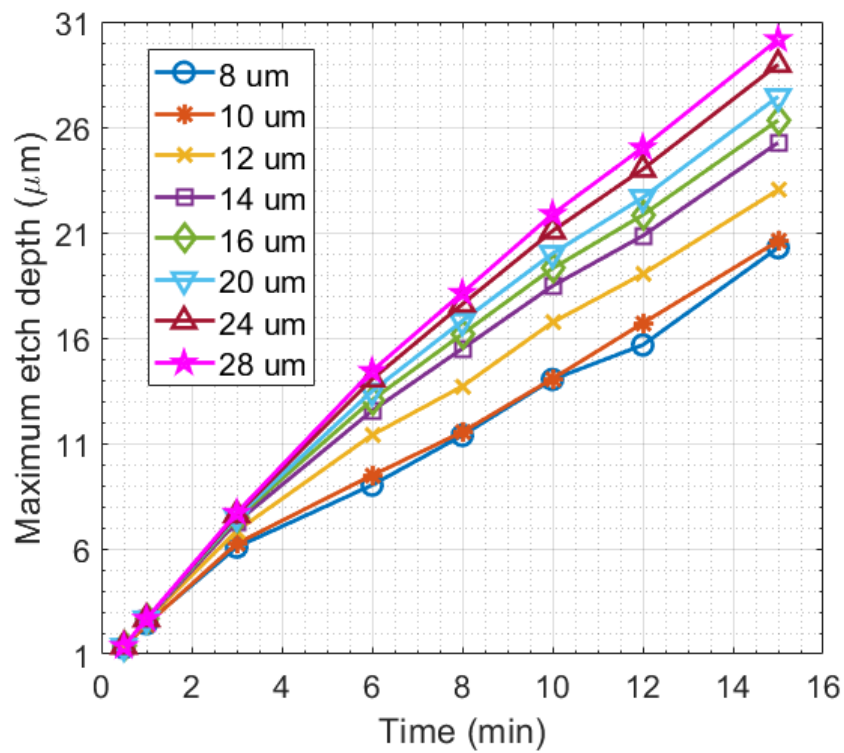
Fig. 6.8 Etch depth vs etch time for pattern set 2.
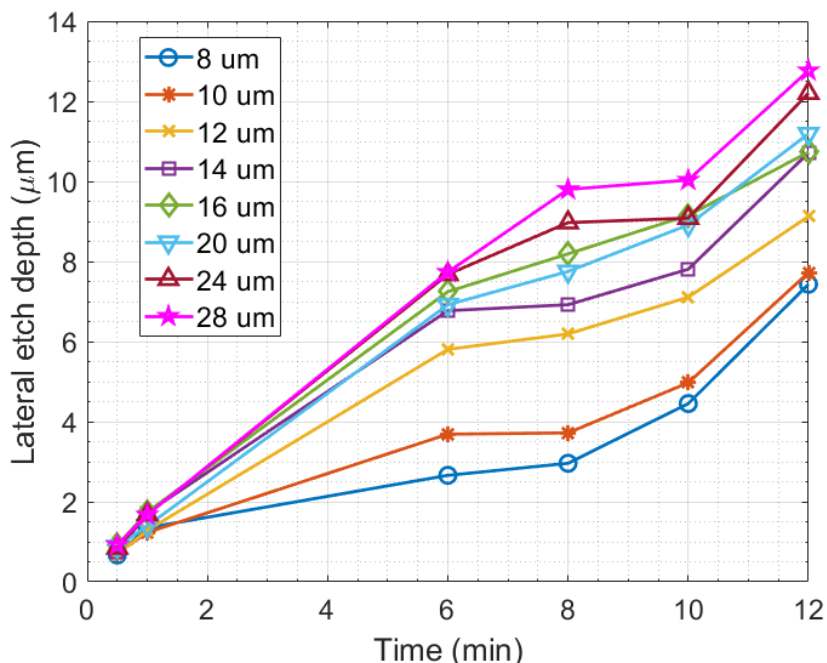
Fig. 6.9 Lateral etch depth vs etch time for pattern 2.

increases with the line width, due to the increase in the amount of flux that can enter the trench. As the etch time increases, the aspect ratio of the trench also increases, and it was found that the etch rate at the bottom of the features is much slower than the etch rate at the surface. This is due to the phenomenon generally referred to as "Aspect Ratio Dependent Etching (ARDE)" or "RIE lag". The etch rate (ER) at any point is given by [127]:

$$ER_{total} = ER_{thermal} + ER_{physical} + ER_{ion}. \tag{6.2}$$

Since this etch is completely chemical $ER_{physical} = ER_{ion} = 0$. Therefore the total etch rate is equal to $ER_{thermal}$ which is the etch rate due to the spontaneous etching of silicon by fluorine atoms in the absence of ion bombardment, and is given by [127]:

$$ER_{thermal} = k_0 \cdot Q_F \cdot exp\left(\frac{-E_a}{k_b T}\right), \tag{6.3}$$

where k_0 and k_b are constants, Q_F is the flux of the fluorine atoms, E_a is the activation energy and T is the absolute temperature. Therefore, at constant temperature, the etch rate is directly

proportional to Q_F. The etch rate at the bottom of a trench can be calculated using the following equation:

$$ER_{bottom} = \frac{Q_{F(bottom)}}{Q_{F(top)}} \times ER_{top}. \tag{6.4}$$

The relevant mechanisms that govern the flux at the bottom (in completely chemical etch with bias=0, i.e no energy and ionic component to the etch) are [90]:

1. Transport of neutrals

2. Neutral shadowing

3. Surface diffusion

4. Bulk diffusion

At the pressure level reported in this study, the mean free path of the particles (l) is in the range of millimeters, whereas the feature dimensions (d) are in the micrometer range. Therefore, the Knudsen number ($Kn = l/d$) is larger than one, indicating that particle-particle interactions are rare, and can be ignored. The particle-surface interactions are the dominant mechanism, and this dictates the neutral transport inside a feature. The neutrals strike the surfaces inside a feature, and are either scattered or react with the surface. The probability of this reaction S has been shown to be around 0.06 (for SF_6 in ICP plasma without RF bias) [121]. When the neutrals impinge upon the surface inside a feature, they lose all the directional information they possess [128], and the reflection angle follows the cosine law [127]. For example, in the case of DRIE (with passivated sidewalls), the sidewall reactions with the neutral can be considered to be completely inert, and the etch rate at the bottom of the trench is given by [129]:

$$ER_{bottom} = ER_{top} \times \frac{K}{K + S - KS}, \tag{6.5}$$

where K is the molecular flow transmission probability (dependent on the aspect ratio). However, since the sidewalls in our study react with the fluorine radicals, the above equation does not predict the etch rate accurately.

At the surface of the substrate, the neutrals are exposed to open field flux (which is the equal to the neutral angular distribution function (isotropic)). However, this is restricted inside a feature, due to neutral shadowing. This causes the surfaces without an open line of sight to have lower neutral flux. The etch rate due to the neutral shadowing effect can be estimated by assuming that the radicals are completely lost when incident on the sidewall surface [90]:

$$ER_{bottom} = v.S.Q_{F(top)}.sin\left[arctan\frac{A}{2}\right],\tag{6.6}$$

where v is the volume removed per reacting neutral and A is the aspect ratio of the feature.
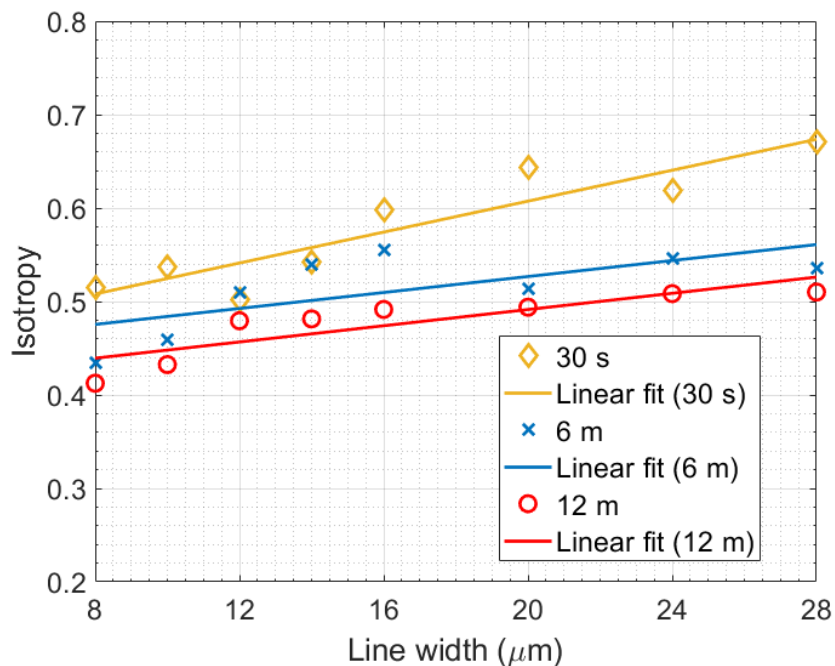
Fig. 6.10 Isotropy of the etch for a range of times vs line width.

Surface diffusion is the phenomenon where the radicals are adsorbed on the upper sidewalls, and diffuse along the surface of the etch profile [127]. This mechanism is not a prominent effect due to the geometry of the etch as well as the reactive sidewalls. Bulk diffusion is also a mechanism that can be ignored, due to the large mean free path and the dimensions of the etched features [90].

Figure 6.9 presents the lateral etch depth measured. It can be seen that the lateral etch rate increases with line width. The measurements in Figure 6.9 are accompanied by some noise due to measurement inaccuracies mainly arising from the mask roughness. From Figure 6.10, it can be seen that the degree of isotropy increases on the line width. This can be attributed to the fact that the amount of flux entering a trench is dependent on the trench width. As mentioned earlier, the neutrals that do not react with the bottom of the trench are reflected from the surface, therefore allowing them to react with the sidewalls. Hence, a larger volume of flux would lead to increased lateral etching, increasing the isotropy. The isotropy is also found to decrease with time due to the increase in the aspect ratio.

It is clear that the dominant etching mechanisms that determine the etch rate in the trenches are neutral transport and neutral shadowing. An exact prediction of the etch profile and rate could be attempted using the geometry of the structure and Monte-Carlo simulations.

6.4   Summary and Perspective

In this chapter we have carried out an in-depth investigation of the SF_6 isotropic etch characteristics, and we have demonstrated its use as a viable alternative to other isotropic etch processes. This method presents an opportunity to perform these etches to isolate membranes, release MEMS structures etc., without the need for specialised etching equipment. The etch rates achieved during the study demonstrate that the etch duration can be comparable or faster than the XeF_2 vapour etch process. In the next chapter, the effect of this chemistry on other materials such as silicon nitride, silica, NCD and polymers is analysed.

Chapter 7

Etch rates of various materials in ICP SF$_6$ and their selectivity to silicon.[1]

7.1   Introduction

As mentioned in the previous chapter, dry etching techniques have been explored and developed for isotropic etching in order to overcome issues associated with wet etching. We have described the characterisation of isotropic etching using SF_6 in the previous chapter. Due to the extent of the use of complementary materials in the design of devices, the effect of the etchants on these materials is necessary [63][130]. In this chapter, the etch rates of silicon dielectric derivatives, SiO_2 and Si_xN_y, polymeric materials (positive-tone photoresists ("PR"), negative-tone PR and the structural PR "SU-8"), and synthetic diamond (NCD) are studied.

As described in Chapter 4, NCD can be used along with silicon in various micro and nano structures due to its excellent thermal, mechanical, optical and chemical properties [107]. Suspended diamond structures have been demonstrated previously using wet chemical etching [131]. We have earlier described the design and fabrication of waveguides fabricated in NCD. It was found that the dimensions of the fabricated structure did not match the designed structure. It was postulated that the SF_6 plasma etching had an effect on the NCD

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[1]The work presented in this chapter is being prepared for publishing as a journal article.

surface, leading to etching and surface roughness. However, subsequent tests indicated that the a pure SF_6 ICP-RIE process had very little effect on the NCD surface.

7.2   Experimental methods

The materials included in this study are SiO_2, Si_xN_y, AZ-1505 positive-tone PR, AZ-nLOF 2020 negative-tone PR, SU-8 5 and NCD. The materials were prepared as described below:

- The SiO_2 film was grown by thermally oxidizing a silicon wafer to a thickness of $2\mu m$.

- A $400\,nm$ low-stress Si_xN_y film was grown on silicon substrate using an LPCVD (Low Pressure Chemical Vapour Deposition) reactor.

- The NCD film was grown to a thickness of $\sim 600\,nm$ in a CVD reactor then polished using CMP (Chemical Mechanical Polishing) to $\sim 6\,nm$ RMS roughness, as described by E.L.H. Thomas et al. [114].

- The AZ-1505 and AZ-nLOF 2020 photoresists as well as the SU-8 5 were spin-coated over the silicon substrates. After the spin coating, the AZ-nLOF 2020 and SU-8 films were UV cured (in a mask aligner).

The sample was chosen to be $1\,cm \times 1\,cm$ silicon chips, etched on a 4" silicon carrier wafer in order to mitigate the loading effect. All the samples were cleaned using the standard degrease process:

1. 5 minutes soak in methanol (with ultrasonic agitation).

2. 5 minutes soak in acetone (with ultrasonic agitation).

3. 5 minutes soak in isopropanol (with ultrasonic agitation).

4. 2 minutes rinse in flowing DI water.

5. Blow dry with nitrogen gun.

6. 10 minutes dehydration bake at 250 $^\circ C$.

In the case of the polymer samples, the cleaning step was performed before the spin coating.

A 100 nm layer of chromium was sputter-coated using a Leybold 350 system, in order to form the etch mask. The mask chosen was a set of 8 500 μm diameter circles separated diagonally across each chip by 990 μm gap. The circular patterns were defined in a 500 nm thick AZ-1505 positive-tone PR, exposed with a Hg broadband UV illumination bulb and finally developed in a diluted AZ-726 MIF developer (2:1 developer:DI water) solution. The patterns were transferred to the chromium mask using the commercially available CR-7 chromium wet etchant.
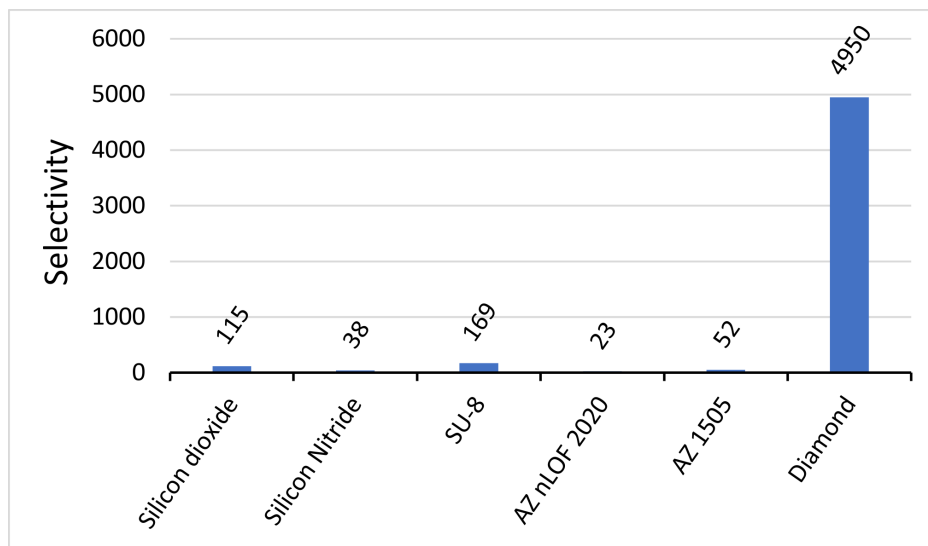
Fig. 7.1 Selectivity of silicon over tested materials in SF_6 ICP etching.

The prepared samples were etched using SF_6 in an ICP-RIE OXFORD PlasmaPro 100 Cobra^{300} machine. Different etch times between 5 and 15 minutes were chosen for all materials, except the NCD sample. The NCD etch times were varied between 30 and 90 minutes, due to the material's high resistivity against SF_6 plasma. The samples were all etched using the same etch recipe. The chamber pressure was set to 30 mT, and the substrate temperature to 20 $^\circ C$. The ICP power was 2000 W with a bias of 0 V. Finally, the SF_6 flow rate was set to 50 sccm. The samples were fixed to the surface using Teflon tape on the edges.

SiO$_2$	Si$_x$N$_y$	AZ-1505	AZ-2020	SU-8	NCD
19.13	58.54	42.2	94.4	13	0.44

Table 7.1 Etch rates (nm/min) of tested materials in SF_6 ICP etching

7.3 Results and Discussion

The etch rates of the tested materials are reported in Table 7.1. Since this etch is completely chemical in nature, the etching is due to the neutrals rather than the ions which are common in most RIE processes. Specifically, NCD shows exceptionally low etch rate, which can be attributed to its inertness and high chemical resistance. Dry etching of diamond is performed using mainly oxygen and/or fluorine-containing chemicals in RIE reactors [132][99][133][76]. The reaction between the carbon atoms in the diamond crystal lattice and the oxygen/fluorine atoms requires the catalytic assistance of the energetic ions' impingement. Without the presence of the energetic ions, this reaction is not triggered, and therefore the etch rate of NCD is very low.

(a) Before etch.

(b) After etch.
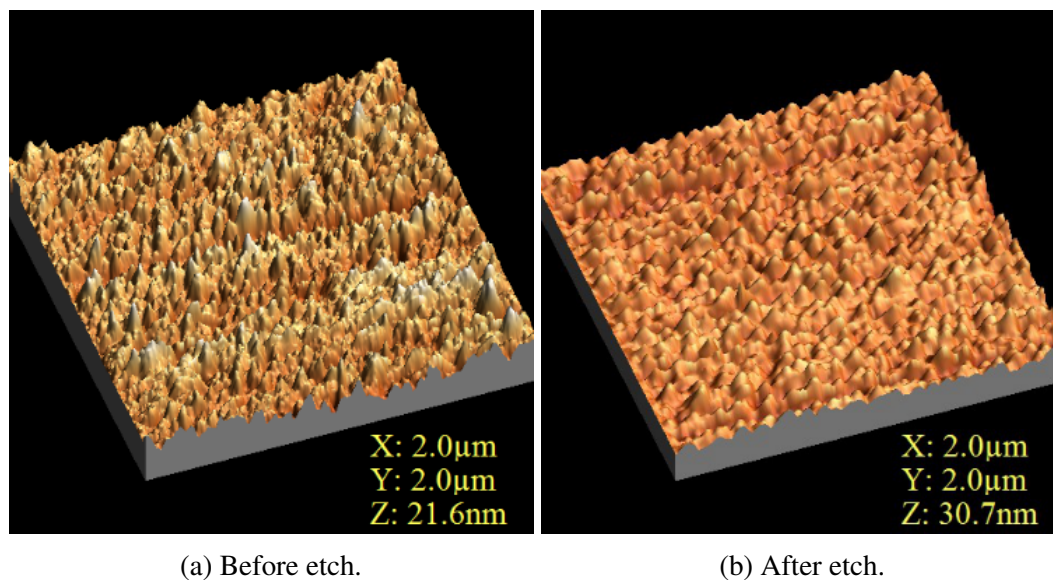
Fig. 7.2 AFM profiles of Si_xN_y before and after 10 minutes of ICP SF_6 etching showing the slight increase in roughness.

The Si_xN_y etch rate in SF_6 ICP is 3-times faster than the etch rate of SiO_2. The nitride atoms in the Si_xN_y layer react with the fluorine atoms in the SF_6 plasma to produce nitrogen trifluoride (NF_3) [63]. On the other hand, the oxygen atoms in the SiO_2 film require the presence of another element [63] (e.g. carbon) in the plasma to react with. Therefore, the ionization and removal of the oxygen atoms from the film delays the etching process.

The three polymeric masks, AZ-1505, AZ-nLOF 2020 and SU-8 5, showed very different etch rates in SF_6 with SU-8 5 being the most resilient with an etch rate of $13\,nm/min$ and the negative-tone PR AZ-nLOF 2020 being the least resilient with an etch rate of $94.4\,nm/min$. The slow etch rate of SU-8 5 was expected due to the strong cross-linking of the exposed polymer. Surprisingly, the positive-tone PR showed higher resistance to the plasma than the cross-linked negative-tone PR. This could be a specific result for these two PRs, where the links in the exposed AZ-nLOF 2020 PR are weaker than their counterparts in the unexposed AZ-1505 PR.

(a) Before etch.$\qquad$(b) After etch.
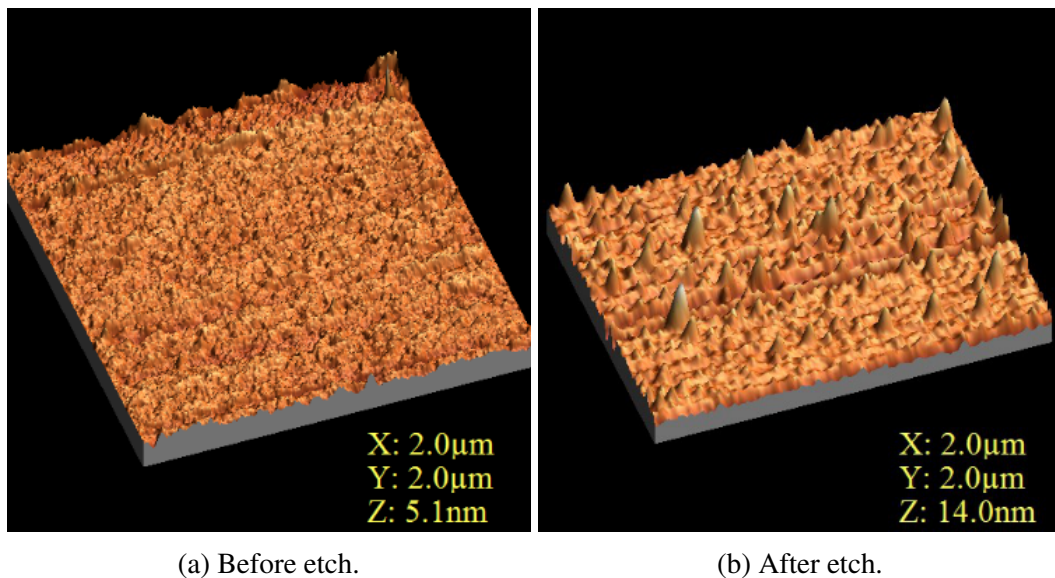
Fig. 7.3 AFM profiles of SiO_2 before and after 10 minutes of ICP SF_6 etching. The increase in the amplitude of the features can be clearly seen.

Since the tested materials are either etch masks during SF_6 ICP processing of silicon, or would co-exist with silicon during etching, their selectivity against silicon is presented in Figure 7.1. The silicon etch rate obtained in the previous chapter was used to calculate the

results in Figure 7.1. It can be discerned that Si_xN_y is not an ideal choice as an etch mask for this process, as the photoresists have etch rates that are comparable to the nitride etch rates, along with being much easier and faster to pattern. If the design consists of nitride structures, they would have to be protected during the etch. The same applies to SiO_2 structures as well. However, as shown later, SiO_2 maintains a relatively smooth surface after SF_6 ICP etching. Hence, it can be etched simultaneously with silicon without compromising its operational parameters (for example in the fabrication of optical waveguides).

(a) Before etch.   (b) After etch.
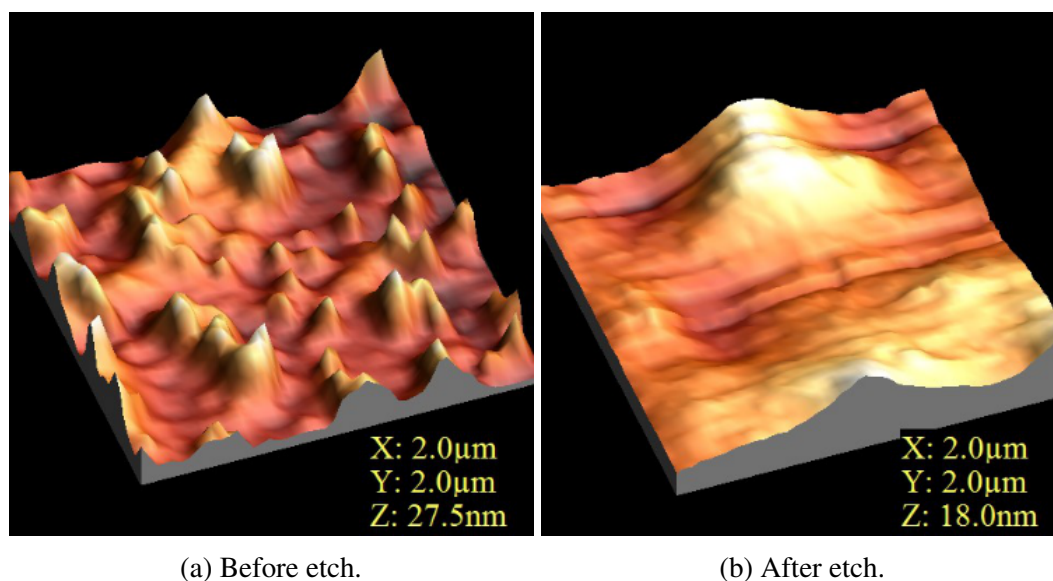
Fig. 7.4 AFM profiles of NCD before and after 10 minutes of ICP SF_6 etching. The decrease in the roughness is visible.

It can also been seen that the selectivity of NCD over silicon is exceedingly high. As a result of this, suspended diamond membranes over silicon substrates can be created without the need of protective layers. Conventionally, polymeric layers (such as resists) or metallic layers (such as chromium) are used as protective layers for dry etching. Polymer layers can be removed either through wet etching (which can compromise the integrity of the suspended diamond membrane), or oxygen plasma etching (which reacts with diamond, and leads to etching). Metal removal is generally performed through wet etching. As NCD was found to be very resilient in this etch chemistry, no protective coating would be required for silicon undercutting, therefore simplifying the fabrication process.

	SiO$_2$	Si$_x$N$_y$	AZ1505	AZ2020	SU-8	NCD
Before etch	0.3	2.4	0.5	0.4	0.4	4.6
After etch	1.1	2.5	2.6	1.9	2.7	3.1
% increase	267	4	420	375	575	-33

Table 7.2 RMS roughness (*nm*) before & after 10 mins of SF_6 ICP plasma etching for all materials and 1hr for NCD, and the % increase in RMS surface roughness

A parameter of importance during plasma etching is surface roughness. Table 7.2 presents the RMS surface roughness before and after 1 hour of SF_6 ICP etching for NCD and 10 minutes for the rest of the materials. It also shows the percentage change in surface roughness after etching. It was found that the surface roughness increased for most materials, ranging from 4% for Si_xN_y, to 575% for SU-8. The surface roughness of NCD, however, decreased during the course of the etch.

(a) Before etch.   (b) After etch.
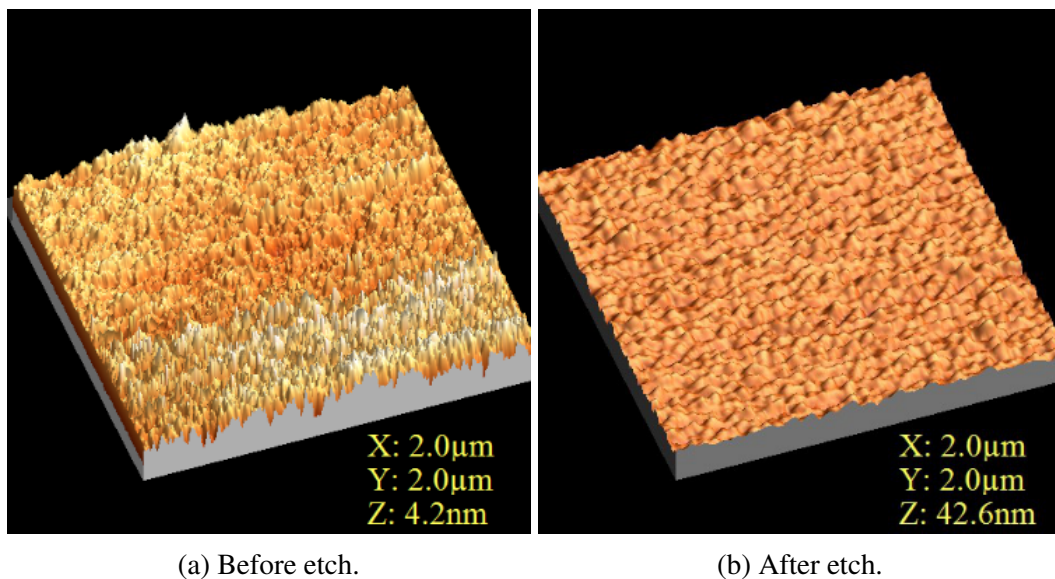
Fig. 7.5 AFM profiles of AZ-1505 before and after 10 minutes of ICP SF_6 etching showing the increase in the amplitude of the features.

The RMS roughness increase for the AZ-1505 and AZ-nLOF 2020 resists was about 500% the initial surface roughness. The surface roughness for both resists was found to be uniform, without any exceptionally high or broad peaks, as depicted in Figure 7.5 and Figure 7.6. The etch rate of the SU-8 layer was found to be 13 *nm*/*min*, and the surface

roughness was 2.44 nm. As a result, the layer remained relatively unaffected by the isotropic silicon etching. As shown in Figure 7.7, SU-8 films exposed to SF_6 ICP etching show uniform surface roughness with no irregularly large peaks or troughs.

(a) Before etch.　　　　　　　　　　　　(b) After etch.

Fig. 7.6 AFM profiles of AZ-nLOF 2020 before and after 10 minutes of ICP SF_6 etching. The increase in roughness can be clearly seen.

As SF_6 etches Si_xN_y readily, the nitride layer exhibits a higher etch rate in the plasma than the polymers or SiO_2. The etch rate of Si_xN_y was found to be 58 nm/min, and the surface roughness increased marginally, as seen in Figure 7.2. In the case of SiO_2, the surface roughness was found to increase from 0.3 nm to 1.1 nm. However, this value is within the acceptable limits for a vast range of applications including optical wave guiding. Although the RMS roughness of etched SiO_2 is low, the etch was associated with the formation of "spikes" on the surface, as shown in Figure 7.3.

As mentioned earlier, due to the fact that the NCD layer has a very low etch rate during the etch, it does not require a protective coating during the etch. However, for certain applications such as nanophotonics, which are highly sensitive to surface roughness, the etch roughness generated from the process is more critical than the etch rate, as the etch resilience can often be mitigated during the fabrication process design. It has been demonstrated previously [133] that reactive ion etching is a viable polishing technique after CMP for diamond films.

Therefore, it was expected that the NCD surface roughness would decrease after the etch. It was found from the study that the RMS roughness after one hour of SF_6 ICP etching was reduced by 33% (from 4.6 nm down to 3.1 nm). Due to its excellent selectivity versus silicon and the decrease in surface roughness, this process can be used to create suspended NCD structures on silicon substrates.

(a) Before etch. (b) After etch.
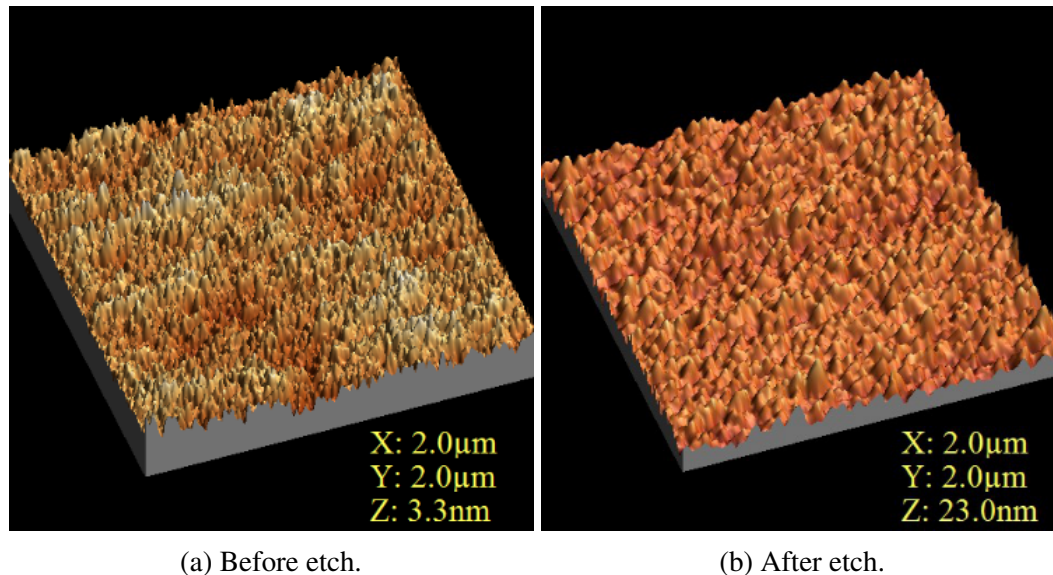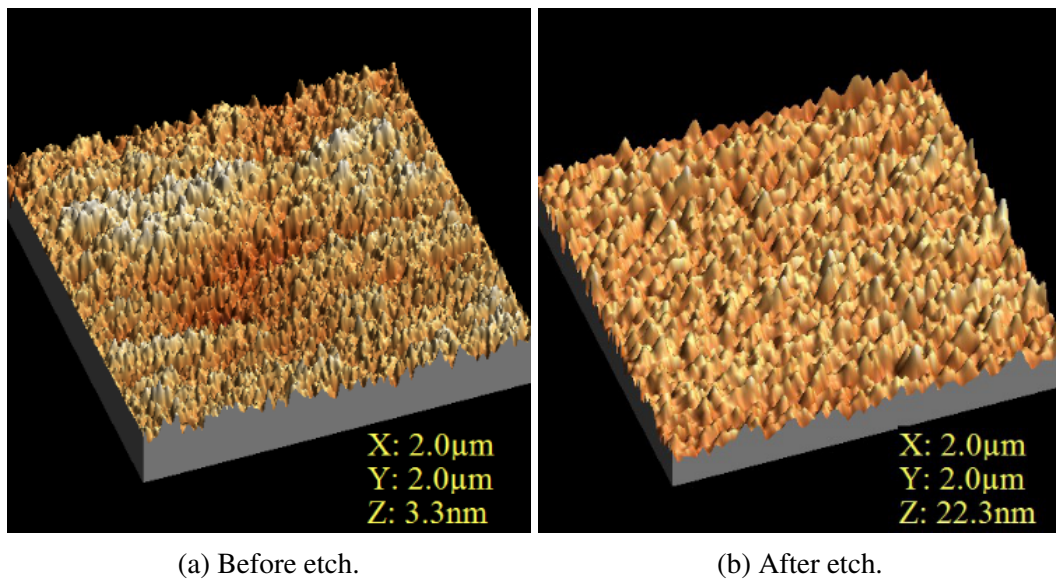
Fig. 7.7 AFM profiles of SU-8 before and after 10 minutes of ICP SF_6 etching. The increase in roughness can be clearly seen.

It can be seen from the AFM scan of the NCD surface, that after 60 minutes of SF_6 ICP etching, the overall surface becomes smoother, except for a few broad peaks (Figure 7.4). This clearly demonstrates the polishing behaviour of the etch. It was found that before the etching, the NCD surface contained multiple sharp peaks with maximum roughness of 27.5 nm. However, after the etch, the roughness of the surface decreased to a maximum value of 18 nm, with the few broad and smooth peaks dominating the surface. The AFM scans establish that the SF_6 ICP plasma etching reduces the number of roughness peaks, RMS roughness and the maximum roughness values, and therefore can be considered a feasible method of NCD surface polishing.

7.4   Summary and Perspective

In this chapter the effect of SF_6 ICP plasma on other materials such as silicon nitride, silica, NCD and polymers is analysed. This has not be reported earlier, and is crucial in the context of this thesis, as the materials studied in this chapter are often used along with the optical material of choice. The behaviour of the materials during the etch was largely as expected, with silica and silicon nitride exhibiting significant etch rates. The polymers were also affected by the fluorinated plasma, with SU-8 being the most resilient. NCD proved to be the most resilient material, offering a selectivity of 5000:1 vs silicon. It was also found that the roughness of the NCD surface decreases after the etching process. This result in particular is of significance as it shows that NCD can be used as an optical or masking material without necessitating further protection. Also, this process can be used as a polishing step in order to reduce the scattering losses when using NCD as an optical material.

Chapter 8

Fabrication of a suspended membrane through bonding

In the earlier chapters, we have presented a design and process to fabricate suspended structures, i.e. top down isotropic etching. An alternative method is presented in this chapter through a novel chip-scale bonding technique. This technique enables the integration of other structures on the chip (such as micro-resonators) which otherwise is challenging. Another advantage of this method is the flexibility that is offered; as the two chips are bonded, the thickness of the bonding material can be varied to accommodate design requirements. Here, a step-by-step process used for the fabrication of such a device is presented.

As the final device is formed by bonding two separately processed chips, the fabrication can be easily described by the processes performed on the top and bottom chips individually. An important design consideration for the fabrication process of this device is the choice of materials. As the process includes various wet and dry etching steps, the other materials used have to remain unaffected.

The substrate of choice for the bottom chip was thermally oxidised silicon chips. The oxide layer acts as a structural under-layer for any mask material that is used. Various substrate materials were considered for the top chip. Silicon nitride on indium phosphide
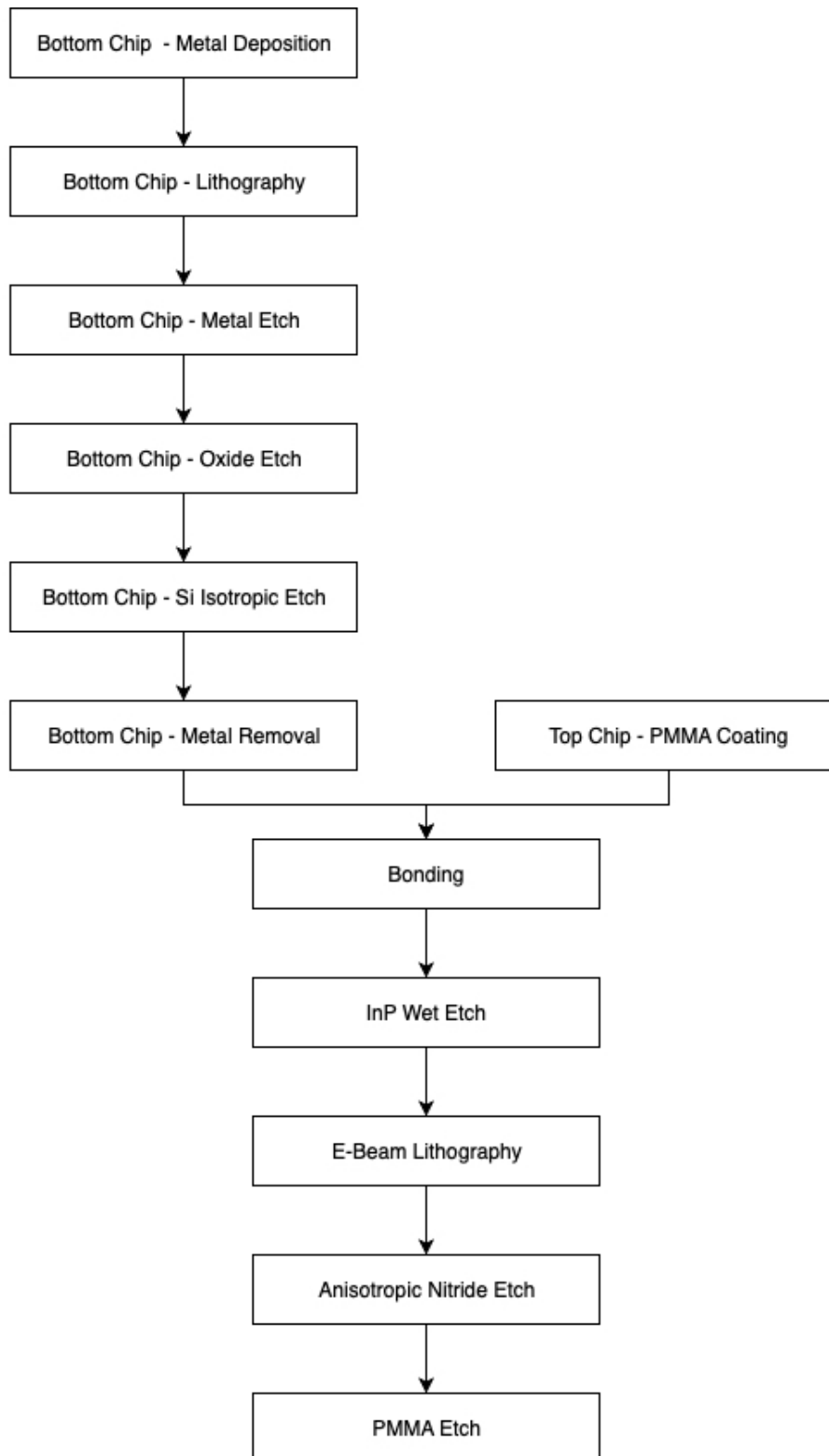
Fig. 8.1 Overview of the bonding process.

(*InP*) was chosen for the top chip due to the relative ease of wet etching the *InP* layer and growing the nitride layer. The entire fabrication process is presented in Figure 8.1.

8.1 Lower chip fabrication

(a) Oxidised silicon chip.

(b) With patterned chromium mask.

(c) After oxide and isotropic Si etch.

(d) Post chromium etch.
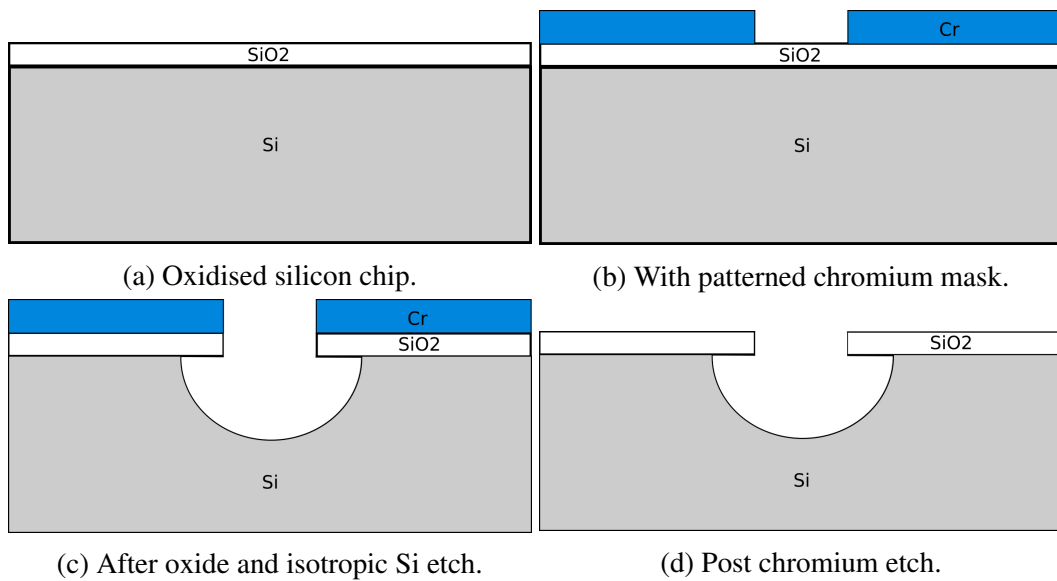
Fig. 8.2 Bottom chip processing.

The lower chip size was chosen to be $1 \, cm \times 1 \, cm$. The metal mask layer can then be patterned using photolithography through two main methods: lift-off lithography and metal etching. In the lift-off process, the metal layer is deposited over a patterned photoresist layer. This photoresist layer is "lifted-off" through resist removal (often using ultrasonic agitation), removing the metal covering the resist surface. The area not covered with resist is therefore covered in metal. This is a widely used technique and is especially useful for patterning intricate features. Lift-off requires the resist profile to be either vertical or have a strong undercut to prevent the sidewalls being coated; special resists (such as AZ nLOF series and the LOR series) have therefore been developed. The other technique, metal etching, is easier to achieve and enables patterning thicker metal layers. In this process, the metal layer is deposited before the photoresist layer. After exposing and developing the photoresist, the metal layer is etched using chemical etchants.
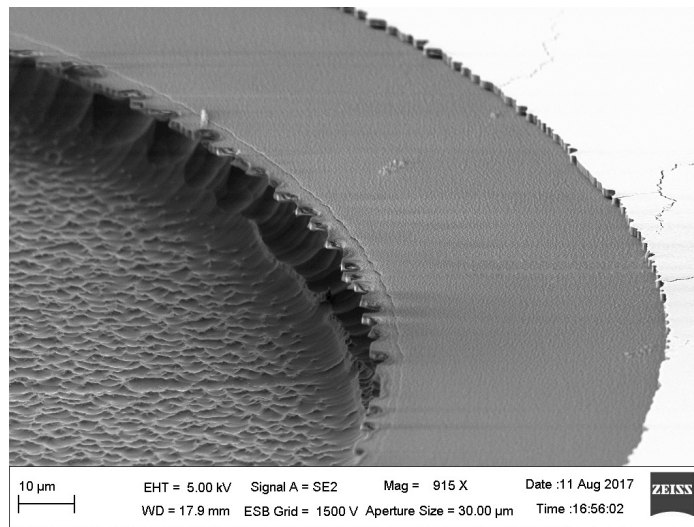
Fig. 8.3 Silicon undercut for the bottom chip.

For the process described in this chapter, the mask material chosen was chromium, as it is widely available and offers very good selectivity in hydrofluoric acid [134]. The lower chip was initially covered with a chromium layer in order to form an etch mask that can be used to pattern both the oxide and the silicon layers. 60 *nm* of chromium was deposited using sputtering at $2 \times 10^{-5} mbar$ and 250 W RF power. The working principle of this process has been described in Chapter 2. The thickness was verified through profilometry over a thickness monitor.

A positive resist, AZ 1505, was chosen to pattern the metal layer. The pattern chosen was a series of circles of diameter 500 *μm*, as it can be easily etched isotropically. Once the pattern was developed, the underlying chromium layer was etched using a commercially available etchant called "CR-7" (Figure 8.2b), which is a combination of ceric ammonium nitrate $((NH_4)_2 [Ce (NO_3)_6])$ and perchloric acid $(HClO_4)$. The etch rate of this etch is roughly 1 *nm*/*min*. Following the chromium etch, the oxide layer under the *Cr* mask can be wet etched. Hydrofluoric acid (HF) is commonly used to etch oxide. It is an extremely hazardous chemical that aggressively etches most materials [56]. In order to reduce the etch rate, as well as to control the lateral etch rate, Buffered Oxide Etch (BOE) is used. BOE is a mixture of a buffering agent and HF, and is available in different concentrations. The BOE

used in this study was a 7:1 mixture of 40% ammonium fluoride (NH_4F) and 49% HF, and has an etch rate of approximately 100 nm/min.

The exposed silicon was etched in an ICP-RIE, an Oxford Instruments PlasmaPro 100 Cobra[300]. The chamber pressure was set to 30 mT, and the substrate temperature to $20°$ C. The ICP power was 2000 W with a bias of 0 V. Finally, the SF_6 flow rate was set to 50 sccm. Since the bias is set at 0 V, this etch is completely chemical in nature, and therefore results in an isotropic profile(Figure 8.2c and Figure 8.3). A more detailed study of this etch is reported in Chapter 6. After the etch, the resist was removed using MICROPOSIT remover 1165 (with agitation) and the remaining chromium was etched using CR-7 (Figure 8.2d).

8.2   Top chip fabrication
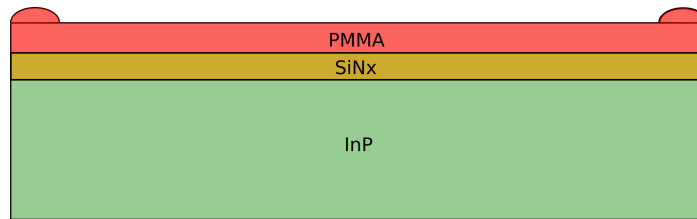
Fig. 8.4 Top chip with PMMA.

As mentioned earlier, the top chip comprises of approximately 300 nm of silicon nitride over indium phosphide (InP). The size of this chip was chosen to be 1.4 $\mu m \times$ 1.4 μm, so that the edge beads are not in contact with the lower chip during the bonding step. This is illustrated in Figure 8.5 and Figure 8.6. The chip was spin-coated at 2000 rpm for 45 seconds with 950 PMMA A, which will be the layer used to bond the two chips. It was soft-baked for 60 seconds at $180°$ C as recommended by the data sheet. This resulted in a layer around 1.8 μm thick at the center, with the edge beads between 2.2 μm and 2.4 μm thick (Figure 8.4).
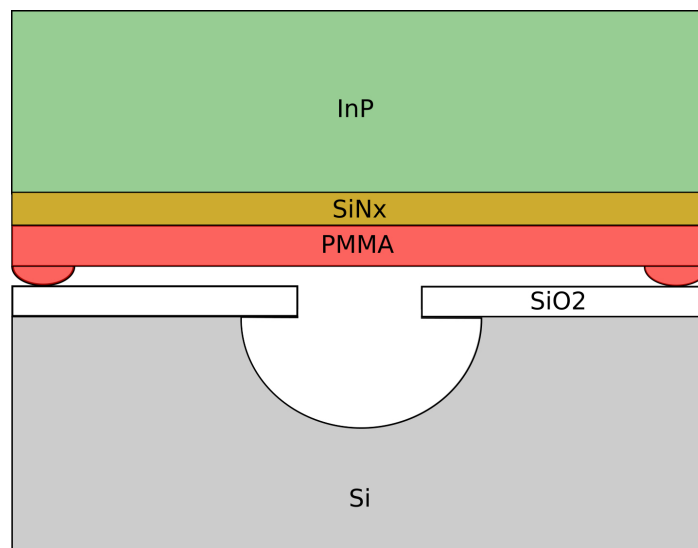
Fig. 8.5 Imperfect bond formed due to edge bead.

8.3   Chip scale bonding
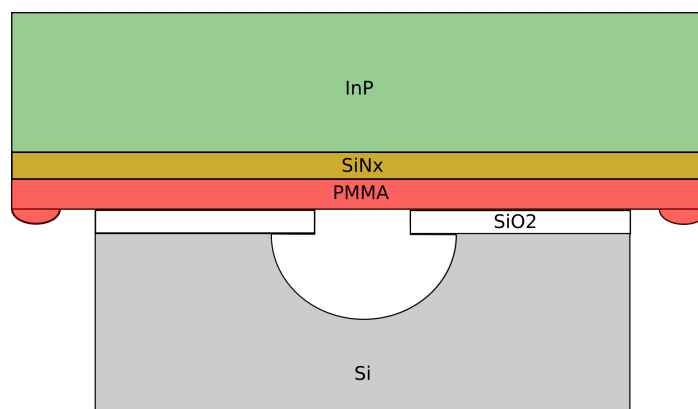
Fig. 8.6 Bonding using larger top chip.

Various techniques for bonding have been demonstrated, including direct hydrophilic wafer bonding [135] and vacuum bonding [136]. Other methods make use of a bonding layer including SU-8 [137], Epoxy [138] and PMMA [139]. Since the bonding process reported here was designed for a chip scale fabrication process, PMMA bonding using a bonding machine was challenging due to alignment issues. Also, because of the extremely brittle nature of *InP*, the chips cracked under pressure. Epoxy bonding using EPO-TEK 301 was

also explored; however, this process introduced a large amount of air bubbles in the bonding layer which could not be completely eliminated. The method presented by Eaton and Risbud in [140] delivered the best results. In this method, instead of applying pressure over the complete chip surface, localised pressure is applied. The steps involved in this process are presented below:

1. Bake the PMMA coated chip at $180°$ C for 15 mins.

2. Place the other chip over the PMMA coated chip carefully, ensuring that the PMMA edge bead is completely avoided.

3. Immediately place the two chips on to a hotplate set at $160°$ C.

4. Apply localised pressure over the backside of the chip using a ball-point pen covering the entire surface.

5. Bake the bonded chips at $160°$ C for 5 mins, and slowly cool down.
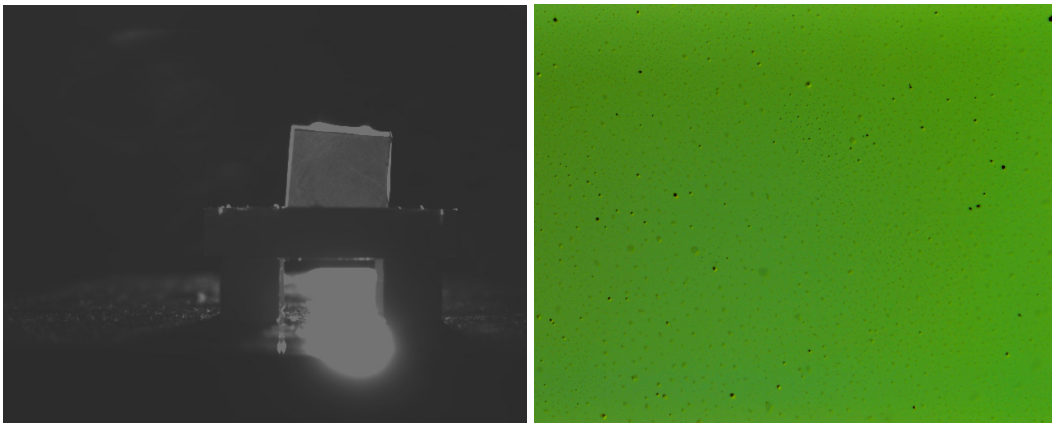
(a) IR image of bonded chip. (b) Bond between a glass chip and a Si chip.

Fig. 8.7 The images used to determine the bonding quality. The lack of voids in the bonding layer can be seen in the IR image. The quality of the bond between the glass and the silicon chip can seen with no visible defects.

8.4   Bonded chip fabrication

(a) After InP etch.

(b) The overhanging parts of the wafer broken.

(c) After E-beam patterning.

(d) After anisotropic nitride etch.

(e) PMMA anisotropic etch.

(f) PMMA isotropic etch.
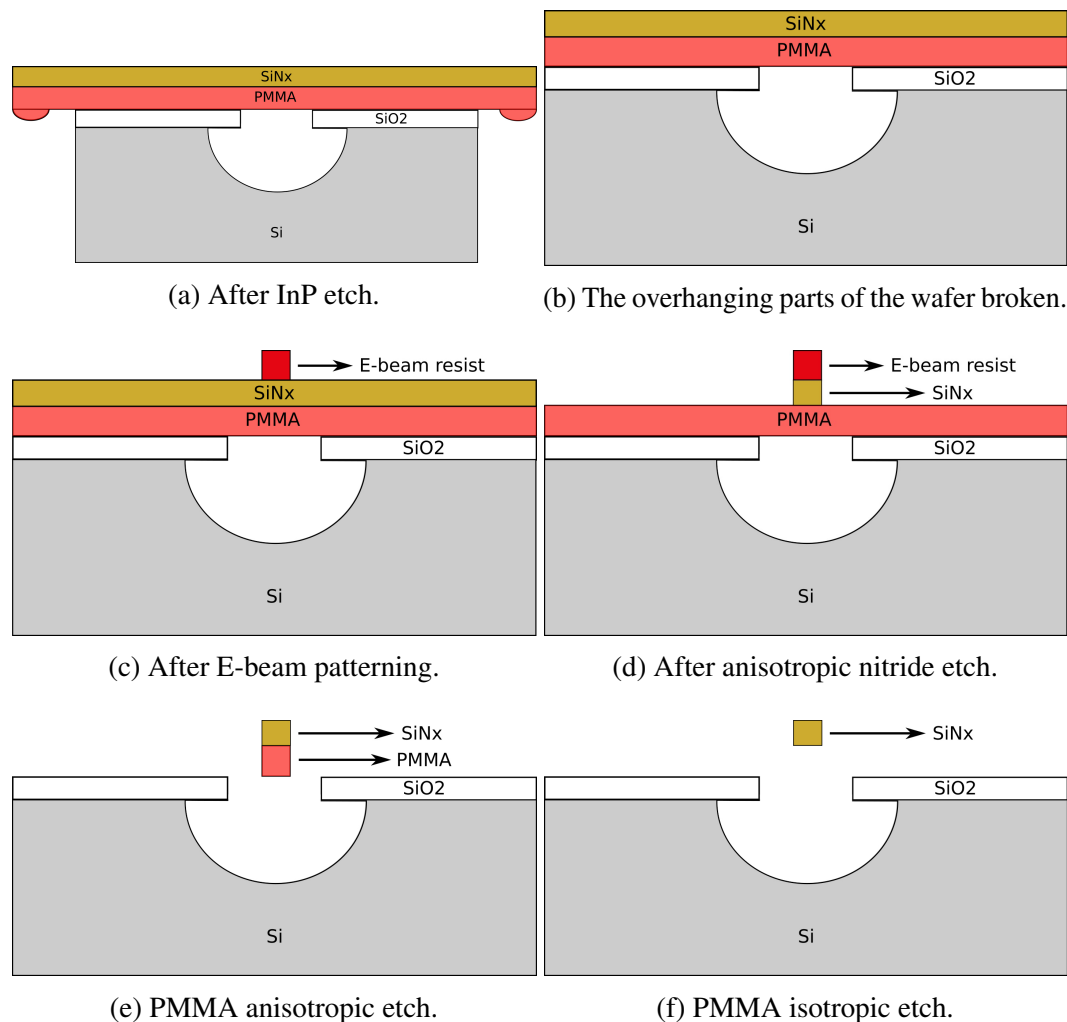
Fig. 8.8 Bonded chip processing. The advantage of using a larger top chip can be seen. The E-beam resist is applied and patterned following the InP etch. The nitride layer is then etched anisotropically, after which the PMMA layer can be etched either anisotropically or isotropically.

Once the chips are bonded, the next step involves removing the *InP* layer through wet etching. The chip was placed with the *InP* layer facing upwards in hydrochloric acid, etching the layer completely in around 1 hour. The unsupported parts of the PMMA and the nitride layers are removed during the rinsing process.
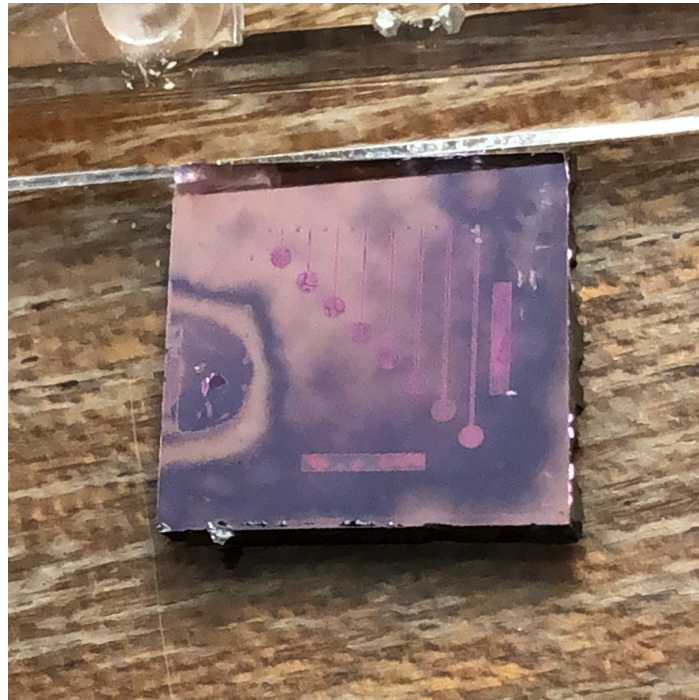
Fig. 8.9 An image showing the suspended nitride membrane over voids with the venting ducts visible. The entire surface of the chip is covered in PMMA and nitride, and can be patterned using E-beam or optical lithography.

The main issue is the air trapped in the voids during the bonding process. This can lead to problems such as membrane de-lamination as well as membrane rupture during vacuum processing. One way to overcome this issue is by lithographically defining venting ducts that lead to the edge of the chip.

Since the nitride and PMMA layers are directly over the voids in the silicon layer, a test pattern was written using E-beam lithography in order to ensure that the features do not get distorted due to charging effects (Figure 8.11). The patterned nitride layer was completely etched anisotropically in a RIE system. A detailed study of this etch is presented in Chapter 4.

The underlying PMMA layer can also be etched using RIE. The recipe used for the etch is presented in Table 8.1. The entire bottom chip fabrication process is shown in Figure 8.8
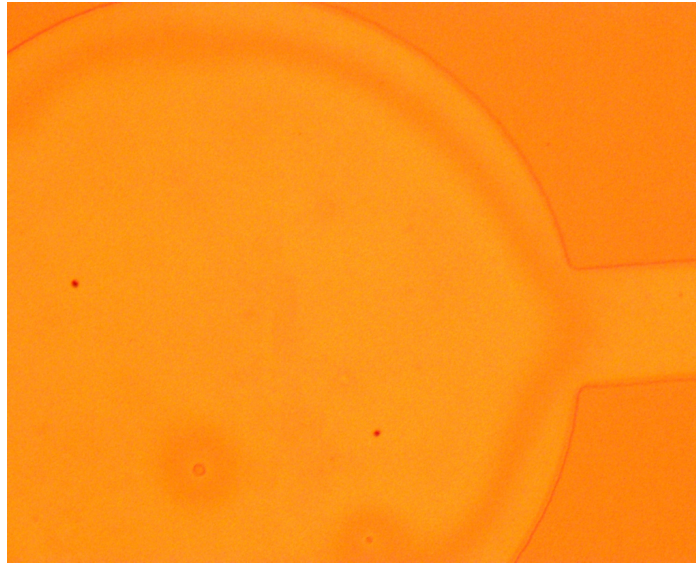
Fig. 8.10 An optical image of the bonded membrane over a void showing the bonding quality.
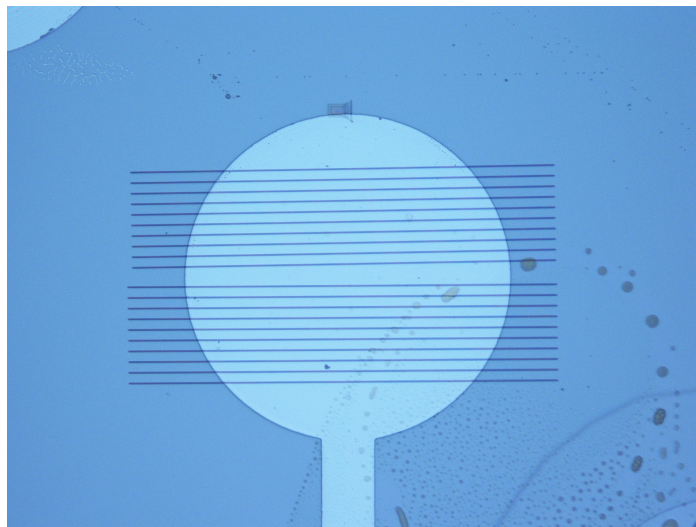
Fig. 8.11 E-beam patterns over void. The features show no distortion.

O_2 (*sccm*)	RF Power (*W*)	Pressure (*mTorr*)	Time (*min*)
40	200	80	20

Table 8.1 PMMA etch parameters

Figure 8.12a shows the fabricated chip, with the anisotropic removal of PMMA. The PMMA layer under the nitride structure is clearly visible. In Figure 8.12b, the PMMA was removed using isotropic etching of PMMA, and the hanging nitride membrane can be seen suspended over the void.

(a)   (b)
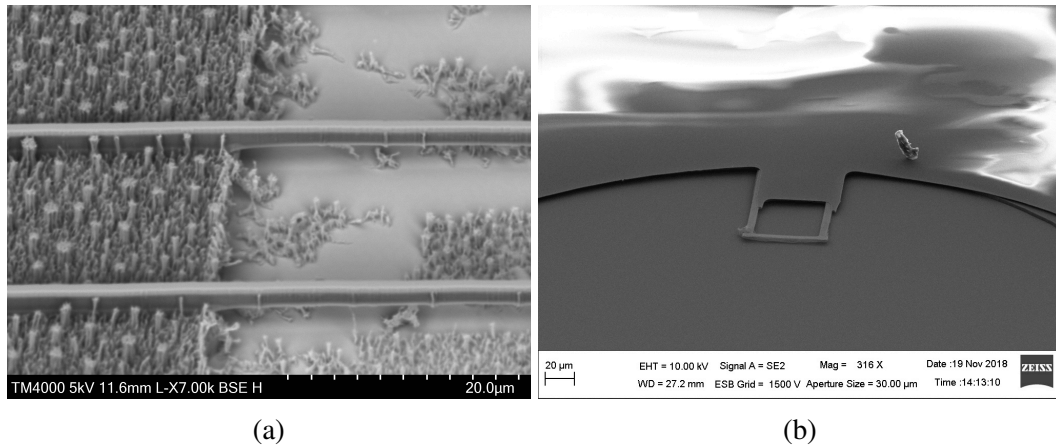
Fig. 8.12 Suspended structures over void.

8.5 Summary and Perspective

In this chapter, a novel bonding process has been presented, along with the steps required to fabricate a suspended structure. As mentioned earlier, this method has some advantages over the etching approach including allowing the use of a wider range of materials as well as greater MEMS tuning flexibility. However, some considerations have to be made before using this approach, including the correct choice of materials. Various bonding techniques were tried, and the best results were obtained by the application of localised force using a ball point pen.

Chapter 9

Conclusion

In this work, we have explored the design and fabrication of suspended structures and membranes, along with studying the etching processes in detail.

In Chapter 2 and Chapter 3, the fundamental background used in the thesis was presented. In Chapter 4, the anisotropic etching of silicon, silicon nitride and diamond was studied, with the fabrication of waveguides as the focus. For the silicon etching, fluorine based etchants were chosen due to their wide availability and versatile nature. Two different gas mixtures were used, a $SF_6 : CHF_3 : O_2$ mixture and a $SF_6 : CHF_3$ mixture. In the case of the former, a process known as the Black Silicon Method was used to "engineer" the etch. In the case of the latter, the flow rates of the two gases were varied to arrive at the optimal recipe. Satisfactory results were obtained through both chemistries. The $SF_6 : CHF_3$ mixture resulted in a better profile; however, because of its low selectivity, it can be used only to etch shallow features or if the mask thickness is very high. The $SF_6 : CHF_3 : O_2$ mixture resulted in a good compromise between the selectivity and the profile. The anisotropic etching of low stress silicon nitride was also studied and the ideal etch parameters were found. Though the addition of O_2 to CHF_3 is often recommended, we found that the best results were obtained using a pure CHF_3 plasma. This yielded a high selectivity (5.07) to E-Beam resist, along with smooth and vertical sidewalls. The anisotropic etching of Nano-crystalline Diamond was implemented using the widely reported oxygen plasma process. An important consideration during the process was the choice of mask, as conventional polymer masks are easily etched

in O_2 plasma. Since the focus of the etch was the fabrication of waveguide structures, using metal masks for this purpose was challenging due to the dimensional constraints. Therefore, HSQ was chosen as the mask material due to its excellent etch resistance in O_2 plasma. As a result, vertical and smooth sidewalls were achieved, along with the ability to etch deep features.

A hybrid silicon/diamond suspended air-clad waveguide platform fabricated from nanocrystalline diamond thin films for operation at 1550 nm was demonstrated in Chapter 5. Due to the wide transmission window of diamond, this platform can be easily scaled to operate over a wide section of the optical spectrum, covering the UV to the far infrared and therefore can have a large range of applications ranging from visible light integrated photonics to far-infrared optical sensing. Optical characterization of the waveguides at 1550 nm yielded an average optical loss of $4.67 \pm 0.47\ dB/mm$.

In Chapter 6, it has been demonstrated that isotropic SF_6 etching of silicon is a viable alternative to other isotropic etch processes. This method presents an opportunity to perform these etches to isolate membranes, release MEMS structures etc., without the need for specialised etching equipment. The absence of a liquid phase etch eliminates the need for critical phase drying and reduces the possibility of collapse and stiction. The etch rates achieved during the study demonstrate that the etch duration can be comparable to the XeF_2 vapour etch process.

The etch rates of several materials in SF_6 ICP etching, and their selectivity against silicon was reported in Chapter 7. The measured etch rates are $19.13\ nm/min$ for SiO_2, $58.54\ nm/min$ for SiN, $42.2\ nm/min$ for AZ-1505 PR, $94.4\ nm/min$ for AZ-nLOF 2020 PR, $13\ nm/min$ for SU-8 and $0.44\ nm/min$ for NCD. The silicon selectivity versus NCD was found to be 5000:1, which is promising for creating suspended NCD membranes over silicon substrates using plasma etching. The generated surface roughness for tested materials from short and moderate etching times is within acceptable limits for most applications. This etching technique was also found to be an effective polishing technique for NCD films following the CMP process, in order to increase their smoothness.

Finally in Chapter 8, a novel bonding process was presented, along with the steps required to fabricate a suspended structure.

Several significant developments have been made during the course of this thesis. Firstly, we have demonstrated the suitability of diamond as an optical material. The NCD waveguide architecture presented in this work can be used for various applications such as mid-IR communication and gas sensing. The waveguide losses presented in our work are also better or comparable with other NCD waveguides using different architectures. A novel method of undercutting the silicon layer utilising SF_6 ICP-RIE plasma was also presented in this work. This offers a fabrication technique that enables the fabrication of the waveguide in a CMOS compatible fab, thereby reducing cost and complexity. Also, as shown in Chapter 7, this etching techinique offers great selectivity versus diamond, as well as reducing the surface roughness. Finally, we have outlined a bonding method in Chapter 8 for the fabrication of suspended membranes. This along with the development of the NCD platform enables the integration of waveguides with other devices (such as micro-toroid resonators). Due to the material properties as well as the flexibility afforded by the architecture, this is an ideal platform for MEMS actuation.

9.1 Future Vision

The results achieved during this study have been promising, and new research directions may be further explored:

1. In Chapter 5, light was coupled to the waveguides using edge coupling. As mentioned in the chapter, the diamond membrane tends to sag at the edges due to the higher etch rate. The insertion losses can be reduced by the use of grating couplers.

2. The isotropic SF_6 etching mechanism is described in Chapter 6. None of the existing models accurately predict the etch rate achieved. Therefore, a Monte-Carlo simulation can be performed in order to better estimate the etch rate.

3. In Chapter 7, the etch rates, selectivity and surface roughness are measured for various materials using the chosen etch recipe. The etch parameters such as ICP power, chamber pressure, temperature and flow rate can be varied to better understand the etch behaviour.

4. The bonding process described in Chapter 8 can be developed further through the use of different materials such as NCD.

Appendix A

Photolithography recipes

The photolithography recipes used during the fabrication processes detailed in this work are presented here. All the samples were $1cm \times 1cm$ silicon chips (manually diced) and cleaned using the standard degrease process. After the spin coating step, the photoresist layer was allowed to rest for at least 10 minutes. Following the development of the photoresist, the samples were rinsed for at least 2 minutes under flowing DI water, and dried using a nitrogen gun. In order to measure the film thickness, the resist was scratched using a scalpel, and the thickness measured using profilometry.

Step	Details
Spin coating	10 sec @ 500 rpm, 50 sec @ 4000 rpm
Ramp	1000 rpm/sec
Soft bake	90 sec @ 100 $^{\circ}C$ (hotplate)
Exposure	140 mJ/cm^2 in broadband Hg vapour UV lamp
Development	60 sec (with agitation) in MF-319 developer

Table A.1 S-1818 photoresist (1.7 μm film thickness)

Step	Details
Spin coating	10 sec @ 1000 rpm, 50 sec @ 3000 rpm
Ramp	1000 rpm/sec
Soft bake	2 min @ 100 $^{\circ}C$ (hotplate)
Exposure	196 mJ/cm^2 in broadband Hg vapour UV lamp
Post exposure bake	60 sec @ 100 $^{\circ}C$ (hotplate)
Development	60 sec (with agitation) in AZ-726 developer

Table A.2 AZ nLof 2020 photoresist (2 μm film thickness)

Step	Details
Spin coating	10 sec @ 1000 rpm, 50 sec @ 4000 rpm
Ramp	1000 rpm/sec
Soft bake	1 min @ 100 $^{\circ}C$ (hotplate)
Exposure	112 mJ/cm^2 in broadband Hg vapour UV lamp
Development	60 sec (with agitation) in AZ-726 developer (diluted 3:1 with DI water)
Hard bake	1 min @ 120 $^{\circ}C$ (hotplate)

Table A.3 AZ 1505 photoresist (450 nm film thickness)

Step	Details
Spin coating	5 sec @ 500 rpm, 30 sec @ 3500 rpm
Ramp	200 rpm/sec
Soft bake	60 sec @ 65 $^{\circ}C$, 3 min @ 95 $^{\circ}C$ (hotplate)
Exposure	84 mJ/cm^2 in broadband Hg vapour UV lamp
Post exposure bake	60 sec @ 65 $^{\circ}C$, 60 sec @ 95 $^{\circ}C$ (hotplate)
Development	90 sec (with agitation) in PGMEA
Hard bake	5 min @ 200 $^{\circ}C$ (hotplate)

Table A.4 SU8-5 (1.7 μm film thickness)

Step	Details
Spin coating	10 sec @ 500 rpm, 50 sec @ 3500 rpm
Ramp	1000 rpm/sec
Soft bake	5 min @ 190 $^{\circ}C$ (hotplate)

Table A.5 PMMA (1.75 μm film thickness)

References

[1] Carlos Errando-Herranz, Frank Niklaus, Göran Stemme, and Kristinn B. Gylfason. Low-power microelectromechanically tunable silicon photonic ring resonator add-drop filter. *Optics Letters*, 40(15):3556–3559, August 2015.

[2] Sangyoon Han, Tae Joon Seok, Niels Quack, Byung-Wook Yoo, and Ming C. Wu. Large-scale silicon photonic switches with movable directional couplers. *Optica*, 2(4):370–375, April 2015.

[3] Pao Tai Lin, Vivek Singh, Juejun Hu, Kathleen Richardson, J. David Musgraves, Igor Luzinov, Joel Hensley, Lionel C. Kimerling, and Anu Agarwal. Chip-scale Mid-Infrared chemical sensors using air-clad pedestal silicon waveguides. *Lab on a Chip*, 13(11):2161–2166, May 2013.

[4] James Clerk Maxwell. A Dynamical Theory of the Electromagnetic Field. *Philosophical Transactions of the Royal Society of London*, 155:459–512, January 1865.

[5] Desmond Rodney Lim. *Device integration for silicon microphotonic platforms*. Thesis, Massachusetts Institute of Technology, 2000.

[6] Daniel Fleisch. *A Student's Guide to Maxwell's Equations*. Cambridge University Press, Cambridge, 2008.

[7] Eric Harvey. Design and fabrication of silicon on insulator optical waveguide devices. *Theses*, September 2006.

[8] Graham T. Reed and Andrew P. Knights. *Silicon Photonics: An Introduction*. John Wiley & Sons, October 2004.

[9] Matthew N. O. Sadiku. Elements of electromagnetics, January 2014.

[10] Eugene Hecht. *Optics 4th Edition*. 1998.

[11] John A. Buck. *Fundamentals of Optical Fibers*. John Wiley & Sons, April 2004.

[12] Graham T. Reed. *Silicon Photonics: The State of the Art*. John Wiley & Sons, May 2008.

[13] Amnon Yariv and Pochi Yeh. *Photonics: Optical Electronics in Modern Communications*. Oxford University Press, 2007.

[14] Ryuichi Watanabe and Kiyoshi Nosu. Slab waveguide demultiplexer for multimode optical transmission in the 1.0–1.4-um wavelength region. *Applied Optics*, 19(21):3588–3590, November 1980.

[15] D. Mergerian, E. C. Malarkey, R. P. Pautienus, J. C. Bradley, G. E. Marx, L. D. Hutcheson, and A. L. Kellner. Operational integrated optical R.F. spectrum analyzer. *Applied Optics*, 19(18):3033–3034, September 1980.

[16] U. Fischer, T. Zinke, J. R. Kropp, F. Arndt, and K. Petermann. 0.1 dB/cm waveguide losses in single-mode SOI rib waveguides. *IEEE Photonics Technology Letters*, 8(5):647–648, May 1996.

[17] Kevin K. Lee, Desmond R. Lim, Hsin-Chiao Luan, Anuradha Agarwal, James Foresi, and Lionel C. Kimerling. Effect of size and roughness on light transmission in a Si/SiO2 waveguide: Experiments and model. *Applied Physics Letters*, 77(11):1617–1619, September 2000.

[18] Kevin K. Lee, Desmond R. Lim, Lionel C. Kimerling, Jangho Shin, and Franco Cerrina. Fabrication of ultralow-loss Si/SiO_2 waveguides by roughness reduction. *Optics Letters*, 26(23):1888, December 2001.

[19] J. M. Fedeli, E. Augendre, J. M. Hartmann, L. Vivien, P. Grosse, V. Mazzocchi, W. Bogaerts, D. Van Thourhout, and F. Schrank. Photonics and electronics integration in the HELIOS project. In *7th IEEE International Conference on Group IV Photonics*, pages 356–358, September 2010.

[20] C. Gunn. CMOS Photonics for High-Speed Interconnects. *IEEE Micro*, 26(2):58–66, March 2006.

[21] Wim Bogaerts, Pieter Dumon, Dries Van Thourhout, Dirk Taillaert, Patrick Jaenen, Johan Wouters, Stephan Beckx, Vincent Wiaux, and Roel G. Baets. Compact Wavelength-Selective Functions in Silicon-on-Insulator Photonic Wires. *IEEE Journal of Selected Topics in Quantum Electronics*, 12(6):1394–1401, November 2006.

[22] Yi Zhang. *A Toolbox of Optimized Silicon Photonics Devices*. Thesis, May 2015.

[23] G. Roelkens, L. Liu, D. Liang, R. Jones, A. Fang, B. Koch, and J. Bowers. III-V/silicon photonics for on-chip and intra-chip optical interconnects. *Laser & Photonics Reviews*, 4(6):751–779.

[24] Alexander W. Fang, Hyundai Park, Oded Cohen, Richard Jones, Mario J. Paniccia, and John E. Bowers. Electrically pumped hybrid AlGaInAs-silicon evanescent laser. *Optics Express*, 14(20):9203, 2006.

[25] Joost Brouckaert, Gunther Roelkens, Dries Van Thourhout, and Roel Baets. Compact InAlAs–InGaAs Metal– Semiconductor– Metal Photodetectors Integrated on Silicon-on-Insulator Waveguides. *IEEE Photonics Technology Letters*, 19(19):1484–1486, October 2007.

[26] Florian Krach, Holger Schwarzmann, Anton J. Bauer, Tobias Erlbacher, and Lothar Frey. Silicon nitride, a high potential dielectric for 600v integrated RC snubber applications. *Journal of Vacuum Science & Technology B*, 33(1):01A112, January 2015.

[27] J. Yota, J. Hander, and A. A. Saleh. A comparative study on inductively-coupled plasma high-density plasma, plasma-enhanced, and low pressure chemical vapor deposition silicon nitride films. *Journal of Vacuum Science & Technology A*, 18(2):372–376, March 2000.

[28] Jared F. Bauters, Martijn J. R. Heck, Demis John, Daoxin Dai, Ming-Chun Tien, Jonathon S. Barton, Arne Leinse, René G. Heideman, Daniel J. Blumenthal, and John E. Bowers. Ultra-low-loss high-aspect-ratio Si3n4 waveguides. *Optics Express*, 19(4):3163–3174, February 2011.

[29] Mohamed Gad-el Hak. *The MEMS Handbook: Design and fabrication*. Taylor & Francis, 2005.

[30] Vaclav Prajzler, Marian Varga, Pavla Nekvindova, Zdenek Remes, and Alexander Kromka. Design and investigation of properties of nanocrystalline diamond optical planar waveguides. *Optics Express*, 21(7):8417, April 2013.

[31] George E. Harlow and American Museum of Natural History. *The Nature of Diamonds*. Cambridge University Press, 1998.

[32] T. Tsuchizawa, K. Yamada, H. Fukuda, T. Watanabe, Jun-ichi Takahashi, M. Takahashi, T. Shoji, E. Tamechika, S. Itabashi, and H. Morita. Microphotonics devices based on silicon microfabrication technology. *IEEE Journal of Selected Topics in Quantum Electronics*, 11(1):232–240, January 2005.

[33] Dietrich Marcuse. Mode Conversion Caused by Surface Imperfections of a Dielectric Slab Waveguide. *Bell System Technical Journal*, 48(10):3187–3215, July 2013.

[34] Encyclopedia of Laser Physics and Technology - phase velocity, light.

[35] Encyclopedia of Laser Physics and Technology - group velocity, light, envelope.

[36] Graham T. Reed, Goran Z. Masanovic, William R. Headley, Ching Eng Png, Seong P. Chan, Soon T. Lim, Vittorio M. N. Passaro, D. Hak, Oded Cohen, and Mario J. Paniccia. Small devices in SOI: fabrication and design issues. page 75, July 2004.

[37] R. Courant. Variational methods for the solution of problems of equilibrium and vibrations. *Bulletin of the American Mathematical Society*, 49(1):1–23, 1943.

[38] K. K. Gupta and J. L. Meek. A Brief History of the Beginning of the Finite Element Method. *International Journal for Numerical Methods in Engineering*, 39(22):3761–3774.

[39] Kane Yee. Numerical solution of initial boundary value problems involving maxwell's equations in isotropic media. *IEEE Transactions on Antennas and Propagation*, 14(3):302–307, May 1966.

[40] P. Bienstman and R. Baets. Optical modelling of photonic crystals and VCSELs using eigenmode expansion and perfectly matched layers. *Optical and Quantum Electronics*, 33(4-5):327–341, April 2001.

[41] Wim Bogaerts and Diedrik Vermeulen. Off chip coupling. In *Handbook of silicon photonics*, pages 97–138. Taylor & Francis, 2013.

[42] Sharee McNab, Nikolaj Moll, and Yurii Vlasov. Ultra-low loss photonic integrated circuit with membrane-type photonic crystal waveguides. *Optics Express*, 11(22):2927, November 2003.

[43] Regis Orobtchouk. On Chip Optical Waveguide Interconnect: the Problem of the In/Out Coupling. In Lorenzo Pavesi and Gérard Guillot, editors, *Optical Interconnects*, volume 119, pages 263–290. Springer Berlin Heidelberg, Berlin, Heidelberg, 2006.

[44] A. E. J. Lim, J. Song, Q. Fang, C. Li, X. Tu, N. Duan, K. K. Chen, R. P. C. Tern, and T. Y. Liow. Review of Silicon Photonics Foundry Efforts. *IEEE Journal of Selected Topics in Quantum Electronics*, 20(4):405–416, July 2014.

[45] Attila Mekis, Sherif Abdalla, Peter M. De Dobbelaere, Dennis Foltz, Steffen Gloeckner, Steven Hovey, Steven Jackson, Yi Liang, Michael Mack, Gianlorenzo Masini, Rafaela Novais, Mark Peterson, Thierry Pinguet, Subal Sahni, Jeff Schramm, Michael Sharp, Daniel Song, Brian P. Welch, Kosei Yokoyama, and Shuhuan Yu. Scaling CMOS photonics transceivers beyond 100 Gb/s. In *Optoelectronic Integrated Circuits XIV*, volume 8265, page 82650A. International Society for Optics and Photonics, February 2012.

[46] Wissem Sfar Zaoui, Andreas Kunze, Wolfgang Vogel, Manfred Berroth, Jörg Butschke, Florian Letzkus, and Joachim Burghartz. Bridging the gap between optical fibers and silicon photonic integrated circuits. *Optics Express*, 22(2):1277, January 2014.

[47] John Covey and Ray T. Chen. Efficient perfectly vertical fiber-to-chip grating coupler for silicon horizontal multiple slot waveguides. *Optics Express*, 21(9):10886, May 2013.

[48] Marc J. Madou. *Manufacturing Techniques for Microfabrication and Nanotechnology*. CRC Press, June 2011.

[49] Harry J. Levinson. *Principles of Lithography*. SPIE Press, 2005.

[50] Yoshio Nishi, Robert Doering, and Robert Doering. *Handbook of Semiconductor Manufacturing Technology*. CRC Press, December 2017.

[51] Microchemicals - Resists, Developers and Removers.

[52] Microchemicals - Rehydration of Photoresists.

[53] Microchemicals - Etching with Hydrofluoric Acid.

[54] K. R. Williams and R. S. Muller. Etch rates for micromachining processing. *Journal of Microelectromechanical Systems*, 5(4):256–269, December 1996.

[55] C. H. Mastrangelo and C. H. Hsu. Mechanical stability and adhesion of microstructures under capillary forces. II. Experiments. *Journal of Microelectromechanical Systems*, 2(1):44–55, March 1993.

[56] K. R. Williams, K. Gupta, and M. Wasilik. Etch rates for micromachining processing-Part II. *Journal of Microelectromechanical Systems*, 12(6):761–778, December 2003.

[57] H. Baltes, O. Paul, and O. Brand. Micromachined thermally based CMOS microsensors. *Proceedings of the IEEE*, 86(8):1660–1678, August 1998.

[58] H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgärtel. Anisotropic Etching of Crystalline Silicon in Alkaline Solutions I . Orientation Dependence and Behavior of Passivation Layers. *Journal of The Electrochemical Society*, 137(11):3612–3626, November 1990.

[59] Ion G. Stiharu, Rama B. Bhat, Mojtaba Kahrizi, and Leslie M. Landsberger. Influence of the stress state in silicon on the anisotropic etching process. In *Laser-Assisted Fabrication of Thin Films and Microstructures*, volume 2045, pages 254–262. International Society for Optics and Photonics, February 1994.

[60] Don L. Kendall. A new theory for the anisotropic etching of silicon and some underdeveloped chemical micromachining concepts. *Journal of Vacuum Science & Technology A*, 8(4):3598–3605, July 1990.

[61] C. J. Pugh. *End Point Detection in Reactive Ion Etching*. Doctoral, UCL (University College London), April 2013.

[62] Richard C. Jaeger. *Introduction to Microelectronic Fabrication*. Prentice Hall, 2002.

[63] Fouad Karouta. A practical approach to reactive ion etching. *Journal of Physics D: Applied Physics*, 47(23):233501, May 2014.

[64] Leonel R. Arana, Nuria de Mas, Raymond Schmidt, Aleksander J. Franz, Martin A. Schmidt, and Klavs F. Jensen. Isotropic etching of silicon in fluorine gas for MEMS micromachining. *Journal of Micromechanics and Microengineering*, 17(2):384–392, January 2007.

[65] P. B. Chu, J. T. Chen, R. Yeh, G. Lin, J. C. P. Huang, B. A. Warneke, and S. J. Pister. Controlled pulse-etching with xenon difluoride. In *Proceedings of International Solid State Sensors and Actuators Conference (Transducers '97)*, volume 1, pages 665–668 vol.1, June 1997.

[66] David W Oxtoby and Norman H Nachtrieb. *Principles of modern chemistry*. Saunders College, Philadelphia, 1986.

[67] R. Hoppe, W. Dähne, H. Mattauch, and K. Rödder. Fluorination of Xenon. *Angewandte Chemie International Edition in English*, 1(11):599–599, November 1962.

[68] C. L. Chernick, H. H. Claassen, P. R. Fields, H. H. Hyman, J. G. Malm, W. M. Manning, M. S. Matheson, L. A. Quarterman, F. Schreiner, H. H. Selig, I. Sheft, S. Siegel, E. N. Sloth, L. Stein, M. H. Studier, J. L. Weeks, and M. H. Zirin. Fluorine Compounds of Xenon and Radon. *Science*, 138(3537):136–138, October 1962.

[69] E. Hoffman, B. Warneke, E. Kruglick, J. Weigold, and K. S. J. Pister. 3d structures with piezoresistive sensors in standard CMOS. In *Proceedings IEEE Micro Electro Mechanical Systems. 1995*, pages 288–, January 1995.

[70] D. Xu, B. Xiong, G. Wu, Y. Wang, X. Sun, and Y. Wang. Isotropic Silicon Etching With XeF2 Gas for Wafer-Level Micromachining Applications. *Journal of Microelectromechanical Systems*, 21(6):1436–1444, December 2012.

[71] Henri Jansen, Han Gardeniers, Meint de Boer, Miko Elwenspoek, and Jan Fluitman. A survey on the reactive ion etching of silicon in microtechnology. *Journal of Micromechanics and Microengineering*, 6(1):14–28, March 1996.

[72] Rob Legtenberg, Henri Jansen, Meint de Boer, and Miko Elwenspoek. Anisotropic Reactive Ion Etching of Silicon Using SF 6 / O 2 / CHF 3 Gas Mixtures. *Journal of The Electrochemical Society*, 142(6):2020–2028, June 1995.

[73] C. Hedlund, H.-O. Blom, and S. Berg. Microloading effect in reactive ion etching. *Journal of Vacuum Science & Technology A*, 12(4):1962–1965, July 1994.

[74] H.-C. Liu, Y.-H. Lin, and W. Hsu. Sidewall roughness control in advanced silicon etch process. *Microsystem Technologies*, 10(1):29–34, December 2003.

[75] N. Daldosso, M. Melchiorri, F. Riboli, M. Girardini, G. Pucker, M. Crivellari, P. Bellutti, A. Lui, and L. Pavesi. Comparison among various Si3n4 waveguide geometries grown within a CMOS fabrication pilot line. *Journal of Lightwave Technology*, 22(7):1734–1740, July 2004.

[76] Mark P. Hiscocks, Kumaravelu Ganesan, Brant C. Gibson, Shane T. Huntington, François Ladouceur, and Steven Prawer. Diamond waveguides fabricated by reactive ion etching. *Optics Express*, 16(24):19512–19519, November 2008.

[77] Aly Abdou, Parashara Panduranga, Jens Richter, Evan L. H. Thomas, Soumen Mandal, Oliver A. Williams, Jeremy Witzens, and Maziar P. Nezhad. Air-clad suspended nanocrystalline diamond ridge waveguides. *Optics Express*, 26(11):13883–13890, May 2018.

[78] Chung-Yen Chao, W. Fung, and L. J. Guo. Polymer microring resonators for biochemical sensing applications. *IEEE Journal of Selected Topics in Quantum Electronics*, 12(1):134–142, January 2006.

[79] Henri Jansen, Meint de Boer, Johannes Burger, Rob Legtenberg, and Miko Elwenspoek. The black silicon method II:The effect of mask material and loading on the reactive ion etching of deep silicon trenches. *Microelectronic Engineering*, 27(1):475–480, February 1995.

[80] E. Gogolides, S. Grigoropoulos, and A.G. Nassiopoulos. Highly anisotropic room-temperature sub-half-micron Si reactive ion etching using fluorine only containing gases. *Microelectronic Engineering*, 27(1-4):449–452, February 1995.

[81] Shinichi Tachi, Kazunori Tsujimoto, and Sadayuki Okudaira. Low-temperature reactive ion etching and microwave plasma etching of silicon. *Applied Physics Letters*, 52(8):616–618, February 1988.

[82] M. A. Blauw, E. van der Drift, G. Marcos, and A. Rhallabi. Modeling of fluorine-based high-density plasma etching of anisotropic silicon trenches with oxygen sidewall passivation. *Journal of Applied Physics*, 94(10):6311–6318, October 2003.

[83] F. Laerme, A. Schilp, K. Funk, and M. Offenberg. Bosch deep silicon etching: improving uniformity and etch rate for advanced MEMS applications. In *Technical Digest. IEEE International MEMS 99 Conference. Twelfth IEEE International Conference on Micro Electro Mechanical Systems (Cat. No.99CH36291)*, pages 211–216, January 1999.

[84] Franz Laermer and Andrea Schilp. Method of anisotropically etching silicon, March 1996.

[85] D. C. Hays, K. B. Jung, Y. B. Hahn, E. S. Lambers, S. J. Pearton, J. Donahue, D. Johnson, and R. J. Shul. Comparison of F 2-Based Gases for High-Rate Dry Etching of Si. *Journal of The Electrochemical Society*, 146(10):3812–3816, October 1999.

[86] Daniel L. Flamm, Vincent M. Donnelly, and John A. Mucha. The reaction of fluorine atoms with silicon. *Journal of Applied Physics*, 52(5):3633–3639, May 1981.

[87] Tsengyou Syau, B. Jayant Baliga, and Raymond W. Hamaker. Reactive Ion Etching of Silicon Trenches Using SF 6 / O 2 Gas Mixtures. *Journal of The Electrochemical Society*, 138(10):3076–3081, October 1991.

[88] H. Jansen, M. de Boer, R. Legtenberg, and M. Elwenspoek. The black silicon method: a universal method for determining the parameter setting of a fluorine-based reactive ion etcher in deep silicon trench etching with profile control. *Journal of Micromechanics and Microengineering*, 5(2):115–120, June 1995.

[89] J. C. Arnold and H. H. Sawin. Charging of pattern features during plasma etching. *Journal of Applied Physics*, 70(10):5314–5317, November 1991.

[90] Richard A. Gottscho, C. W. Jurgensen, and D. J. Vitkavage. Microscopic uniformity in plasma etching. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, 10(5):2133–2147, September 1992.

[91] Khaled A. Alshaltami, Muhammad Morshed, Cezar Gaman, Jim Conway, and Stephen Daniels. Experimental investigation of SF6–O2 plasma for advancement of the anisotropic Si etch process. *Journal of Vacuum Science & Technology A*, 35(3):031307, April 2017.

[92] Johann W. Bartha, Johann Greschner, M. Puech, and P. Maquin. Low temperature etching of Si in high density plasma using SF6/O2. *Microelectronic Engineering*, 27(1):453–456, February 1995.

[93] S. Grigoropoulos, E. Gogolides, A. D. Tserepi, and A. G. Nassiopoulos. Highly anisotropic silicon reactive ion etching for nanofabrication using mixtures of SF6/CHF3 gases. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, 15(3):640–645, May 1997.

[94] K. E. Petersen. Silicon as a mechanical material. *Proceedings of the IEEE*, 70(5):420–457, May 1982.

[95] R. F. Wolffenbuttel, J. F. L. Goosen, and P. M. Sarro. Design considerations for a permanent-rotor-charge-excited micromotor with an electrostatic bearing. *Sensors and Actuators A: Physical*, 27(1):583–590, May 1991.

[96] B. D. Pant and U. S. Tandon. Etching of Silicon Nitride in CCl2f2, CHF3, SiF4, and SF6 Reactive Plasma: A Comparative Study. *Plasma Chemistry and Plasma Processing*, 19(4):545–563, December 1999.

[97] T. C. Mele, J. Nulman, and J. P. Krusius. Selective and anisotropic reactive ion etch of LPCVD silicon nitride with CHF3 based gases. *Journal of Vacuum Science & Technology B: Microelectronics Processing and Phenomena*, 2(4):684–687, October 1984.

[98] Y. X. Li, P. J. French, and R. F. Wolffenbuttel. Selective reactive ion etching of silicon nitride over silicon using CHF3 with N2 addition. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, 13(5):2008–2012, September 1995.

[99] Yutaka Ando, Yoshiki Nishibayashi, Koji Kobashi, Takashi Hirao, and Kenjiro Oura. Smooth and high-rate reactive ion etching of diamond. *Diamond and Related Materials*, 11(3):824–827, March 2002.

[100] Luozhou Li, Matthew Trusheim, Ophir Gaathon, Kim Kisslinger, Ching-Jung Cheng, Ming Lu, Dong Su, Xinwen Yao, Hsu-Cheng Huang, Igal Bayn, Abraham Wolcott, Richard M. Osgood, and Dirk Englund. Reactive ion etching: Optimized diamond membrane fabrication for transmission electron microscopy. *Journal of Vacuum Science & Technology B*, 31(6):06FF01, July 2013.

[101] Z. G. Hu, P. Prunici, P. Hess, and K. H. Chen. Optical properties of nanocrystalline diamond films from mid-infrared to ultraviolet using reflectometry and ellipsometry. *Journal of Materials Science: Materials in Electronics*, 18(1):37–41, October 2007.

[102] Birgit J. M. Hausmann, Brendan Shields, Qimin Quan, Patrick Maletinsky, Murray McCutcheon, Jennifer T. Choy, Tom M. Babinec, Alexander Kubanek, Amir Yacoby, Mikhail D. Lukin, and Marko Loncar. Integrated Diamond Networks for Quantum Nanophotonics. *Nano Letters*, 12(3):1578–1582, March 2012.

[103] Afaq H. Piracha, Patrik Rath, Kumaravelu Ganesan, Stefan Kühn, Wolfram H. P. Pernice, and Steven Prawer. Scalable Fabrication of Integrated Nanophotonic Circuits on Arrays of Thin Single Crystal Diamond Membrane Windows. *Nano Letters*, 16(5):3341–3347, May 2016.

[104] F. Gao, J. Van Erps, Z. Huang, H. Thienpont, R. G. Beausoleil, and N. Vermeulen. Directional Coupler Based on Single-Crystal Diamond Waveguides. *IEEE Journal of Selected Topics in Quantum Electronics*, 24(6):1–9, November 2018.

[105] Yoichi Hirose and Yuki Terasawa. Synthesis of Diamond Thin Films by Thermal CVD Using Organic Compounds. *Japanese Journal of Applied Physics*, 25(6A):L519, June 1986.

[106] Y. Liou, A. Inspektor, R. Weimer, and R. Messier. Low-temperature diamond deposition by microwave plasma-enhanced chemical vapor deposition. *Applied Physics Letters*, 55(7):631–633, August 1989.

[107] O.A. Williams. Nanocrystalline diamond. *Diamond and Related Materials*, 20(5-6):621–640, May 2011.

[108] Nico Gruhler, Taro Yoshikawa, Patrik Rath, Georgia Lewes-Malandrakis, Edgar Schmidhammer, Christoph Nebel, and Wolfram H. P. Pernice. Diamond on aluminum nitride as a platform for integrated photonic circuits. *physica status solidi (a)*, 213(8):2075–2080, 2016.

[109] P. Rath, N. Gruhler, S. Khasminskaya, C. Nebel, C. Wild, and W. H. P. Pernice. Waferscale nanophotonic circuits made from diamond-on-insulator substrates. *Optics Express*, 21(9):11031–11036, May 2013.

[110] J. Soler Penades, A. Ortega-Moñux, M. Nedeljkovic, J. G. Wangüemert-Pérez, R. Halir, A. Z. Khokhar, C. Alonso-Ramos, Z. Qu, I. Molina-Fernández, P. Cheben, and G. Z. Mashanovich. Suspended silicon mid-infrared waveguide devices with subwavelength grating metamaterial cladding. *Optics Express*, 24(20):22908–22916, October 2016.

[111] Z. Cheng, X. Chen, C. Y. Wong, K. Xu, and H. K. Tsang. Mid-infrared Suspended Membrane Waveguide and Ring Resonator on Silicon-on-Insulator. *IEEE Photonics Journal*, 4(5):1510–1519, October 2012.

[112] X. Checoury, D. Néel, P. Boucaud, C. Gesset, H. Girard, S. Saada, and P. Bergonzo. Nanocrystalline diamond photonics platform with high quality factor photonic crystal cavities. *Applied Physics Letters*, 101(17):171115, October 2012.

[113] D. M. Shyroki. Exact Equivalent Straight Waveguide Model for Bent and Twisted Waveguides. *IEEE Transactions on Microwave Theory and Techniques*, 56(2):414–419, February 2008.

[114] Evan L. H. Thomas, Geoffrey W. Nelson, Soumen Mandal, John S. Foord, and Oliver A. Williams. Chemical mechanical polishing of thin film diamond. *Carbon*, 68:473–479, March 2014.

[115] Mikael Malmström, Mikael Karlsson, Pontus Forsberg, Yixiao Cai, Fredrik Nikolajeff, and Fredrik Laurell. Waveguides in polycrystalline diamond for mid-IR sensing. *Optical Materials Express*, 6(4):1286–1295, April 2016.

[116] J. M. Dodson, J. R. Brandon, H. K. Dhillon, I. Friel, S. L. Geoghegan, T. P. Mollart, P. Santini, G. A. Scarsbrook, D. J. Twitchen, A. J. Whitehead, J. J. Wilman, and H. de Wit. Single crystal and polycrystalline CVD diamond for demanding optical applications. In *Window and Dome Technologies and Materials XII*, volume 8016, page 80160L. International Society for Optics and Photonics, May 2011.

[117] F. P. Payne and J. P. R. Lacey. A theoretical analysis of scattering loss from planar optical waveguides. *Optical and Quantum Electronics*, 26(10):977–986, October 1994.

[118] H. Jansen, M. de Boer, and M. Elwenspoek. The black silicon method. VI. High aspect ratio trench etching for MEMS applications. In *Proceedings of Ninth International Workshop on Micro Electromechanical Systems*, pages 250–257, February 1996.

[119] M D Henry, S Walavalkar, A Homyk, and A Scherer. Alumina etch masks for fabrication of high-aspect-ratio silicon micropillars and nanopillars. *Nanotechnology*, 20(25):255305, June 2009.

[120] C. J. Mogab. The Loading Effect in Plasma Etching. *Journal of The Electrochemical Society*, 124(8):1262–1268, August 1977.

[121] Vincent M. Donnelly. Review Article: Reactions of fluorine atoms with silicon, revisited, again. *Journal of Vacuum Science & Technology A*, 35(5):05C202, May 2017.

[122] R. Knizikevičius and V. Kopustinskas. Influence of temperature on the formation of SiF2 molecules. *Microelectronic Engineering*, 157:42–45, May 2016.

[123] O Painter, R K Lee, A Scherer, A Yariv, J D O'Brien, P D Dapkus, and I Kim. Two-Dimensional Photonic Band-Gap Defect Mode Laser. 284:4, 1999.

[124] Maziar P. Nezhad, Aleksandar Simic, Olesya Bondarenko, Boris Slutsky, Amit Mizrahi, Liang Feng, Vitaliy Lomakin, and Yeshaiahu Fainman. Room-temperature subwavelength metallo-dielectric lasers. *Nature Photonics*, 4(6):395–399, June 2010.

[125] Liuqing He, Yuhao Guo, Zhaohong Han, Kazumi Wada, Lionel C. Kimerling, Jurgen Michel, Anuradha M. Agarwal, Guifang Li, and Lin Zhang. Loss reduction of silicon-on-insulator waveguides for deep mid-infrared applications. *Optics Letters*, 42(17):3454–3457, September 2017.

[126] D. K. Armani, T. J. Kippenberg, S. M. Spillane, and K. J. Vahala. Ultra-high- Q toroid microcavity on a chip. *Nature*, 421(6926):925, February 2003.

[127] John C. Arnold, David C. Gray, and Herbert H. Sawin. Influence of reactant transport on fluorine reactive ion etching of deep trenches in silicon. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, 11(6):2071–2080, November 1993.

[128] Burkhard E. Volland. Profile simulations of gas chopping etching processes : model development and comparison with experiments. July 2004.

[129] J. W. Coburn and Harold F. Winters. Conductance considerations in the reactive ion etching of high aspect ratio features. *Applied Physics Letters*, 55(26):2730–2732, December 1989.

[130] Riccardo d'Agostino and Daniel L. Flamm. Plasma etching of Si and SiO2 in SF6–O2 mixtures. *Journal of Applied Physics*, 52(1):162–167, January 1981.

[131] Jicheng Zhang, Minjie Zhou, Weidong Wu, and Yongjian Tang. Fabrication of Diamond Microstructures by Using Dry and Wet Etching Methods. *Plasma Science and Technology*, 15(6):552–554, June 2013.

[132] P. W. Leech, G. K. Reeves, and A. Holland. Reactive ion etching of diamond in CF4, O2, O2 and Ar-based mixtures. *Journal of Materials Science*, 36(14):3453–3459, July 2001.

[133] Gopi M. R. Sirineni, H. A. Naseem, A. P. Malshe, and W. D. Brown. Reactive ion etching of diamond as a means of enhancing chemically-assisted mechanical polishing efficiency. *Diamond and Related Materials*, 6(8):952–958, May 1997.

[134] Victor Hägglund. *Characterization of masking layers for deep wet etching in borofloat glass*. PhD thesis.

[135] V. Masteika, J. Kowal, N. St J. Braithwaite, and T. Rogers. A Review of Hydrophilic Silicon Wafer Bonding. *ECS Journal of Solid State Science and Technology*, 3(4):Q42–Q54, January 2014.

[136] Y. Feng. Silicon Direct Bonding on Vacuum and Force. In *2006 International Conference on Mechatronics and Automation*, pages 491–496, June 2006.

[137] Liming Yu, Francis E H Tay, Guolin Xu, Bangtao Chen, Marioara Avram, and Ciprian Iliescu. Adhesive bonding with SU-8 at wafer level for microfluidic devices. *Journal of Physics: Conference Series*, 34:776–781, April 2006.

[138] Yong-Kook Kim, Eun-Kyung Kim, and Soo-Won Kim. Low temperature epoxy bonding for wafer level MEMS packaging - ScienceDirect. 2007.

[139] F. Niklaus, P. Enoksson, E. Kalvesten, and G. Stemme. Void-free full wafer adhesive bonding. In *Proceedings IEEE Thirteenth Annual International Conference on Micro Electro Mechanical Systems (Cat. No.00CH36308)*, pages 247–252, January 2000.

[140] William P. Eaton, Subhash H. Risbud, and Rosemary L. Smith. Silicon wafer-to-wafer bonding at T<200 ° c with polymethylmethacrylate. *Applied Physics Letters*, 65(4):439–441, July 1994.