Original Research Paper

Design and Development of Multilevel Inverter (MLI) for Convert Direct Current to Alternating Current Using MATLAB Simulation

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Abstract: This paper presented the design and development of a multilevel inverter (MLI). The demand for better electronic devices increases rapidly. The multilevel inverter (MLI) which convert direct current (DC) to alternating current (AC) are widely used in the industry. The objective of this research is to design and simulate the 3-level and 3-level NPC MLI module using PLECS software. To develop the switching technique for each level of NPC MLI, and To analyse and validate the MLI in terms of harmonic. Although there is already an inverter in the market, the researcher still pursues to improve the efficiency, total harmonic distortion (THD), and reduce the size of the MLI. A THD can be improved using the suitable modulation technique and the size of the MLI can be reduced by designing better topologies. The modular NPC is using the three-level NPC as the main module and the number of levels can be increased by adding 2 level NPC modules to the main module. The switching technique was created to control the NPC MLI for each level.

1. Introduction

In a power system, the power electronic devices are utilized in an inverter and control of electrical power. The inverter in the power system fits both tasks by converting DC to AC and controlling the frequency of the AC which is the output. The multilevel inverter is used to produce a sinusoidal voltage waveform from several levels of DC voltage. However, a two-level voltage source converter incapable to get good system performance and efficiencies such as optimum filter size, THD and losses. The improved performance and efficiency of a high voltage system can be achieved by the use of a multilevel inverter [1]. As the level of inverter increases, the stress on each device can be reduced proportionally, which leads to increased voltage handling capacity of inverter and avoids a bulky & expensive step-up transformer from the application [2]. In this research, we try to achieve the goal to reduce stress on each device by adding a module to increase the number of levels for NPC MLI. To achieve the desired output AC voltage the semiconductor devices in the inverter must be controlled using a way that can minimize the harmonic. The commonly available switching technique is the selective harmonic elimination (SHE) method at the fundamental frequency, for which transcendental equations characterizing harmonics are solved to compute switching angles [3] [4].

2. Literature Review

An inverter is an essential part of any renewable energy power conversion for converting the power from DC to AC. The inverter output can be classified into two types such as square wave (two-level) and quasi square wave (three-level or modified square wave) [5]. Although the square wave and quasi-square wave inverters can be adequate for some viable applications which are still accessible in the market they are not prescribed to new plans because of their exceptionally low-quality waveform [5] [6]. To overcome this drawback, a multi-stepped waveform was introduced by the multilevel inverter (MLI) concept. MLI waveform can be divided into two types such as low-frequency multi-stepped waveform and high-frequency multi-stepped waveform using pulse width modulation (PWM). Passive filters are essential to obtain a sinusoidal output voltage waveform. High-frequency multistep waveform requires fewer passive filters when compared to other waveforms [6]. MLI comprises an array of the power semiconductor devices and DC/capacitor voltages which generates output voltage levels with stepped waveform [7]. The aim of MLI is to generate a near sinusoidal voltage waveform with several steps by utilizing the proper switching signal of the semiconductor devices and isolated or non-isolated DC voltage sources [8]. Increasing the number of levels in the output waveform leads to attaining pure sinusoidal voltage without expensive passive filters and bulky transformers [8] [9]. In low voltage applications, the two-level inverter can be used but MLI can achieve more in terms of voltage THD and losses. Because when the level of MLI increases then the near-perfect sinusoidal voltage is achieved thus resulting in the better voltage THD and less harmonic.

Figure 1 shows one phase limb of a two-level inverter and two-level waveform without PWM [10].
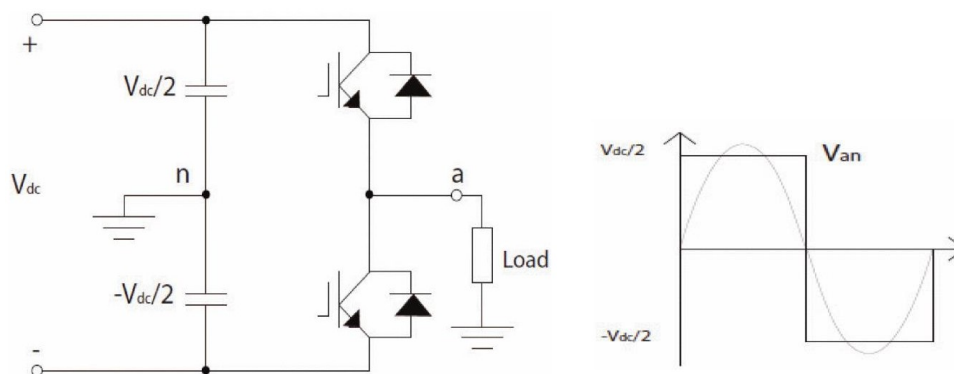

Figure 1. One phase Limb of a Two-Level Inverter and a Two-Level Waveform without PWM

In paper Koshti & Rao [11] the author discusses about the MLI topologies and the control strategies. The input voltage can be obtained from dc battery, energy storage capacitors or any kind of renewable energy sources.
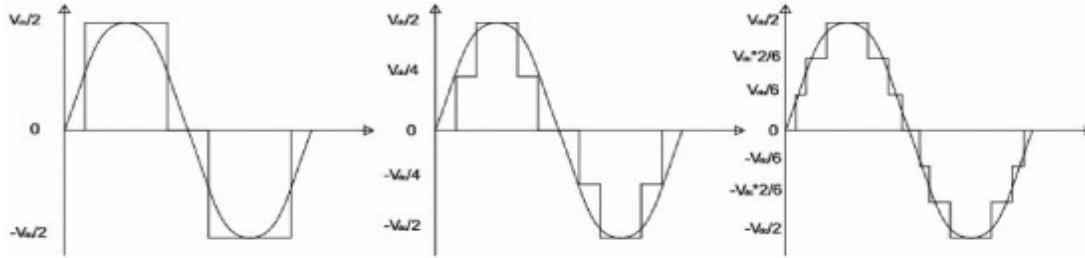

Figure 2. Level Waveform, 5-Level Waveform and a 7-Level Multilevel Waveform [11].

In Figure 2 the different of each level of inverter make the difference in sinusoidal wave. Based on Figure 2, the waveform become more sinusoidal as the level increase.

2.1. Neutral Point Clamped

The neutral point clamped (NPC) three-level inverter was first introduced by A. Nabae, I. Takahashi and H. Akagi in 1980 and published in 1981 [3]. With this circuit configuration, the voltage stress on its power switching devices is half that for the conventional two-level inverter. Because of this nature, it was applied to medium and high voltage drives [10]. The NPC inverter has lower line-to-line and common-mode voltage steps, more frequent voltage steps in one carrier cycle, and a lower ripple component in the output current for the same carrier frequency [10]. These are significant merits for motor drives over the conventional two-level inverters in the form of lower stress to the motor windings and bearings.

Figure 3 shows the circuit diagram of the NPC three-level inverter. This is also a three-phase inverter.
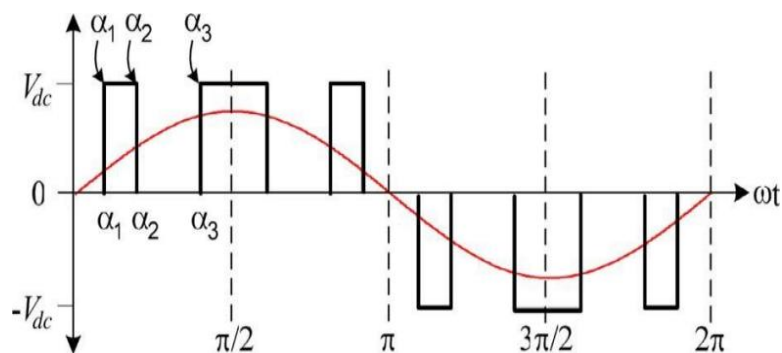

Figure 3. The neutral Point Clamped Three-Level Inverter Circuit Topology [10]

In Figure 3, when IGBTs QU1 and QU2 are turned on, output U is connected to the positive rail (P) of the dc bus. When QU2 and QU3 are on, it is connected to the mid-point (0) of the dc bus, and when QU3 and QU4 are on, it is connected to the negative rail (N) [10].

Table 1 shows the relation between the Switching States and Output Voltage [10].

Table 1. Relation between Switching States and Output Voltage

	Q_{u1}	Q_{u2}	Q_{u3}	Q_{u4}	V_u
Switching State	ON	ON	OFF	OFF	+E/2
	OFF	OFF	ON	ON	-E/2
	OFF	ON	ON	OFF	0

2.2. Selective Harmonic Elimination

Selective Harmonic Elimination (SHE) is a fairly good technique for controlling the three-level inverter. This is because the equipment needs to operate at very low frequency to reduce the semiconductor losses. Figure 2.2 shows the load voltage generated by a three-level NPC inverter. Using three switching angles α1, α2, and α3 and 90° symmetry, three harmonics can be controlled [12]. SHE-PWM is based on the Fourier series decomposition of the periodic PWM voltage waveform generated by the power electronics converter [13].

SHE technique is used to optimize switching angles of a cascaded multilevel inverter so as to produce required fundamental voltage along with improved staircase waveform in terms of total harmonic distortion (THD). Number of nonlinear transcendental equation will be s and number of harmonics to be eliminated becomes (s-1) in SHE formulation if the number of cells used in cascade multilevel inverter is s per phase.The most important part of the UPS is the inverter. Usually designed using Cascaded H-bridge MLI technology. Cascaded H-bridge multilevel technology is more appropriate for this particular application as the input is in the form of four separate batteries, which are used to achieve a stepped AC voltage waveform at the output [14].

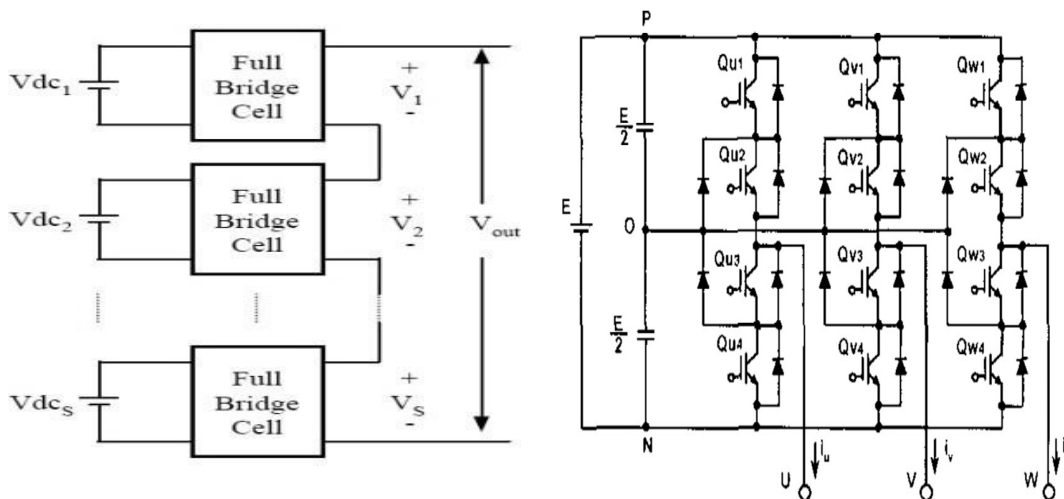Figure 4 shows topology of cascaded H-bridge multi-level Inverter [14].

Figure 4: Topology of cascaded H-bridge multi-level Inverter

The voltages of each of the four batteries are approximately equal and thus equal step size is

assumed, reducing the complexity of the controller. Therefore, this can be identified as a symmetrical source inverter. Furthermore, the use of equal size batteries gives the advantage of easy replacement as well [14]. The relationship between the number of DC sources and the output levels are given by the following equation [15].

3. Methodology

The progress for the research completion will be discussed in this chapter. Besides of the literature review, the methodology involves designing, simulation, hardware development and experimental work. This method is used to make sure the progress of the research will be more systematic.This research which is "Design and Development of Multilevel Inverter" requires the designing and development process. The designing process require several approaches same with the development process. Before the development process, there are simulation process which is very important in this research. Figure 5 shows the flowchart of the research.
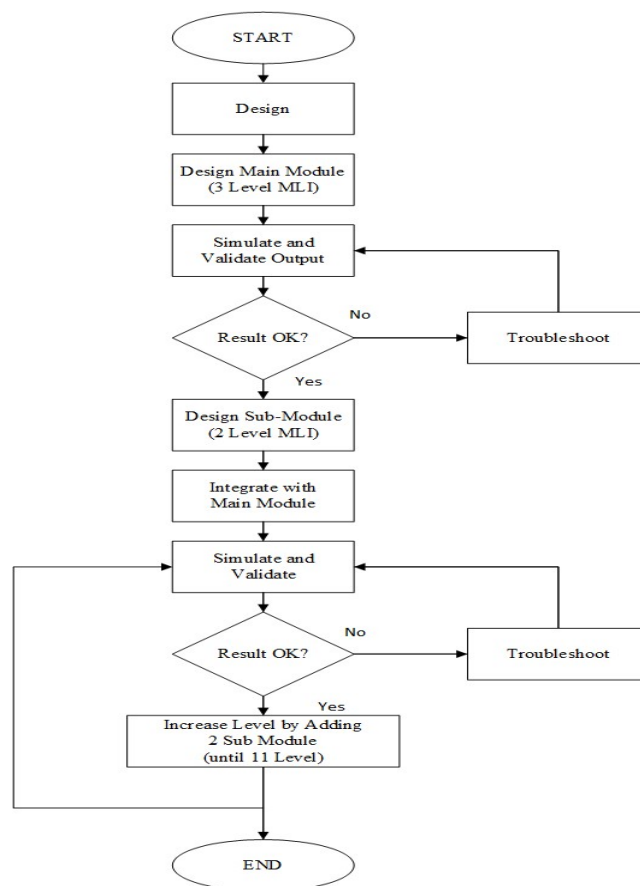

Figure 5. Flowchart of the Research

In this research the PLECS software will be used. This software is similar to the MATLAB Simulink but PLECS is simpler. Besides this software require a less storage than MATLAB Simulink which has bigger files. PLECS also provided better parameter option for each component in simulation thus make the designing and simulation process easier. In this research the 3-level MLI were used. This 3-level MLI will be the main circuit for MLI module. Another reason why 3-level MLI were chosen instead of 2-level MLI was the waveform of 3-level MLI were more sinusoidal than

2-level MLI waveform. Figure 6 shown the research designs the MLI circuit for 3 phase application. For these 3 phases the number of IGBT become 12 in the circuit.
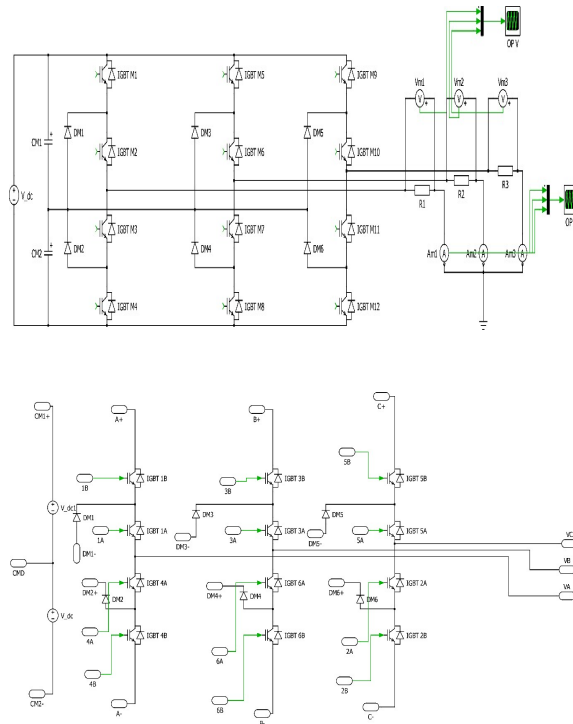

Figure 6. MLI circuit for 3 Phase Application

4. Results

The circuit consist of 12 switches with 12 switching signals. By using pulse generator, the switching signal with different duty cycle and phase delay is entered. The voltage source is 100V and the capacitor is replaced by 25V voltage source to simulate the voltage levels by capacitor. As shown in Figure 7 the voltage output for 3 level is recorded. They are flowing smoothly and didn't show any break.
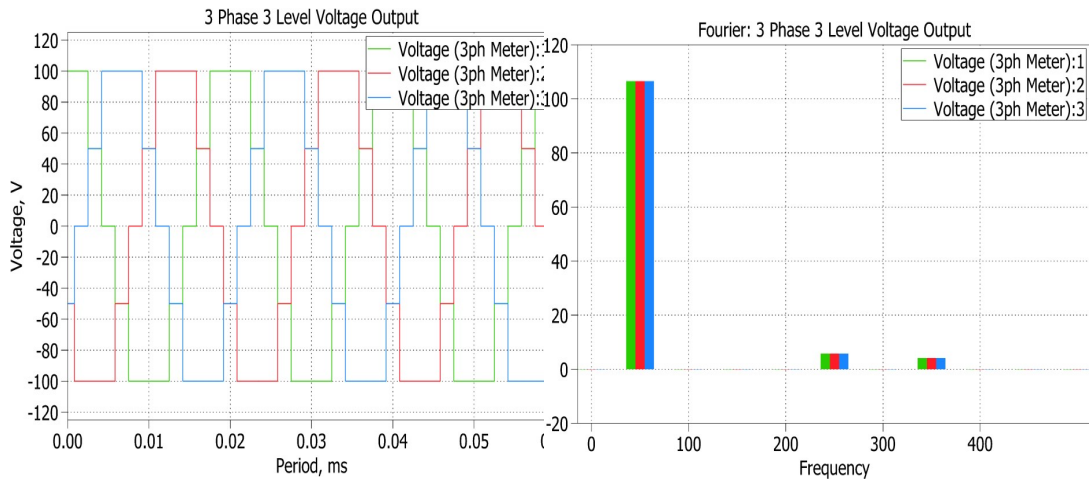

Figure 7. The Fourier Spectrum for 3 Level NPC MLI

5. Conclusion

The Neutral Point Clamped Multilevel Inverter module shows that as the inverter level increases, the THD also decreases accordingly. The 3th harmonics found in the system can be reduced by using filters. Levels can be raised further over 11 levels to get a lower THD by using the MLI NPC module. Although THD is still high compared to other switching techniques this technique will be able to compensate by using a high level of MLI NPC. But using high-level MLI NPCs will increase the cost of the system. The switching for this circuit can be further enhanced to reduce THD even at lower levels.

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