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The Bias Dependence of CMOS 1/F Noise Statistics, its Modeling and Impact on RF Circuits

Mete Erturk
University of Vermont

THE BIAS DEPENDENCE OF CMOS 1/F NOISE STATISTICS, ITS MODELING AND IMPACT ON RF CIRCUITS

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Mete Erturk

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Dissertation Examination Committee:

Tian Xia, Ph.D. — Advisor

William F. Clark, Ph.D. — Committee Member

Walter J. Varhue, Ph.D. — Committee Member

Stephen Titcomb, Ph.D. — Committee Member

Helene M. Langevin, Ph.D. — Chairperson

Frances E. Carr, Ph.D. — Vice President for Research and Dean of Graduate Studies

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Abstract

In the last decade, wireless network routers, multi-media devices with Bluetooth© or similar communication capabilities, mobile cell-phones, and other "RF" devices have found widespread use in the consumer market. The integration and cost advantages of CMOS-only chips have attracted circuit designers in academia and industry, and CMOS technology is now a strong contender along with BiCMOS, and III-V semiconductors for analog / mixed signal and radio frequency applications. RF CMOS technology has numerous advantages that come with the feasibility of system-on-chip. These advantages include reduced fabrication cost and reduced pin count due to die sharing between analog and digital portions. Perhaps the most critical disadvantage of RF CMOS is the very high 1/f noise levels observed in MOSFETs in comparison to BJTs (bipolar-junction transistor). The silicon – silicondioxide interface is crucial to the operation of all MOSFETs, and unlike bipolar devices, MOSFETs are largely surface conductive devices, with device current flowing at or near the interface. This leads to the large 1/f noise associated with FETs. There has been on-going research to study the physical mechanism of 1/f noise. The compact models used to predict device noise in circuit simulations have also been improved.

It has recently been observed that 1/f noise increases during the lifetime of a transistor. Also, large statistical variations in noise level have been reported. The existing models fail to explain such variability in 1/f noise. The work presented here extends the state-of-the art of 1/f noise modeling through experimental and theoretical analysis of noise reliability and statistics. A new model is developed based on a novel theory that investigates the relationship between the spatial profile of interface traps and the bias dependence of 1/f noise. The theory is tested against device noise measurements, as well as RF circuit phase noise measurements.

Acknowledgements

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Table of Contents

List of Tables

List of Figures

1. Introduction

The primary motivation behind this dissertation is presented in this section.

1.1 RF CMOS and System-On-Chip

In the last decade, wireless network routers, multi-media devices with Bluetooth© or similar communication capabilities, mobile cell-phones, and other "RF" devices have found widespread use in the consumer market. The integration and cost advantages of CMOS-only chips have attracted circuit designers in academia and industry, and CMOS technology is now a strong contender along with BiCMOS, and III-V semiconductors for analog / mixed signal and radio frequency applications.

Since practically every electronic system has a digital portion, and virtually all modern digital circuits are implemented in CMOS, use of MOSFETs for the entire system makes single chip radios, very compact circuit boards, and low-cost high-performance systems a possibility. CMOS technology has numerous advantages that come with the feasibility of system-on-chip. These advantages include reduced fabrication cost and reduced pin count due to die sharing between analog and digital portions. Additionally, foundry offerings of CMOS technologies are beginning to include high-Q passives such as varactors, MIMs, and thick-metal inductors. Accurate device models intended for use in analog circuits and libraries for standard digital / analog circuit blocks are now part of foundry design kits for CMOS technologies.

1.2 RF CMOS Challenges

There are many reasons to prefer a pure CMOS technology over BiCMOS or III-V technologies. However, as in all aspects of engineering, there are some trade-offs some 'pros & cons' to be considered. For instance, MOSFETs have limited linearity and gain when compared to bipolar transistors. Gate leakage is another major problem for ICs implemented in recent technology nodes such as 65nm and 45nm CMOS. Technology scaling leads to a reduction in gate dielectric thickness, which increases the leakage current between the transistor gate and channel. Substrate noise coupling within various segments of the system-on-chip is particularly challenging for pure CMOS designs since fast-switching digital circuits share the same die with sensitive analog components. Modern bipolar transistors utilize Silicon Germanium base regions and typically have higher unit-gain-frequency (f_t) than MOSFETs making them more suitable for high frequency applications. The f_t advantage of SiGe HBTs also implies that for a given frequency of operation, the MOSFET will require larger current and hence more power. Most of the limitations of the CMOS technology can be addressed by offering multiple "flavors" of the FET in a foundry technology offering. Within the same lithography node, many types of MOSFETs can be built on the same wafer. Oxide thickness, threshold voltage, and doping profiles can be effectively "tuned" to create a range of behaviors capturing conflicting needs of area, speed, mismatch, linearity, and noise.

However, in most cases the fundamental device structure of the transistor can not be altered without prohibitive cost. The silicon – silicondioxide interface is crucial to the

operation of all MOSFETs, and unlike bipolar devices, MOSFETs are largely surface conductive devices, with device current flowing at or near the interface. This leads to the high levels of low-frequency noise associated with FETs, perhaps the most critical disadvantage they have over bipolar transistors. Low-frequency noise can be a limiting factor for VCO's, mixers, PLLs, and the popular direct conversion (zero-IF) receiver architecture.

1.3 Impact of Low-frequency Noise on Circuits and Systems

Low-frequency noise must be kept to a minimum in many circuits and systems. Particularly, the Voltage Controlled Oscillator (VCO) is a circuit that is highly susceptible to transistor low-frequency noise. VCOs are used in many systems, with the most common usage being as part of a frequency synthesizer in RF transmitters and receivers. The low phase noise requirement of the VCO is often a critical design specification that can be challenging to achieve with low-cost on-chip RF CMOS components. A widely used VCO schematic is shown in Figure 1.1.

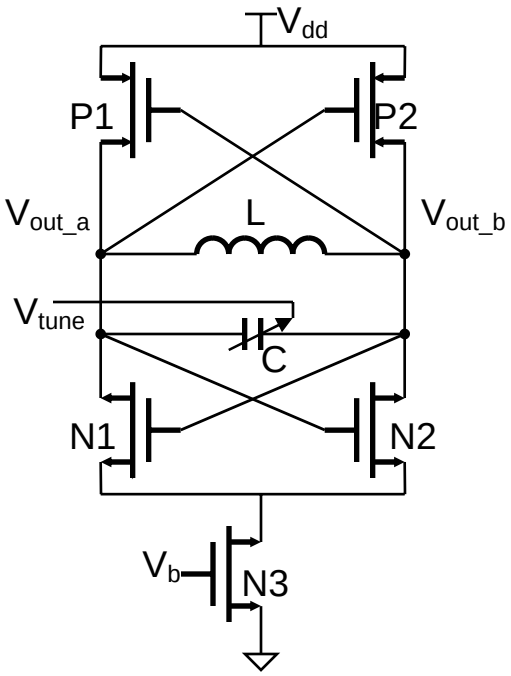


Figure 1.1: LC tank based VCO schematic commonly used in RF CMOS systems.

Transistor N3 is used as the tail current source driving the cross-coupled complementary differential pairs of N1-N2 and P1-P2. The oscillation frequency is equal to:

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} \tag{1.1.}$$

The variable capacitor (C) coupled with the on-chip inductor (L) constitute the resonance tank. The low-frequency noise of the transistors used in the VCO contributes to phase noise in a number of ways.

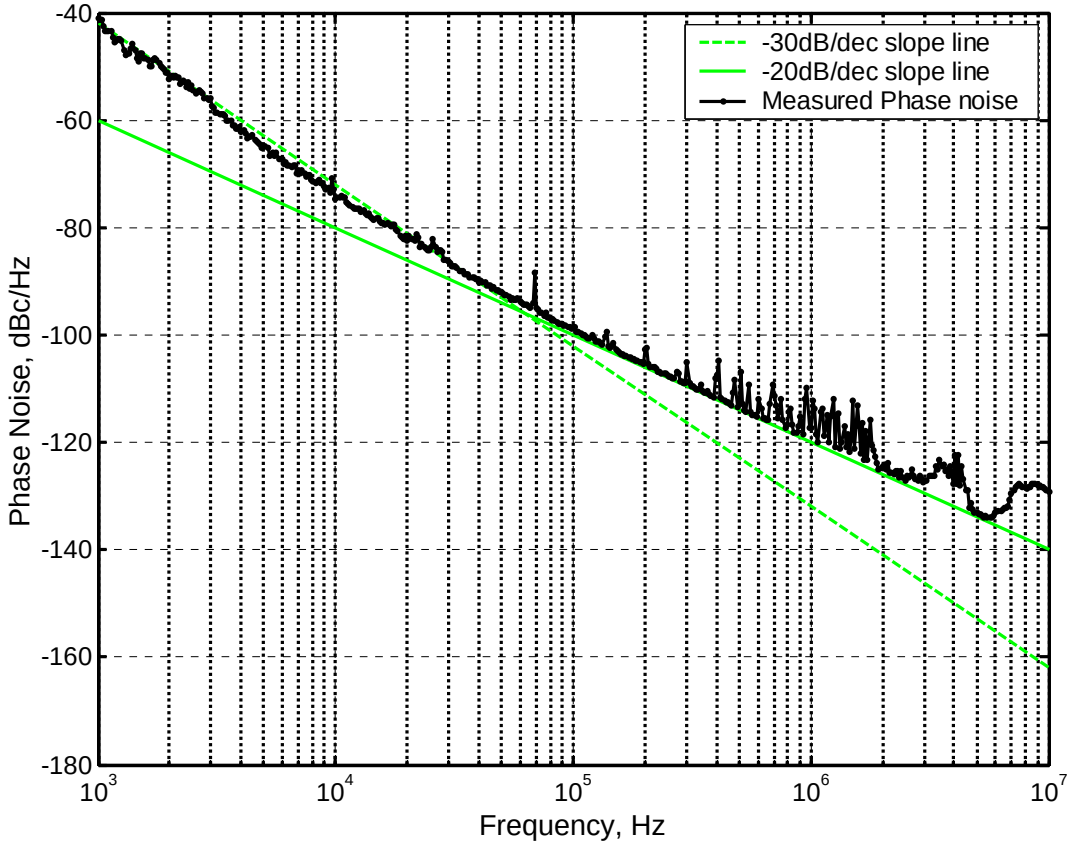


Figure 1.2: VCO measurement illustrating the two distinct regions in phase noise.

Any noise in the current source (N3) will be up-converted to phase noise due to the mixing behavior of the cross coupled differential pair. Therefore low-frequency noise in N3 directly contributes to VCO phase noise. Furthermore, the oscillation frequency is a function of the common-mode voltage drop across the variable capacitor, through the voltage dependent capacitance in equation 1.1. Low-frequency noise of the transistors in the circuit modulates the common-mode voltage at the output nodes of the VCO. Therefore, the oscillation frequency is modulated yielding increased phase noise. Typical

phase noise plot of a VCO shows two distinct regions with a "-30dBc/dec slope region due to the low-frequency noise in the system and a "-20dBc/dec slope" region due to the white noise in the system. Figure 1.2 shows a 0.13um RF CMOS VCO we have designed and characterized the two regions of phase noise are shown. Device low-frequency noise directly contributes to the "close-in" phase noise, as observed in frequencies up to about 60kHz.

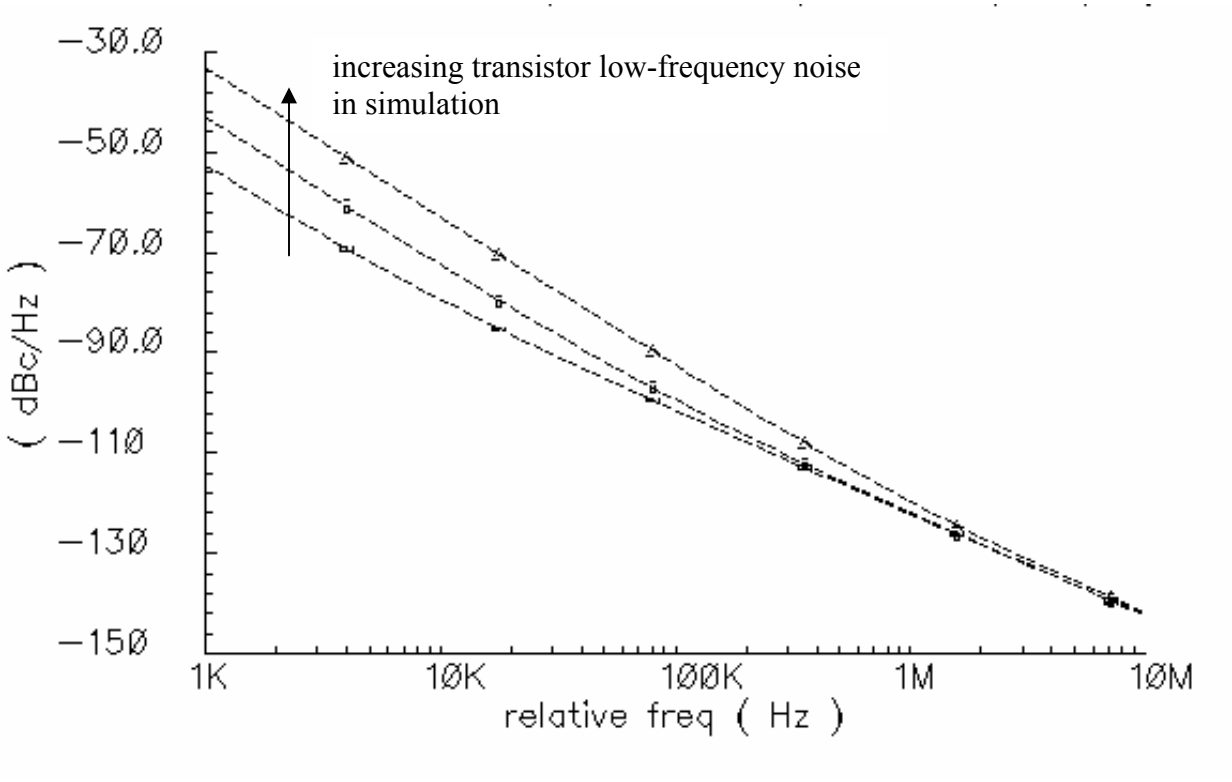


Figure 1.3: SpectreRF© simulation showing the impact of transistor low-frequency noise on VCO phase noise.

In Figure 1.3 the impact of increasing transistor low-frequency noise on VCO phase noise is shown with 3 different simulations. In each simulation, the low-frequency noise level

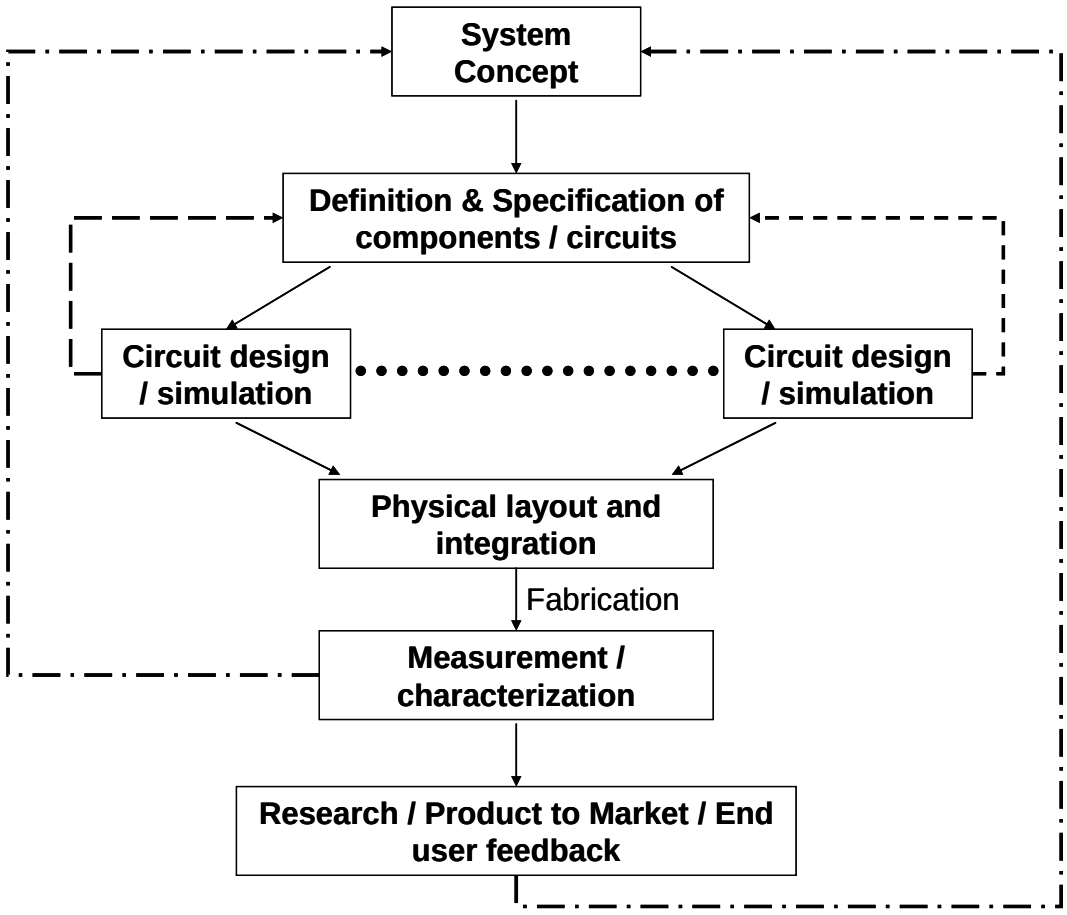
of the active devices is altered by adjusting the BSIM model parameters. Note that the close in phase noise increases with increasing device low-frequency noise. There are circuit techniques to reduce the contribution of transistor low-frequency noise to VCO phase noise [Hajimiri, 1999]

VCOs are not the only components of an analog / RF system susceptible to transistor low-frequency noise. Any circuit that relies on the mixing of a DC current level to produce an output must be designed with low-frequency noise in mind. At the system level, the popular direct conversion transceiver architecture (also known as Zero-IF) particularly suffers from transistor low-frequency noise. This is because for this system most of the processing takes place in the part of the frequency spectrum where low-frequency noise is dominant. Therefore low-frequency noise limits performance not only by means of up-conversion as in the VCO, but directly due to the overlap between noise spectrum and signal spectrum.

It is critical that transistor low-frequency noise is mitigated as much as possible through improved manufacturing and device design. An improved understanding of the technology scaling of low-frequency noise is essential for better defining future circuits and systems. Perhaps just as crucial is the need for accurate device models that can predict all aspects of low-frequency noise including reliability and statistical site-to-site variation.

1.4 Compact Modeling and Design Kits

A typical integrated circuit design flow can be summarized with the following flow chart:



Design kits are generally used in the circuit simulation and layout stages. A scalable compact model and a parameterized graphical cell are provided for each device used in the circuit. The accuracy of the compact models is very important for successful design of integrated circuits.

In terms of MOSFET low-frequency noise, the device model must accurately predict the noise power spectral density at a given frequency. The dependence of the noise power to device size and operating bias (such as the drain, gate, source, and body voltages) must be captured in the model. Furthermore any change in the noise level over the usage of the transistor (reliability) and any uncertainty in the noise level due to random variations among devices (statistics) must be accounted for.

1.5 Dissertation Organization

This dissertation is devoted to the analysis and modeling of low-frequency noise in modern MOSFETs, particularly its reliability and statistics. Chapter 2 presents the current models used to predict or simulate MOSFET low-frequency noise, and discusses their strengths and limitations. In chapter 3, we discuss the impact of technology scaling on MOSFET low-frequency noise. Chapter 4 and 5 deal with modeling aspects of low-frequency noise not currently considered in existing models, namely the reliability of low-frequency noise and the statistical variations in low-frequency noise. Based on the insights gained, we provide detailed analysis of the gate voltage and inversion layer spatial profile dependence of low-frequency noise statistics in chapter 6. The question of the relationship between gate bias and site-to-site noise variation is answered. We provide a means of capturing the bias dependence of noise variation within the BSIM framework. In section 7, the impact of transistor 1/f noise on RF CMOS VCO phase noise is studied. Phase noise measurements are compared to simulation results using various 1/f noise models. Finally, in section 8 we conclude this dissertation and suggest future work.

2. Classical Models for MOSFET Low-Frequency Noise

2.1 Noise Modeling

The drain current of a MOSFET exhibits noise spectrum that typically consists of two distinct regions. From DC up to a certain corner frequency (f_c) the noise spectrum is roughly inversely proportional to frequency. Low-frequency noise is therefore also called 1/f noise, or flicker noise. f_c is a function of transistor size, quality of the Si – SiO_2 interface, oxide thickness, and noise measurement conditions such as gate and drain voltages. The noise observed for frequencies less than f_c (low-frequency noise) is the main topic of this study. Beyond f_c thermal noise with its characteristic white (flat) spectrum is observed.

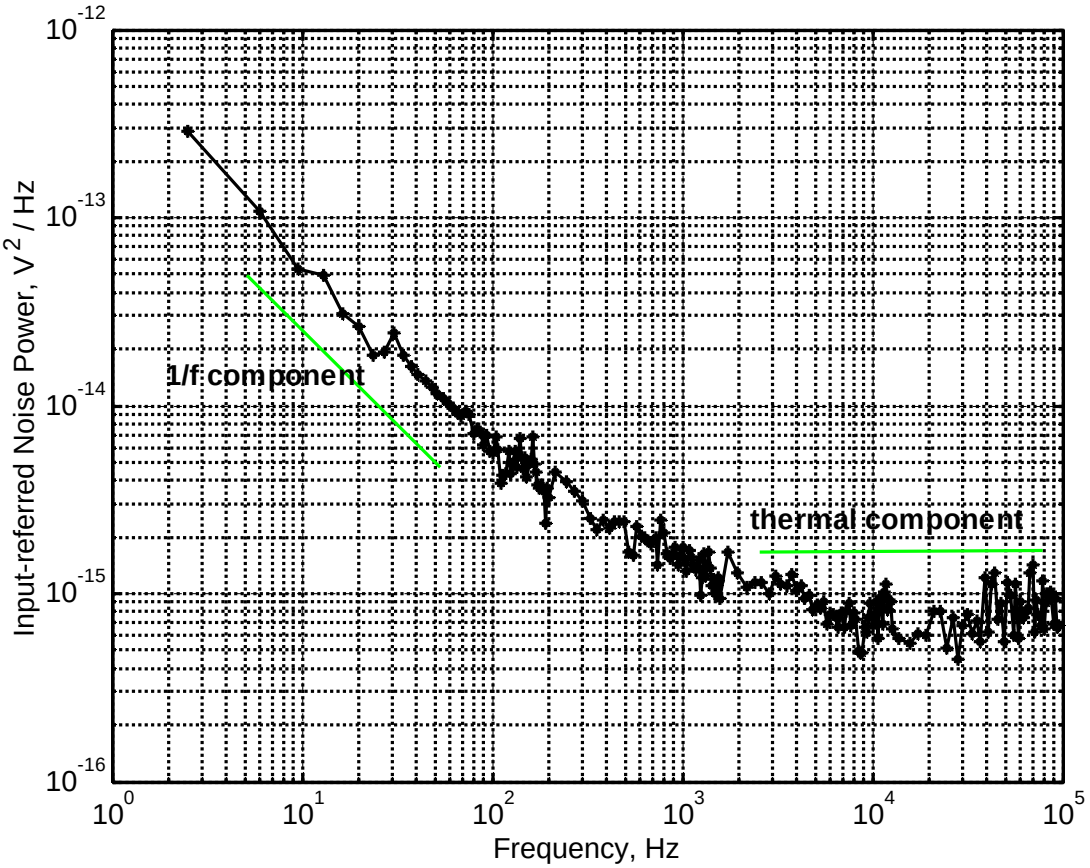


Figure 2.1: Measured low-frequency noise, fc ≈ 2kHz, 0.18μm CMOS, W=100μm, L=1μm, Vgs=0.45V Vds=1V.

For the purposes of analysis, modeling, and simulation, there are two ways of representing the MOSFET noise. These are the "input-referred noise", or S_{vg}, and "output-referred noise", or S_{id}. As shown in Figure 2.2 S_{vg} is a measure of the noise power of a voltage source to be placed in series with the gate voltage of a noiseless MOSFET, whereas S_{id} is a measure of the noise power of a current source to be placed in parallel with the drain current of a noiseless MOSFET. S_{id} and S_{vg} are related with the device transconductance, or:

$$S_{vg} = \frac{S_{id}}{g_m{}^2} \tag{2.1.}$$

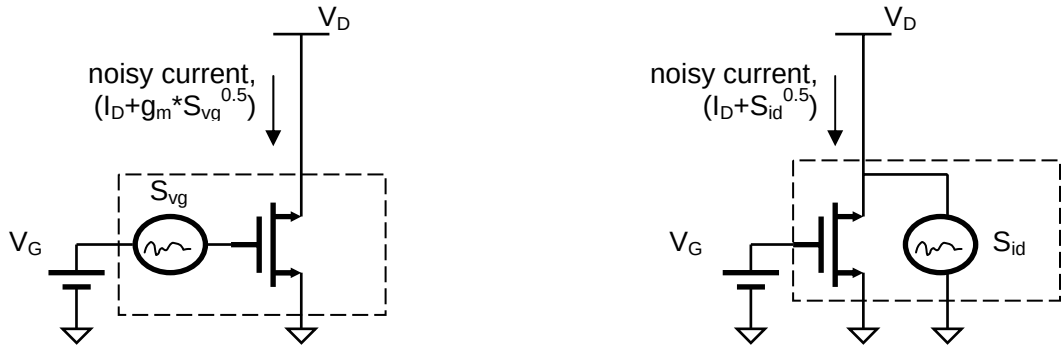


Figure 2.2: Equivalent representations of noise, showing input-referred and output-referred noise sources.

Note that the current in a MOSFET is proportional to the mobility of carriers, μ, and also proportional to the number of free carriers, N. Therefore the fluctuations in the current can be caused by the stochastic perturbations in either, or both, of these parameters. In fact over the years two schools of thought have emerged on the physical basis of 1/f noise and these are the so called Number Fluctuation Theory and the Mobility Fluctuation Theory.

2.2 McWhorter's number fluctuation theory

Perhaps the most striking aspect of low-frequency noise is its frequency dependence. Why does the noise in the drain current of a MOSFET have a power spectral density that is roughly inversely proportional to frequency? The number fluctuation theory initially proposed by McWorther [McWorther, 1957] for the 1/f noise observed in germanium

assumes that the origin of the fluctuations is the tunneling of charge carriers at the semiconductor interface to and from traps which are located in the oxide close to the interface. Each trapping / detrapping event will lead to discrete fluctuations in the current, such that for a single trap, the observed current fluctuation would resemble a random telegraph signal, with two possible states, high and low, and two time constants corresponding to the average high time and the average low time. In fact, we now observe such phenomena in very small area transistors [Celik-Butler, 2000], and it has been appropriately termed as RTS (random telegraph signal). The spectrum of such a two-parameter random signal was first studied by Machlup [Machlup, 1954], and revisited in terms of its relevance to MOSFET 1/f noise by Kirton and Uren in [Kirton, 1989]. Such RTS is shown to have a power spectrum given by:

$$S(f) = \frac{4(\Delta I)^2}{(\tau_0 + \tau_1)\left[\left(\frac{1}{\tau_0} + \frac{1}{\tau_1}\right)^2 + (2\pi f)\right]} \tag{2.2.}$$

where τ_0 and τ_1 are the two time constants corresponding to the average high and low times, and ΔI is the amplitude of current fluctuation. In McWorther's model, he associates a single tunneling time constant to each trap (such that in (2.2) τ_0 and τ_1 are equal) and that this time constant varies with distance x from the interface where:

$$\tau = t_0 \cdot e^{\gamma \cdot x} \tag{2.3.}$$

The tunneling parameter γ is of the order of 10^8 cm^{-1} and the attempt time t_0 is approximately 10^{-10} s for the Si-SiO_2 interface [Simoen, 98]. McWorther's model also assumes that there is a uniform (in space) trap density parallel to the interface. Then the power spectral density in the total number of carriers in an elemental area ($\Delta y \Delta z$) can be arrived at by integrating the contribution of the traps across space and energy:

$$S_N(f) = 4\int_0^{x_1}\int_{E_v}^{E_c} N_{ot}(E)\cdot f_T(E)\cdot(1-f_T(E))\cdot\frac{\tau_1}{1+(2\pi f\tau_1)^2}\cdot\Delta y\cdot\Delta z\cdot dE\cdot dx \quad (2.4.)$$

In (2.4) $N_{ot}(E)$ is the density of traps with energy E, $f_T(E)$ gives the electron occupation probability of the trap with energy E, x1 is the vertical coordinate beyond which the trap contribution to 1/f noise is negligible. Note that the product $f_T(1-f_T)$ is sharply peaked within a few kT of the surface Fermi level. As shown by McWorther [McWorther, 1957], (2.4) reduces to a 1/f like spectrum for a sufficient spread in the time constants, τ_1. McWorther's model assumes a distribution of tunneling time constants due the uniform distribution of traps in the spatial plane parallel to the Si-SiO_2 interface.

The number fluctuation power spectral density derived in (2.4), can be used to obtain a current noise spectral density for a MOSFET in linear region [Christensson, 1968; Reimbold 1984]. The drain current fluctuations in the elemental area $\Delta y \Delta z$ can be expressed as [Simoen, 1999]:

$$\Delta I_D = \frac{\mu V_{DS} q \delta N \Delta y \Delta z}{L^2} \tag{2.5.}$$

and the drain current noise power spectral density is:

$$S_{id} = \left(\frac{I_D}{WL}\right)^2 \frac{q^2}{C_{ox}{}^2 (V_{GS} - V_T)^2} S_N \tag{2.6.}$$

where C_{ox} is the gate oxide capacitance per cm^2, V_{GS} the gate voltage, V_T the threshold voltage. Note that often low-frequency noise is reported input-referred (gate referred), which can be extracted from (2.6), by dividing the current noise with the square of the transconductance, g_m:

$$S_{vg} = \frac{S_{id}}{g_m{}^2} = \frac{q^2 S_N}{(WLC_{ox})^2} \tag{2.7.}$$

In (2.7) we assume the drain to source voltage is small and therefore $g_m = I_D/(V_{GS}-V_T)$. Finally, combining (2.7) and (2.2), assuming that the trap density is uniform in energy, and utilizing the fact that $f_T(1-f_T)$ is only non-zero within a few kT of the surface Fermi level E_F, we can arrive in the following expression for the input-referred low-frequency noise power spectral density for a MOSFET (given in V^2/Hz) [Simoen, 1999 and Jayaraman, 1989]:

$$S_{vg} = \frac{kTq^2}{8WLC_{ox}\alpha_t}\frac{N_{ot}(E_F)}{f} \tag{2.8.}$$

The expression for the input-referred noise given by (2.8) predicts no gate bias dependence. According to (2.8), as long as the transistor is biased in strong-inversion and in the linear region of operation, noise measurements under different gate voltages should yield the same noise power. However experimental data show the contrary. pFETs generally show a strong gate bias dependence for S_{vg}, and sub-micron nFETs are seen to exhibit some variation in the noise level under different gate voltages. In Figure 2.3 noise data from various 0.13μm nFETs and pFETs are shown. Note the strong increase in the input-referred noise level for the pFETs. The nFETs also show an increase with increasing gate bias.

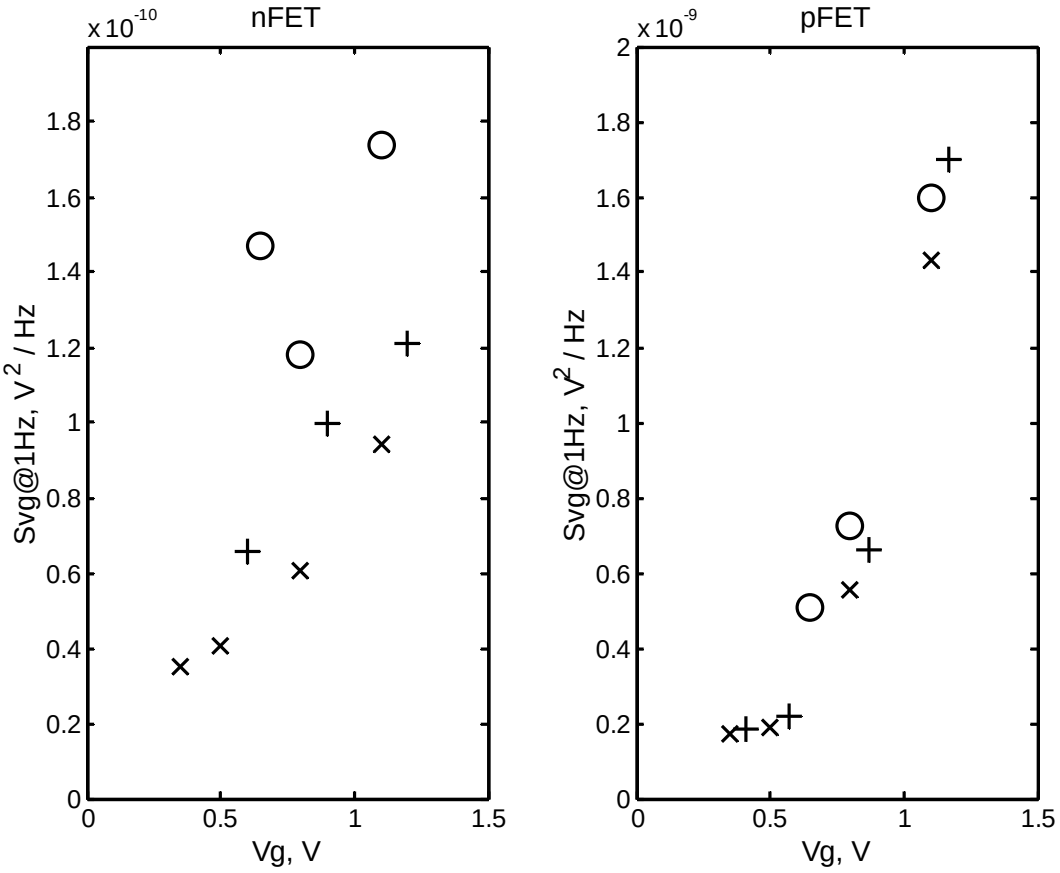


Figure 2.3: Measured input-referred noise from 0.13μm nFETs and pFETs. (+) standard devices, (o) low-power devices, (X) low-threshold-voltage devices.

Such experimental findings led to the challenging of the number fluctuation theory of MOSFET low-frequency noise, since it was unable to capture the gate-bias dependence of the input-referred noise power.

2.3 Hooge's mobility fluctuation theory

In this model, the drain current noise is attributed to fluctuations of the carrier mobility [Hooge, 1981 and 1982]. The physical basis for the mobility fluctuation can be due the fluctuations of the scattering cross section entering the collision probability [Ghibaudo, 1991], however the mobility fluctuation theory is generally accepted to be purely empirical in nature. Hooge had observed that the current noise spectral density for a range of materials could be represented by an empirical relationship:

$$\frac{S_I}{I^2} = \frac{\alpha_H}{Nf} \tag{2.9.}$$

where N is the total number of carriers contributing to conduction, and α_H is Hooge's empirical constant. Initially, α_H was proposed as universal constant valid for all materials, with a value of approximately 10^{-3}, however nowadays α_H is considered a fitting parameter, taking on different values for different materials and even different processing of the same material. For example the same material would have a high value for α_H if it has a large number of defects and a low value for α_H if it has a crystalline form and few defects. For silicon, values have been found in the range $5\text{x}10^{-6}$ to $2\text{x}10^{-3}$ [Hooge, 1994]. Hooge's mobility fluctuation theory can be adapted for the 1/f noise of a MOSFET in linear operation, which yields [Hooge, 1994 and Van Damme, 1994]:

$$S_{vg} = \frac{q\alpha_H}{C_{ox}WLf}(V_{GS} - V_T) \tag{2.10.}$$

which predicts a linear dependence on the gate overdrive voltage (V_{GS}-V_T). Due to this gate bias dependence in the Hooge model, it has been proposed as an alternative to the number fluctuation model, especially to be used for pFETs. The physical reasoning behind using separate models for nFETs (where the number fluctuation theory is more appropriate) and pFETs (where the mobility fluctuation theory shows better agreement with data) was based on the fact that pFETs were considered bulk, or buried channel, devices, whereas nFETs are surface channel devices. This is true when the same n+ polysilicon gate material is used for both pFETs and nFETs. However, in modern sub-micron CMOS technologies, both pFETs and nFETs function as surface channel devices since nFETs use an n+ polysilicon gate and pFETs use a p+ polysilicon gate. Therefore, it is no longer scientifically sound to have two separate models for the nFET and pFET low-frequency noise.

The mobility fluctuation theory predicts a 1/N dependence for the normalized current noise as given in (2.9), which indicates that in the subthreshold regime the noise should increase exponentially. Experimental data however usually does not agree with this prediction of (2.9) for the subthresold regime [Simoen, 1999]. The other often cited issue with the mobility fluctuation model of low-frequency noise, is the empirical nature of the Hooge parameter a_H. There is no widely accepted theory to explain the wide range of

values reported for α_H, which may suggest that the Hooge mobility fluctuation theory when applied to MOSFET 1/f noise should be considered a purely mathematical construct without any physical basis.

2.4 Reevaluation of the Problem Based on First Principles

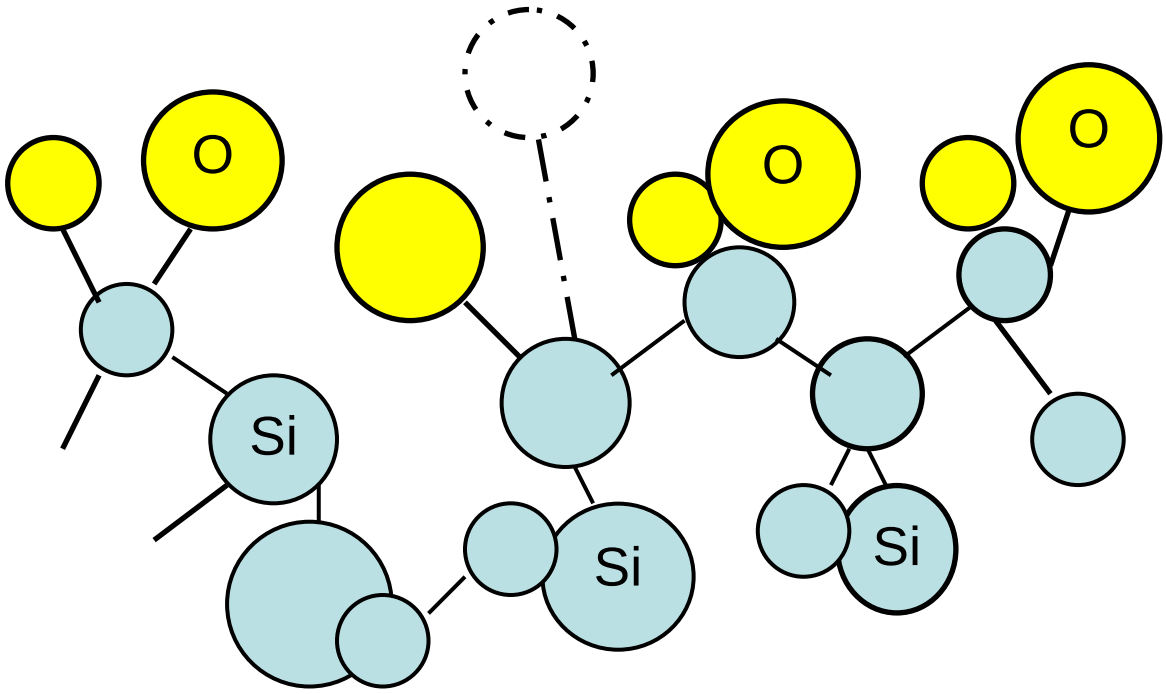


Figure 2.4 : Dangling bond (dashed) shown at the interface between Silicon and Silicon Dioxide.

There is strong evidence on the correlation between carrier traps and low-frequency noise of MOSFETs. Carrier traps emerge from local 'imperfections' within the device dielectric, at the dielectric-semiconductor interface, and within the semiconductor, where a charge carrier has a probability of being trapped or captured, removed from conduction

for a period of time, and released or emitted back to the channel. A somewhat rudimentary representation of an interface trap is shown in Figure 2.4. A “dangling bond” of Silicon is one that is not bound to an Oxygen or another Silicon atom, ready to accept an electron. Typically in device processing, the number of such dangling bonds is kept at a minimum since they affect device characteristics in unwanted ways [Pierret, 1996]. Standard process includes a high temperature anneal with a Hydrogen based gas, where such “active” bonds are passivated by Hydrogen atoms. However, it is impossible to remove all dangling bonds from the interface.

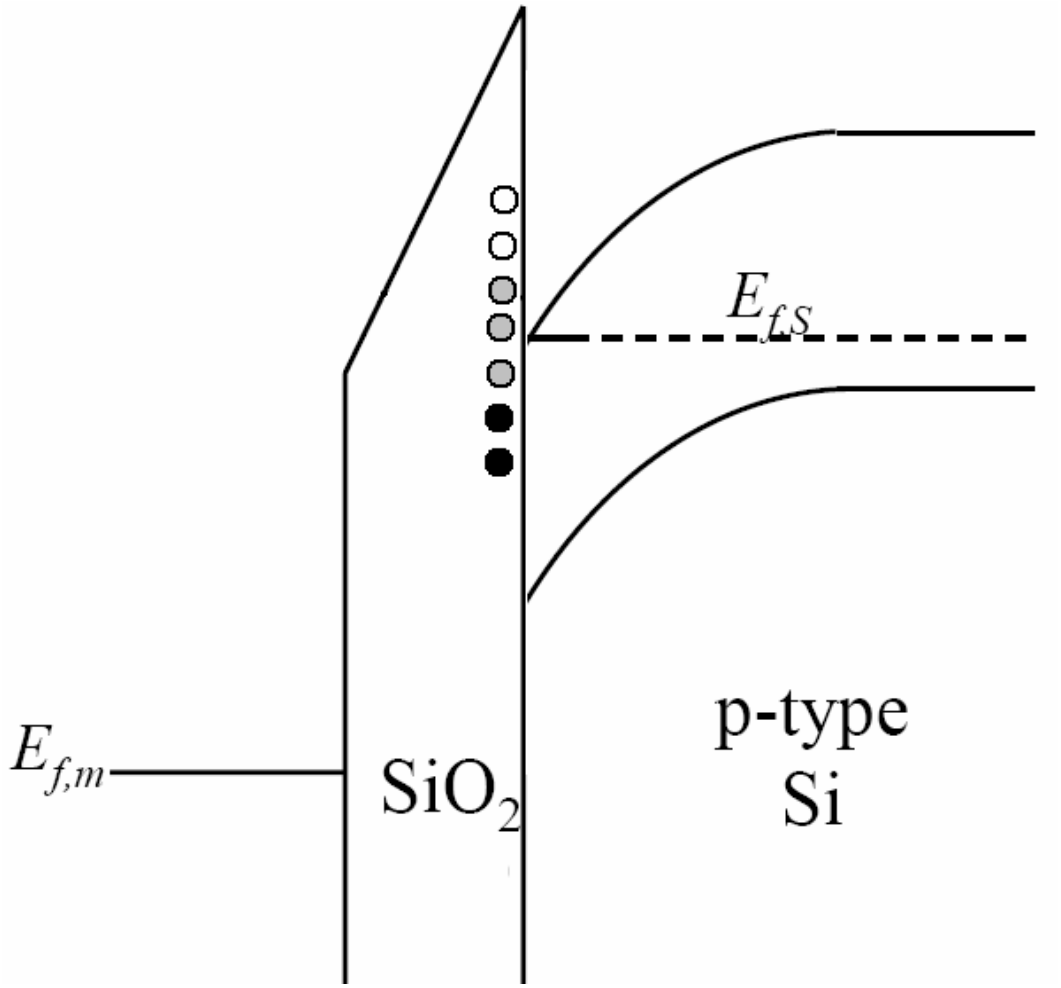


Figure 2.5 : Band-diagram representation of the MOS structure with carrier traps.

In Figure 2.5, a band diagram representation of the MOS structure with carrier traps in energy is shown. The traps with energy levels significantly below the quasi-Fermi level at the surface (E_{fs}) will be all filled with carriers (black circles) whereas the traps with energy levels significantly above E_{fs} will be empty (white circles). The traps with energy levels within a few kT of E_{fs} (grey circles) however will have a probability of being filled or empty, and therefore they act as active charge traps with capture and emission events taking place, affecting device current.

Each capture or emission modulates the total current with a Lorentzian power spectrum. Given that there are traps of various energy levels, spatial locations, and time constants, there is an ensemble of Lorentzians affecting transistor current. Figure 2.6 shows 6 such Lorentzians and their sum, which has roughly a 1/f slope.

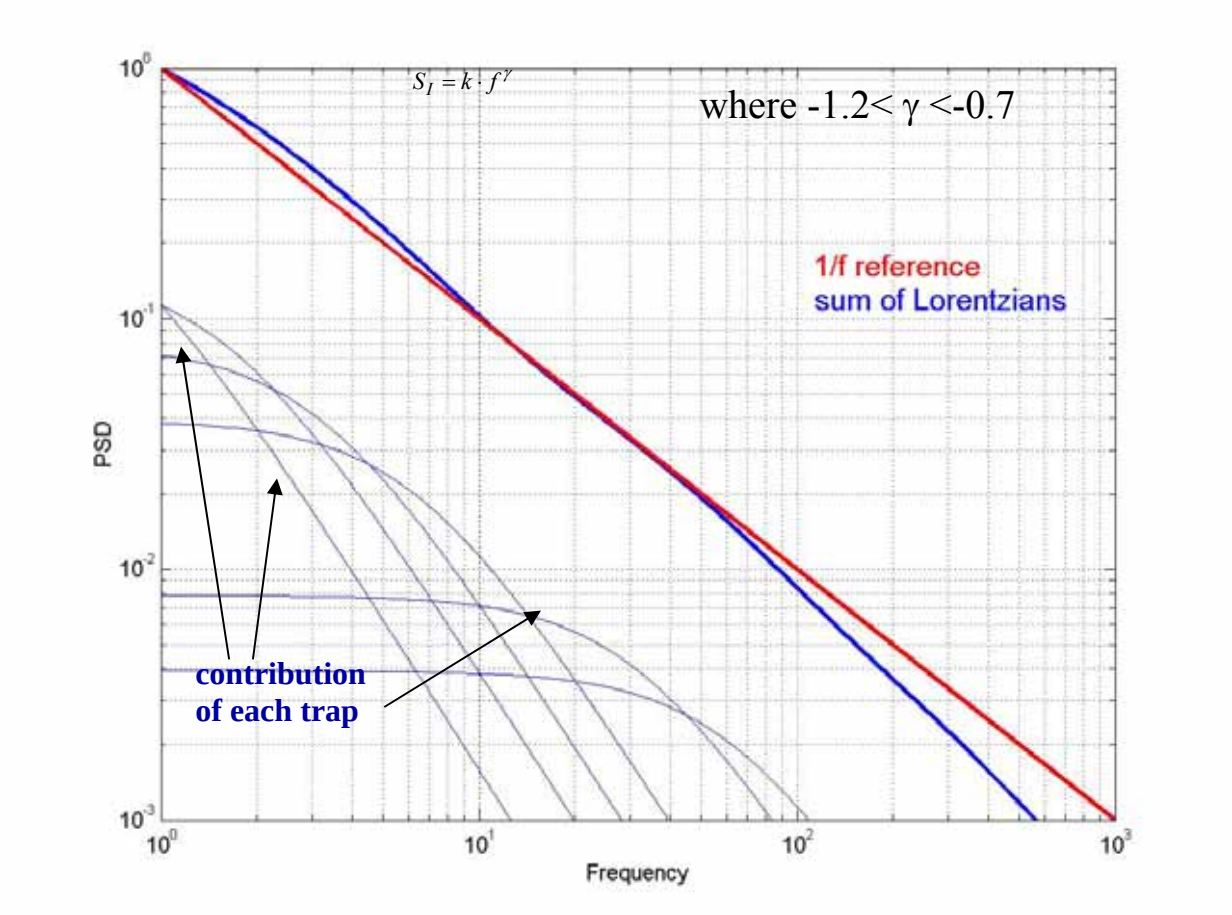


Figure 2.6 : Sum of Lorentzians add up to 1/f like spectrum.

Thorough understanding of how a trapped carrier affects device current is a matter of ongoing research. Particularly trap location along the transistor channel length requires a careful analysis because, along with the spatial inversion profile, the relevance of the trap in terms of its contribution to device noise, is bias dependent.

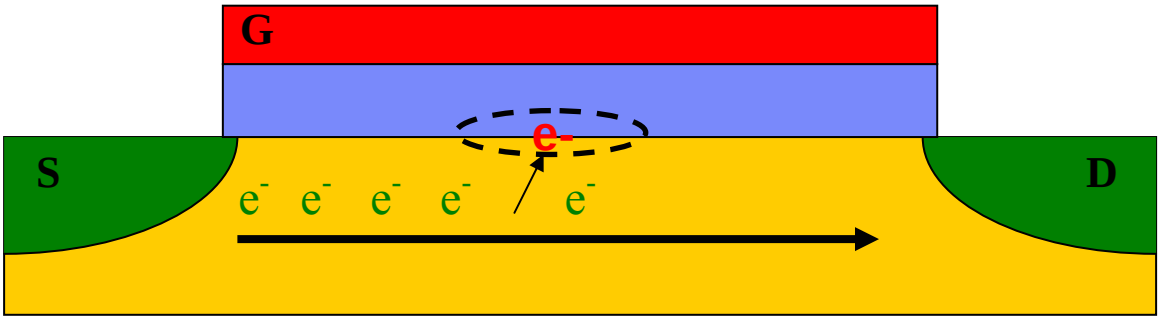


Figure 2.7 : FET cross section with number and mobility of carriers modulated due to trapped charge.

A trapped electron is shown in the FET cross section in Figure 2.7. The trapped charge reduces the number of carriers available for conduction due to a modulation in the flat-band voltage. It also affects local channel mobility due to Coulomb scattering events.

2.5 Unified (Correlated) Low-Frequency Noise Models

Since the number fluctuation theory alone fails to explain the gate bias dependence observed in the low-frequency noise, and the mobility fluctuation theory alone is empirical in nature and often over predicts the gate bias dependence, theories that combine the two have been studied by several groups [Mikoshiba, 1982; Hung, 1990;

Ghibaudo, 1991]. The findings on the RTS of small area devices also supported the unified theories since it was demonstrated that the high amplitudes of the current perturbation can not be explained by the simple reduction of the number of free carriers due to a trapping event.

Modern compact models for MOSFETs, based on BSIM4 or MOS Model 11, use the low-frequency noise model that is derived from Hung's unified model for 1/f noise [Hung, 1990]. In this model the carrier number fluctuation model is extended to include the Coulomb scattering of free charge carriers at trapped oxide charge. Consequently, not only the number of carriers in the channel but also the effective mobility in the channel fluctuates. The two phenomena, carrier number fluctuation and mobility fluctuation are therefore correlated. The input referred noise power spectral density is then given by:

$$S_{vg} = \frac{kTq^2}{\gamma f WLC_{ox}{}^2}(1+\alpha\mu N)^2 N_t(E_F) \qquad (2.11.)$$

where α is a scattering coefficient which is a function of the local carrier density due to the screening effect as well as the distance of the trap from the interface.

While the unified low-frequency noise model has received general acceptance, the scattering coefficient α is shown to require non-physical values in order to fit this model

to various sets of measured data [Vandamme, 2000], and it has been suggested that the unified model lacks physical basis in this regard. Nevertheless, the unified noise model has been implemented into MOSFET models and is used by analog/mixed signal and RF circuit designers.

2.6 BSIM Implementation

In the present BSIM implementation, correlated carrier number and mobility fluctuations are assumed to be the source of MOSFET flicker noise. Since the BSIM model is an extension to the number fluctuation theory, an apparent trap density (N_t) is defined to give the same level of noise in the absence of mobility fluctuations [Hung, 1990]. Three fitting parameters are used to attain N_t:

$$N_t = NOIA + NOIB \cdot N_{inv} + NOIC \cdot N_{inv}^2 \tag{2.12.}$$

with N_{inv} being the inversion carrier density. The noise level at a given bias condition is modeled to be proportional to N_t. To a first-order, it can be said that parameter NOIA contributes to noise at all bias conditions, and parameters NOIB and NOIC contribute to noise at higher gate voltages. To model MOSFET flicker noise, one has to determine the values for NOIA, NOIB, and NOIC that gives the best fit to measured data. The bias dependence of the input-referred noise power (Svg) is captured by the relative values of the three fitting parameters. For example, for devices where there is a strong increase in

Svg at high gate voltages, the ratio of NOIC/NOIA would be high in comparison to its value for devices where there is a weak increase in Svg at high gate voltages. Parameters NOIB and NOIC are introduced because the original number fluctuations theory does not predict any increase in Svg with respect to increased gate bias.

The final formulation for the noise level takes the following form:

$$S_{vg} = \frac{1}{{g_m}^2}\frac{kTq^2\mu_{eff}I_{ds}}{C_{ox}{L_{eff}}^2 A_{bulk} f^{ef} 10^{10}}\left[\begin{array}{l} NOIA\cdot\log\left(\frac{N_0+N^*}{N_l+N^*}\right)+NOIB\cdot\left(N_0-N_l\right)+ \\ \frac{NOIC}{2}\left({N_0}^2-{N_l}^2\right)\end{array}\right] + \frac{1}{{g_m}^2}\frac{kT{I_{ds}}^2\Delta L_{CLM}}{W_{eff}{L_{eff}}^2 f^{ef} 10^{10}}\cdot\frac{NOIA+NOIB\cdot N_l+NOIC\cdot {N_l}^2}{\left(N_l+N^*\right)^2} \quad (2.13.)$$

where μ_{eff} is the effective mobility at the given bias condition, and L_{eff} and W_{eff} are the effective channel length and width, respectively. The parameter N_0 is the charge density at the source end and N_l is the charge density at the drain end, given by:

$$N_0 = \frac{Cox}{q}\cdot Vgs \quad (2.14.)$$

$$N_l = \frac{Cox}{q}\cdot Vgs\cdot\left(1-\frac{A_{bulk}Vds}{Vgs+2Vt}\right) \quad (2.15.)$$

N^* is another charge term given by:

$$N^* = kT \cdot \frac{Cox + Cd + CIT}{q} \tag{2.16.}$$

where CIT is another BSIM model parameter based on the DC curve and Cd is the depletion capacitance. The details of equation (2.13) can be found in the BSIM manual [BSIM, 2007]. To model 1/f noise, one must extract from data, or determine by some other means the values for *NOIA*, *NOIB*, *NOIC*, and the frequency power *ef*.

3. Technology Scaling of MOSFET Low-Frequency Noise

3.1 Digital versus Analog Scaling

The semiconductor manufacturing technology has held up a remarkable exponential rate of increase in the number of devices that can be crammed in a given area of Silicon. The minimum feature size, which effectively dictates the smallest transistor that can be made, has been halved many times in the last two decades. The economic force driving this scaling has been the demand for more processing capability in microprocessors used in digital computing devices such as main frames, personal computers, and servers. The following table shows typical FET parameters from 4 technology nodes.

Technology Node (nm)	**Vt (mV)**	**Vdd_max (V)**	**Cox (F/m^2)**	**min. WxL (μm^2)**	**Typical peak f_T (GHz)**	**min. WxL for 1mA current source* (μm^2)**
250	500	2.5	0.0059	0.3x0.24	40	171
180	440	1.8	0.0082	0.22x0.18	55	25.4
130	370	1.2	0.0090	0.16x0.12	90	12.8
90	280	1.0	0.0165	0.12x0.08	~150	2.2

Table 1: Summary of CMOS Technology Nodes

*Note that in digital circuits, the minimum attainable device geometry is quite relevant since it often dictates the total number of gates, or amount of memory, that can be implemented for a given area of Silicon. However for analog circuits, minimum sized transistors are hardly ever used due to sensitivity to mismatch, process tolerance, and 1/f noise. Therefore, here we introduce another metric, the minimum transistor area for a diode connected, 1mA current source, biased with 100mV gate overdrive. This is a typical configuration relevant for many analog circuits, such as differential amplifiers, VCOs, etc.

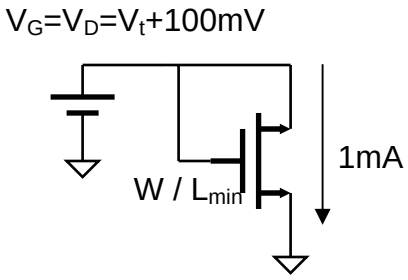


Figure 3.1: Current source used to determine the analog scaling minimum WxL.

3.2 Impact of Scaling on Trap Uncertainty

It is worthwhile to investigate the trend in MOSFET low-frequency noise with respect to technology scaling. Rewriting equation (2.11) with respect to gate voltage and threshold voltage, and assuming a uniform charge distribution we have:

$$S_{vg} = \frac{kTq^2}{\gamma f WLC_{ox}{}^2}\left(1+\alpha\mu\frac{(Vgs-Vt)\cdot C_{ox}}{q}\right)^2 N_t(E_F) \qquad (3.1.)$$

Therefore, the technology scaling induced reduction in the area term ($W*L$) is offset to some extent with the increase in C_{ox}. There is not a drastic increase in 1/f noise with technology scaling. However, as the transistor area is the reduced, the discrete nature of carrier traps has a significant impact on noise reliability and noise statistics. The actual problem with scaling is the increased uncertainty in the number of traps per transistor. This issue is dealt with in the next two chapters.

4. Modeling of Noise Reliability

4.1 Impact of Hot Carrier Stress on MOSFETs

Reliability issues have received considerable attention in the context of digital circuits. Electromigration, dielectric breakdown, and hot-carrier induced on-current degradation have been extensively studied. However, reliability of analog/mixed signal and RF integrated circuits require separate attention. Analog and RF circuits are typically more sensitive to noise and transconductance degradation than digital circuits. The transistors in digital circuits usually operate in the linear region. In contrast, transistors in analog circuits exploit all regions of operation including weak-inversion, triode and saturation. Particularly, under saturation transistors are subject to high drain voltage for fixed amounts of time, making the Drain-Avalanche-Hot-Carrier (DAHC) phenomenon considerably more prominent. To determine the reliability of a transistor with respect to DAHC, devices are subject to hot-carrier stress under maximum substrate current conditions.

4.2 Noise Reliability and Deuterium

As stated in the previous section, the MOSFET 1/f noise is strongly correlated to the density of traps in the gate dielectric and at the Si-SiO_2 interface. In fact 1/f noise has been proposed as a diagnostic tool for reliability [Vandamme, 1994]. The density of interface states increases considerably during the lifetime of a device. This is attributed to the creation of dangling bonds at the Si-SiO_2 interface as a result of the removal of the

passivation (typically H_2) due to repeated collisions with hot-carriers. DAHC (Drain Avalanche Hot Carrier) is a severe reliability concern which leads to threshold voltage / saturation current shifts and can cause circuit failure after a period of operation. It has been shown that low-frequency noise of MOSFETs increases considerably after hot-carrier stress [Brederlow, 2002; Erturk, 2004]. The increase in the density of interface traps can be described by [Hu, 1985]:

$$\Delta N_{it} = A(kt)^m \tag{4.1.}$$

where t is stress time, k is a device constant (representing stress current, transistor width, saturation voltage, etc.), A is a process dependent coefficient, and m is the power of the time dependence of the damage evolution. To a first order, (4.1) can be used along with any of the low-frequency noise models that incorporate trap density (i.e. eq. (2.8)) to predict the increase in low-frequency noise as a result of electrical stress.

Presently under investigation is the location of the hot-carrier induced traps in space and energy, and how this affects their contribution to low-frequency noise. Note that the models discussed above assume a uniform distribution of traps in space and energy. However, hot-carrier induced traps are more likely to be generated closer to the drain side of the transistor and this phenomenon has been illustrated in [Erturk, 2004] by comparing noise data in forward and reverse modes of saturation for the transistor. Here reverse

saturation is defined as the alternating of the drain and source terminals of the device-under-test between stress and noise measurement.

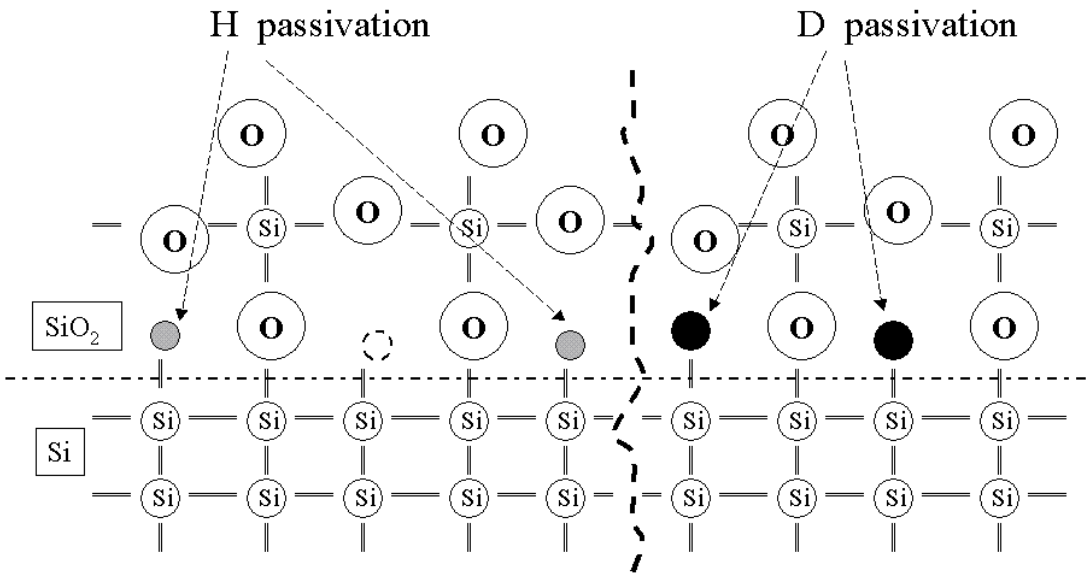


Figure 4.1: H2 or D2 passivated Si - SiO2 interface. A dangling bond due to the removal of a hydrogen atom also shown.

Another novel idea that has recently been investigated is the correlation between the type of species used to passivate the Si-SiO_2 interface and hot-carrier degradation of low-frequency noise. Typically, the dangling bonds found at the Si-SiO_2 interface are passivated with Hydrogen due to its pervasive abundance in the transistor fabrication process. Deuterium has been proposed by a number of research groups as an alternative to Hydrogen to improve transistor lifetime by increasing the immunity of the Si-SiO_2 interface to collisions with hot-carriers [Kizilyalli, 1997; Clark, 1999].

Since use of Deuterium at the interface retards the trap generation process, eq. (4.1) can be re-written with possible reductions in A or m. It has been experimentally shown that transistors subject to a Deuterium process have noise lifetime that is several orders of magnitude larger that transistors that are fabricated using a standard Hydrogen based process.

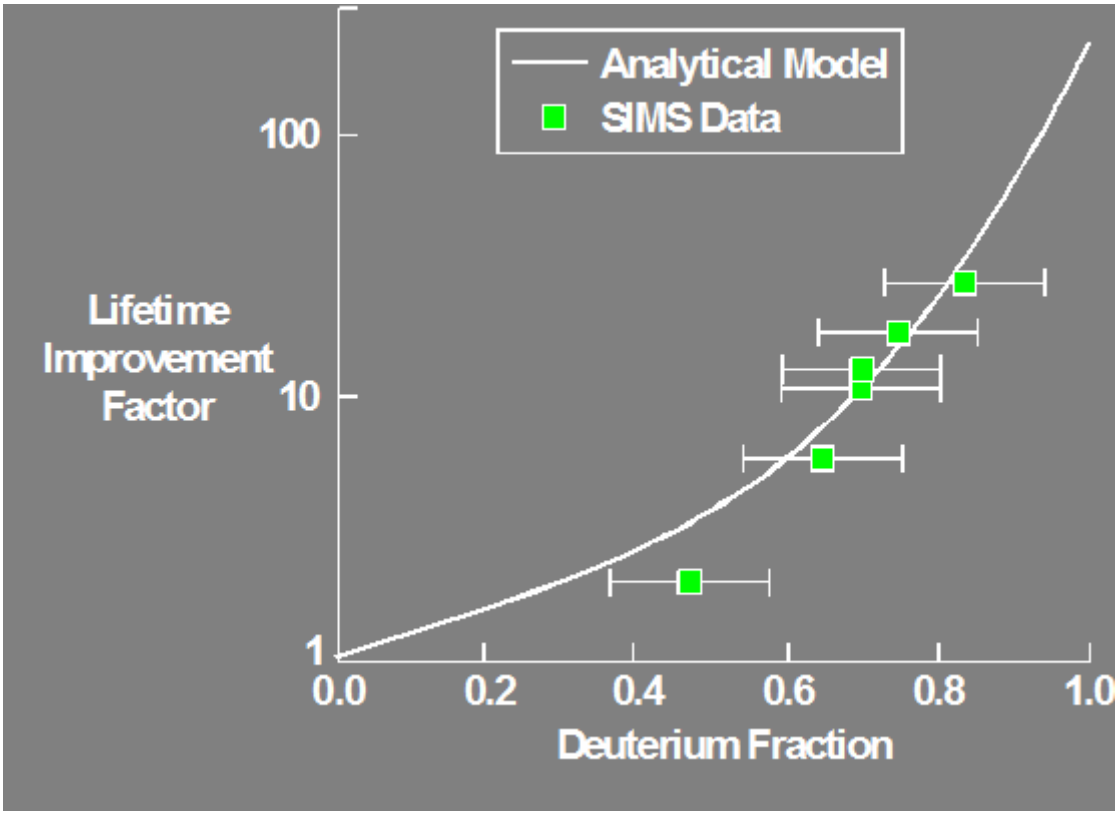


Figure 4.2: Lifetime improvement has been shown to be correlated to Deuterium fraction passivating the interface.

Stress conditions devised for digital circuit operation are not appropriate for analog / RF circuit reliability. For instance, hot-carrier stress can be performed with elevated drain

and gate voltages (channel-hot-carrier) which is appropriate for digital circuits. Hot-carrier stress can also be performed with elevated drain voltage and the gate voltage set at a level that leads to peak substrate current (drain avalanche hot-carrier) which is more appropriate for analog / RF circuits. The reliability of RF integrated circuits has recently gained attention of researchers [Xiao, 2004].

One of the earlier studies on 1/f noise and hot-carrier damage is by Tsai et. al [Tsai, 1993]. In this study the 1/f noise in the drain current of hot-carrier damaged MOSFETs biased in weak inversion is studied. Tsai et. al have treated the interface traps N_{it}, and oxide traps N_{ot} separately. By the use of biased annealing treatment, the density of oxide traps were decreased while at the same time the density of interface traps were increased. This study has shown that while the very-low-frequency portion of the measured 1/f noise is correlated with N_{ot}, the high-frequency portion of the 1/f noise is correlated with N_{it}. This finding is in agreement with the McWorther number fluctuation theory which attributes the time constant and hence the spectrum of each trap to its spatial location, with traps closer to the interface having shorter time constants and hence higher frequencies in their noise power-spectral density.

Celik-Butler et. al have shown in [Celik-Butler, 1988] that the Si-SiO_2 interface trap density can be determined by 1/f noise measurements. In their study, flicker noise measurements were performed at cryogenic temperatures of 20 to 280K. The Fermi level was calculated at each temperature, and, using McWorther's model, the density of

interface traps was calculated at energy levels corresponding to the position of the Fermi level at that temperature. The use of 1/f noise measurements was proposed as an alternate method to measure the oxide trap and slow interface-state densities with energies close to the band edges.

An interesting study on MOSFET interface traps is by Silva et. al [Silva, 1989]. In that study, the authors report a transformation process with which hot-electron-induced traps change their energy over time. It is shown that after hot-electron injection the overall density of interface traps increase with time, followed by a long period of trap transformation during which a portion of the interface traps with energies above midgap gradually converts in new interface traps below midgap. The authors do not propose a physical model for the transformation process.

Use of Deuterium on the surface passivation of MOSFETs has been studied by many authors [Kizilyalli, 1997; Ference, 1999; Clark, 1999; Cheng, 2001 and others]. It is generally reported that Deuterium improves device lifetime by hardening the interface (making the Si-SiO_2 interface more immune to hot-carriers). The combined effect of deuterium anneals and deuterated barrier-nitride processing are discussed in [Ference, 1999]. Chen et. al [Chen, 2000] have elegantly shown that the deuterium effect can be used to probe the physical mechanism of the interface trap generation in MOSFETs due to hot-carrier stress. In their studies, the “hot carrier injection theory” is invalidated and it

is shown that channel hot electrons, not carriers injected into the gate oxide, are primarily responsible for interface trap generation.

Device lifetime improvements due to deuterium passivation at different steps of device manufacturing are addressed by Lee et. al in [Lee, 1999]. The authors report lifetime improvements due to deuterium, even after multiple metallization steps on devices with nitride sidewall spacers. As would be predicted by theory, comparison of electrical measurements and SIMS profiles show that the lifetime improvement correlates with the amount of deuterium present at the Si-SiO_2 interface.

Cheng et. al [Cheng, 2001] offer a mathematical model to quantify the effect of deuterium passivation on the rate of interface trap generation. According to their model the rate of interface trap generation R(t) ($R(t)=dN_{it}(t)/dt$), can be expressed by the sum of two components:

$$R(t) = R^H(t) + R^D(t) \tag{4.2.}$$

where $R^H(t)$ and $R^D(t)$ are desorption rates of hydrogen and deuterium, respectively. The authors then show that the difference between the rate of interface trap generation for a fully hydrogen-passivated transistor and a transistor that has been subject to deuterium processing can be given by:

$$R_O^H(t) - R(t) = C_D[R_O^H(t) - R_O^D(t)] \quad (4.3.)$$

where C_D is the deuterium passivation fraction and $R^D{}_O(t)$ and $R^H{}_O(t)$ are interface trap generation rates for fully hydrogen-passivated and fully deuterium passivated transistors, respectively.

The studies mentioned above have not investigated the relationship between Detuerium and 1/f noise reliability. The impact of deuterium annealing on 1/f was noise briefly addressed by Ohguro et. al in [Ohguro, 2003]. However a quite minor improvement in the noise level was reported when deuterium was used instead of hydrogen. We have run extensive experiments on 1/f noise of deuterated and hydrogenated transistors at various hot-carrier stress times and have shown a great deal of 1/f noise lifetime improvement when deuterium is used in passivating the interface. Our findings are in agreement of the aforementioned studies where a strong correlation between 1/f noise and interface trap density was shown [Celik-Butler, 1988] and that interface-trap generation process can be retarded by use of deuterium [Kizilyalli, 1997]. Our findings are the first published results on the hot-carrier degradation of the 1/f noise of detuerated 90nm nFETs, [Erturk, 2004].

The next task is to develop an analytical model to project transistor noise lifetime improvement when deuterium instead of hydrogen is used in the passivation of interface traps. In this regard, Cheng et al [Cheng, 03] have developed the following analysis. For

a transistor in which some interface traps are passivated with deuterium (while others are passivated with hydrogen) the following expression holds:

$$\Delta N_{it}^{H}(t) - \Delta N_{it}^{M}(t) = C_D[\Delta N_{it}^{H}(t) - \Delta N_{it}^{D}(t)] \qquad (4.4.)$$

Equation (4.4) is a re-write of equation (4.3), with the parameters redefined for clarity. In equation (4.4), $\Delta N_{it}^{H}(t)$, $\Delta N_{it}^{D}(t)$, and $\Delta N_{it}^{M}(t)$ are interface trap generation at a given stress time, t, in the fully H-passivated, fully D-passivated, and mix-passivated transistors, respectively. Now (4.4) and (4.1) can be combined to write:

$$A_H t^m - A_M t^m = C_D(A_H t^m - A_D t^m) \qquad (4.5.)$$

or

$$A_M = A_H - C_D(A_H - A_D) \qquad (4.6.)$$

where A_H, A_D, and A_M are the prefactors (in eq. 4.1) for the fully H-passivated, fully D-passivated, and mix-passivated transistors, respectively. Cheng then shows that with an extraction of A_H and A_D from fully hydrogenated and fully deuterated transistors using the charge pumping technique to measure the density of interface traps generated, one can define the lifetime improvement as the ratio of stress time required to create the same number of interface traps in mix-passivated transistors to that of H-passivated transistors:

$$IMP = \left[\frac{1}{1 - C_D(1-\gamma)} \right]^{1/n} \tag{4.7.}$$

where the isotope factor $\gamma = A_D/A_H$

4.3 BSIM Modeling of Noise Reliability

The 1/f noise model implemented in recent versions of BSIM is based on the so called unified (or correlated) 1/f noise theory initially developed by Hung et. al [Hung, 1990] and Ghibaudo et al. [Ghibaudo, 1991]. In this model, the physical origin of the low-frequency noise is oxide and interface traps similar to McWorther's original number fluctuation theory [McWorther, 1957]. The BSIM model also states that trapped charge modulates local channel mobility causing correlated carrier number and mobility fluctuations within the transistor channel. In the Berkeley Short Channel IGFET Model (BSIM), the input referred noise spectral density is a linear function of the three noise parameters:

$$S_{vg} = f(Noia, Noib, Noic). \tag{4.8.}$$

According to the BSIM model, 1/f noise is proportional to trap density and the gate bias dependence of S_{vg} is captured by the relative ratios of *Noia*, *Noib*, and *Noic*, the three fitting parameters of the model. The most effective extraction metrology of the three

noise parameters is still a matter of debate [Heijningen, 1998], however it can be postulated that each parameter is directly proportional to trap density [Heijningen, 1998]. Therefore the time evolution of trap density due to hot-carrier effects can be directly applied to *Noia*, *Noib*, and *Noic*.

A. Trap Density Reliability Model

It is well known that DAHC (drain avalanche hot carrier) phenomena leads to an increase in trap density in MOSFETs. The hot-carrier induced trap density based on equation (4.1) is:

$$N_{t,HC} = \beta(\lambda t)^m \tag{4.9.}$$

where t is stress time, λ is constant representing stress current, transistor width, etc., β is a process parameter that determines the immunity of the Si – SiO_2 to hot-carriers, and m is the power of the time dependence of damage evolution [Hu, 1985].

In (4.9), stress conditions determine the hot-carrier induced trap density. To translate this to a device life time model, we have to make certain assumptions on the typical biasing conditions of the transistor. For many RF and Analog / Mixed Signal circuits, the transistors operate under strong drain bias (Vd ≈ 0.75·Vdd) and low gate overdrive (Vgs-

Vt ≈ 75mV). These conditions are in fact very susceptible to interface state creation due to the increased likelihood of drain avalanche.

The time evolution of the three BSIM noise parameters can thus be written as:

$$
\begin{aligned}
Noia(t) &= Noia_{t0}\,\frac{N_{t0}+N_{t,HC}}{N_{t0}},\\
Noib(t) &= Noic_{t0}\,\frac{N_{t0}+N_{t,HC}}{N_{t0}},\\
Noic(t) &= Noic_{t0}\,\frac{N_{t0}+N_{t,HC}}{N_{t0}}.
\end{aligned}
\qquad (4.10.)
$$

In (4.10), $Noia_{t0}$, $Noib_{t0}$, $Noic_{t0}$, are the time-zero values of the noise parameters, and N_{t0} is the time-zero trap density.

The time evolution of the average trap density created by hot carrier stress can be estimated by equation (4.9). Traps at the drain edge, above the pinch-off region, have little contribution to low-frequency noise since the current in this region flows within the bulk silicon at a distance from the surface. However, close to the pinch-off point in the inverted segment of the channel, traps have a dominating influence on low-frequency noise. In this region, a small number of carriers flowing near the interface carry the transistor current due to the elevated carrier velocity. Therefore, trapping / detrapping induced carrier number and mobility fluctuations in this region lead to substantial low-

frequency noise in the total drain current of the transistor. It was demonstrated in [Brederlow, 2002] that the hot-carrier degradation of the low-frequency noise can be approximated by:

$$\Delta S_{V_g}(t) \approx S_0 \cdot N_{t,HC}(t) \cdot \frac{a_0}{y_0} \cdot \left(\frac{4}{6}\Delta^3 + \frac{3}{2}\Delta^2 \cdot d \cdot t^n \right) \tag{4.11.}$$

where S_0 is a constant that contains the frequency behavior and other attributes of the noise, a_0 is a constant determining the average slope of the decreasing noise efficiency in the channel length axis, and Δ is the distance between the pinch-off point and the channel position of diminishing noise effectiveness before stress. Note that the pinch off point also shifts after electrical stress. In (4.11), n is the power of the time dependence of this shift, d is a constant describing its amplitude, and y_0 is a normalization constant [Brederlow, 2002].

In this study, we show that deuterium processing retards noise degradation and hence improves the lifetime of RF ICs. (4.9) can be scaled and rewritten as:

$$N_{t,HC}^{D}(t) = \kappa \cdot a \cdot (kt)^{m^*} \tag{4.12.}$$

where κ and m* are fitting parameters related to the percentage of the Si atoms at the interface that are passivated with D_2. Note that H_2 is pervasively present in device

fabrication and therefore a fraction of the total interface will have H_2 passivation instead of D_2.

For the purpose of comparing the deuterium process to a standard hydrogen process, the low-frequency noise degradation can also be estimated by (4.13), where f (f^* for deuterium) is a function that represents the amount of noise contribution of generated traps for a given value of Vgs and Vds:

$$\Delta S_{V_g}^{D}(t) = S_0 \cdot N^{D}{}_{t,HC}(t) \cdot f^{*}(Vgs, Vds) \qquad (4.13.)$$

4.4 Experimental Results

The figure shows the pre-stress and post-stress noise measurements from the two wafers, as well as simulations using our BSIM noise reliability model. Pre-stress and post-stress interface trap densities have been measured using the charge pumping technique. The increase in trap density has been directly applied to the three noise parameters as specified in equation (4.10).

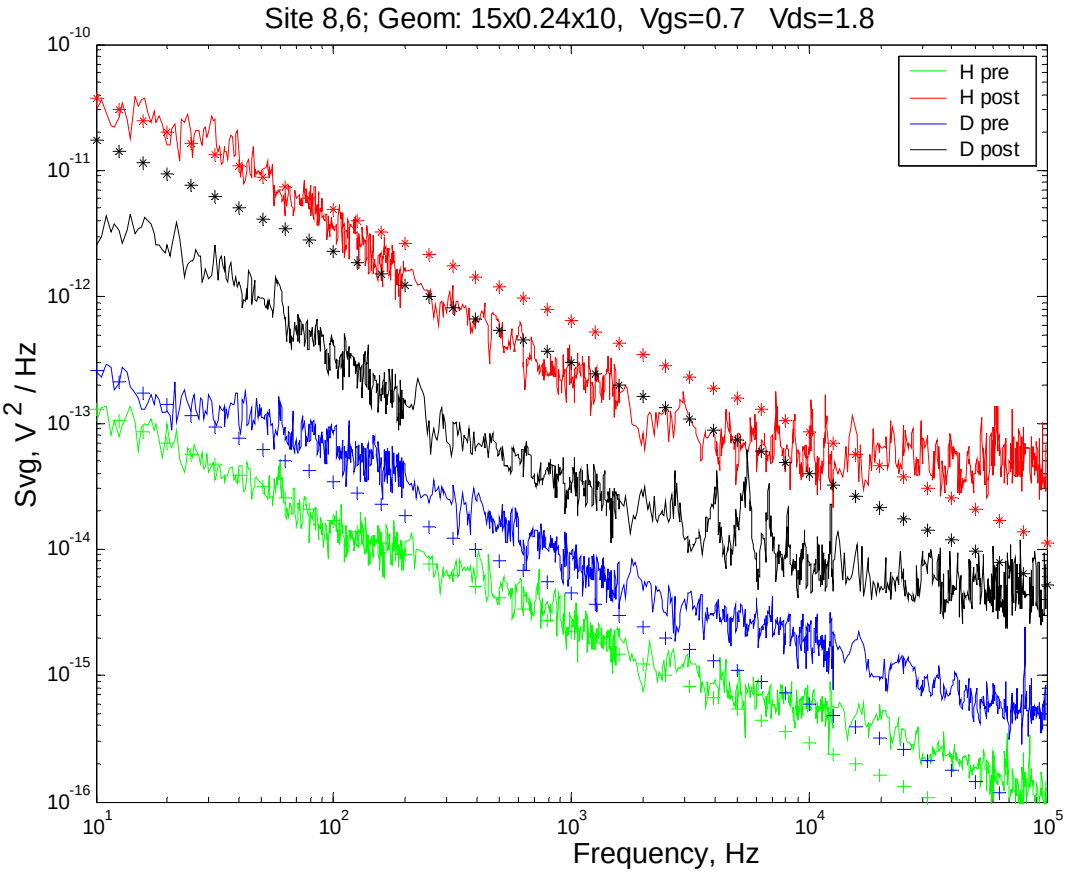


Figure 4.3: Pre-stress and post stress data from Hydrogen and Deuterium processed wafers.

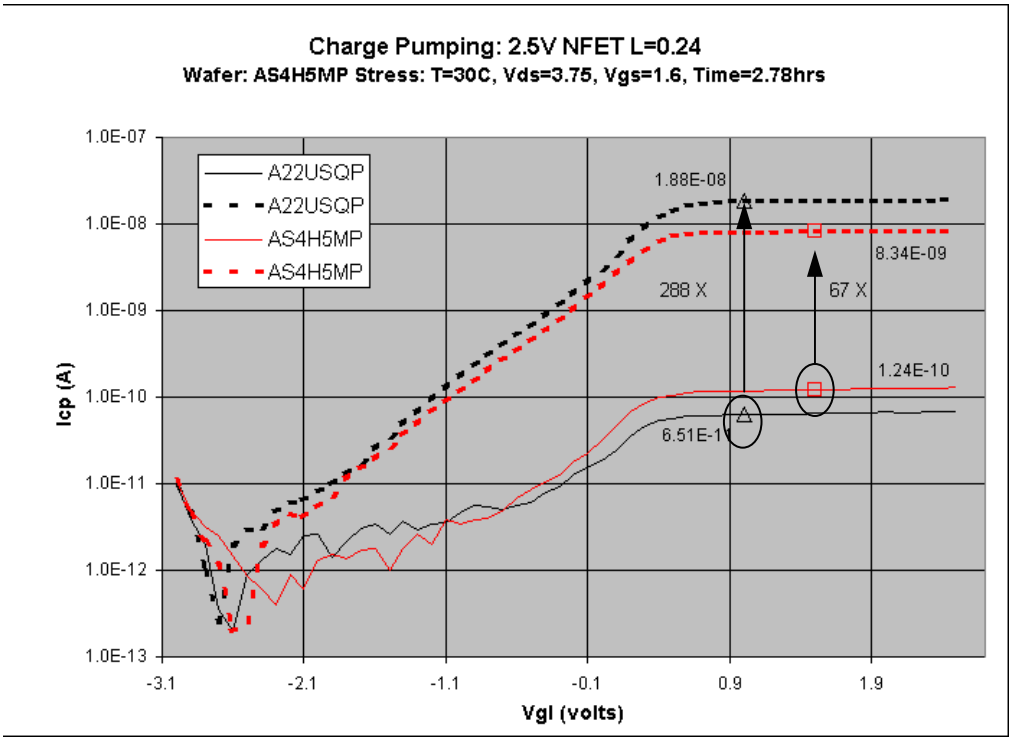


Figure 4.4: Charge-pump current shows relative degradation of (H) and (D) wafers.

Since trap density is directly proportional to the charge pumping current, it can be deduced that the standard wafer has shown a 288 times increase in trap density, whereas the deuterated wafer has shown a 67 times increase in trap density.

Excellent agreement for the hydrogen wafer is observed. However, the simulation results over predict the noise degradation in the deuterium wafer. Also it has been observed that at higher gate biases there is no difference between the post-stress noise measured from the standard wafer and the deuterated wafer. These results are attributed to the fact that

devices in this sample have been over stressed causing considerable degradation in device threshold voltage, transconductance, etc.

Transistors used in the study were fabricated using a 1.2V 90nm CMOS process. Wafers were subject either to deuterated film and anneal process or standard hydrogen based process. The details of the deuterium process are reported in [Clark, 1999]. DC characterization and hot-carrier stress were done using HP4156A precision semiconductor parametric analyzer. LFN measurements were taken using BTA9812B noise analyzer and HP35670A dynamic signal analyzer. Noise data were gathered under various gate and drain biases. DC and noise measurements were taken on the same devices before and after electrical stress. The stress was performed at high drain bias, 2.1V, and a gate bias that yielded measured maximum substrate current. The dimensions of the devices were 10μm/0.08μm and 10μm/0.24μm. The 0.08μm gate length devices were stressed for 600 seconds and the 0.24μm gate length devices were stressed for 2, 3, 6 and 11 hours.

Measurements show that after stress the input-referred noise power of the 0.08μm gate length transistors increased by more than 27dB for the standard processed wafer and only 1dB for the deuterated wafer (Fig. 4.5). For such short gate lengths, a small number of stress induced traps can alter the overall LFN. Therefore, the trap distribution is not

uniform in space or in energy, and the noise degradation varies strongly with gate and drain bias conditions (Figs. 4.6 and 4.7).

For the 0.24μm gate length nFETs, more than 13dB noise degradation has been measured in the standard process wafer for a three-hour stress. The wafer processed in deuterium showed no observable noise degradation (Fig. 4.8) for the same stress time. For this larger device, a uniform energy distribution for the stress induced traps can be assumed. However, the traps are selectively generated on the drain side of the channel as a result of the drain-avalanche hot carrier phenomenon. Consequently, the post-stress LFN is fairly gate bias independent and a small reduction in the overall degradation is observed at high drain bias (Figs. 4.9 and 4.10). The screening of some of the traps due to the pinch-off region leads to the observed drain bias dependence.

The fact that interface traps are selectively generated closer to the drain side of the transistor is further illustrated by taking noise measurements in reverse and forward modes of operation. The reverse mode is defined as the switching of the source-drain terminals of the transistor between stress and noise measurements. Figs. 4.11 and 4.12 show these results for the transistor biased in saturation and linear regions of operation, respectively. For the linear region there is no observable difference between the two modes. When the transistor is biased in saturation, reverse mode shows larger noise degradation. This illustrates that the pinch off region formed on the drain side screens

some of the interface traps generated, and that there is a larger concentration of traps generated on the side defined as the drain during stress.

As can be seen in Fig. 4.13 the degradation in LFN is correlated to the degradation in drain current. It is also observed (Fig. 4.14) that there is correlation between noise degradation and threshold voltage increase. Note that D_2 has a more direct impact on noise since it slows the interface trap generation process however it does not affect other hot-carrier phenomena, such as charge trapping into the gate dielectric, which may affect threshold voltage but not low-frequency noise.

Figures 4.15 and 4.16 show the measured noise degradation with respect to stress time for the 0.24μm channel length nFET. In these figures, the symbols represent measured data and the solid lines show the fitting of (4.10) to the data. For the two bias conditions $\kappa \cdot f^*/f$ and m^*/m are extracted from the figures and these results are summarized in Table I.

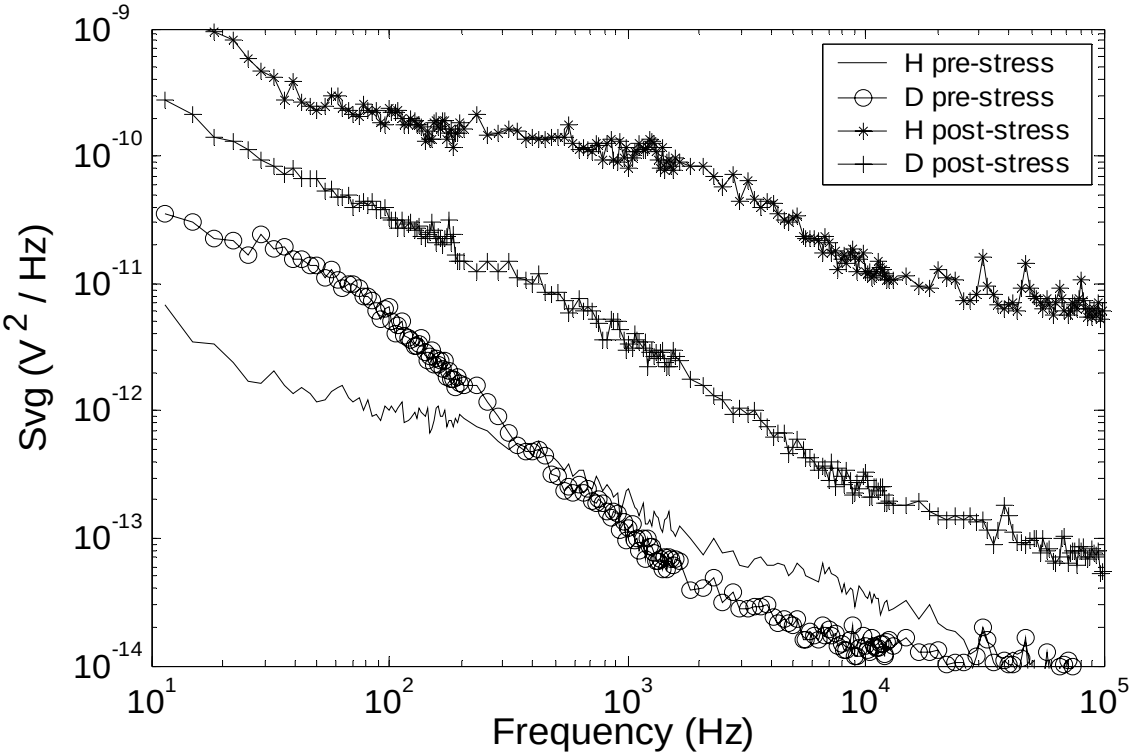


Figure 4.5: Pre- and post-stress input-referred noise. W / L = 10μm / 0.08μm. Vgs=0.5V, Vds=0.3V. 600s stress.

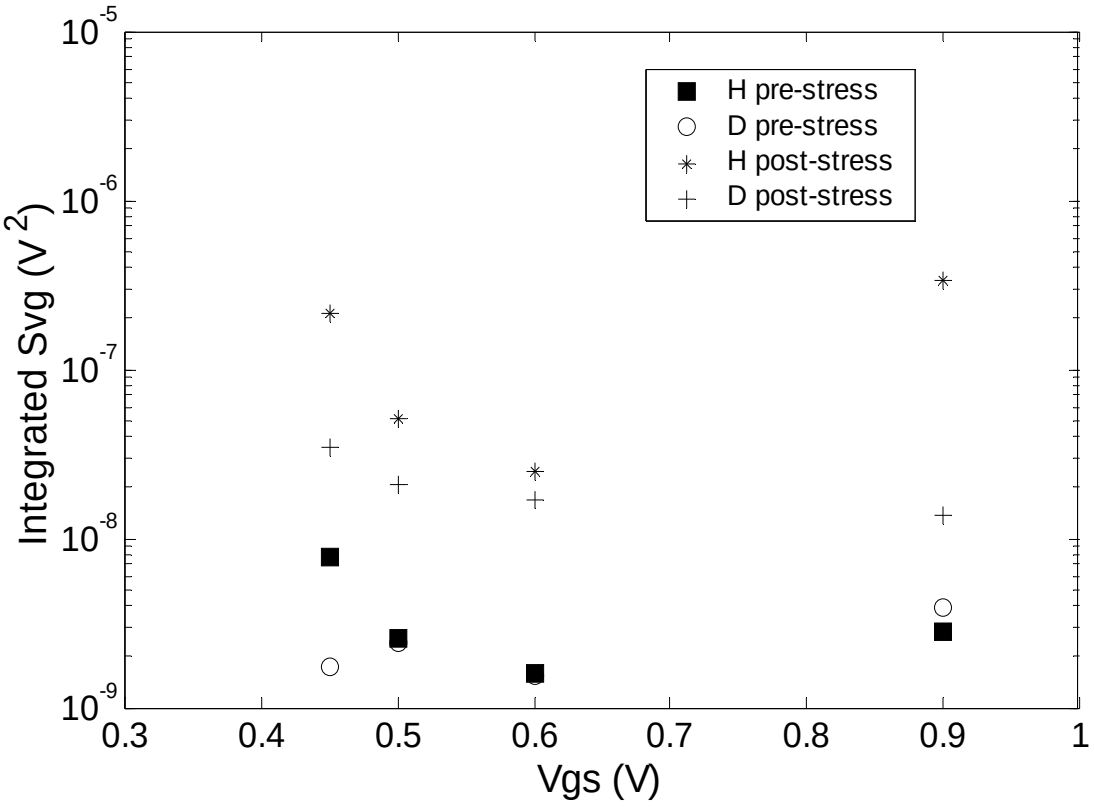


Figure 4.6: Integrated input-referred noise vs. gate bias. W / L = 10 μm / 0.08 μm. Vds=0.9 V. Increased variation with gate bias after stress.

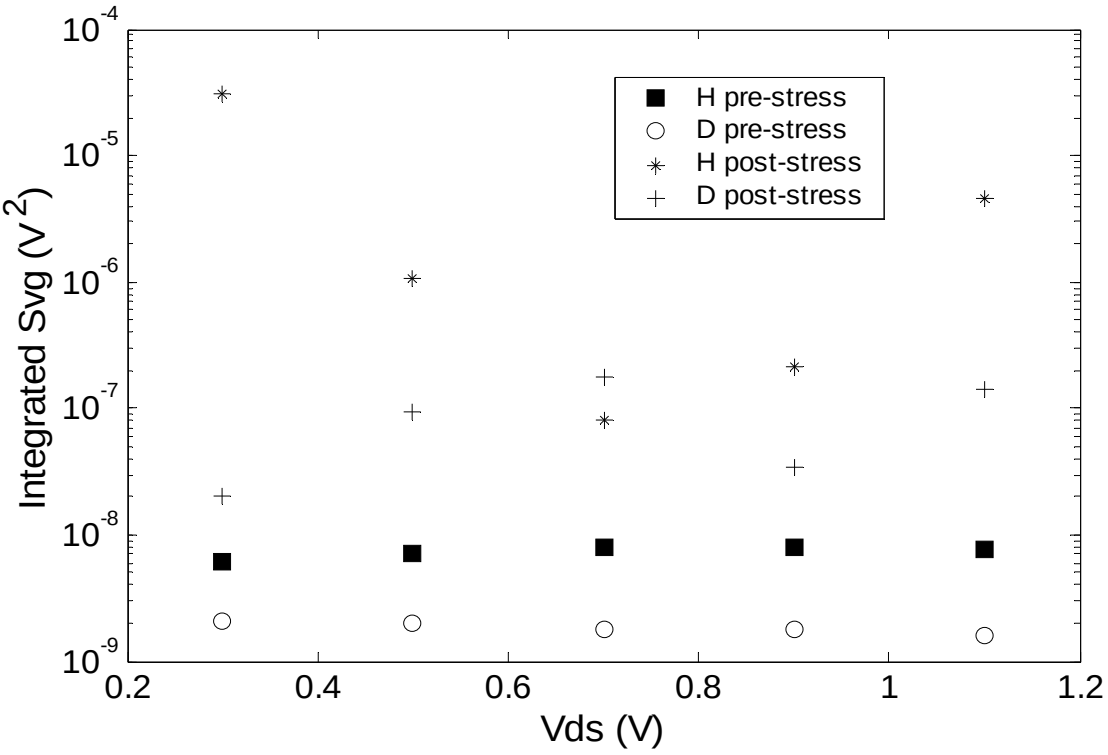


Figure 4.7: Integrated input-referred noise vs. drain bias. W / L = 10 μm / 0.08 μm. Vgs=0.45 V. Increased variation with drain bias after stress.

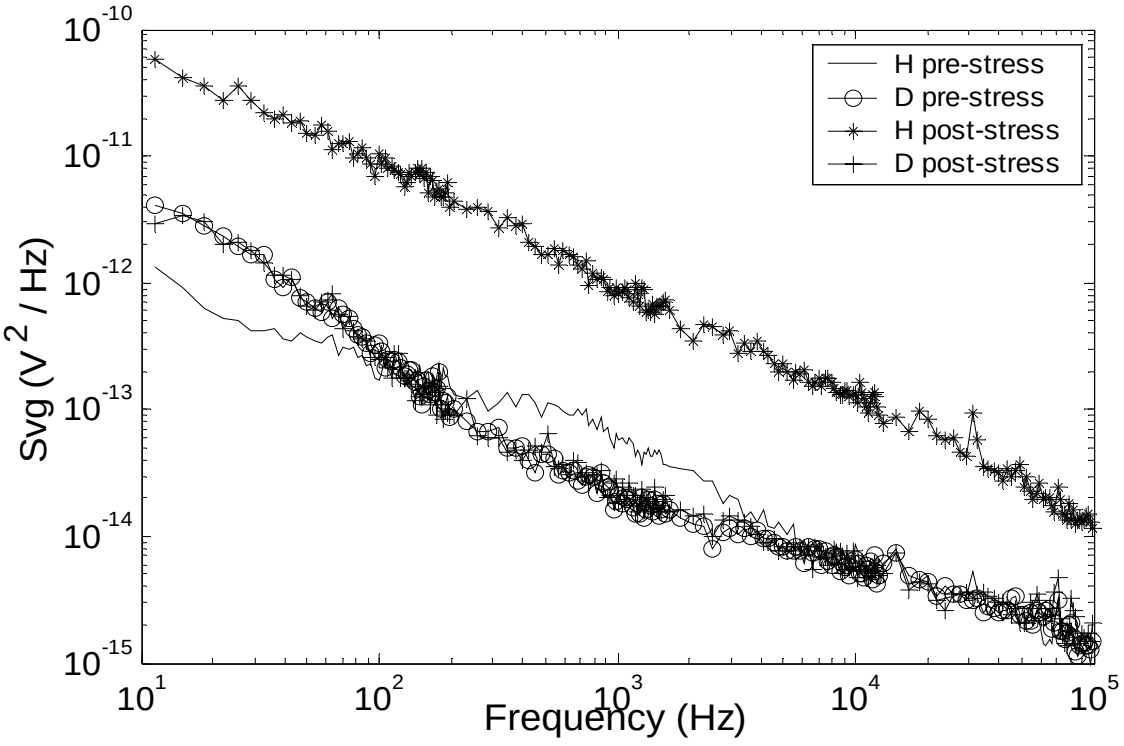


Figure 4.8: Pre- and post-stress input-referred noise. W / L = 10 μm / 0.24 μm. Vgs=0.5V, Vds=0.3V. 3hr stress.

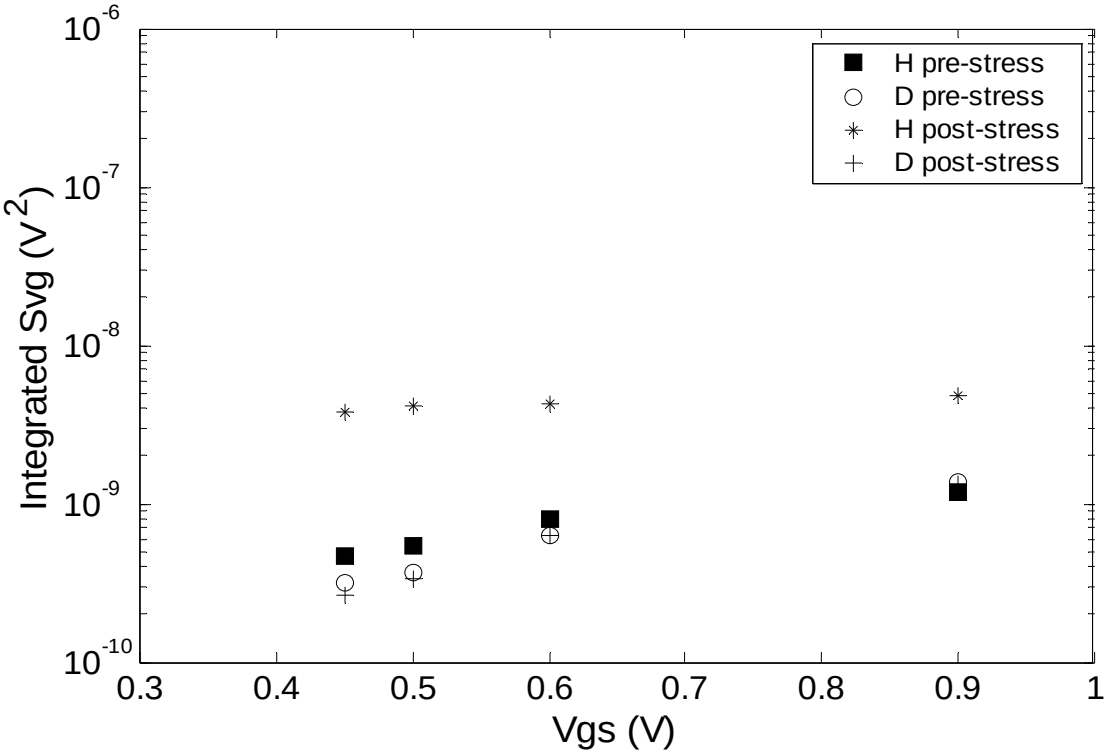


Figure 4.9: Integrated input-referred noise vs. gate bias. W / L = 10μm / 0.24μm. Vds=0.9V.

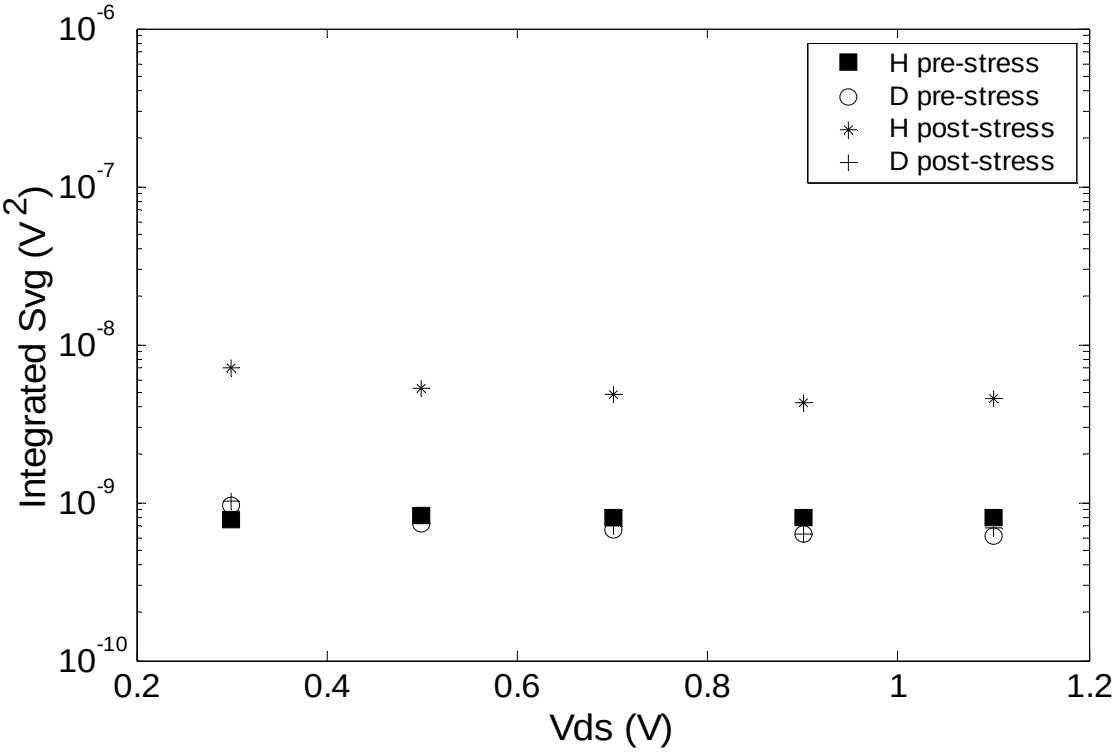


Figure 4.10: Integrated input-referred noise vs. drain bias. W / L = 10 μm / 0.24μm. Vgs=0.45V.

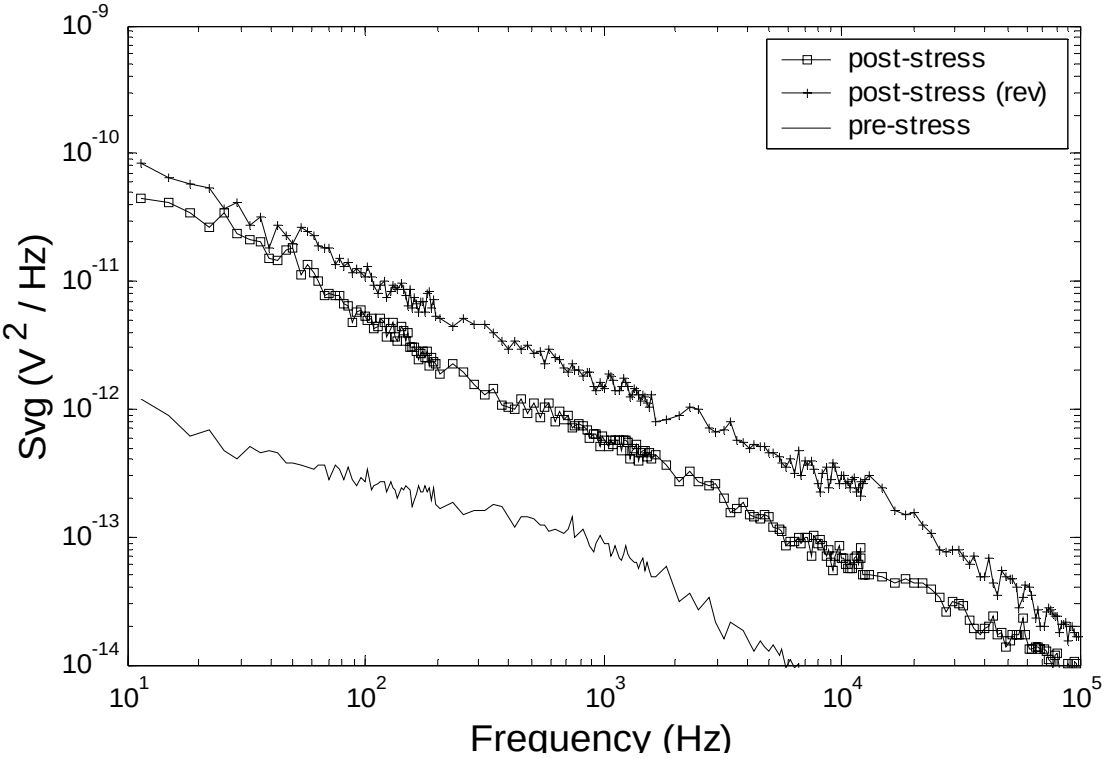


Figure 4.11: Forward and reverse mode noise measurements for standard (H2) device in saturation region. Vgs=0.6V, Vds=1.1V.

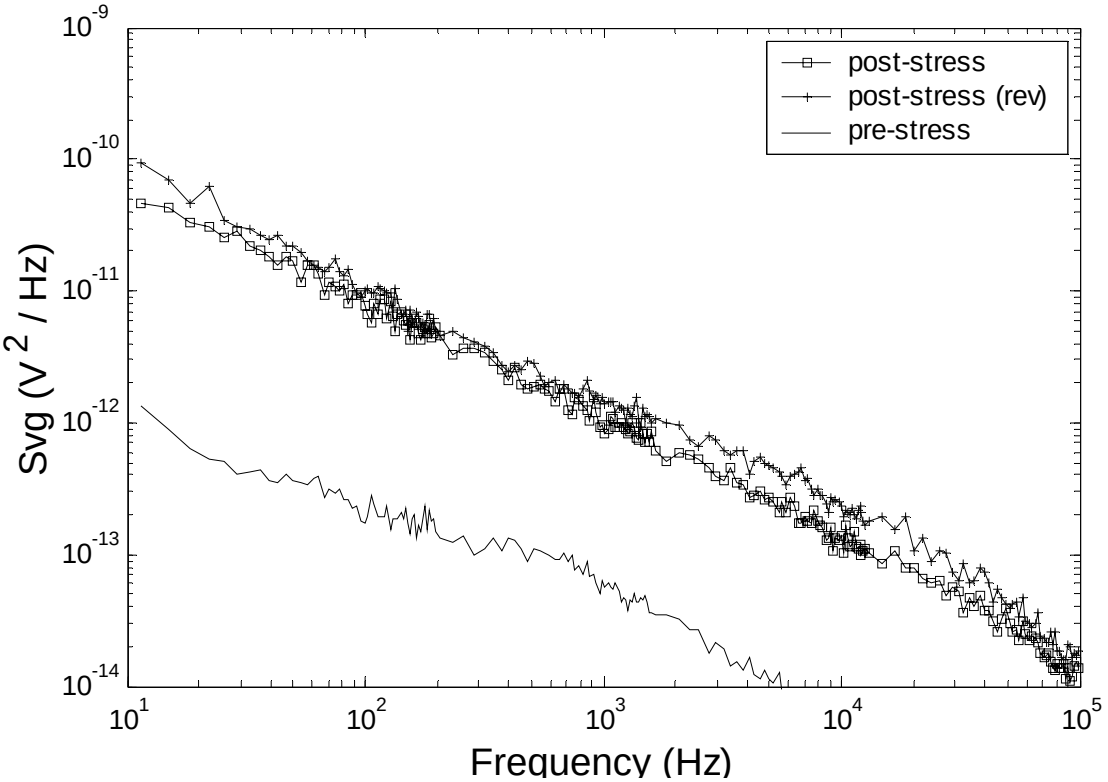


Figure 4.12: Forward and reverse mode noise measurements for standard (H2) device in linear region. Vgs=0.6V, Vds=0.1V.

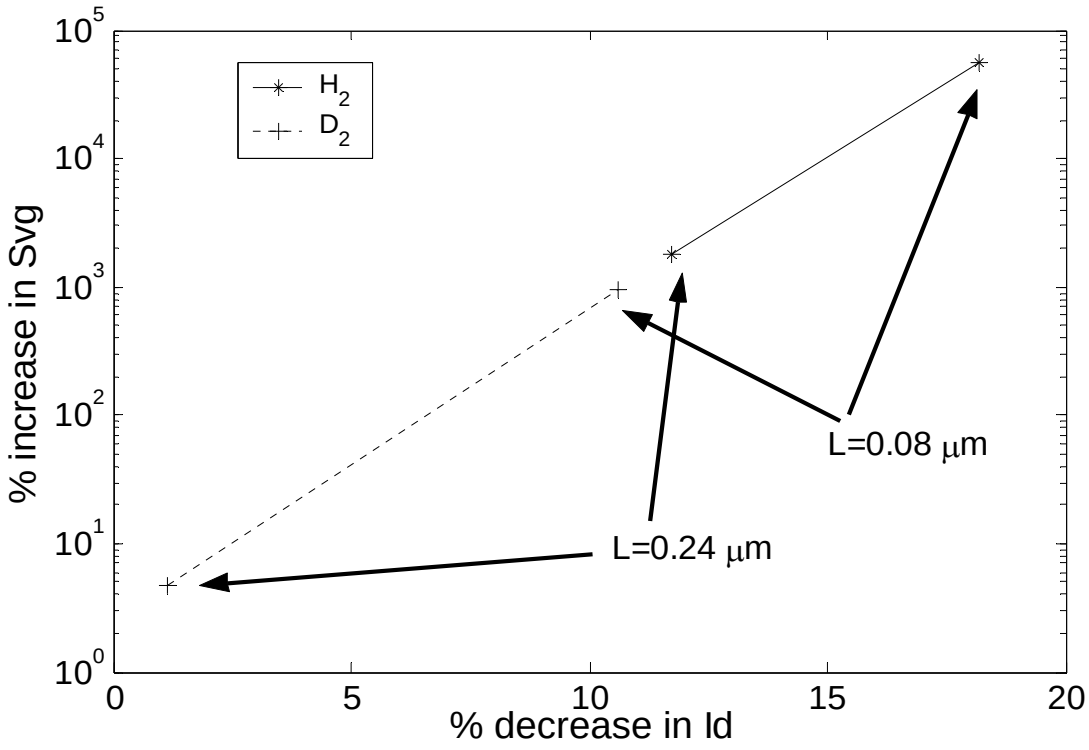


Figure 4.13: Noise degradation vs. current degradation for the 0.08 μm and 0.24 μm gate length nFETs from the standard (H2) and deuterated (D2) wafers. Measured at Vgs=0.5 V, Vds=0.3 V. 600s and 3hr stress for the 0.08μm and 0.24 μm, respectively.

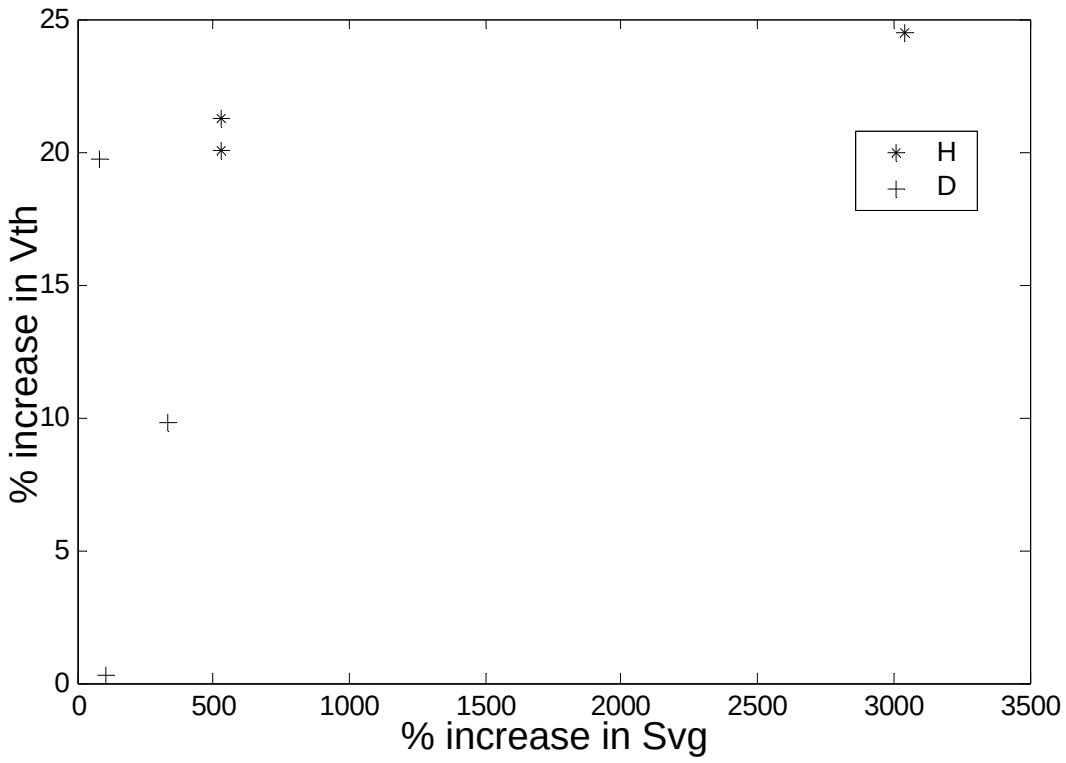


Figure 4.14: Measured threshold voltage increase versus noise increase for various stress times.

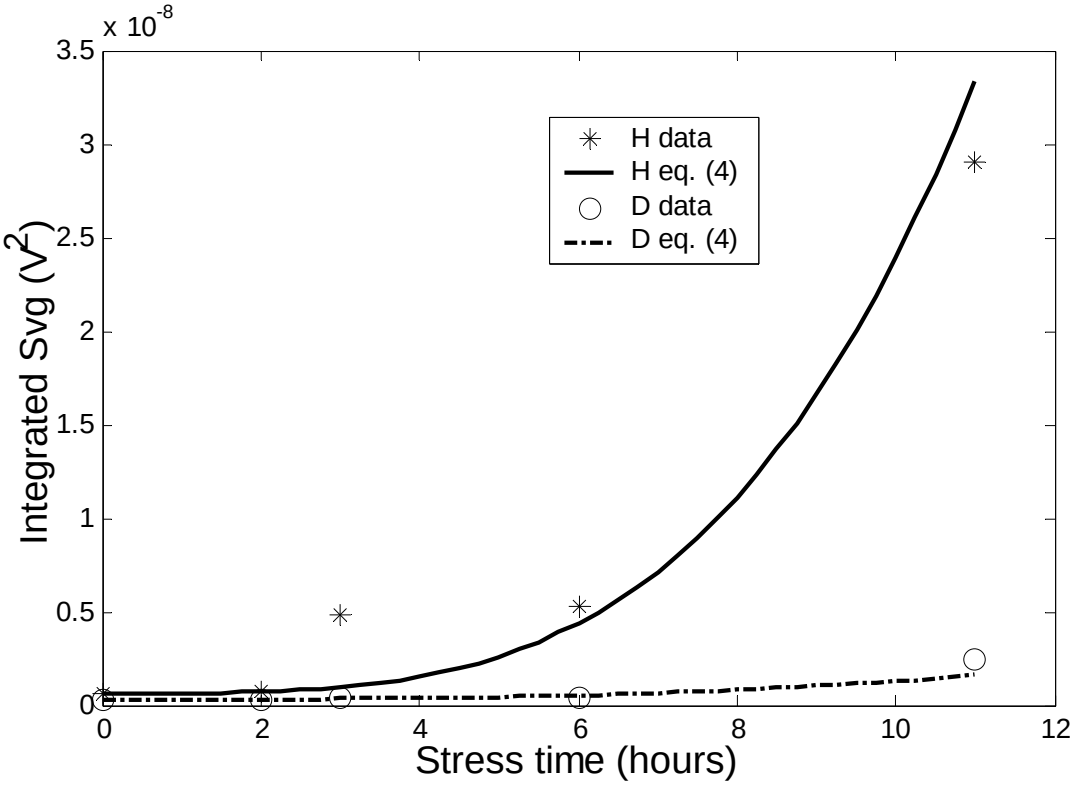


Figure 4.15: Noise degradation over time for Vgs=0.5 V, Vds=0.7 V.

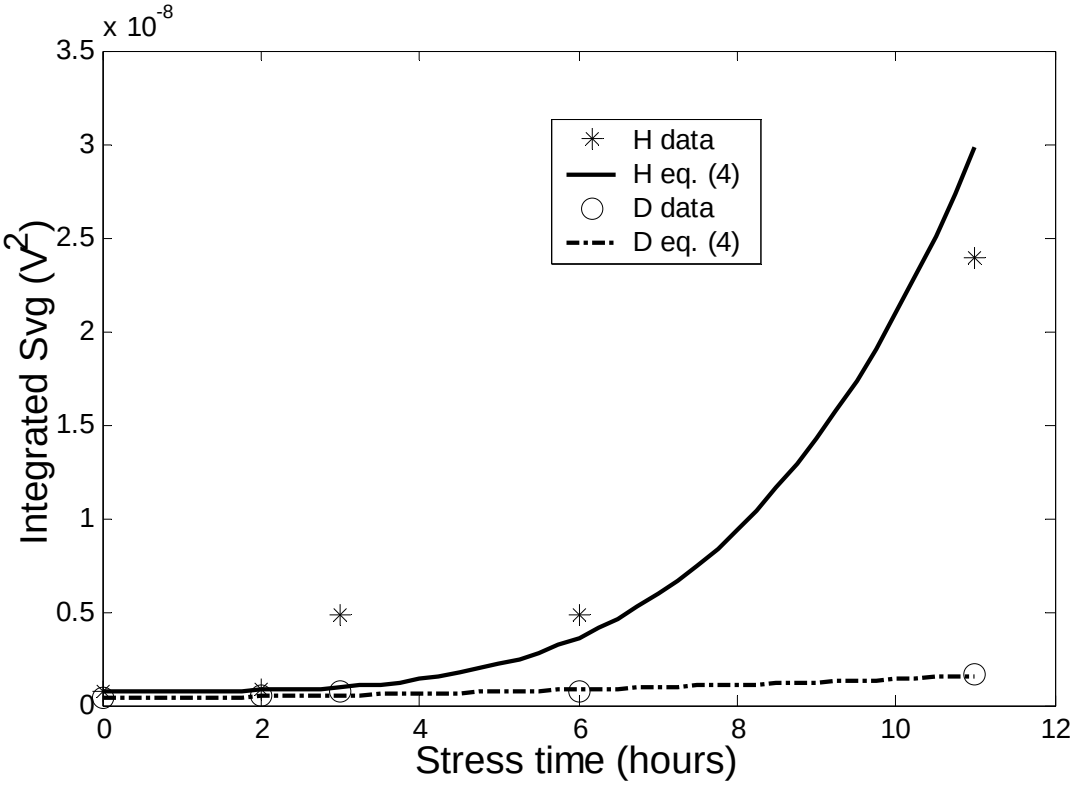


Figure 4.16: Noise degradation over time for Vgs=0.6 V, Vds=0.7 V.

	Bias 1	**Bias 2**
$\kappa \cdot f^*/f$	**0.1847**	**8.6808**
m^*/m	**0.8197**	**0.4150**

Table 2: Extracted reliability model parameters.

5. Modeling of Noise Statistics

5.1 Statistical Noise Variations

The number of traps found in a particular MOSFET device area follows a Poisson distribution. As such, for modern submicron MOSFETs, trap density can not be treated as a fixed process constant.

Technology:	Minimum area for Id=1mA @ Vgs=Vds=Vth+0.1V, L=Lmin	approx. # of traps:
250nm	**171 μm^2**	**8550**
180nm	**25.4 μm^2**	**1279**
130nm	**12.8 μm^2**	**640**
90nm	**2.2 μm^2**	**110**

Table 3: Number of traps likely to be found in a transistor in analog circuits, based on typical trap densities reported in literature.

Since the variance of a Poisson distribution is equal to its mean, we can define the uncertainty in the number of traps, and thus in trap density as:

$$\frac{\sigma(\#traps)}{<\#traps>} = \frac{\sqrt{N_t WL}}{N_t WL} = \frac{1}{\sqrt{N_t WL}} \tag{5.1.}$$

As the transistor dimensions area reduced, the uncertainty in the number of traps increases.

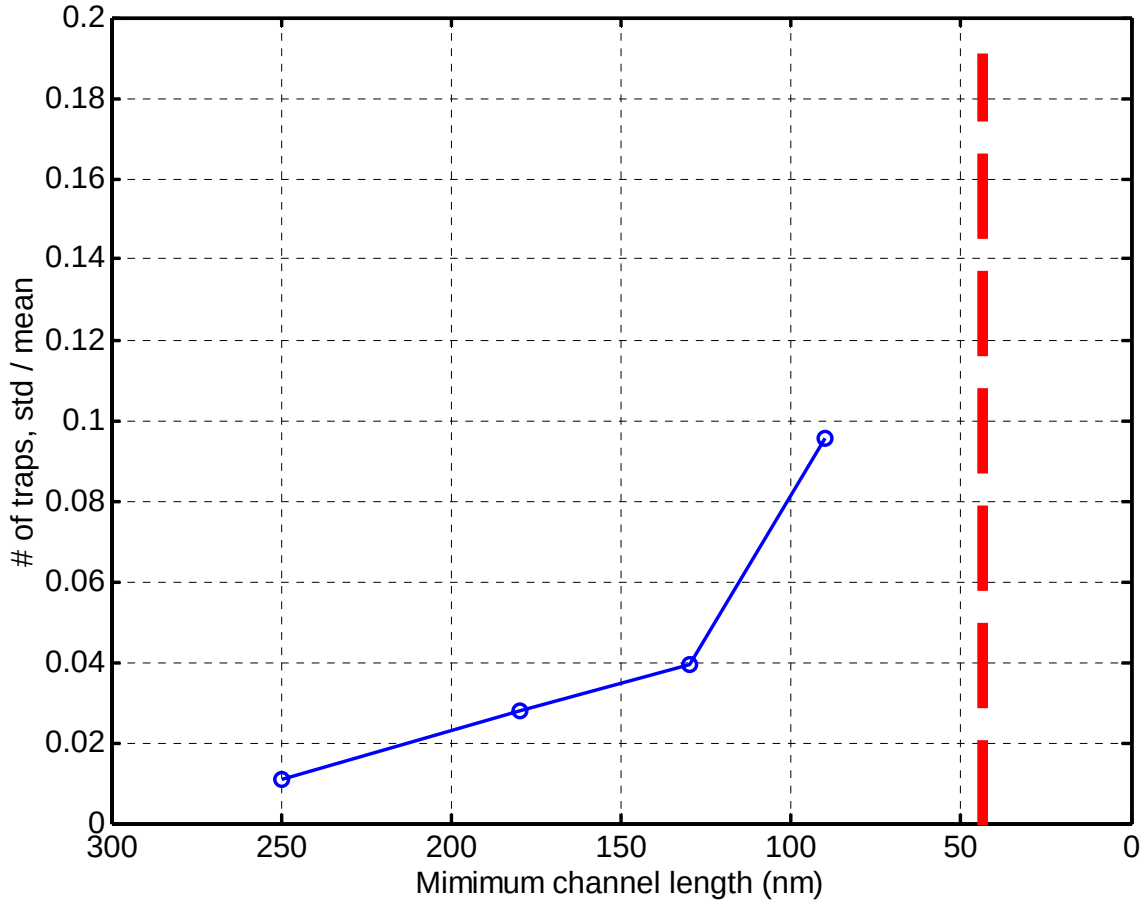


Figure 5.1: Trap uncertainty versus decreasing minimum channel length.

Carrier traps are the main source of MOSFET flicker noise. When modeling flicker noise, trap density must be treated as a random variable for which statistical properties (such as expected value and variance) must be verified experimentally. In fact, more than an order of magnitude of noise power variation can be observed in measurements on submicron FETs. This variation translates to 10dBc/Hz fluctuations in the close-in phase noise of an RF CMOS VCO. Given that many analog and RF circuits have such a sensitivity to flicker noise, it is essential to utilize a quantitative approach to design optimization that

accounts for noise statistics. In this paper, we present a methodology for modeling flicker noise statistics, and compare results from 130nm and 180nm MOSFETs. The noise variation increases as transistor area is reduced, and as gate overdrive is decreased. This area and bias dependence is implemented in the new model. We utilize an extensive database where all the relevant data are stored and easily accessed.

5.2 BSIM Implementation of a Statistical Noise Model

We gather noise data from 60 devices which are randomly chosen from 6 wafers. In addition to the sample size, it is also important to measure multi-finger and single-finger FETs of different geometries to capture the area dependence of the noise statistics. Measurements are taken at multiple bias points to identify the dependence of noise statistics on Vds and Vgs. A single measurement is defined to be the data for a single device type, size, and bias; such as low-Vt nfet, with W/L of 10μm/0.12μm, Vgs=0.6V, and Vds=1.0V. We generate a database which, for each measurement, contains a matrix of Svg vs. frequency, transconductance, drain current, wafer id, and site id. From the Svg vs. frequency matrix, we extract ϕ, such that ϕ_i / f^{ef} gives the best fit to the i^{th} measurement; ef is treated as a constant and typically has a value close to 1, f is frequency. The final database contains all the relevant information for analyzing various trends in noise statistics. Such analysis yields useful information on the area dependence of noise variance, the bias dependence of noise variance, correlation between noise variation and transconductance variation, wafer-to-wafer and site-to-site variability, etc.

Organization of the large volume of data in an easily accessible database allows for efficient data analysis and model development.

Before we can implement the statistical extension to the BSIM noise model, we must start with a nominal model that accurately captures the average noise level as a function of bias for each device type. The nominal model is based on measurements taken on process-centered wafers, with a large selection of bias points. The determination of the nominal values of the noise parameters is achieved by a combination of automated least-squares fitting and educated trial-and-error with the knowledge that the three parameters have different contributions based on gate voltage (through N_{inv}).

From the flicker noise database, we have observed that the distribution of ϕ is asymmetric for all measurements. The origin of the noise variation is the variability between the number of traps found in a particular device versus the expected value of the number of traps for that device area. For straight forward implementation in simulators, the Lognormal distribution can be used to skew the noise parameters with mean and variance extracted from the noise database.

A multiplier, k, is obtained from each measurement, such that:

$$\begin{aligned} \phi_{worst-case} &= k \cdot \phi_{\text{nominal}} \\ \phi_{best-case} &= \frac{1}{k} \cdot \phi_{\text{nominal}} \end{aligned} \tag{5.2.}$$

Note that the value of k is dependent on device type, device size, and bias conditions. To make the model scalable with area and bias, we must scale the multiplier accordingly. Since the underlying mechanism of noise variation follows Poisson statistics, the worst-case multiplier scales with the square root of area. Therefore in our implementation, k is extracted from a moderate device geometry (W=10μm, L=0.12μm, # of fingers=10). Its scaling with respect to device area is verified through comparisons with the rest of the geometries in the noise database. It is also observed that the value of k is reduced for higher gate voltages. This reduction in variability is discussed in detail in the next chapter.

In addition to a worst-case model, it is of primary interest for circuit designers to be able to run Monte Carlo simulations, or pick corner-values that are statistically more relevant than the 3-σ point. Therefore the scaling of the noise parameters is tied to a Gaussian distribution which is used as multiplier on the worst-case noise level with proper area scaling:

$$M = \ln(k) - \min(\ln\sqrt{\frac{w \cdot l}{A_0}}, 0) \tag{5.3.}$$

$$NOIA = NOIA_{\text{nominal}} * e^{D \cdot M} \tag{5.4.}$$

$$NOIB = NOIB_{\text{nominal}} * e^{D \cdot \frac{M}{J}} \tag{5.5.}$$

$$NOIC = NOIC_{\text{nominal}} * e^{D \cdot \frac{M}{J^2}} \tag{5.6.}$$

k is multiplier extracted from a moderate sized device at low overdrive voltage; A_0 is the area of the device from which k is extracted; w and l, are the width and length of the device being simulated. For $w*l > A_0$, M is pinned at ln(k); for $w*l < A_0$, M increases according to the square-root of area dependence. The noise multipliers are scaled by a Gaussian random variable, D, and a fitting parameter, J, which captures the bias dependence of noise variation. The exponent of the Gaussian product gives the Lognormal distribution, with which the nominal values of the noise parameters are scaled (eqs. 5.3-5.5). The value of D is fixed in Corner simulations, and follows a Gaussian distribution in Monte Carlo simulations.

With this methodology, we have introduced two new parameters required for the statistical model (k and J), in addition to the three parameters required for the nominal model ($NOIA_{nominal}$, $NOIB_{nominal}$, $NOIC_{nominal}$); k is a measure of noise variability, and J is a measure of the bias dependence of noise statistics.

5.3 Model Results and Hardware Correlation

We have studied the noise statistics of regular-Vt FET pairs (nfet & pfet) from the 180nm CMOS node, and regular-Vt, low-power, low-Vt, thick-oxide, and high-voltage thick-oxide FET pairs, as well as zero-Vt, and thick-oxide zero-Vt nFETs, from a 130nm node. Fig. 5.2 shows measured noise from 180nm and 130nm regular-Vt nFETs. Note that the variation in noise level is fairly close between the two technology nodes. Technology scaling has not had a negative impact on noise variation, other than that introduced by area reduction. Model to hardware correlation is provided in Figs. 5.3 and 5.4, also illustrating the gate bias dependence of noise variation, and its capture by the new statistical model. A Monte Carlo vs. Corner simulation is shown in Fig. 5.5. This capability allows designers to optimize simulation statistics against other process variations, and pick corner values of interest. Fig 5.6 shows Corner runs for different areas. The noise is normalized to illustrate the variation with respect to area. Fig. 5.7 shows nominal and 3-σ simulations for a sweep of gate voltages.

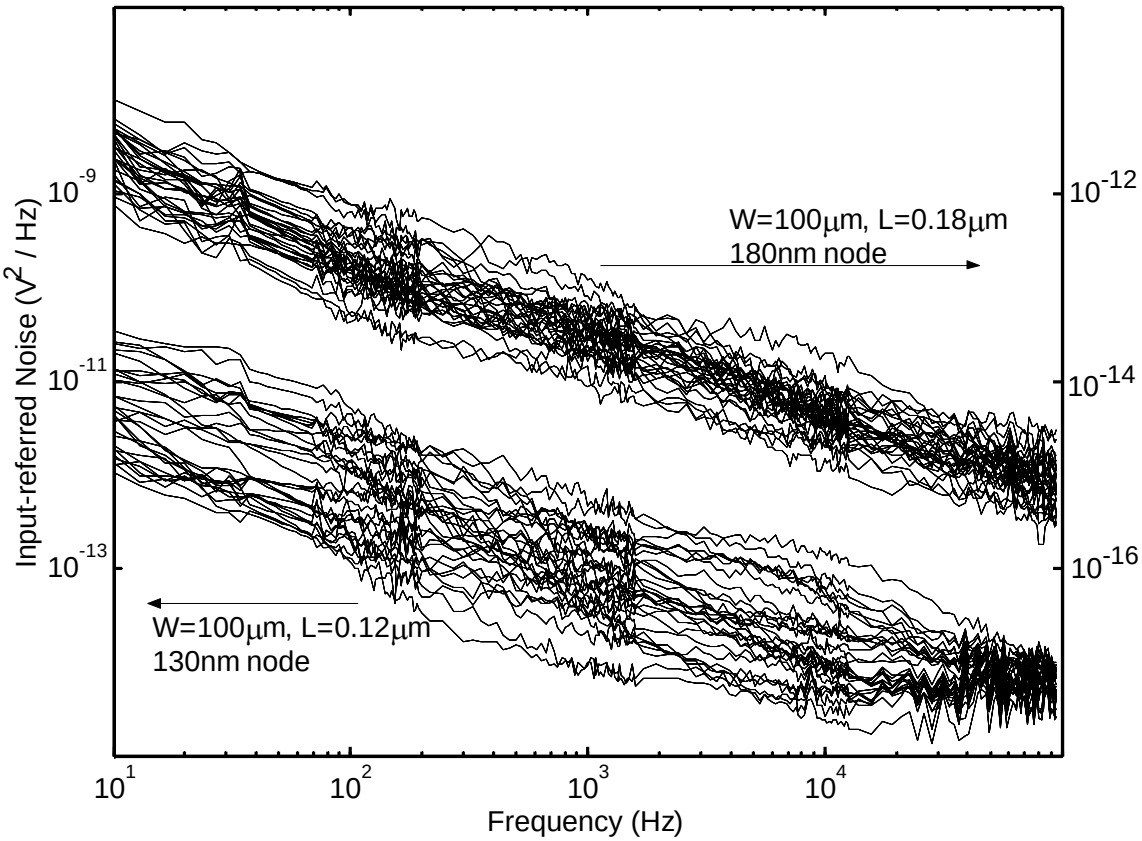


Figure 5.2: 130nm and 180nm FETs show similar noise variation. Spread decreases with increased area.

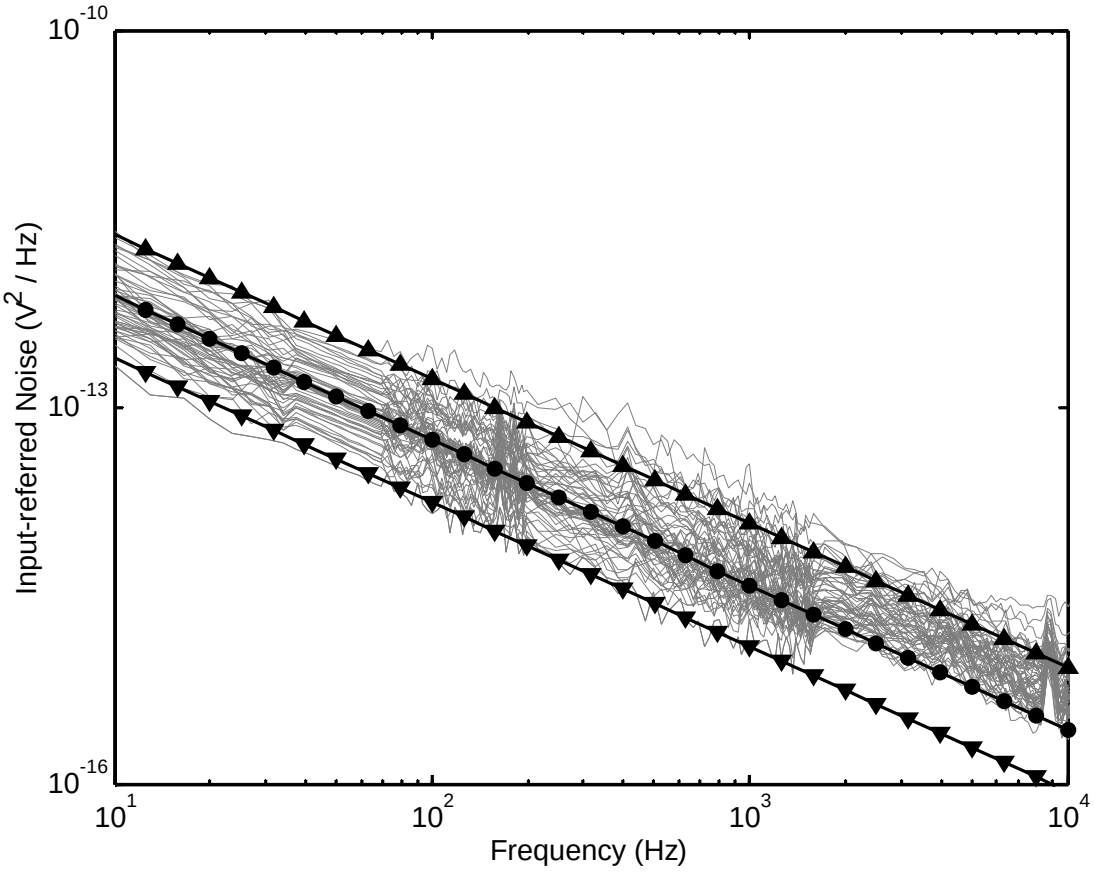


Figure 5.3: Nominal, worst-case, and best case; model vs. hardware, pFET W=100μm, L=0.12μm, Vds=1.0V, Vgs=0.41V.

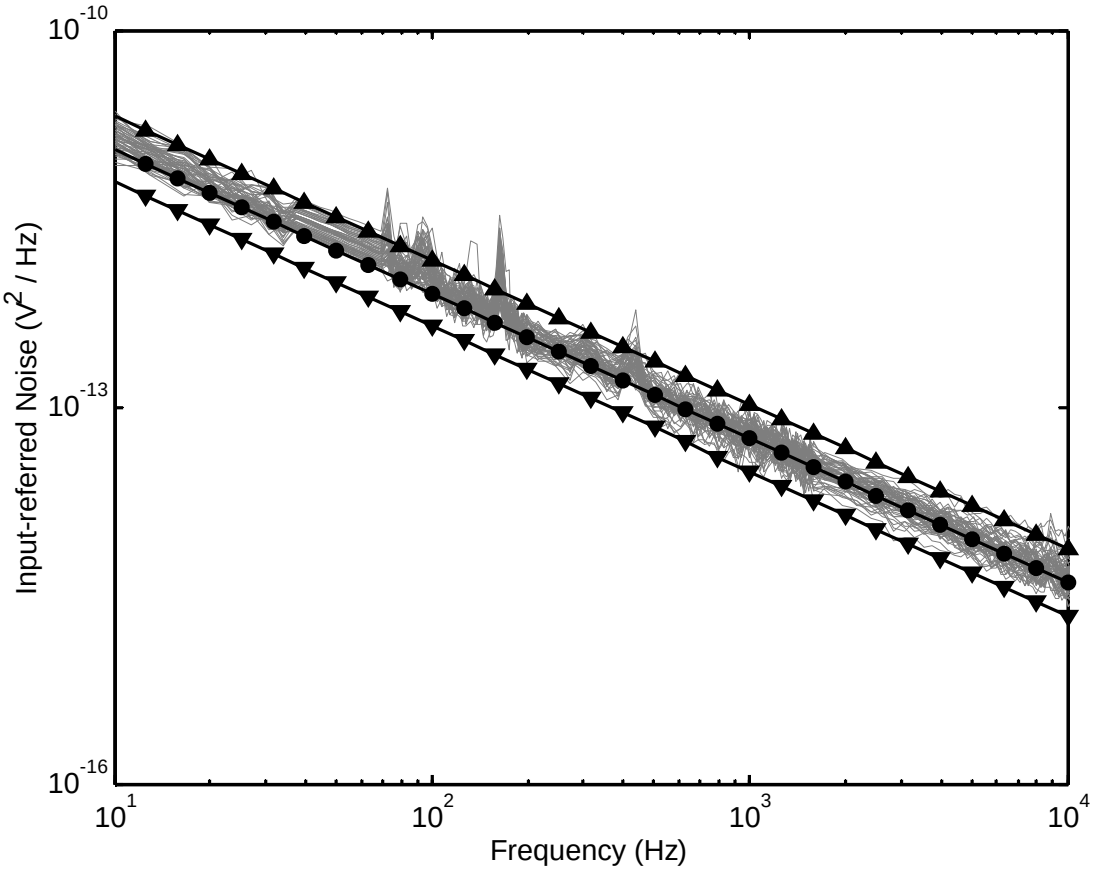


Figure 5.4: Nominal, worst-case, and best case; model vs. hardware, pFET W=100μm, L=0.12μm, Vds=1.0V, Vgs=1.17V. Note the reduction in spread at higher gate bias.

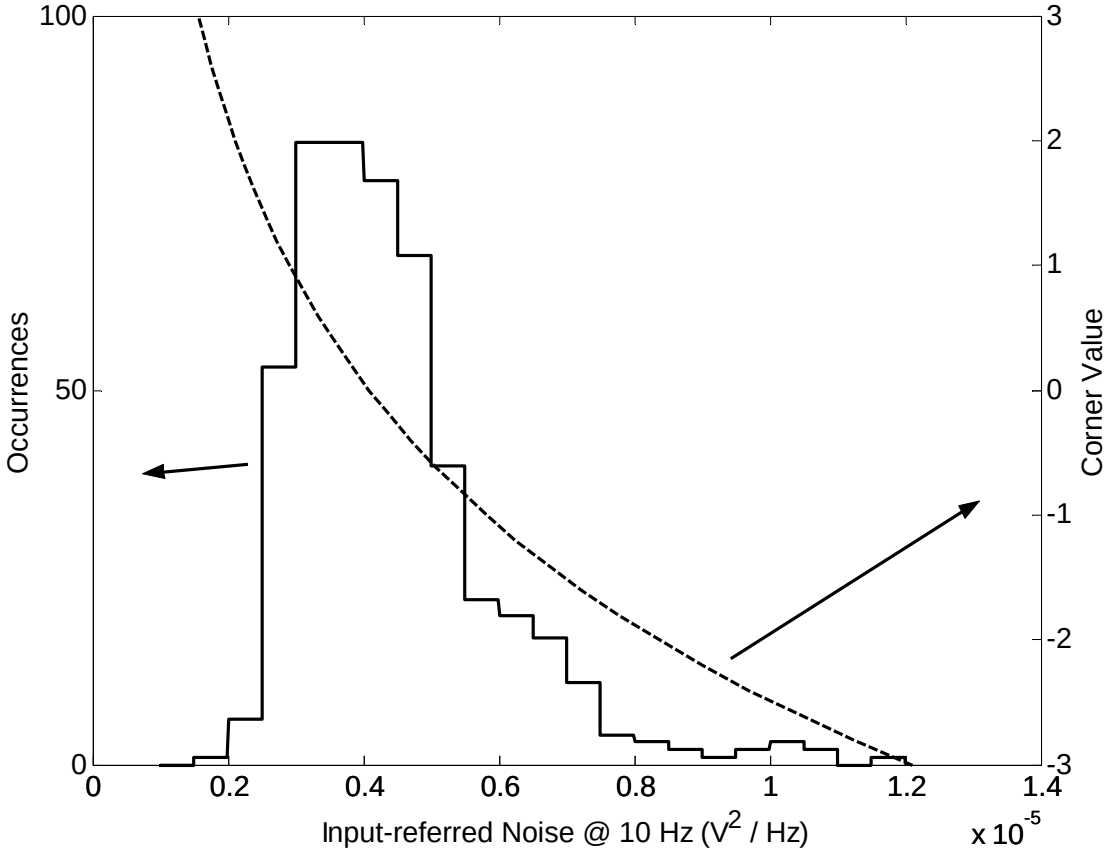


Figure 5.5: Monte Carlo and Corner runs, nFET, W=10μm, L=0.12μm, Vds=1.0V, Vgs=0.9V.

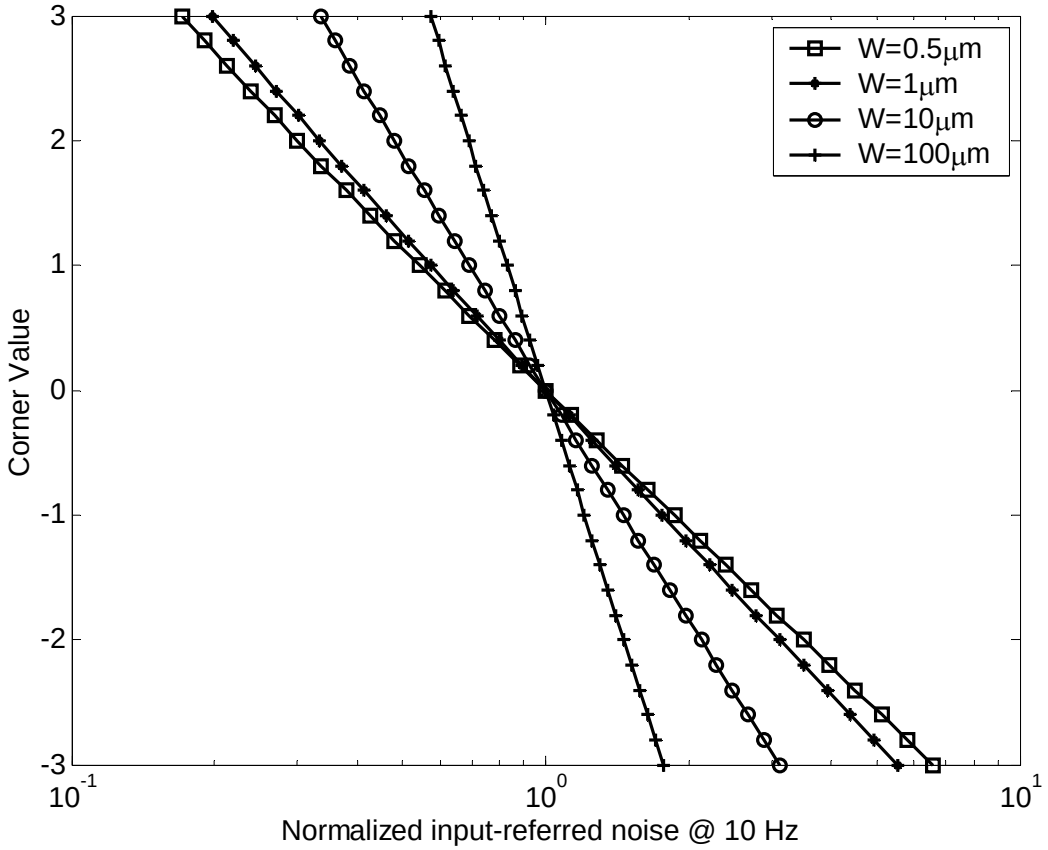


Figure 5.6: Corner runs for various gate widths, nFET, L=0.12μm, Vds=1.0V, Vgs=0.7V. Noise is normalized to show relative variation.

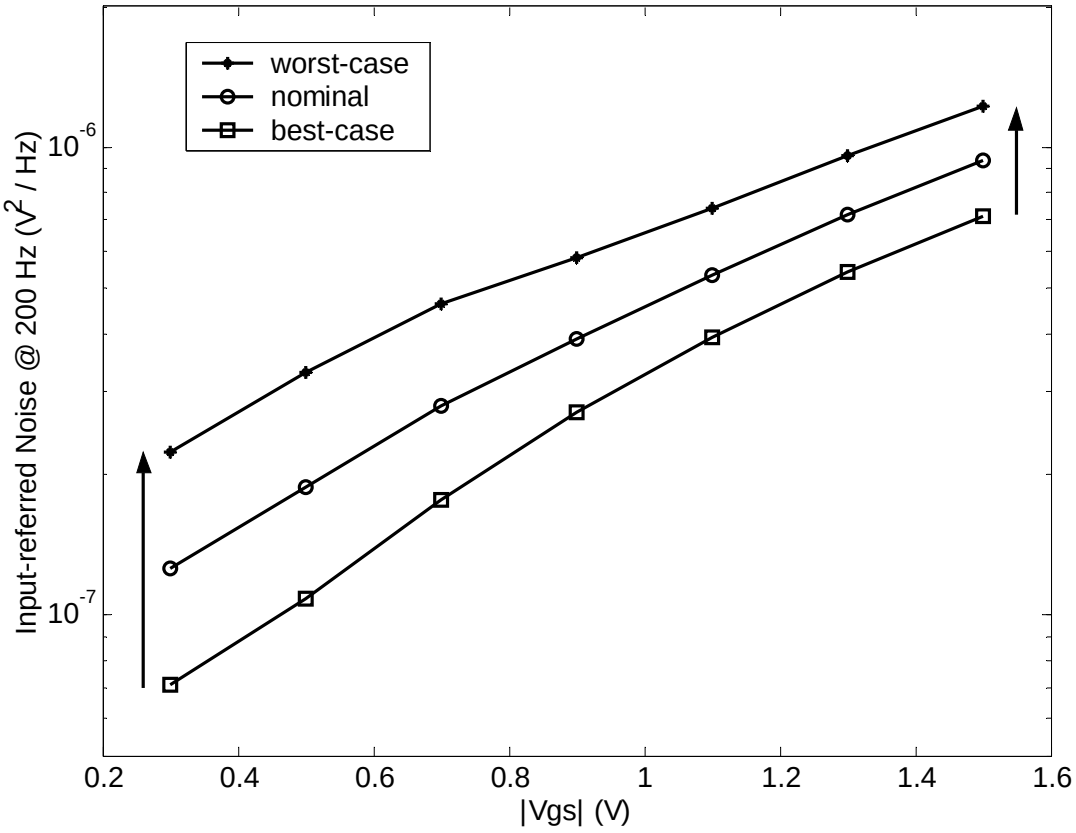


Figure 5.7: Relative noise variation is reduced as overdrive is increased. Simulations for pFET, W=100μm, L=0.12μm, Vds=1.0V.

6. Gate Voltage – Inversion Layer Profile Dependence

6.1 The Null Hypothesis – Correlation to Overdrive Voltage

As the gate voltage gets closer to the threshold voltage, all electrical characteristics of the device dependent of overdrive voltage will show increased statistical variability. The typical 15% variability in threshold voltage, translates to a halving of the overdrive voltage (Vod) when the gate voltage is only 30% higher than threshold. Therefore one explanation of the aforementioned gate bias dependence of noise statistics could be simple correlation to Vod which has a bias dependent relative uncertainty.

In a population of devices threshold voltage, drain current and transconductance show correlated distributions. In the following figure drain current (x-axis) and transconductance (y-axis) are shown for a population of 60 FETs.

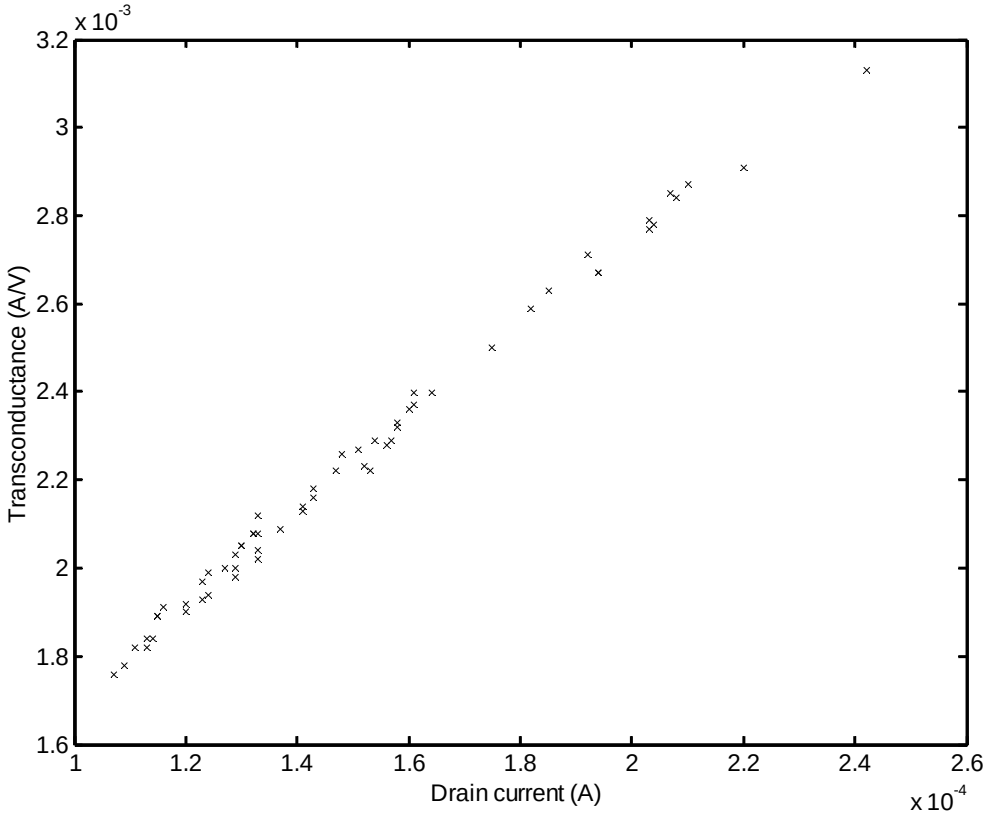


Figure 6.1: Transconductance versus drain current for a population of 60 FETs.

Using the r-value correlation test for the null hypothesis, a level significance (p) of 0.325 acceptable for a test of correlation for a sample of 60, the test shows a very strong correlation between drain current and transconductance (r-value=0.997). However, when applied to test the correlation between noise level and drain current or the correlation between noise level and transconductance, the test shows no correlation with r-values of 0.132 and 0.126 respectively. The lack of correlation can also be visually extracted from the following figure. Also note that while g_m and I_d variations are within +/- 30% of their

respective mean value, the noise variation spans more than an order of magnitude (1000%).

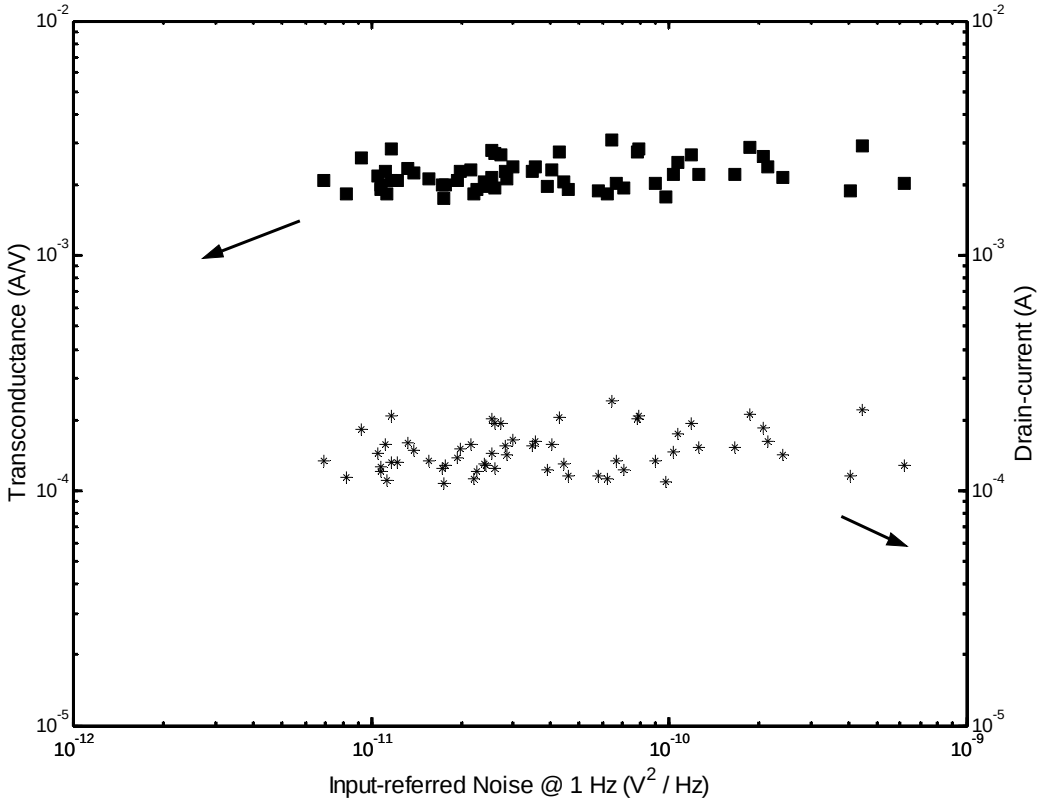


Figure 6.2: Variations in transconductance (left) and drain current (right) are not correlated to the variations in 1/f noise

Finally we can look at individual device behavior in terms of 1/f noise level at low Vgs, at high Vgs, and how it relates to the drain current of the same set of devices. The following figure is from three devices that exhibit the same noise level at high overdrive, but show considerably different noise levels at low overdrive even though the measured drain current is found to vary by only about 5%.

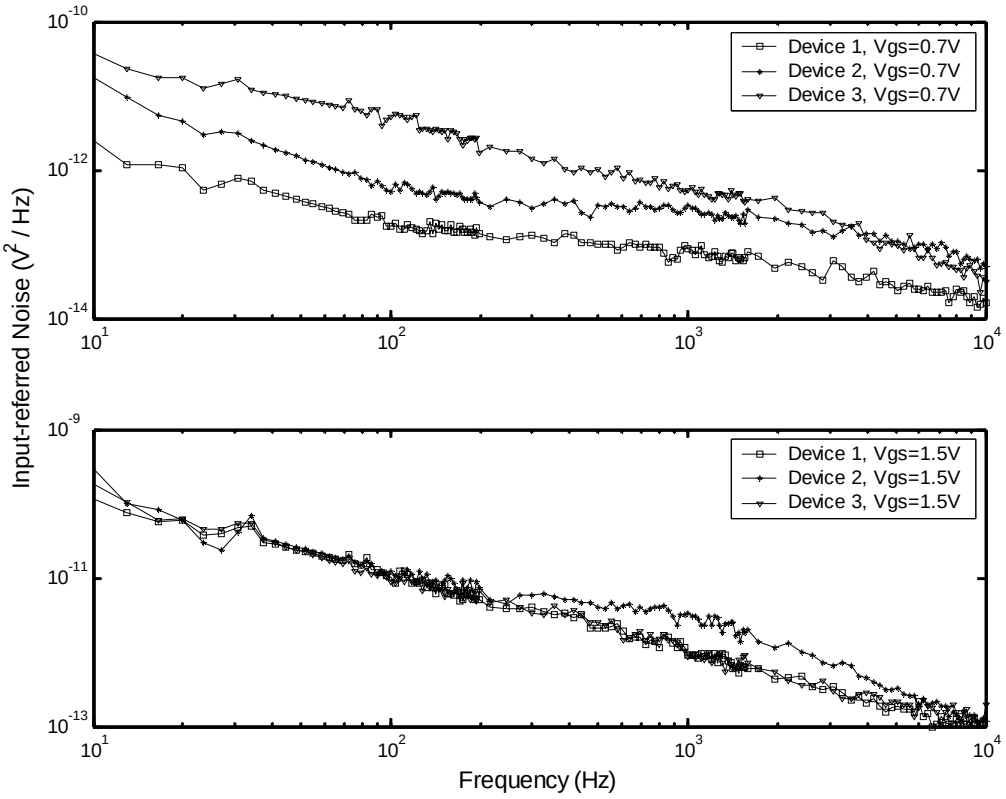


Figure 6.3: Three nFETs biased in the linear region, Vds=0.2V. (a) Large noise variations observed for Vgs=0.7V, (b) noise variations vanish for Vgs=1.5V. W=10μm, L=0.18μm.

The data and correlation tests indicate that the bias dependence of noise variability can not be due to correlation to Vod.

6.2 Trap Location and Mobility Fluctuations

The mobility fluctuation induced by a trapped charge is a function of the local inversion layer density within the proximity of the trap. High density inversion charge can screen

the Coulomb field originated at the trap, diminishing its impact on local mobility. The effective mobility can be calculated by Matthiesen's rule:

$$\mu_{eff} = \left(\frac{1}{\mu_B} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{Cit}} \right)^{-1} \tag{6.1.}$$

The mobility is limited by phonon scattering (μ_B), surface roughness scattering (μ_{sr}), ionized impurity scattering (μ_{ph}), and Coulomb scattering due to trapped charge (μ_{Cit}). Surface scattering and phonon scattering grow with increased gate voltage. As μ_B and μ_{sr} are reduced, the effective mobility becomes less sensitive to trapped charge. This bias dependence in the trap induced mobility fluctuation (α) must be captured in a model that accurately deals with noise statistics.

In [Vandamme, 2000] the data from [Koga, 1994] is shown to be best represented by an inverse square dependence on inversion layer density:

$$\alpha = \frac{1}{\mu_{co}\sqrt{N_{inv}}} \tag{6.2.}$$

We can generalize this expression, to apply to individual traps as follows:

$$\alpha_i = \frac{\kappa e^{-x_i / x_o}}{[(Ninv(y_i)]^{\beta}} \tag{6.3.}$$

$$\alpha = \frac{1}{n_t}\sum_{i=1}^{n_t}\alpha_i \tag{6.4.}$$

where α_i represents the contribution to mobility fluctuation of the i^{th} trap when it is charged; x_i is the trap height from the dielectric-semiconductor interface, x_o is the characteristic length associated with the exponential decay, y_i is the y coordinate of the trap along the channel from source to drain; and $N_{inv}(y)$ is the inversion layer density at location y_i. [Erturk, 2007] When $\kappa = 1/\mu_{c0}$, β=0.5, and ignoring trap location i.e. xi=0 and Ninv $\neq f(y)$ (or δNinv/δy = 0), the proposed general model reduces to the more specific case in (6.7).

6.3 Spatial Trap Statistics

Interface traps are distributed across the chip surface. Assuming there is equal probability for a trap to be found at any point along the channel length (y) and dielectric thickness (x), x_i and y_i are independent uniformly distributed random variables, with variances $\sigma_x^2 = T_{ox}^2/12$ and $\sigma_y^2 = L_{eff}^2/12$ respectively, with T_{ox} representing the gate dielectric thickness, and L_{eff} representing the effective channel length. We can then compute the uncertainty in α_i using the propagation of uncertainty method [Kline, 1953]:

$$\sigma_\alpha = \left[\left(\frac{\partial \alpha_i}{\partial x}\sigma x\right)^2 + \left(\frac{\partial \alpha_i}{\partial y}\sigma y\right)^2\right]^{1/2} \tag{6.5.}$$

substituting and simplifying we get:

$$\sigma_\alpha = \frac{\alpha_i}{\sqrt{12}}\left[T_{ox}{}^2 + \left(\frac{L_{eff}\beta}{N_{inv}(y)} \cdot \frac{\partial(N_{inv}(y))}{\partial y} \right)^2 \right]^{1/2} \qquad (6.6.)$$

To further simplify the above equation, we need to know $N_{inv}(y)$ with respect to bias. It is difficult to obtain an accurate, closed-form expression for $N_{inv}(y)$ for modern MOSFETs [Gummel, 2001]. Using TCAD simulations (T-SUPREM4, FIELDAY), we have studied the inversion layer and mobility profile of the devices for which the noise data is shown in the following figure:

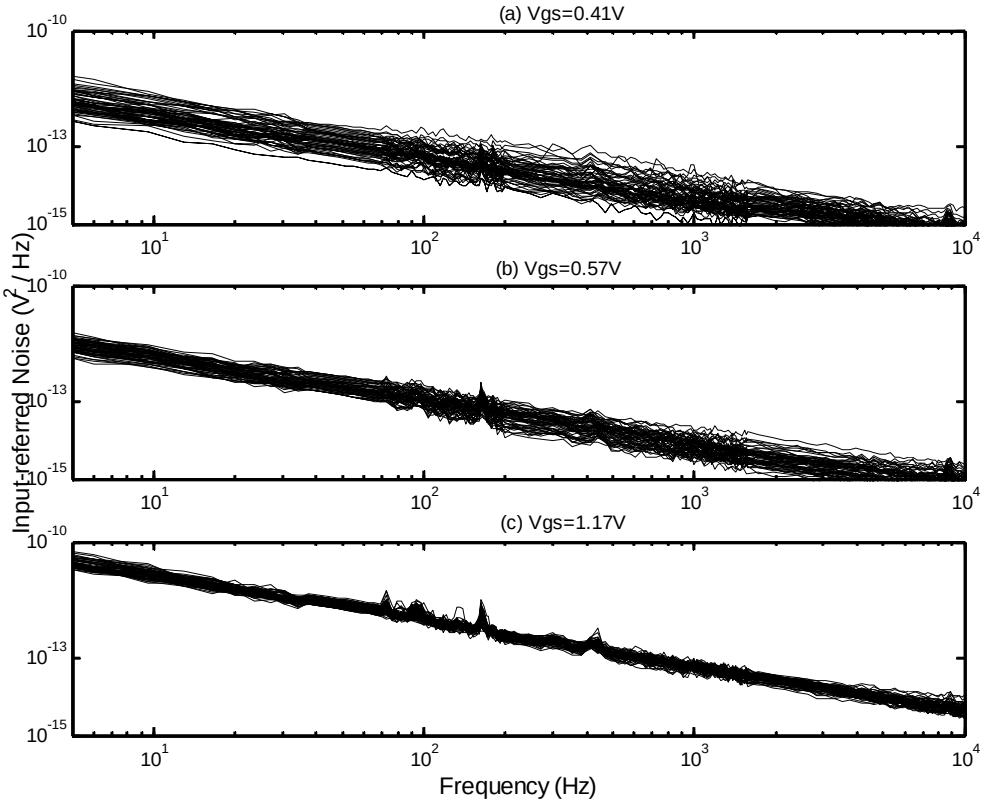


Figure 6.4: Noise variation is shown to decrease as gate voltage is increased. pFET, W=100μm, L=0.12μm, Vds=1.0V.

The TCAD simulation results are plotted in the following figure. A general trend for the bias dependence of σ_α can be extracted from the TCAD data, by noting that (i) $N_{inv}(y)$ increases with increasing gate bias, and (ii) $\delta N_{inv}(y) / \delta y$ decreases with increasing gate bias due to the reduction in pinch-off and more uniform channel formation.

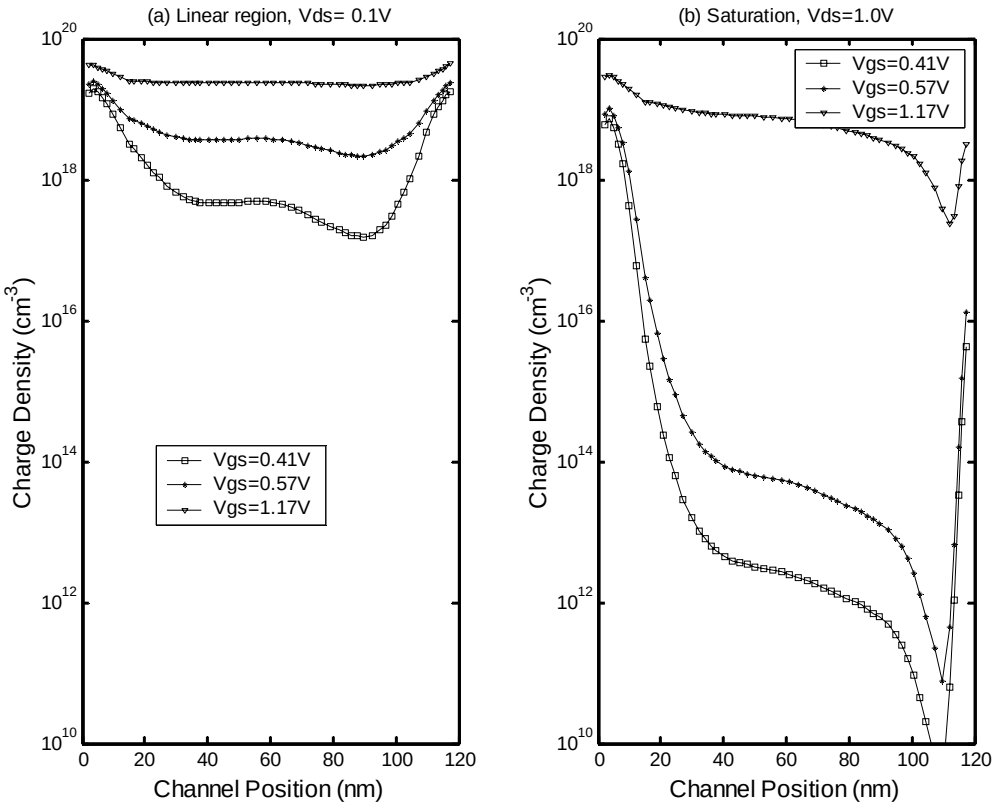


Figure 6.5: Charge density profile along the channel length of the pFET, W=100μm, L=0.12μm. (a) Linear region, Vds=0.1V, (b) Saturation, Vds=1.0V. pFET.

The local mobility along the channel length also has a spatial profile that is more uniform under high-Vgs low-Vds conditions and becomes non-uniform as the device goes into saturation, as illustrated by the TCAD data in the following figure:

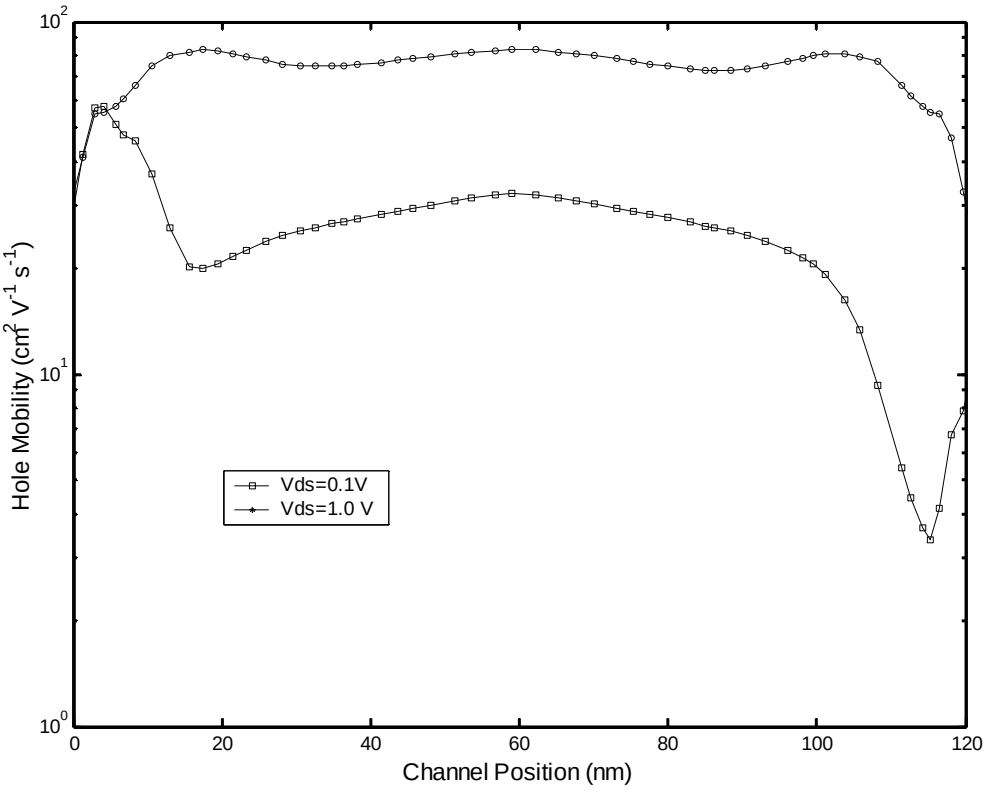


Figure 6.6: Hole mobility along the channel length. Vgs=1.17V, pFET, W=100pFET, W=100μm, L=0.12μm. Linear region and saturation.

In the linear regime $N_{inv}(y)$ increases and $\delta N_{inv}(y) / \delta y$ approaches zero, with increasing gate voltage. The second term in (6.11) vanishes and α is reduced. Under saturation, with increasing Vgs, $N_{inv}(y)$ increases and $\delta N_{inv}(y) / \delta y$ decreases. It follows that, for both regions of operation, the uncertainty in α decreases with increasing gate voltage.

In the generally accepted formula for input referred noise

$$S_{vg} = \frac{kTq^2}{\gamma f WLC_{ox}{}^2}(1+\alpha\mu\frac{(Vgs-Vt)\cdot C_{ox}}{q})^2 N_t(E_F) \qquad (6.7.)$$

both trap density N_t and the level of trap induced mobility scattering α have device-to-device statistical variability. While the variability of α is bias dependent as predicted by equation (6.11), the variability in N_t is not a function of bias, but rather it is dependent on device dimensions. Due to the discrete nature of the number of traps, N_t is expected to follow Poisson statistics. The number of traps for the i^{th} device, $n_{t,i}$, has an expected value of WLN_t, where WL is the device area. The variance of a Poisson random variable is equal to its mean value, thus the uncertainty in the number of traps, as defined to be the ratio of the square-root of variance to mean, is:

$$\frac{\sigma n_t}{\langle n_t \rangle} = \frac{\sqrt{WLN_t}}{WLN_t} = \sqrt{\frac{1}{WLN_t}} \tag{6.8.}$$

We have demonstrated that the site-to-site variability of 1/f noise is largely due to the statistics of trap density and location, and not correlated to other process variations in threshold voltage, g_m, etc. As gate voltage is increased, N_{inv} grows and becomes more uniform in space, reducing the impact of trap location on α, and hence reducing the uncertainty in α. This leads to a bias dependent variability in measured 1/f noise, with the largest noise variability found under low-Vgs high-Vds operation. Such conditions are most typical for analog and RF circuits. The findings of this work necessitate the reconsideration of the biasing conditions of transistors in noise sensitive circuits.

6.4 Graphical Representation of Spatial Trap Statistics

In the preceding analysis we have shown that a steep gradient in the inversion layer profile leads to a large variation in 1/f noise due to the increased sensitivity to trap location. To visualize this effect consider two traps at two different locations along the channel of a MOSFET, as illustrated by the 'circle' and 'diamond' in the following figure:

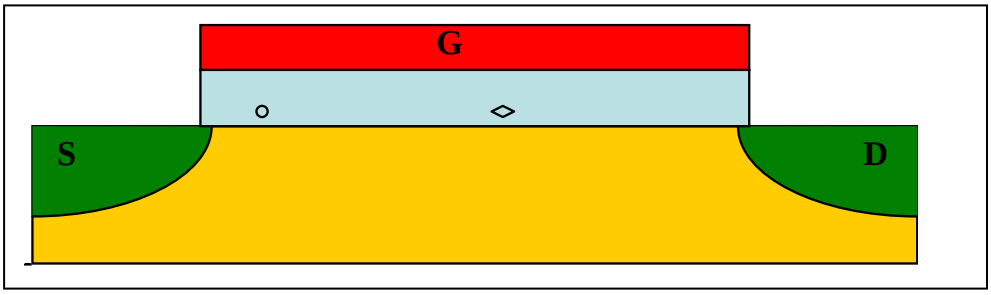


Figure 6.7: Traps located at different points across the channel of a MOSFET

When the inversion layer has a uniform spatial profile, both traps interact with similar carrier densities, exhibiting similar mobility fluctuations:

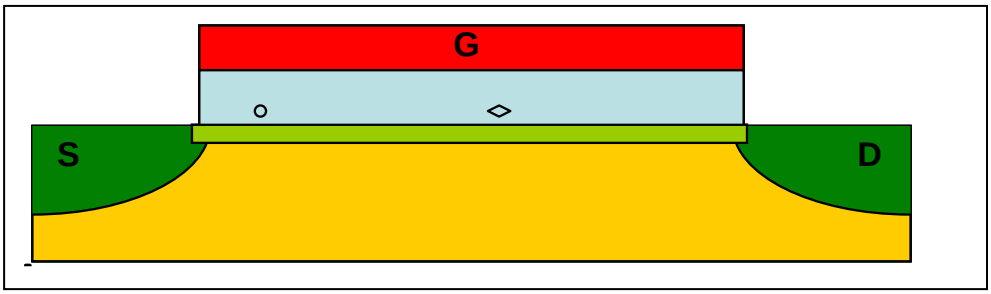


Figure 6.8: Under uniform inversion layer each trap contributes to 1/f noise similarly.

However, when the inversion layer has a non-uniform spatial profile, each trap will exhibit different mobility fluctuations due to the difference in carrier density within their vicinity:

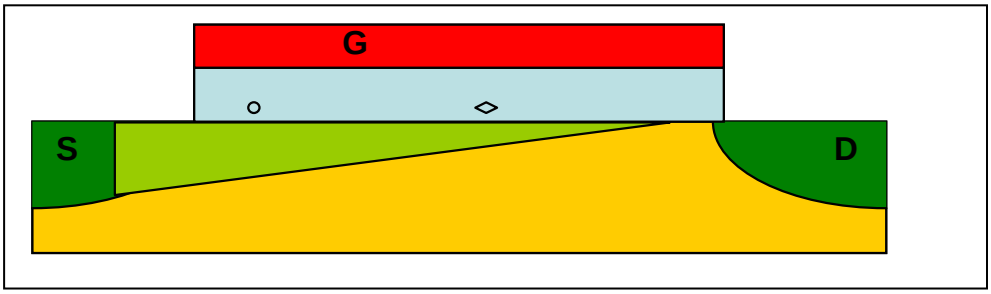


Figure 6.9: With inversion layer gradient, the contribution of each trap to 1/f noise changes.

In the extreme case, with high Vdd and low Vgs bias, one of the traps may infact show no contribution to low- frequency noise:

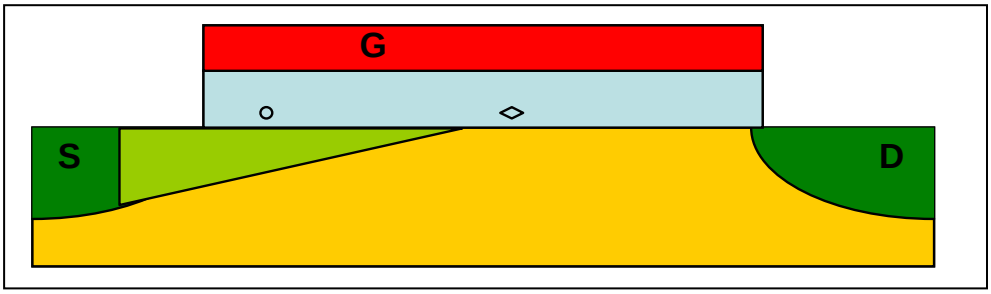


Figure 6.10: During pinch-off, some traps may stop contributing to 1/f noise altogether.

This graphical representation is only used to illustrate the implications of equation 6.11.

7. RF CMOS VCO Phase Noise

7.1 Low-Frequency Noise Upconversion

The Voltage Controlled Oscillator is one of the key components of many analog systems. It offers the unique functionality of 'adjustable output frequency'. As shown in Fig. 1.1 (repeated in 7.6 for completeness) a VCO utilizes an inductor-capacitor tank, where the changes in capacitance lead to changes in oscillation frequency. This feature is used in filtering applications as well as in phase-locking in PLL (phase-locked loop) based frequency synthesizers.

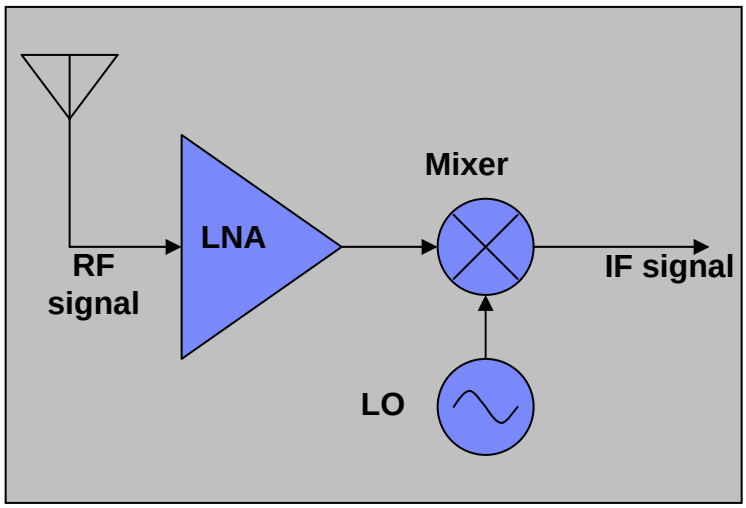


Figure 7.1: Front-end of a wireless communication system.

The LO (local oscillator) output is used to downconvert the RF signal. When multiplied, two sine waves produce a frequency shift, or

$$\sin(\omega_1 t)\times\sin(\omega_2 t)=\frac{1}{2}\left(\cos((\omega_1-\omega_2)t)-\cos((\omega_1+\omega_2)t)\right) \qquad (7.1.)$$

Therefore it is critical that local oscillator does not have any sidebands in the frequency domain.

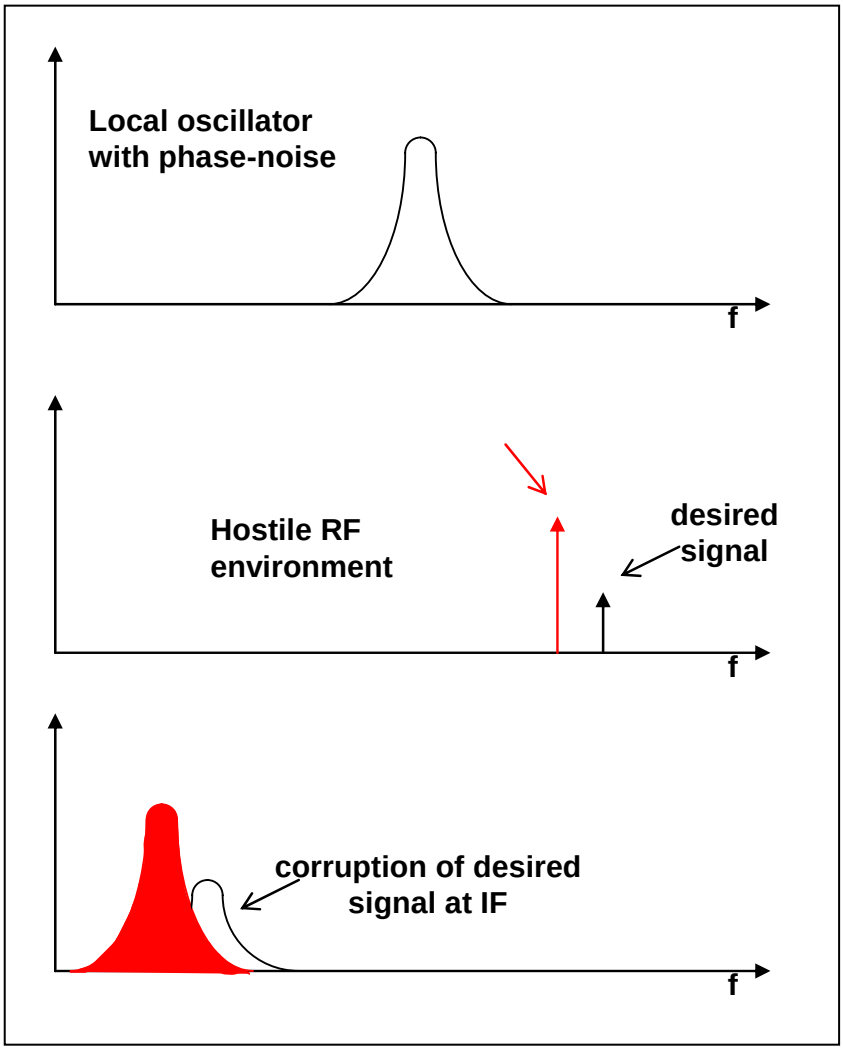


Figure 7.2: Frequency domain representation of phase noise.

In an ideal oscillator, the output waveform is a pure sinusoid, which is given by:

$$Y = A\cos(\omega t + \phi) \tag{7.2.}$$

where A, ω, and ϕ are the amplitude, frequency, and phase of the output waveform respectively. All three of these parameters are ideally constant. In an ideal tunable oscillator, the value of ω can be externally modified, however once set, it does not exhibit any random variations in time. Such a waveform is shown in the following figure. Note that the zero-crossing of the waveform are equally spaced. In other words there is no uncertainty in the phase of this waveform.

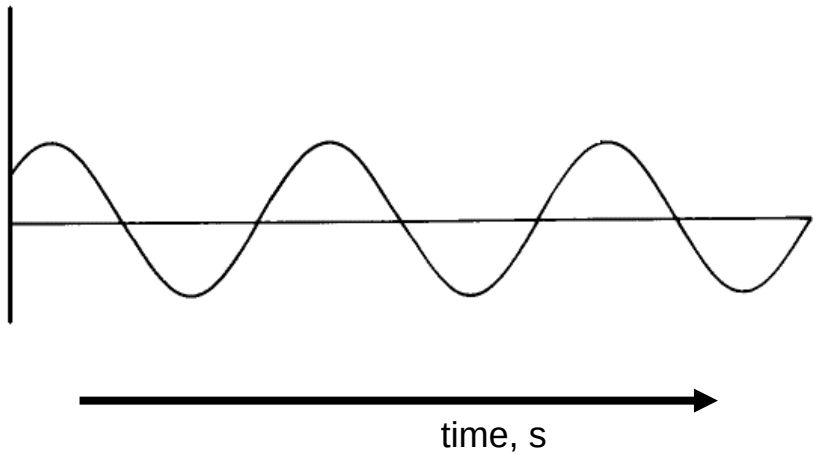


Figure 7.3: Pure sinusoid.

The ideal waveform does not have any harmonics. In other words it is represented as a single spike in the frequency domain. In some real oscillators this assumption does not hold. In the time domain the output waveform of such oscillators may look like:

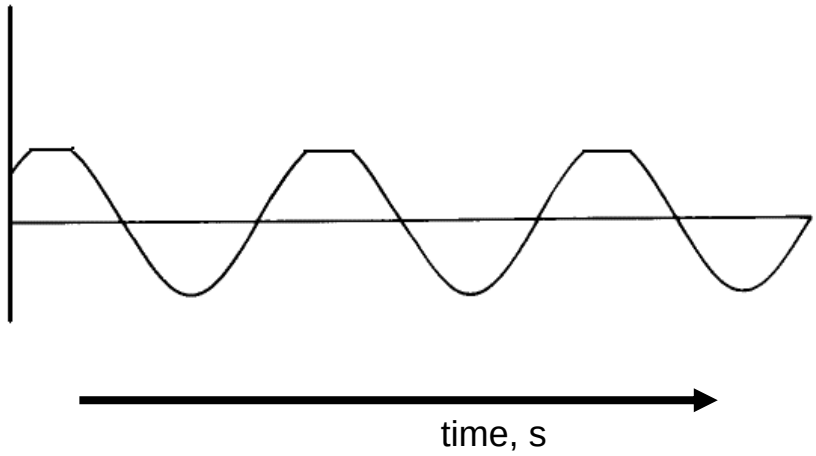


Figure 7.4: Distorted sinusoid.

This effect is known as ‘clipping’ or ‘distortion’, and it leads to extra components in the frequency domain.

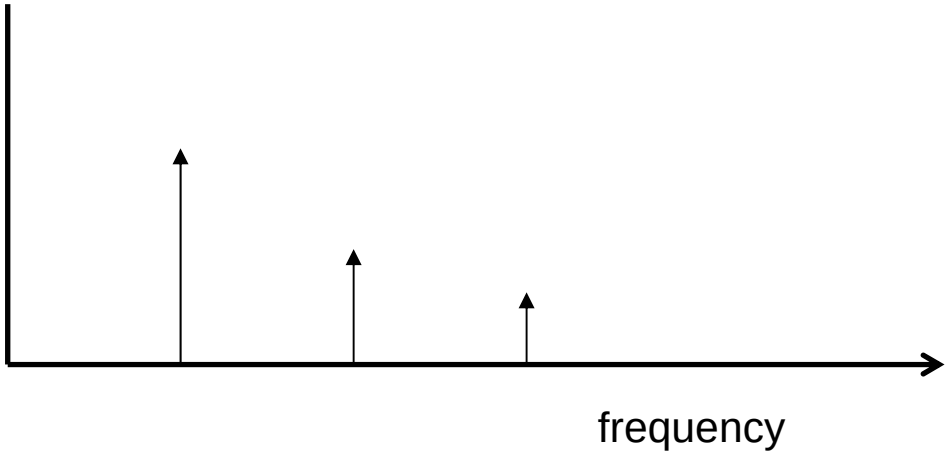


Figure 7.5: Spectrum of distorted waveform.

In the context of RF VCOs utilizing the common LC tank configuration, as shown below, there are two common mechanisms that limit the amplitude of the waveform.

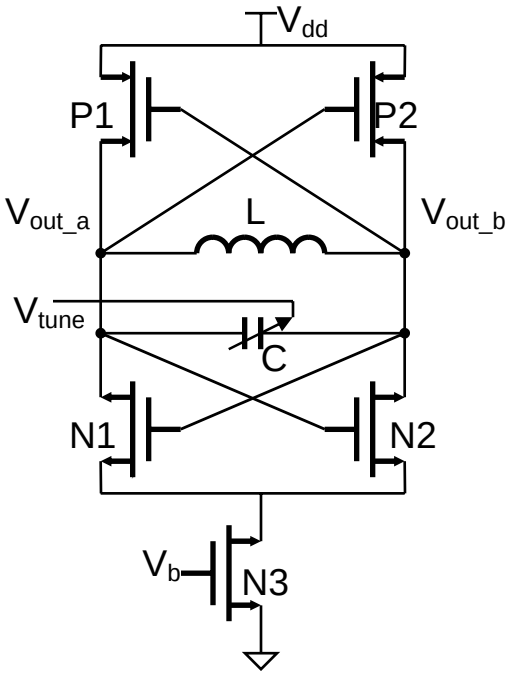


Figure 7.6: LC tank based VCO schematic commonly used in RF CMOS systems.

(i) In the voltage-limited operation of a VCO, the output amplitude is limited by the power supply, or 'rail' voltages. In this mode amplitude distortion is possible and the output spectrum is likely to exhibit the harmonics shown in Fig 7.5.

(ii) In the current-limited operation of a VCO, the output amplitude is limited by the biasing current of the circuit, for instance I_{N3} (I_{bias}) in the schematic shown in Fig 7.6. In this mode amplitude distortion is unlikely and the output spectrum is free of harmonics.

In most applications utilizing a VCO, the spectral purity of the waveform is of great importance, and therefore the current-limited operation is preferred. The value of I_{bias} impacts the output waveform in a number of ways. To a first order, the amplitude is A is proportional to I_{bias}, or

$$A = k_1 \cdot I_{bias} \tag{7.3.}$$

In addition to determining the oscillation amplitude, I_{bias} plays another critical, but somewhat indirect, role in determining the oscillation frequency, ω. Note that ω is determined by:

$$\omega = \frac{1}{\sqrt{LC}} \tag{7.4.}$$

where L is the tank inductance and C is the tank capacitance set by a variable capacitor:

$$C = k_2 \cdot V_{cap} \tag{7.5.}$$

Real varactors do not have a linear C-V curve for all bias points. However a typical C-V curve does have a region where capacitance varies linearly with voltage as depicted by equation 7.4. The voltage across the capacitor is given by:

$$V_{cap} = V_{tune} - V_{out,CMM} \tag{7.6.}$$

V_{tune} is set external to the VCO and for the purpose of this discussion is assumed to be noise free. The common-mode output voltage, $V_{out,CMM}$, is given by:

$$V_{out,CMM} = V_{dd} - \left(I_{bias} \cdot R_p \right) \tag{7.7.}$$

where R_p is the effective resistance of the each of the pFETs in the pFET pair.

As the bias current determines the oscillation frequency, any modulation in the current will alter the oscillation phase. If the frequency decreases with a small change in current, this moves the waveform zero-crossing further in time. Even if the current level and oscillation frequency return back to its fixed predetermined value, the change in phase is not recovered in a free running (non-phase-locked) oscillator.

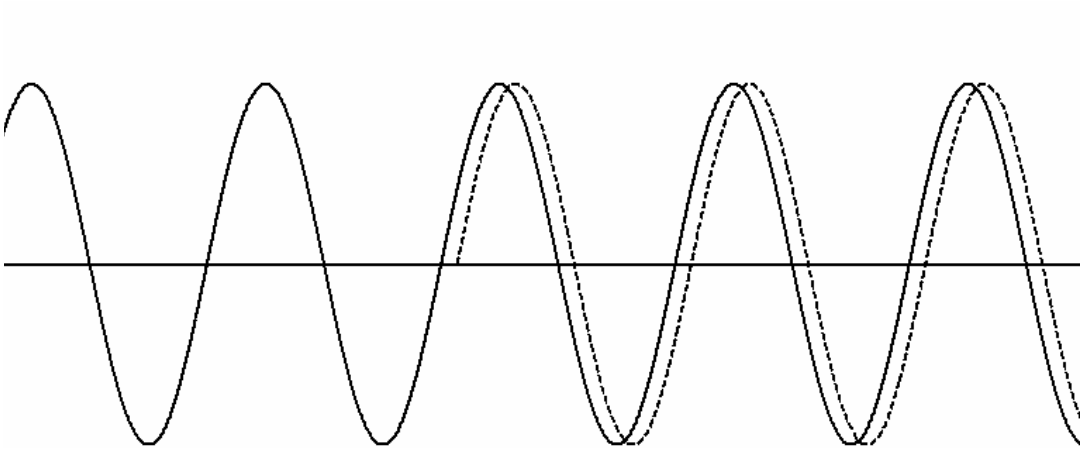


Figure 7.7: The modulation in phase can be due to a frequency shift or an amplitude shift.

I_{bias} cannot be assumed to be noise free. At any given point in time it maybe perturbed by a low-frequency noise causing trapping event, or

$$I_{bias} = I_{bias,\,fixed} + \Delta I \ . \tag{7.8.}$$

The change in drain current modulates the amplitude of the oscillation (equation 7.2), the frequency of operation (equation 7.3 through 7.6), and as a combined effect of the two, the phase of the oscillation, thus

$$\phi(t) = f(k_1, k_2, I_{bias}, \phi_0) \, . \tag{7.9.}$$

The functional relationship is fairly complex [Hajimiri, 1999], but for the purpose of this dissertation, *f* does not need to be written in close form.

From the preceding analysis we can study the impact of noise in I_{bias} on VCO output. Equation 7.1 can be rewritten as

$$Y = k_1 \cdot I_{bias} \cos\left(\frac{t}{\sqrt{L \cdot k_2 (V_{tune} - (V_{dd} - I_{bias} \cdot R_p)}} + f(k_1, k_2, I_{bias}, \phi_0) \right) \qquad (7.10.)$$

Equation 7.10 can be used to study the up-conversion of low-frequency noise in I_{bias} to VCO phase noise. For instance we can see that for oscillators with large frequency gain, where k_2 is large, noise in I_{bias} will be further amplified. Similarly keeping the effective resistance of the cross-coupled transistor pair will reduce the phase noise contribution of the 1/f noise in I_{bias}. It is shown in [Hajimiri, 1999] that keeping the waveform symmetric also reduces 1/f noise up-conversion.

7.2 Design & Fabrication of RF CMOS VCOs

Up to now there has been no published data or analysis on the statistical variability of VCO phase noise that can be seen in a population oscillator circuits. In this section of this dissertation, I present experimental data, theoretical analysis, and model-to-hardware correlation on VCO phase noise statistics. The findings of this study are crucial for the RF IC design community since VCOs are used in a wide range of systems-on-chip. An

accurate model that predicts the statistical variations in VCO phase noise is necessary for successful designs.

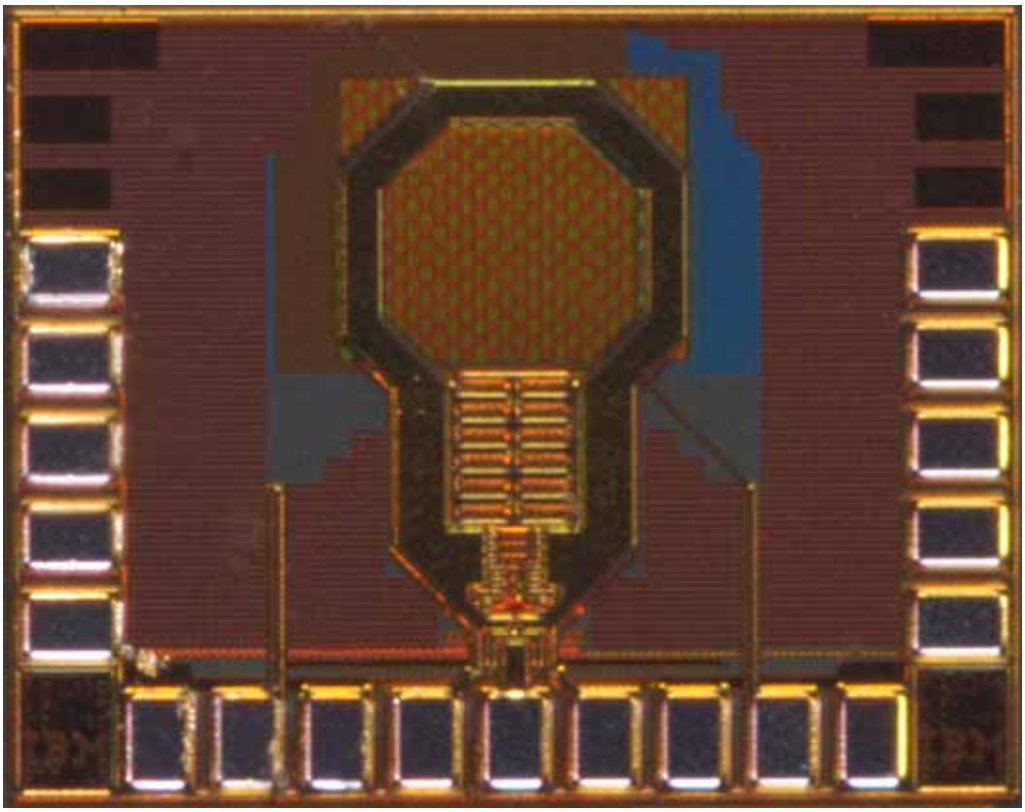


Figure 7.8: VCO Chip micrograph.

To study statistics of VCO phase noise, we have designed and fabricated an RFCMOS VCO suitable for GSM applications using a 180nm BiCMOS design kit and process. In this negative-resistance LC-tank design, we use an on-chip inductor constructed with dedicated analog metal which is 4um thick and only has 7mΩ/square sheet resistance. The variable capacitance of the LC-tank is achieved using a p-n junction diode that is readily available as a 'free' varactor in this process. Along with the varactor, high-Q

MIM (metal-insulator-metal) capacitors are used in the tank. The tank loss regeneration is achieved by cross-coupled nFET & pFET pairs. The tail current source establishing the DC operating point and driving the differential circuit is a nFET sized for reduced 1/f noise, while keeping gate leakage and chip area in consideration.

Figure 7.9: Population of VCO chips used in Statistical Analysis.

Note that the goal of this analysis is not to achieve the lowest possible phase noise in this technology, but rather to illustrate the impact of transistor 1/f noise variations on circuit phase noise.

7.3 Data Analysis and Model Correlation

Phase noise measurements have been taken using Agilent E5052A Phase Noise Analyzer. The E5052A is also used as the power supply, providing the power to the VCO, as well as the tuning voltage. When powered with a 3V supply voltage, the VCO consumes 16.73 to 16.82 mA of current, and can be tuned from 3.24GHz to 3.34GHz. The phase noise measured on a single chip is shown in Fig. 7.10. The transition between the -30dBc/Hz per decade and -20dBc/Hz per decade slope takes place around 300kHz offset frequency.

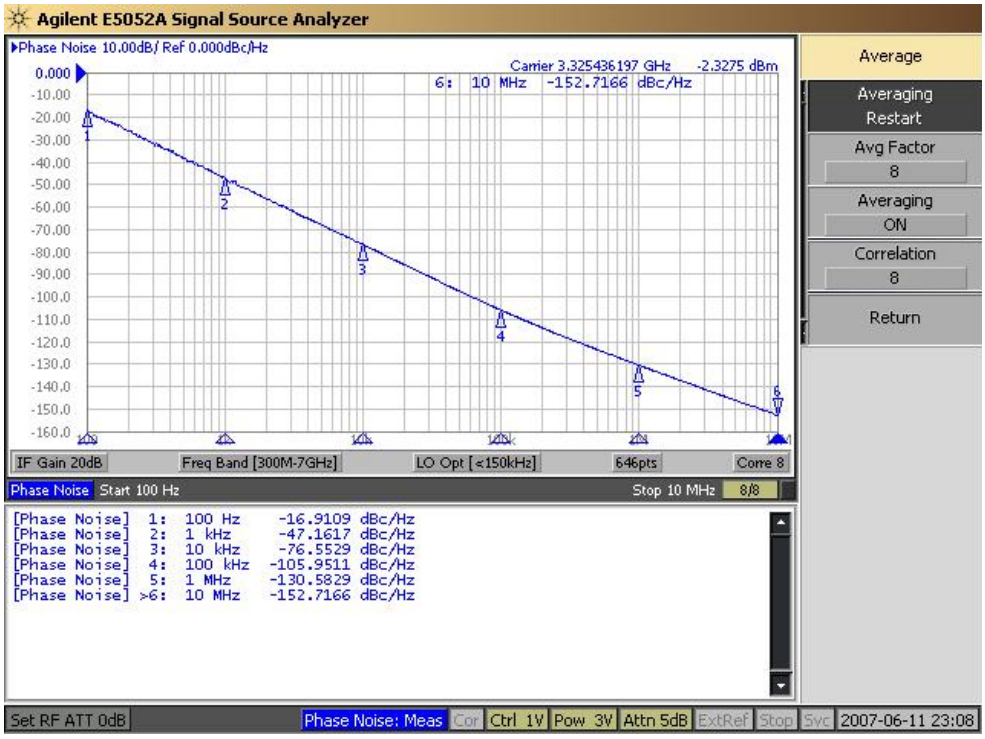


Figure 7.10: Phase noise measured on a single chip.

This design suffers from 1/f noise up-conversion as can be seen in the -30dBc/Hz per decade slope of close-in phase noise. Therefore the site-to-site variation in device 1/f noise is expected to be seen in measured phase noise. To test this hypothesis we

compared phase noise measurements to simulations using two versions of our recently developed statistical 1/f noise model. Phase noise measurements have been taken from a population of 50 VCO chips. The measured phase noise is overlaid with 3 simulation runs, (i) worst case prediction of the model, (ii) nominal prediction of the model, and (iii) best case prediction of the model.

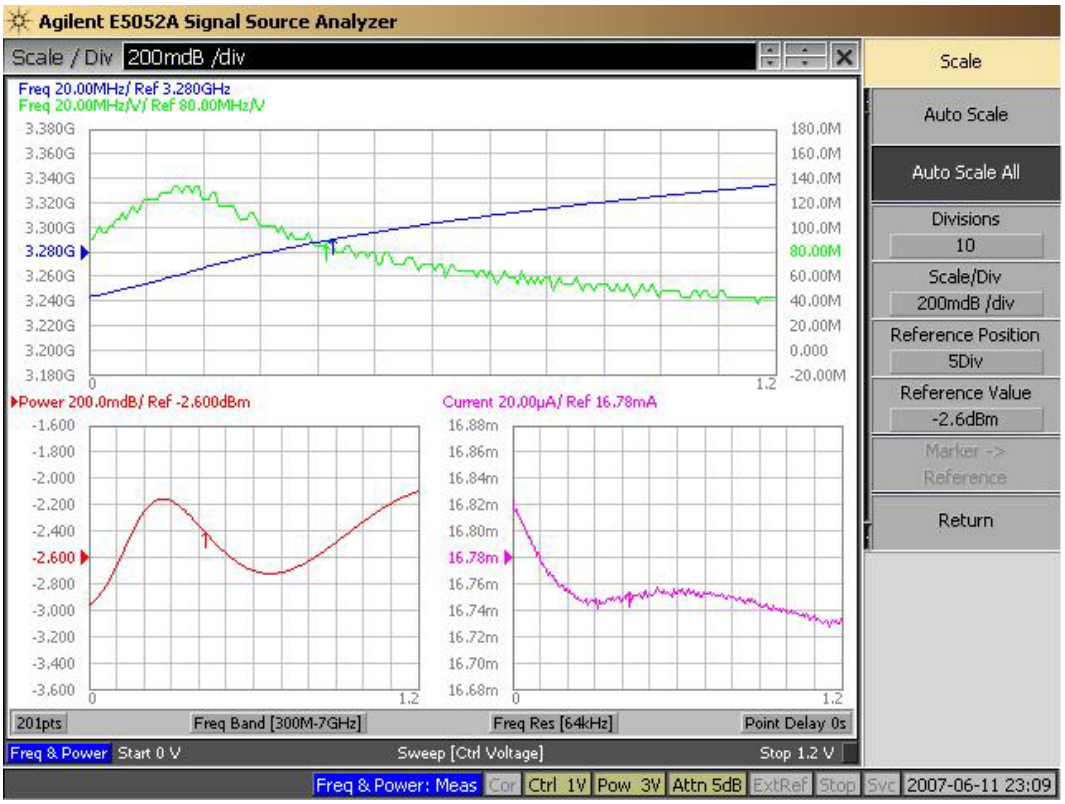


Figure 7.11: Measured VCO tuning curve, power consumption, and current.

In our initial "bias independent statistical 1/f noise model", a 3-σ noise multiplier is extracted from measured data. This multiplier is then applied to all three BSIM noise modeling parameters, NOIA, NOIB, and NOIC. This effectively scales the noise power

regardless of gate or drain bias. The bias independent model accurately predicts the device area dependence of noise variability as shown in [Erturk, 2005]. In the following figure, we show close-in phase noise measurements, as well simulation results with the bias-independent statistical 1/f noise model. The worst-case – best-case model simulations span the variation seen in measurement. However, the prediction in the phase noise spread is too pessimistic. This is attributed to the fact that 1/f noise variability is reduced with increasing gate bias.

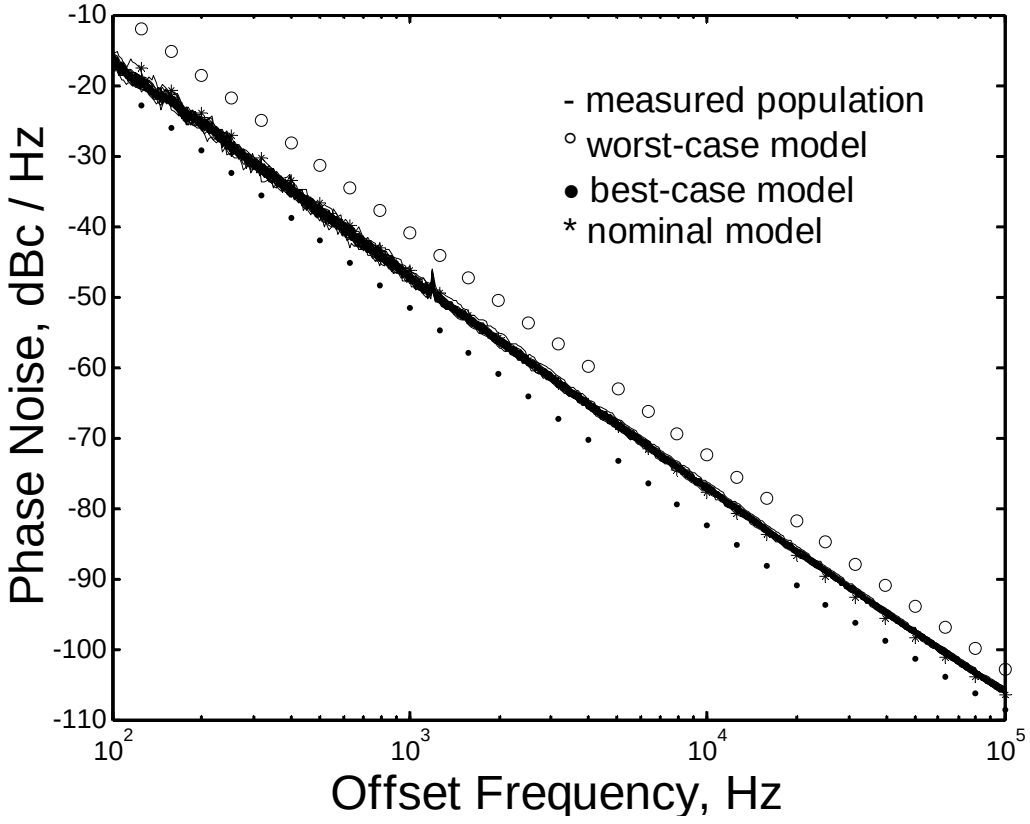


Figure 7.12: Measured and simulated statistical phase noise. Vdd=3V, Vtune=1V, Vbias=2.6V.

As discussed in Chapter 6, 1/f noise is less sensitive to trap location as the channel becomes more uniform. In other words, as the gate voltage is increased, the site to site variation observed in 1/f noise is reduced. To capture this effect in noise simulations, we assign different multipliers to each of the noise parameters, NOIA, NOIB and NOIC as shown in Chapter 5, equations 5.4 through 5.6. Figure 7.13 shows simulations using this the bias-dependent model, whereas Figure 7.12 shows simulation results with the earlier version of our model where each noise parameter was scaled with the same multiplier. As can be seen, a much better correlation to measurement is observed when separate multipliers are used to scale the noise parameters.

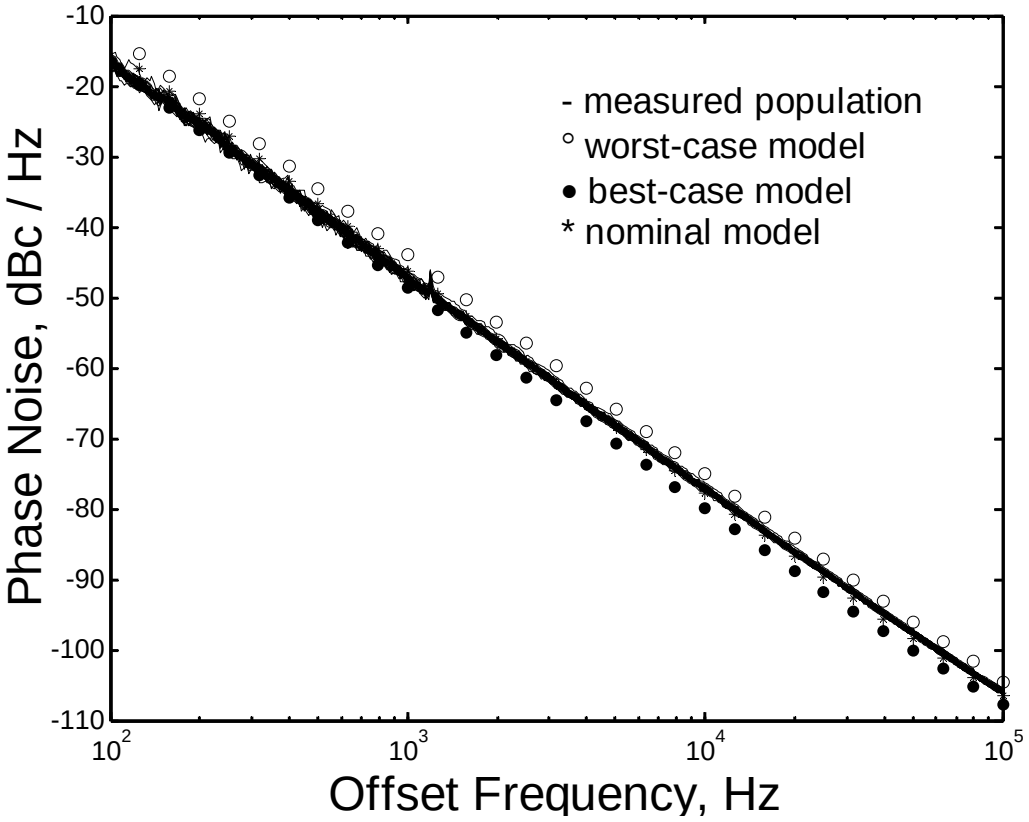


Figure 7.13: Measured and simulated statistical phase noise, using the bias-dependent statistical 1/f noise model. Vdd=3V, Vtune=1V, Vbias=2.6V.

As shown in Fig. 7.13, the worst-case – best-case model simulations span the variation seen in measurement without any excess over-prediction of phase noise variability. This improved model enables circuit designers accurately trade-off power, cost, and performance.

The phase noise simulations are run on the VCO schematic. The process statistics simulation feature of the design kit is employed. A particular "noise-corner parameter" is

used to control transistor noise statistics. The noise-corner parameter is set to 0 for nominal model prediction. The model implementation was summarized in the equations of Chapter 5:

$$M = \ln(k) - \min(\ln\sqrt{\frac{w \cdot l}{A_0}}, 0) \tag{7.11.}$$

$$NOIA = NOIA_{\text{nominal}} * e^{D \cdot M} \tag{7.12.}$$

$$NOIB = NOIB_{\text{nominal}} * e^{D \cdot \frac{M}{J}} \tag{7.13.}$$

$$NOIC = NOIC_{\text{nominal}} * e^{D \cdot \frac{M}{J^2}} \tag{7.14.}$$

During the nominal simulations *D* has a value of 0. As such the 3 noise parameters, NOIA, NOIB, and NOIC acquire their nominal values.

For worst-case simulations the noise-corner parameter is set to 3. At the same time, other corner parameters controlling transistor characteristics (such channel length tolerance) are set to 3 as well, producing the "worst corner". In this case, *D* is equal to 3 in eqs. 7.12 - 7.14, increasing the final values of NOIA, NOIB and NOIC. Similarly *D* is equal to -3 for the best case simulations, reducing the final values of the noise parameters.

In the initial phase of our model, the bias dependence of noise statistics was not addressed. In other words J was assumed to be 1. The prediction of this model is shown in Fig. 7.12. In the improved model (Fig. 7.13) J is another fitting parameter extracted from measurement.

In summary, we measured phase noise from a population of 50 VCO chips to study the impact of the variations in device 1/f noise on circuit phase noise. We observed that phase noise has significant variability, 3dBc/Hz, at close-in frequencies, where 1/f noise gets up-converted. The variability at higher frequencies is less than 0.5dBc/Hz. The measurements have been compared to simulations employing two versions of statistical 1/f noise models. In the first model, the bias dependence of 1/f noise variability is not included. All three BSIM noise parameters are scaled with the same multiplier based on a Lognormal distribution. This model over-predicts the spread in VCO phase noise. The improved model, which independently scales the BSIM noise parameters to account for the bias dependence of 1/f noise statistics, accurately predicts the spread in VCO phase noise. The findings of this study are crucial for RFIC designers employing VCOs in their circuits. It is shown that without an accurate statistical 1/f noise model VCO phase noise can be grossly misestimated in simulations.

8. Conclusions and Future Considerations

A novel statistical model for MOSFET 1/f noise has been presented in this dissertation. The development of such a model requires thorough understanding of the impact of trap density, as well as trap spatial distribution, on 1/f noise.

In the first phase of this research, reliability experiments have been used to illustrate the impact of trap location on MOSFET 1/f noise. It has been shown that samples processed in a deuterium environment are much less likely to suffer from 1/f noise increase over the life time of the transistor. Electrical stress causing asymmetric damage, such as the Drain-Avalanche-Hot-Carrier effect, where interface traps are generated closer to the drain of the transistor, has been employed along with 1/f noise measurements taken in (i) linear, (ii) forward saturation, and (iii) reverse saturation modes. It has been concluded that the inversion charge within proximity of a trap influences the amount of 1/f noise caused by that trap. Under pinch-off, where the inversion density goes to zero near the drain, some of the DAHC induced interface states are found to be completely inactive in terms of their contribution to 1/f noise. Very high inversion charge density is found to mask the mobility fluctuations induced by the trap, whereas a low inversion charge density increases the amount of 1/f noise caused by the trap. A 1/f noise reliability model has been presented and its predictions are compared to measurements from devices subjected to electrical stress in Deuterium and Hydrogen passivated samples.

Next, 1/f noise measurements have been taken on various populations of transistors to study the device-to-device variability of 1/f noise. The geometry dependence of variability has been shown to be well predicted with a Poisson distribution for the total number of traps found in a given area. The bias dependence of the noise statistics has been attributed to the relationship between trap location and inversion charge spatial profile. The sensitivity to trap location has been used in developing a BSIM based statistical noise model which shows excellent agreement with hardware measurements. Through a novel expression derived for the uncertainty in the mobility fluctuation term, α,

$$\sigma_\alpha = \frac{\alpha_i}{\sqrt{12}}\left[T_{ox}{}^2 + \left(\frac{L_{eff}\beta}{N_{inv}(y)} \cdot \frac{\partial(N_{inv}(y))}{\partial y} \right)^2 \right]^{1/2} \qquad (8.1.)$$

we have shown that the gradient of the inversion layer plays a significant role in determining the variability in low-frequency noise.

The new models have been used in simulations at the device level as well as at the circuit level. Phase noise has been measured on a population of RF CMOS VCOs and compared to statistical simulations. It is shown that the bias dependence is a key factor in predicting the phase noise variability observed in measurements. The models developed within this dissertation have been shown to accurately predict the circuit-to-circuit variations in measured phase noise.

For further study, development of a closed form expression for the inversion layer density as it relates to carrier traps is of particular interest. In the present dissertation TCAD (Technology Computer Aided Design) tools have been used to simulate the inversion charge profile. In addition, statistical noise measurements and modeling in the time domain would provide further insights on the physics of 1/f noise. Such a model would also benefit circuit designers better understand the time domain properties of noise sensitive circuits and systems. The emerging areas of Multigate Field Effect Transistors, and metal gate devices with high permeability dielectrics have many questions to be answered on the topic of 1/f noise modeling.

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