Supporting Information for: Solution-Processed CdS Transistors with High Electron Mobility

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1. Detailed X-ray Photoelectron (XPS) Spectra

XPS spectra were collected for CdS films on substrates consisting of silicon with a 40 nm layer of thermally evaporated Au. A close-up of the Au 4f region (**Fig. S1a**) reveals that some Au signal is still apparent after depositing the CdS layer, indicating that the films do not completely cover the Au surface or are very thin in places (less than ~30 nm thick). A close-up of the Cd 3d region (**Fig. S1b**) reveals binding energies of 412.25 and 405.35 eV for cadmium $3d_{3/2}$ and $3d_{5/2}$ orbitals, respectively, consistent with Cd-S bonding. A close-up of the S 2p region (**Fig. S1c**) reveals binding energies of 163.0 and 161.9 eV for sulfur $2p_{1/2}$ and $2p_{3/2}$ orbitals, respectively, consistent with the presence of a metal sulfide. Very little difference is apparent in the XPS spectra of films prepared from either **CdTNT** or **CdTDT**.

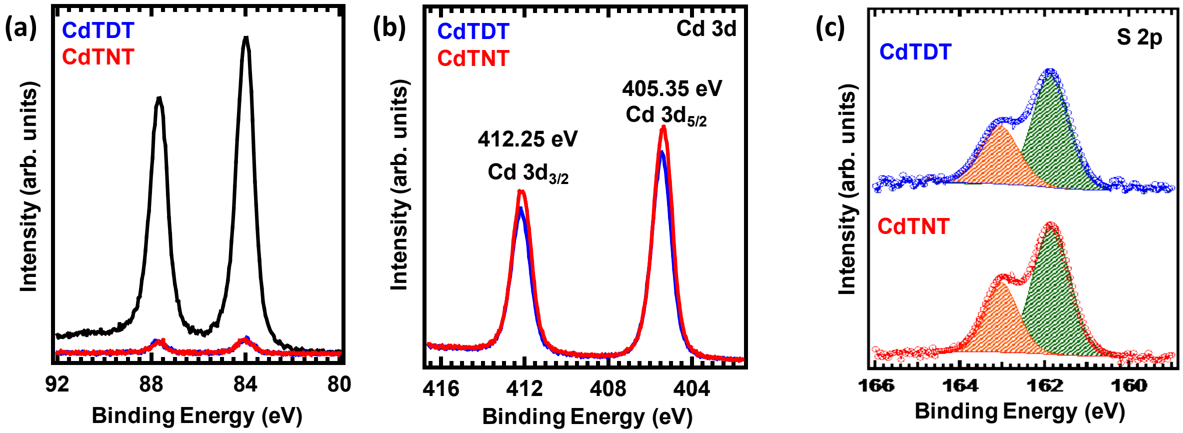

Figure S1 | XPS spectra. a) Close-up of Au 4f region of XPS spectra. b) Close-up of Cd 3d region of spectra. c) Close-up of S 2p region of spectra.

2. UV-vis Absorption

A UV-vis absorption spectrum was collected from a CdS film prepared by spincoating a **CdTNT** film on a glass substrate and annealing at 300 °C for 30 min in a nitrogen atmosphere (**Fig. S2a**). The spectrum exhibits an onset at 524 nm, yielding an optical bandgap of 2.37 eV.

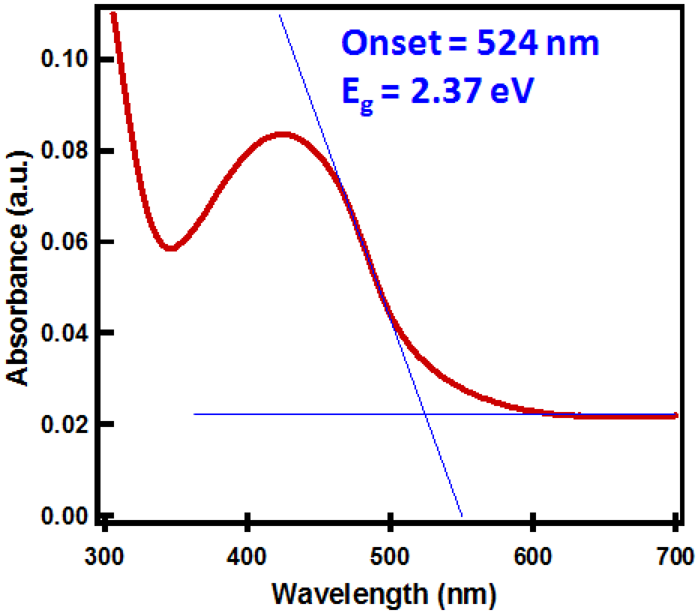

Figure S2 | UV-vis absorption spectrum of CdS film prepared by annealing a spin-coated **CdTNT** at 300 °C for 30 min.

3. Ultraviolet Photoelectron (UPS) Spectra

UPS spectra were collected from the same CdS films reported in the XPS section (**Fig. S3**). UPS spectra indicate a high binding energy cutoff of 16.41 +/- 0.05 eV for films prepared from either **CdTNT** or **CdTDT**. Subtracting this energy from the photon energy (21.22 eV) yields a workfunction of 4.81 +/- 0.05 eV. The low binding energy onset region may be used to calculate the valence band energy, however, the onset is very gradual making it difficult to accurately determine the energy of the band edge. The valence band energy was estimated from the low binding energy onset and determined to be ~6.65 eV for CdS prepared from both **CdTNT** and **CdTDT**. Subtracting the optical band gap from the valence band energy yields an approximation of the conduction band energy (~4.3 eV).

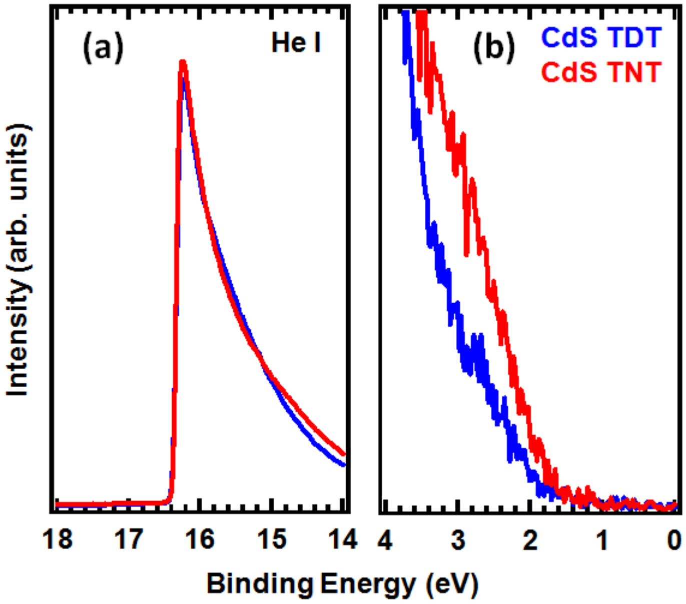

Figure S3 | Ultraviolet photoelectron spectra of CdS films prepared from **CdTNT** and **CdTDT**. a) Secondary edge region used to determine work function. b) Low binding energy onset region used to determine valence band energy.

4. X-ray Diffraction

X-ray diffraction was performed on CdS films prepared from thiolates in order to characterize their crystal structure. Single layers did not yield a strong enough signal to identify. Thus, 8 layers were prepared on a silicon substrate (as described in the experimental section of the main text) using **CdTNT** precursor. The diffraction pattern of a film prepared in this way is reported in **Fig. S4** and can be identified as the Greenockite phase of CdS.

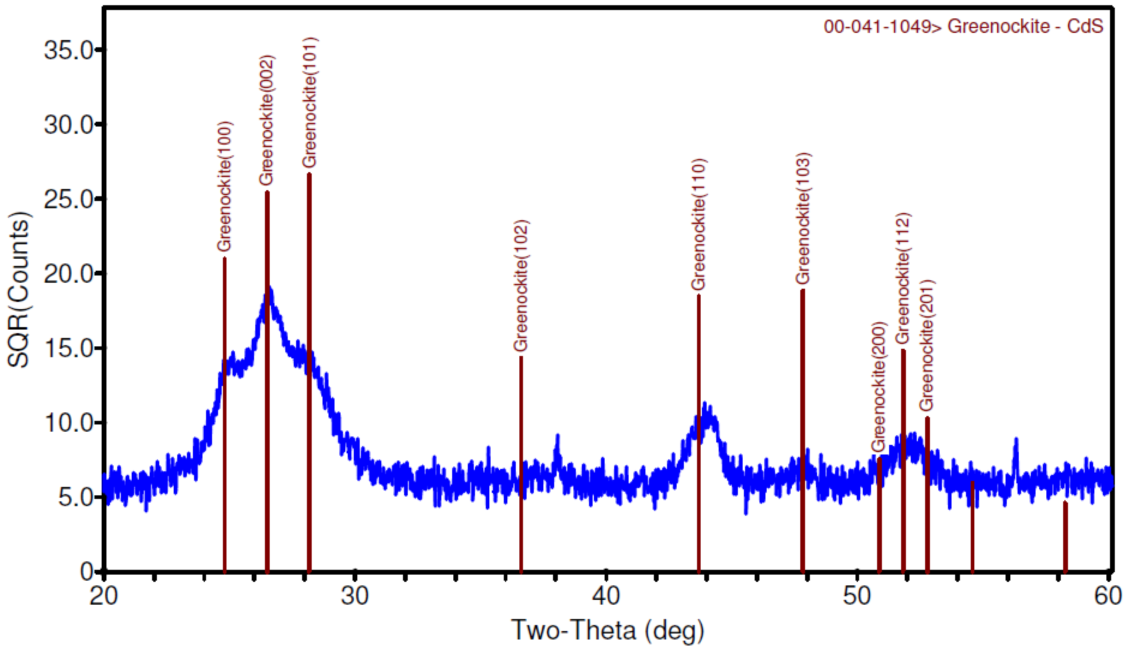

Figure S4 | X-ray diffractogram of CdS film prepared by sequentially spincoating **CdTNT** and annealing at 300 ^{o}C for 5 min. seven times, followed by a final layer of spincoated **CdTNT** and annealing at 300 ^{o}C for 30 min.

5. Comparison of Transistor Characteristics of Pristine CdS Films and Films Exposed to Air

The effect of air exposure and subsequent annealing on the performance of field effect transistors prepared from **CdTNT** were investigated. Transfer curves of pristine devices, devices after air exposure and devices after air exposure and a final annealing step in nitrogen are reported in **Fig. S5**. The pristine devices exhibit a negative turn-on voltage and a high current in the off state. This could be explained by the presence of free charge carriers or n-doping in the pristine device. Exposure to air dramatically alters the transfer characteristics of the devices, leading to dramatically reduced current through the devices and pronounced hysteresis between the forward and reverse scans. A final annealing step at 300 ^{o}C in a nitrogen environment greatly improves the device characteristics, which exhibit relatively low off currents compared to pristine devices and improved carrier mobility compared to air-exposed devices. Exposure of the thiolate to sulfur during annealing at lower temperatures (160 ^{o}C) leads to yellow CdS films which are much smoother than the films annealed at 300 ^{o}C, however, in contrast to the n-type transport behavior observed in the other films, these devices turn on at negative gate bias and show weak p-type transport.

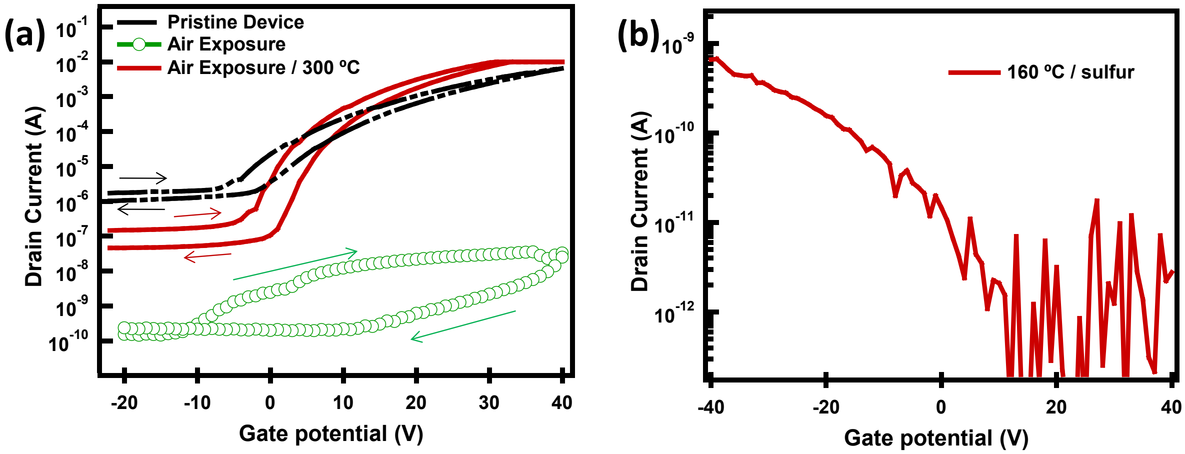

Figure S5 | Transfer curve of CdS devices. a) Comparison of pristine CdTNT devices after annealing at 300 ^{o}C to devices exposed to air (1 hr.) and devices after air exposure and additional annealing for 30 min. at 300 ^{o}C in nitrogen. b) Device prepared by annealing a CdTDT film in the presence of elemental sulfur at 160 ^{o}C for 15 min.

6. Device Stability

A brief investigation of film and device stability was carried out. CdS films were prepared from CdTNT as usual following the optimized procedure described in the main text and stored in air for 1 week, followed by annealing in nitrogen and electrode evaporation. These devices exhibited mobilities of 35 cm^2/Vs, similar to control devices. Devices were aged in a glovebox (with O_2 content <20 ppm) for 1 week. A small decrease in current and mobility was observed from 30 cm^2/Vs (pristine) to 18 cm^2/Vs (week old). After annealing at 300 ^{o}C for 20 min in nitrogen, the performance was largely recovered and the devices exhibited a mobility of 34 cm^2/Vs; slightly higher than the original mobility, though the overall current was slightly lower and the threshold voltage increased from 8V to 14 V. These curves are plotted in **Figure S6a**. To investigate the air stability of the finished FETs, completed devices were also aged in air for 1 week, then brought into a nitrogen filled glovebox and annealed at 300 ^{o}C for 20 min. The overall change was very similar to that observed for the devices aged in nitrogen, where the currents decreased slightly and the threshold voltage increased slightly. The original mobility was 45 cm^2/Vs and the mobility after aging in air for 1 week and annealing in nitrogen was 41 cm^2/Vs. These curves are plotted in **Figure S6b**.

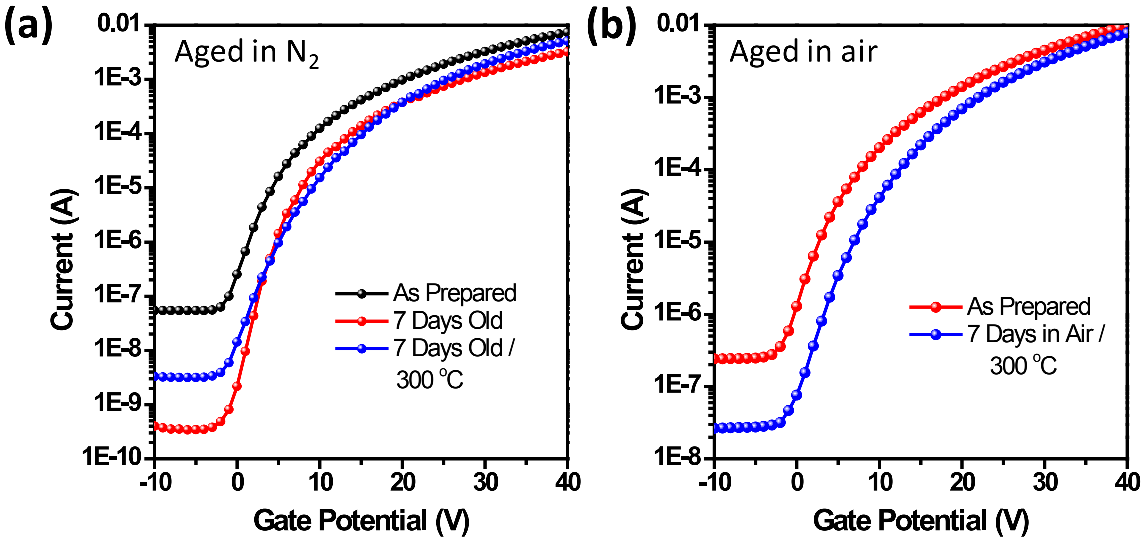

Figure S6 | Transfer curve of CdS devices. a) Comparison of pristine CdTNT based devices after storing in nitrogen for 1 week and subsequently annealing. b) Comparison of pristine CdTNT based devices after storing in air for 1 week and annealing.

7. Appearance of CdS Films on Glass Substrates

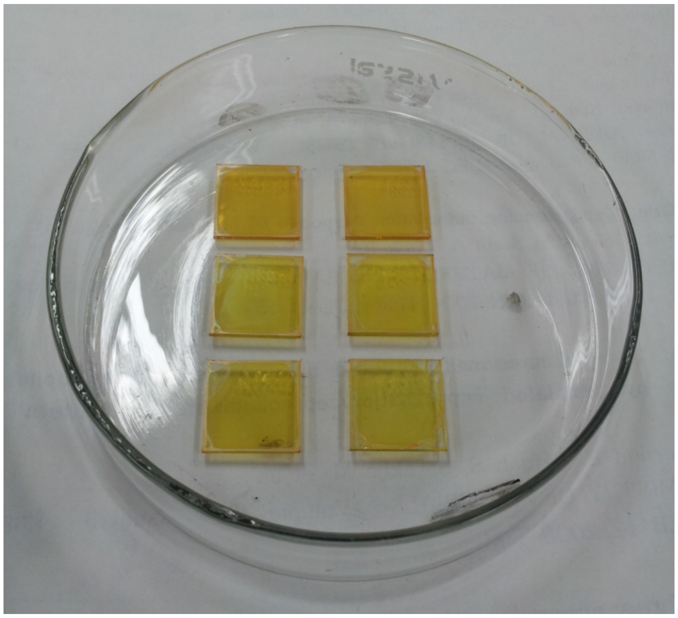

Figure S6 | Digital image of CdS films deposited by spincoating a CdTNT solution in chloroform (8 mg/mL) onto glass substrates and thermally annealing at 300 °C.

8. Experimental Details

CdTNT Synthesis. Cadmium oxide (Aldrich, 99.99%, 115 mg), tert-nonyl mercaptan, (Aldrich, >97%, 400 µL) and 10 mL of chloroform are placed in a tightly-capped 20 mL vial and magnetically stirred at 50 ^{o}C until the brown CdO has dissolved and a viscous, translucent solution is obtained (this typically takes 3-8 weeks). The solution is diluted to 20 mL with additional chloroform, passed through a 0.45 µm PTFE syringe filter and precipitated directly into 200 mL of well-stirred ethanol. The supernatant liquid is decanted and the solid is rinsed with additional ethanol, then dried under a stream of argon. The material is sensitive to UV light.

CdTDT Synthesis. The same procedure employed for CdTNT is used to prepare CdTDT, with the exception that 100 mg of cadmium oxide are used, and tert-dodecyl mercaptan, (Aldrich, >98.5%, 400 µL) is used instead of tert-nonyl mercaptan.

CdTNT Synthesis (II). Cadmium acetate (Aldrich, 99.995%, 200 mg), tert-nonyl mercaptan, (Aldrich, >97%, 1 mL) and 10 mL of chloroform are placed in a tightly-capped 20 mL vial and magnetically stirred at 50 ^{o}C overnight yielding a transparent solution. The solution is diluted to 20 mL with additional chloroform, passed through a 0.45 µm PTFE syringe filter and precipitated directly into 200 mL of well-stirred ethanol. The supernatant liquid is decanted and the solid is rinsed with additional ethanol (50 mL), then immersed in a 2% solution of tert-nonyl mercaptan in ethanol for 1 hour. Again, the supernatant liquid is decanted and the solid is rinsed with additional ethanol (3 x 50 mL) then dried under a stream of argon.

FET Fabrication and Characterization. Silicon substrates with a 200 nm oxide layer (Silicon Prime Wafer) were cleaned by scrubbing in a detergent solution, sonicating in a detergent solution (10 min), sonicating in DI water (2 x 10 min) and sonicating in isopropanol (10 min), then blown dry with compressed nitrogen. The substrates were kept in a closed petri dish in an oven at 100 ^{o}C until used. CdTNT or CdTDT were dissolved in chloroform in a nitrogen filled glovebox at concentrations of 8 mg/mL or 15 mg/mL, respectively. The solutions were passed through a 0.45 µm PTFE syringe filter (with some difficulty) and kept in pre-cleaned vials. The solutions were spin-coated by rapidly dispensing 40 µL at a time (using a micropipette) onto pre-cleaned Si/SiO_2 substrates which were already spinning at 1500 rpm. The viscous nature of the solution and low boiling point of chloroform require that the solution be dispensed quickly, before the material on tip of the pipette becomes gelatinous, which tends to result in blemishes in the spincoated film. The films were then annealed on a hotplate under a nitrogen atmosphere at 300 ^{o}C for 30 min. A digital image of CdS films prepared on glass substrates is included as a reference showing good quality CdS films free of visible blemishes. If two or more layers were deposited, the first layer(s) were annealed at 300 °C for 5 min, while the final layer was annealed at 300 °C for 30 min. Source and drain contacts were deposited by thermally evaporating Ag slugs (Alfa Aesar, 99.99%) at a pressure of ~ 10^{-6} Torr through shadow masks to yield devices having a channel length of 50 µm and a length to width ratio of 48. Devices were tested using a probe station equipped with a Keithley 4200 semiconductor characterization system under a nitrogen atmosphere.

Solar Cell Fabrication and Characterization. Solar cells were prepared beginning with indium tin oxide (ITO) substrates which were cleaned by scrubbing in a detergent solution, followed by sonication in in a detergent solution (10 minutes), dionized water (10 minutes, twice) and isopropanol (10 minutes). A zinc oxide layer was deposited on top of the ITO substrate in an adaptation of a previously described procedure by spincoating (at 3000 rpm) and annealing (at 110 °C) a filtered precusur solution consisting of 300 µL of diethyl zinc solution (5 wt% in toluene) and 600 µL of anhydrous tetrahydrofuran. CdS layers were prepared as described above, using CdTNT and a single annealing step at 300 °C for 1 minute. PTB7 layers were deposited by spincoating a 10 mg/mL solution in chlorobenzene at 1200 rpm. Devices were completed by thermally evaporating MoO_3/Au electrodes (5 nm / 80 nm) under a vacuum of 10^{-6} Torr through a shadow mask yielding devices with an active area of 13 mm^2. Current density – voltage characteristics were characterized under simulated AM 1.5G solar radiation using a Xenon arc lamp equipped with a KG5 optical filter and calibrated at 100 mW/cm^2 intensity using an NREL certified standard silicon photodiode. External quantum efficiency (EQE) measurements were obtained using a PV measurements OE system equipped with a Xenon arc lamp where monochromated light was chopped at a frequency of 100 Hz and photocurrent response detected with a lock-in amplifier and compared to a reference silicon photodiode.