Simple odd number frequency divider with 50% duty cycle

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Abstract: A simple odd number frequency divider with 50% duty cycle is presented. The odd number frequency divider consists of a general odd number counter and the proposed duty cycle trimming circuit. The duty cycle trimming circuit can output 50% duty cycle with only additional six transistors. A prototype divide-by-5 circuit with 50% duty cycle was implemented for a 500-Mb/s $\sim$ 5.6-Gb/s 1:10 CDR/DEMUX IC in a $0.13\,\mu m$ 1P8M CMOS process.

Keywords: odd number frequency divider, duty cycle

Classification: Integrated circuits

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1 Introduction

Odd number frequency dividers are often used in frequency synthesizers, clock generators, clock and data recovery (CDR) circuits, demultiplexers

(DEMUXs), etc [1, 2, 3]. For an example, a 2:10 DEMUX of a high speed serial interface receiver may need a divide-by-5 circuit for output clock signal generation. Although odd number frequency dividers do not have 50% duty cycle, they are sometimes required to have exact 50% duty cycle. It is because both of rising and falling edges of the divided clock signal can be used for efficient high speed operation. To obtain 50% duty cycle, special types of latches or flipflops have been generally used for odd number frequency dividers [2, 3, 4, 5]. A negative level sensitive latch was used in [2] and a current switchable D flipflop (DFF) was used in [3, 4, 5] for dual edge triggering operation in odd number frequency dividers. However, those special latches and flipflops require more circuit complexity and are not appropriate when a rail-to-rail signal swing is needed.

In this paper, we present a simple full swing odd number frequency divider with 50% duty cycle. The presented odd number frequency divider consists of a general odd number counter and the proposed duty cycle trimming circuit. For the odd number counter, single edge triggered CMOS DFFs are used. The duty cycle trimming circuit can output 50% duty cycle with only additional six transistors: i.e. one NMOS transistor, one PMOS transistor and a pair of cross-coupled inverters.

2 Proposed duty cycle trimming circuit

Fig. 1 shows the proposed odd number frequency divider with the division ratio of 5. It consists of a divide-by-5 circuit and a new duty cycle trimming circuit. The divide-by-5 circuit contains three rising-edge triggered DFFs and one NAND gate. The duty cycle of the divider's output clock signal, X, is not 50% but 60% because all the DFFs of the divide-by-5 circuit are triggered by the rising edge of the input clock signal, CLK_{IN}. So, the proposed duty cycle trimming circuit is added after this divider. The duty cycle trimming circuit consists of two transistors, M1 and M2, and a pair of cross-coupled inverters, INV_1 and INV_2, as shown in Fig. 1. M1 and M2 are an NMOS transistor and a PMOS transistor, of which gate, source and drain terminals are connected to each other. Because both gates of M1 and M2 are driven by the same CLK_{IN}, M1 can be turned on when $CLK_{IN}=1$ and M2 can be turned on when $CLK_{IN}=0$. Between the cross-coupled inverters, INV_1 and INV_2, the transistor sizes of INV_2 are designed much smaller than those of INV_1 and other transistors of M1, M2, and $DFF_1 \sim DFF_3$.

To explain the operation of the proposed duty cycle trimming circuit, we derived the truth table of this duty cycle trimming circuit as shown in Fig. 2 (a). First, let's assume $CLK_{IN}=0$ and X=0. When $CLK_{IN}=0$, M1 is turned off and M2 can be turned on. But X=0 makes the turn-on resistance of M2 very high and the cross-coupled inverters hold their values at Y and CLK_{OUT}. Second, let's assume $CLK_{IN}=0$ and X=1. Now M2 is turned on with the low turn-on resistance and Y equals X regardless of its previous value, i.e. Y=X=1. It is because the transistor sizes of INV_2 are designed much smaller than those of DFF_3. So, $CLK_{OUT}=0$. Third, let's assume
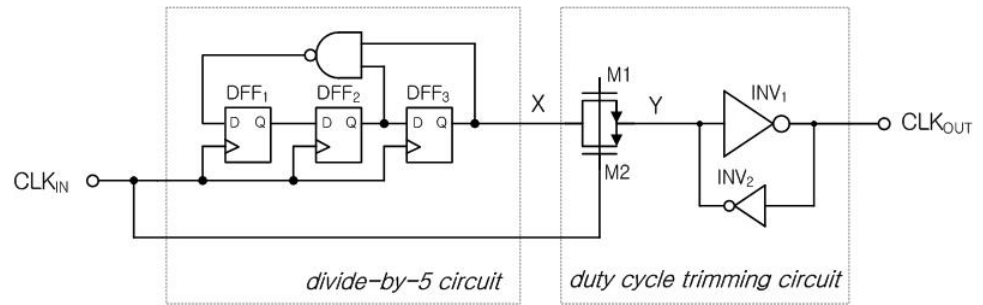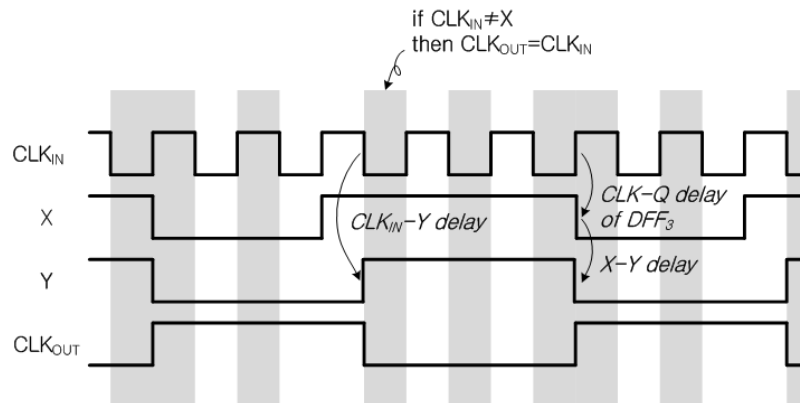
Fig. 1. Divide-by-5 circuit with the proposed duty cycle trimming circuit


(a)

(b)

Fig. 2. (a) Truth table and (b) timing diagram of the proposed duty cycle trimming circuit

$CLK_{IN}=1$ and $X=0$. In this case, M2 is turned off, M1 is turned on with the low turn-on resistance and Y becomes X, i.e. $Y=X=0$, due to the same reason as the second case. So, $CLK_{OUT}=1$. Finally, let's assume $CLK_{IN}=1$ and $X=1$. Because $CLK_{IN}=1$, M2 is turned off and M1 can be turned on. However, $X=1$ makes the turn-on resistance of M1 very high and the cross-coupled inverters hold their values at Y and CLK_{OUT}. By summarizing the above discussion, the truth table of Fig. 2 (a) is obtained. Looking carefully this truth table, we can simply say that "if $CLK_{IN} \neq X$ then $CLK_{OUT}=CLK_{IN}$".

Based on the obtained truth table, the timing diagram of the proposed duty cycle trimming circuit is drawn as shown in Fig. 2 (b). In this timing diagram, X is the divided-by-5 clock signal, of which duty cycle is not 50% but
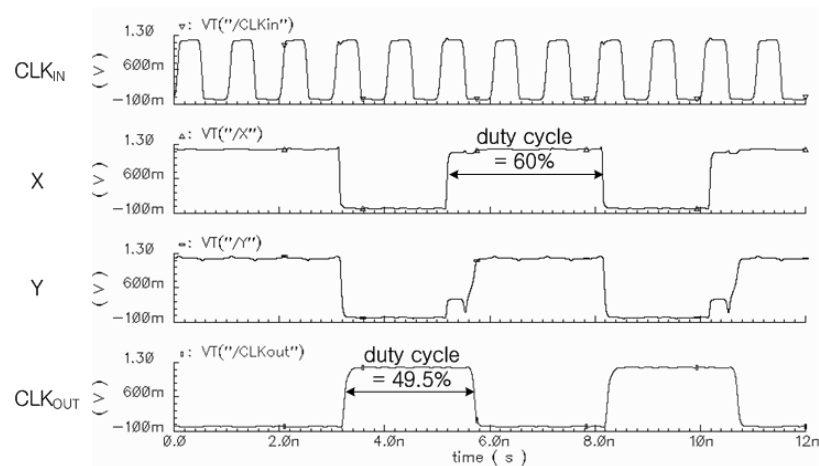
(a)
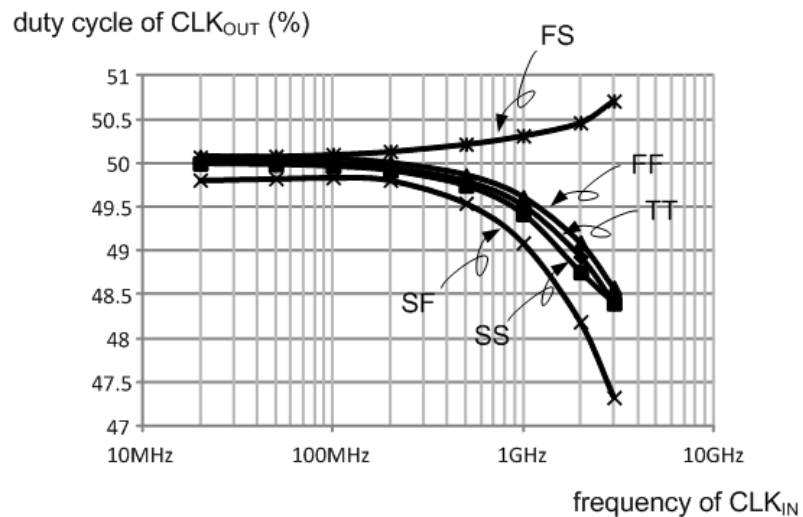
(b)

Fig. 3. (a) Simulated waveforms of the proposed duty cycle trimming circuit and (b) frequency response of the corrected duty cycle of CLK_{OUT}

60%. After duty cycle trimming, the duty cycles of Y and CLK_{OUT} are corrected as shown in Fig. 2 (b). Because the rising edge of Y is triggered by the falling edge of CLK_{IN} and the falling edge of Y is triggered by the falling edge of X which is triggered by the rising edge of CLK_{IN}, the duty cycles of Y and CLK_{OUT} are affected by the duty cycle of CLK_{IN}, CLK_{IN}-Y delay, X-Y delay and CLK-Q delay of DFF_3 as shown in Fig. 2 (b). Let's consider those effects carefully. First, the duty cycle of CLK_{IN} is directly related to the duty cycle of CLK_{OUT}. If the input duty cycle error of CLK_{IN} is 10%, then the corrected output duty cycle of CLK_{OUT} will be 10%/N, where N is the division ratio of the odd number frequency divider. Fortunately, CLK_{IN} comes directly from the integrated voltage controlled oscillator (VCO) and has almost 50% duty cycle in general. Second, CLK_{IN}-Y delay and X-Y delay can be matched by properly choosing the sizes of M1 and M2 to have the same equivalent turn-on

resistance. But small mismatch may exist between CLK_{IN}-Y delay and X-Y delay depending on the process variation. The transistor sizes of M1 and M2 were $(W/L)_{M1}=0.5\,\mu m/0.13\,\mu m$ and $(W/L)_{M2}=1\,\mu m/0.13\,\mu m$, respectively. Finally, CLK-Q delay of DFF_3 may limit the accuracy of the duty cycle of CLK_{OUT}. However, it is relatively small for low frequency operation and starts to show up as the CLK_{IN} frequency increases. To compensate the CLK-Q delay of DFF_3 for high speed operation, an appropriate buffer can be inserted to CLK_{IN} before CLK_{IN} drives the gates of M1 and M2. This CLK-Q delay of DFF_3 depends on the process variations. Although the timing diagram of Fig. 2 (b) shows the case of a divide-by-5 circuit, any odd number frequency divider can be incorporated with the proposed duty cycle trimming circuit for 50% duty cycle.

3 Simulation results and conclusion

The divide-by-5 circuit and the proposed duty cycle trimming circuit were designed for a 500-Mb/s $\sim$ 5.6-Gb/s 1:10 CDR/DEMUX IC in a $0.13\,\mu m$ 1P8M CMOS process. Fig. 3 (a) shows the simulated waveforms of CLK_{IN}, X, Y and CLK_{OUT} of the proposed duty cycle trimming circuit. The simulated waveforms agree well with the timing diagram shown in Fig. 2 (b). The small ripple on the waveform of Y is generated when CLK_{IN}=X=1 and Y=0 because of the high but not infinite turn-on resistance of M1. This ripple can be reduced by designing INV_2 with a bit larger transistors. Due to the proposed duty cycle trimming circuit, the output duty cycle of CLK_{OUT} is corrected from 60% to 49.5% when the input clock frequency of 1 GHz is applied to the proposed divide-by-5 circuit. Fig. 3 (b) shows the frequency responses of the corrected duty cycle of the divide-by-5 circuit and the duty cycle trimming circuit for the process variations, TT, FF, SS, FS and SF. The duty cycle of CLK_{OUT} deviates from 50% as the operating frequency increases. The duty cycle of CLK_{OUT} is within 2.7% from 50% over the frequency range from 20 MHz to 3 GHz, which satisfies the required clock frequency range, i.e. 250 MHz $\sim$ 2.8 GHz, for the 500-Mb/s $\sim$ 5.6-Gb/s 1:10 CDR/DEMUX IC with a half rate phase detector. The maximum frequency range is limited not by the duty cycle trimming circuit but by the divide-by-5 circuit, because the D-Q delay of DFFs and the propagation delay of the NAND gate limit the maximum operating speed of the frequency divider.

In conclusion, the proposed duty cycle trimming circuit provides 50% duty cycle for full swing odd number frequency dividers at the cost of only additional six transistors.

Acknowledgments