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# A high resolution and high linearity 45 nm CMOS fully digital voltage sensor for low power applications

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**Abstract:** This paper proposes a design of voltage sensor with new controllable delay element (CDE) having high linearity and high resolution. The proposed CDE uses power supply node to measure the voltage value. However, the delay increases exponentially at low voltage level. In this paper we add a PMOS header in parallel with the conventional CDE to compensate the delay degradation at lower voltage. We develop a 16-levels fully digital voltage sensor with a voltage range of 0.8 $\sim$ 1.1 V and 20 mV resolution by using of the proposed delay elements. The proposed circuit is designed and simulated in a 45 nm CMOS process. The simulation results show the feasibility of the high resolution and high linearity at low voltage by using of the proposed delay elements.

**Keywords:** voltage sensor, digital, delay element, low voltage, high resolution, high linearity

**Classification:** Integrated circuits

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## 1 Introduction

As the CMOS technologies reach the deep sub-micron regime, integrated circuits (ICs) encounter scaling impediments such that reducing power dissipation is the biggest roadblock in the design of digital circuits. The high demand for mobile devices is also requiring designers to lower the operating voltage level to reduce the dynamic power which is quadratic dependency with voltage [1].

Increasing chip density and more aggressive scaling affect how a chip responds to parameters such as process corners, voltage, and temperature (PVT) [2]. Thus, more accurate understanding of these parameters can provide circuit designers with insight into how to improve the chip behavior.

A controllable delay element (CDE) is a circuit that produces a delayed output waveform which is similar to its input in the form of controlled current or voltage values. The CDEs have many applications in VLSI or analog circuits. They can be used in digital delay locked loops (DLLs) [4], phase locked loops (PLLs) [5], digitally controlled oscillators (DCOs) [6], microprocessor [7], memory circuits [8], and sensor applications [9]. Moreover, as the supply voltage is scaled down below 1 V for reducing power consumption, voltage variation has become one of the major sources of uncertainty as shown in Fig. 1 [3], which makes sensing the voltage fluctuation at low voltage accurately highly important. In order to measure the voltage variations

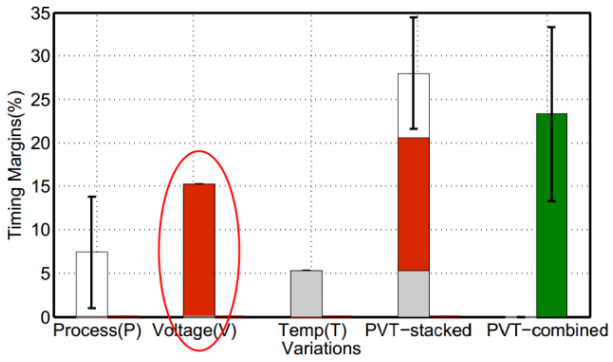


**Fig. 1.** Impact of PVT variations on timing margins [3].


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precisely, the resolution of the sensor must be high. Besides, high linearity in the main delay element of the voltage sensor is required for ease of design and high accuracy.

In 45 nm designs, the supply voltage can be below 1 V to reduce dynamic power consumption. A traditional dynamic voltage scaling (DVS) technique requires voltage to change dynamically within the range of half of the nominal voltage [10]. Even though we can reduce the dynamic power, the delay increases significantly at lower voltage. Therefore, we require new design methodology in the CDE to compensate the delay degradation at low voltage. In this paper, a design of 16-levels digital voltage sensor for lower voltage applications with high resolution and high linearity is presented by employing new CDE.

## 2 The controllable delay element (CDE)

One of the popular approaches to implement a delay cell is to use current-starved inverters [11] shown in Fig. 2-a. The mechanism for controlling the delay of each inverter is to limit the current available to discharge the load capacitance of the gate by adding an extra series NMOS device under the NMOS of the inverter. The added NMOS transistor is controlled by a control voltage at the gate terminal which determines the available discharge current. However, this approach has a drawback of a nonlinear relationship between control voltage and propagation delay. Another approach to implement a delay cell is to use power supply controlled inverter [12] as shown in Fig. 2-b. Propagation delay of an inverter are shown in the Eq. (1) and (2). As can be seen from the following equations, the delay of an inverter is a strong function of its supply voltage (i.e., $V_{DD}$).

$$\begin{aligned} &t_{p(\text{HL or LH})} = 0.69 R_{eq(\text{n or p})} C_L \\ &\text{with } R_{eq(\text{n or p})} = \frac{3}{4} \frac{V_{DD}}{I_{DSAT(\text{n or p})}} \left(1 - \frac{7}{9} \lambda V_{DD}\right) \end{aligned} \tag{1}$$

$$I_{DSAT(\text{n or p})} = k' \frac{W}{L} \left( (V_{DD} - V_{th}) V_{DSAT} - \frac{V_{DSAT}^2}{2} \right) \tag{2}$$

Therefore, the delay of the input pulse signal is a function of $V_{in}$ and, in other words, determined according to the value of $V_{in}$ in Fig. 2-b. With the idea mentioned above, the control voltage $V_{in}$ is used as the supply voltage of the inverter in order to control the delay as designers want. But this approach suffers from the same drawback - nonlinearity. The delay of the supply voltage controlled inverter has considerable nonlinearity with the input voltage as shown in Fig. 3-b. At low voltage level, the low-to-high propagation delay ($t_{pLH}$) degrades significantly in the supply voltage controlled inverter because as the supply voltage approaches $V_{th}$, the $I_{DSAT}$ decreases rapidly, hence $R_{eq}$ dramatically increases as shown in Eq. (1) and (2). In order to reduce the degree of nonlinearity of delay elements, the architecture shown in Fig. 2-c is proposed [13]. An ordinary inverter is placed above in parallel with the conventional power supply controlled inverter. The additional


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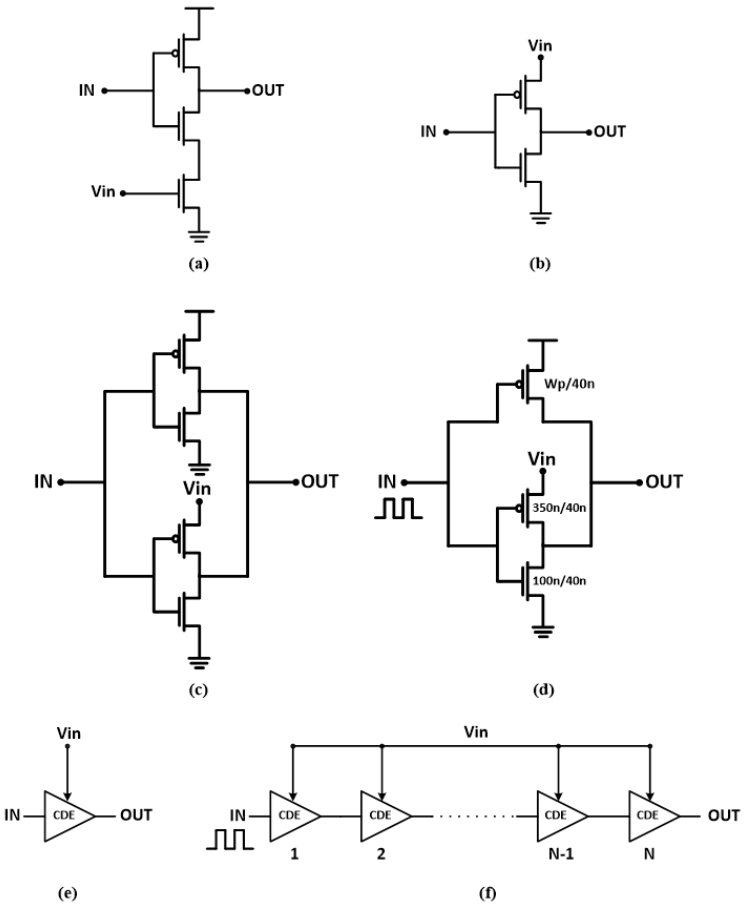


**Fig. 2.** Controllable delay element (CDE): schematic of current-starved inverter (a), supply voltage controlled inverter (b), modified supply voltage controlled inverter (c) and proposed CDE (d). The symbol of CDE (e) and a chain of N delay elements (f).

normal inverter can help the $t_{pLH}$ transition. Therefore, the linearity can be achieved in the overall voltage range.

However, the biggest drawback of the design Fig. 2-c is the area overhead due to the additional parallel inverter in the CDE. Therefore, in this paper, we propose a new CDE in which only a small PMOS is inserted in parallel with the supply voltage controlled inverter to maintain the linearity at the lower voltage. A simulation indicates that a carefully sized single PMOS is good enough to compensate the delay degradation. The measuring voltage is attached to the power supply node of the pull-up devices of the inverter and it affects mainly the low-to-high transition. Therefore, the parallel compensating PMOS can help the low-to-high transition at the lower voltage level. By adding a single PMOS we can achieve two main advantages; at first, the overall area overhead reduces compare to the Fig. 2-c. Second, the diffusion capacitance at the output becomes smaller and speed becomes faster.

For the proposed CDE as shown in the Fig. 2-d, we conduct timing simulations to obtain the optimum size of the additional PMOS. The plot of the


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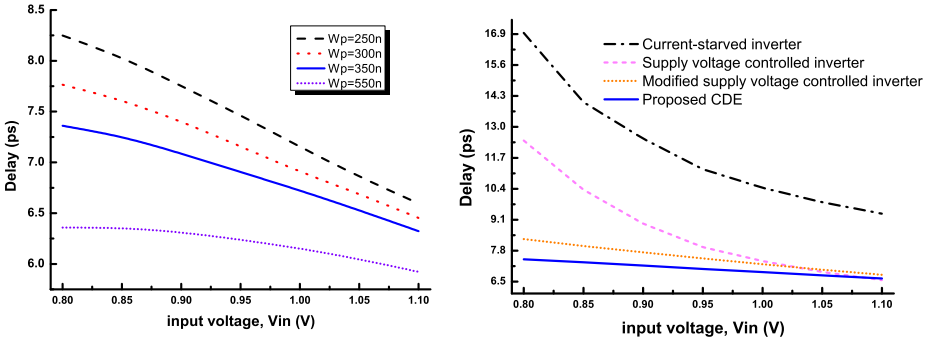


(a) (b)

**Fig. 3.** (a) The delay sensitivity to input voltage for various PMOS size in the proposed CDE (i.e., Fig. 2-d) and (b) the linearity comparison of various CDEs.

delay sensitivity to the input voltage for various PMOS width is shown in the Fig. 3-a. As shown in the figure, there is a significant delay impact when PMOS size get reduced. Therefore, we chose $W_p = 350\,\text{nm}$ for our voltage sensor to minimize the delay impact with good linearity at low voltage. The delay vs. input voltage ($V_{in}$) values of the four CDE cases mentioned above are shown in Fig. 3-b. As can be seen, the delay increases remarkably at the voltage below 1 V in the conventional inverter CDEs. But the proposed CDE which is in solid blue line shows high linear delay with respect to the entire voltage value.

In this paper, a novel controllable delay element architecture, which has both high linearity and smaller counts of transistor, is proposed as shown in Fig. 2-d. The proposed controllable delay inverter consists of an ordinary inverter and a single PMOS in parallel. Hence, in this schematic, the delay is controlled by the delay of both the ordinary inverter and the additional PMOS. Each of the delay elements is composed of two inverter proposed, becoming a buffer. Based on the amount of delay required, the number of stages of controllable delay buffer can be determined. The rising edge of the pulse travels through the delay element with a certain amount of delay, while the control signal comes at the source terminal of the PMOS transistor in the inverter. Each of CDE enables that the rising edge of pulse takes some time to reach the last CDE. The measured sensitivity of the proposed CDE is approximately $\Delta t_p/\Delta V_{in} \approx 53.6$ ps/V. It is well known that the correlation coefficient is widely used as a measure of the strength of linear dependence between two variables. The correlation coefficients (R) are obtained for the four curves in Fig. 3-b. In the case of current-starved inverter, $R = -0.95175$, for supply voltage controlled inverter, $R = -0.95135$ and $R = -0.99875$ for modified supply voltage controlled inverter while for the case of the proposed CDE, $R = -0.9999$. The operation of the proposed CDE is described as follows:

The nominal supply voltage ($V_{DD}$) of the proposed CDE is 1.1 V in a 45 nm process. The clock signal comes at the gates of inverter and the gate


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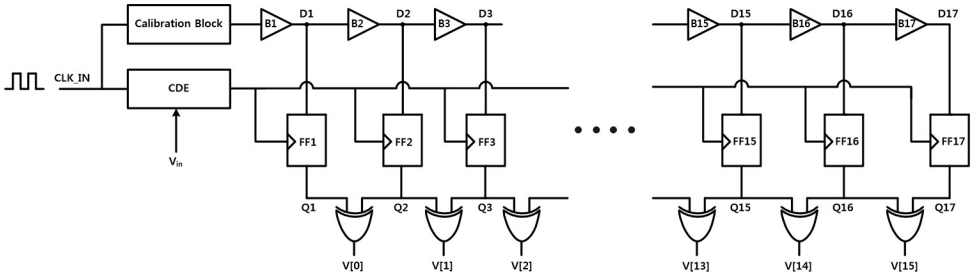


**Fig. 4.** A schematic of the proposed voltage sensor.

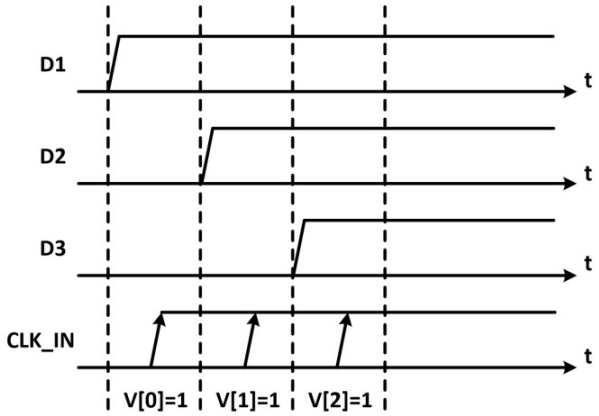


**Fig. 5.** Operating principle of the proposed voltage sensor.

of PMOS in parallel, while the source terminal of the PMOS in the inverter tied to control voltage ($V_{in}$) within the range of 0.8 $\sim$ 1.1 V. According to the Eq. (1), the input clock signal propagation delay of the CDE can be controlled by $V_{in}$. And the additional compensating PMOS can help the low-to-high transition at lower voltage levels. The amount of the delay for each voltage level is set by increasing the number of stages of CDEs.

## 3 Operation principle of the proposed voltage sensor

The proposed voltage sensor, shown in Fig. 4, consists of a series of CDEs, a calibration block, positive-edge trigger flip-flops, delay buffer stages, and XOR gates. The operating principle of the proposed voltage sensor is described as follows:

Fig. 5 presents the operating principle of our design. Once the clock signal passes through the calibration block, the clock signal is delayed a certain amount of time by the delay buffers to create the lag between consecutive D signals of the positive-edge flip-flops. At the same time, the propagation delay of the clock through the CDE is controlled by the CDE. The rising edge of the clock is shifted into the gap between two adjacent D signals of the flip-flops. The shifting delay of the rising edge of the clock is determined according to the value of $V_{in}$. The buffer stages (B1 $\sim$ B16) are inserted and the number of buffer stages is carefully determined to provide exact delay gap between adjacent FFs. The delay interval between two adjacent D signals is


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chosen to be two times of setup time of flip-flops to provide enough process variation margin of the design. The signal controlled by CDE will occur in the middle of the interval. If D input of a flip-flop (FF) comes early before (setup time) the clock signal (CLK_IN), the D data can be transferred through the flip-flops.

The time gap between the clock signals is fixed according to the input voltage value after implementing the CDE. The size of buffer stages is fixed and the number of buffer stages determines the arrival time of D inputs. At the Q outputs of the FFs, XOR gates are employed to detect the difference between two adjacent Q outputs. The calibration block is a chain of buffer stages to calibrate and synchronize the clock rising edge between output of the CDE and the calibration block. There is only one output XOR gate that will have a high value to indicate the specific input voltage value at any time of operation. Finally, according to the value of XOR gates, the voltage value which is attached to the terminal of $V_{in}$ can be known in digital form.

## 4 Simulation results

In order to validate the circuit operation with the proposed CDE, we conducted simulations by creating a schematic of the proposed designs in a device-level simulation tool [15], using a commercial 45 nm CMOS process.

Usually, non-ideal effects increase the difference from the ideal values of analog-to-digital converters (ADC). The difference between the ideal and non-ideal values can be explained in the differential nonlinearity (DNL) value [14]. The DNL for the entire voltage sensor used in this paper is from $-0.35$ LSB to $-0.2$ LSB, with 1 LSB = 20 mV that represents the value of resolution. In addition, corner simulations should be presented to confirm the robustness of the circuit against process variations. Together with typical corner, fast and slow corner simulations are conducted. The control voltage ($V_{in}$) changes from 0.8 V to 1.1 V with 20 mV increments. The transfer curves of the voltage sensor for various process corners are shown in Fig. 6. As shown in the figure, our design is working properly at a typical process condition because the delay of CDEs are designed based on the typical corner. However, there is overestimation and underestimation at the lower input voltage (i.e., $V_{in} \leq 1.0$ V) by the fast corner and the slow corder, respectively. These errors can be reduced by increasing the delay margin between FFs in the voltage sensor.

As shown in Fig. 7, the sinusoidal waveform is used as an input signal to validate the circuit operation in the dynamic voltage change. If the voltage variation is applied to the $V_{in}$ terminal, the proposed voltage sensor produces the corresponding digital outputs according to applied voltage variation. As expected, only one of XOR gates outputs gets high value at any time. According to the simulation results, the operation of voltage sensor is verified in accordance with the theoretical analysis presented in previous sections.


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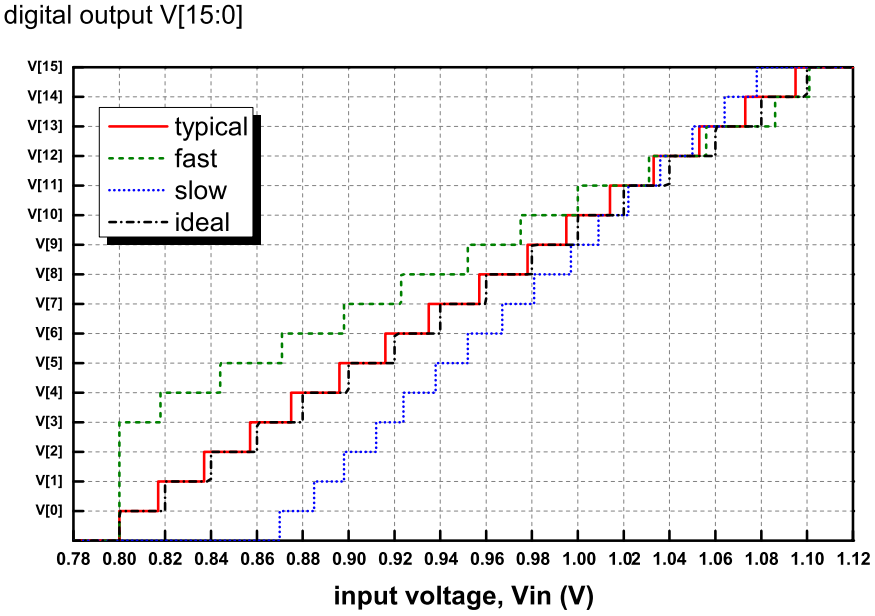


**Fig. 6.** Transfer curve of corner simulations in the range of control voltage ($V_{in}$).

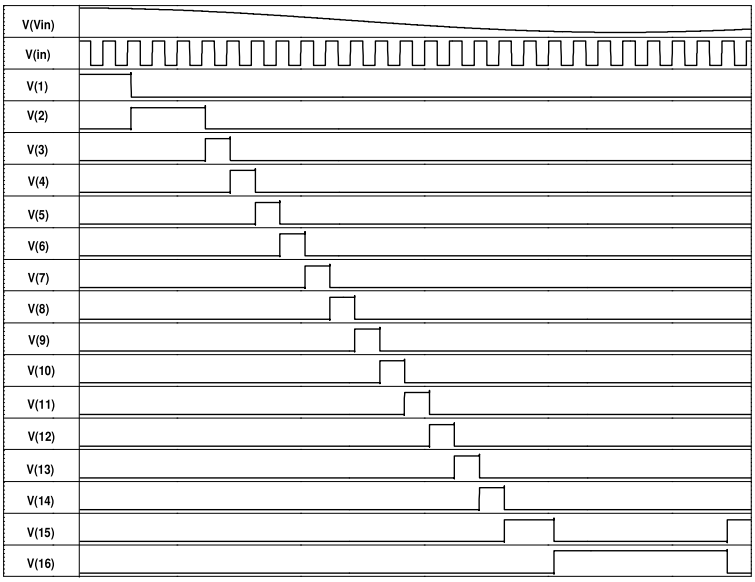


**Fig. 7.** Simulation results of $V_{in}$ (sinusoidal input of 0.8 V to 1.1 V) and digital outputs: 16-levels output V[0] ∼ V [15].

## 5 Conclusions

In this paper we propose a new architecture for controllable delay element (CDE). The proposed CDE, which has high resolution (20 mV), high linearity, and relatively small footprint, is compared with other architectures. The proposed CDE is used as a main element to implement a fully digital voltage sensor for low power applications in 45 nm CMOS. The simulation results show that the proposed voltage sensor can be used to monitor a wide voltage range (i.e., up to below 300 mV of the nominal voltage) with high resolution.


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