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LETTER

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Trapezoidal approximation for on-current modeling of 45-nm non-rectilinear gate shape

Myunghwan Ryu and Youngmin Kim[a)]

UNIST, Ulsan, Republic of Korea

a) *youngmin@unist.ac.kr*

Abstract: In this paper, a simple and accurate modeling technique that analyzes a non-rectilinear gate (NRG) transistor with a simplified trapezoidal approximation method is proposed. To approximate a non-rectangular channel shape into a trapezoidal shape, we extract three geometry-dependent parameters from post-lithographic patterns: the minimum channel length from the slices (L_{min}), maximum channel length from the slices (L_{max}), and effective channel width (W_{eff}). We slice the NRG transistor gate along its width, sort these slices according to their sizes, and then use trapezoidal approximation. A physics-based technology computer aided design (TCAD) simulation is used to verify our model in a typical 45-nm process. The developed model requires fewer computations and less runtime as compared to the previous approaches. Therefore, a full chip post-lithography analysis (PLA) becomes feasible.

Keywords: NRG, effective length, effective width, post-lithography simulation, TCAD

Classification: Electron devices, circuits, and systems

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1 Introduction

As the scale of semiconductor devices has decreased to the sub-wavelength regime, the imperfect shape of gate patterning caused by process variation has increased significantly. Because of the slow evolution of the photolithography technology, it is too difficult to obtain perfectly rectangular lithographic patterns. Therefore, line-edge roughness (LER) (Fig. 1) occurs in the order of several nanometers and does not decrease as the device shrinks. This has evolved into a critical problem in nanometer regimes [2]. This problem leads to serious device parameter fluctuations and makes circuit analysis difficult. Because of the LER effect, the discrepancies in the analysis of device performance caused by the non-rectilinear gate (NRG) effect have worsened with rapid CMOS technology scaling.

Furthermore, in circuit analysis, a substantial discrepancy is observed between the results of post-lithography simulations and the results of circuit simulations, leading to significant impacts on timing and power analysis [3]. The operation of a device with an NRG can be predicted by TCAD simulations; however, a circuit-level simulation involving a large number of transistors is very time consuming. Thus, it is important to not only capture the effect of an NRG with sufficient accuracy but also incorporate the effects into standard circuit simulation tools such as SPICE with a reasonable simulation time.

Thus far, several post-lithographic simulation (PLS) techniques that can handle NRG transistors have been proposed [3, 4, 5, 6, 7]. Most of these techniques are based on a gate slicing method and an equivalent gate length (EGL) method, which use the summation of I_{on} and I_{off} in each slice after uniformly partitioning a given device channel into small slices. The gate slicing method is used to compute the current of the NRG devices, and the EGL method maps the computed on or off current to an equivalent device suitable for on or off state simulations [4]. The NRG channel region is divided uniformly along the width of the device, and then, the summation of each device slice is carried out to obtain the same current.

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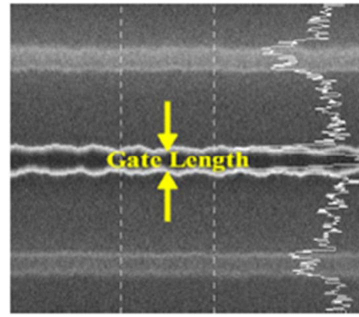

Fig. 1. SEM image of line-edge roughness at 65 nm process, Intel [1]

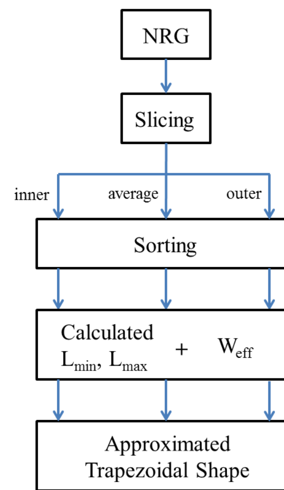

Fig. 2. Procedure to approximate NRG transistor into trapezoidal shape.

The on-off characteristics of the devices are modeled through these approaches, which can analyze the electrical characteristics caused by the imperfect gate shape of transistors and show good agreement with SPICE results. However, modeling using these approaches is not only cumbersome but also requires a large amount of resources (i.e., many mathematical calculations and a long runtime).

In this paper, we propose a technique for simple and accurate modeling that analyzes an NRG transistor with a simplified trapezoidal approximation method. The procedure of the trapezoidal approximation method is shown in Fig. 2. On the basis of our model, three geometry-dependent parameters (L_{min}, L_{max}, W_{eff}) from post-lithographic patterns are extracted in three different cases: inner, outer, and average approximations. The scanning electron microscope (SEM) images of the practical channel region of the metal-oxide-semiconductor (MOS) transistor that is distorted from the designed rectangular shape and one of the slices after slicing the channel region are shown in Fig. 3 and Fig. 4, respectively. To validate the trapezoidal approximation, we intentionally introduce irregularities in the length of the channel along the width of the channel. We analyze an NRG by slicing uniformly along the width of the channel, depending on the length of the slices,

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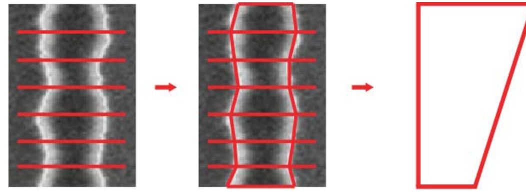

Fig. 3. SEM image of a gate with LER with slicing and the final trapezoidal approximation.

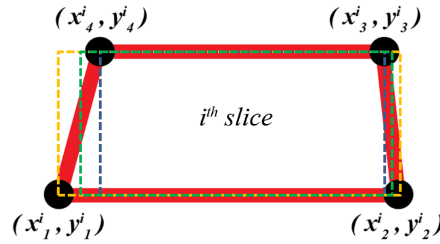

Fig. 4. Blue line: inner approximation, green line: average approximation, and yellow line: outer approximation. Note, we use the average approximation method in this study.

and then, the slices are sorted according to their sizes by the simple modeling method of trapezoidal approximation. This method is used to approximate an NRG into a trapezoidal shape with the length of the biggest slice (L_{max}) and the length of the smallest slice (L_{min}) to obtain the same electrical characteristics (I_{on}) of the transistors compared to the original NRG.

$$\begin{cases} L^i_{inner} = |\min(x^i_2, x^i_3) - \max(x^i_1, x^i_4)| \\ L^i_{outer} = |\max(x^i_2, x^i_3) - \min(x^i_1, x^i_4)| \end{cases}$$

where $1 \leq i \leq n$; $n = \#$ of slices, x^i_n in Fig. 4

1) average approximation

$$\begin{cases} L_{\min} = \min(\frac{L^1_{inner}+L^1_{outer}}{2}, \cdots, \frac{L^i_{inner}+L^i_{outer}}{2}, \cdots, \frac{L^n_{inner}+L^n_{outer}}{2}) \\ L_{\max} = \max(\frac{L^1_{inner}+L^1_{outer}}{2}, \cdots, \frac{L^i_{inner}+L^i_{outer}}{2}, \cdots, \frac{L^n_{inner}+L^n_{outer}}{2}) \end{cases}$$

The advantage of the proposed trapezoidal approximation models is to obtain accurate on-currents for various NRG devices with simple calculations without TCAD simulations and slicing methodology used in [3, 4, 5]. The accuracy and simplicity come from the consideration of edge effect by W_{eff} and the use of only three geometry parameters to obtain the on-current of transistors, respectively.

2 Trapezoidal approximation model

Assuming that the NRG has a hexagonal shape, modeling with the trapezoidal approximation is proposed. As shown in Figs. 5 (a) and (b), each shape has two points near the center, and the shapes are two representative examples (in the case of HDL > 0, HDL < 0, respectively, where HDL is the half

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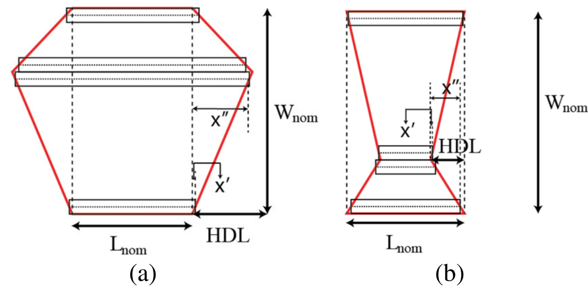

Fig. 5. Two representative non-rectangular transistors in the channel region: (a) HDL > 0, (b) HDL< 0.

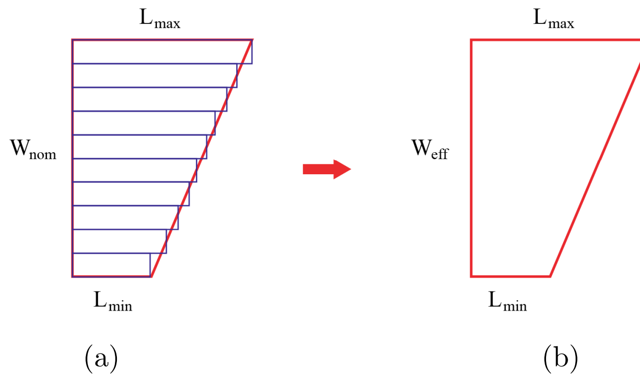

Fig. 6. Approximated equivalent trapezoidal channel; (a) trapezoidal shape after sorting according to size, (b) trapezoidal shape with effective width.

delta length; variation of the gate shape at one side) of various hexagonal shapes. Once the coordinates of any LER shape are given, we can extract L_{min} and L_{max} on the basis of the inner, outer, and average approximations, as shown below. In this study, the average approximation is used to obtain L_{min} and L_{max} since its result provides the minimum error with the original pattern compared to inner or outer approximations. The extracted L_{min} and L_{max} from our model can be used to approximate the fictitious NRG shape into a trapezoidal shape.

Fig. 6 (a) shows an array of slices in the descending order of size, forming an approximated trapezoidal shape by connections between the upper right point in the largest slice and the lower right point in the smallest slice, and Fig. 6 (b) shows the approximated trapezoidal shape with effective width W_{eff}. This figure shows the approximated shape as a trapezoid that has a length of the top aspect of L_{max} and a length of the bottom aspect of L_{min} as calculated by the equation proposed above.

It is known that threshold voltage (V_{Th}) and the current characteristics are different along the channel, which is the so-called "edge effect"— a type of inverse narrow width effect [8, 9, 10, 11, 12]. There are several factors causing the device threshold voltage to be non-uniform along the channel width, such as fringing capacitance due to line-end extension [10], dopant scattering due to shallow trench isolation (STI) edges [10], and the well proximity effect

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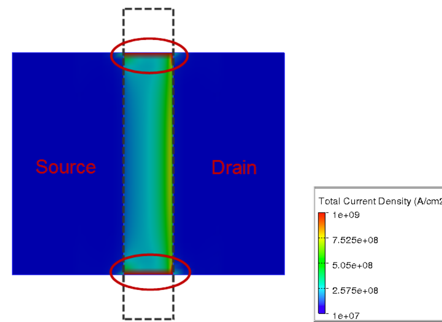

Fig. 7. TCAD simulation showing edge effects; note that there is a much higher current density in the edge region than in the center.

(WPE) [13, 14], which are pronounced near the device edges and roll off sharply towards the center of the device [5].

In this paper, in order to consider the edge effects by the effective channel length, a weighting factor (effective width W_{eff}) is introduced. The current density profile over a metal-oxide-semiconductor field-effect transistor (MOSFET) device obtained in our simulation is shown in Fig. 7. As shown in this figure, the current density in the edge region is higher than that in the center region of the channel. When only two parameters are used, i.e., L_{min} and L_{max}, there are still significant discrepancies between the original shape and the trapezoidal approximated shape. This is mainly because the simple trapezoidal shape doesn't distinguish between the slices from the center and from the edge. We extract L_{min} and L_{max} in a simple NRG channel that has a hexagonal shape. In addition, in order to reduce the approximation errors in the trapezoidal method, we extract W_{eff} by curve-fitting from the TCAD simulation results of the various NRG structures with sweeping of HDL amount and locations of the maximum variation. The fitting is just one time procedure, therefore, for different technology process, simple TCAD extractions are enough to derive W_{eff} for various channel length at the edge and center. The equivalent trapezoidal shape is verified by TCAD to compare I_{on} of the original transistors.

3 TCAD setup & model verification

I_D versus V_{DS} data based on a published 45-nm SPICE model [15] is used to calibrate parameters for the TCAD simulation. To verify the accuracy of our model, a 3D TCAD simulation tool, Silvaco Atlas [16], is used. The parameters used in the TCAD simulation are shown in Table I.

The representative fictitious NRG transistor structure created by TCAD is shown in Fig. 8 (a), and the approximated trapezoidal structure calculated by the proposed modeling method is shown in Fig. 8 (b). To generate simple and representative LER shapes, we sweep both the channel length variation (i.e., HDL from −10 to +10) and the location of the variation in the device width direction with a step of 10 nm. A comparison of I_{on} between the NRG transistor and the approximated trapezoidal transistor by the proposed model

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Table I. 45 nm TCAD model parameters

Parameters	Value
Channel length (nominal)	45 nm
Channel width (nominal)	0.2 um
V_{DD}	1.0 V
T_{ox}	1.5 nm
Channel doping	3.92e+18 cm^{-3}
N_{SUB}	1e+15 cm^{-3}
Junction depth	20 nm
S/D region to gate poly	0.04 um
STI width	0.1 um
STI depth	0.3 um

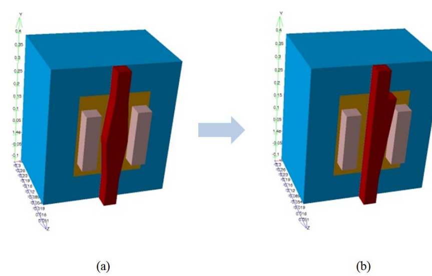

Fig. 8. 3D TCAD structures for model verification: (a) hexagonal shape, and (b) approximated trapezoidal shape.

at HDL = −10 nm and +7 nm is shown in Figs. 9 (a) and (b), respectively.

The model accuracy is verified for 40 transistor samples, and the error distributions for both the case of the simulated NRG transistor without W_{eff} and the proposed model with W_{eff} are shown in Fig. 10. The vacant black squares show the results when the trapezoidal approximations are followed by L_{min} and L_{max}. On the other hand, the red dots show the results when the NRG transistors are approximated by L_{min}, L_{max}, and W_{eff}, thus considering the edge effect. As shown in this figure, the error distribution decreases significantly in the case with W_{eff} compared to that without W_{eff}. Without the weighting factor (W_{eff}), the absolute average error is 3.67%; however, this decreases to 0.31% after applying the width weighting factor. As a result of the introduction of the effective width, the model accuracy is improved by 92% as compared to the case without the effective width.

4 Case study

The developed model is applied to the realistic NRG shapes generated from post-lithography simulations of NOR and NAND gates. The post-lithography data are acquired from Mentor Graphics Calibre Workbench [17] simulations, and Fig. 11 shows the post-lithography images of NOR3 and NAND3 gates. The polygon coordinates of the NRG shapes are obtained in the marked re-

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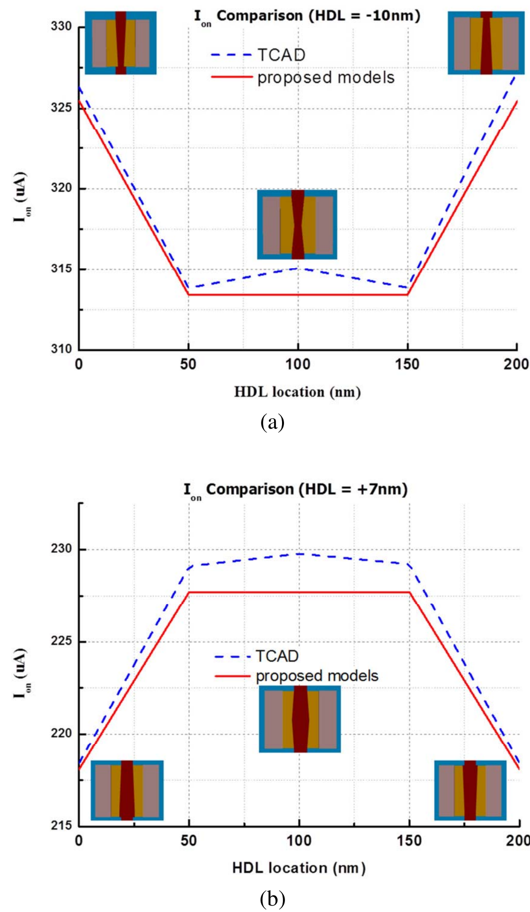

Fig. 9. Comparison of on-current: (a) in the case of HDL $= -10$ and (b) HDL $= +7$ m, where HDL location is the channel length variation point

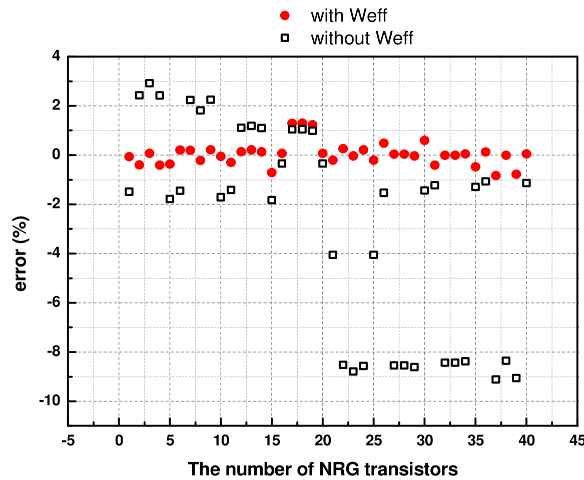

Fig. 10. I_{on} modeling error distribution.

gions. As mentioned in section 2, after the coordinates of the NRG shapes are acquired from the post-lithography images, the two parameters L_{min} and L_{max} are extracted as coarse tuning parameters, and the effective width parameter W_{eff} is applied as an additional fine-tuning parameter to our model. The weighting factor for the edge or center is selected depending on the dom-

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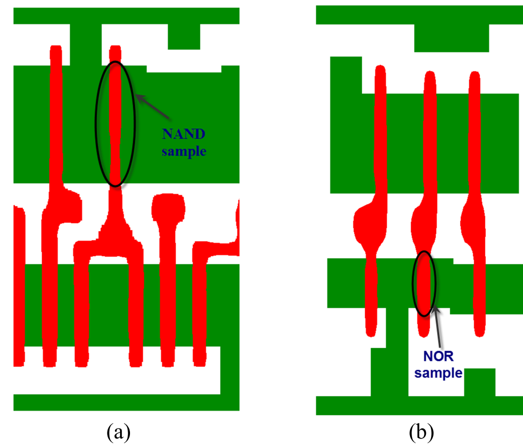

Fig. 11. Post-lithography images of (a) NAND3 and (b) NOR3

Table II. I_{on} comparison between TCAD results and the proposed models for logic gates.

Test cells	Lithography TCAD		Proposed models $I_{on}(\mu A)$		Absolute error (%)	
	I_{on} (μA)	runtime (s)	w/o weighting	w/ weighting	w/o weighting	w/ weighting
NOR3	288.9	779.7	286.7	287.8	0.76	0.36
NAND3	301.2	669.3	304.1	301.2	0.97	0.01

inant variation location along the channel width used to extract W_{eff}. The results of the TCAD simulations show sufficiently accurate agreement with the TCAD results whose three parameters are determined by the proposed trapezoidal approximation.

The simulation results and comparison errors are summarized in Table II. In the case of the on-state ($V_{DS} = V_{DD}$, $V_{GS} = V_{DD}$), the absolute errors of the developed model are only 0.76% and 0.97% for NOR and NAND cases, respectively. This result implies that the proposed model can be applied to an arbitrary imperfect shape with good accuracy, and the accuracy can be improved even more with a width-aware weighting factor. After applying the weighting factor, the absolute error is improved significantly (i.e., from 0.01% to less than 0.36%). This improvement in the model accuracy originates from the fact that the model with W_{eff} can capture the edge effect well and the results show the effectiveness of using the weighting factor in the approximation.

5 Conclusions and future works

We show that the I_{on} characteristics can be modeled by trapezoidal approximation with a simple and fast method using three parameters: L_{min}, L_{max}, and W_{eff}. The electrical characteristics of the LER gate are approximated by a trapezoidal shape, which is acquired by the length of the longest slice,

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the length of the smallest slice, and the weighting factor, instead of taking the summation of all the slices into account. The results of the TCAD simulation show that the proposed model is suitable for device simulation with edge effects, and its error for I_{on} is around 1% for various NRG transistors. For a more realistic application of the proposed model, we apply the model to NOR and NAND post-lithography images. The absolute errors of the model are 0.76% and 0.97% for the NOR and NAND cases, respectively. The accuracy can even be improved to be within less than 0.36% by adopting the width-location-dependent factor (W_{eff}). However, a relatively simple model limits the off-current approximation. Therefore, we are going to continue studying the compact shaping modeling method that can be applied to both I_{on} and I_{off} while retaining the fast speed of the PLS and the simplicity of modeling. Furthermore, we intend to study not only gate shape variation but also the diffusion of devices (e.g., source and drain side) together, which are expected to increase the edge effects and thus require precise modeling.

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