Ultra-wideband CMOS signal generators using tunable linear superposition

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Department of Electrical Engineering
(Analog, Digital and RF Circuit design)

Graduate school of UNIST

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Dong Uk Kim

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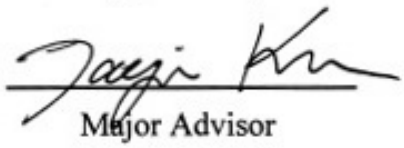

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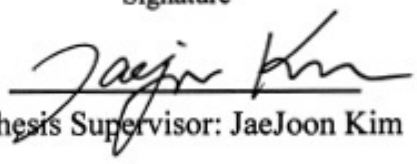

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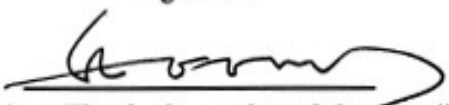

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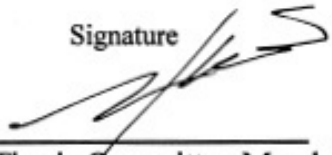

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Abstract

Wireless communication frequency bandwidth and center frequency are have been widening for high speed transmission of data. But the frequency bandwidth a transceiver can cover is severely limited. The circuit designed in the paper, called "signal generator", can offer a variety of wireless bandwidths. In this paper, a ultra wideband signal generator, based in 65nm CMOS technology, is designed after proposing and verifying two different types of signal generator design.

The first version design of the signal generator is proposed, which is composed of a four-stage LC-ring voltage-controlled oscillator (VCO) and a frequency synthesis circuit. A new concept of tunable linear superposition is proposed for wideband frequency synthesis and implemented to provide VCO core (1X)/ twofold (2X)/ quadruple (4X) programmable frequency multiplication function. In order to expand frequency coverage further, the LC-ring VCO adopted the tunable inductors which are composed of switchable bondwire pairs. A ultra-wideband operation from 4.3GHz to 27.4GHz was experimentally verified

The second version design of the signal generator using a reconfigurable phase selection process is proposed, which is proposed and consists of a multi-phase signal generation and a programmable frequency multiplication. This chip is proposed for wideband frequency synthesis and implemented to provide VCO core (1X)/ twofold (2X)/ quadruple (4X) and octuplet (8X) programmable frequency multiplication function. An LC-ring oscillator and a selective rectifying combiner are reconstructed adaptively for various frequency synthesis modes, minimizing their power consumption. A fully-integrated prototype verified to have very wide frequency characteristic from 6.3GHz to 59.4GHz.

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Nomenclature

PA	Power Amplifier
LNA	Low Noise Amplifier
VCO	Voltage Controlled Oscillator
ADC	Analog to Digital converter
DAC	Digital to Analog converter
Q	Quality factor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
DC	Direct current
AC	Alternating current
RF	Radio Frequency
NMOS	N-channel Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
PDK	Process Design Kit.

Chapter I

Introduction

With wireless communication technology developing and the needs increasing, a variety of frequency ranges for wireless communication have been used. Frequency ranges has been incrementally widening in the direction from Low frequency to High frequency and the wireless frequency device application fields are shown in fig 1.1. Among frequency bandwidths, the bandwidth ranges from the relatively low one, mobile cellular frequency bandwidth (800~2.3 GHz) to the relatively high one, automotive radar frequency bandwidth (76~77.5 GHz), which are almost every frequency bandwidth feasible in CMOS process, have been used. But the frequency bandwidths from the signal generator (for example, VCO) offering these ranges and from the mixer that can modulate and demodulate frequency signals don't cover all frequency bandwidths being currently used. This result causes a disadvantage that it requires a great number of transceiver chips, and so big areas and power consumption. Hence, in order to cover these problems, this paper presents a signal generator design method which offer the whole existing wireless frequency bands currently used. Chapter 1 gives a brief explanation on the signal generator (VCOs) now available and the motivation for the design method which the paper suggests. Chapter 2 shows, based on signal generator structure's (VCOs) operation principles, the circuit compensating the disadvantages of the present structure will be introduced. Chapter 3 shows experimental results and presents the feasibility of the new type signal generator. Chapter 4 involves a discussion of our future works. Finally, chapter 5 concludes this paper.

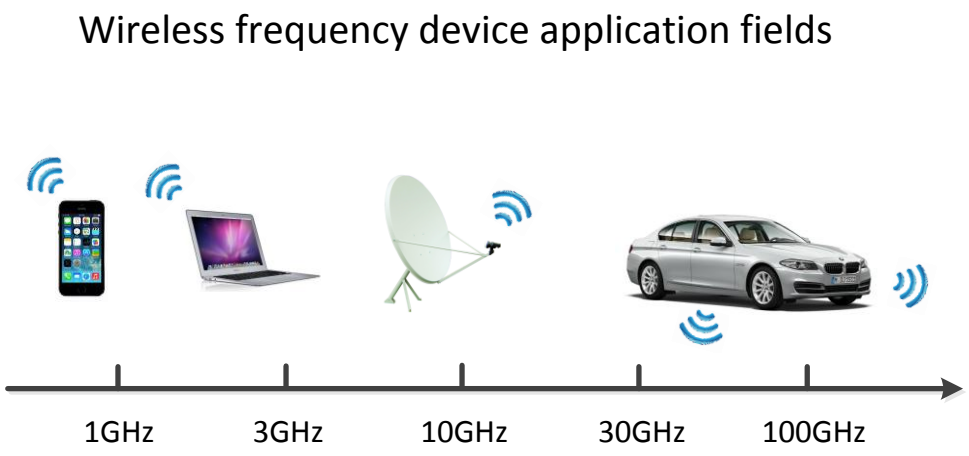


Figure 1.1. Wireless frequency device application fields

1.1 Signal generator develop motivation.

Against the backdrop of the releases of integrated chips supporting a variety of wireless communication standards, the most important work for supporting much larger variety of communication standards requires the technology of VCOs with a wide frequency band feature. In the same vein, recent researches have presented various efforts based on LC VCO. The Wideband VCO technology has been realized by controlling the capacitance value of LC tank inductors such as switched capacitor, switched inductor, and switched couple inductor, and so on [1-3]. The method of maximizing such characteristics designs a wide band VCO [4] using capacitance multiple structures with a switch and the combination of inductor switching and transformer inductor, but has a limitation that the device only deals with a band range below 5GHz. In the case of another structure that realizes a signal generator [5] to cover most low frequency band, designed through combining a divider and a multiplexer with VCOs using switched transformer inductor, it also realized low frequency band range below 10 GHz. The more communication standards using such high millimeter frequency band as 60GHz and 77GHz appear, the more researches using frequency multiplier [6] have followed recently. However, those researches are restricted to the possibility of realizing a technology, and thus lead to the relative lack of realization of wideband characteristic structures. In this paper, a wideband frequency signal generator is proposed acting as a kind of programmable wideband frequency multiplier. It consists of two-step operation, the first one is multi-phase signal generation, and the second one is programmable frequency signal generation. And frequency dividers are working well in the low frequency bandwidth. If we use a frequency divider as well, we can develop the signal generator which covers all currently used frequency bandwidths. That proposal is shown in fig 1.2.

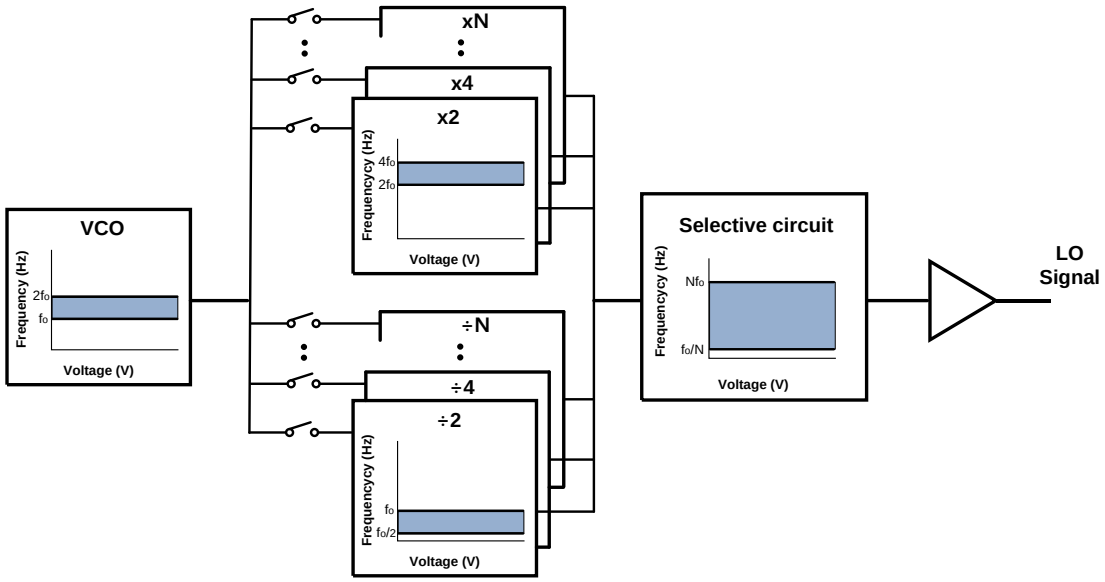


Figure 1.2. Main idea for signal generator

Chapter II

Design the Ultra Wideband Signal generator

2.1 The Basic of RF transceiver

The structure for RF wireless communication is shown in fig 2.1. Antenna, LNA, Downconverter, ADC (Analog to Digital Converter) and Digital baseband processor are the receiver parts (RX) which recover the original signal by receiving wireless frequency signal.

Also, Antenna, PA, Upconverter, DAC(Digital to Analog Converter) and Digital baseband processor are the transmitters (TX) which convert the original frequency to a certain frequency by sending data in order to make the transmit easier[10]. The device that generates the standard frequency for modulation and demodulation is called oscillator.

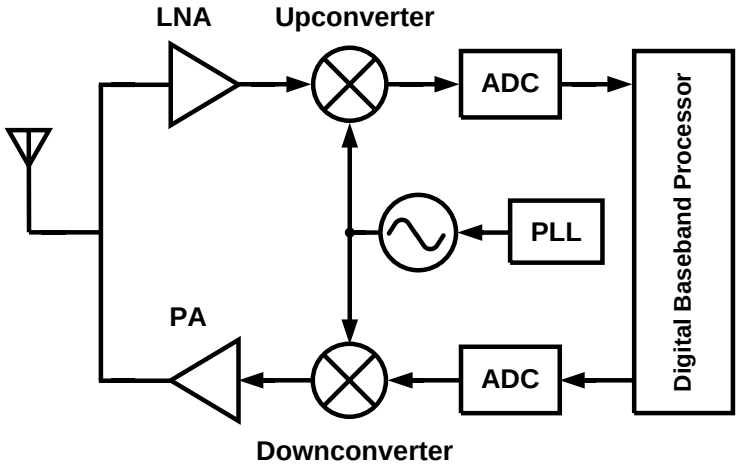


Figure 2.1. Generic RF transceiver

2.2 Oscillation Principle of LC Oscillator

Oscillator is a device which generates voltage signal with a phase. This device oscillating in a negative feedback circuit structure which doesn't affect any signal is shown in fig 2.2. Negative feedback circuit's closed loop gain is given by

$$\frac{Y}{X}(s)=\frac{H(s)}{1+H(s)} \tag{2.1}$$

At this point, an Oscillation condition is that the absolute value of H(s) is bigger than 1, and the phase of H(s) is 180°. Another Oscillation condition is that the phase of H(s) is 0° or 360° in positive feedback. The next section shows how to get the desirable frequency signals and how this device oscillates despite not affecting any signal.

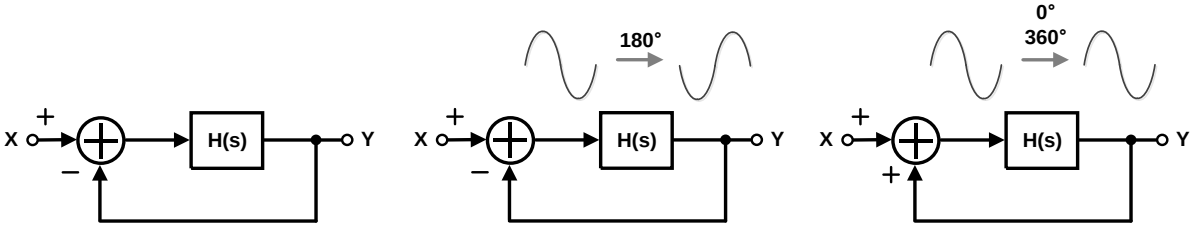


Figure 2.2. Feedback loop for oscillation

2.2.1 LC resonance frequency

The LC oscillator can obtain a certain frequency through resonance of LC. The general LC oscillator induces oscillation through this principle and generates voltage signals. As shown in fig 2.3(a), the impedance in the LC circuit is maximum when an imaginary number is 0. The impedance is given by

$$Z_{eq}(S)=sL_1+\frac{1}{sC_1} \tag{2.2}$$

Assuming the imaginary number is 0, the resonance frequency is calculated.
And hence,

$$\omega_o=\frac{1}{\sqrt{L_1C_1}} \tag{2.3}$$

But inductance and capacitance have the resistance elements in the ideal circuit, The Inductor has much bigger resistance than the Capacitor. So, adding a series resistance at the inductor can structure a RLC circuit as shown in fig 2.3(b). At this point, the impedance is given by

$$Z_{eq}(S) = \frac{R_s + L_1 s}{1 + L_1 s^2 + R_s C_1 s} \tag{2.4}$$

And hence,

$$\left| Z_{eq}(S = j\omega) \right|^2 = \frac{R_s{}^2 + L_1{}^2 \omega^2}{\left(1 - L_1 C_1 \omega^2\right)^2 + R_s^2 C_1^2 \omega^2} \tag{2.5}$$

Then, Z_{eq} is maximum near $f_o = 1/\sqrt{L_1 C_1}$ as resonance frequency according to the equation 2.3 and appears as an impedance with a certain value on R_S. These characteristics of ideal and non-ideal impedance are shown in fig 2.4. The characteristics of ideal and non-ideal imprudence affect oscillation frequency. The ideal impedance with a LC resonance characteristic converts the oscillation signal into the impulse signal. However, the real impedance generates an irregular oscillation frequency signal owing to the resistance of the inductor and capacitance. The performance of the inductor and capacitance can be revealed in a Q(quality factor) value and the equation is given by

$$Q_L = \frac{\omega L_1}{R_s} \quad Q_C = \frac{\omega C_1}{R_s} \tag{2.6}$$

At this point, Q_C value is much higher than Q_L value. Thus, the usual analysis ignores R_C which is series resistance of the capacitor. So the analysis should be done in consideration of the series resistance of the inductor. This non-ideality affects oscillation frequency and other external factors function in this process. The performance index which defines the quality is phase noise. The next chapter explains phase noise in CMOS environment.

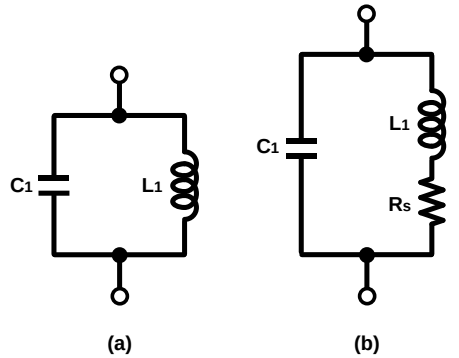


Figure 2.3. (a) Ideal parallel LC schematic (b) Non-ideal parallel LC schematic

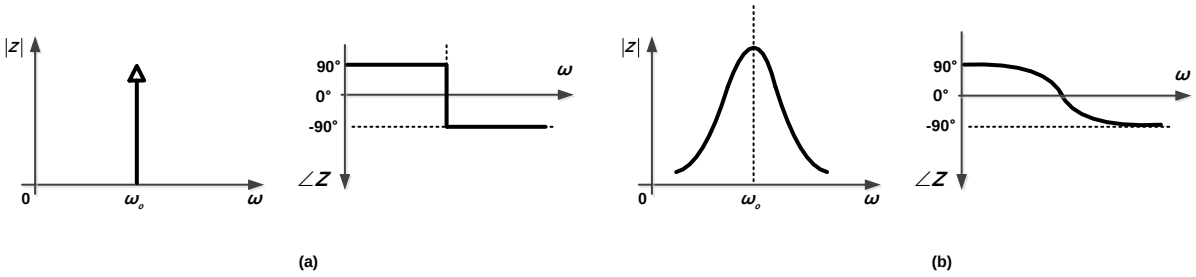


Figure 2.4. (a) Ideal impedance amplitude & phase (b) Non-ideal impedance amplitude & phase

2.2.2 Phase Noise in CMOS environment

The noise types fall into two in CMOS environment. The one is Resistor Thermal Noise and the other one is Flicker Noise. The Resistor thermal noise is shown in fig 2.5,
And the spectrum density is given by

$$S_v(f) = 4kTR, \qquad f \geq 0 \tag{2.7}$$

The given equation is proportional to the absolute temperature T and shows the regular value until 100 THz as decreasing from the higher frequency. The Flicker noise is differentiated on CMOS processes. As charge carriers move at the interface, some are randomly trapped and later release by such energy states, introducing “flicker” noise in the drain current. But the apparent reason has not been revealed. This noise spectrum is shown in fig2.6.
The assumed equation is given by

$$\overline{V_n^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \tag{2.8}$$

The equation called as '1/f noise' shows that the noise value is determined by 1/f without the given parameter. By the two noise effects shown earlier, oscillation frequency signal spectrum is generated based on the oscillation frequency in similar shapes to Flicker noise and Thermal noise.

Besides, the noise by the Q value of the LC as explained above and other various noises cause noise near oscillation frequency. The gap of spectrum between the desirable oscillation frequency signal and the offset frequency signal is called "phase noise" and is given by

$$-PhaseNoise\left[{}^{dBc}\!/_{Hz}\right] \tag{2.9}$$

This shows that what the efforts are to set the phase noise to the minimum in the design part. The first one is to minimize the Q values of both inductor and capacitor to reduce the Phase Noise, but the capacitor which is devised in CMOS process is unchangeable in structure design. So, modifying the structure of the inductor finds the most proper Q value. The second one is to minimize the noises either into the power line or caused in external circumstances. However, since the Flicker noise and Resistor noise is already determined by CMOS process, they cannot be dealt with by a designer. Further information will be available in the circuit design section.

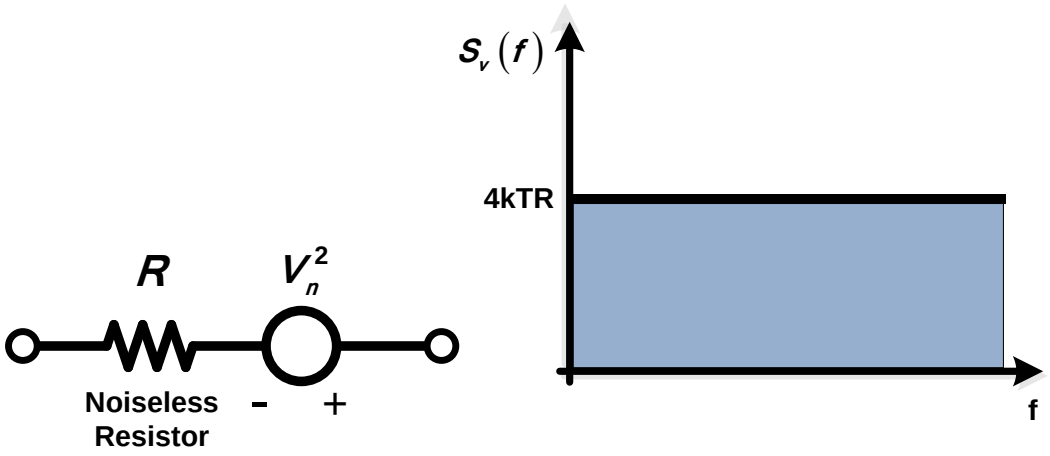


Figure 2.5. Resistor Thermal Noise

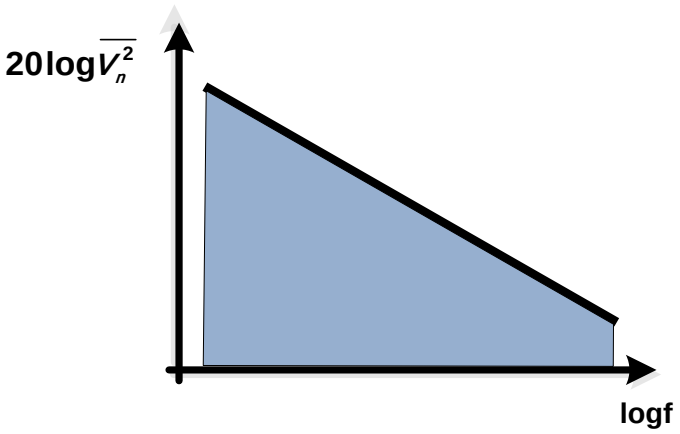


Figure 2.6. Flicker Noise

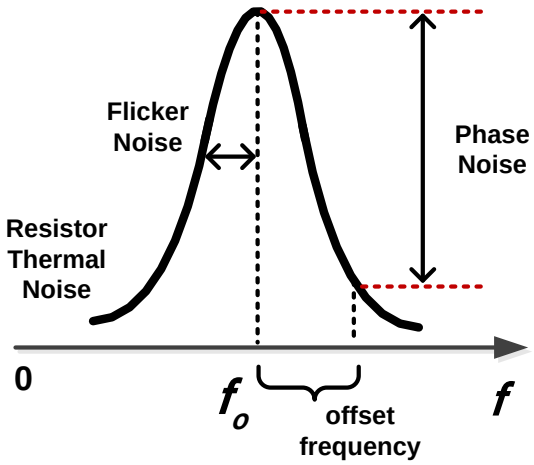


Figure 2.7. Phase Noise spectrum

2.3 Design consideration of Signal generator

The previous chapters are about how oscillating occurs through feedback circuits and the particles to determine the oscillation frequency are inductor and capacitor. In the background of this principle, this chapter contributes how to convert into a schematic design. For this, the amplifier in the common source structure shown in fig 2.8(a) should be considered. The amplifier in the structure, as shown in fig 2.8(b),

at the resonance frequency point of the LC has the maximum amplitude value, and the phaser of the Vout is 180°, as shown in fig 2.8(c).

The equation is given by

$$-g_m R_p \left[V \big/ V \right] \tag{2.10}$$

The last chapter showed that when the feedback loop is positive and the feedback signal phases are 0° or 360°, the oscillation, then, occurs. So, the output signal from the first common source amplifier goes into the input port of the second common source amplifier and the output signal of the second common source amplifier goes to the input port of the first common source amplifier. Then, oscillation occurs through the LC resonance frequency, under the condition that the voltage gain is $g_m^2 R_p^2 \geq 1$. Through passive impedance transformation,

The equation is given by

$$R_p = R_s \cdot \left(Q^2 + 1 \right) \sim R_s \cdot Q^2 \tag{2.11}$$

Since the equation 2.6 gives the Q_L value, the equation is given by

$$g_m \geq \frac{RC}{L} \tag{2.12}$$

This equation becomes an important design parameter at the oscillator design stage. The non-ideality of the inductor and capacitor being explained, the non-ideality of MOSFET is not dealt with so fat. So, the next chapter describes the non-ideality of MOSFET.

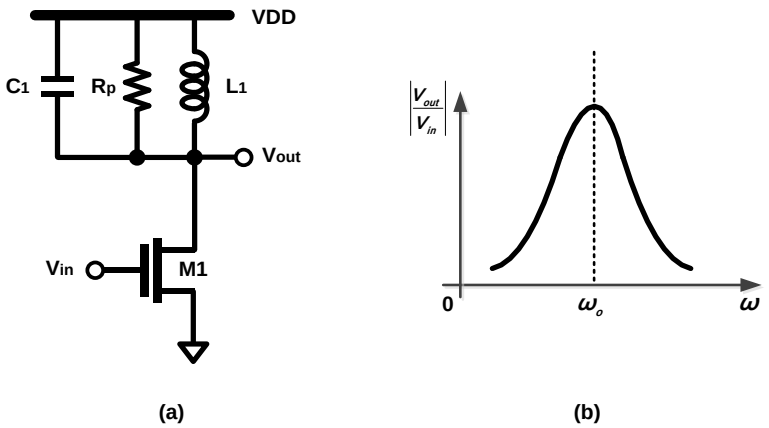


Figure 2.8. (a) Common source amplifier with LC impedance (b) Gain of amplifier

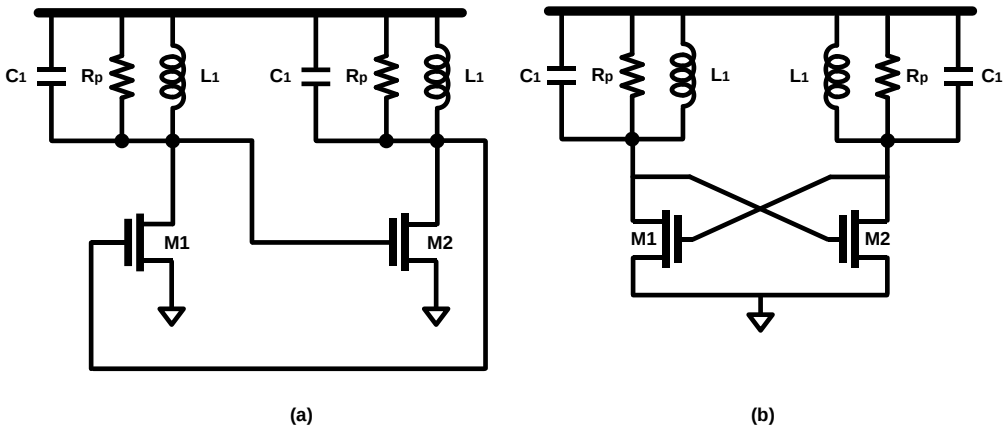


Figure 2.9. (a) Two common source amplifier in feedback loop (b) Redrawing of the oscillator

2.3.1 MOSFET Non-ideality

MOSFET has a lot of parasitic capacitance and resistance according to CMOS process. NMOS with several parameter is shown in fig 2.10(a)[11]. The oscillator in consideration of the parameter is shown in fig 2.10(b). Due to the non-ideality of MOS, the oscillation frequency (2.3) and the oscillation equation (2.12) differs a little. The equation with all parameters in consideration is given by

$$\omega_o = \frac{1}{\sqrt{L\left(C_1 + C_{GS} + 4C_{GD}\right)}}, g_m \geq \frac{1}{R_{DS}} + \frac{R\left(C_1 + C_{GS} + 4C_{GD}\right)}{L} \tag{2.13}$$

Now, the oscillation frequency and gin parameter determine the specs of the VCO. The oscillation frequency of the circuit presented in fig.2.10 is set by the resonance frequency of the inductor and capacitor. The way to convert the fixed oscillation frequency into wideband is considered as follows.

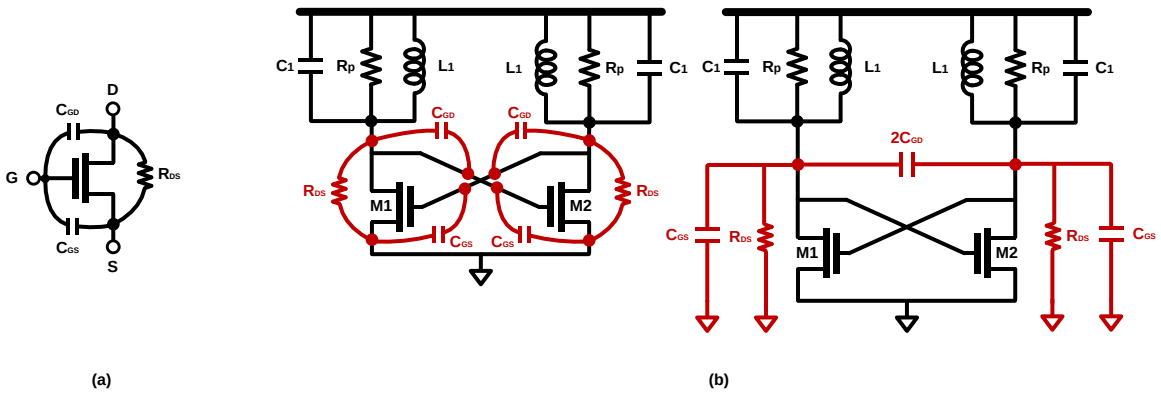


Figure 2.10. (a) MOSFET non-ideal parasitic elements. (b) Redrawing of the oscillator in parasitic

2.3.2 Wideband oscillator

In order for the oscillator to offer wide frequency bandwidths, the equation 2.13 is presented to describe the design to offer more variable frequency bandwidth by modifying the values of the inductance and capacitance. The circuits which are capable to provide wide frequency bandwidths are presented as follows. The first circuit shown in fig 2.11 is to use varactor diode and tune the oscillation frequencies. This circuit is known as “VCO (Voltage Controlled Oscillator)”, and is the most common in the oscillator structure. The paper refers to the combination of the inductor and the capacitor as LC Tank and explains various ways of tuning frequencies through the combination, as shown in fig 2.11. The fig 2.12 shows the variety of tuning techniques. The second circuit, shown in fig 2.12(a), offers discrete tuning through the multiple array and switches of the capacitor. The third circuit, shown in fig 2.12(b), offers discrete tuning through the multiple array and switches of the inductor. The fourth circuit, as shown in 2.12(c), uses mutual inductance and changes oscillation frequency through variation of the impedance when switching. Finally, the circuit structure in fig 2.12(d) configures oscillation frequency as attaching a switch onto the spiral inductor which is used in a general CMOS process changes the inductor values [12]. Aside from those explained, there are various techniques for tuning frequency. However, the limitation for LC tuning range is easily noticed in that the techniques are dependent on the simple combination of the inductor and the capacitor for tuning frequencies, and has a maximum limit owing to the oscillation condition. Beside the LC tuning method, the dividing method and the multiplying method can change frequency, which are used for other external structures. In this paper, the next chapter explains the frequency multiply method.

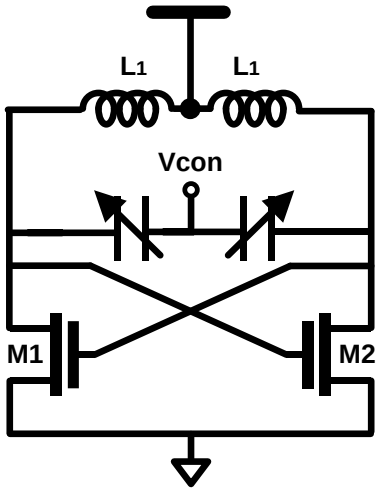


Figure 2.11. Schematic of VCO

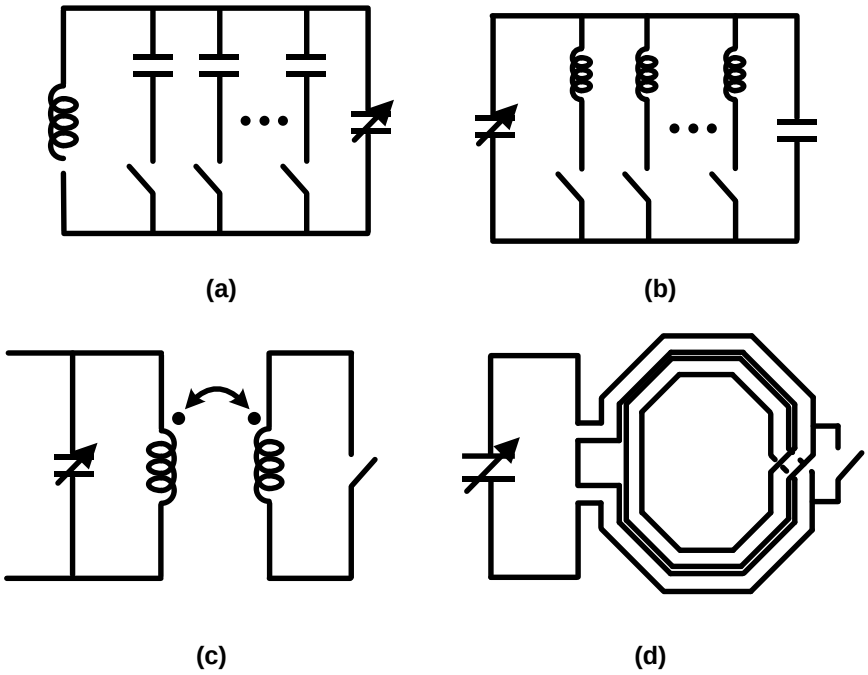


Figure 2.12. Schematic of LC Tank

2.3.3 Theory of the frequency multiplication

Previous chapter mainly describes the oscillator design process and the frequency tuning process with modifying the structures of the LC tank. Structure change of the LC tank has a limitation in frequency tuning range. In order to obtain wider frequency bandwidth, the need for another external structure design is required. So, this section contributes explanation on the external structure called as "Frequency multiplier." The frequency multiplier is the circuit using linear superposition of sinusoidal signal. If the differential phase signals(0,π) overlap at one node, which is called as "linear superposition", the signal generates twofold frequency signal, and the results are presented in [13]. As shown in fig 2.12, if the circuit is realized into a bias circuit through the DC voltage of the gates in the two NMOS, and the pure AC signal without DC voltage goes to the gates of two NMOS through the capacitor, the signals are rectified such that the full waive rectified current is detected at the current path node, as shown in fig 2.12. Fourier series is given by

$$f(t) = \sum_{n=-\infty}^{\infty} F_n e^{jn\omega_o t} \qquad \text{at } T=\pi,\ w_o=2$$

$$F_n = \frac{1}{T}\int_0^T f(t) e^{-jn\omega_o t} dt$$

$$= \frac{1}{\pi}\int_{0}^{\pi} \sin te^{-j2nt}dt$$

$$= \frac{2}{\pi\left(1-4n^2\right)}$$

$$\therefore\ f(t) = \frac{2}{\pi}\sum_{n=-\infty}^{\infty}\frac{1}{\left(1-4n^2\right)}e^{j2nt} \tag{2.14}$$

Fourier series shows that F0 term is removed and since 2fo term, harmonic occurs.

Also, the differential signal(π/2, 3π/2) of the opposite phase is solved with Fourier series in the same way, the result is given by

$$f(t) = \frac{2}{\pi}\sum_{n=-\infty}^{\infty}(-1)^n\frac{1}{\left(1-4n^2\right)}e^{j2nt} \tag{2.15}$$

If the equation (2.14) and the equation (2.15) are combined, $2f_o$ signal is removed, and then only $4f_o$ signal is detected. This verification can be used to generate 2x frequency, and summarized in an equation as follows.

$$I_{N=2k} = \frac{4}{\pi}\left(\frac{k}{2} - \frac{k}{(2k-1)(2k+1)}\cos(2k\omega_o t)\right) \tag{2.16}$$

1~Nf0 frequency can be generated through the equation and the remarkable frequenc(y bandwidth is feasible. In order to use this method, the oscillator to generate multiple phase signals is required. The next chapter explains the oscillator to obtain multiple phase signals.

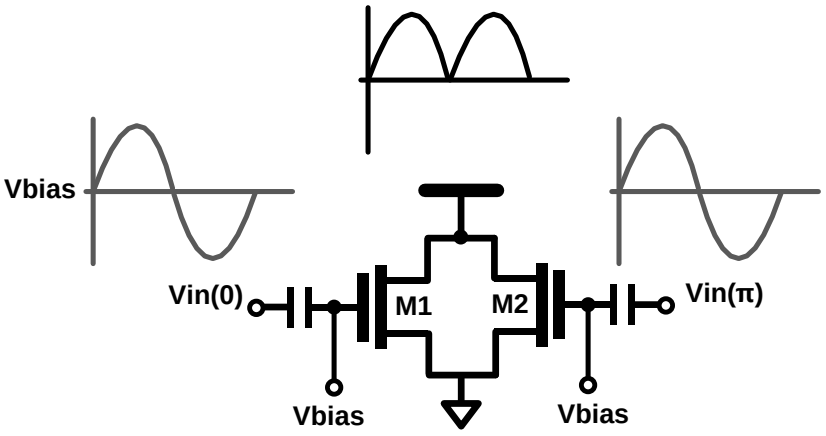


Figure 2.11. Schematic of the frequency multiplier

2.3.4 LC Ring type VCOs

In order for an oscillator to obtain multiple phase signals, the circuit is organized in a way that multiple phases comes from the signal with phase fixed. In this chapter, the LC ring type VCOs which can generate multiphase signals are explained. The LC Ring type VCOs has a structure, shown in fig 2.12, where 2N phase signals can be generated through N-stage VCO [14]. For example, if a circuit is structured in 2-stage VCO, it generates 4 phase signals, and if in 4-stage VCO, it generates 8 phase signals. The principle for the device is presented in fig 2.13. If the device in $-g_m$ cell and amp cell is structured in a way shown in 2.13(b), the equation for X is given by

$$X = (\alpha_1 Y - X) H(s)$$

(2.17)

In a equivalent way, Y is given by

$$Y = (\alpha_2 X - Y) H(s) \tag{2.18}$$

If the equations (2.17) and (2.18) are solved with a simultaneous equation, the equation is given by

$$(\alpha_2 X^2 - \alpha_1 Y^2)[1 + H(s)] = 0 \tag{2.19}$$

As a result of (2.19), at oscillation frequency, 1+H(s)=0 hence

$$\alpha_2 X^2 = \alpha_1 Y^2 \tag{2.20}$$

Based on these equations, if gains (α_1 , α_2) of amp cell are the same, the circuits is made in in-phase, where the equation is $X = \pm Y$ and the phase gap is none. But if the amp cell is made in anti-phase, the gain value of amp cell is $\alpha_1 = -\alpha_2$, where the equation is $X = \pm jY$. Thus, the phase gap is 90°, -90°. Also, if the LC Ring type logic is made to the number of VCO (N), in the same way as fig 2.13, the equations for X, Y, …, Z are given by, as follows.

$$X = (\alpha_N Z - X) H(s) \tag{2.21}$$

$$Y = (\alpha_1 X - Y) H(s) \tag{2.22}$$

$$Z = (\alpha_{N-1}(Z - 1) - Z) H(s) \tag{2.23}$$

If the equation is interpreted, the phase signal as below is found in accordance to the number of VCO(N)

$$0,\ \frac{\pi}{N},\ \frac{2\pi}{N}\ldots,\ \frac{(2N-2)\pi}{N} \tag{2.24}$$

Therefore using this structure can generate multi-phase signal.

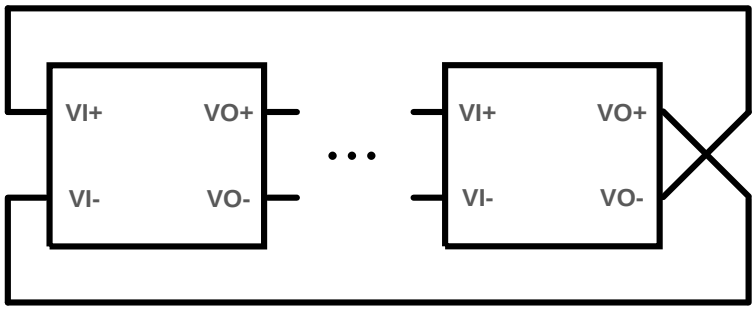


Figure 2.12. Logic of LC Ring VCO

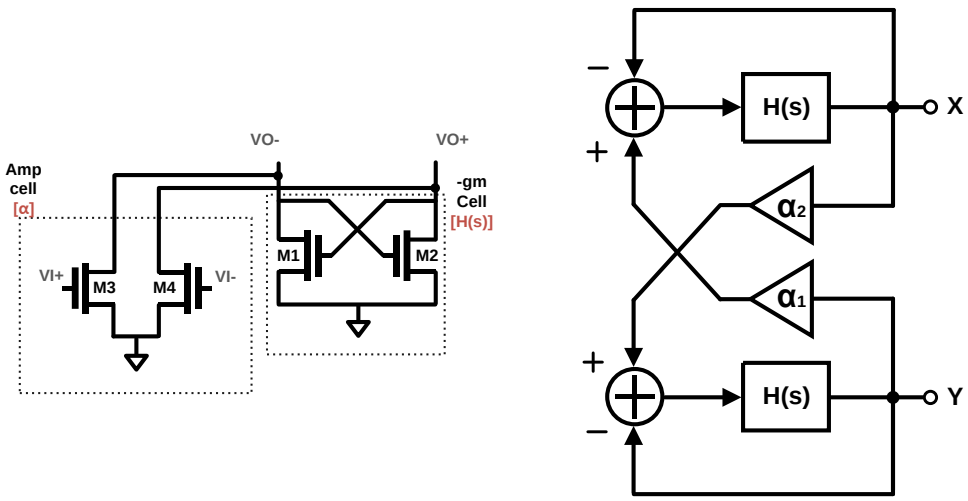


Figure 2.13. (a) Oscillator with amp cell (b) Feedback model of quadrature oscillator

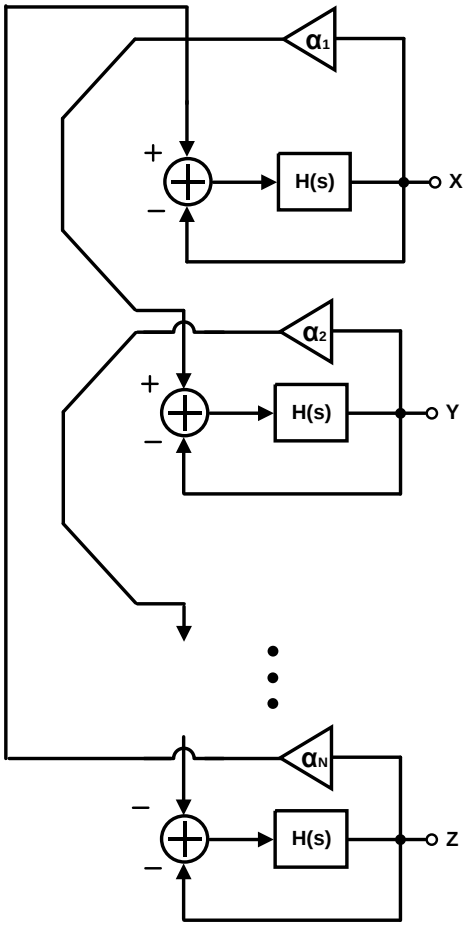


Figure 2.14. Feedback model of LC ring type of oscillator

2.4 Proposed Ultra wideband signal generators

In this principle, this chapter explains the ultra-wide band signal generator which can cover the whole existing wireless frequency bands. There have been three types of signal generators for the basic principle of the Ultra wide band signal generator, and each type has a different characteristic. The common ground between three different signal generators of a certain characteristic is that a multiplier is used. The frequency multiplier is organized to have a programmable characteristic and select the desirable frequency. These characteristics are presented in fig 2.15. Once N-phase of same frequency signal is generated with use of the LC ring type VCOs, twofold (2X), quadruple (4X), …, N-fold (NX) multiple frequencies are provided. If $f_o \sim 2f_o$ frequency can be provide. $f_o \sim Nf_o$ frequency in succession can be provided. So, with use of the operational characteristic, this structure of programmable frequency multiplier can cover the whole frequency bandwidths for wireless communication. In the next chapter, the other two designs using the same concept are presented.

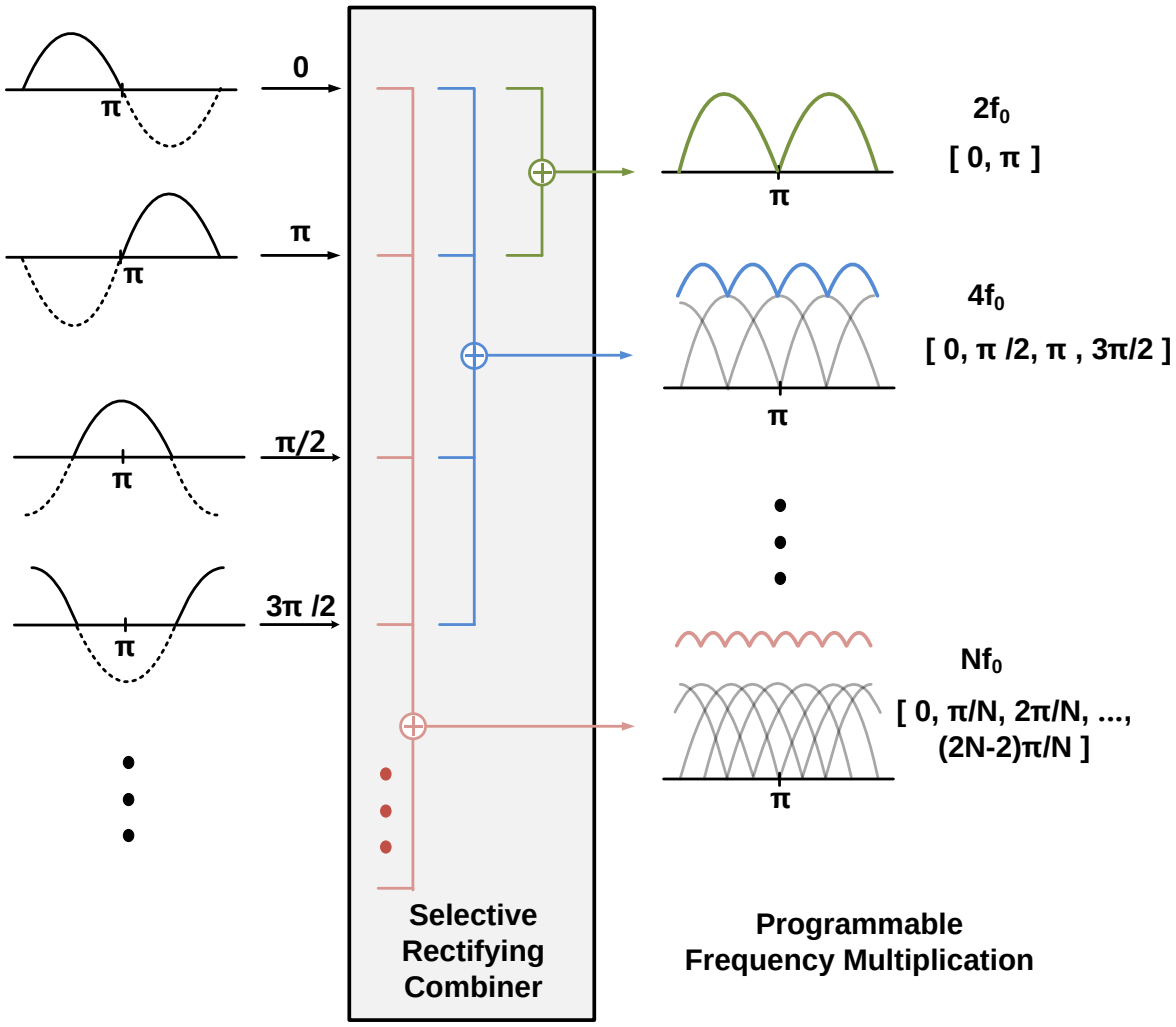


Figure 2.15. Conceptual diagram of selective frequency synthesis.

2.4.1 Signal generator with programmable wire bonding inductor VCO

The signal generator proposed in the paper offer, at large, two design methods. The one is a design method of VCO core, and the other one is the frequency multiplier design method. So, this chapter offers two design methods which are VCO and frequency multiplier.

1. VCO design

The structure of VCO used in this paper is shown in fig 2.16. This structure using bond wire inductor is hard to make the structure of the inductor in the way shown in fig 2.11. So, here, with use of VCO structure with PMOS, not the structure of the g_m cell which is widely used, a circuit of a 4-stage LC ring type is designed. This structure is called as "VCO using NMOS & PMOS cross coupled pairs". Using the VCO structure with PMOS has an advantage that the oscillation frequency can be set only by using

a single inductor, and twofold voltage swing occurs since the gain is obtained by using the current once more. LC tank is structured with bondwire inductor and the varactor diode. In the CMOS process, the spiral inductor is widely used for the processing characteristic. But the bondwire inductor has an advantage that it gives a higher Q value than the spiral inductor, thus, capable of covering wider band frequency with switching. But, because of switching the inductor, the problem of providing discrete frequency bandwidths is dealt with use of the varactor diode in order that the continuous frequency sweep is available.

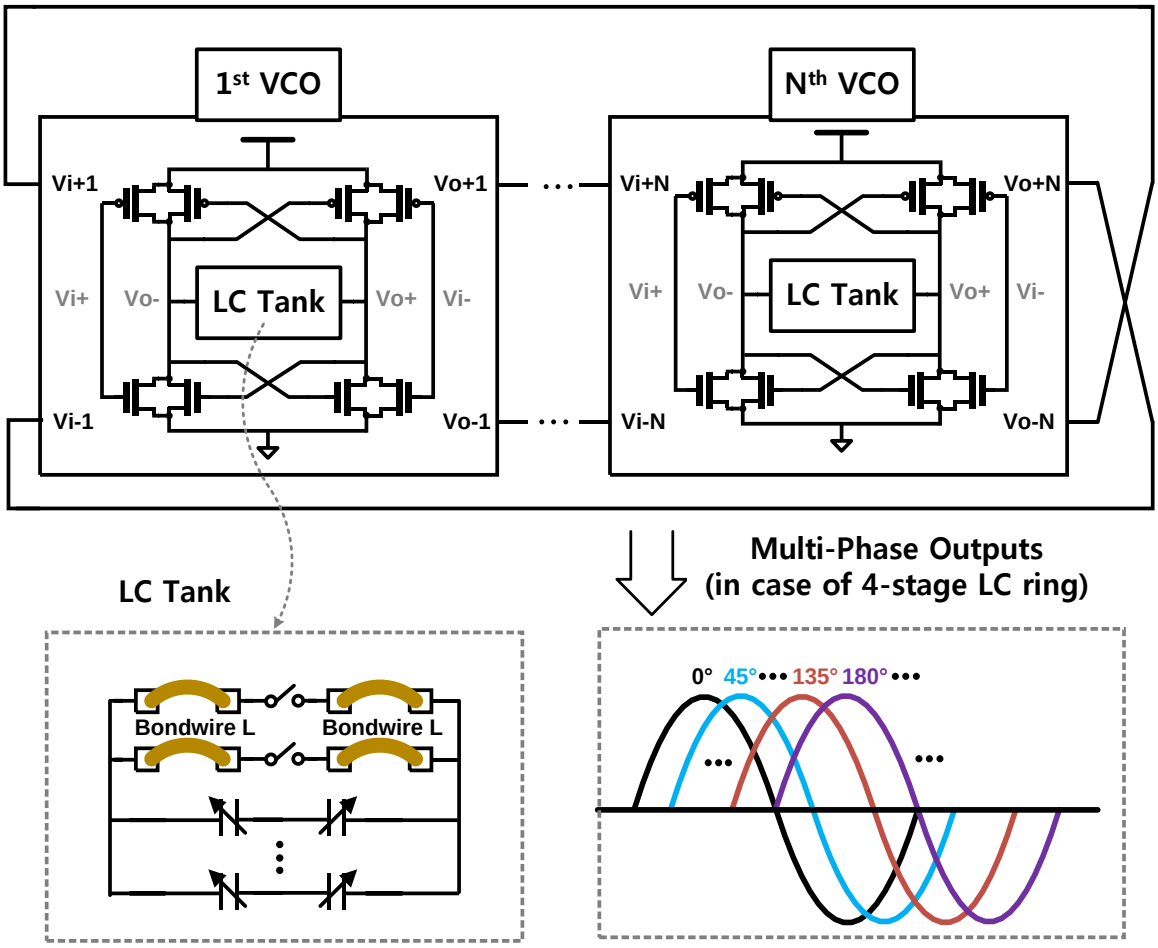


Figure 2.16. Multi-phase signal generation using a LC-ring oscillator with bondwire inductors

2. Frequency multiplier design

The frequency multiplier schematic used in the paper is shown in fig 2.17. The outputs of the 4-stage LC ring type VCOs are connected to each frequency multiplier with a switch. Its programmable or t unable characteristic is achieved through SW1–SW3 switches. If SW1 is turned on and others are turned off, 0 and π phases are selected to provide 2X frequency multiplication according the linear superposition. If both SW1 and SW2 are on, four-phase signals $(0, \pi/2, \pi, 3\pi/2)$ are combined together, and 4X frequency multiplication is implemented. Finally if every switch (SW1–SW3) is on, eight-phase signals are selected for the frequency synthesis, resulting in 8 X frequency multiplication. In this way, the proposed structure can provide the tunable multip lication characteristic of 2X, 4X, and 8X. A four-stage LC-ring VCO generates eight-phase si gnals of the same frequency. To expand its frequency range, two switchable bondwire-inducto r pairs are adopted to implement the tunable inductance like [2–3]. The frequency synthesis part is implemented by locating SW1–SW3 switches at input nodes of NMOS pairs (M1–M8). Depending on SW1–SW3 values, multi-phase outputs of the LC-ring VCO are selectively con nected to the frequency synthesis block. These selected VCO output voltages are converted in to multi-phase currents and summed together, providing programmable frequency multiplication of 2X, 4X, and 8X. According to [13], the synthesis output current is numerically written by expression 2.16. , where k is the control input for the frequency synthesis, w0 is the VCO fr equency. The condition of k=1 gives 2X frequency multiplication, and generally the k value means k times frequency multiplication. Therefore, the tuning capability of the proposed frequ ency synthesis is achieved by changing the k value which is implemented as SW1–SW3. This work was compared with previous works in table 1, where it can be known that this work would be one of successful wideband design methods.

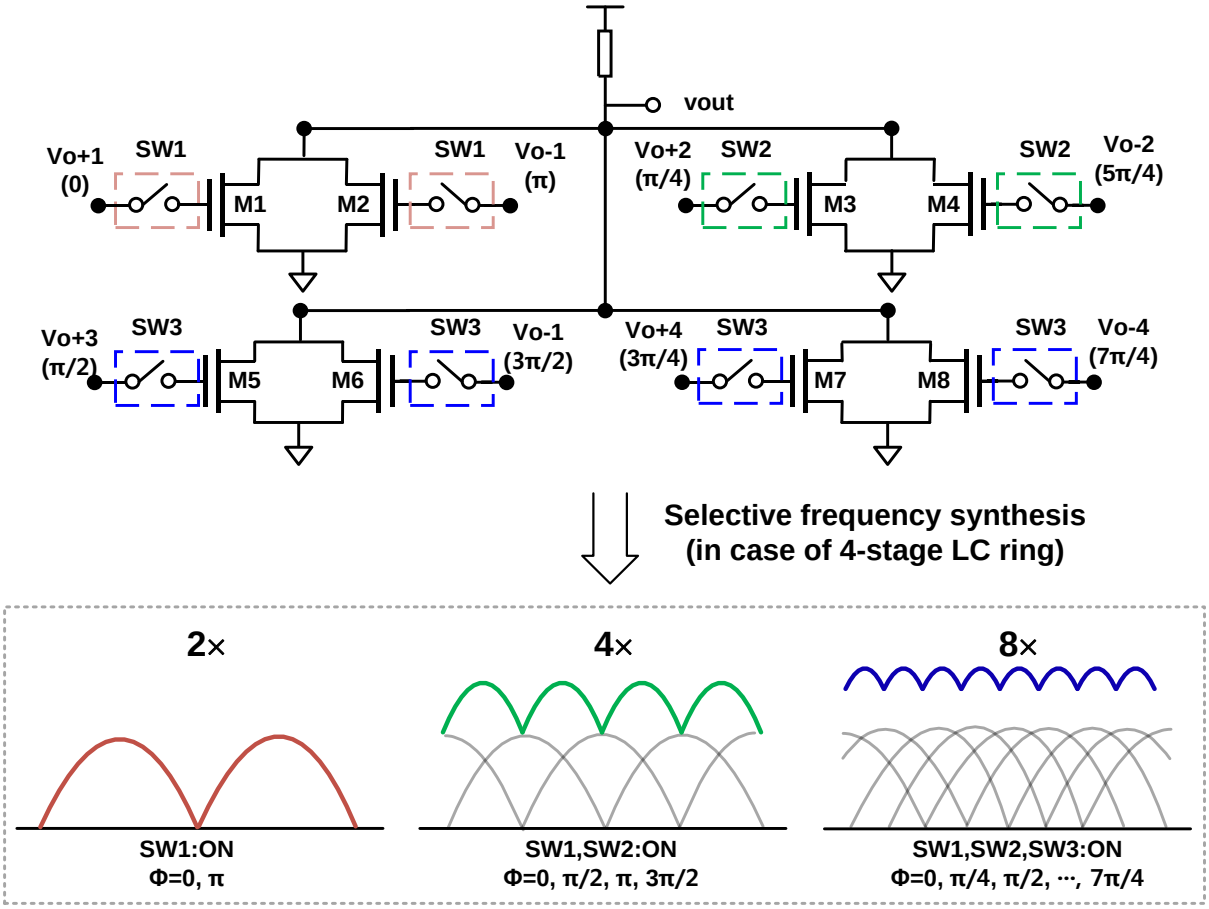


Figure 2.17. Selective frequency synthesis circuit and programmable frequency multiplication

	2x frequency	4x frequency	8x frequency
sw1	ON	ON	ON
sw2	OFF	ON	ON
sw3	OFF	OFF	ON

Table 2-1. Truth table of frequency multiplier

3. Chip layout & photograph

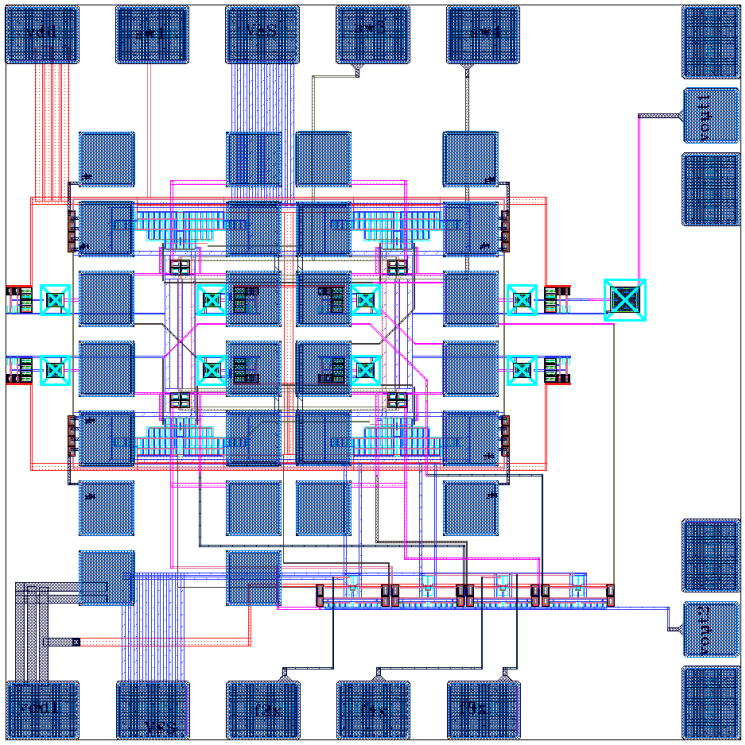


Figure 2.18. Layout of signal generator with programmable wire bonding inductor VCO

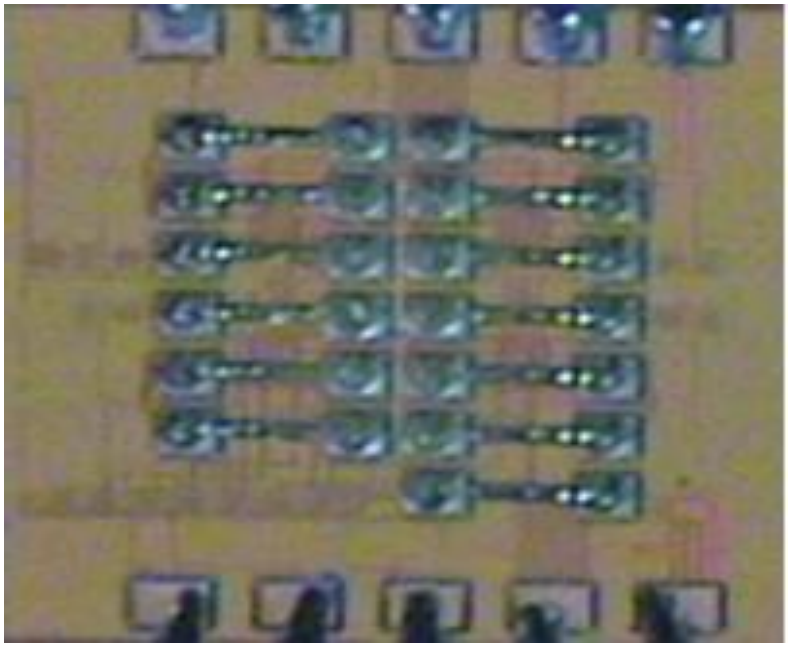


Figure 2.19. Chip photograph of signal generator with programmable wire bonding inductor VCO

2.4.2 Signal generator using reconfigurable selective combination

1. VCO design

The VCO structure used in the paper is shown in fig 2.20. The difference with the previous structure is that the device is accompanied with spiral inductor instead of bondwire inductor. Also, the VCO structure with amp cell made only in NMOS is designed instead of the VCO using NMOS and PMOS cross coupled pairs. The first changed point is that although bondwire inductor is a structure that can be switched with a high Q value, spiral inductor is used instead of bondwire inductor since the LC-ring structure which we propose is hard to be designed with a symmetric structure. The second changed point is that the VCO made only in NMOS, instead of the VCO using NMOS and PMOS cross coupled pairs, has an advantage of generating a higher frequency range by offering low parasitic cap. Thus, the second version is designed by having changed the two points. From the structure shown in fig 2.17, the switch is removed and, instead, the VCO is designed to have a reconfigurable structure in order to minimize power consumption and multiply frequency, as shown in fig 2.21(a). The next chapter explains the reconfigurable LC-Ring VCO and the frequency multiplier.

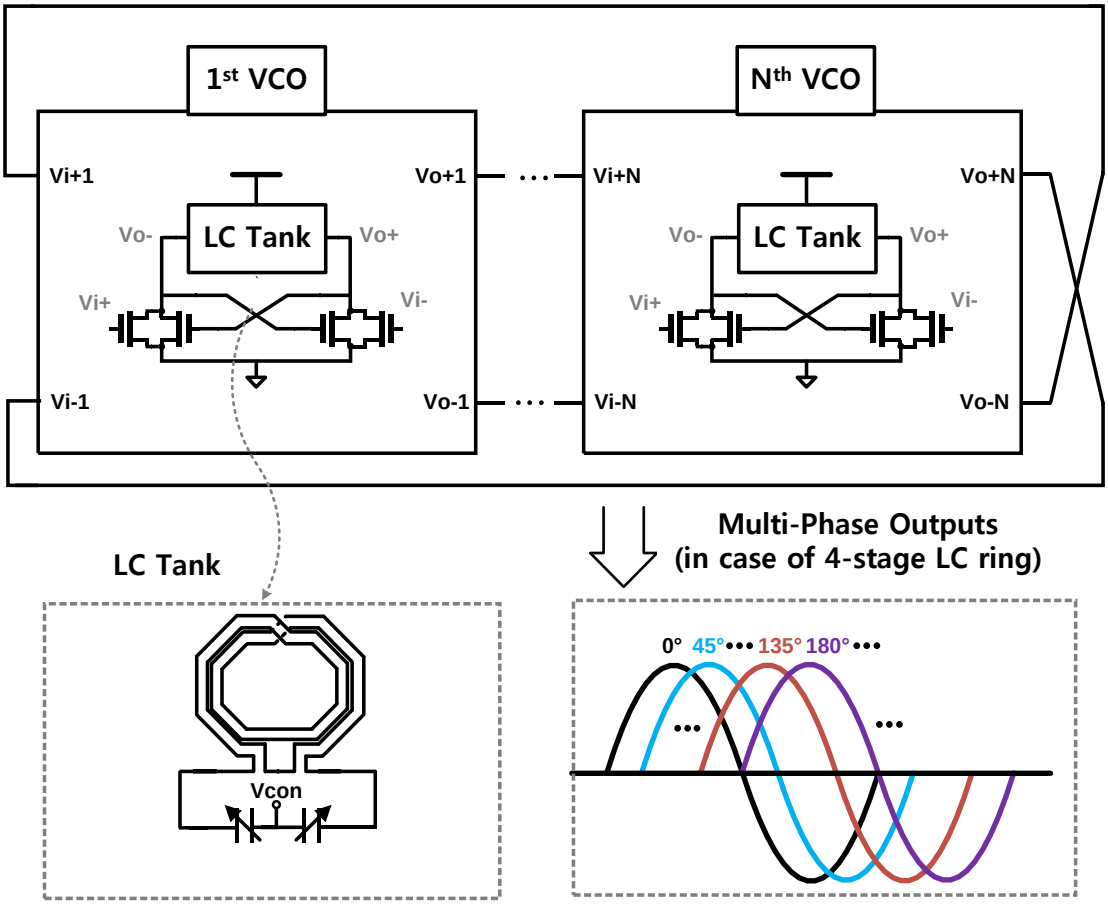
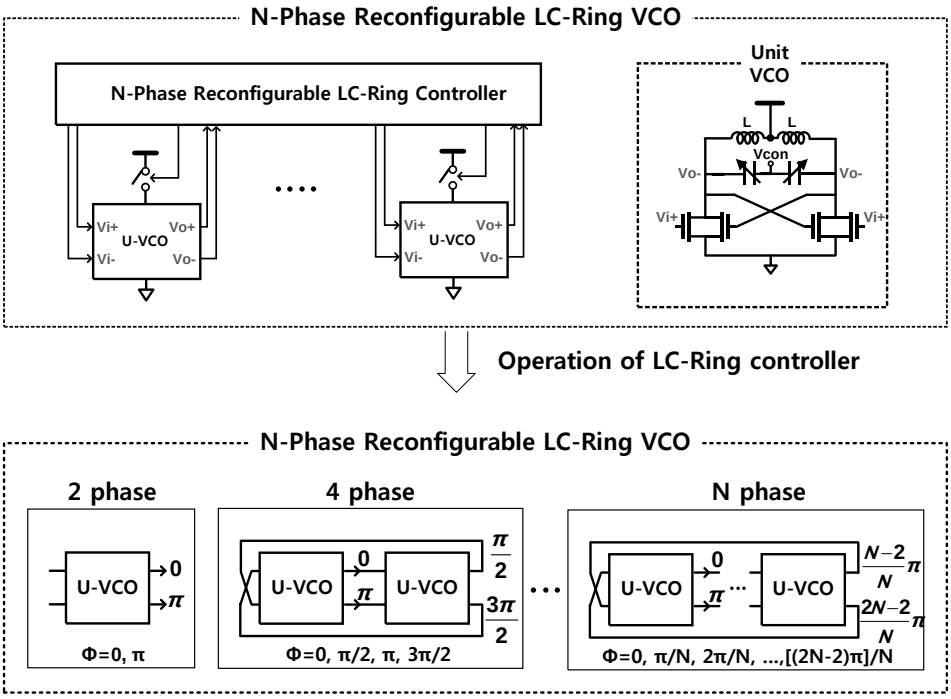


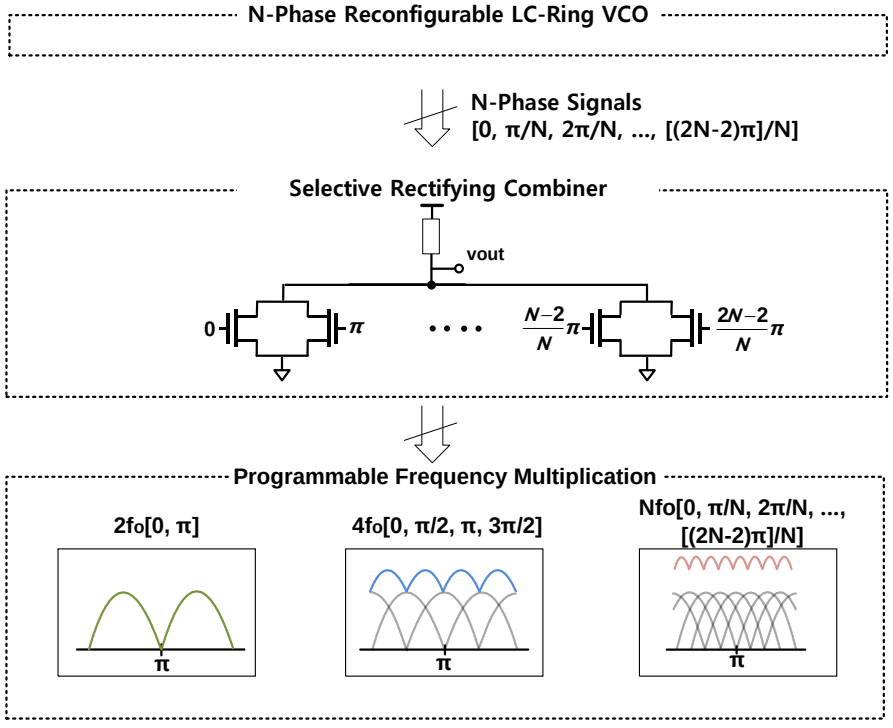
Figure 2.20 Multi-phase signal generation using LC-ring oscillator with spiral inductors

2. Reconfigurable selective controller and frequency multiplier

The operation principle and structure is shown in fig 2.19. Multi-phase signals can be generated through ring oscillators or multi-phase dividers, but this work is based on the LC-ring structure [14] since LC-tuned circuits are preferred for low noise performance. Fig. 2. 21 represents a simplified schematic and conceptual operation of the proposed wideband signal generator. N-phase outputs of a LC-ring VCO are directly connected to a selective rectifying combiner like Fig. 2(a). Since programmable frequency multiplication uses different number of phases, the LC ring is designed to have a reconfigurable structure in order to minimize the power dissipation. As in Fig. 2.21(b), two fold (2X) multiplication mode uses only single LC VCO, and Quadruple (4X) mode uses two-stage ring. In this way, only required number of unit LC oscillator is activated and the others are turned off. N-phase LC-ring outputs are directly connected to gate inputs of NMOS array in the selective rectifying combiner. If two differential signals of 0 and π phases are activated and the others are deactivated by turning on/off PMOS transistors on top of unit VCOs in the LC ring, only two NMOS transistors corresponding to 0 and π phases synthesizes twofold frequency of 2fo. If four-phase signal of 0, $\pi/2$, π, and $3\pi/2$ are activated by turning on two preceding VCOs and constructing a quadrature LC ring as in Fig.2.21(b), the selective combiner works as 4 times frequency multiplier. Activation of every unit VCO gives N-phase signals and the corresponding combiner output becomes N-fold frequency (N). In this way, controlling the number of activated unit VCOs and making the corresponding LC ring structure result in a kind of programmable frequency multiplication function.



(a)



(b)

Figure 2.21 Proposed wideband signal generator: (a) schematic of Reconfigurable VCOs and operation. b) Operation of the programmable frequency multiplication.

3. Chip layout & photograph

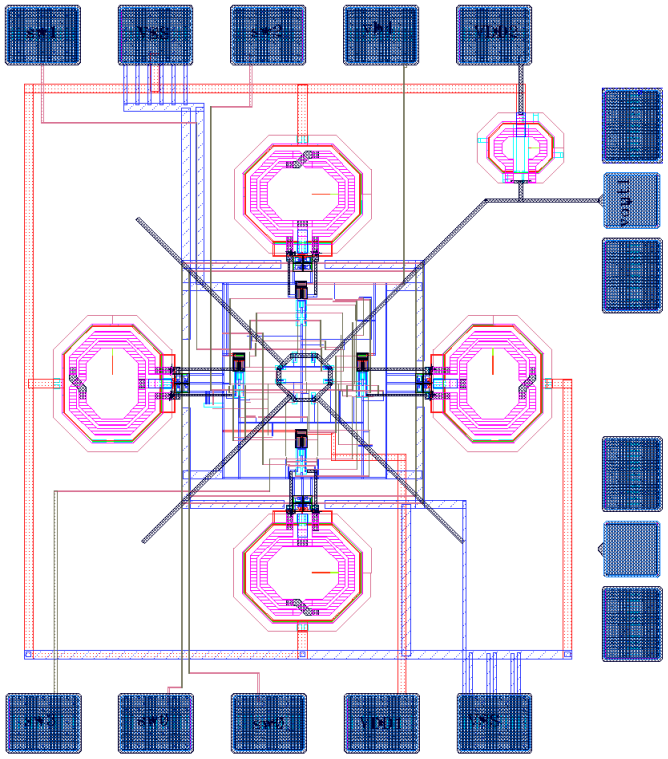


Figure 2.22. Layout of Signal generator using reconfigurable selective combination

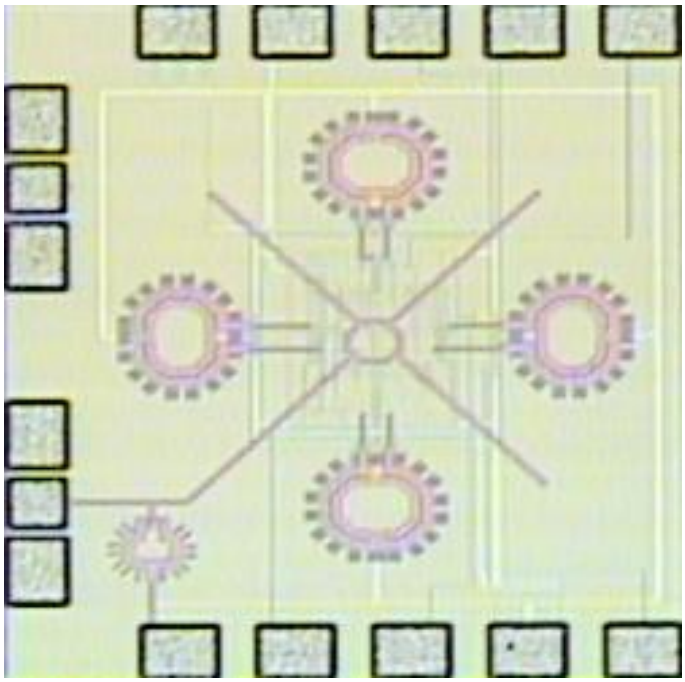


Figure 2.23. Chip photograph of Signal generator using reconfigurable selective combination

Chapter III

Experimental results

3.1 Experimental environment

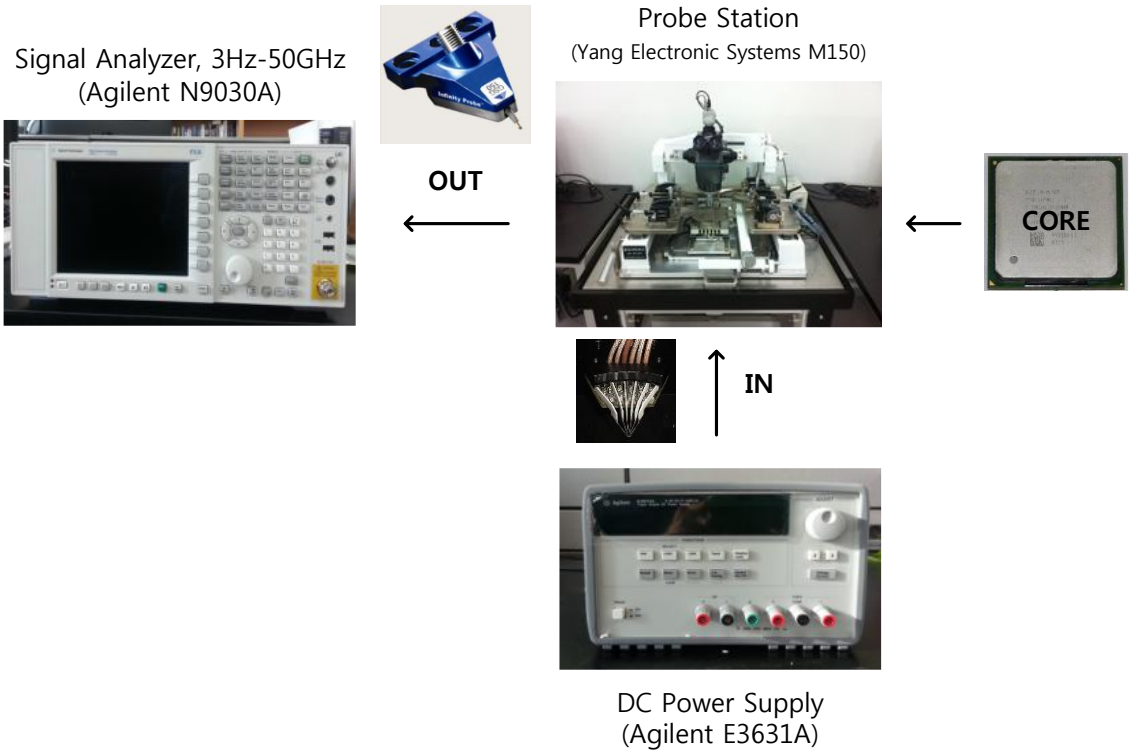


Figure 3.1 Process chip test measurement

3.2 Results of Signal generator with programmable wire bonding inductor VCO

A prototype of the proposed signal generator was fabricated in a 65 nm CMOS process. The die photo graph is shown in fig 2.19, where its die size is 1mm x 1mm and its core size is 0.65mm x 0.85mm. A four-stage LC ring VCOs is implemented and each unit VCO cell includes two pairs of switchable bondwire inductors to provide wide tuning range and also accommodate bondwire's inductance variance. The length of each bondwire inductor is 200um.

3.2.1 Frequency band width of signal generator

The results of frequency bandwidth that we obtain through the experiment are shown in fig 3.2. The tunable frequency bandwidth graph of VCO core structure using bondwire inductor switching is VCO core (1X), and the figure can be twofold (2X) or quadruple (4X) through frequency multiplier's programmable characteristic. The reason why the graph lacks octuple (8X) frequency is that the chip in symmetric structure is difficult to design due to the bondwire inductor structure, and generate multiphase unless the symmetric structure is designed. That results in the lack of octuple (8X) frequency. Finally, The LC-ring VCO has the frequency range of 4.3.5–6.3GHz. Base on this VCO frequency range, twofold (2X)/ quadruple (4X) frequency multiplications provided their corresponding ranges of 4.3–6.8GHz, 8.6~13.62GHz, 17.4–27.4GHz. Therefore, the overall frequency coverage is roughly from 4.3GHz to 27.4GHz. So, the next version overcomes the disadvantages of this structure.

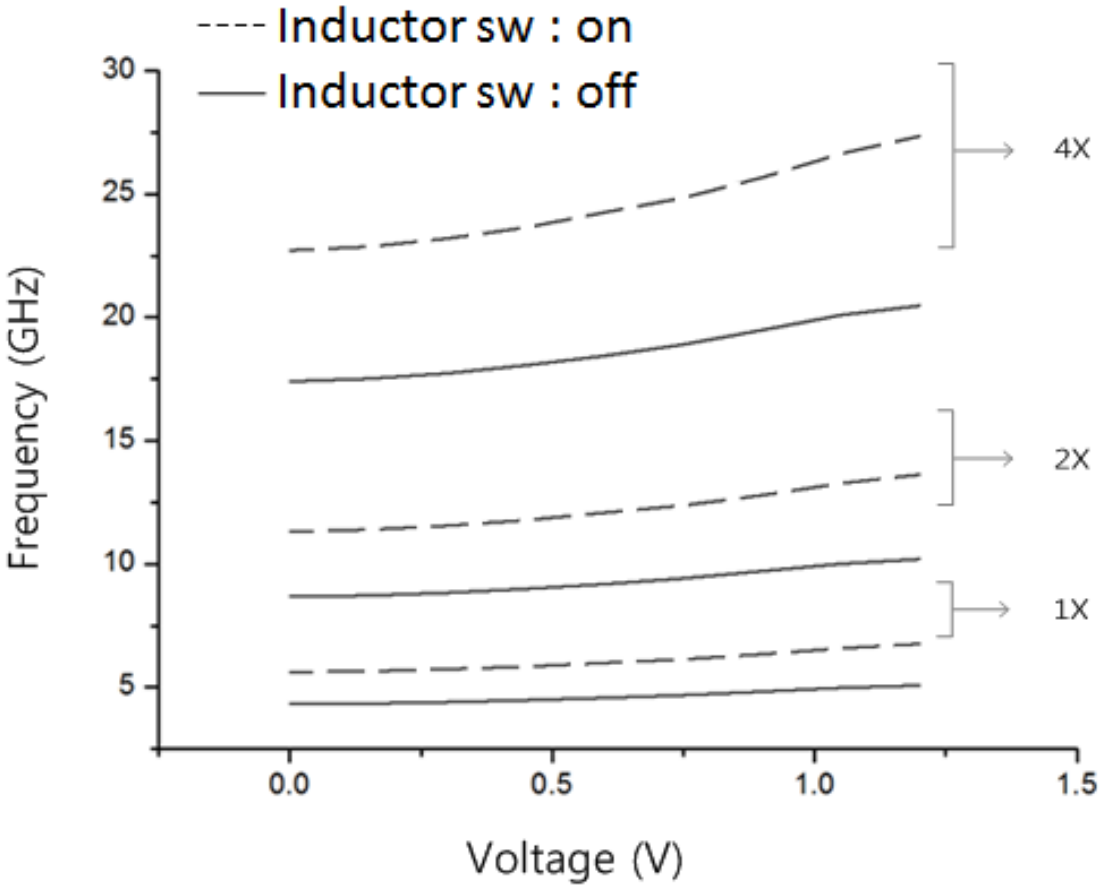


Figure 3.2 Frequency characteristic of a prototype signal generator

3.2.2 Output spectrum & Phase noise of signal generator

Output spectrum and phase noise results are shown in fig 3.3. 1x frequency is measured as 4.3GHz, a signal of VCO core. Because of the difficulty of oscillation at the preset frequency, raising the inductance of the inductor by applying the equation 2.13 generates lower frequency than the preset frequency. The method to raise the inductance of the inductor is shown in fig 3.4. Through the method of changing the bondwire inductor shape, the more stable status capable of oscillation is achieved. Also, the output spectrum resulting from the frequency multiplier is twofold (2X) or quadruple (4X). Phase noise is -91dBc/Hz at 1MHz offset from 4.3GHz carrier.

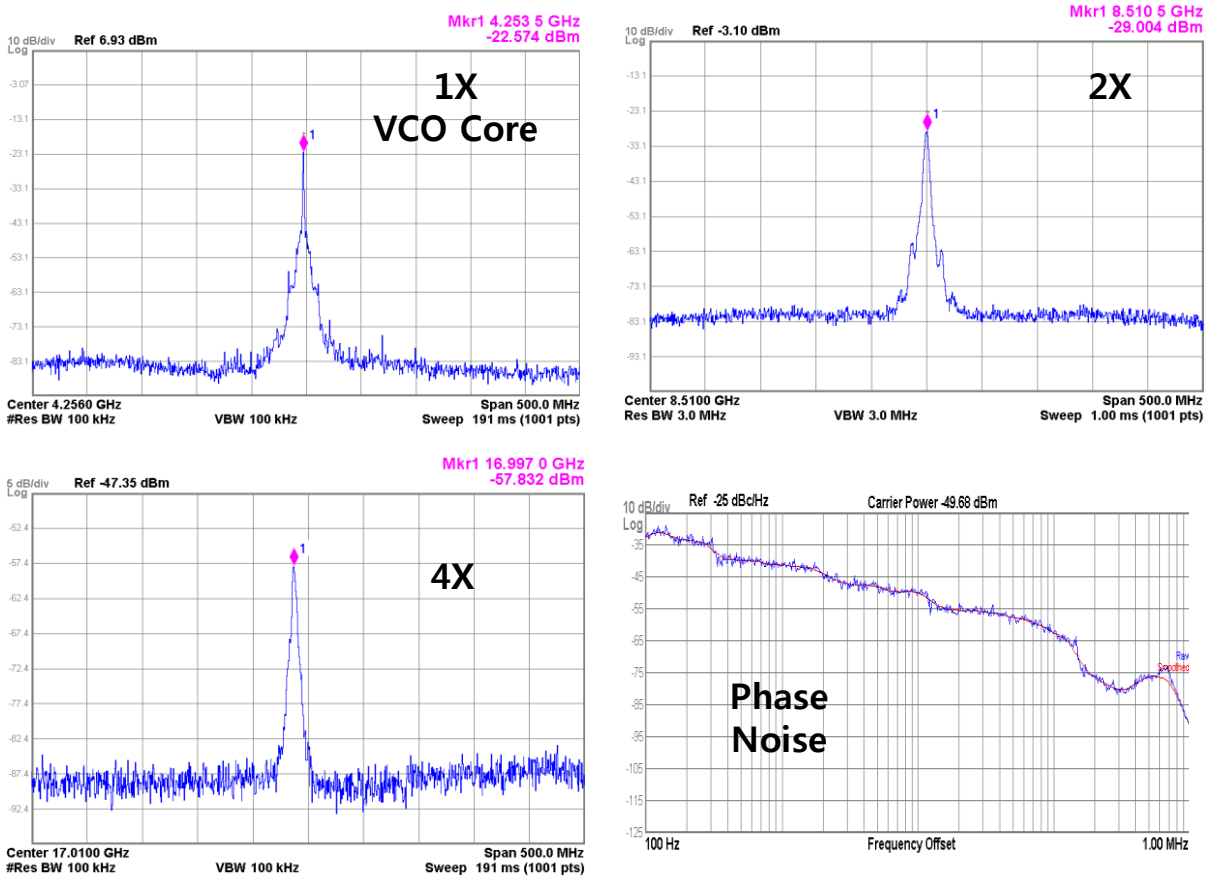


Figure 3.3 Measured 1x/2x/4x output spectrums of signal generator & phase noise from 4.3GHz carrier frequency

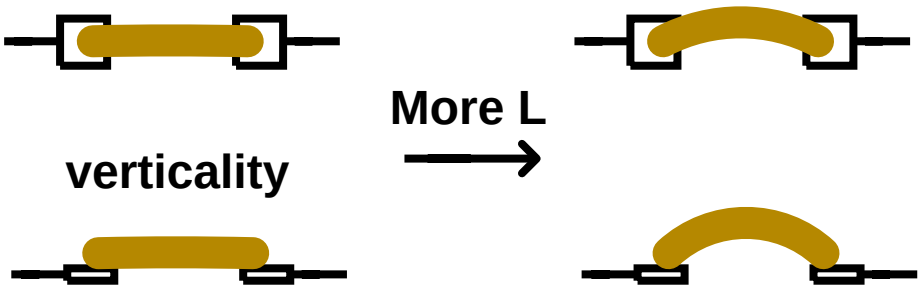


Figure 3.4 Making process of wire bonding inductor for big inductance

3.3 Results of Signal generator using reconfigurable selective combination

A prototype of the proposed signal generator was fabricated in a 65 nm CMOS process. The die photo graph is shown in fig 2.23, where a LC-ring multi-phase signal generator and its selective rectifying combiner were fully integrated. Whose die area is about 1mm x 1mm. Four-stage LC ring was implemented to provide quadruple mode frequency multiplication of 1x,2x,4x, and 8x. Each unit Each unit VCO uses one symmetric spiral inductor for its LC tank, and the overall signal generator includes four integrated inductors which are symmetrically located to minimized mismatches among unit VCOs.

3.3.1 Frequency band width of signal generator

The frequency bandwidth achieved through the experiment is shown in fig 3.5. The maximum octuple (8X) wideband characteristic is measured unlike the result of the previous version of signal generator with programmable wire bonding inductor VCO. Selective rectifying combiner provides three selectable frequency bands; 12.56-15.4GHz for 2×, 25.08-30.5GHz for 4×, and 48.6.1-59.4GHz for 8× mode. These quadruple-mode frequency characteristics results in very wide frequency range from 6.3GHz to 59.4GHz. If these results are amended by the divider-based multiplexing technique in [15], lower-side frequency range below 6GHz can be easily covered. It means, most existing frequency bands until 60GHz might be covered through the combination of this proposed work and the previous lower-side multiplexing technology. But since the LC tuning range of the VCO core is narrow, the frequency range multiplied is wide. Further works are required to solve these problems

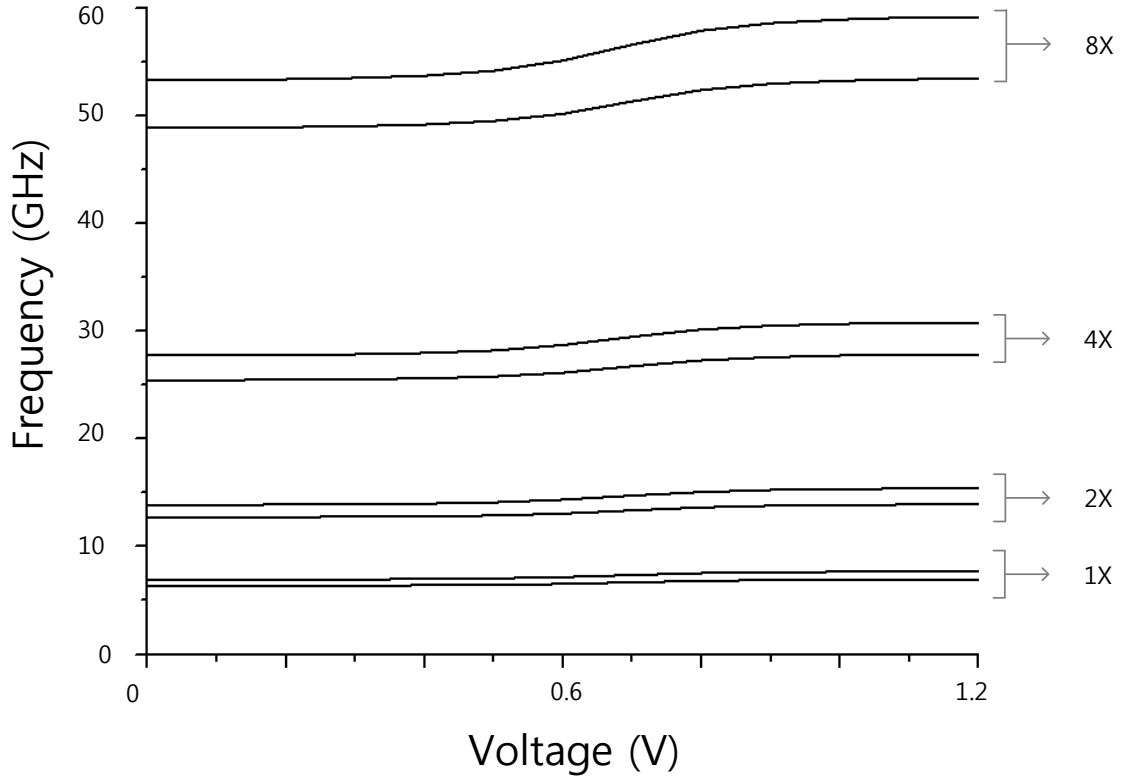


Figure 3.5 Frequency characteristic of a prototype signal generator

3.3.2 Output spectrum & Phase noise of signal generator

Output spectrum and phase noise results are shown in fig 3.6. The signal of VCO core is 1X frequency, which is not measured because the output ports of VCO core are not designed. However, the frequency multiplier is used for VCO core such that if without the VCO core, the signal generator doesn't operate. Accordingly, VCO core frequency can be assumed, and the core frequency, by applying the equation of diving twofold (2X) frequency by two. For this reason, these measured spectrum results only involve twofold (2X), quadruple (4X), and octuple (8X) output spectrums. Phase noise is -96.4dBc/Hz at 1MHz offset from 12.7GHz carrier. With a 1.2V supply, its power dissipation is from 35.2 to 53.5 mW. Each unit VCO consumes 6.2 mW and overall power changes depending on the operating mode since the corresponding number of active unit VCOs is adapted. This work was compared with previous works in Table I, where it can be known that this work would be one of successful wideband design methods.

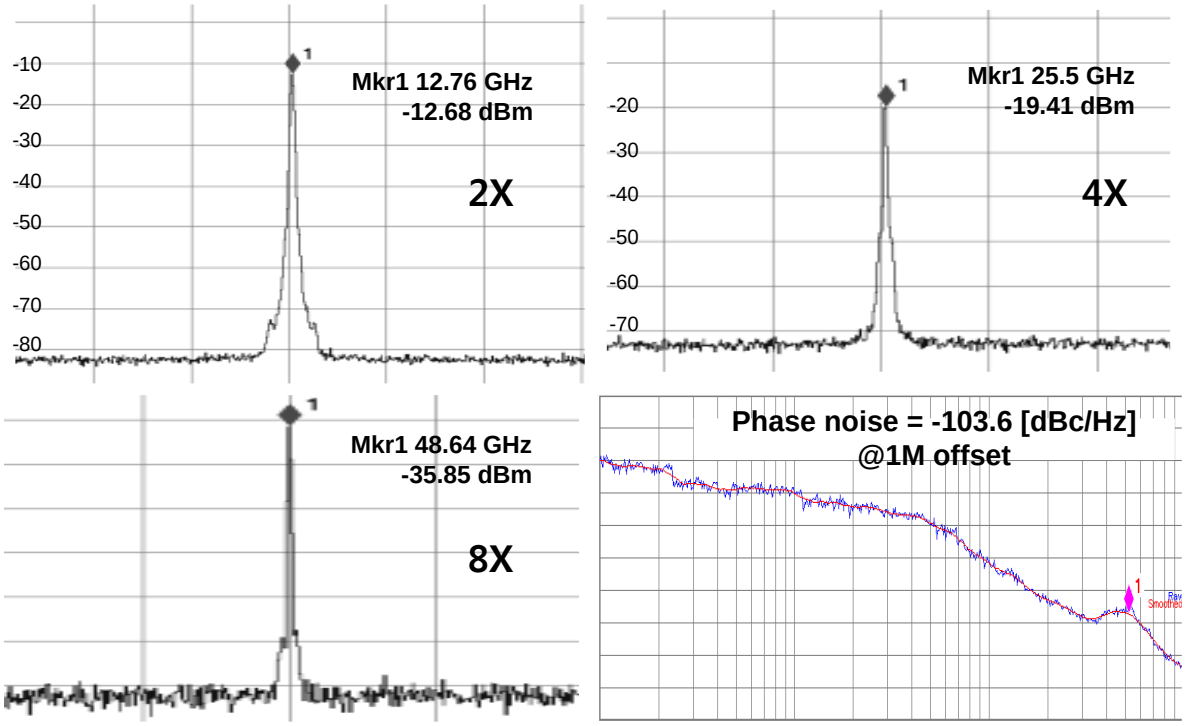


Figure 3.6 Measured 2x/4x/8x output spectrums of signal generator & phase noise from 12.8GHz carrier frequency

Ref	Frequency (GHz)	Circuit Topology	PDISS (mW)	Tech
[10]	64.8-71	VCO Only (Tuable vararctor)	5.4	65nm SOI
[11]	52-58	VCO+ Push-Push structure	10	130nm CMOS
[12]	57-63	VCO+ Frequency tripler	36	65nm CMOS
[13]	57.5-90.1	VCO Only (Switching transformer)	8.4/11	65nm CMOS
This work	**6.3-60.8 Quadruple band**	**VCO + Programmable multiplier**	**8/30**	**65nm CMOS**

Table 3-1. Comparison of CMOS Signal generators

Chapter IV

Future Works

4.1 New Structure of VCOs

In order to provide twofold (2X), quadruple (4X) and N-fold (NX) frequency bandwidths feasible in the frequency multiplier, the frequency bandwidth of VCO core should be two times the oscillation frequency. For such high frequency bandwidths, the need for another VCO structure is required. This paper is to explain and propose the structure of such a VCO as an alternative.

The structure design which the paper proposes is shown in fig 4.1, the design is designed with the quadrature type[20] made of two major VCOs, which consist of the two minor VCOs designed in an in-phase structure. The minor VCOs structured in in-phase determines Z value by using transformer inductor and changes the direction of the current to control mutual inductance, so much as to offer wideband frequency bandwidths [21]. Also, the two major VCOs designed in the quadrature type structure, through reconfigurable method, can generate two or four phase signals. Therefore, frequency multiplier can generate twofold (2X) or quadruple (4X) frequency signals. Using such a structure together with the multiple array cap structure can design the multi-phase quadrature wideband VCOs using the transformer inductor, which are feasible to generate at least two times more of frequency bandwidth than the oscillation frequency. Therefore, designing a signal generator using a new type structure of VCO and a frequency multiplier can support the whole existing wireless frequency bandwidths.

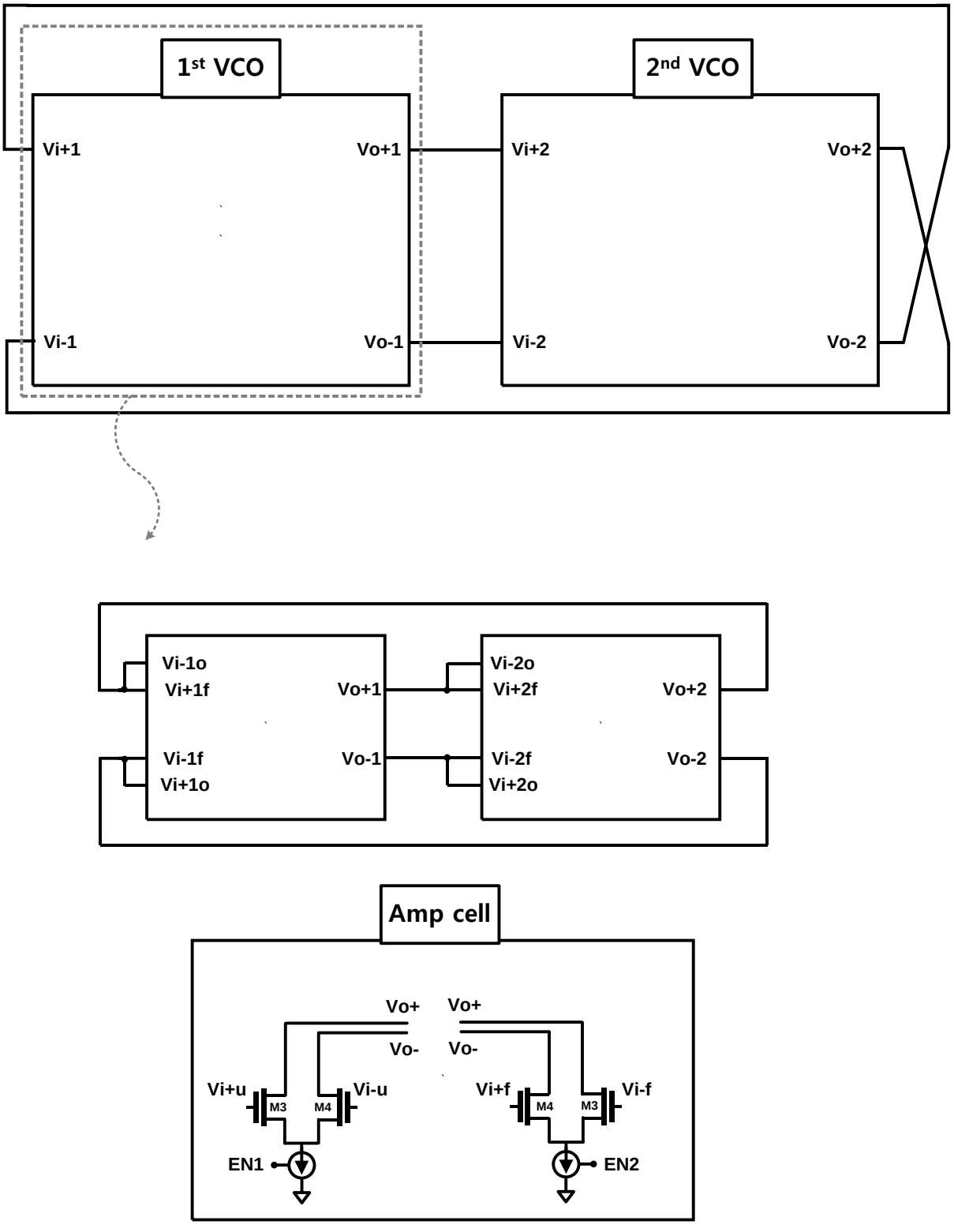


Figure 4.1 Concept of new design VCOs

Chapter V

Conclusion

The paper deals with the design of an Ultra wideband signal generator and the concepts of the VCO, the most important device for the design of a signal generator. It involves understanding of LC resonance, the minimal gm of MOSFET, phase noise and how to minimize the phase noise, and the design method. Also, the structure for multi-phase signal generation is explained. Finally, understanding the concept of frequency multipliers, which is the most important contribution of this paper, leads to the method to design such a multiplier, which gives the understanding of the way to generate VCO core (1X), twofold(2X), quadruple(4X),…, and N-fold(NX) frequency bandwidths by applying a programmable structure.

All the processes to design the schematic with a cadence tool, to the layout with a virtuoso tool, and to the fabrication with TSMC 65nm process are utilized to obtain experimental results, which leads to designing a ultra wideband signal generator which can generate at most 6-60GHz wideband frequency bandwidths. The first version of Signal generator, signal generator of wire bonding type using the concept of tunable linear superposition was proposed and experimentally verified to expand the existing wideband technology limit of signal generators. With a four-stage LC-ring VCO and a programmable frequency synthesis circuit, the tunable linear superposition concept was implemented, which can provide the programmable frequency multiplication. If LC tank circuits are modified to include many variable capacitor arrays like [2-3], the whole frequency range from 5GHz to 30GHz would be continuously covered. Also if this signal generator includes conventional CMOS frequency dividers which are known to work well in the frequency range of the prototype VCO, it might cover the whole existing frequency bands below 30GHz. Second version of signal generator, A fully-integrated CMOS wideband signal generator is presented. A reconfigurable frequency-synthesis structure was proposed and experimentally verified to have very wide frequency characteristic of 6–60GHz and also have optimal power consumption which is adaptively optimized for various operating modes. Considering CMOS frequency dividers are working well below 6GHz, this work is supposed to be one of meaningful advancement for supporting the whole existing wireless frequency bands until 60GHz.

The results suggest the feasibility of designing a more capable wideband signal generator and a more complete version of ultra wideband signal generator through the continuous efforts of additional researches.

Appendix

1. Varactor diode

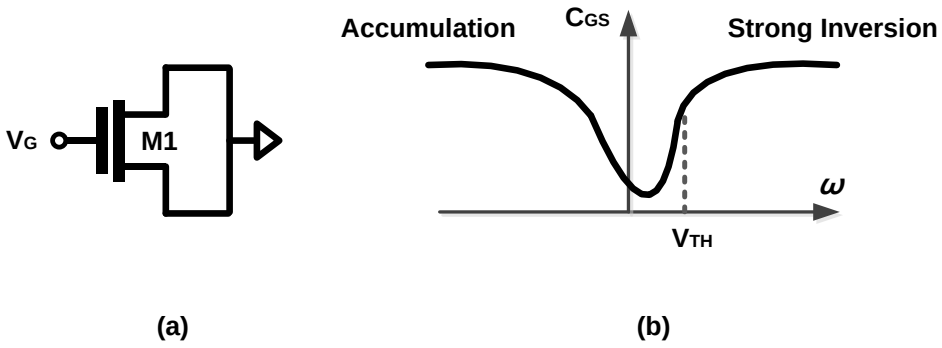


Figure A1. (a) Schematic of varactor diode (b) Capacitance-voltage characteristic of an NMOS device

2. VCO using NMOS & PMOS cross coupled pairs

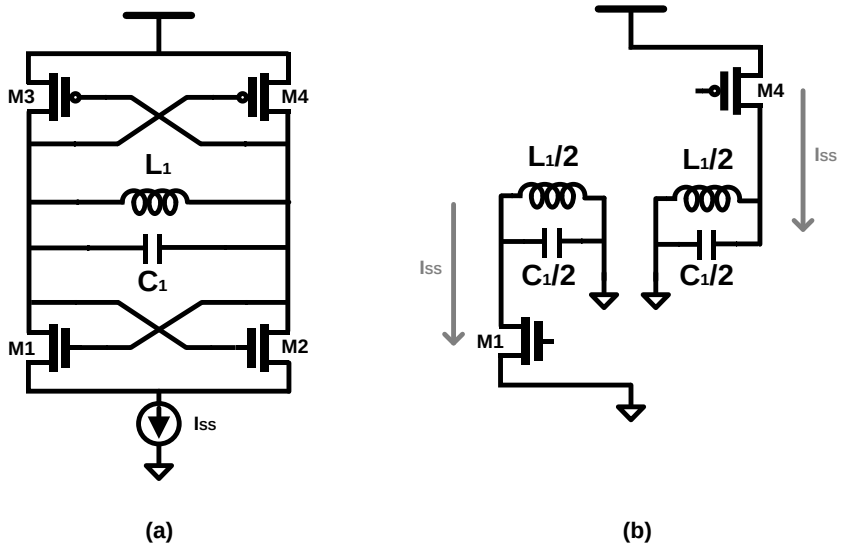
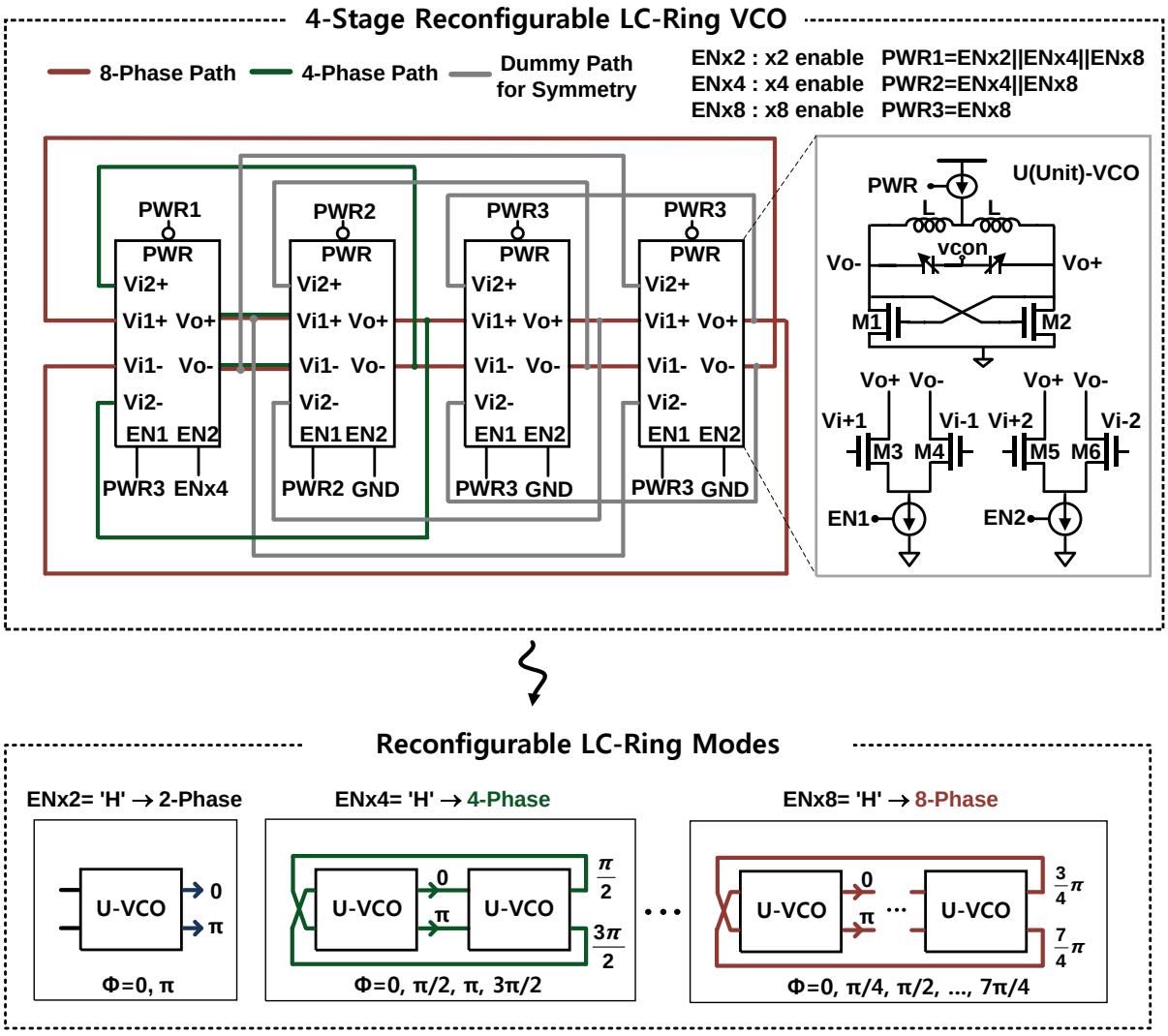


Figure A2. (a) Schematic of VCO using NMOS and PMOS cross coupled pairs, (b) Current flow through floating resonator when M1 and M4 are on

3. N-Phase Reconfigurable LC Ring controller



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