Tunnel Junction-Embedded Field-Effect Transistor for Negative Differential Resistance and Its Multi-Valued Logic and Memory Applications

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Tunnel Junction-Embedded Field-Effect Transistor for Negative Differential Resistance and Its Multi-Valued Logic and Memory Applications

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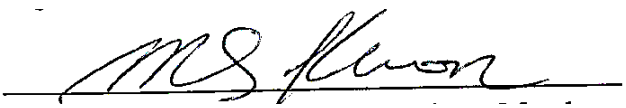

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Abstract

I propose a novel negative differential resistance (NDR) device with ultra-high peak-to-valley current ratio (PVCR) by combining *pn* tunnel diode with transistor. The embedded transistors suppress the valley current with transistor off-leakage current level. With various configurations of *pn* diode and transistor, single or multiple NDR characteristics obtained and each operation principle is explained clearly. Each composed device is analyzed in detail and NDR characteristics are examined device design parameters. In the single NDR case, operation voltage is below 0.5V, which is good at power density. In the multiple NDR case, band-to-band tunneling (BTBT) in tunnel junction provides the first peak, and second peak and valley are generated from the suppression of diode current by off-state transistor. For the digital applications, introduced tri-state voltage transfer circuit makes NDR device take single input operation. Moreover, by using complementary multiple NDR devices, 5-state memory is demonstrated only with four transistors.

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Nomenclature

BTBT	Band-to-band tunneling
CMOS	Complementary metal-oxide-semiconductor
DC	Direct current
GAA	Gate all around
JFET	Juntion field-effect transistor
JL	Junctionless
JLFET	Juntionless field-effect transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
MVL	Multi-valued logic
MVM	Multi-valued memory
NDR	Negative differential resistance
***n*NDR**	*n*-type negative differential resistance
***p*NDR**	*p*-type negative differential resistance
NQS	Non-quasi-static
PVCR	Peak-to-valley current ratio
QS	Quasi-static
RF	Radio frequency
RITD	Resonant interband tunneling diode
RTD	Resonant tunneling diode
SCE	Short channel effect
SNW	Silicon nanowire
SPICE	Simulation program with integrated circuit emphasis

SS	Subthreshold swing
TAT	Trap-assisted tunneling
TCAD	Technology computer-aided design
VJL	Vertical junctionless
WF	Workfunction

Chapter 1

Introduction

The negative differential resistance (NDR) devices are promising alternative device performing multifunctional operation based on its nonmonotonic behavior. Moreover multiple NDR devices offer much promise by reducing circuit complexity and enhancing the performance in terms of chip area and power consumption, taking full the advantages of single NDR devices. In this thesis, I propose novel NDR devices with single and multiple NDR characteristics and demonstrate its superiority compared with previous works.

1.1 Negative Differential Resistance Devices

The NDR device which has negative slop in certain region of the I-V curve as shown in Fig. 1-1 are innovative device for multi-valued logic (MVL) and memory (MVM) applications, oscillators, amplifiers, and neuromorphic network in terms of speed, power, and density. By virtue of its potential capacities, there are many device and circuit researches described how to produce NDR characteristics. In early research, it was found in arc discharge device and vacuum tube device with dynatron exhibit NDR effects [1]. After progressing in solid-state technology, NDR characteristics could be practical. Of the solid-state device, quantum tunneling diodes (called tunnel diode or Esaki diode; first discover of NDR characteristics in solid state technology with heavily doped *pn* junction based no germanium material [2]) and resonant tunneling diode (RTD) have received most attention.

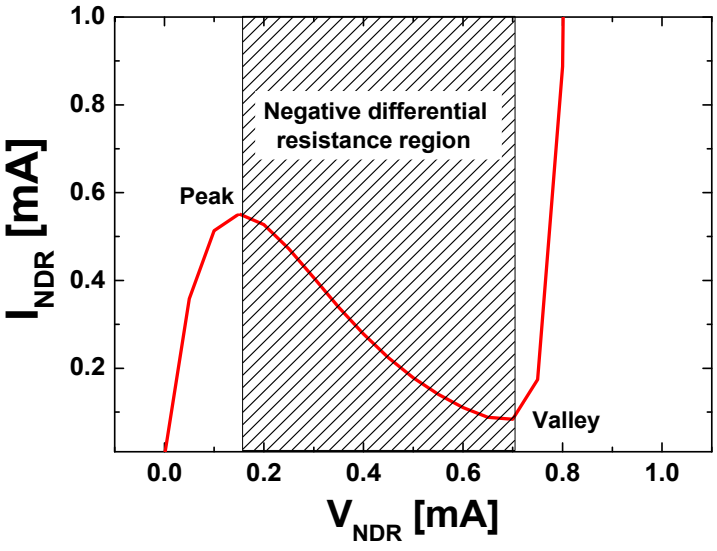


Figure 1-1: The negative differential resistance characteristics.

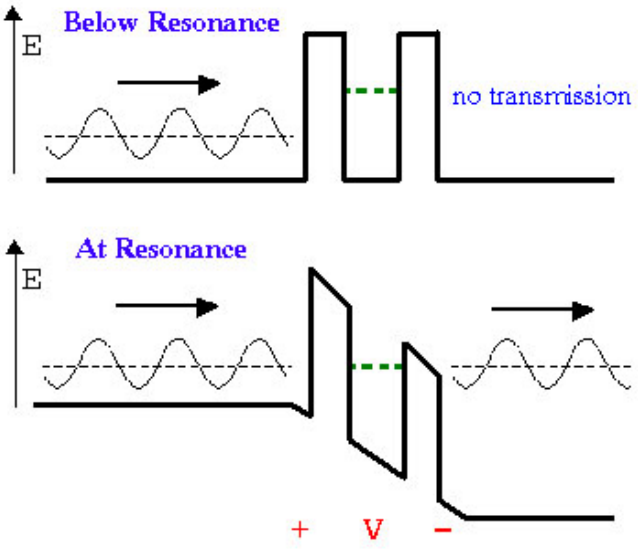


Figure 1-2 The operation principled of resonant tunneling diode, which figure is refer at nanoHub [3]

In this thesis, *pn* tunnel diode is used in part of proposed device for silicon based simple structure and it has further discussion in section II. Figure 1-2 shows the operation principle of RTD device [3]. In RTD devices, quantum well surrounded by very thin layer barriers is formed and carriers have only discrete energy values inside the quantum well. When a voltage is applied across the RTD, resonance between transmission and reflection can be happen so that carriers can tunnel through some resonant state at discrete energy level.

However, those devices have been in problem for practical applications from two perspectives. First, the III-V materials for RTD device are not compatible with complementary metal-oxide-semiconductor (CMOS) technology and its device has low peak-to-valley current ratio (PVCR). Second, tunnel diode with Si or SiGe material which is compatible with CMOS process has also low PVCR below 10 by the trap-assisted tunneling (TAT) current through the forbidden band-gap [4, 5]. Therefore, many researches focused on the improvement of PVCR over 100 based on the metal-oxide-semiconductor field-effect transistor (MOSFET) structure instead of simple tunnel diode. Enhanced surface generation in SiGe-based gated diode is exploited for PVCR of 300 around at 3V [6, 7]. Other works show the PVCR over 1000 with breakdown mechanism of gate bipolar device in MOSFET structure [8, 9]. Recently, some research succeed to obtain high PVCR at relatively low operation voltage by suppressing transistor on current at the off-leakage with another depletion mode MOSFET [10] or inverter circuits [11]. In terms of the multiple NDR characteristics for MVL/MVM applications, however, it needs more complicated circuit for 4-state logic at 3V [12]. In other multiple NDR-based MVL/MVM applications, the series connection of resonant interband tunneling diode (RITD) with double peaks based on InAs/AlSb/GaSb at 1.5V [13] or Si/SiGe at 3V [14].

1.2 Our Approach

In this thesis, I propose novel single and multiple NDR devices with ultra-high PVCR over 10^6 at 1V, based on tunnel junction-embedded filed-effect transistor, which suppress the valley current with transistor off-leakage level. In the multiple NDR devices, band-to-Band tunneling (BTBT) in tunnel junction provides the first peak, and the second peak and valley are generated from the suppression of diode current by the off-state transistor. Therefore, embedded transistor has a primary role for peak and valley currents and ultra-high PVCR. By using gate all around (GAA) silicon nanowire (SNW) transistor which has high gate controllability, transistor's ability is improved. Through comparison between carrier injection mechanisms, variety device configuration can be organized. Moreover, I generalize propose multiple NDR device in conventional MOSFET structure for practical applications. Figure 1-3 shows the conceptual schematic and symbol of proposed NDR device based on MOSFET structure. These multiple NDR characteristics can be controlled by doping concentration of tunnel diode and threshold voltage of embedded transistors. In the latch circuit for MVL/MVP applications, by introducing tri-state voltage transfer circuit, compact design with minimum cell size is feasible. In the complementary multiple NDR devices, 5-state memory is demonstrated only with four transistors.

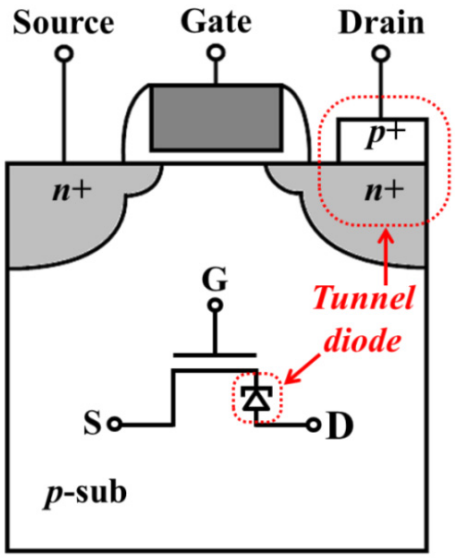


Figure 1-3. Conceptual schematic and symbol of propose NDR device based on tunnel junction-embedded MOSFET

1.3 Thesis Overview

In the introduction, I reviewed the previous work of other research groups and bring up a topic. A general concept and outline were expressed. In section II, the vertical junctionless (VJL) GAA SNW

field-effect-transistor is introduced for embedded transistor, which has superior gate controllability and low subthreshold swing (SS). And in section III, I applied concept of our NDR device to conventional MOSFET. In the sub-section of II and III, each constituting devices of proposed NDR are analyzed and device operation principle is described with energy band diagrams. In addition, the effects of device design parameters on NDR are presented. By using only 4 devices, 5-state latch circuit simulation is demonstrated for MVL/MVM applications in section IV. The future works are presented in section V, finally, a summary and conclusion follow in section VI. This thesis based on my accepted papers in journal and conferences [15-18].

Chapter 2

NDR Device based on Nanowire Junctionless Field-Effect-Transistor and PN Tunnel Junction

The vertical junctionless (VJL) silicon nanowire (SNW) field-effect transistor (FET) as embedded transistor of proposed NDR device is considered from DC to RF characteristics and *pn* tunnel junction is reviewed in-depth. At the end of this chapter, proposed NDR device structure, operation principle and variety NDR characteristics with different carrier injection mechanism are presented.

2.1 Vertical Junctionless Silicon Nanowire Field-Effect-Transistor

The scaling limit of the CMOS commands a new type of device. To avoid the short channel effects (SCEs) and increase gate controllability, various attempts have been made as shown in Fig. 2-1, and GAA SNW structures have received much attention [19–25]. In the nanowire CMOS, however, challenges for making an abrupt source and drain junction profile have been faced. The junctionless (JL) device has been proposed as a solution to junction induced problems [26–29]. According to these viewpoints, JL SNW FETs can be a breakthrough for the problems of conventional CMOS devices. The VJL SNW FET has merits in relatively simple fabrication and high device density [30-34].

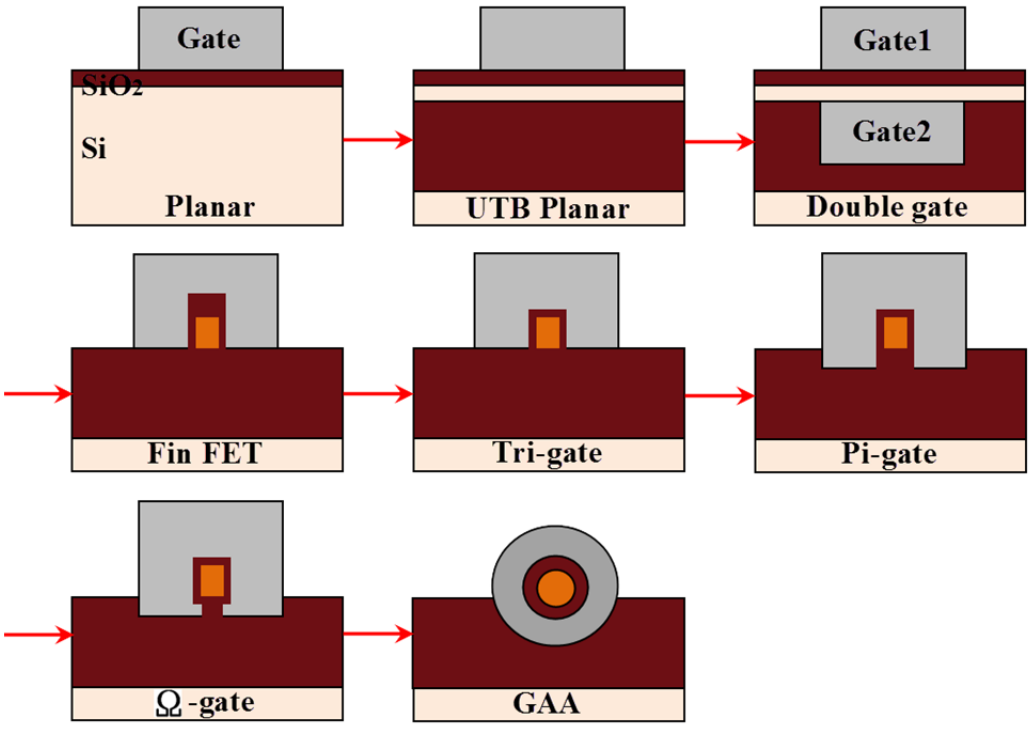


Figure 2-1. Progression of device structure

2.1.1 Device Structure and Operation Principle

The JLFET has no junction between channel and source/drain region and its operation principle is similar to the junction field-effect transistor (JFET). In the JFET, the gate voltage varies the depletion width of a junction. Figure 2-2 shows the simplified cross-sectional view and device operation of JFET. The JFET has heavily doped *p*+ region and lightly doped channel region [36]. At the off state channel region is fully depleted by *pn* junction. When depletion width decreases owing to positive bias, current can flow through the opened channel. At the high drain voltage, channel is pinch-off as shown in Fig. 2-2(c) and current is saturated. The difference between JFET and JLFET is that JLFET has only heavily doped channel. A 3D schematic view and 2D cross-sectional view for JL SNW FET

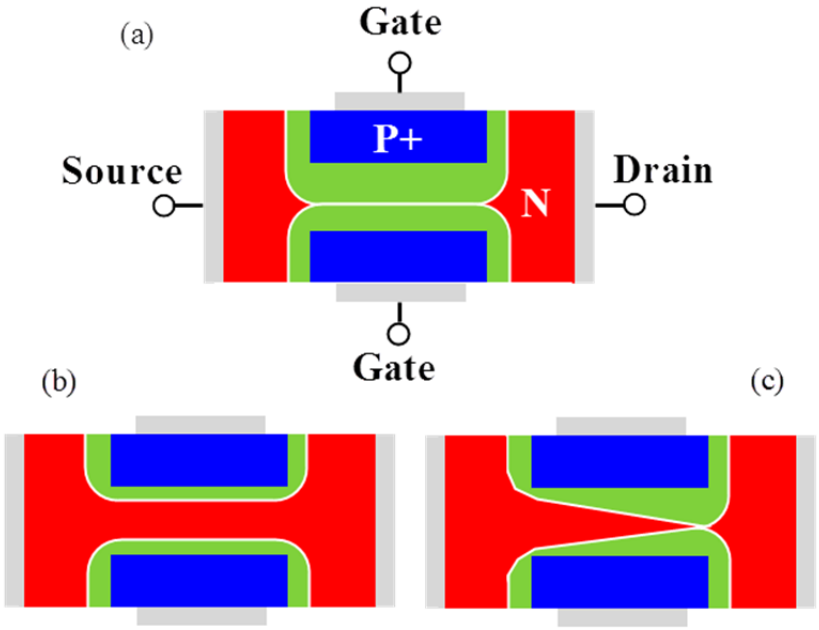


Figure 2-2. The 2D cross-sectional schematic view and device operation of JFET [36]: (a) off state, (b) on state with low V_{DS}, and (c) pinch-off state at high V_{DS}

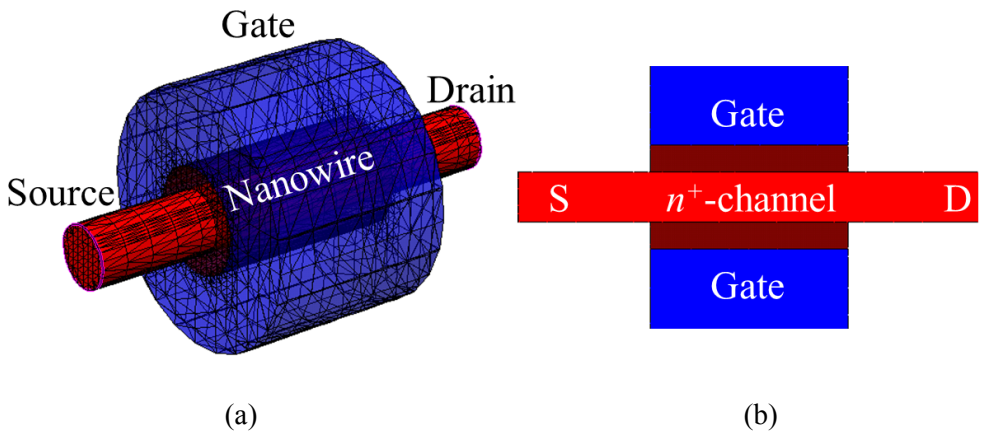


Figure 2-3. Device schematic of JL SNW FET: (a) 3D schematic view and 2D cross-sectional view

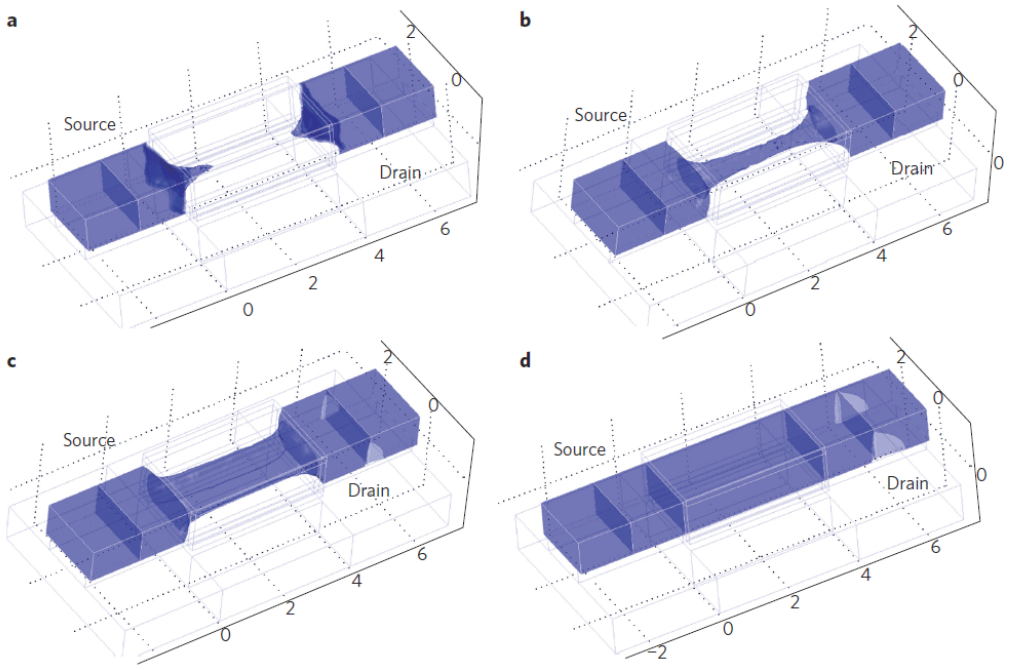


Figure 2-4. Electron concentration of n-type JLFET at different gate voltage [37]: (a) $V_G<V_{TH}$, (b) and (c) $V_G=V_{TH}$, and (d) $V_G= V_{FB} >V_{TH}$

are shown in Fig. 2-3(a) and (b), respectively. For fully depleted channel at off state, SNW should be thin and narrow. Compared with MOSFET, the JLFET and JFET have volume conduction, i.e. currents flow through the body. In Fig 2-4 shows the electron concentration of *n*-type JLFET at different gate voltage (V_G) [37]. When V_G is lower than threshold voltage (V_{TH}), channel region is fully depleted owing to work function difference between gate and SNW. At the $V_G=V_{TH,}$ a string shaped channel of connects source and drain. As V_G increased, the channel expands and has become a simple resistor at the flat band voltage (V_{FT}), i.e. $V_G= V_{FB} >V_{TH}$.

A 3D schematic view of VJL SNW FET is shown in Fig. 2-5. In the case of vertical SNW FETs, the substrate-related components are connected only to the drain side. The VJL SNW FET was designed with a gate length (L_G) of 30nm and channel diameter (D_n) of 10nm, and gate oxide thickness (T_{ox}) of 3.5nm. The *p*-type doping concentration of the substrate is $5\times10^{15}cm^{-3}$ and the *n*-type doping concentrations of channel and S/D regions are $2\times10^{19}cm^{-3}$. To investigate the substrate effect, three different substrate thicknesses were chosen, and will be referred to as the device without substrate (w/o Sub.), device with a relatively small substrate thickness (Thin Sub., T_{si}=60 nm), and device with a relatively large substrate thickness (Thick Sub., T_{si}=896.5nm). Except the T_{si}, all of the design values are the same in w/o Sub., Thin Sub., and Thick Sub. Device simulation is performed using a Sentaurus Device 3D simulation tool. In the 3D technology computer-aided-design (TCAD) simulations, a Shockley–Read–Hall model and a band-to-band tunneling model were added to consider the recombination, generation, and tunneling in a highly doped channel.

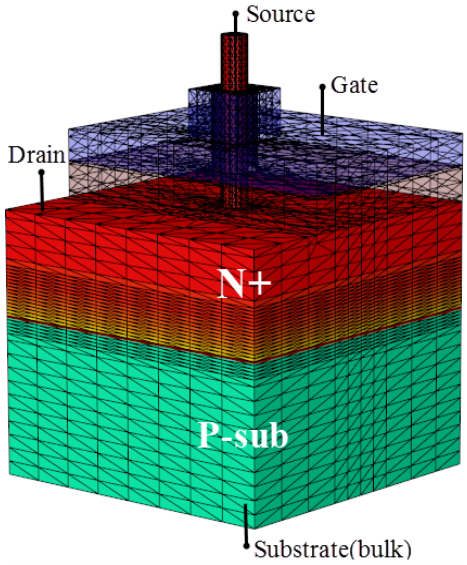
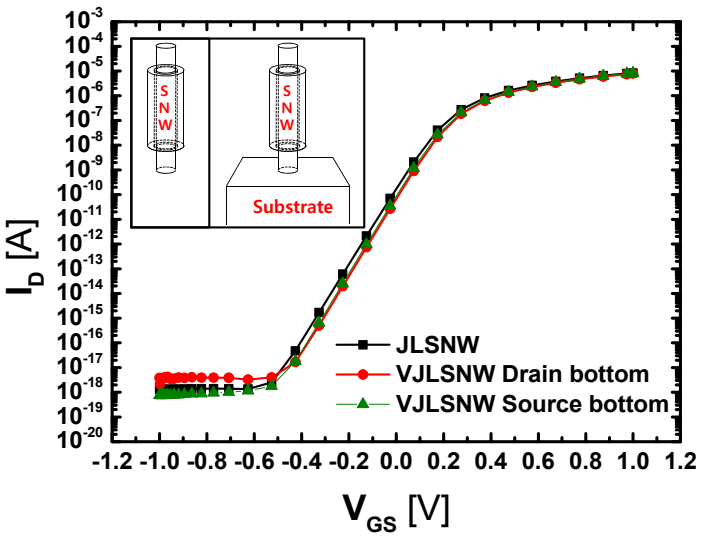


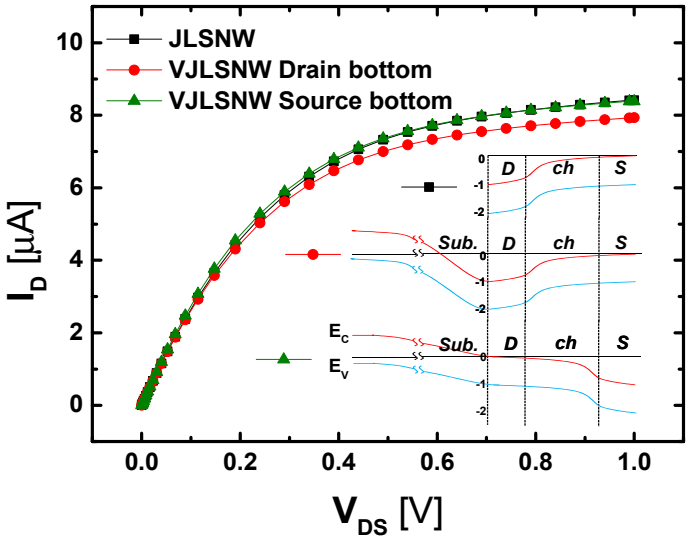
Figure 2-5. 3D schematic view of VJL SNW FET

2.1.2 DC characteristics

Figure 2-6 shows DC characteristics in the VJL SNW and JL SNW. In principle, the VJL SNW FET with the source bottom structure, when the bottom electrode is assigned to the source, shows exactly the same DC curves as the JL SNW FET. In Fig. 2-6(a), the off-current of the VJL SNW FET with the drain bottom structure is larger than that of the JL SNW FET owing to the leakage current through the *pn* junction between the drain and the substrate. In Fig. 2-6(b), the on-current of the VJL SNW FET with the drain bottom structure is smaller than that of the JL SNW FET owing to the current distribution through the substrate. The electric field between the drain and substrate influences the DC characteristic of the VJL SNW. In the VJL SNW FET with the drain bottom case, the threshold

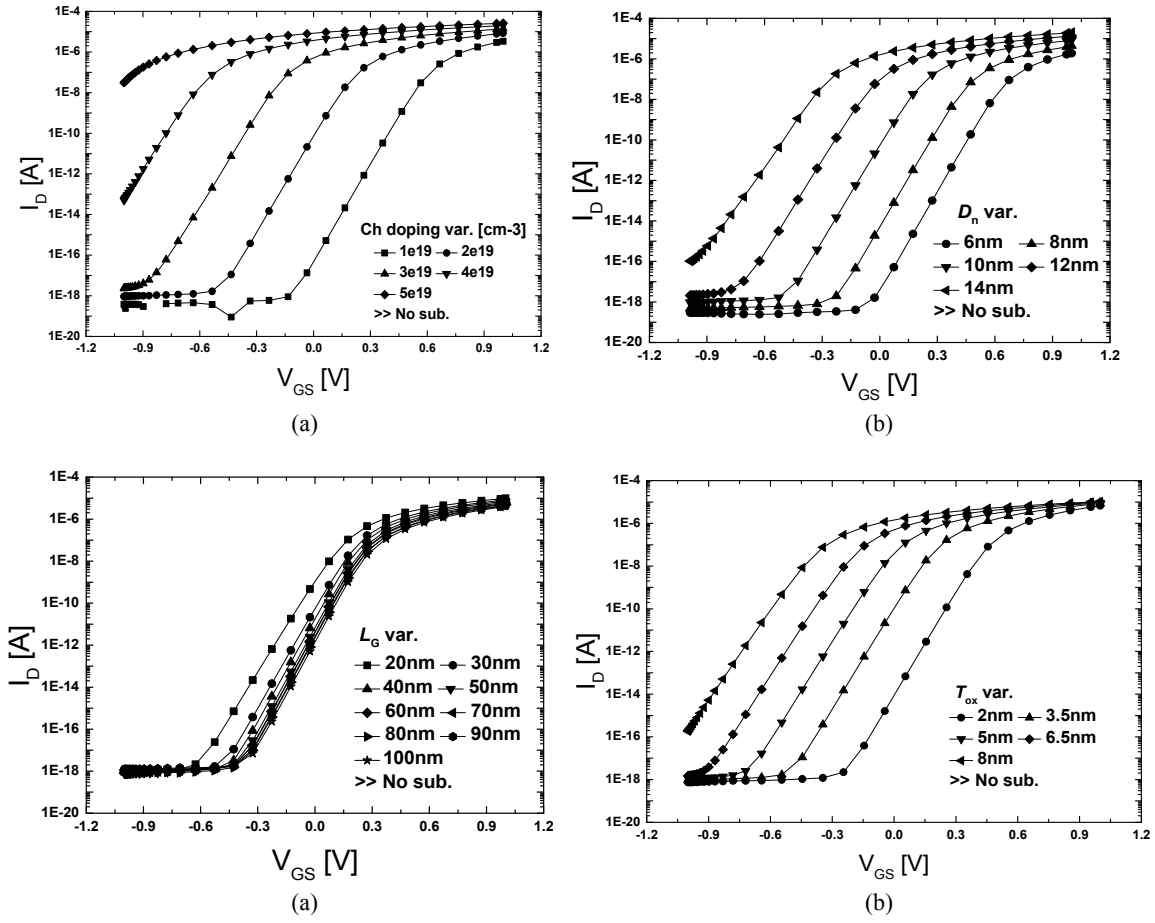


(a)



(b)

Figure 2-6. DC characteristic in VJL SNW FET with drain bottom and source bottom structure and JL SNW FET: (a) I_D-V_{GS} curves with structures and (b) I_D-V_{DS} curves and band diagrams



(a) (b)

(a) (b)

Figure 2-7. I_D-V_{GS} characteristics of JL SNW FET with various design parameters: (a) JL doping concentration, (b) diameter of NW, (c) channel length, and (d) gate oxide thickness

voltage (V_{th}) is 0.21 V, using a constant current method at 100 nA, and the subthreshold swing (SS) is 78.7 mV/decade. To investigate the effect of design parameters on device, additional test was done in I_D-V_G characteristics. Figure 2-7 shows that when NW has thick, short, high doping concentration, and smaller T_{ox}, higher current flow but off current couldn't be grabbed.

2.1.3 RF characteristics

The scaling of CMOS has result in a strong improvement in the RF performance [38]. Consequently, CMOS has become a variable option for analog RF application and RF system-on-chip. Recently, studies of MOSFET and JL SNW FET for RF application have been reported. However, no investigation of the substrate-related components in RF regime such as the substrate resistance (R_{sub}) and drain-to-substrate capacitance (C_{sub}) of VJL SNW FETs has been reported yet. For accurate RF modeling of the realistic VJL SNW FETs, substrate-related parameters are important in the high-frequency operation regime [39–43]. In this part, we propose an extraction method of R_{sub} and C_{sub} of VJL SNW FETs and investigate the substrate effects in the high-frequency regime based on rigorous three-dimensional (3D) device simulation. An analytical extraction of parameters has been performed using Y-parameter analysis on the quasi-static (QS) small signal model, which is good enough to extract the substrate-related parameters of vertical devices accurately in the off-state regime, even though our previous work used the non-quasi-static (NQS) model in terms of the model accuracy for the intrinsic parameters [44].

A 2D cross-sectional view of VJL SNW FET in Fig. 2-5 is shown in Figs. 2-8(a). In the case of vertical SNW FETs, the substrate-related components are connected only to the drain side, while those

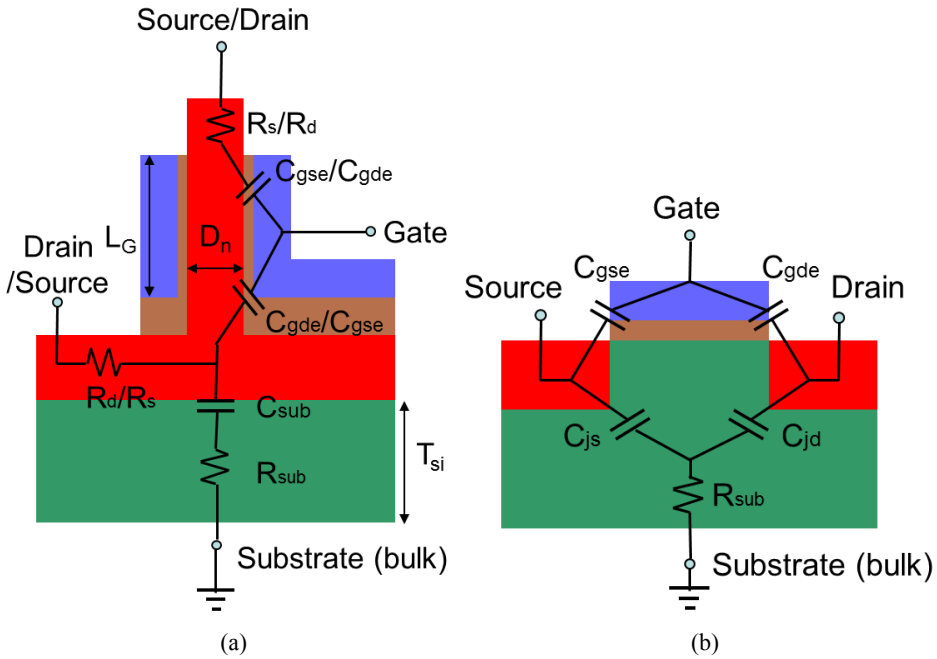


Figure 2-8. 2D cross sectional view with small signal model: (a) VJL SNW FET and (b) conventional MOSFET

of planar MOSFETs are connected to both the source and drain sides by junction capacitances, as shown in Fig. 2-8(b). Therefore, the extraction method for R_{sub} and C_{sub} has to be different from the conventional method [45].

Quasi-static small signal model

Figures 2-9(a) and 2-9(b) show the off-state QS model of the VJL SNW FET with substrate components, C_{sub} and R_{sub}, for drain bottom and source bottom structures, respectively [46]. Using small signal components in Fig. 2-8(a), the equivalent circuit at the off-state can be derived as in Fig. 2-9(a). C_{gde} and C_{gse} are the extrinsic gate-to-drain and gate-to source capacitances, respectively. C_{sub} is the drain-substrate junction capacitance. R_s, R_d, and R_{sub} are the source, drain, and substrate resistances in sequence. In the case of devices with the source bottom structure, substrate-related components have negligibly small effects on RF performance as well as DC current characteristics (Fig. 2-6). This will be discussed later by using extracted parameters. The parameter extraction and

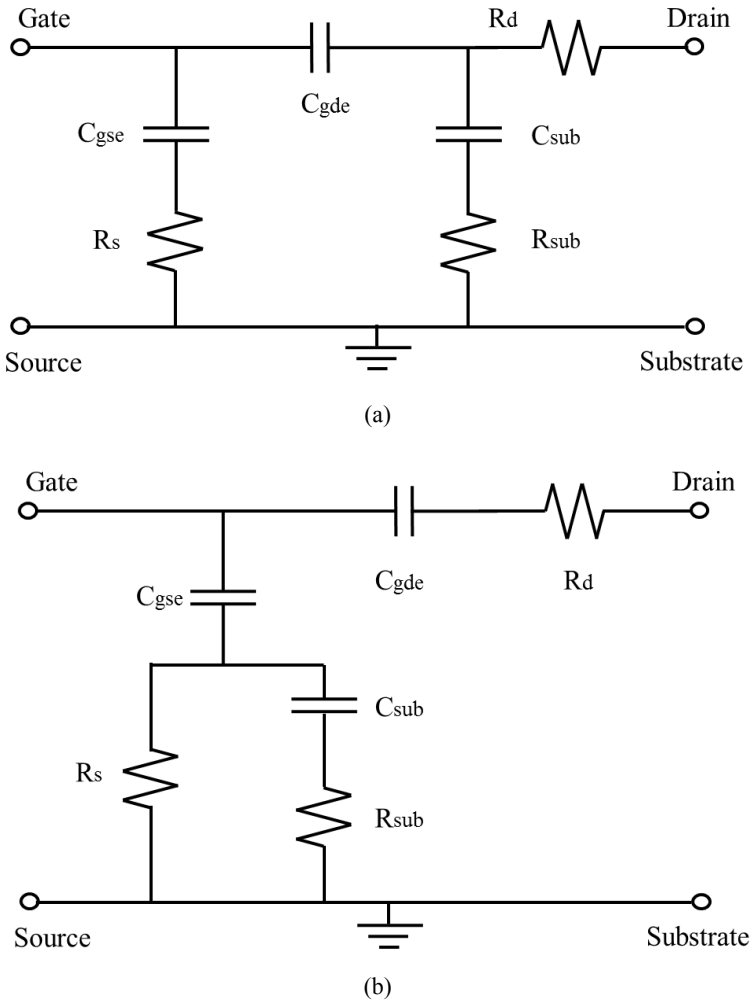


Figure 2-9. Quasi-static small signal model of VJL SWN FET at an off state (V_{GS}=0V). (a) Drain bottom structure. (b) Source bottom structure

modeling in this work focus mainly on the VJL SNW FETs with the drain bottom structure when the bottom electrode is assigned as the drain. For the VJL SNW FETs with the drain bottom structure, the equivalent circuit at the off-state can be analyzed in terms of Y-parameters as follows:

$$\mathrm{Y}_{11} = \omega^2\left(\mathrm{C}_{gse}{}^2 R_s + \mathrm{C}_{gde}{}^2 R_d\right) + j\omega\left(\mathrm{C}_{gde} + \mathrm{C}_{gse}\right), \tag{1}$$

$$\mathrm{Y}_{12} = -\omega^2\left(\mathrm{C}_{gde} R_d (C_{sub} + \mathrm{C}_{gde})\right) - j\omega \mathrm{C}_{gde}, \tag{2}$$

$$\mathrm{Y}_{21} = -\omega^2\left(\mathrm{C}_{gde} R_d (C_{sub} R_{sub} + \mathrm{C}_{gde})\right) - j\omega C_{gde}, \tag{3}$$

$$\mathrm{Y}_{22} = \omega^2\left(\mathrm{C}_{sub}{}^2 R_{sub} + R_d\left(\mathrm{C}_{sub} + \mathrm{C}_{gde}\right)^2\right) + j\omega\left(\mathrm{C}_{sub} + \mathrm{C}_{gde}\right). \tag{4}$$

Model parameters R_s, R_d, R_{sub}, C_{gde}, C_{gse}, and C_{dsub} can be expressed by the following equations:

$$R_d = \frac{\mathrm{Re}(\mathrm{Y}_{12})}{\omega^2 C_{gde}(C_{sub} + C_{gde})}, \tag{5}$$

$$R_s = \frac{\mathrm{Re}(\mathrm{Y}_{11}) - \omega^2 C_{gde}{}^2 R_d}{\omega^2 C_{gse}{}^2}, \tag{6}$$

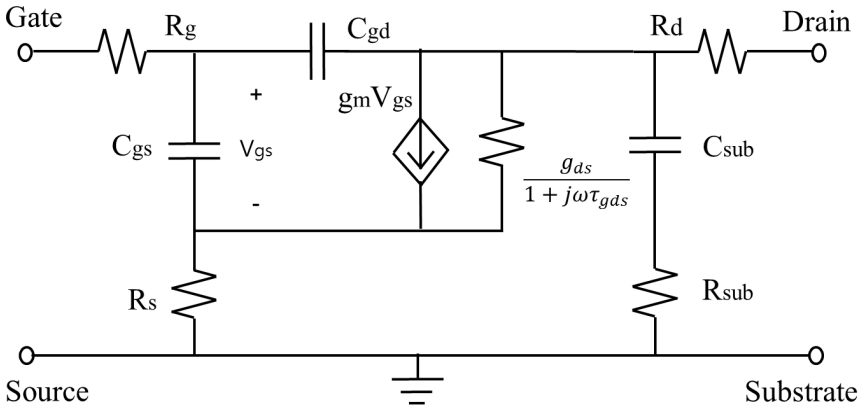
$$R_{sub} = \frac{\mathrm{Re}(\mathrm{Y}_{22}) - \omega^2 R_d (C_{sub} + C_{gde})^2}{\omega^2 C_{sub}{}^2}, \tag{7}$$

$$C_{gde} = -\frac{\mathrm{Im}(\mathrm{Y}_{12})}{\omega}, \tag{8}$$

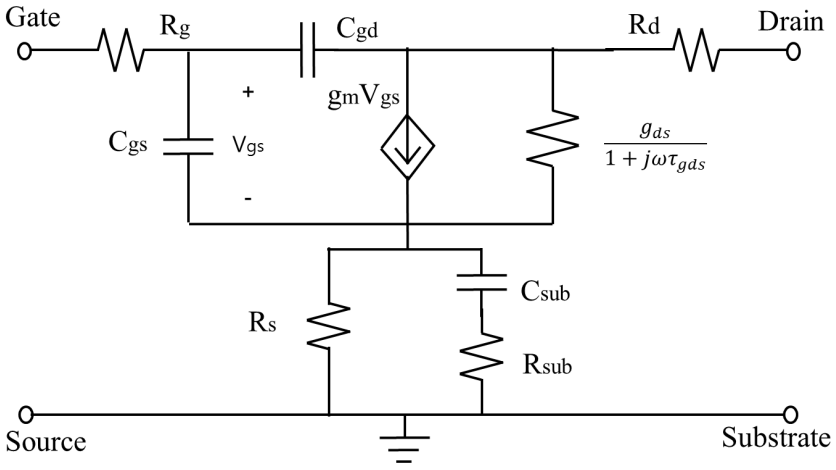
$$C_{gse} = \frac{\mathrm{Im}(\mathrm{Y}_{11}) + \mathrm{Im}(\mathrm{Y}_{12})}{\omega}, \tag{9}$$

$$C_{sub} = \frac{\mathrm{Im}(\mathrm{Y}_{22}) + \mathrm{Im}(\mathrm{Y}_{12})}{\omega}. \tag{10}$$

Figure 2-10 shows the equivalent circuit at the strong inversion region ($V_{GS} > V_{th}$). R_g is the effective gate resistance, which consists of the gate electrode resistance and the distributed channel resistance. This R_g in Fig. 2-10 represents only the distributed channel resistance in the on-state regime owing to the negligibly small gate electrode resistance as in our previous work with metal gate assumption [44]. Therefore, the off-state RF model in Fig. 2-9 can neglect the effective gate resistance



(a)



(b)

Figure 2-10. Quasi-static small signal model of VJL SWN FET in strong inversion region ($V_{GS} > V_{th}$): (a) Drain bottom structure. (b) Source bottom structure

component since there is no distributed channel resistance owing to the absence of the inversion layer in the off-state regime [47]. The values of R_s, R_d, R_{sub}, C_{gde}, C_{gse}, and C_{sub} are extracted at the off-state. After de-embedding the off-state parameters, R_s, R_d, R_{sub}, C_{gde}, C_{gse}, and C_{sub}, the equivalent circuit components at the on-state can be analyzed in terms of Y-parameters as follows:

$$\mathrm{Y}_{11} = \omega^2 R_g\left(\mathrm{C}_{gd} + \mathrm{C}_{gs}\right)^2 + j\omega\left(\mathrm{C}_{gd} + \mathrm{C}_{gs}\right), \tag{11}$$

$$\mathrm{Y}_{12} = -\omega^2 R_g \mathrm{C}_{gd}\left(\mathrm{C}_{gd} + \mathrm{C}_{gs}\right) - j\omega \mathrm{C}_{gd}, \tag{12}$$

$$Y_{21} = g_m - \omega^2 R_g \mathrm{C}_{gd}\left(\mathrm{C}_{gd} + \mathrm{C}_{gs}\right) - j\omega C_{gd}, \tag{13}$$

$$Y_{22} = g_{ds} + \omega^2 R_g C_{gd}^{\ 2} + j\omega(C_{gd} - g_{ds}\tau_{gds}) \quad (14)$$

As shown in Fig. 2-10 and eq. (14), the drain conductance (g_{ds}) with delay (τ_{gds}) has been considered based on the NQS formalism since it can be significant in the linear region [48]. From eq. (14), we can extract the delay from the imaginary part of Y_{22} as $\tau_{gds} = 1/g_{ds} \times \mathrm{Im}(-Y_{22}/\omega + C_{gd})$. The model parameters of R_g, C_{gs}, C_{gd}, g_m, and g_{ds} can be expressed by the following equations:

$$R_g = \frac{\mathrm{Re}(Y_{11})}{\mathrm{Im}(Y_{11})^2}, \quad (15)$$

$$C_{gd} = -\frac{\mathrm{Im}(Y_{21})}{\omega}, \quad (16)$$

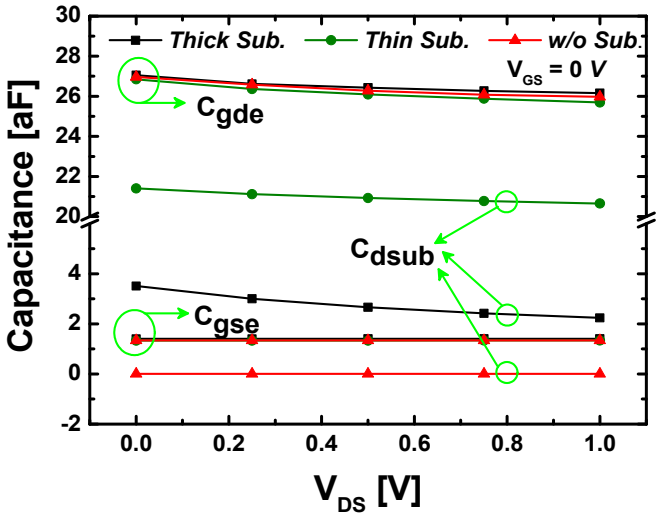
$$C_{gs} = \frac{\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12})}{\omega}, \quad (17)$$

$$g_{ds} = \mathrm{Re}(Y_{22})|_{\omega^2=0}, \quad (18)$$

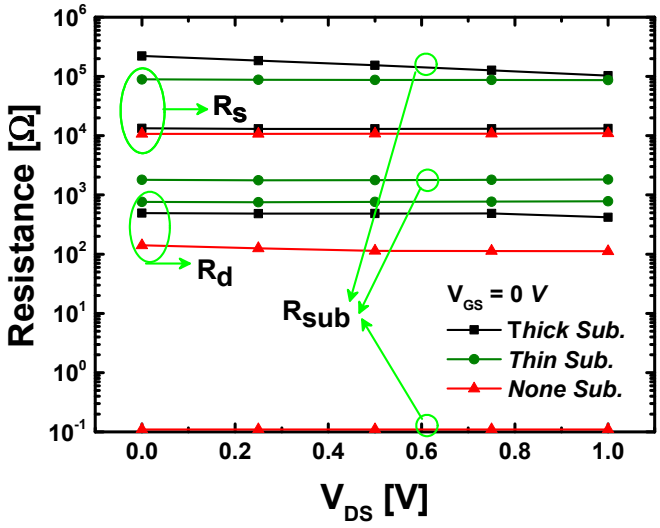
$$g_m = \mathrm{Re}(Y_{21})|_{\omega^2=0}. \quad (19)$$

Using the extracted values of capacitance, resistance, and conductance, the f_t, f_{max}, and transport delay (τ) of the channel charge can be derived. To verify the model, the result from HSPICE circuit simulation using parameters extracted from eqs. (5)–(10) and (15)–(19) will be compared with the device simulation result.

Result and discussion The Y-parameters can be extracted by 3D device simulation and the complete quasi-static small signal parameters are extracted using the method described in the previous section. Figure 2-11 shows the small-signal parameters at the off-state and compares the result with different T_{si}. In Fig. 2-11(a), C_{sub} decreases as V_{DS} increases owing to the expansion of the depletion width between the drain and the substrate. C_{sub} has also been influenced by T_{si}. The w/o Sub. case has no junction capacitance between the drain and the substrate. In the case of Thin Sub., we chose the substrate thickness so that the *p*-type substrate is fully depleted before reaching its expected width and full depletion width can be obtained owing to low substrate doping concentrations [49]. Therefore, C_{sub} of the Thick Sub. case is smaller than that of the Thin Sub. case. On the other hand, C_{gde} and C_{gse} are maintained as nearly constant values despite the different T_{si} and V_{DS}. In Fig. 2-11(b), R_{sub} decreases with the increase in V_{DS} and the decrease in T_{si} because the current path length through the



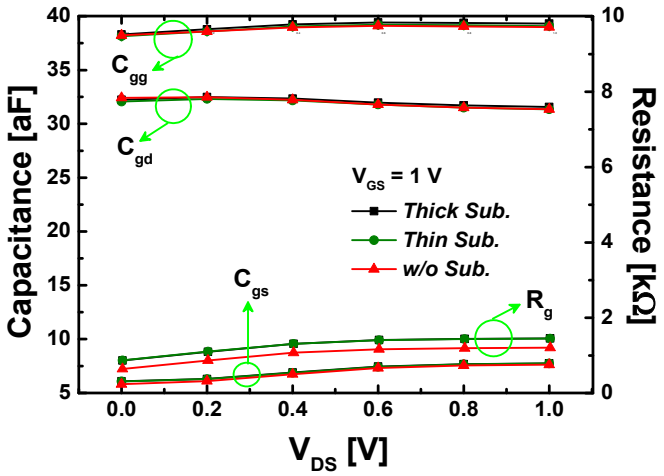
(a)



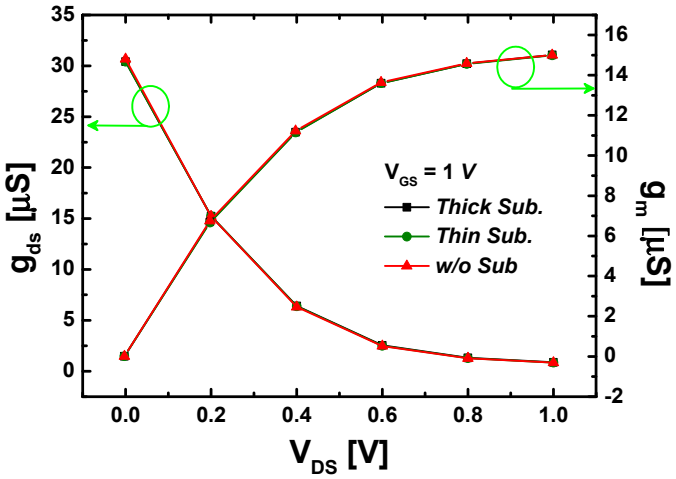
(b)

Figure 2-11. Smal-signal parameter extraction results of VJL SNW FETs with Thick Sub., Thin Sub., and w/o Sub. at an off state: (a) $C_{gde}/C_{gse}/C_{sub}$ and (b) $R_{sub}/R_s/R_d$

substrate is reduced by the expansion of the depletion width, while R_s and R_d are kept as constant values. Figure 2-12 shows the small signal parameters in the strong inversion region (V_{GS} = 1 V). The capacitance, resistance, and conductance show little change with the variation of T_{si} in the on-state. In Fig. 2-12(a), C_{gd} is larger than C_{gs} at V_{DS} = 0V owing to the parallel capacitance with a relatively thick oxide between the drain and gate, as shown in Fig. 2-5. When V_{DS} increases, C_{gd} decreases owing to the reduction of charge at the near drain side, whereas C_{gs} increases owing to the increase in charge at the near source side. At the saturation voltage, C_{gd} and C_{gs} remain constant. The total gate input capacitance (C_{gg}) is simply extracted by the summation of C_{gd} and C_{gs}. In Fig. 2-12(b), the trans-conductance g_m and conductance g_{ds} show the current drivability. Using the extracted parameters, the



(a)



(b)

Figure 2-12. Small-signal parameter extraction results of VJL SNW FETs with Thick Sub., Thin Sub., and w/o Sub. in strong inversion region: (a) $C_{gg}/C_{gd}/C_{gs}/R_g$ and (b) g_m/g_{ds}

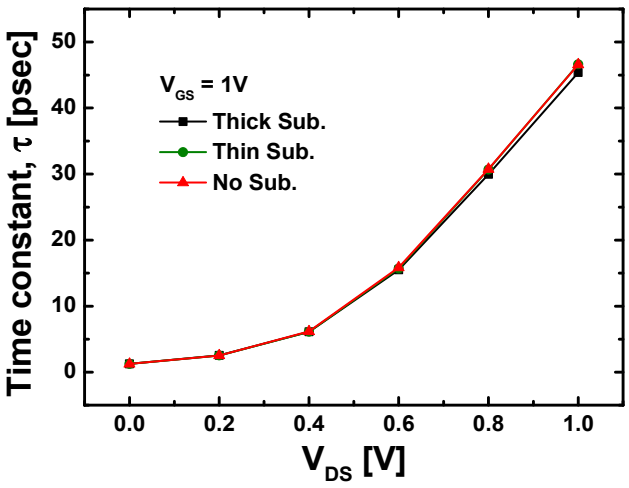


Figure 2-13. Time constant according to V_{DS} and T_{si}

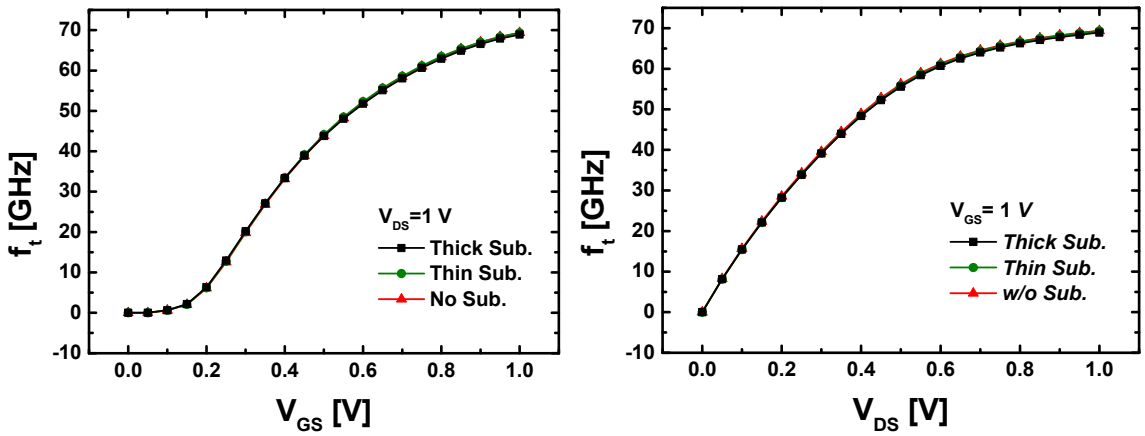


Figure 2-14. Cut-off frequency with variations of T_{si}: (a) gate voltage V_{GS} and (b) drain voltage V_{DS}.

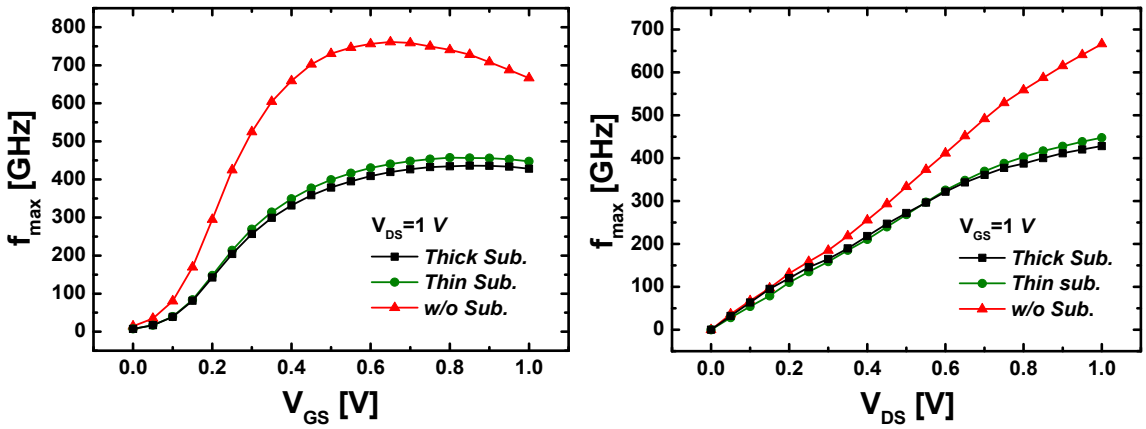


Figure 2-15. Maximum oscillation frequency with variations of T_{si}: (a) gate voltage V_{GS} and (b) drain voltage V_{DS}

transport delay (τ) of channel charge can be calculated by $C_{gg}\times V_{DD}/I_d$, as shown in Fig. 2-13, which indicates that T_{si} has no effect on τ since the gate capacitance and channel resistance remain constant with various T_{si} values [46]. To estimate the RF performance, f_t and f_{max} are considered in Figs. 2-14 and 2-15, respectively. In 3D device simulation, f_t and f_{max} are extracted using the *dBPoint* method, which has extrapolation of experimental data to the unit gain point [50]. In Fig. 2-14, f_t remains constant with various T_{si} values. On the other hand, f_{max} results in a significant difference between the devices with and without a substrate owing to substrate-related component effects, as shown in Fig. 2-15. The parameters for VJL SNW FETs at V_{GS} = 1V are summarized in Table I. In the case of the VJL SNW FETs with the source bottom structure, the effect of R_{sub} and C_{sub} is generally very small. The impedance caused by R_s, R_{sub}, and C_{sub} in Fig. 4(b) can be expressed as follows:

$$Z = \frac{R_s \cdot \sqrt{[1+\omega^2 C_{sub}^2 R_{sub}(R_{sub}+R_s)]^2 + \omega^2 R_s^2 C_{sub}^2}}{1+\omega^2 C_{sub}^2 (R_{sub}+R_s)^2}$$

Table I. Values of the parameters for VJL SNW FETs with the drain bottom structure operating at the strong inversion region.

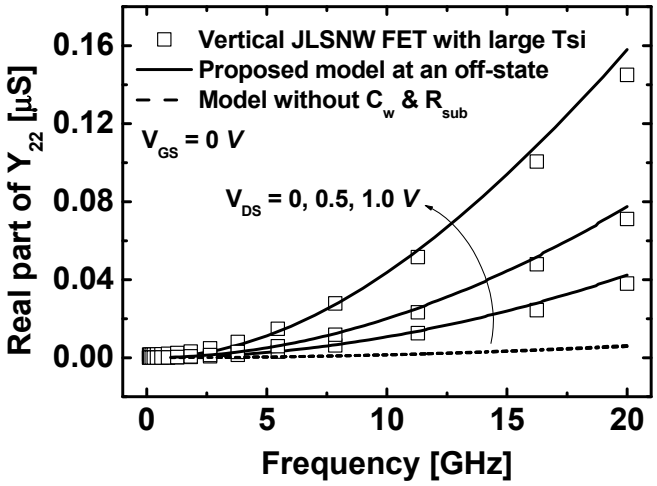
Device	JL SNW FET on *Thick Sub.*		JL SNW FET on *Thin Sub.*	
Drain bias @ $V_{GS}=1V$	$V_{DS}=1V$	$V_{DS}=0.5V$	$V_{DS}=1V$	$V_{DS}=0.5V$
R_g (Ω)	1454	1375	1472	1388
C_{gd} (aF)	31.58	32.17	31.45	32.07
C_{gs} (aF)	7.15	7.76	7.13	7.19
g_m (μS)	15	12.63	13.98	12.62
g_{ds} (μS)	0.87	3.97	0.84	3.92
C_{dsub} (aF)	2.24	2.66	2.06	2.06
R_{sub} (Ω)	103k	154k	1820	1780
R_s (Ω)	13.2k	13k	86.8k	87.3k
R_d (Ω)	419	485	781	761
$_{gds}$ (ps)	14.6	17.5	14.4	17.4

Table II. Values of the ω^2-terms for VJL SNW FETs with the source bottom structure.

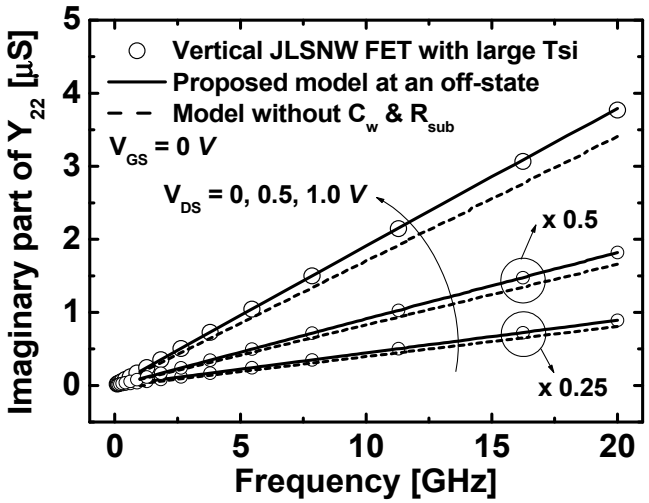
Device	JL SNW FET on *Thick Sub.*		JL SNW FET on *Thin Sub.*	
Drain bias @ $V_{GS}=1V$	$V_{DS}=1V$	$V_{DS}=0.5V$	$V_{DS}=1V$	$V_{DS}=0.5V$
$\omega^2 C_{sub}^2 R_{sub}(R_{sub}+R_s)$ at 100 GHz	2.11×10^{-2}	6.65×10^{-2}	7.93×10^{-6}	7.58×10^{-2}
$\omega^2 R_{sub}^2 C_{sub}^2$ at 100 GHz	2.10×10^{-2}	6.63×10^{-2}	5.55×10^{-6}	5.31×10^{-2}
$\omega^2 C_{sub}^2 (R_{sub}+R_s)^2$ at 100 GHz	2.12×10^{-2}	6.67×10^{-2}	1.13×10^{-5}	1.08×10^{-2}

The values of $\omega^2 C_{sub}^2 R_{sub}(R_{sub}+R_s)$, $\omega^2 R_s^2 C_{sub}^2$, and $\omega^2 C_{sub}^2 (R_{sub}+R_s)^2$ are calculated by the extracted parameters of Table I. Those for the VJL SNW FET with the source bottom structure are summarized in Table II. As shown in Table II, ω^2-terms are much smaller than 1. Therefore, the effect of the substrate-related parameters can be neglected in the VJL SNW FET with the source bottom structure and the effect of R_s is dominant.

To confirm the accuracy of the proposed RF models considering R_{sub} and C_{sub}, the off-state and on-state Y-parameters obtained by HSPICE simulation were compared with the values obtained from 3D



(a)



(b)

Figure 2-16. Model verifications forY_{22}-parameters by using extracted parameters and model of Fig. 2-9 at an off state: (a) real Y_{22} and (b) imaginary Y_{22}

device simulation, as shown in Figs. 2-16 and 2-17, respectively. In addition, the proposed model was verified at the on-state in terms of the S_{22}-parameters by HSPICE simulations. Figure 2-18 shows the comparison between the proposed RF model with R_{sub} and C_{sub} and the model without R_{sub} and C_{sub}. S_{22}-parameters from the proposed model with R_{sub} and C_{sub} (solid line) demonstrate well-matched results with 3D device simulation data (symbol) up to 100GHz in both Thin Sub. and Thick Sub., while the conventional model without considering R_{sub} and C_{sub} (dashed line) cannot reproduce the results of 3D device simulation (symbol) in phase space. The output characteristics of transistors in the RF region can be definitely influenced by R_{sub} and C_{sub}. Therefore, the substrate components should be considered in the realistic vertical SNW devices for the accurate modeling of the RF substrate coupling signal at the output node.

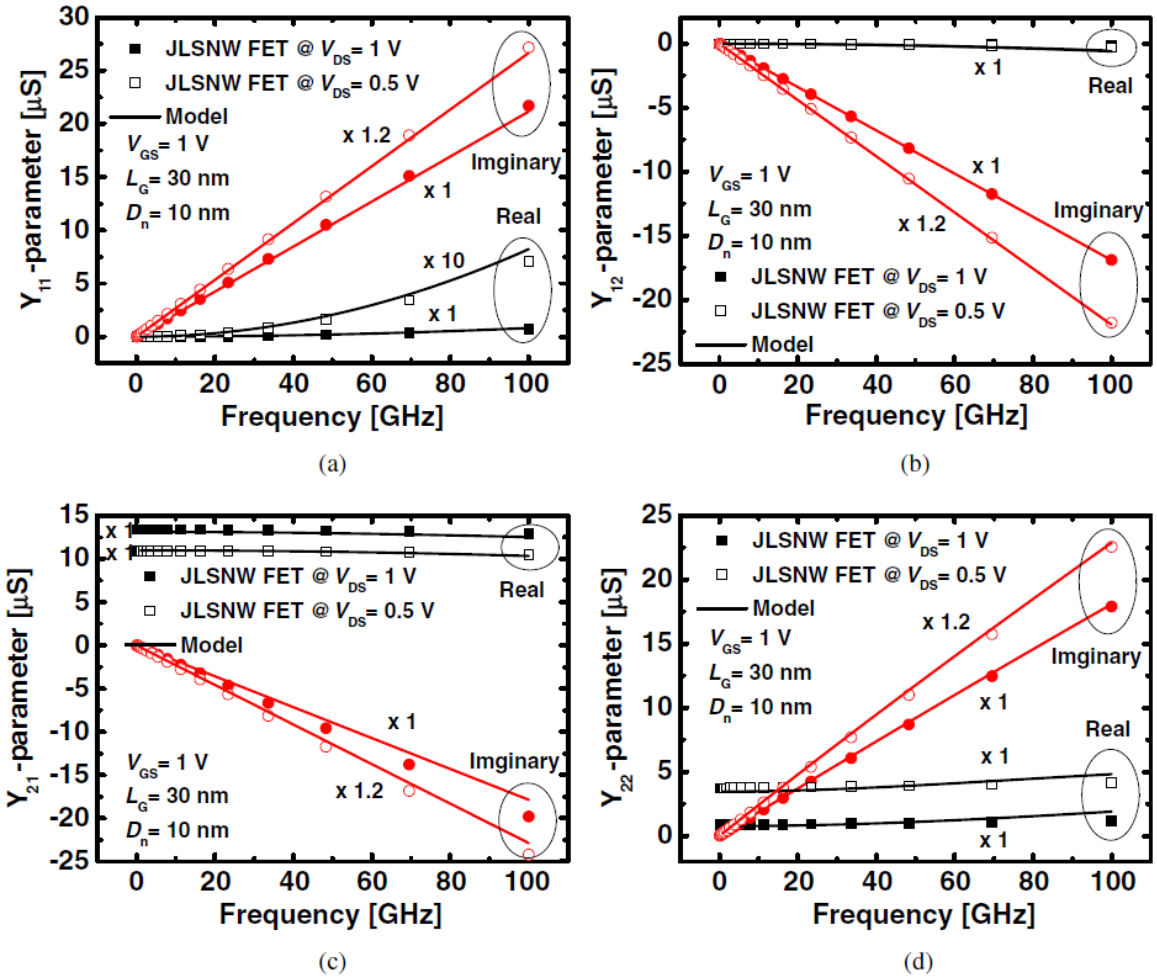


Figure 2-17. Model verifications for Y-parameters by using extracted parameters and model of Fig. 2-10 in strong inversion region: (a) Y_{11} parameter, (b) Y_{12} parameter, (c) Y_{21} parameter, and (d) Y_{22} parameter

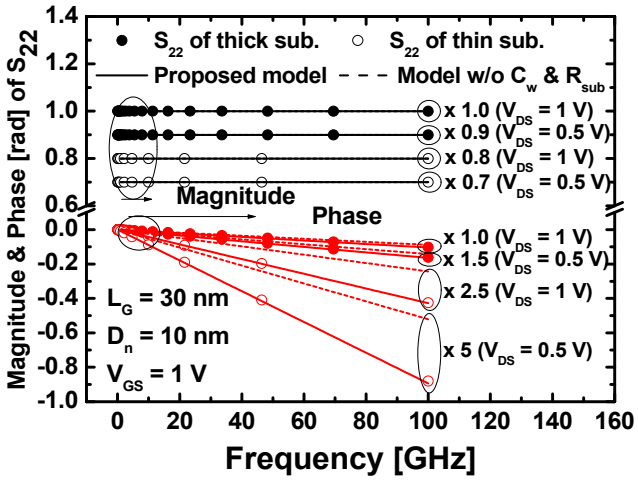


Figure 2-18. Comparison between proposed RF model (solid line) and model without C_{sub} and R_{sub} (dashed line), and 3D simulated (symbol) S_{22}-parameters up to 100GHz at V_{GS}=1.0V

Summary

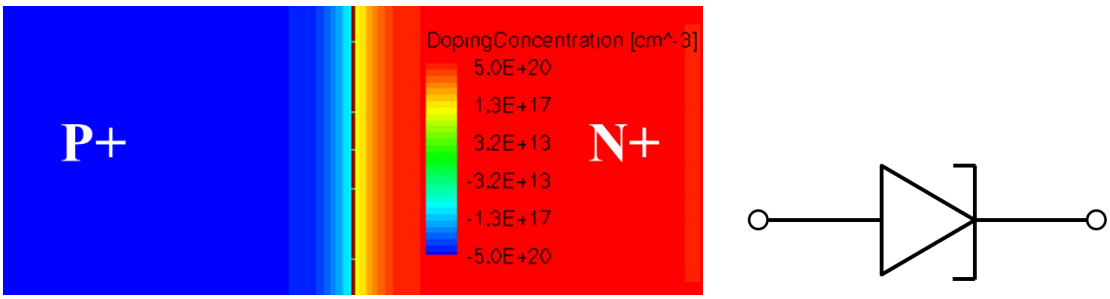
A novel RF model for the VJL SNW FETs with a substrate has been proposed in consideration of the substrate-related components of R_{sub} and C_{sub}. The vertical structure with the inherent substrate effects has been investigated through analyses of model parameters with variation of bias conditions and substrate thickness. The proposed model was well matched with the Y-parameters and the S_{22}-parameter from the 3D device simulation. The results of parameter extraction and model verification have shown that the proposed RF model is accurate and reliable for the description of the substrate effect on the vertical structure.

2.2 PN Tunnel-Junction

A tunnel diode or Esaki diode is a type of semiconductor diode that is capable of very fast operation by using the quantum tunneling phenomenon. A highly doped *pn* junction make very small depletion region and band-to-band tunneling (BTBT) occurs with small forward bias through these depletion region. In addition, tunnel diode exhibit negative differential resistance region and these non-monotonic behavior has the possibility of multifunctional operation.

2.2.1 Device structure and operation principle

Figure 2-19 shows 2D cross-sectional structure and symbol of Esaki tunnel diode which has degenerately doped *pn* junction. Its operation principle can explain with energy band diagram in Fig. 2-20. At steady-state region, conduction band of n-type doped region is below valence band of p-type doped region with very thin depletion width. When small forward bias applied, electrons tunnel from conduction band of n-type region to valance band of p-type region and holes tunnel in reverse



(a) (b)

Figure 2-19. Tunnel diode 2D cross-sectional device schematic (a) and symbol (b)

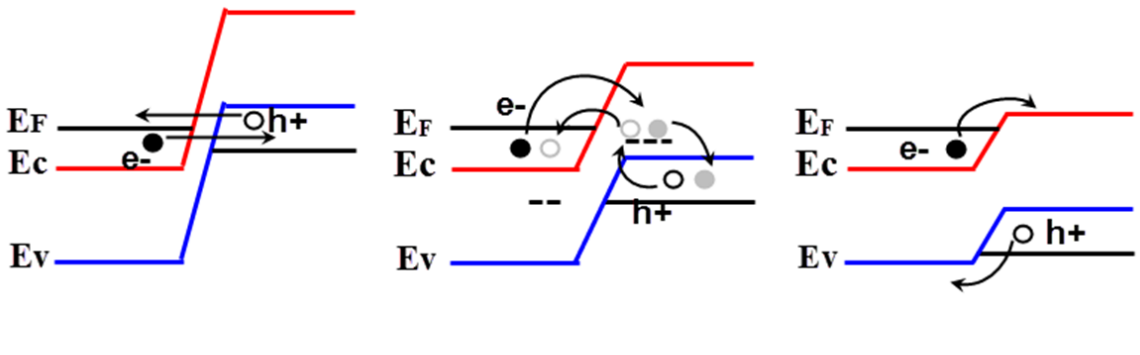


Figure 2-20. Energy band diagram of tunnel diode at different current flow mechanism: (a) band-to-band tunneling, (b) trap-assisted tunneling, and (c) diffusion

direction, which called band-to-band tunneling [Fig. 2-20(a)]. When applied voltage increase further, each band faced with forbidden energy band gap and BTBT current decrease forming peak current and NDR region. However, through the traps in energy band-gap, field-dependent trap-assist tunneling makes valley current [Fig. 2-20(b)]. As voltage increased more, tunnel diode begins to operate as normal diode, where electrons travel by diffusion and no longer by tunneling [Fig. 2-20(c)].

2-2-2. NDR characteristics

Figure 2-21 shows conventional 2-terminal Esaki tunnel diode simulation results which reproduce NDR with realistic valley current owing to TAT with PVCR below 10. In order to use NDR characteristics in real applications, PVCR should be improved over 100. The simulation was performed by using *Sentaurus*™ 3-D TCAD device simulator [51]. To describe BTBT mechanism in

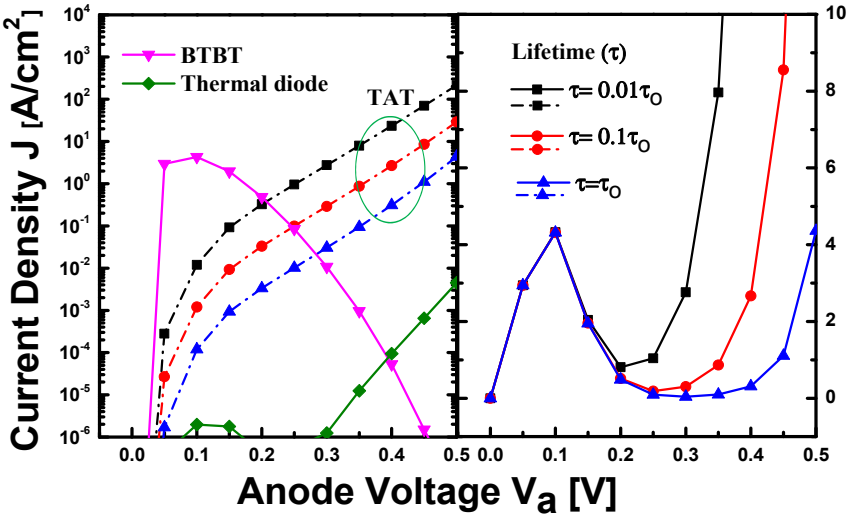


Figure 2-21. J-V characteristics of Esaki tunnel diode with various TAT currents

forward bias of tunnel diode, our numerical BTBT model has been incorporated [52]. For the leakage current behaviors through a forbidden energy band-gap, conventional field-dependent TAT model is used [53].

2.3 Proposed NDR Device

We propose a novel negative differential resistance (NDR) device with ultra-high peak-to-valley current ratio (PVCR) by combining *pn* junction diode with depletion mode nanowire (NW) transistor, which suppress the valley current with transistor off-leakage level. Band-to-band tunneling (BTBT) Esaki diode with degenerately doped *pn* junction can provide multiple switching behavior having multi-peak and valley currents. These multiple NDR characteristics can be controlled by doping concentration of tunnel diode and threshold voltage of NW transistor. By designing our NDR device, PVCR can be over 10^4 at low operation voltage of 0.5 V in a single peak and valley current.

2.3.1 Device structure and operation principle

Figure 2-22(a) and (b) show a three-dimensional (3D) bird's eye view and two-dimensional (2D) cross-sectional schematic of the proposed NDR device, respectively, which is based on the simple

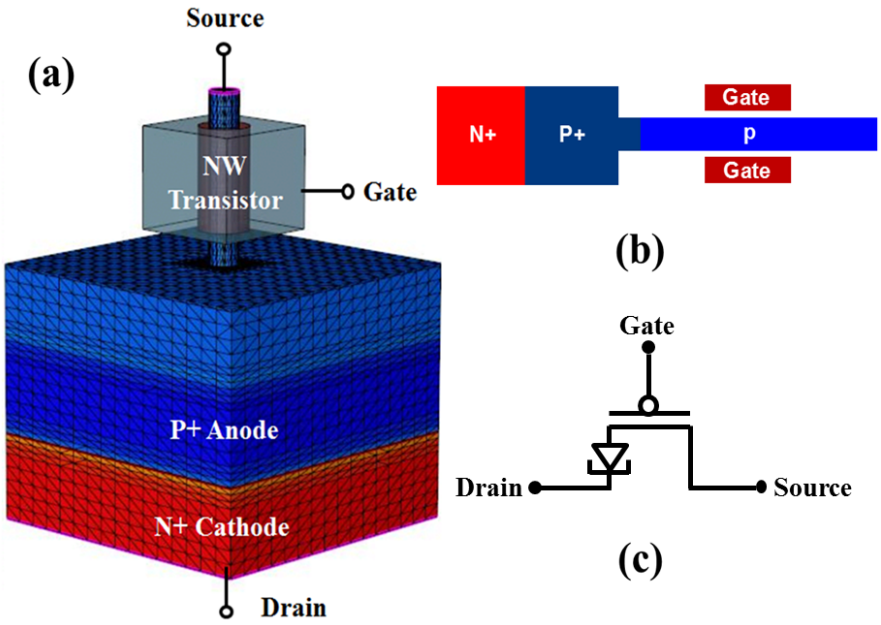


Figure 2-22. Device schematics and circuit symbol of proposed NDR device combined *pn* tunnel junction with *p*-type Si NW transistor: (a) 3D bird's eye view (b) 2D cross-sectional device schematic, and (c) circuit symbol. Si NW transistor controls the carrier (hole) injection from source to diode.

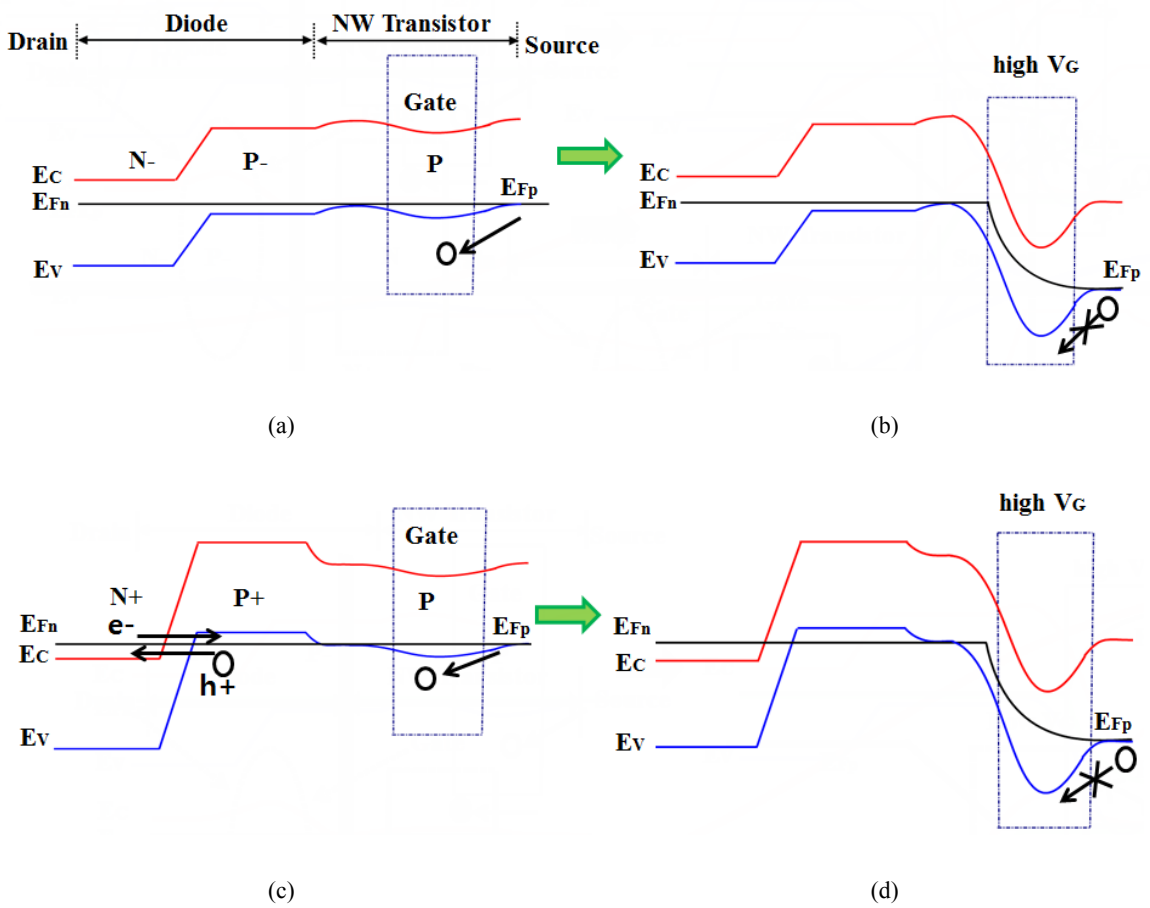


Figure 2-23. Band diagram of NDR device with different doping concentration of diode: (a) Initial band diagram and (b) final band diagram at V_G= 1.6 V and V_S= 1.0 V with low doping device. (c) Initial band diagram and (d) final band diagram at V_G= 1.6 V and V_S= 1.0 V with high doping device.

combination of *pn* tunnel diode and *p*-type Si NW transistor. The circuit symbol of this NDR device can be represented as in Fig. 1(c). The *pn* tunnel diode was designed with both *n*-type and *p*-type doping concentrations of 3×10^{20} cm^{-3} and tunnel junction width of 10nm. The NW transistor had channel radius (R_{ch}) of 5 nm, gate oxide thickness (T_{ox}) of 3.5 nm, and *p*-type doping concentration of 2×10^{19} cm^{-3}. Basic operation principle of our NDR device with ultra-high PVCR is that NW transistor can completely suppress the valley current creating NDR region. Single or multiple NDR curves can be observed by adjusting the threshold voltage of NW transistor.

Figure 2-23 illustrates the operation principle of different doping concentration of *pn* junction by the energy band diagrams. Both of the moderately doped junction and heavily doped tunnel junction can inject the electrons and drain the holes at low gate bias. If we increase the gate bias faster than source bias, the potential barrier for holes increases and thus, NDR can be obtained with ultra-low valley current. In case of tunnel junctions, the higher peak current can be expected due to the BTBT at lower source bias (Fig. 2-23(c)).

2.3.2 Single NDR characteristics

Figure 2-24 shows the NDR characteristics of the *p*-type NW transistors connected to the junction diode with various doping concentrations. As expected from the device operation principle, peak current has been reduced by the increase of built-in potential as doping increases. After the tunnel junction is obtained by degenerate doping, however, both of the increased peak current and lower voltage operation can be achieved due to the additional carrier injection from the tunnel junction at lower bias condition. The proposed NDR devices show the PVCR over 10^4 even though TAT is

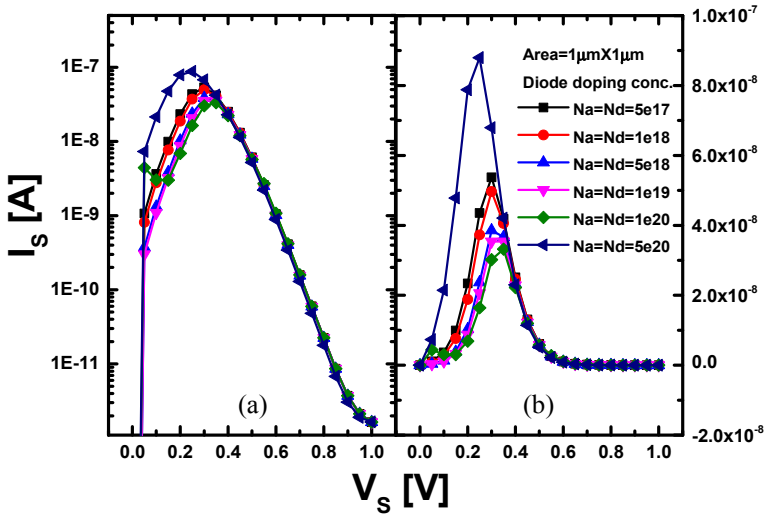


Figure 2-24. The I_S-V_S characteristic of NDR device with *p*-type NW transistor according to the various doping concentration of *pn* junction diode: (a) log scale (b) linear scale. Gate voltage VG has been applied to each data point with larger increasing step of 80 mV than V_S increasing step of 50 mV in this *I-V* plot.

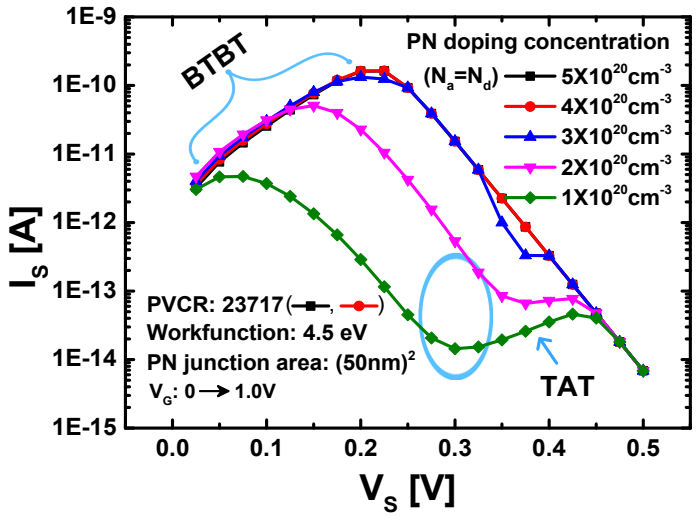


Figure 2-25. NDR characteristics with various doping concentrations of *pn* junction from N_a=N_d=1×10^{20} to 5×10^{20} cm^{-3} by using gate workfunction with WF= 4.5 eV of Si NW transistor. Single NDR curve with ultra-high PVCR over 10^4 can be obtained at low supply voltage of 0.5 V.

allowed with a realistic level in Fig. 2-24(a), since valley current can be completely suppressed due to the depletion under the higher gate bias.

Moreover, as shown in Fig. 2-25, single NDR curves can be obtained with ultra-high PVCR over 10^4 at low supply voltage of 0.5 V by the suppression of valley current from turning-off NW transistor (V_G from 0 to 1 V) with lower gate workfunction (WF= 4.5 eV). It should be noted that single peaks result from BTBT mechanism of tunnel diode since peak current levels can be enhanced by the increase of doping concentration. Higher PVCR over 10^5 can be expected only by considering peak current enhancement (e.g. lower band-gap materials) since the valley current can be always suppressed as off-current of NW transistor at lower operation voltage below 0.5 V.

2.3.3. Multiple NDR characteristics

Figure 2-26 shows the multiple NDR characteristics with multi- peak and valley currents and/or voltages referred to peak1, valley1, peak2, and valley2. As in the insets of Fig. 2-26, the corresponding energy band diagrams with each current component illustrate the operation principle of the multiple NDRs. At low gate bias (on-state) of NW transistor, source voltage can be transferred to *p*-region of tunnel diode. Then, the peak1 and valley1 are caused by BTBT and TAT current of tunnel junction, respectively, as a typical Esaki tunnel diode behavior. After thermal diode current over the

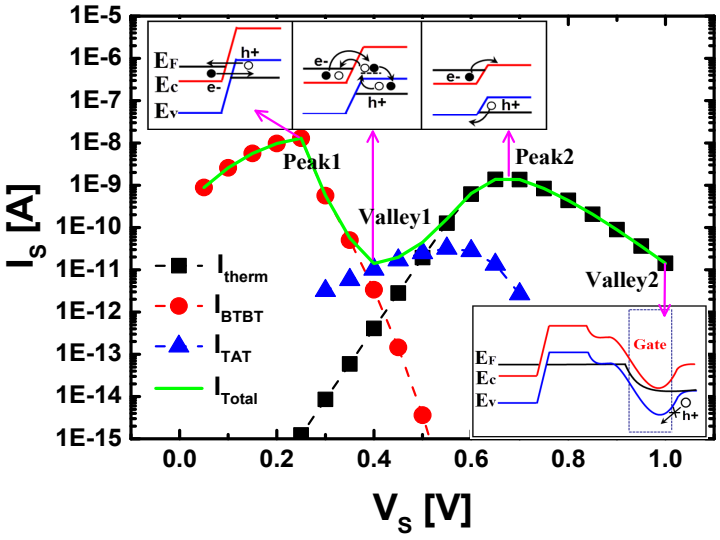


Figure 2-26. Multiple NDR characteristics with the respective current component and the corresponding energy band diagram: Peak1, valley1, and peak2 is caused by normal Esaki tunnel diode behaviors such as BTBT, TAT, and thermionic injection as shown in upper energy band diagrams. Valley2 is suppressed by the increase of potential barrier as shown in lower energy band diagram using faster sweep of gate bias from 0 to 1.5 V than that of source bias from 0 to 1 V.

barrier of forward-biased *pn* junction becomes dominant, the second peak2 and valley2 can be observed by the suppression of diode current owing to increase the gate potential barrier of NW transistor when the gate bias increases faster than source bias.

The multiple NDR characteristics can be controlled by design parameters such as doping concentration, junction area of diode, and threshold voltage of NW transistor. Figure 2-27(a) and (b) show the effects of doping concentration and junction area on the NDR curves, respectively. When doping concentrations of *pn* tunnel junction increase, BTBT current and voltage of peak1 increase by higher potential difference in tunnel junction diode. Valley1 currents which are determined by TAT currents also increase by field enhancement according to the increase of doping level from 1×10^{20} to

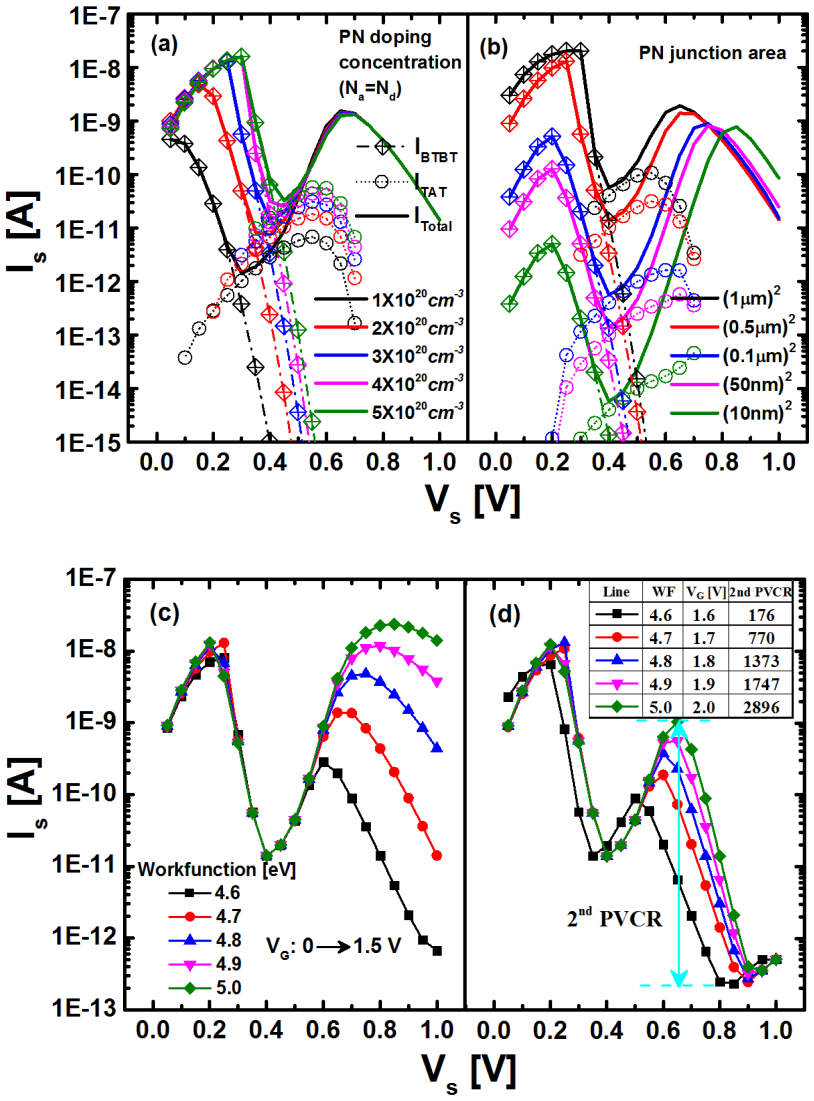


Figure 2-27. The I_s-V_s characteristics with various design parameters: (a) *pn* doping concentrations (b) *pn* junction area of tunnel diode (c) gate workfunction (WF) (d) both gate workfunction (WF) and bias (V_G) of Si NW transistor. Tunnel diode can control the current and voltage levels of peak1 and valley1 and NW transistor can control those of peak2 and valley2.

5×10^{20} cm^{-3}, while thermal diode currents for peak2 remain constant in the degenerate doping range (Fig. 2-27(a)). When the junction area increases, BTBT (peak1), TAT (valley1), and thermal diode (peak2) currents increase as expected (Fig. 2-27(b)). On the other hand, current and voltage levels of valley2 are not affected by junction area and doping concentration since high gate bias (off-state) of NW transistor suppresses the carrier injection into diode region.

Figure 2-27(c) and (d) represent that NW transistor can control the peak2 and valley2 with the threshold voltage (V_{th}), which can be designed by using the various gate workfunction, radius, and doping concentration of NW transistors [54]. In Fig. 2-27(c), when the gate workfunction increases, current and voltage levels of peak2 increase owing to V_{th} shifts in the positive direction of *p*-type Si NW transistor. According to the positive V_{th} shift, there is a trade-off between operation voltage and PVCR for second peak and valley. By applying high gate voltage for high peak2 current, higher (2^{nd}) PVCR can be obtained as shown in Fig. 2-27(d). Therefore, we can design the multiple switching NDR devices with ultra-high PVCR by using device parameters of *pn* junction diode and NW transistor.

2.3.4. Comparison between carrier injection mechanisms

Figure 2-28 shows 2D schematics and symbol of NDR device with *npn* array and its operation principle is illustrated in Fig. 2-29. In this structure, the floating potential of *p*-region can be affected by both the drain and gate bias simultaneously. In case of junction diode with low doping, the injected carriers from *n*-type NW can easily flow to the drain when drain bias increases (Fig. 2-29(a)). If the gate voltage decreases from on-state to off-state while drain bias increases, carrier injection is inhibited by the increased potential barrier due to the depletion under gate region (Fig. 2-29(b)). As shown in Fig. 2-30, doping-dependent NDR characteristics indicate that the peak current increases and shift to lower voltage due to the reduction of potential barrier in the floating p-region when

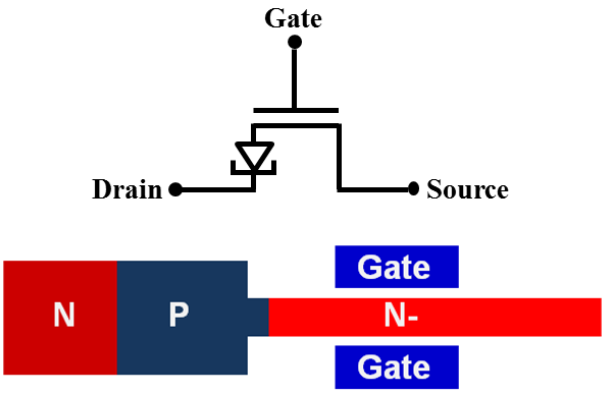


Figure 2-28. Circuit symbol and 2D schematic of *npn* array

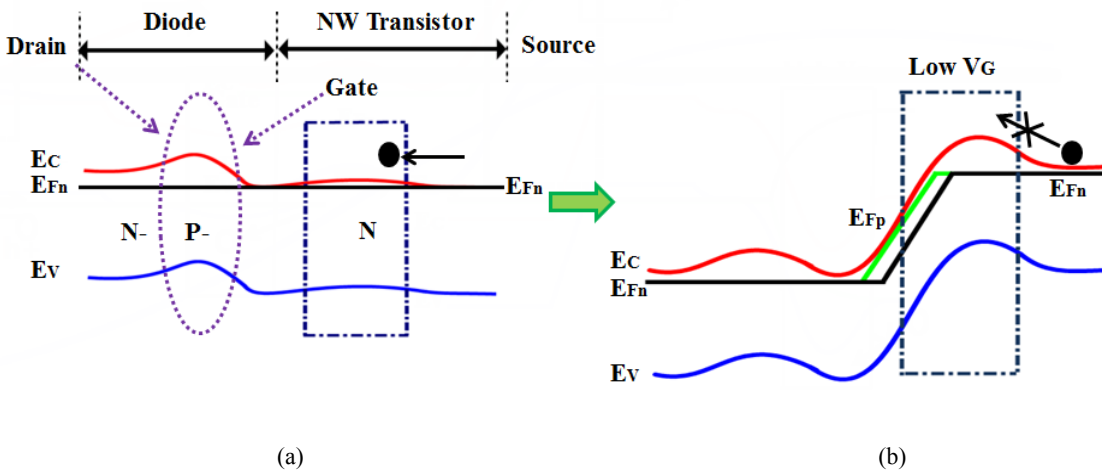


Figure 2-29. Energy band diagram of NDR device with n-type NW transistor: (a) Initial band diagram at increasing current with high V_G and (b) final band diagram at valley current suppression with low V_G.

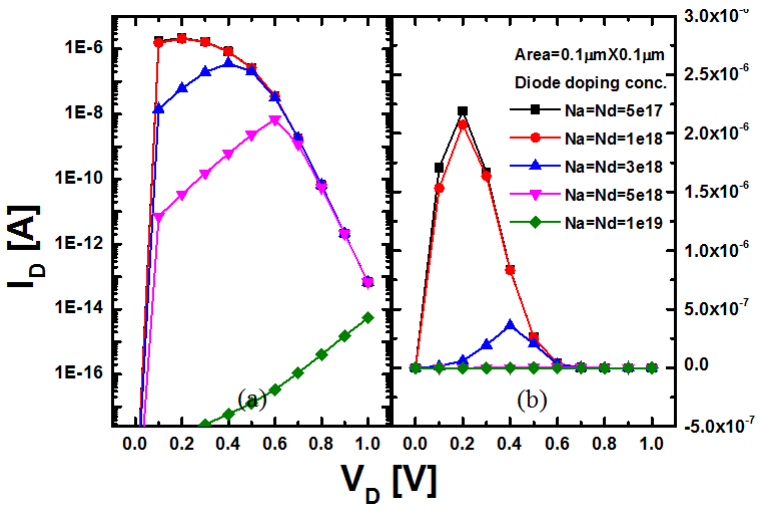


Figure 2-30. The *I-V* characteristic of NDR device with n-type NW transistor according to the various doping concentration of diode: (a) log scale (b) linear scale. Gate voltage V_G has been applied to each data point decreasing step of 50 mV which is same with V_D increasing step in this *I-V* plot.

doping concentration of junction diode decreases as an opposite behavior from the previous case of Fig. 2-22. One of the advantages in this mechanism is that we can accommodate the same step of steps of gate and drain voltage shift onto each current-voltage data point for more compact NDR circuit configuration.

Chapter 3

NDR Device based on Metal-Semiconductor Field-Effect Transistor and PN Tunnel Junction

In this section, I generalize proposed NDR device to *pn* tunnel junction-embedded conventional Si MOSFET structure for practical applications, satisfying both ultra-high PVCR and multiple peaks at 1V. Moreover, in order to solve the issue of simultaneous input sweep, complementary circuit configuration is invented. Device operation principle with a complementary configuration is presented for multiple NDR characteristics and then, the effects of device design parameters on multiple NDR are investigated.

3.1 Device Structure and Operation Principle

Figure 1(a) shows the 2-D cross-sectional view and circuit symbol of the proposed *n*-type NDR (*n*NDR) device based on the simple *n*-MOSFET structure with a degenerately doped *pn* tunnel junction at drain side. In our simulation work, complementary *p*NDR device also can be implemented based on *p*-MOSFET with the tunnel diode, which has been designed with both *n*+ and *p*+ doping concentrations of $5\times10^{20}cm^{-3}$ and a typical junction contact area of $100\times100nm^2$. Figure 3-1(b)

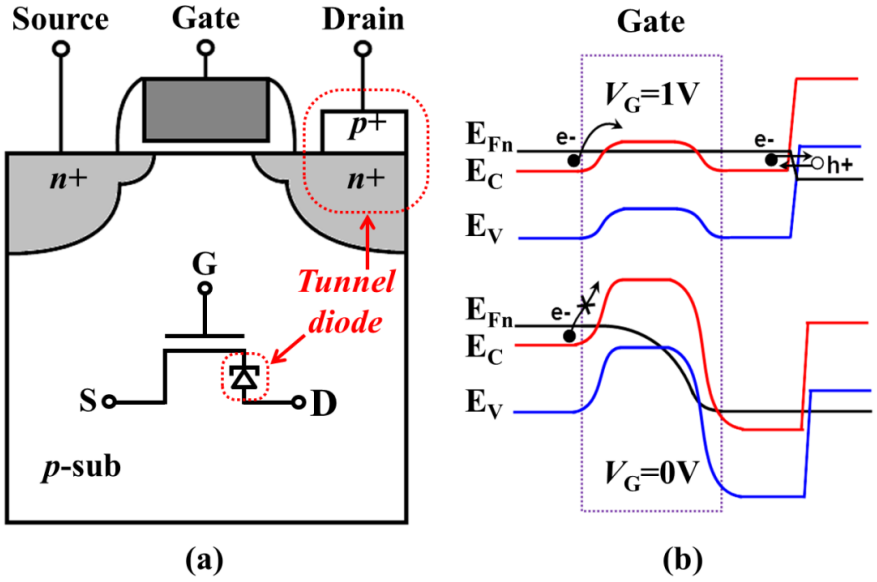


Figure 3-1. (a) Device structure and circuit symbol of the proposed *n*NDR (*n*-type NDR) device combining *pn* tunnel diode with *n*-MOSFET (b) energy-band diagrams with the carrier (electron) injection mechanism at on-state (upper one) and off-state (lower one) of *n*-MOSFET. The *p*NDR (*p*-type NDR) based on *p*-MOSFET can be implemented in a complementary way.

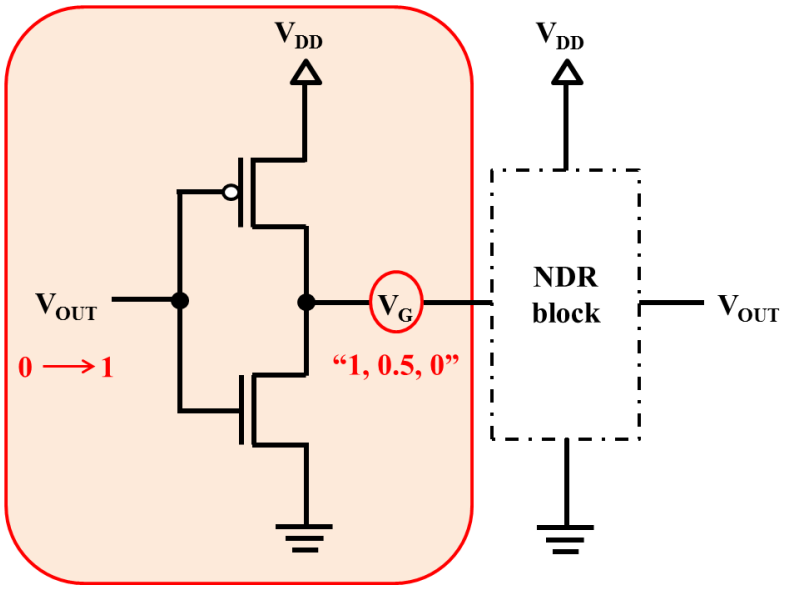
explains the key role of MOSFET for the multiple NDR with ultra-high PVCR by using each energy band diagram at different gate voltages. When the combined MOSFET with tunnel junction operates at the on-state (upper one), it supplies the channel electrons to tunnel diode and then, the first NDR curve by BTBT, TAT, and diffusion as in a normal tunnel diode can be obtained. In the off-state (lower one) case, high channel potential barrier of MOSFET inhibits the flow of electrons so that the device current can be suppressed at MOSFET off-current level.

3.2 Circuit Configuration

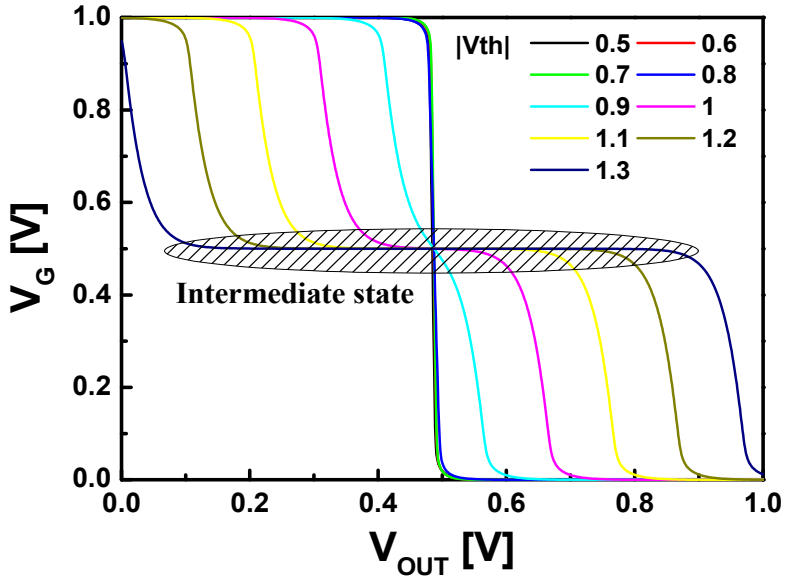
In order to simultaneously sweep at both gate and drain, I introduce tri-state voltage transfer circuit using CMOS inverter. By applying the circuit configuration, ultra-high 2nd PVCR is obtained. In addition, minimum cell size of latch circuit can be reduced.

3.2.1 Tri-state voltage transfer curve

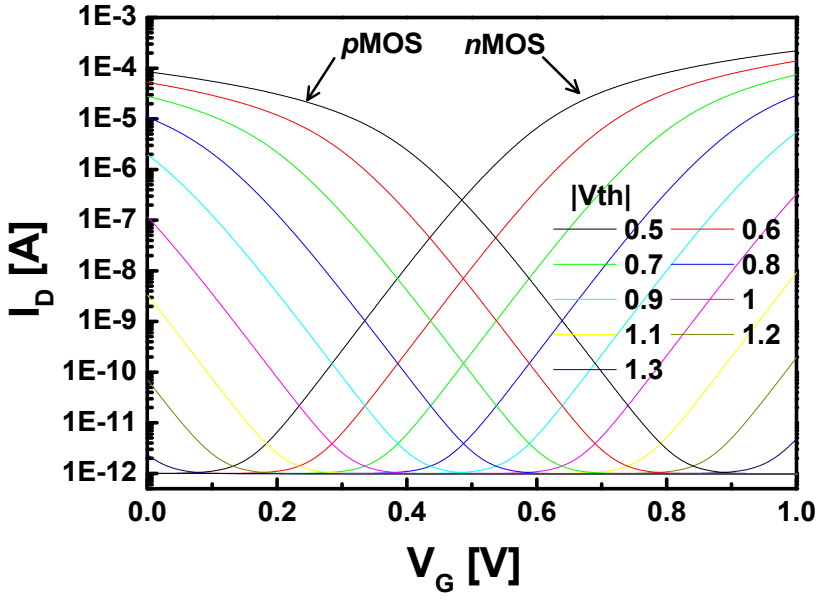
Figure 3-2(a) and (b) shows the tri-state voltage transfer circuit and curve (V_G= 1, 0.5, 0 V) during the single terminal voltage (V_{OUT}) sweep from 0 to 1 V. By using CMOS inverter with each *n*MOS and *p*MOS having $|V_{th}| \geq V_{DD}$, intermediate state (0.5 V) is obtained from the voltage dividing between two off-state *n*/*p*MOS, which is a distinguished characteristic from the conventional CMOS inverter. When V_G changed from 0.5V to 1V, 2nd valley current of *n*NDR is suppressed. On the other hand, When V_G changed from 0.5V to 1V, 2nd valley current of *p*NDR is suppressed. Therefore, tri-state



(a)



(b)

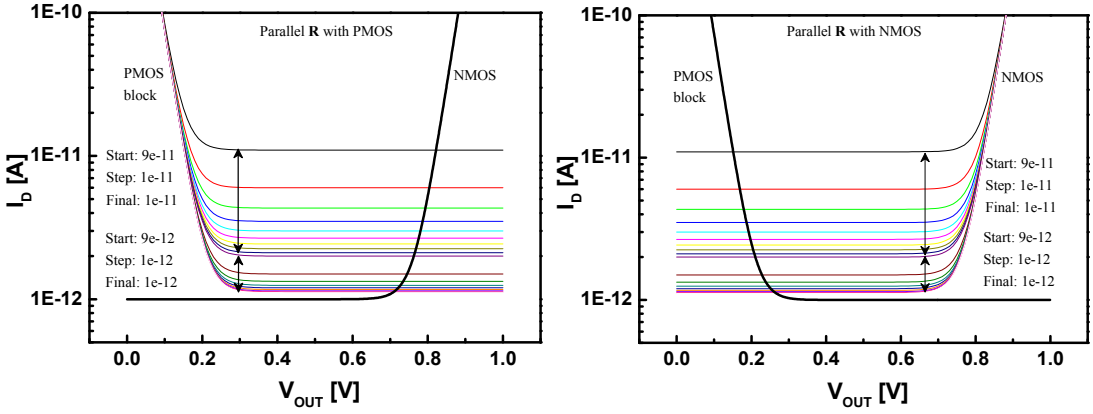


(c)

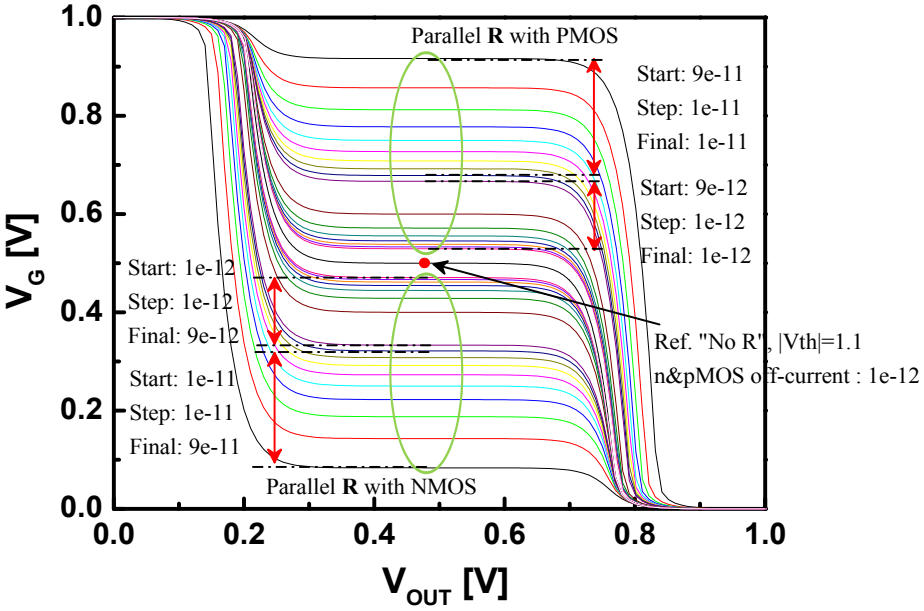
Figure 3-2. The tri-state voltage transfer circuit (a) and curves (b), and its corresponding *I-V* characteristics of *n*MOS and *p*MOS (c).

voltage transfer curve makes the number of transistor of latch circuit is reduced. The latch circuit will be discussed at 3.2.2. Moreover, much higher 2nd PVCR over 10^6 is obtained, owing to faster change of V_G. Figure 3-2(c) shows the corresponding *n*/*p*MOS *I-V* curves. When both n/pMOS go into completely off state, voltage dividing phenomenon could be happen. The intermediate regions are matched with continuous off state regions for both *n*/*p*MOS. As higher $|V_{th}|$ is used, large area of intermediate state can be acceped.

Figure 3-3 shows the tri-state voltage transfer curve with various intermediate values according to miss-matched off current between *n*/*p*MOS. In order to adjust the off state currents, parallel resistance is supplemented. Figure 3-3 (a) and (b) show the *I-V* characteristics of blocks with *p*/*n*MOS with parallel resistance, respectively. When parallel resistance is added with *p*MOS, the off current of block with *p*MOS is adjusted as Fig. 3-3(a). As same way, the off current of block with *n*MOS is modified as Fig. 3-3(b).



(a) (b)



(c)

Figure 3-3. *I-V* characteristics and tri-state voltage transfer curve with various parallel resistances: (a) *I-V* curve of block with *p*MOS and parallel resistance, (b) *I-V* curve of block with *n*MOS and parallel resistance, and (c) tri-state voltage transfer curve.

3.2.2 Latch circuit with proposed NDR device.

Figure 3-4 shows the proposed 5-stable state latch circuit with 4 devices. In order to suppress the valley2 current with complementary V_G for each multiple *n*NDR (V_G= 0 V) and *p*NDR (V_G= 1 V) device, tri-state voltage transfer circuit is introduced. It allows the multiple NDR characteristics in a complementary way for the practical MVL and MVM applications with a compact circuit design. Figure 3-5 shows the simulated multiple NDR *I-V* curves in the complementary NDR devices with

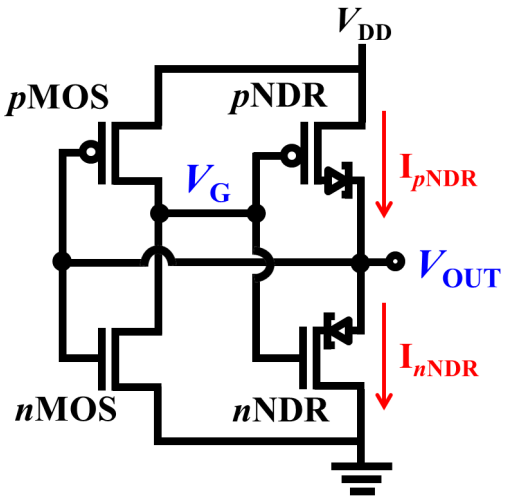


Figure 3-4. The latch circuit configuration with CMOS inverter, *n*NDR, and *p*NDR for complementary multiple NDR based on tri-state V_G transfer during a single terminal V_{OUT} sweep

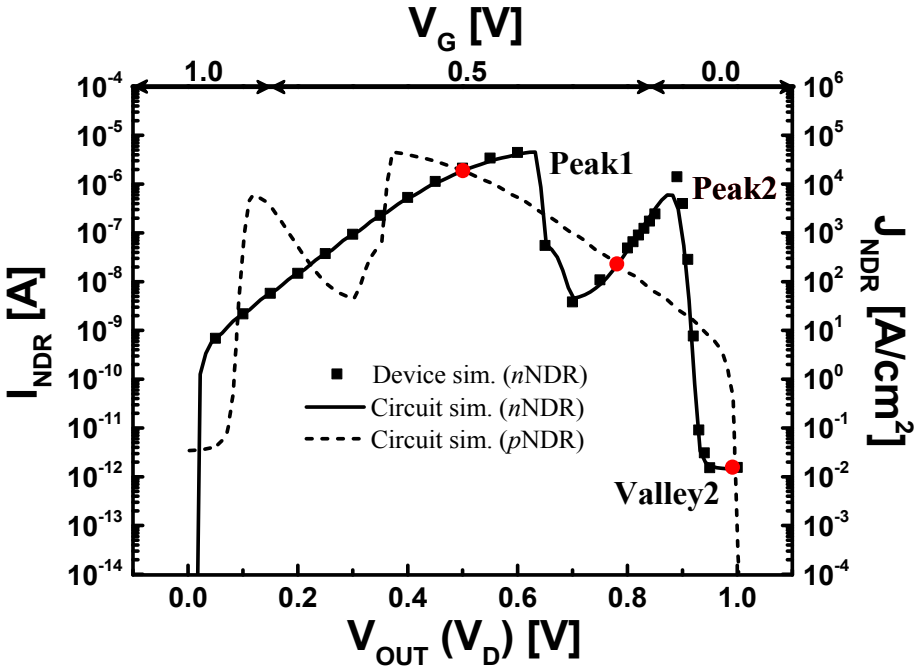


Figure 3-5. Simulated multiple NDR *I-V* characteristics of *n*NDR and *p*NDR from the device and circuit simulations

ultra-high PVCR over 10^6 at V_{DD}= 1 V based on the proposed operation principle where the 1st peak (peak1) and 1st valley (valley1) are generated by a typical tunnel diode behavior and the subsequent 2nd peak (peak2) can be formed by suppressing the 2nd valley (valley2) at the MOSFET off-leakage level (~1 pA) due to the increase of potential barrier from V_G. Device simulation was performed by using *Sentaurus*™ 3-D TCAD device simulator and HSPICE circuit simulation was performed using BSIM4 model (level 54) and piecewise linear current source for peak1 and valley1. The operating points (circle) represent the 5-stable states with only 4 devices in this complementary latch configuration.

3.3 Multiple NDR Characteristics with Ultra-High Peak-to-Valley Current Ratio

The multiple NDR characteristics can be controlled by design parameters such as doping concentration of tunnel junction and the gate workfunction (WF) of the tunnel junction-embedded MOSFETs as shown in Fig. 3-6(a) and (b), respectively. Figure 3-6(a) shows that the peak1 current by BTBT and the valley1current by TAT increase by field enhancement when doping concentration of *pn* tunnel junction increases from 1×10^{20} to 5×10^{20}cm^{-3} without changing 2nd NDR characteristics with peak2 and valley2 current in this degenerate doping range. These simulated doping-dependent peak1 current values have been compared with the experimental data of Si tunnel junction based on BTBT

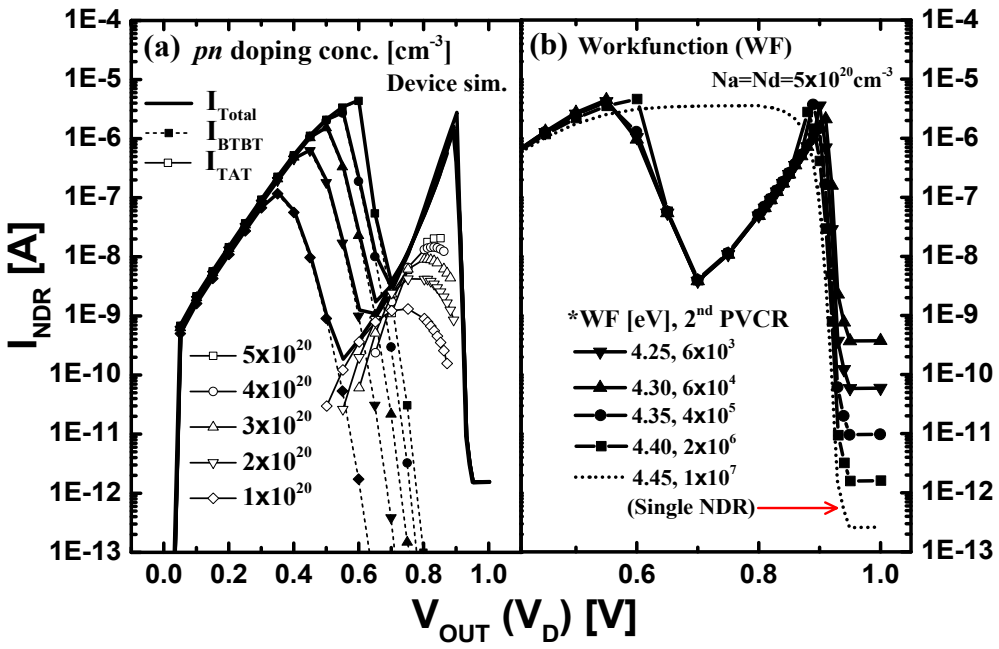


Figure 3-6. Simulation results of *I-V* characteristics with various design parameters: (a) *pn* doping concentrations of tunnel junction and (b) gate workfunction (WF) of MOSFET in NDR device. The 1st and 2nd NDR can be controlled by using design parameters of *pn* tunnel junction and MOSFET, respectively.

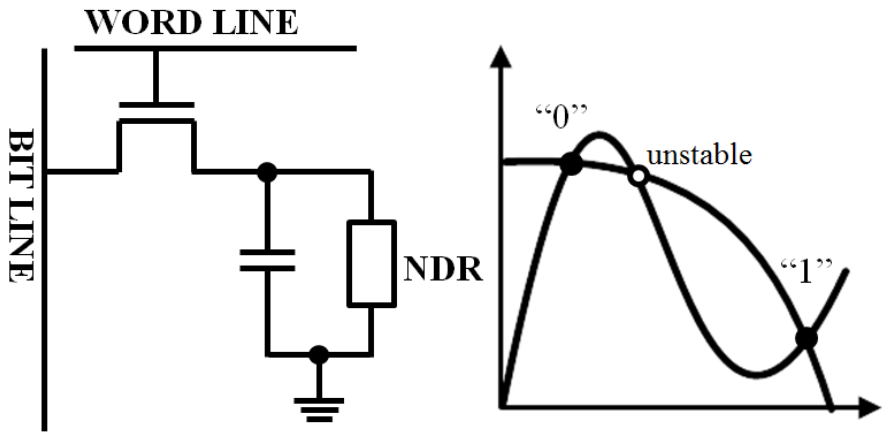
mechanism [55]. Figure 3-6(b) indicates that the 2nd PVCR can be determined by the off-current of the MOSFET at V_G= 0 V, if MOSFET on current is larger than the peak1 current allowing the multiple NDR characteristics. When the threshold voltage increases by changing the gate WF with 150 meV, the 2nd PVCR increases from 10^3 to 10^6 since the MOSFET off-current (valley2) exponentially decreases by $exp(\Delta VT/mk_{BT})$ where m=1.1~1.4 at T= 300K. In case that MOSFET on-current limits the peak1 currents (e.g. WF=4.45eV), however, only single NDR has been observed with PVCR= 10^7 which is corresponding with MOSFET on/off current ratio since the MOSFET channel dominates the current flowing mechanism. Therefore, we can control each 1st and 2nd NDR by using design parameters of *pn* tunnel junction and MOSFET, respectively.

Chapter 4

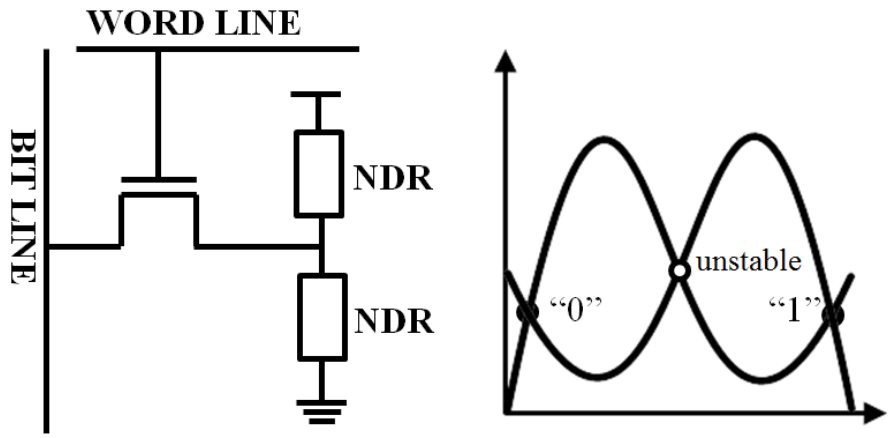
Multi-Valued Logic and Memory Application

Among of the various applications of NDR device, multi-valued logic (MVL) and memory (MVM) applications are stood out in digital logics. Based on NDR device, static random access memory (SRAM) can be realized with smaller cell size compared with conventional one. In addition, by using the multiple NDRs device, more than "2" is memorized. There are two methods for SRAM as shown in Fig. 4-1 [6, 56]. Figure 4-1(a) used one NDR and one capacitor and Figure 4-1(b) used two NDR device. In the mimetic *I-V* curves, there are two stable (black circle) and one unstable (white one) states.

Figure 4-2 shows the transient simulation results of the latch circuit in the Fig. 3-4 demonstrating 5-state memory with only 4 transistors. By obtaining the peak1 voltage above 0.5V as in Fig. 3-3, the



(a)



(b)

Figure 4-1. Basic concept of NDR SRAM and its operation schemes: (a) one NDR and one capacitor and (b) two NDRs

delay for the "2" state can be comparable with other states since the stable operating point is crossing around high peak current not low valley's one. Moreover, the 1st PVCR becomes less important than 2nd PVCR in this operating condition. For the realistic delay estimation, Si tunnel diode experimental data have been referenced as the peak current levels of 15 μA [57] and 1st PVCR of 5 [58] in the dotted line results. As shown in the simulation results with solid and dashed line, delay can be more reduced below 5 ns by increasing the peak currents up to 60 μA. Thus, it can be expected that the speed of 5-state MVL/MVM operation can be enhanced further by developing the tunnel junction technology with high peak current density.

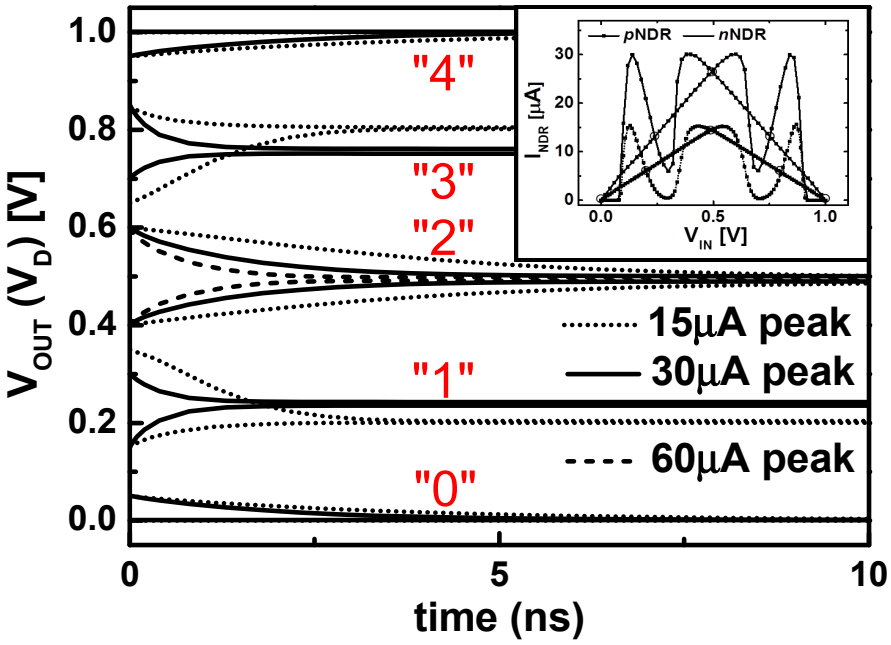


Figure 4-2. Transient simulation results of the latch circuit (Fig. 3-4). Initial states of V_{OUT} with variations of ± 100 mV are converged to 5- states. The dotted line's 1st peaks and PVCR are referenced by experimental data [2, 13].

Chapter 5

Summary & Conclusion

In this thesis, I proposed the novel NDR device with ultra-high PVCR over 10^6 having complementary single and multiple NDR characteristics at 1 V operation based on *pn* tunnel junction-embedded VJL SNW FET structure and *pn* tunnel junction-embedded MOSFET structure. The *pn* tunnel diode makes faster and higher peak currents owing to BTBT phenomenon. Transistor suppressed valley currents at MOSFET off current level. With various device configurations between *pn* diode and transistor, diverse single and multiple NDR characteristics were obtained. These NDR characteristics have been investigated with the analysis of each current component (BTBT, TAT, and diffusion) according to the device design parameters. In the multiple NDR characteristics, the *pn* tunnel junction controls the 1^{st} NDR and transistors control the 2^{nd} NDR characteristics. Moreover, introduced tri-state voltage transfer circuits make ultra-high 2^{nd} PVCR and single input sweep (V_{OUT}) operation. In addition, the 5-state memory can be obtained with 4 transistors in a complementary NDR-based latch circuit.

Chapter 6

Future Works

In this chapter, I will briefly introduced future works in three directions, fabrication, memory, and neuromorphic application. In the fabrications, NDR devices will be realized by adding one more mask layer at conventional MOSFET process. In the multi-valued memory applications, I will develop the introduced latch circuit and make SRAM circuit with compact design. Finally, in the neuromorphic applications, the existing fundamental concept of neuromorphic network is applied to our NDR device.

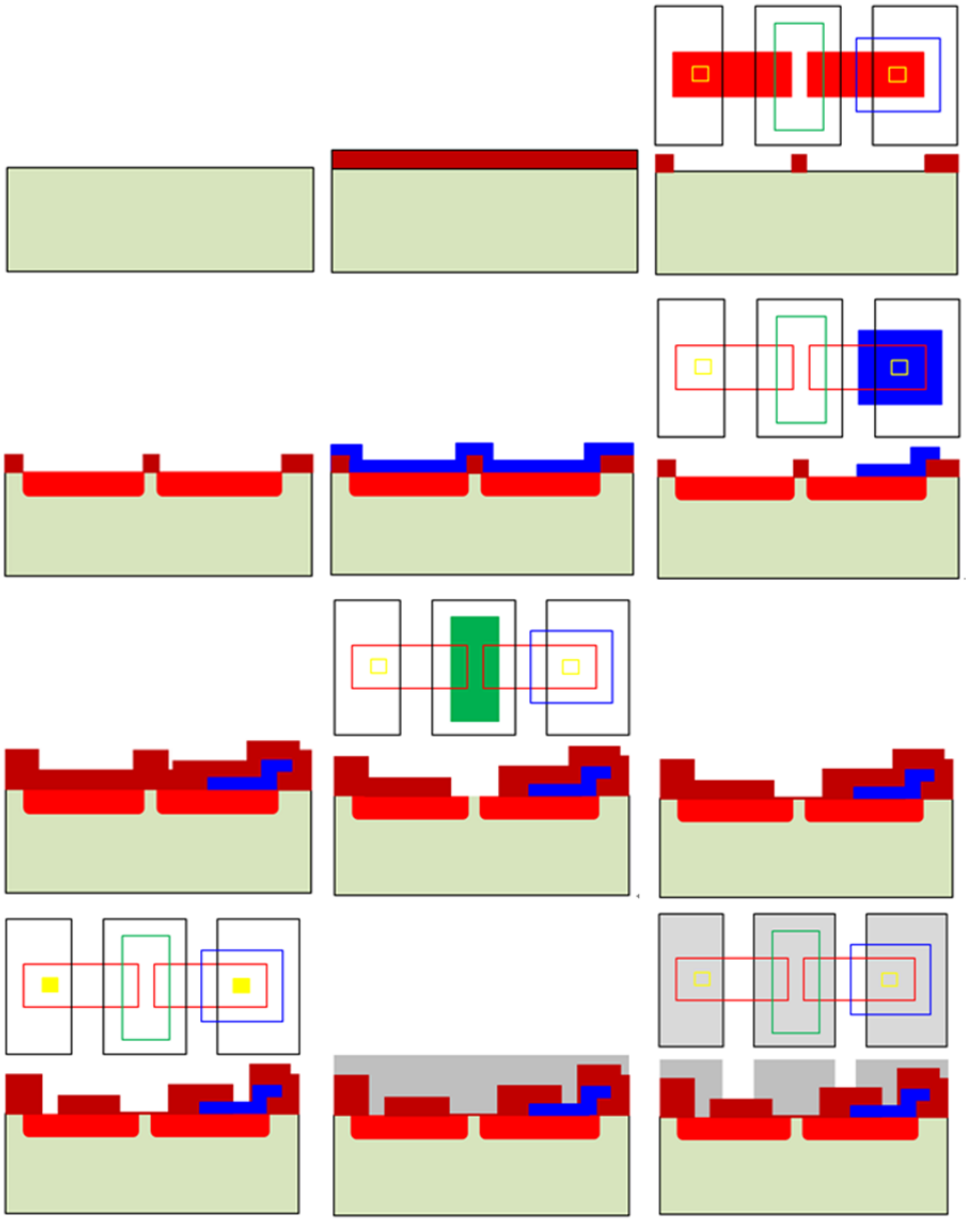


Figure 6-1. The process flow of metal-gate *n*NDR process set up with 5 mask layer

Figure 6-1 shows the process flow of proposed *n*NDR device based on metal-gate *n*MOS process. For the *p*+ layer the blue make is introduced. At the *p*-type substrate, the field oxide is growed and patterned for source/drain doping process. In order to make *pn* tunnel junction, *p*+ doped silicon layer is deposited above *n*+ doped drain and patterned. Another way for *pn* junction is diffusion process for inversion from *n*+ to *p*+. Followed process is same with metal-gate MOSFET process. The gate open and contact hole open process is came. After metal deposition, electrode is divided into 3 region for gate/source/drain.

In order to develop the latch circuit to SRAM, read and write method should be supplemented. In terms of speed, 1st and 2nd peak currents will be reinforced with low band-gap materials. For the accurate simulation data, BTBT and TAT model should be improvement.

Figure 6-2 is summarized neuromorphic network and its memory and inference method. When both connected neurons have input of 1, synapse increases the intensity. When both inputs have -1, synapse doesn't change the intensity. On the other hand, if both neurons have different input values, synapse

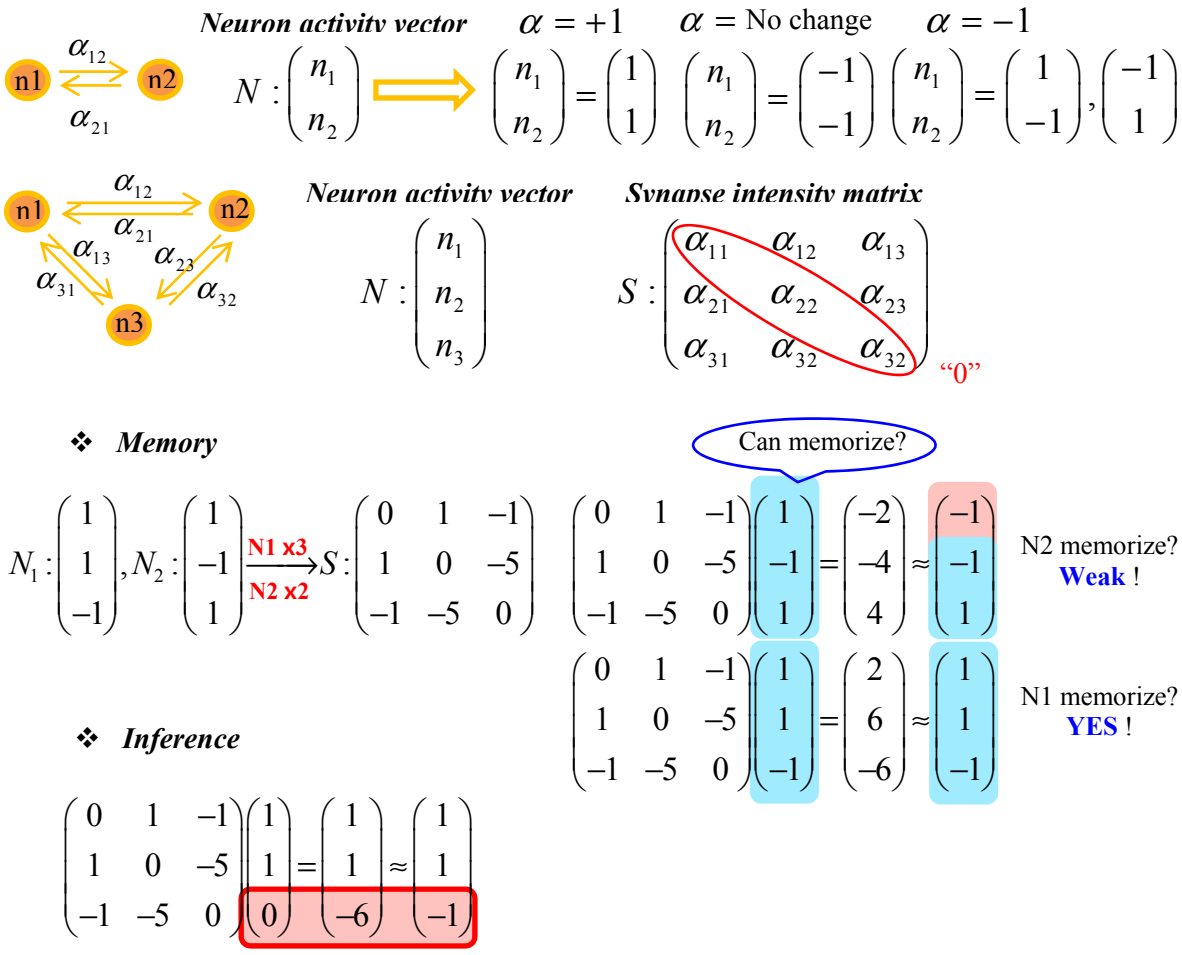


Figure 6-2. The summary of neuromorphic network and its memory and inference method

will decrease the intensity. According to the neuron active vector from bi-directional switching device, synapse intensity matrix is calculated and memorized with quantum dot structure. In Fig. 6-2, the three times input (N1) is well memorized, but two times input (N2) is week memorized. Therefore, neuromorphic device judges the importance of data according to its frequency. For the inference application, when the input has 0, network infers the data. By using this mechanism, new process paradigm will be realized.

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