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Article:

Comparative Analysis of VDMOS/LDMOS Power Transistors for RF Amplifiers

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Abstract—A comparison between the RF performance of vertical and lateral power MOSFETs is presented. The role of each parasitic parameter in the assessment of the power gain, 1-dB compression point, efficiency, stability, and output matching is evaluated quantitatively using new analytical expressions derived from a ten-element model. This study reveals that the contribution of the parasitic parameter on degradation of performance depends upon the specific technology and generic perceptions of source inductance and feedback capacitance in VDMOS degradation may not always hold. This conclusion is supported by a detailed analysis of three devices of the same power rating from three different commercial vendors. A methodology for optimizing a device technology, specifically for RF performance and power amplifier performance is demonstrated.

Index Terms—Efficiency, lateral diffused MOSFET (LDMOSFET), power gain (PG), stability factor, vertical diffused MOSFET (VDMOSFET).

I. INTRODUCTION

TWO structures of silicon MOSFETs are widely used in RF communication systems: 1) the lateral diffused MOSFET (LDMOSFET) and 2) the vertical diffused MOSFET (VDMOSFET). These structures differ in performance [1], [2]: the LDMOS with higher power gain (PG) and efficiency (η) is more suitable at frequencies in excess of 1 GHz, whereas the smaller degradation of input signal and enhanced stability logically makes the VDMOS suitable for low-frequency broadband applications.

Trivedi and Shenai [1] and Leong [2] first examined the issue of the VDMOS versus the LDMOS. These studies revealed global considerations, explaining the most appropriate choice of structure for a specific application. However, the origin of these differences was not explained, though most of the degradation of the VDMOS is widely attributed to the inductance of the source wire, necessary to package the device as well as the gate to drain capacitance. In [2], the LP801 (lateral structure) and the F2012 (vertical structure), both from Polyfet, Santa Clara, CA [3], were compared. Some of their results are recapitulated in Table I, confirming the enhanced output power and gain of the lateral device.

TABLE I
SOME RF COMPARISON BETWEEN LP801 AND F2012

Frequency	Transistor	Power Ouput	Power Gain	Efficiency
1000 MHz	LP801	15 W	12 dB	60%
	F2012	10 W	10 dB	35%
500 MHz	LP801	20 W	13 dB	70%
	F2012	15 W	12 dB	45%

Leong also demonstrated that instability takes effect at lower frequencies for the VDMOSFET, whereas it extends into the operating bandwidth and beyond in the case of the lateral structure. While a lower out-of-band instability can be overcome without major deterioration of performance in the operating frequency, with resistive loading of the gate circuit, instabilities in the operating band and above are more difficult to cancel and force the designer to deal with a compromise [2].

The methodology of this paper is the utilization of new analytical expressions to determine optimum matching impedances for the power MOSFET. Source and load impedances are recalculated for different values of intrinsic parameters and PG, efficiency, and stability simulated with ADS[1] via the harmonic balance (HB) approach. To perform this study, a set of three transistors, which deliver similar output power and operate at the same frequency, is considered. The three devices (one lateral and two vertical) are commercial parts from three different vendors, which can deliver about 4 W at 1 GHz. For the purpose of anonymity, the considered devices will be named as LD, VD_1, and VD_2 for the lateral and the two vertical parts, respectively. Furthermore, the performance has been evaluated by gradually modifying one (or several) parasitic parameter of the VDMOS at a time to equal that of the corresponding value(s) for the lateral counterpart. This ensures that the degradation can be attributed to the specific parameter(s) alone. The considered power amplifiers are single stage amplifiers (class AB, common source amplifier); input and output of the devices are matched to the 50-Ω environment using lumped elements matching networks (low-pass matching network).

Main characteristics of the three transistors are summarized in Table II. Table III depicts values of parasitic parameters (in accordance with the model used in [4]). The models of the two vertical devices are provided by the vendors, whereas the model of the LDMOS is extracted from measured scattering parameters using the same extraction procedure [5]–[7]; an optimization is then applied on these parameters in order to ensure a perfect match between simulated and measured data. The validity of all the models is verified via HB simulations. DC and RF performances (gain, output power, efficiency) are simulated

[1]Polyfet Website. [Online]. Available: http://polyfet.com

TABLE II
RF CHARACTERISTICS OF ALL CONSIDERED DEVICES

Transistor	Power Gain	Max η	Max PAE
LD	22.144 dB	66.167 %	59.64 %
VD₁	13.4002 dB	50.020 %	40.610 %
VD₂	14.1548 dB	58.246 %	53.117 %

TABLE III
VALUES OF INTRINSIC PARAMETERS FOR ALL CONSIDERED DEVICES

Device	R_g [Ω]	L_g [nH]	L_s [nH]	L_d [nH]
LD	1.248	1.66	0.0379	0.827
VD₁	5.27	1.25	0.35	0.75
VD₂	2.5	1.401	0.1464	0.026

Device	C_{gs} [pF]	C_{gd} [pF]	C_{ds} [pF]	g_m [S]
LD	6.739	0.07675	2.75	0.24
VD₁	12.8	0.64	6	0.273
VD₂	15.01	0.5158	9	0.29
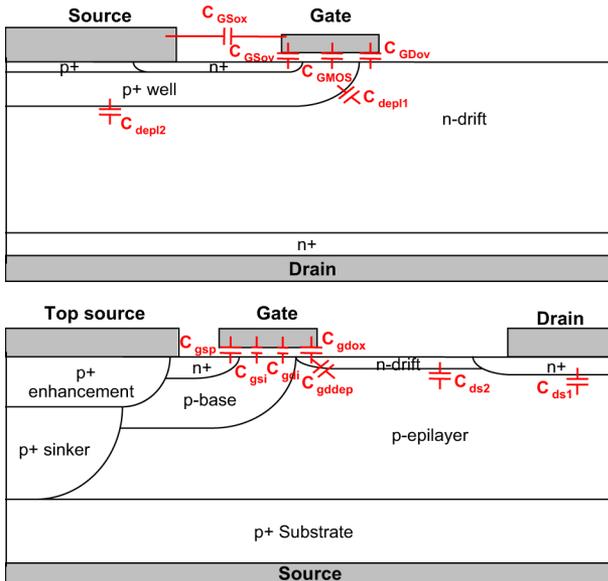
Fig. 1. Cross sections of RF power VDMOS and LDMOS transistors with parasitic capacitances.

with ADS and the model is validated through a comparison with measured data.

Fig. 1 shows the cross sections of the two structures. The parasitic capacitances of the VDMOS can be written as

$$C_{gs} = C_{GSox} + C_{GSov} + C_{GMOS} + C_{GDov} \tag{1}$$

$$C_{ds} = C_{depl1} + C_{depl2} \tag{2}$$

$$C_{gd} = \left(\frac{1}{C_{GMOS}} + \frac{1}{C_{GDov}} \right)^{-1} + C_{GDov}. \tag{3}$$

The capacitances for the LDMOS are

$$C_{gs} = C_{gsp} + C_{gsi} \tag{4}$$

$$C_{gd} = C_{gdi} + \left(C_{gdox}^{-1} + C_{gddep}^{-1} \right)^{-1} \tag{5}$$

$$C_{ds} = C_{ds1} + C_{ds2}. \tag{6}$$
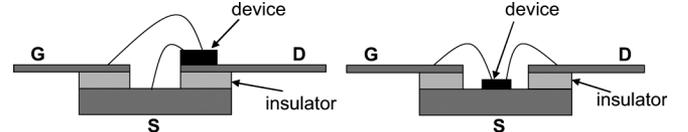
Fig. 2. Types of package for (*left*) vertical and (*right*) lateral RF DMOS.
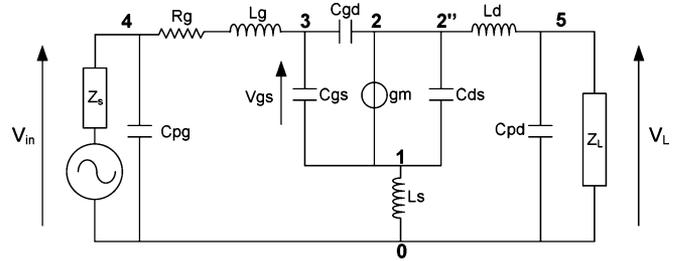
Fig. 3. Transistor model including matching impedances, gate resistance, source inductance, and a nonlinear voltage-controlled current generator. In L_g, L_d, C_{pg}, and C_{pd} were not considered.

The gate-to-drain capacitance is directly related to the overlap of the gate oxide onto the heavily doped $n+$ source region. The topology of LDMOS allows for minimum overlap, leading to smaller feedback capacitance than in VDMOS [8] (Table III).

Fig. 2 shows the package for the two devices. The drain of the vertical device is directly contacted to the drain terminal of the package, whereas bond wires attach the gate and source terminals to the package. On the other hand, the source of the LDMOS is directly contacted to the package; gate and drain are attached with bond wires to the corresponding terminals of the package. This explains the higher values of drain inductance in the case of the LDMOS (Table III).

This paper is organized as follows. The new analytic expressions for the transistor model are explained in Section II. In Section III, PG and efficiency are examined. In Section IV the stability is analyzed. In Section V, the issue of output matching is discussed.

II. NEW ANALYTICAL EXPRESSIONS

Analytical expressions for matching impedances and PG based on the transistor model of Fig. 3 have been presented in [9]–[11] under the assumption of zero gate and drain inductances (L_g, L_d), and zero gate and drain capacitances (C_{pg}, C_{pd}). The PG and optimum source and load impedance were given as

$$Z_L = \frac{[\omega^2 C_{ds} L_s R_{opt} - R_{opt} + j\omega L_s (1 - g_{ds} R_{opt})]g_m - \omega^2 C_{gs} L_s}{[j\omega(C_{ds} + C_{gd})R_{opt} - (1 - g_{ds}R_{opt})]g_m + j\omega C_{gd}} \tag{7}$$

$$Z_S = R_g + \frac{L_s g_m (1 - g_{ds} R_{opt})}{C_{gs} + C_{gd}(1 + R_{opt} g_m)} + j \frac{1 + \omega^2 L_s (C_{ds} R_{opt} g_m - C_{gs})}{\omega[C_{gs} + C_{gd}(1 + R_{opt} g_m)]} \tag{8}$$

$$G = \frac{R_{opt} g_m^2}{\left[\frac{(C_{gs} + C_{gd}(1 + R_{opt} g_m))^2 R_g}{+ L_s g_m (1 - g_{ds} R_{opt})(C_{gs} + C_{gd} + C_{gd} R_{opt} g_m)} \right] \omega^2} \tag{9}$$

where ω is the angular frequency, L_s is the source inductance, C_{gs} is the gate-to-source capacitance, C_{gd} is the gate-to-drain capacitance, C_{ds} is the drain-to-source capacitance, g_m is the transconductance, R_{opt} is the load line optimum resistance, Z_L is the optimum load impedance, and Z_S is the optimum source impedance. The value of the model parameters are extracted at the application frequency and bias.

Proceeding as in [10], the optimum load impedance Z_L is determined by forcing the current generator to see a real output impedance R_{opt}, the load-line resistance, associated with the maximum voltage and current swings [12]. The optimum source impedance Z_S is determined as the conjugate match of the transistor's input impedance.

Circuit analysis of Fig. 3 reveals (10)–(17), shown at the bottom of this page.

Using (8)–(11), optimum source and load impedances are calculated using

$$Z_S = \left(\frac{V_{\mathrm{IN}}}{I_{\mathrm{IN}}}\right)^* \tag{18}$$

$$Z_L = \left(\frac{V_L}{I_L}\right) \tag{19}$$

where $*$ denotes the conjugate.

These expressions yield (20) and (21), shown at the bottom of this page, where $Z_g = R_g + j\omega L_g$. The expressions of input and output power are, respectively, obtained as the power delivered to the transistor under conjugate match conditions and

as the power dissipated by the load-line resistance [12]. These definitions yield

$$P_{\mathrm{out}} = \frac{1}{2}R_{\mathrm{opt}}(g_m V_{\mathrm{gs}})^2 \tag{22}$$

$$P_{\mathrm{in}} = \frac{1}{2}\mathrm{Re}\left\{V_{\mathrm{in}} \cdot I_{\mathrm{in}}^*\right\}. \tag{23}$$

The PG is then defined as

$$PG = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}}. \tag{24}$$

HB simulations have been used as a benchmark for the verification of the accuracy of these expressions. The vertical device is biased at $V_{\mathrm{gsq}} = 3.25$ V($I_{\mathrm{dsq}} = 200$ mA). Matching impedances and PG are compared using our earlier expressions [10] with those presented here with source/load–pull simulations (Figs. 4 and 5). PG and gain compression are calculated and presented in Table IV. G_{calc} corresponds to the PG calculated using the analytical expressions from [10] and this study. G_{sim} and $P_{1\,\mathrm{dB}}$ correspond, respectively, to the simulated PG and the simulated 1-dB compression point when matching impedances are determined via source/load–pull simulations in ADS, equations from [10] and (20) and (21).

Figs. 4 and 5 reveal that the additional parasitic parameters yield significant improvement in the calculation of optimum source and load impedances. The source impedance calculated using (20) is located on the load cycle, which is about 0.2 dB from the optimal impedance $Z_{S,\mathrm{opt}}$. On the other hand, the

$$V_{\mathrm{IN}} = V_{40} = V_{43} + V_{31} + V_{10} \tag{10}$$

$$I_{\mathrm{IN}} = I_{43} + I_{40} \tag{11}$$

$$V_L = V_{50} = V_{52} + V_{21} + V_{10} \tag{12}$$

$$I_L = I_{25} - I_{50} \tag{13}$$

$$V_{\mathrm{IN}} = \lfloor j\omega C_{\mathrm{gd}}Z_g\left(1 + g_m R_{\mathrm{opt}}\right) + j\omega C_{\mathrm{gs}}Z_g + 1 + j\omega L_s\left(j\omega C_{\mathrm{gs}} + g_m - j\omega C_{\mathrm{ds}}g_m R_{\mathrm{opt}}\right)\rfloor V_{\mathrm{gs}} \tag{14}$$

$$I_{\mathrm{IN}} = \begin{bmatrix} j\omega C_{\mathrm{gd}}\left(1 + g_m R_{\mathrm{opt}}\right) + j\omega C_{\mathrm{gs}} - \omega^2 C_{pg}C_{\mathrm{gd}}Z_g\left(1 + g_m R_{\mathrm{opt}}\right) - \omega^2 C_{pg}C_{\mathrm{gs}}Z_g \\ + j\omega C_{pg} - \omega^2 C_{pg}L_s\left(j\omega C_{\mathrm{gs}} + g_m - j\omega C_{\mathrm{ds}}g_m R_{\mathrm{opt}}\right) \end{bmatrix} V_{\mathrm{gs}} \tag{15}$$

$$V_L = \lfloor j\omega L_d\lfloor -j\omega C_{\mathrm{gd}}\left(1 + g_m R_{\mathrm{opt}}\right) + g_m - j\omega C_{\mathrm{ds}}g_m R_{\mathrm{opt}}\rfloor - g_m R_{\mathrm{opt}} + j\omega L_s\left(j\omega C_{\mathrm{gs}} + g_m - j\omega C_{\mathrm{ds}}g_m R_{\mathrm{opt}}\right)\rfloor V_{\mathrm{gs}} \tag{16}$$

$$I_L = \begin{bmatrix} j\omega C_{\mathrm{gd}}\left(1 + g_m R_{\mathrm{opt}}\right) - g_m + j\omega C_{\mathrm{ds}}g_m R_{\mathrm{opt}} + \omega^2 C_{pd}L_d\lfloor -j\omega C_{\mathrm{gd}}\left(1 + g_m R_{\mathrm{opt}}\right) \\ + g_m - j\omega C_{\mathrm{ds}}g_m R_{\mathrm{opt}}\rfloor + j\omega C_{pd}g_m R_{\mathrm{opt}} + \omega^2 C_{pd}L_s\left[j\omega C_{\mathrm{gs}} + g_m - j\omega C_{\mathrm{ds}}g_m R_{\mathrm{opt}}\right] \end{bmatrix} V_{\mathrm{gs}} \tag{17}$$

$$Z_S = \mathrm{conj}\left\{\frac{j\omega C_{\mathrm{gd}}Z_g\left(1 + g_m R_{\mathrm{opt}}\right) + j\omega C_{\mathrm{gs}}Z_g + 1 + Z_s\left[j\omega C_{\mathrm{gs}} + g_m - j\omega C_{\mathrm{ds}}g_m R_{\mathrm{opt}}\right]}{j\omega\left[C_{\mathrm{gd}}\left(1 + g_m R_{\mathrm{opt}}\right) + C_{\mathrm{gs}}\right]} + C_{pg}\left[j\omega\left[C_{\mathrm{gd}}Z_g\left(1 + g_m R_{\mathrm{opt}} + C_{\mathrm{gs}}Z_g + L_s\left(j\omega C_{\mathrm{gs}} + g_m - j\omega C_{\mathrm{ds}}g_m R_{\mathrm{opt}}\right)\right)\right] + 1\right]\right\} \tag{20}$$

$$Z_L = \frac{\left\{j\omega L_d\lfloor -j\omega C_{\mathrm{gd}}\left(1 + g_m R_{\mathrm{opt}}\right) + g_m - j\omega C_{\mathrm{ds}}g_m R_{\mathrm{opt}}\rfloor - j\omega C_{pd}g_m R_{\mathrm{opt}} - \omega^2 C_{pd}L_s\left[j\omega C_{\mathrm{gs}} + g_m - j\omega C_{\mathrm{ds}}g_m R_{\mathrm{opt}}\right]\right\}}{\left\{\left[j\omega C_{\mathrm{gd}}\left(1 + g_m R_{\mathrm{opt}}\right) - g_m + j\omega C_{\mathrm{ds}}g_m R_{\mathrm{opt}}\right] + \omega^2 C_{pd}L_s\left[j\omega C_{\mathrm{gs}} + g_m - j\omega C_{\mathrm{ds}}g_m R_{\mathrm{opt}}\right] + \omega^2 C_{pd}L_d\left[-j\omega C_{\mathrm{gd}}\left(1 + g_m R_{\mathrm{opt}}\right) + g_m - j\omega C_{\mathrm{ds}}g_m R_{\mathrm{opt}}\right] + j\omega C_{pd}g_m R_{\mathrm{opt}}\right\}} \tag{21}$$
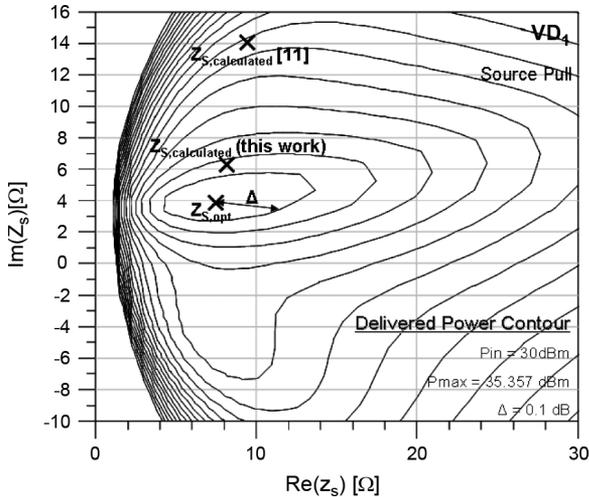
Fig. 4. Source–pull delivered power contours in the class AB ($I_{\mathrm{ds}q} = 0.2$ A) single-tone simulation.
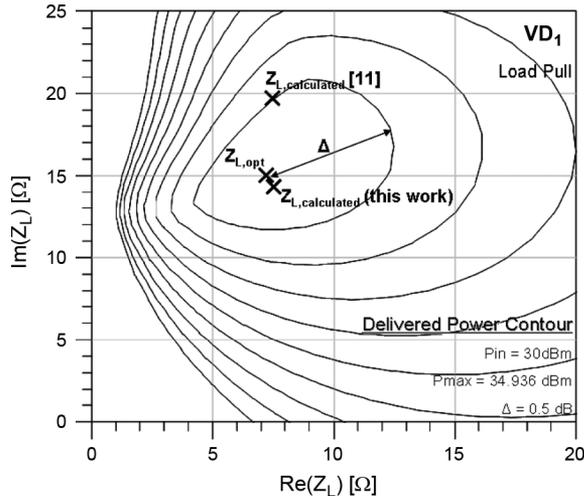
Fig. 5. Load–pull delivered power contours in the class AB ($I_{\mathrm{ds}q} = 0.2$ A) single-tone simulation.

TABLE IV
PG AT SMALL INPUT LEVELS, OPTIMUM LOAD
AND SOURCE IMPEDANCE VALUES

Method	$Z_S[\Omega]$	$Z_L[\Omega]$	$G_{\mathrm{calc}}[\mathrm{dB}]$	$G_{\mathrm{sim}}[\mathrm{dB}]$	$P_{\mathrm{1dB}}[\mathrm{W}]$
HB ADS simulation	7.69 + j3.821	7.14+j14.82	-	13.586	3.964
Work in [11]	9.12+j14.73	7.85+j19.22	13.4002	12.074	2.419
This work	8.756+j6.968	7.69+j14.41	13.4002	13.470	4.029

that additional circuit elements are purely capacitive and inductive. When these elements are not considered in the calculation of matching impedances (expressions from [10]), the imaginary parts are overestimated, creating a mismatch between source/load and input/output, respectively, and leading to a lower PG and 1-dB compression point.

Table IV shows that the PG calculated using expressions from [10] and the present work lead to the same value because the additional parameters L_g, C_{pg}, C_{pd}, and L_d have no influence. When matching impedances from [10] are considered, however, the simulated PG is 1.4 dB lower than the calculated gain. On the other hand, when matching impedances from the new expressions in the current work are used, the calculated value of PG is close to the simulated one, about 0.116 dB lower. Finally, when impedances obtained via source/load–pull simulations are considered, the simulated PG is about 0.186 dB higher than the calculated value. The 1-dB compression point $P_{1\ \mathrm{dB}}$ also differs depending on the matching impedances: the $P_{1\ \mathrm{dB}}$ obtained with the new analytical expressions is very close to the one obtained with HB (4.03 and 3.96 W, respectively). On the other hand, $P_{1\ \mathrm{dB}}$ obtained with expressions from [10] is largely lower than the expected performance of the device (only 2.42 W), leading to worse linearity.

These new expressions are even more relevant for GaN HEMTs.

III. ANALYSIS OF POWER PERFORMANCE

A. PG

As pointed out in Section II, L_g, L_d, C_{pd}, C_{pg}, and C_{ds} have no significant influence on PG. For this reason, only the influence of R_g, L_s, C_{gd}, C_{gs}, and R_{opt} are evaluated. The calculated PG using parameters from Table III confirms that LDMOS presents better performance: calculated gain is equal to 22.144 dB for the LDMOS against 13.469 and 14.229 dB for VD_1 and VD_2, respectively (an average difference of 8.3 dB between the two structures). However, when the value of L_s in both VDMOSs is reduced to the corresponding value in LDMOS, the PG of the LDMOS is not attained, indicating a nonnegligible role of other parasitic parameters.

1) Role of a Single Parameter: Fig. 6 and Table V reveal that, among both vertical devices, different parameters cause the more important losses of PG—not necessarily the source inductance alone.

The gate-to-drain capacitance and the gate-to-source capacitance constitute the main cause of loss of PG, respectively, for VD_1 and VD_2. In case of VD_2, when C_{GS} is increased, the current through L_S rises, leading to a reduction of the output power, and thus, the PG. In case of VD_1, the Miller effect induces the same phenomenon: the impedance Z_{Miller}, in parallel with the gate-to-source capacitance, appears at the input of the current generator. When the value of C_{gd} is increased, the parallel association $C_{gs}//Z_{\mathrm{Miller}}$ also rises, increasing the current through L_s.

Following C_{gs} and C_{gd}, the source inductance is, in both cases, the second most important parameter that affects the PG.

Finally, resistive losses due to the higher gate resistance of the VDMOS seem the least important.

previous expression [10] gives a source impedance located on a cycle that is about 0.7 dB from $Z_{S,\mathrm{opt}}$. Similarly, the load impedance is calculated with more accuracy when the new expression is used: whereas the impedance calculated using [10] is located on the cycle that is 0.5 dB from the optimal impedance $Z_{L,\mathrm{opt}}$, the new expression gives an impedance located closer than the optimal value (about 0.05 dB). It is noticed that the imaginary value of the matching impedances is improved compared to previous expressions in [10]. This is due to the fact

Fig. 6. Evolution of the PG of vertical devices. Each parameter is gradually set to the corresponding value in the LD. On the x-axis, LD and VD correspond to the parameter values in LDMOS and VDMOS, respectively, with delta defined as $(Vd - Ld)/3$. C_{pg}, C_{pd}, L_g, L_d, and C_{ds} have no influence on PG.

Fig. 7. Percentage of LDMOSFET PG reached as a function of the value of g_m.

TABLE V
GAIN OF PG WITH RESPECT TO PARASITIC PARAMETERS

Parameter	VD$_2$		VD$_1$	
	PG [dB]	Gain of PG [dB]	PG [dB]	Gain of PG [dB]
R_g	15.4643	1.24	15.9250	2.45
L_s	16.0475	1.82	15.4523	1.98
C_{gs}	17.8666	3.64	15.2782	1.81
C_{gd}	15.3031	1.07	17.0374	3.57

TABLE VI
PERCENTAGE OF LDMOS' PG REACHED WHEN TWO
AND THREE PARAMETERS ARE OPTIMIZED

Parameters	% of LDMOS' PG reached		Parameters	% OF LDMOS' PG REACHED	
	VD$_2$	VD$_1$		VD$_2$	VD$_1$
R_g , L_s	82.64	93.86	L_s , R_g , C_{gs}	101.3	103.3
R_g , C_{gd}	74.47	84.96	L_s , R_g , C_{gd}	88.41	112.3
R_g , C_{gs}	84.78	78.62	L_s , C_{gd} , C_{gs}	104.15	110.6
L_s , C_{gd}	78.7	90.51	R_g , C_{gd} , C_{gs}	92.97	97.19
L_s , C_{gs}	92.83	80.31			
C_{gd} , C_{gs}	89.79	91.88			

This clearly demonstrates that the lower PG of vertical devices, usually attributed to the higher value of source inductance, is not necessarily correct. Since the loss in PG is due to the leakage current through the source, C_{gs} and C_{gd} must also be considered as elements of great importance to explain lower performance of the VDMOS. Beyond this, each vertical device must be individually considered in order to identify the parameter that causes the highest loss of PG for its optimization.

2) Influence of Many Parameters: When all parasitic parameters of the vertical devices, except the transconductance g_m and the load line resistance R_{opt}, are reduced to the corresponding LDMOS values, the calculated PG of the VDMOS structure is higher than that of the LDMOS. This is due to the higher values of g_m and R_{opt}, which tend to increase the value of the PG of the VDMOS.

Matching impedances and PG are next recalculated when two and three parameters are optimized simultaneously. These results are summarized in Table VI.

With two parameters simultaneously modified, a higher PG (about 93% of LDMOS for both devices) is attained with L_s and C_{gs} (VD_2) and R_g and L_s (VD_1). On the other hand, a lower PG is attained when $\{R_g, C_{gd}\}$ (VD_2) and $\{R_g, C_{gs}\}$ (VD_1) are optimized. This is expected since the braces $\{L_s, C_{gs}\}$ and $\{R_g, L_s\}$ have great influence in the loss of PG for, respectively, the first and second vertical devices (Table V).

The PG of LDMOS can be attained with the optimization of three parameters only (Table VI). This is due to the higher values of the transconductance and the load line resistance in the case of both vertical devices.

3) Influence of Transconductance: Apart from parasitic parameters, higher PG can be achieved via transconductance g_m. An assessment of the maximum PG attainable is given as the limit of (16) as the value of g_m approaches infinity

$$\lim_{g_m \to \infty} G = \frac{1}{\omega^2 \left[R_g C_{gd}^2 R_{opt} + L_s C_{gd} R_{opt} \right]} \quad (25)$$

$$\lim_{g_m \to \infty} G_{dB} = -10 \cdot \log\lfloor \omega^2 \left(R_g C_{gd}^2 R_{opt} + L_s C_{gd} R_{opt} \right) \rfloor. \quad (26)$$

Equations (25) and (26) correspond, respectively, to linear and logarithmic scales. Using values of parasitic parameters from Table III, this limit gives about 18 dB in the case of VD_1 and 24 dB in the case of VD_2. This means that, depending on the considered device, the PG of LDMOS is either not reached or is attained and even exceeded (in the case of VD_2, the LDMOS PG is attained from $g_m = 2.5$ S) with only the optimization of g_m. The increase of g_m also implies the increase of the output power and the 1-dB compression point. Fig. 7 shows the evolution of PG with respect to g_m for the considered devices.

4) Influence of Load-Line Resistance R_{opt}: The load-line resistance presented to the current generator is usually higher in the case of vertical structures than lateral ones [13]. When the values of R_{opt} in the VDMOS are set to the corresponding one in the LDMOS, the PG is depreciated (a decrease of about 1.5 dB is observed). This indicates that the higher value of R_{opt} together with transconductance can maintain the PG of the vertical device at a reasonable level compared to the LDMOS.

TABLE VII
PG AT SMALL INPUT LEVELS, OPTIMUM LOAD AND SOURCE IMPEDANCE
VALUES WHEN DEVICES ARE OPERATED AT 32 V

Method	$Z_S[\Omega]$	$Z_L[\Omega]$	$G_{sim}[dB]$	% of LDMOS	$P_{1dB}[W]$
VD_1	8.45+j7.38	6.75+j15.09	13.64	62%	4.8
VD_2	3.85+j2.84	5.29+j13.83	16.545	75%	4.2

A possibility to improve the PG is, therefore, to increase again R_{opt} by operating the transistor at higher drain quiescent voltage V_{dsq}.

R_{opt} is defined as [12]

$$R_{opt} = \frac{V_{max}}{I_{max}} = \frac{2\left(V_{dsq} - V_{knee}\right)}{I_{max}} \frac{2\pi\left(1 - \cos\left(\frac{\alpha}{2}\right)\right)}{\alpha - \sin\alpha} \tag{27}$$

where α is the conduction angle.

If V_{dsq} increases, the maximum voltage swing V_{max} is increased as the knee voltage V_{knee} remains constant. The maximum current swing I_{max} also remains constant so the load-line resistance value increases. From (9), it can be demonstrated that an increase of R_{opt} leads to an increase of the PG.

The two vertical devices are now operated at 32 V, instead of 28 V previously. The drain–source breakdown voltage of these devices (65 V for both devices) allows such an operation, though at a price of reducing the margin for reliability. Table VII summarizes results of new simulations. In both cases, the PG and the 1-dB compression point are improved. This is particularly true in the case of VD_2, where a 2-dB higher PG and an improvement of the $P_{1\,dB}$ (about 0.5 W) are observed.

This demonstrates that when drain–source breakdown voltage allows it, another alternative, without any optimization of parasitic parameters, is to present a higher load-line resistance to the current generator by increasing the drain bias.

B. Efficiency

In Section III-A.4, the role of parasitic parameters, optimal load–line resistance, and transconductance in the loss of PG have been determined. However, efficiency η and power-added efficiency (PAE) are also important characteristics in certain applications of amplification. Table II shows such characteristics in the case of the three considered devices and confirms the better performance of the lateral structure [1], [2]. In this comparison, the devices are biased so that they deliver the same drain current I_{dsq}.

Efficiency and PAE are calculated using the well-known formulas [13]

$$\eta = \frac{P_{RFout}}{P_{DC}} = \frac{P_{RFout}}{V_{DC} \times I_{DC}} \tag{28}$$

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}} = \frac{P_{RFout} - P_{RFin}}{V_{DC} \times I_{DC}}. \tag{29}$$

1) Influence of Parasitic Parameters: Similar to Section III-B, the role of each parasitic parameter is observed. L_g, L_d, C_{ds}, C_{pg}, and C_{pd} are now considered as they may
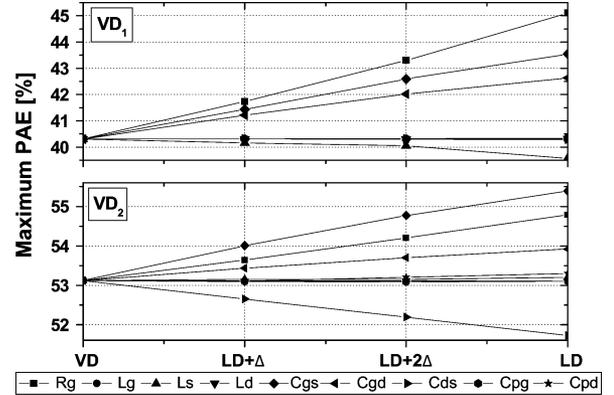
Fig. 8. Evolution of PAE when the value of each parasitic parameter in VDMOS is increased up to the one in LDMOS.

significantly influence the input power, and thus, the PAE. The obtained results are summarized in Fig. 8.

The resistive losses due to the gate resistance have the most important impact on the PAE; an enhancement of about 5% is observed when the value of R_g is reduced to the corresponding value in LD. C_{gs} and C_{gd} also play an important role. The other parameters have very negligible influence on the PAE.

The lower efficiency of the VD_2 compared to the lateral device is mainly due to its higher gate-to-source capacitance rather than it higher gate resistance. The resistive losses of R_g remains, however, an important parameter for the PAE. On the other hand, C_{ds} tends to maintain the level of the PAE: a depreciation of the PAE is observed when the value is reduced to the value of C_{ds} in the lateral device. The other parameters have a negligible influence on efficiency.

2) Influence of Load-Line Resistance: When a higher load-line resistance is imposed to the current generator, the PA exhibits a higher output power [see (22)]. Indeed, the higher load line resistance in the case of the VDMOS allows greater voltage swing (since V_{knee} is lower than in the case of the LDMOS) while the current swing remains similar to the LDMOS, leading to a higher output power.

The drain efficiency is directly related to the output power, and the PAE to the PG (see (22) and (23), respectively): at a given dc power, the drain efficiency increases with output power and the PAE with PG.

This demonstrates that the higher value of load-line resistance tends to maintain the level of the efficiency of vertical devices against the lateral counterpart. An easy way to improve the efficiency of the PA is to increase of the drain bias voltage, provided the device can sustain any possible surges of power during operation.

IV. STABILITY

The stability of a device is quantified through the k factor [14]. A convenient formula is given in [15] by

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{30}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$.
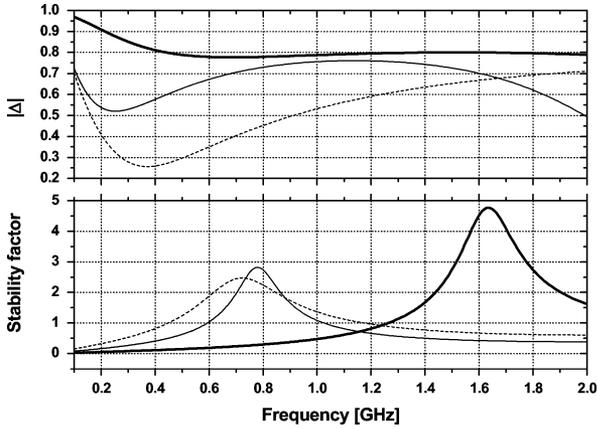
Fig. 9. $|\Delta|$ and stability factors plotted for the three devices from 100 MHz to 2 GHz. Bold line: LD; dashed line: VD_1; and line: VD_2.

Fig. 10. Influence of each parasitic parameter in the stability factor from 100 MHz to 2 GHz. Bold line: initial LDMOS; dashed line: parameter set to the one in the VD_1; line: the parasitic parameter is set to the corresponding one in D_2.

The amplifier is unconditionally stable when k is higher than 1 and $|\Delta|$ is lower than unity. If k is ranged between -1 and $+1$, the amplifier is then said to be potentially stable.

Fig. 9 shows the $|\Delta|$ and k factors for the three devices between 100 MHz–2 GHz. As demonstrated by Leong [2], the vertical device is potentially unstable at low frequencies only (below 400 and 600 MHz for VD_1 and VD_2, respectively), whereas the instability band extends at higher frequencies (up to 1.21 GHz) in the case of the LDMOS. The bands of unconditional stability are 0.4–1.2 GHz for VD_1, 0.6–1.01 GHz for VD_2, and 1.21–2 GHz for the lateral device. The potential instability outside these bands can cause a design challenge.

1) Influence of Parasitic Parameters: Fig. 10 shows the stability factor plotted when values of parasitic parameters in the LDMOS are optimized. The stability factor is not affected by L_g, L_d, C_{pd}, and C_{pg}.

Only the lower value of C_{gd} in the LDMOS contributes to maintain the unconditional stability at low frequencies: the device indeed becomes potentially unstable over the entire range of frequencies when C_{gd} is set to the corresponding values from VD_1 and VD_2 [see Fig. 10(d)].

Indeed, using the Miller transformation, the gate-to-drain capacitance is equivalent to the impedance Z_f

$$Z_f = \frac{Z_{C_{gd}}}{1-G} \qquad (31)$$

where $G = g_m V_{gs}$.

Z_f is in parallel with the source inductance. Thus, when the value of C_{gd} is decreased, the value of Z_f increases and the parallel association $Z_f // L_s$, which connect the source of the device to the ground, increases, improving the stability in the low-frequency region [16].

The other parameters are thus responsible for the poor stability of the lateral device below 1.25 GHz. When the gate resistance is increased, an offset is applied to the stability factor over the entire range of frequency, leading to a wider band of unconditional stability around the same center frequency [see Fig. 10(a)].
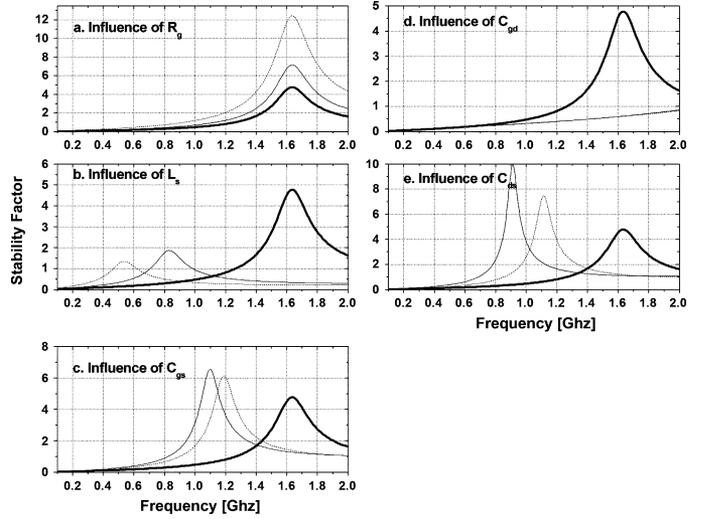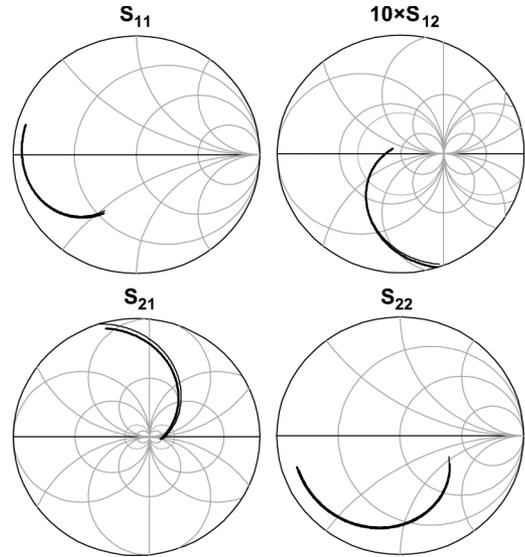
Fig. 11. Influence of the drain bias voltage on the scattering parameters. Bold line: $V_{dsq} = 28$ V; line: $V_{dsq} = 32$ V.

The decrease of C_{gs} and C_{ds} tends to shift the band of stability towards lower frequencies, but the resulting bandwidth is narrower [see Fig. 10(c) and (e)]. Finally, when L_s is increased up to VDMOS' values, the band of unconditional stability is largely shifted towards lower frequencies (around 0.5 and 0.8 GHz). However, a negative offset is applied to the range of frequencies, making the stability bandwidth narrower.

The band of unconditional stability for the LDMOS is narrower and at higher frequency, mainly due to the combined action of the low gate resistance that controls the bandwidth and the source inductance that controls the center frequency of the stability band. As underlined by Leong [2], a resistive loading of the gate can thus be used to overcome instability.

2) Influence of Load-Line Resistance: Fig. 11 shows the S-parameters of the lateral device when the drain of the device
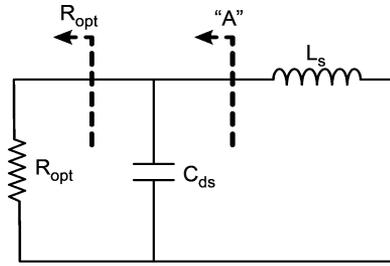
Fig. 12. Basic lumped elements low-pass matching network. The value of load-line resistance R_{opt} at plane "A" can be dramatically reduced by the value of the output capacitance.

TABLE VIII
VALUES OF LOAD-LINE RESISTANCES, OUTPUT CAPACITANCES AND
TRANSFORMED REAL COMPONENTS OF THE THREE CONSIDERED DEVICES

Device	R_{opt} [Ω]	C_{ds}	Re{Z_A} [Ω]
LD	29.9693	2.75 pF	23.632
VD$_1$	65.0483	6 pF	9.2746
VD$_2$	40.2271	9 pF	6.5148

is biased at 28 and 32 V. It is noticed that the difference between S-parametes is very small, the stability factor can be assumed equal between these two drain bias conditions. An enhancement of the load-line resistance, when the drain bias is slightly increased from 28 to 32 V, has no influence on the stability factor and can thus be considered when improving PG and efficiency (Section III).

V. OUTPUT MATCHING

As pointed out by Cripps [13], the unmatchability of RF transistors for power applications is not only due to the load-line resistance R_{opt}, but also to the output capacitance C_{ds}. Indeed, the real part of the load-line resistance can be dramatically reduced by the drain-to-source capacitance. At plane "A" (cf. Fig. 12), the real part of the impedance is

$$\mathrm{Re}\{Z_A\} = \frac{R_{\mathrm{opt}}}{1 + (\omega R_{\mathrm{opt}} C_{\mathrm{ds}})^2}. \tag{32}$$

Equation (32) reveals that the higher the value of output capacitance; the lower is the transformed real component at plane "A" ($\mathrm{Re}\{Z_A\}$). Values of the real part of impedance seen at plane "A" are calculated and summarized in Table VIII. The load line resistances are considered for the previous class AB operation.

Despite the fact that the vertical structure presents a higher load line resistance (about 65 and 40 Ω for D_1 and VD_2, respectively, against 30 Ω for the LD), the higher value of output capacitance C_{ds} (6 and 9 pF for VD_1 and VD_2 against only 2.75 pF for the lateral structure) reduces R_{opt} dramatically, making the vertical devices the least convenient structure for output matching.

VI. CONCLUSION

In this paper, new analytical expressions derived from a ten-elements model are developed for calculation of optimum matching impedances and associated PG. The inclusion of the drain and gate inductances shows significant improvement in

the determination of optimal matching impedances $Z_{S,\mathrm{opt}}$ and $Z_{L,\mathrm{opt}}$, as ascertained via HB simulations Using these expressions, a comparison of the RF performance between lateral and vertical DMOS has been performed. The role of each parasitic parameter has been identified to explain differences in RF performance. This study confirms the superiority of the lateral structure in terms of PG, efficiency, and output matching. It is confirmed that the latter is due to the lower value of output capacitance C_{ds} of the lateral device. However, this work reveals that the lower performance of the vertical device in terms of PG and efficiency are not necessarily due to any one element; the importance of parasitic parameters depends on each device technology individually. The most prominent of these are $C_{\mathrm{gd}}(VD_1)$ and $C_{\mathrm{gs}}(VD_2)$ to explain the loss of PG and $R_g(VD_1)$ and $C_{\mathrm{gs}}(VD_2)$ to explain the poor efficiency. The lateral structure suffers from worse performance of stability, mainly due to the lower value of R_g and L_s. Such knowledge of the quantitative role of each parasitic parameter is useful for design optimization of silicon MOSFETs technology used in RF applications. Given that process and device simulators yield little information about the RF performance of a device, this paper has described a methodology to achieve this challenge at low cost.

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