Advanced Control Design for Voltage Scaling Converters

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***Abstract*—In low-power electronics, achieving a high energy efficiency has great relevance. Nowadays, Global Asynchronous Local Synchronous Systems enables to use a Local Dynamic Voltage Scaling architecture, this technique allows achieve a high energy efficiency. Moreover, Local Dynamic Voltage Scaling can be implemented using different approaches. One of them is Vdd-Hopping technique. In this paper, different controllers are designed for a Vdd-Hopping system implemented in a novel discrete converter in order to search for control strategies that present better performance in terms of dissipated energy reduction. It is shown here that some of the provided control strategies not only reduce the dissipated energy, but also improves the current transients are improved.**

I. Introduction

The development of low-power electronics devices has raised up in recent years. Very-Large-Scale Integration (VLSI) is mostly used in information technology related products, such as PCs, mobile devices and digital consumer equipments. The future ubiquitous electronics needs gigantic number of chips and at the same time every chip should be implemented at the lower power level.

In a chip, several levels of supply voltages are required for reducing power consumption, therefore an integrated DC-DC converter is an important component. These converters have to generate voltages in the typical rage of $0.8V - 2.5V$ from a source of $3.3V$.

The most commonly used topologies in DC-DC converters in low power electronics are: continuous buck converters [5, 7, 8], boost converters [6] and buck-boost converters or charge pump [2], among others. Nevertheless, discrete converters can achieve a larger energy-efficiency, as the Power Supply Selector (PSS) presented in [4], which deal with Local Dynamic Voltage Scaling (LDVS) [1, 9] adapted to Globally Asynchronous and Locally Synchronous Systems (GALS) [3]. The main idea for GALS system is to replace the global clock by several independent synchronous blocks which operate with an own internal clock and they are communicated asynchronous by each other. This mode of operation provides additional flexibility which allows to use energy-aware converter structures such as Dynamic Voltage Scaling (DVS) architectures.

DVS modifies the voltage supply processor in order to minimize the amount consumed energy; the processor will work at the minimum performance level required by the processes activity.

In this case, LDVS is based on Vdd-hopping technique which fulfills LDVS by dynamically changing supply voltage V_{dd}. Operation principle is to use two voltage levels instead of a continuously adjustable voltage. Vdd-hopping system is made up of a discrete DC-DC converter called Power Supply Selector with the two voltage levels refereed before.

The main control problem in low-energy DC-DC converters is to achieve a high energy-efficiency, a low cost and a reduced size. DC-DC converters must be able to adapt to various loading conditions and achieve high efficiency over a wide load-current range, which is critical for extended battery life. Moreover, keep the rate of change of the device voltage providing a correct and reliable operation during the switch transition is also important.

A simple discrete controller was proposed to handle the two-voltage level Vdd-hopping structure proposed by [4]. In this control structure only one transistor can be switched at each sampling period. This limits the ability to the converted to make fast transitions, and hence the possibly to optimize the energy consumption. In this paper, we propose a set of alternative controllers, developed for improving the tracking capability and its regulation characteristic with respect to varying loads. As a side effect it is also observed that the energy-efficiency of Vdd-hopping system is improved, and that the transient current peaks are also reduced. The controllers are developed assuming that more than one transistor can be switched on or off.

The paper also compares our results to the intuitive controller proposed in [4] in terms of transient responses, quality of the induced load current and energy dissipated by the switches transistors.

The different controllers are tested and compared in Matlab simulations.

The rest of this work is organized as follows: in Sect. II the circuit model of the Vdd-hopping is presented just as its properties and the error equation for fulfilling a tracking. This model is used for designing different controllers in Sect. III. An evaluation performance of the controllers is seen in Sect. IV. In Sect. V the dissipated energy during the transition for the different developed controllers is evaluated. A general discussion of the controllers performance is made in Sect. VI.

The work closes with a section of conclusions.

II. Model of the Vdd-hopping

The aim of DC-DC converters in portable electronic systems is to obtain a high efficiency, low cost, reduced size and low noise, since the battery capacity is limited in any portable electronic device. These converters can further enhance battery run-time.

A. Electrical model

There is a novel discrete DC-DC converter presented in [4] called Power Supply Selector (PSS) which principal advantages are: it has a reduced size, negligible dissipated energy, low cost and it does not need passive components. It uses the technique Vdd-hopping for getting a Local Dynamic Voltage Scaling (LDVS) architecture for a globally asynchronous and locally synchronous system.

Vdd-hopping is basically made up, as it is shown in Fig. 1, of a PSS and two external supply voltages which will provide a high voltage level, V_{high}, for a unit running at nominal speed and a low voltage level, V_{low}, for a unit running at reduced speed. For simplicity, a voltage supply is considered, V_{high}, accomplishing the two voltage levels with this only voltage supply. With this assumption about the supply voltage, at least one transistor must be always switched on. v_c is the voltage output of the system.

PSS is constituted for a group of PMOS transistors connected in parallel with common drain, source and bulk but separated gates in order to scale the output voltage from V_{high} to V_{low} and vice versa. Moreover, there is a PMOS transistor which connects the V_{low} to the output just on time that the last transistor of the set of PMOS is switched-off; this is made for reducing the energy dissipated when the unit running at low speed. Other component in the PSS is a control block commands the PMOS transistors and a signal comparator. The control block has as inputs: a clock (CLK), a signal which orders the starting hopping sequence (LPM), and the signal from a comparator, and as outputs the control signal for commissioning the switch of the PMOS transistors. The desired reference voltage is v_r, and it is given by the designer as a time-function, usually with a constat slope.

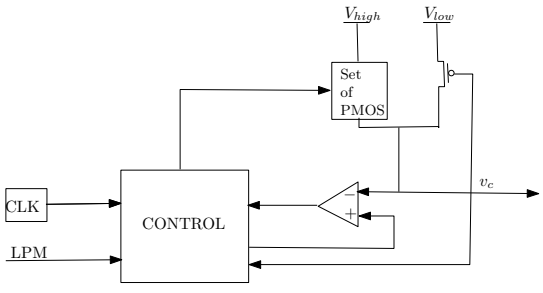

Fig. 1: Power Supply Selector Architecture

The load model for this kind of low-power system usually is an impedance which depends on the chip frequency, f, and also on the core voltage, v_c. It is shown in Fig. 2. The load model can also be completed with a leakage current source due to the aggregated effect of the PMOS leaks transistors.

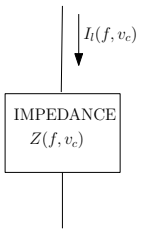

Fig. 2: Load model

B. Electrical model for control design

Figure 3 shows an electrical representation of the Vdd-hopping with the voltage supply, V_{high} together with the load.

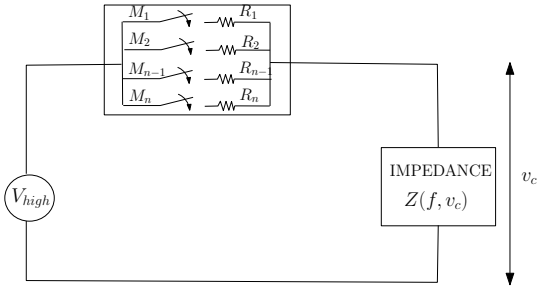

Fig. 3: Vdd-hopping, voltage supply and load

Assumption 1: The PMOS transistors are modeled as ideal resistors when they are switched-on. They are considered to have the same electrical characteristics.

Letting $V_h = V_{high}$, the voltage loop equation yields the relation

$$I_l(v_c) = \frac{V_h - v_c(t)}{R(u_k)} \tag{1}$$

where $R(u_k) \triangleq \frac{R_0}{u_k}$ being u_k the number of transistors switched on, therefore, $u_k \in \mathcal{U} = \{1, 2, ..N\}$ and it will be the control law. On the other hand, R_0 is the transistor electrical characteristic, that in this case, is the same for all transistors $R_0 = R_1 = R_2 = \ldots = R_N$.

I_l, that is the current through the set of PMOS transistors, depends only on the $v_c(t)$, since the frequency on the load depend on the $v_c(t)$ in this system, therefore it will vary during the hopping transitions.

Combining the specific form of the load impedance with (1), the voltage dynamic expression can be compactly expressed as:

$$\dot{v}_c(t) = -\beta(v_c)v_c(t) + b(V_h - v_c(t))u_k - \delta \tag{2}$$

where:

- $\beta(v_c) > 0$ depends on the load.
- b and δ depend on the parameters of the system and they are positives.

Note that (2) is a nonlinear system

$$\dot{v}_c(t) = -f(v_c) + g(v_c)u_k - \delta \quad (3)$$

Property 1: The system (3) has the following properties

i) $f : D \to \mathbb{R}^+$ and $g : D \to \mathbb{R}^+$ are globally Lipschitz from a domain $D \subset \mathbb{R}^+$ into $\mathbb{R}^+$

ii) f and g are positive-semidefinite

iii) the state v_c is strictly positive

iv) $\delta \in \mathbb{R}^+$ can be seen as a constant perturbation

Letting rewrite the system (2)

$$\dot{v}_c(t) = -(\beta(v_c)(bu_k + v_c(t)))v_c(t) + bV_h u_k - \delta$$

the associated error equation is:

$$\begin{aligned} \dot{e}(t) &= -(\beta(v_c) + bu_k)e(t) \\ &\quad +(bu_k + \beta(v_c))v_r(t) - bV_h u_k + \delta + \dot{v}_r \end{aligned} \quad (4)$$

which can be compactly written as:

$$\dot{e}(t) = -(\beta(v_c) + bu_k)e(t) + \beta(v_c)v_r(t) + \varrho \quad (5)$$

where $\varrho = bu_k v_r(t) - bV_h u_k + \delta + \dot{v}_r$. As u_k, v_r, and v_c are bounded signals (u_k belongs to a finite set of integer values, and v_c is the output of a passive circuit), then we have that $\varrho \leq \varrho_0$, where ϱ_0 is some positive constant.

The following theorem shows that the error system is open-loop stable.

Theorem 1: Consider the following:

1) $v_c(t)$ and $v_r(t)$ are such that $v_c(t) \in F \subset \mathbb{R}^+$, for all t, where F is a bounded subset of positive real numbers, and $v_r(t)$ is a bounded reference,
2) $\beta(v_c) > 0, \forall v_c \in F$,
3) $\varrho \leq \varrho_0$, with $\varrho_0 > 0$

then System (4) is globally stable in the sense that for all initial condition $e(0)$, the solutions $e(t)$ tend to a ball of radius r_0.

Proof: Following Lyapunov's arguments, we take $V_0 = \frac{e^2(t)}{2}$ and taking time-derivatives, together with assumptions $1-3$ of the Theorem, we have

$$\begin{aligned} \dot{V}_0 &\leq -(\beta(v_c) + bu_k)e^2(t) + e(t)(|\beta(v_c)||v_r(t)| + \varrho_0) \\ &= -e^2(t)\left[(\beta(v_c) + bu_k) - \frac{|\beta(v_c)||v_r(t)| + \varrho_0}{|e|}\right] \leq 0 \end{aligned}$$

Then $\dot{V}_0$ is negative-semidefinite as long as the term in the square brackets is positive, i.e.

$$\beta(v_c) + bu_k \geq \frac{|\beta(v_c)||v_r(t)| + \varrho_0}{|e|}$$

or equivalent in the e domain, if

$$|e| \geq \frac{|\beta(v_c)||v_r(t)| + \varrho_0}{\beta(v_c) + bu_k} = \frac{|v_r(t)| + \frac{\varrho_0}{|\beta(v_c)|}}{1 + b\frac{u_k}{|\beta(v_c)|}} := r$$

Note that the function r is positive, and monotonically in its argument v_c. In the System (4), $\beta(v_c)$ increases with v_c, thus the two limit values of r are, $r_1(t) = \lim_{v_c \to 0} r = |v_r(t)|$, and $r_2(t) = \lim_{v_c \to \infty} \frac{\varrho_0}{b|u_k|}$, therefore, the radius r_0 can be defined as:

$$r_0 = \sup_{t \geq 0} \max\{r_1(t), r_2(t)\}$$

■

III. Control laws

As it was seen before, the system (1) is a stable first order nonlinear system. Nevertheless, in low-power system there is certain requirements like minimal dissipated energy, minimal current peaks through the set of PMOS, minimal transition time, etc, which can be achieved with a suitable control law.

The objective of this section is to present three alternative control strategies to the one used in the original work [4]. All these controllers are designed to provide stable behaviors, and different control methodologies are used in each case.

A. An intuitive control

The original problem raised by the authors of [4] is a tracking problem of the voltage v_c respect to a time-varying reference voltage signal. The control implemented by the authors is

$$u_{k+1} = u_k + sign(e)$$

where e is the tracking error ($e(t) = v_c(t) - v_r(t)$), as defined before, and u_k is the control law. As this controller has been designed from intuition, we named here 'intuitive control'. With this control law, one only transistor can be switched on or off at every sampling time. For the development of other controllers, we are going to assume that more than one transistor can be switched on or off at the same time period.

The number of transistors used is $N = 24$. Note that there is always, at least, one active transistor. The voltage supply is $V_h = 1.2V$. $v_r(t)$ follows a linear time evolution between $V_{low} = 0.8V$ and $V_h = 1.2 - \Delta$, with a slope specified by the user.

Remark 1: The achieved maximal voltage, v_c, must be $V_{max} = V_h - \Delta$ where $\Delta \in \mathbb{R}$ and is small. It depends on the voltage supply, the PMOS transistors electrical characteristic and the load.

Taking the data reported in [4], the PMOS transistors have a value $R_0 = 31.41\Omega$, the capacitance is $C = 9nF$, the threshold voltage is $V_{th} = 0.4V$, and clock frequency system is $f = 500MHz$. The transition time for rising or falling is $300ns$. The slope of v_c is $1.015 \cdot 10^6 V/s$ and Δ is $0.09V$.

In Fig. 4, a simulation of this controller is shown by using Matlab. Note that the current through the transistors, as expected, presents peaks every time that a PMOS is switched on or off.

In what follow, we propose other control alternatives, which are designed under the hypothesis that several transistors can be switched on or off simultaneously, as long as the number of transistor is limited by 1 or N.

B. Controller No. 1: linear controller

The first controller is a linear one, designed to cope with possible steady-state errors. This controller is not based on the explicit knowledge of the system. The proposed control law is:

$$u_k = u_{k-1} + K_1(e_k - \varphi_k) + K_2 e_k$$

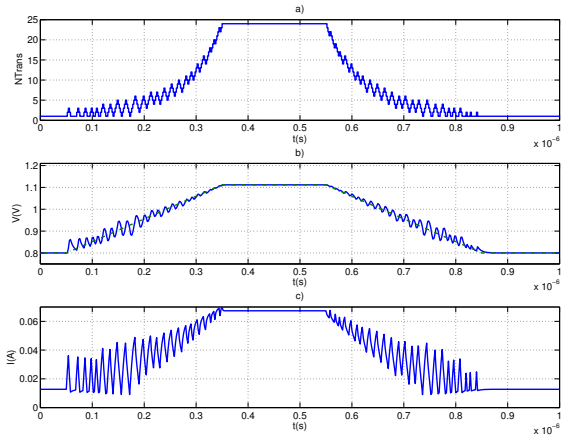

Fig. 4: Intuitive control. a) Evolution of the number of switched-on PMOS, b) evolution of the v_r (dashed) and evolution of v_c (solid). c) evolution of the current I_l.

where K_1 and K_2 are positive constants and φ_k is a function of the past values of e_k.

This control law can be shown to display the suited stability properties, with the ability to compensate for unknown and slowly time-varying leakage in the load.

Figure 5 shows a simulation of this control strategy. This controller could be the most suitable for physic implementation, since it does not require model information and it provides a good performance in both voltage and current variables respect to the intuitive control, although it has more oscillation in the current signal than using the others controllers.

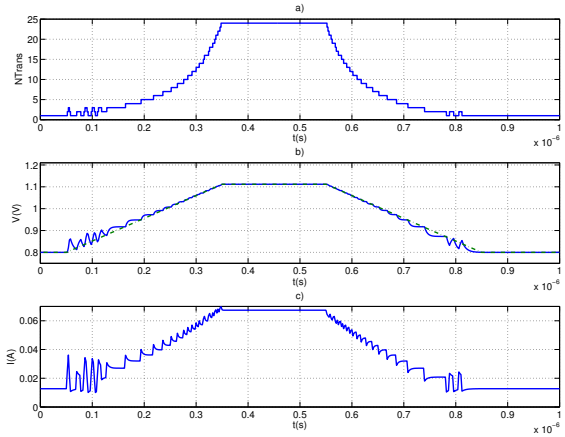

Fig. 5: Control No.1. a) Evolution of the number of active PMOS, b) evolution of the v_r (dashed) and evolution of v_c in blue. c) evolution of the current I_l.

C. Controller No.2: linearization by feedback

For the second proposed controller is designed by using feedback linearization technique. This lead to an approximate linearized system in closed loop, as the control inputs are discrete, and the error equation continuous in time.

Under the realistic assumption, that the control variable is limited to the discrete interval $\{1, N\}$. The controller No.2 has the following discrete-time form:

$$u_k = \frac{bT(v_{rk} - e_k - V_h)u_{k-1} - K_3T(e_k - \varphi_k) - K_4e_kT}{bT(\varphi_k - e_k + v_{r_k} - v_{r_{k-1}} - V_h)} + \frac{-T\beta_k(v_c)(v_{r_k} - v_{r_{k-1}}) - \delta T - v_{r_k} + 2v_{r_{k-1}} - v_{r_{k-2}}}{bT(\varphi_k - e_k + v_{r_k} - v_{r_{k-1}} - V_h)}$$

where K_3 and K_4 are positive constants, $T = \frac{1}{f}$ is the sampling time and φ_k is a function depending on the past values of e_k.

The gains of this controller are adjusted using information from the system, that is, using the explicit knowledge of $\beta(v_c)$, b and δ. Nevertheless, some level of robustness with respect to this information is inherent to the control methodology.

The simulation results using controller No.2 are shown in Fig. 6.

Observe, that the current peaks have been reduced considerably, achieving a smoother current signal. Moreover, the voltage evolution tracks to the voltage reference without hardly oscillation. Therefore, the dissipated energy will be reduced, as it will be seen below.

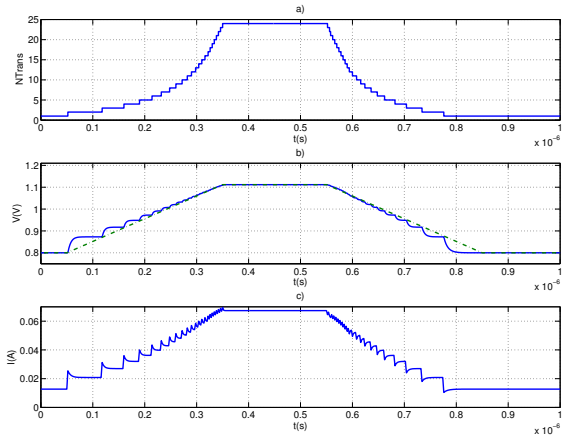

Fig. 6: Control No. 2. a) Evolution of the number of switched-on PMOS, b) evolution of the v_r (dashed) and evolution of v_c (solid). c) evolution of the current

D. Controller No.3: Lyapunov-based design

The last proposed controller, Lyapunov's stability arguments are used.

Taking a Lyapunov function candidate, the control law can be now designed so that the time-derivative of the function $V(e)$ is definite negative. As the system is open-loop stable, it only resumes to cancel time-dependent terms resulting from the tracking problem considered here. In this case, the controller contains only feedforward terms used to accommodate the system trajectories to those of the desired reference. As

before this control law will depend explicitly of the system model.

The control law resulting from this approach is of the form

$$u_k = \frac{bT(v_{r_k} - V_h)u_{k-1} - T\beta_k(v_c)(v_{r_k} - v_{r_{k-1}})}{bT(v_{r_k} - v_{r_{k-1}} - V_h)} + \frac{-\delta T - v_{r_k} + 2v_{r_{k-1}} - v_{r_{k-2}}}{bT(v_{r_k} - v_{r_{k-1}} - V_h)}$$

A simulation of this controller is shown in Fig. 7. As it can be seen, it also reduces the current peaks. The voltage and current evolutions are smoother than using the controller No.2, obtaining an important dissipated energy reduction. Note, moreover, that this controller is more simple than the controller No.2, therefore, it will be easier to implementation.

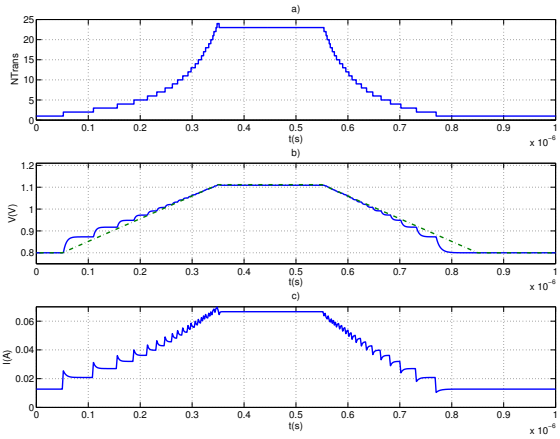

Fig. 7: Control No. 3. a) Evolution of the number of switched-on PMOS, b) evolution of the v_r (dashed) and evolution of v_c (solid). c) evolution of the current I_l.

IV. Performance evaluation

A performance evaluation is made in this section of the different controllers presented before.

The voltage signal is evaluated by means of the error of the voltage v_c respect to its reference v_r. This evaluation is made computing the mean and variance error. The current signal is evaluated for the maximum current peak produced.

The following table present the mean error, variance and maximum current peak.

	Mean Error	Variance Error	Max. Current peak
Intuitive	$3.32 \cdot 10^{-3}$	$6.42 \cdot 10^{-5}$	$4.0 \cdot 10^{-2}$
No.1	$2.65 \cdot 10^{-3}$	$3.08 \cdot 10^{-5}$	$2.5 \cdot 10^{-2}$
No.2	$2.49 \cdot 10^{-3}$	$3.01 \cdot 10^{-5}$	$0.5 \cdot 10^{-2}$
No.3	$3.11 \cdot 10^{-3}$	$5.94 \cdot 10^{-5}$	$0.5 \cdot 10^{-2}$

TABLE I: Table of parameters for performance evaluation

Note, that the controller No.1, No.2 and No.3 improve the tracking error of the voltage signal respect to the intuitive control. Note that this tracking error is larger using the controller No. 3 than using the controller No. 2, that is why the controller No.3. only contains feedforward terms doing the voltage evolution smoother.

On the other hand, the maximum current peak is much smaller using the controllers developed in this paper than using the intuitive control, getting the smaller maximum current peak with the controller No.2 and No.3.

V. Energy evaluation

The dissipated energy during the transitory in the set of PMOS depends on the type of employed control law; thus on the switching sequence. For instance, oscillatory current profile can be obtained with certain controllers. This non-smooth behavior of the current transient may result in a higher energy consumption.

As energy can be quantified precisely for a given voltage reference profile, the purpose of this section is to evaluate the energy cost associated with each of the controllers presented in previous section.

It can be visually observer from the simulations presented before that due to the smoother behavior of both voltage and current obtained with the controller No.1-3, their energy consumption, when compared to the intuitive controller will be improved.

This observation is corroborated in Fig. 8 which shows the dissipated energy,

$$E = \int_{t_0}^{t_f} VIdt$$

in the PMOS transistors during the rising transitory, t_0 is the initial transition time and t_f is the final transition time (assume that the falling transitory is similar). Note that the largest dissipated energy is accomplished with the intuitive control. And the smallest dissipated energy is got with the controller No.3, since it has the smallest current peaks, as it is seen in Fig. 7, and the smoothest voltage evolution (as it was seen before). Noting the Fig. 5 and Fig. 6 it is easy to understand that the energy dissipated using the controller No.1 is larger than using the controller No.2 or No.3.

The cumulate dissipated energy in the time interval from the time that the LPM orders to start the rising transitory, until that the V_h is reached are given in the next TABLE II

DISSIPATED TOTAL ENERGY (J)	
Intuitive control	$7.17 \cdot 10^{-6}$
Control No.1	$6.86 \cdot 10^{-6}$
Control No.2	$6.20 \cdot 10^{-6}$
Control No.3	$4.86 \cdot 10^{-6}$

TABLE II: Table of the energy dissipated

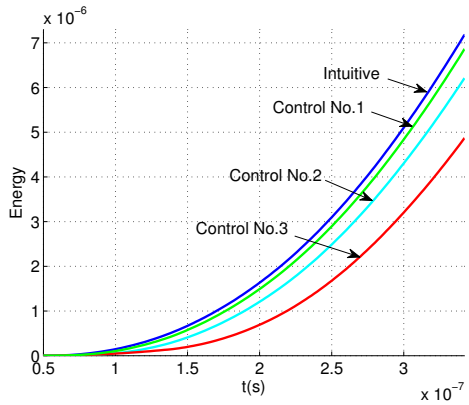

Fig. 8: Energy dissipated during the rising transitory

VI. Controllers global performance: discussion

The intuitive control proposed by the authors in [4] has been shown to provide a reasonable tracking at expenses of an oscillatory behavior due to its own limitation of one step variation at time. However current signal time-profiles present high frequency behaviors with some substantial peaks, in particular when the total PMOS parallel resistances are larger. This seems to be the main cause of larger dissipated energy.

Controller No. 1, is a linear controller which does not need any model knowledge, making easy and more robust its implementation. This controller also reduces the current peaks produced by using the intuitive control. The dissipated energy reduction is in this case a 4.32%, when compared to the intuitive controller.

Controller No.2 yields a smother current and voltage time-profiles, reducing the current peaks, but it requires system knowledge. In terms of a consumed energy per voltage transition, this controller improves the intuitive control by 13.52%. We can also note a slight phase delay, in particular in the low-voltage zone.

Controller No.3, requires also model knowledge. This controller yields the smoother behavior with respect both voltage and current time-profiles. The reasons is that this design yield a controller that basically contains feedforward terms only. The stabilization of the system is insured by the inherent stabilization properties of the open-loop system. In spite of that, this controller improves a 32.77% the energy use when compare to the intuitive control.

Controller No. 3 with respect to others tested controllers allows a substantial improvement in the performances of both: energy cost (which depends on the current peaks) and voltage tracking (e.i. mean and variance voltage error). Controller No. 3. can be a good option for improving the energy efficiency in the Vdd-hopping system.

VII. Conclusion

In this work different controllers are designed for the Vdd-hopping with the aim of reducing the dissipated energy, minimizing the current peaks in the set of PMOS transistors. These controllers have been compared with the intuitive control used in [4]. Most of these controllers get, in general, better performance in terms of transient responses and/or dissipated energy. Their results come from the possibility to let such controllers to switch more than one transistor at once.

From this evaluation, the controller No.3 seem to be the most suitable for the final implementation, since it improves the energy efficiency as well as the tracking voltage. As future work, these results will be validated by using VHDL-AMS simulators, since the Vdd-hopping system with the load is an hybrid system (the control will be implemented digitally) between analog and digital elements.

Acknowledgment

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