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***Abstract*— In this paper, we address the architecture of multistandard simultaneous reception receivers and we aim at improving both the complexity and the power consumption of the analog front-end. To this end we propose an architecture using the double orthogonal translation technique in order to multiplex two received signals. A study case concerning the simultaneous reception of 802.11g and UMTS signals is developed in this article.**

***Index Terms*— double orthogonal frequency translation, multistandard simultaneous reception, power consumption, complexity.**

I. Introduction

In the wireless telecommunications embedded domain, we can observe a request of multiple functionalities expected from the devices also impacting on the classical constraints of power consumption and complexity. Several new services have appeared such as video streaming and high-speed data transfer. They either use already existing wireless standards or need new dedicated ones. Because of the need for using simultaneously different services and therefore different standards, the transceivers able of processing simultaneously several standards have to be developed.

In this paper we focus on the reception part of a multistandard simultaneous processing transceiver. The present state of the art is using stacked-up dedicated front-ends in order to simultaneously receive several standards. One of its major drawbacks is the bad performance-power-complexity trade-off due to the parallelization of the processing stages.

In order to obtain a better trade-off, we propose a new architecture for multistandard simultaneous reception inspired by the image rejection double IQ architecture [1]. It uses a single front-end capable of multiplexing the two input signals, once separately filtered and amplified, of translating the resulting signal in the baseband domain and then of demultiplexing the two signals in the digital domain.

This paper consists of three parts. Following this introduction, section II describes this novel architecture and shows simulated results of the simultaneous 802.11g/UMTS reception, further details have been already published [2]. In section III a comparative power consumption study between the proposed architecture and the state of the art is presented. It consists in a theoretical study using power models for each block [3] and a state of the art of analogical circuits used by the two architectures [4]-[9]. Finally, conclusions of this study are drawn.

II. Double IQ Multistandard Simultaneous Reception Architecture

In wireless telecommunications, the integration of IQ baseband translation structures in the receiver chain has become a common procedure. The simple IQ architecture is usually used in the receiver front-end design in order to reduce the bandwidth of baseband signals treated by the ADC.

Meanwhile, the orthogonal frequency translation technique is also used to eliminate the image frequency during the translation steps of heterodyne front-end architectures [1]. The image frequency rejection technique consists in using two orthogonal frequency translations. After the double orthogonal translation, a signal processing block uses the four baseband signals to eliminate the image frequency signal.

This monostandard image rejection architecture relies on the advantage of orthogonalizing the useful signal and the signal occupying its image frequency band. Even though the spectrums of the two signals are completely overlapped after the first frequency translation, this orthogonalization allows the baseband processing to theoretically eliminate the image frequency component while reconstructing the useful one.

This paper assesses the use of the double orthogonal translation technique to develop a multistandard simultaneous reception front-end [2]. The main idea is to consider that the signal from the image band becomes another useful signal. The architecture and the spectrum evolution of such a receiver, able of treating simultaneously two standards, are developed in Fig. 1. The parallelization of the input stages of the front-end imposes the use of two dedicated antennas, two dedicated RF band filters and two dedicated LNAs. The gain control stage is realized by the input stages, each LNA being dedicated to the gain control of one of the signals. Once the two signals are well filtered and amplified, an addition of the two outputs is made. The resulting signal is then processed by a double orthogonal translation structure. The frequency of the oscillator used by the first stage is ably chosen in such a manner that each of the two useful signals occupies a spectrum in the image band of the other. This implies a complete overlapping of the spectrums of the two signals in the intermediate frequency domain. After the second orthogonal frequency translation and after the digitalization of the four resulting signals, two parallel processing are implemented, each of them composed of a series of basic operations. Each of them reconstructs one of the two useful signals, while rejecting the other. As a result, the output

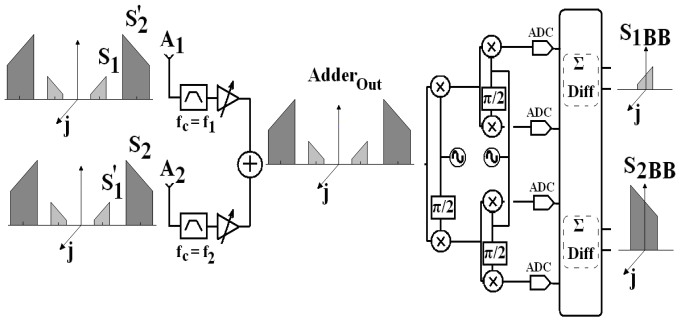

Fig. 1 High complementary standard rejection multistandard simultaneous reception architecture.

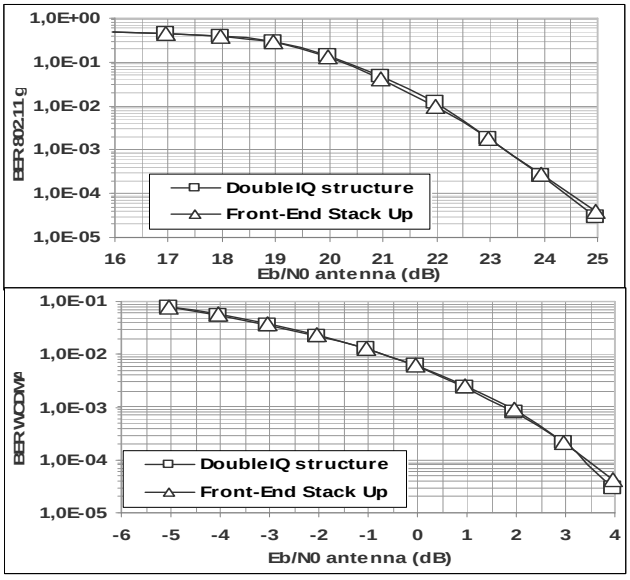

Fig. 2 802.11g and WCDMA BER evolutions during multistandard simultaneous reception using the two types of receivers

signals of this final block are the two useful signals translated in baseband.

The choice of the standards used for our study case is WLAN (802.11g) and WCDMA-FDD because of their growing importance. Several simulation of the structure presented in Fig. 1 were performed using the ADS software provided by Agilent Technologies. One of this series of simulations concerns the BER (Bit Error Rate) evolution of the two study case standards when being simultaneously received by a structure using the state of the art front-end stack-up architecture and the proposed double IQ architecture.

In order to achieve a good performance comparison between the multistandard single frond-end receiver and the front-end stack-up, the blocks used during the simulation have the same typical metrics (gain, noise figure, 1 dB compression point, third order interception point) in both cases. As it can be seen from Fig. 2 the performance of the two architectures during the simultaneous reception of the two standards is almost identical. Meanwhile, these simulations do not take into account the orthogonal mismatches of the IQ translation blocks. An additional study concerning this issue has been made and will be presented in an extended version of this paper. The conclusions impose a basic digital algorithm (Least Mean Squares) in order to mitigate the impact of these

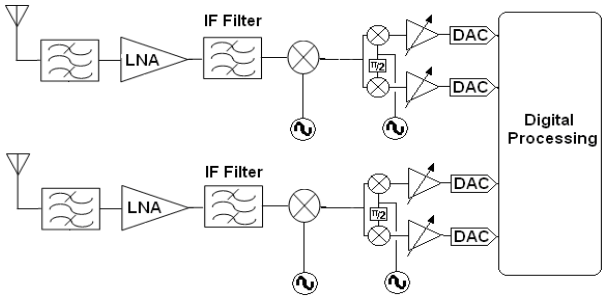

Fig. 3 State of the art of simultaneous reception - Stacked-up heterodyne dedicated front-end architecture.

mismatches on the signal quality. For our study case the results obtained by using this adaptive algorithm show a complete mitigation of the IQ mismatches. In the same time, the same study concludes that the power consumption of this algorithm is not significant compared to that of the whole receiver composed of the analog front-end described here and of the digital signal processing part.

III. Power And Complexity Issues

When designing an embedded front-end, the main issues to be considered are the power consumption and the complexity of the structure. Generally these two issues are related: the growing complexity involves the use of spare elements which increases the power consumption. In this paper we propose an innovating architecture which allows the reduction of the analogical front-end power consumption and complexity during a multistandard simultaneous reception. In order to reveal these reductions, this section presents a study comparing the proposed structure to the state of the art of the multiband simultaneous reception architecture – the front-end stack-up.

While evaluating the performances of the proposed structure, it can be seen that it has the same advantages and the same drawbacks as the stack-up structure using two heterodyne front-end. Therefore the comparison will be made between the double IQ structure presented in Fig. 1 and the stacked-up heterodyne dedicated front-end architecture presented in Fig. 3.

The theoretical part of the power comparison study relies on energy models of each type of block used in the two architectures. These energy models are presented in [3], along with a system level energy evaluation. In order to realize a global evaluation of the power consumption of the two structures, the theoretical study takes into account the state of the art of each block used by the two structures, in terms of performance-power trade-off.

A. Filters

There are several analog filters in the analog part of a receiver. These include the RF band select filter, used to suppress the wideband interference signal, the IF filter, used to suppress the interference signal from the image frequency band, and the baseband low-pass filter, used to suppress in-band interference while also helping with the anti–aliasing

problems of the ADC. Passive filters, such as the RF band select filter and the IF filter, do not consume quiescent power and therefore are not included in the global power model.

B. LNA and Mixers

The power consumption model of the mixers used in the two structures, it is a function of the noise figure NF and the gain K:

$$P_{mixer} = k_{mixer} \cdot K / NF \ . \quad (1)$$

In the followings we consider that all the mixers used in the two architectures have the same performances constrains in terms of gain and noise figure and therefore have the same power consumption. One of the better suited mixers offering an excellent performance–power trade-off is presented in [4]. It has a power consumption of 5.6 mW.

The power model of the LNA is similar to that of the mixers as it also depends on the noise figure NF and on the gain A:

$$P_{LNA} = k_{LNA} \cdot A / NF \ . \quad (2)$$

For our study case the two structures use the same couple of dedicated LNAs. The state of the art show a power consumption of 8.04 mW for the WLAN dedicated LNA [5] and of 7.2 mW for the UMTS dedicated LNA [6]. In this study we assume that the power control is performed by the LNAs. This assumption doesn't influence the power study as the LNAs' highest consumption level appears when it operates in the high gain mode.

C. Baseband Amplifier

The baseband amplifier (BA) is used to amplify the signal before conversion. It improves the SNR (Signal to Noise Ratio) of the signal, allowing a better BER. Its power consumption depends on its gain and on its bandwidth:

$$P_{LNA} = k \cdot BW \cdot \sqrt{a_{BA}} \quad (3)$$

where the k coefficient depends on the device dimensions and other process parameters. a_{BA} is the baseband amplifier gain and is assumed to be $a_{BA} = 5$. Here we assume that the UMTS dedicated BA consumes 5mW [3] and the WLAN dedicated BA consumes 10 mW as it has a two times larger bandwidth. For the proposed structure, the BAs are assumed to consume 10 mW.

D. Frequency Synthesizer

Concerning the frequency synthesizer's power consumption, it has a model composed of two separate components: the power consumed by the VCO (Voltage Controlled Oscillator) and that consumed by the PLL (Phase Lock Loop). The consumption of the phase lock loop has a model depending on the reference frequency F_{ref}, on the RF frequency F_{LO}, on the total capacitances C_1 and C_2 loading the RF circuits and on supply voltage V_{dd}:

$$P_{PLL} = b_1 \cdot C_1 \cdot V_{dd}^2 \cdot F_{LO} + b_2 \cdot C_2 \cdot V_{dd}^2 \cdot F_{ref} \quad (4)$$

An LC tank-based VCO has a power model depending on the values of the elements of the LC tank R, L, C, on the noise excess factor NEF along with the phase shift where it is measured $\Delta\omega$, on the phase noise power spectral density S_Φ, on the temperature T and on the Boltzmann constant K:

$$P_{VCO} = C \cdot \left(\frac{R}{L}\right)^3 \cdot NEF \cdot \frac{k \cdot T}{S_\Phi} \cdot \frac{1}{(\Delta\omega)^2} \quad (5)$$

The central frequencies of the state of the art synthesizers used by the two architectures are practically the same, as well as the other metrics. A well suited element is presented in [7]. It consumes 42 mW for an output frequency between 2.6 GHz and 2.9 GHz and a phase noise of -115dBc/Hz @1MHz.

E. Analog to Digital Converters

The analog to digital converters, along with the number of frequency synthesizers, are the key elements of this power consumption comparative study. In fact, except for the ADC and the baseband amplifiers, all the elements used by the two architectures need to fulfill the same performance constrains.

The power model of the ADCs can be defined by:

$$P_{ADC} = \frac{V_{dd}^2 \cdot L_{\min} \cdot \left(f_{sample} + f_{signal}\right)}{10^{(-0.1525 \cdot N_1 + 4.838)}} \quad (6)$$

where N_1 is the resolution of the A/D converter and L_{min} is the minimum channel length of the used CMOS technology. For our study case, the f_{sample} for the UMTS is the same as that of the WLAN, even if the signal has a bandwidth two times smaller, because of the over-sampling that has to be done for this standard. Concerning the ADCs used by the proposed structure, the sampling frequency is equal to that of the WLAN dedicated ADC as the bandwidths of the signals to be digitized in the two cases are equal.

In a receiving front-end architecture, the ADCs' resolution requests depend on several metrics such as the performances offered by the power control stage, but also on the PAPR (Peak to Average Power Ratio) of the signal to be digitized. While the power control stage is the same for the two architectures, we have to evaluate the PAPR evolution when adding an UMTS and a WLAN signal. A theoretical and simulation study was separately done and it reveals a worse case scenario where the final signal's PAPR increases of only 2 dB compared to that on the WLAN input signal. Therefore, while comparing the two structures and for the same power control performances (dedicated LNAs), we considered that the resolution of the ADC used by the proposed architecture is the same as that used in the WLAN dedicated front-end in the stacked-up front-end architecture.

The performance-power trade-off state of the art of ADC dedicated to the UMTS and WLAN are presented in [8] and respectively in [9]. Their power consumption is of 11 mW and 12 mW.

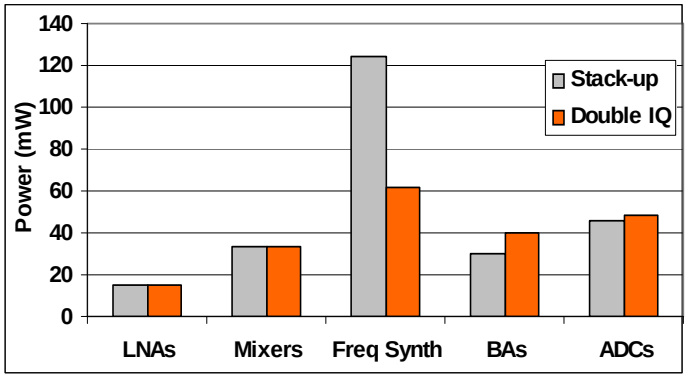

Fig. 4 Consumption of the different block types used by the two architectures.

TABLE I

BASIC ELEMENTS USED BY THE TWO ARCHITECTURES

	Stack-up	Double IQ	Power/Supply
	Quantity	Quantity	mW//V
LNA – UMTS	1	1	7.2//1.8
LNA – WLAN	1	1	8//1
RF-Filters	2	2	-
IF- Filters	2	0	-
Mixers	6	6	5.6//-
RF-Frequency Synthesizers	2	1	42//3
IF-Frequency Synthesizers	2	1	20//
BA – WLAN	2	4	10//-
BA - UMTS	2	0	5//-
ADC – WLAN	2	4	12//2.5
ADC - UMTS	2	0	11//1.8

F. Overall power and complexity evaluation

In order to make a comparative overall power consumption evaluation between the two architectures, a complexity study has to be made in order to evaluate the number of elements that have to be used for each structure. Table 1 summaries the elements used by each of the two architectures, as well as their individual power consumption along with their supply voltage.

As shown here, the proposed architecture needs less components than the state of the art front-end stack-up as it doesn't need image rejection filters and it uses less frequency synthesizers. Therefore, the complexity comparison is favorable to the proposed structure, especially because the image rejection filters are not on-chip integrated elements.

For our study case and for the power consumption levels presented in Table 1 the overall power consumption comparison shows that the proposed structure consumes 216 mW while the state of the art architecture uses 284 mW. This means a 20 % of gain in favor of the single front-end structure assessed in this paper. In order to better understand this power gain, Fig.4 shows the power consumed by every type of block used by the two architectures. This power gain comes essentially from the use of two times less frequency synthesisers, while using the same number of other components.

IV. CONCLUSIONS

In this article, a novel multistandard simultaneous reception architecture was presented. Expected performance of its implementation has been presented for a particular study case – simultaneous reception of two signals using the 802.11g and UMTS standards. The signal processed by the analog part of the receiver presents an excellent spectral efficiency as the two standards spectrums are overlapped after the first IQ stage. Compared to the state of the art represented by the stack-up dedicated front-ends structure, the proposed architecture offers a much better performance-complexity-power trade-off. In fact it is less complex as it uses less electronic blocks (external image rejection filters and frequency synthesizers) for the same performance. In addition to the reduced complexity, the overall power study shows a 20% power gain.

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