

Efficient Multicore Scheduling Of Dataflow Process Networks

Hervé Yviquel, Emmanuel Casseau **IRISA - University of Rennes 1** {firstname.lastname}@irisa.fr

Matthieu Wipliez, Mickaël Raulet **IETR - INSA of Rennes** {firstname.lastname}@insa-rennes.fr

Dataflow Process Networks

Multi-core scheduling strategies



Static mapping of the processes on the cores **Topologies of communications**

A4

A1 and A2 on the first core A3, A4 and A5 on the other one

Multi-core round-robin



- Mesh







Single-core scheduling strategies

Round-robin:

- Simple strategie
- Equal chance of being executed
- No notion of time slice
- Static list of next schedulable actors





Communications



Data-driven / demand-driven :

Results with two different video decoders (in frames per second)

MPEG-4 Simple Profile

MPEG-4 Advanced Video Coding

Strategy	Core	CIF	720p	Speedup	Strategy	Core	QCIF	CIF	Speedup
Round-robin	1	144	15.6	1		1	28.4	7.1	1
	2	265	26.6	1.78	Round-robin	2	55.6	13.9	1.96
	4	494	51.4	3.36		4	90.8	21.2	3.05
Combined	1	154	16.1	1		1	169	40.6	1 🔉
	2	288	27.3	1 75	Combined	2	204	71 /	1 7/

