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Effects of Interface Roughness Scattering on Radio Frequency Performance of Silicon Nanowire Transistors

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The effects of an atomistic interface roughness in n-type silicon nanowire transistors (SiNWT) on the radio frequency performance are analyzed. Interface roughness scattering (IRS) is statistically investigated through a three dimensional full–band quantum transport simulation based on the $sp^3d^5s^*$ tight–binding model. As the diameter of the SiNWT is scaled down below 3 nm, IRS causes a significant reduction of the cut-off frequency. The fluctuations of the conduction band edge due to the rough surface lead to a reflection of electrons through mode-mismatch. This effect reduces the velocity of electrons and hence the transconductance considerably causing a cut-off frequency reduction.

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Since the lengths of silicon (Si) metal-oxide-semiconductor field effect transistor (MOSFET) have been scaled down to the sub-100 nm regime, the cut-off frequency has increased significantly to reach hundreds of gigahertz (GHz)[1–3]. Even though the cut-off frequency is not the only important parameter in radio frequency (RF) MOSFETs, a high cut-off frequency certainly represents a good criterion for Si MOSFETs to catch up with III-V transistors if other shortcomings are overcome. Power losses due to a long skin depth of the Si substrate, a poor noise figure and a high gate resistance[4] are the examples of such obstacles. Recently there have been tremendous efforts to improve the RF performance of the Si MOSFET and it is becoming competitive to III-V high electron mobility transistor (HEMT)/heterojunction bipolar transistor (HBT) or silicon germanium (SiGe) HBT[2,3,5].

Silicon-on-insulator (SOI) multi-gate (MG) structures also have been found to be capable of achieving the cut-off frequency predicted by the international technology roadmap for semiconductors (ITRS)[6] for RF applications while reducing substrate losses and noise figures[7]. Gate-all-around (GAA) siicon nanowire transistors (SiNWTs) have attracted attention since it was found that their cut-off frequency can be much larger than that of planar Si MOSFET[8].

Traditionally, interface roughness scattering (IRS) has been considered as one of the most important scattering mechanisms. At a high effective electric field, IRS dominates

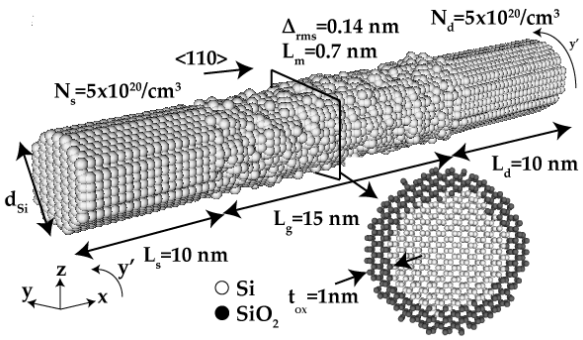

FIG. 1. The simulated silicon nanowire with rough surface in the channel: the root-mean-square roughness height Δ_{rms} and the correlation length L_m are adopted from Ref. 9. The crystal orientation $\langle 110 \rangle$ is selected for the electron transport direction. The source/drain doping density N_s/N_d is set to $5 \times 10^{20}\text{cm}^{-3}$. The diameter of the nanowire d_{Si} varies from 2, 2.5, 3 to 4 nm. The length of the source/drain extension region L_s/L_d, the gate length L_g, and the oxide thickness t_{ox} are shown in the figure. The channel of the nanowire is undoped.

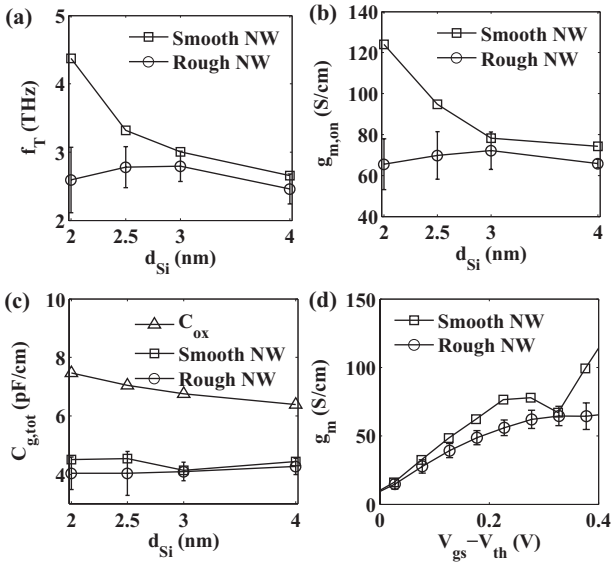

FIG. 2. (a) The cut-off frequency ($f_{\rm T}$), (b) the transconductance ($g_{\rm m,on}$), (c) the total gate capacitance $C_{\rm g,tot}$ vs diameter $d_{\rm Si}$ at the on-state with the gate bias $V_{gs} \sim V_{th} + 0.4V$ with the oxide capacitance $C_{\rm ox} = 2\pi\epsilon_{\rm ox}/\ln\left[2(t_{ox} + d_{\rm Si}/2)/d_{\rm Si}\right]$ where $\epsilon_{\rm ox}$ is the dielectric constant of the oxide, and (d) the transconductance vs gate overdrive for 100 rough nanowire samples (errorbar: standard deviation). All the values except f_T are normalized with the perimeter of the NW.

the universal mobility trend[10]. In SiNWTs, IRS is still an important scattering mechanism reducing the on-current and the mobility significantly from the ballistic values[11].

This paper focuses on the effects of interface roughness scattering on the RF performance of SiNWTs, especially on the cut-off frequency (f_T). For that purpose, a three dimensional full-band quantum transport simulator based on the $sp^3d^5s^*$ tight-binding (TB) model[12,13] is used. As the maximum oscillation frequency (f_{max}) – another important figure of merit of the RF MOSFETs is directly related to the cut-off frequency[8], the effects of IRS on the theoretical limit of the SiNWT's RF performance can be estimated through this study.

The structure of the SiNWT studied in this paper is depicted in Fig. 1 where the oxide layer is described in the cross-sectional view. The model of the interface roughness in the SiNWT used in the simulation is described in Ref. 11 where the influence of the interface roughness scattering on the direct-current (DC) characteristics of SiNWTs is presented. The silicon dioxide (SiO_2) layer is included in the transport calculation[11] to accurately model the wavefunction penetration into the oxide layer.

The cut-off frequency f_T is related to the transconductance $g_{m,on}$ and the total gate

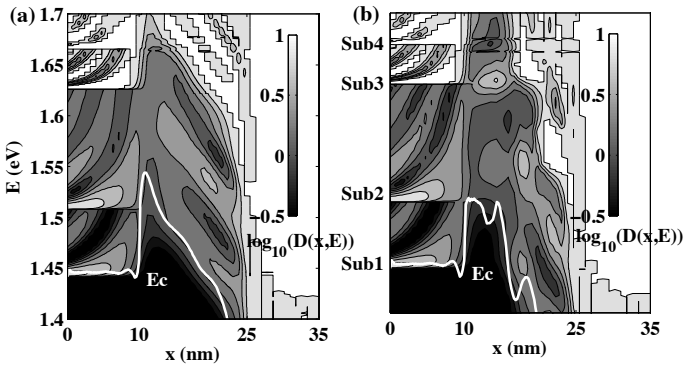

FIG. 3. The density of states $D(x, E)$ in a logarithmic scale for (a) a smooth NW or (b) a rough NW resolved in the transport axis x and the energy E near the on-state with $V_{gs} \sim V_{th} + 0.4V$. The channel of the NWFET starts from $x = 10$ nm and extends to $x = 25$ nm.

capacitance $C_{g,tot}$ through the relationship

$$f_T = \frac{g_{m,on}}{2\pi C_{g,tot}} \tag{1}$$

where $g_{m,on}$ and $C_{g,tot}$ are calculated through the following expressions at the on-state defined by the gate voltage V_{gs} at $V_{th} + 2/3V_{dd}$[14]:

$$g_{m,on} = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{gs}=V_{th}+2/3V_{dd},V_{ds}=V_{dd}} \tag{2}$$

$$C_{g,tot} = q\left.\frac{\partial N_{1D}}{\partial V_{gs}}\right|_{V_{gs}=V_{th}+2/3V_{dd},V_{ds}=V_{dd}} \tag{3}$$

where V_{th} is the threshold voltage, V_{dd} the supply voltage and N_{1D} the total electron density under the gate divided by the gate length. The threshold voltage V_{th} is determined using a critical current $I_c = d_{Si} \times 10^{-7}(A)$.

The simulated cut-off frequency of a smooth nanowire (NW) is shown in Fig. 2(a). The results obtained here are similar to the data calculated in Ref. 8. The cut-off frequency increases as the nanowire diameter decreases. This is to first order a consequence of the improvement of the injection velocity in a $\langle 110 \rangle$ silicon nanowire (SiNW) with smaller diameter[15].

As shown in Fig. 2(b), the transconductance $g_{m,on}$ is reduced significantly by the IRS while $C_{g,tot}$ is not affected much (Fig. 2(c)). The reduction of $g_{m,on}$ is due to reflections caused by the rough interface. A small dip in g_m marked by an arrow in Fig. 2(d) is an indication that the second subband starts to carry the current[16]. In rough NWs, this dip is smoothed out due to subband mixing.

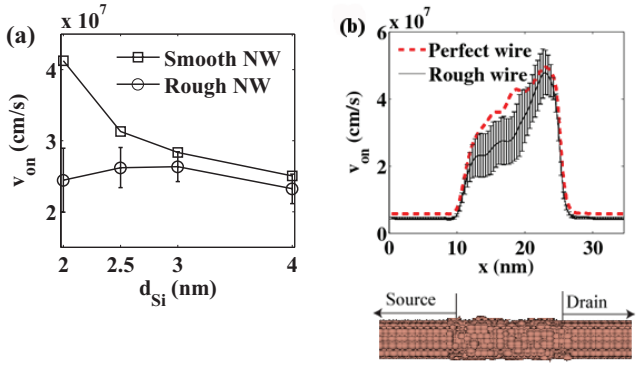

FIG. 4. (a) The average electron velocity at the on-state for NWs with a different diameter and (b) the electron velocity along the channel at the on-state for rough NWs with diameter 2 nm (errorbar: standard deviation).

Mismatches of the subbands throughout the channel of the rough nanowire also can be observed in Fig. 3(b). This causes reflections of electrons causing reduction of the electron velocity which, in turn, reduces the transconductance. Fig. 4(b) shows the electron velocity throughout the smooth NW and the rough NWs with the diameter 2nm. The electron velocity is significantly reduced by interface roughness scattering.

One thing noticeable in Fig. 4(b) is that the IRS causes a reduction of the electron velocity at the beginning of the channel, but not much at the end of the channel. Electrons gain a relatively large kinetic energy due to a large electric field at the end of the channel. As a result, the fluctuation of the conduction band edge at the end of the channel does not affect the electron velocity significantly.

The cut-off frequency relationship (Eq. 1) can also be expressed as

$$f_T = \frac{v_{on}}{2\pi L_g}. \tag{4}$$

Therefore, the average electron velocity v_{on} can be calculated from the cut-off frequency. The transit time under the gate τ_T is determined from v_{on}/L_g, such that the average velocity is an effective velocity with which electrons flow in the channel when a small signal is applied to the gate. As shown in Fig. 4(a), it turns out that v_{on} is higher than the ballistic injection velocity ($\sim 1.5 \times 10^7$cm/s from Ref. 17) because electron velocity is not saturated in the beginning of the channel as in a long channel transistors. It can be observed that the average electron velocity v_{on} is close to the velocity in the middle of the channel.

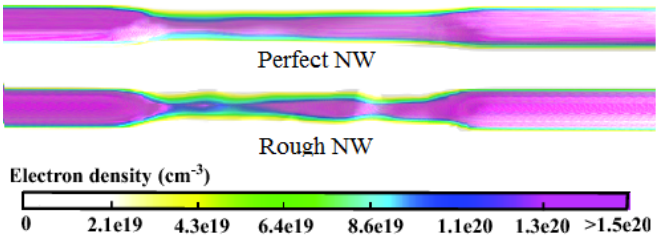

FIG. 5. The electron density from source to drain for (top) the smooth NW and (bottom) the rough NW (the same sample selected for Fig. 3) at the on-state with $V_{gs} \sim V_{th} + 0.4V$.

The total gate capacitance is also an important parameter in the SiNWT. Experimentally it is found that the total gate capacitance is reduced from the oxide capacitance due to volume inversion of carriers in a nanowire[18]. In the simulated NW, the total gate capacitance is found to be much smaller than the oxide capacitance as shown in Fig. 2(c).

Fig. 5 shows the electron density along the NW where it can be observed that the electron density is fluctuating throughout the channel as compared to the smooth NW. Interface roughness causes mode mixing and additional reflections in the current. It does, however, not modify the total density of states (DOS), and therefore the capacitance of the nanowire. Therefore, the total gate capacitance is relatively unaffected by rough interfaces.

In conclusion, the cut-off frequency of SiNWTs is statistically studied through quantum transport simulation using a realistic modeling of the rough Si/SiO_2 interface. It is found that the rough surface causes back-scattering and reduces the velocity of electrons via modifying the DOS in the channel. Mode-mismatch due to interface roughness scattering reduces the overall transconductance, but does not significantly affect the total gate capacitance. In addition to the cut-off frequency degradation, its variability is another issue that should be addressed in RF SiNWTs.

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