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The CDF Run IIb Silicon Detector: Design, preproduction, and performance

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Abstract

A new silicon microstrip detector was designed by the CDF collaboration for the proposed high-luminosity operation of the Tevatron $p\bar{p}$ collider (Run IIb). The detector is radiation-tolerant and will still be functional after exposure to particle fluences of 10^{14} 1-MeV equivalent neutrons/cm^2 and radiation doses of 20 MRad. The detector will maintain or exceed the performance of the current CDF silicon detector throughout Run IIb. It is based on an innovative silicon "supermodule" design. Critical detector components like the custom radiation-hard SVX4 readout chip, the beryllia hybrids and mini-port (repeater) cards, and the silicon sensors fulfill their specifications and were produced with high yields. The design goals and solutions of the CDF Run IIb silicon detector are described, and the performance of preproduction modules is presented in detail. Results relevant for the development of future silicon systems are emphasized.
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1. Introduction

Experiments at hadron colliders at the highest energies have played a crucial role in establishing our current understanding of particle physics [1]. Hadron colliders allow us to study a broad range of research topics and offer unique opportunities for significant discoveries. The Tevatron $p\bar{p}$ collider at the Fermi National Accelerator Laboratory (FNAL) is currently the highest-energy particle accelerator in operation. The physics program of the Tevatron's Run II includes precision electroweak measurements, e.g. the determination of the top quark and W boson masses; bottom and charm physics, e.g. the determination of the B_s mixing parameters; studies of the strong interaction; and searches for a Higgs particle, supersymmetric particles, hidden space-time dimensions, quark substructure, etc. [2].

All of these measurements benefit from a high-resolution tracking detector. Most of them, in particular the Higgs boson search, top physics, and bottom physics, rely heavily on the efficient detection of b-hadrons. This is best provided by the detection of displaced secondary vertices using a silicon tracking detector. The current CDF silicon detector is well-suited for this task. However, radiation damage will cause its performance to degrade substantially after recording integrated luminosities of 4–6 fb^{-1} [3,4]. Since a total of 15 fb^{-1} was expected to be delivered during Run II (most of it in Run IIb), the CDF Run IIb silicon detector was designed [5–7] to replace the presently installed one. A full design of the detector was finished and approved by the Department of Energy in 2002. However, due to budget constraints and significantly reduced luminosity expectations for the Tevatron, the project was canceled in Fall 2003 when it was already in the early preproduction stage.

In this paper the basic design considerations, concepts and the solutions chosen for the Run IIb silicon detector are presented. The detector components and the performance obtained with preproduction silicon modules is described. Results that are of particular relevance for the design of future silicon systems are emphasized.

2. Requirements

The current CDF silicon detector, the Run IIa detector, is described in the literature [2,8–11]. It consists of three sections at different radii and with different coverage in pseudorapidity η: a single-sided beampipe layer (L00); the main silicon vertex detector (SVXII), consisting of five double-sided layers; and the outer intermediate silicon layers (ISL). Together they provide up to 15 precision space points per track within a pseudorapidity range of $|\eta|<2$. The system can be operated at bunch crossing times of 396 and 132 ns. The readout of the entire system takes $\approx 10\,\mu$s due to data sparsification, which allows impact parameter information to be used in the Secondary Vertex Trigger (SVT) [2,12,13]. Benchmark performance achieved with the current calibration and reconstruction tools and from Run II data includes: an asymptotic impact parameter resolution of $\approx 10\,\mu$m [14], a b-jet tagging efficiency in $t\bar{t}$ events of $\approx 50\%$ [15] for high P_T-jets in $|\eta|<1$, a systematic uncertainty in fully reconstructed B hadron lifetimes of ≈ 0.01 ps [16], and a mass resolution of B^+ and B^0 mesons of ≈ 0.3 MeV [17].

The new CDF silicon detector was designed to retain or improve this performance, and improve radiation tolerance greatly, withstanding particle fluences of 10^{14} 1-MeV equivalent neutrons/cm^2 and radiation doses of 20 MRad[1] at the innermost layer. Other important constraints were given by the available physical space (of less than 20 cm outer radius), the need to retain the Run IIa detector data acquisition system, cooling services, and data flow into the SVT trigger system. As for the present detector, precise placement of the sensors relative to their nominal positions is required by the SVT.

[1]These numbers correspond to an integrated luminosity of 15 fb^{-1}, the projected Run IIb luminosity at the start of the project.

3. Design considerations

The radiation sensitivity of the Run IIa detector and its various failure modes were studied in detail [3]. The ISL detector, whose silicon layers are located between radii of 22.6 to 29 cm, is estimated to remain sensitive beyond $40\,\mathrm{fb}^{-1}$ of integrated luminosity. Consequently, the ISL detector was not part of the Run IIb upgrade.

The SVXII and L00 inner layers are much closer to the beam line. Depending on their particular radii and sensor technology, most of them will degrade substantially before collecting $15\,\mathrm{fb}^{-1}$ of data. While a partial replacement of the SVXII and L00 was considered initially [3], a full replacement turned out to be the only practical and preferred solution.

A crucial component of every silicon microstrip detector is the readout chip. The SVX3 chip [18,19] was developed and fabricated in a 0.8 μm bulk CMOS radiation-hard process for the CDF Run IIa detector. The noise performance of this chip is marginal for Run IIb requirements. This would lead to serious design constraints and would limit the performance of the Run IIb silicon system. Since the design of the SVX3 chip, 0.25 μm CMOS processes have become commercially available. These processes are radiation-hard, provided that special design rules are applied [20–22]. Thus an alternative to ordering additional SVX3 wafers was to redesign the chip in a commercial 0.25 μm CMOS process. While the design of a new chip (even with similar functionality) introduced a substantial financial and schedule risk, it offered chances for a much improved yield and noise performance. Given these advantages, a new design, which yielded the SVX4 chip [24–26], was carried through.

Experience from the development of silicon detectors for LHC experiments has shown that radiation-hard double-sided silicon sensors are difficult and expensive to make [28]. For the Run IIb detector single-sided microstrip sensors, based on LHC technology, were chosen. (The same sensor type is used in the L00 of the CDF Run IIa detector.) The sensors are described in more detail in Section 6. The use of single-sided rather than double-sided sensors doubles the sensor material (if the same number of space points are retained). The sensors need active cooling to reduce their radiation-induced leakage currents and to avoid reverse annealing; the cooling tubes and services lead to further material increase. In order to minimize multiple-scattering, conversions, and the corresponding loss of resolution, great care was therefore taken to reduce material elsewhere.

Material reduction was achieved by moving the port card electronics outside the tracking volume, by an innovative "supermodule" or stave design, as well as by a photo-imageable hybrid technology that reduces the hybrid size and trace pitch.

In order to cope with a tight schedule, the mechanical detector design was optimized for ease of construction and assembly wherever possible. The number of critical detector components was drastically reduced compared with the Run IIa detector. Only two different hybrid designs and three sensor types are needed for the Run IIb detector. (In contrast, the L00/SVXII system for Run IIa uses 11 different hybrid designs and corresponding accessories. Two more designs were needed for the ISL.) Existing and reliable technology was selected to the largest extent possible in order to minimize R&D. This, among other reasons, also excluded the use of optical fibers for data transmission and the consideration of an innermost pixel layer.

4. Mechanical layout

4.1. Overall configuration

The CDF Run IIb silicon detector consists of two identical barrels each placed concentrically around the beam line. A photograph of a barrel section is shown in Fig. 1. The barrels consist of two carbon fiber bulkheads and the supermodules they support; the supermodules are described in detail in Section 5. The bulkheads are flat carbon fiber disks with precision mounting fixtures glued in place. The inner bulkhead (located at the center of the interaction region) is 1 mm thick, and the outer one is 2 mm. Carbon fiber has a low thermal expansion coefficient, a long radiation length, and high stiffness. Carbon fiber disks are preferred over beryllium because they are much cheaper and easier to process. During barrel assembly, the supermodules are installed through the holes in the outer bulkhead and then pinned into the mounting holes and slots of the inner bulkhead (not shown), before being fixed to the outer bulkhead.

The bulkheads themselves are supported by a longer, horizontally split cylindrical tube (spacetube) that extends to mounting points at the ISL detector. The beam pipe has an diameter of 2.9 cm, and its central part consists of five bored beryllium tubes that are welded together. The beam pipe walls are 0.5 mm thick.

The supermodules are cooled with 42.5% weight ethylene glycol in water at −15 °C using the existing

Fig. 1. Photograph of supermodules installed in the barrel. The outer bulkhead is on the left.

CDF cooling system, which is designed to operate below atmospheric pressure. This prevents leakage of the coolant into the detector volume. The silicon detector volume is flushed with cooled, dry nitrogen in order to prevent condensation.

4.2. Layer arrangement

The arrangement of the L0 and supermodule layers in the Run IIb silicon detector is shown in Fig. 2, and the radial positions of the layers are listed in Table 1. The innermost layer, L0, of the Run IIb silicon detector consists of 12 castellated "ladders" of single-sided silicon sensors. The arrangement is very similar to L00 of the Run IIa detector. The other layers, L1 to L5, are composed of supermodules. These carry single-sided silicon sensors on their top and bottom sides and correspond to the double-sided silicon ladders of Run IIa. Supermodules may differ in sensor type (axial or stereo strips) on top or on the back but otherwise are identical. Instead of a highly symmetrical wedge structure, the Run IIb detector has an approximate six-fold symmetry, and the relatively wide supermodules are used even at small radii. The Run IIb detector also makes better use of available space by extending farther out radially than the Run IIa detector (to 16.15 cm rather than 10.64 cm), which improves matching with ISL hits.

A 0.25 mm thick carbon fiber/aluminum screen (inner screen) separates the L0 and L1 layers thermally and electrically, and provides additional rigidity to the bulkheads.

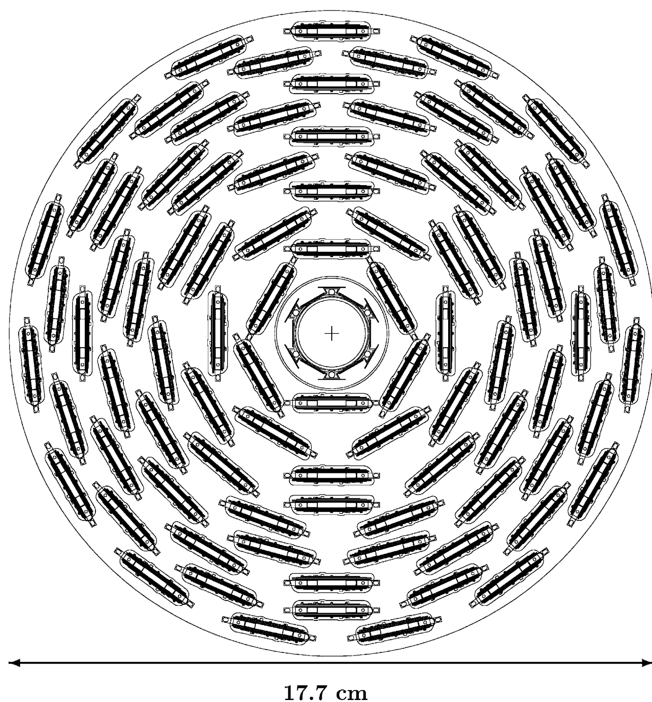

Fig. 2. End view (r–ϕ view) of the Run IIb silicon detector. The inner part shows the castellated L0 layer, and the outer layers are supermodule layers. These two sections are separated by the cylindrical inner screen of the supermodule section.

The predominant use of a single supermodule element allowed 94% of the channels to be built with only one hybrid and two sensor types. For the Run IIa SVXII detector, ten hybrid types, five sensor types, and five different ladder types were used. By minimizing the number of components, component design, procurement, and detector assembly and testing are substantially simplified and accelerated.

The single supermodule approach is pushed to its limit in L1. Here the supermodule width is comparable to the layer radius, and packaging effects lead to an increased incidence angle and a 7.8° gap between adjacent L1 supermodules (see Fig. 3). The gaps are well covered by L0 and L2, and the performance of this layer arrangement is only mildly affected, as is discussed below.

4.3. Expected performance

The expected performance of the Run IIb silicon detector was evaluated in detail for various design options [29]. These include the variation of the radial position of L0, the number and position of the stereo layers, and the choice of stereo sensor angles. One tool is an analytical program that calculates impact parameter and pointing resolution, taking into account the position, hit resolution and material of each silicon layer, as well as the position and material of the beampipe and the inner screen.[2] The program gives an excellent description of Run Ib impact parameter resolutions.

Given the sensors, the hit resolution of the axial layers is conservatively taken to be 7.2 and 10.8 μm for L0 and L1–L5, respectively, as calculated by the sensor pitch $p/\sqrt{12}$. The resolution along the beam direction (z direction), which is given by combining information from the stereo and the nearby axial sensors, is assumed to be 780 μm. The ISL r–ϕ and z resolutions are taken to be 32.3 μm and 2.2 mm, respectively. The predicted impact parameter resolutions are summarized in Table 2. The numbers given do not include the errors introduced by the uncertainties in the collision vertex and misalignment effects, both of the order of 10 μm. These effects will dominate the resolution at high momenta.

The calculated impact parameter resolutions are good. If a track misses L1 and passes through the gap, its resolution deteriorates only slightly. In case of a hypothetical loss of L0, the resolution for high P_T tracks is still good, while the multiple scattering term increases significantly. The latter effect, though undesirable, is unavoidable since multiple scattering is dominated by the material of L0 itself, which has already been minimized. A reduction of the outer layer material budget would only marginally reduce the multiple

[2] For this particular study, the supermodule is conservatively assumed to be 2.0% of a radiation length; the beampipe and the inner screen are assumed to be 0.1% and 0.5%, respectively. For simplicity, no distinction between inner and outer supermodule positions is made, instead the average radial position is taken.

Table 1
Radial location of L0, the supermodule layers, and other objects. The number of chips, sensors, and hybrids per layer are also given. In total, 2304 sensors, 1152 hybrids, and 4464 SVX4 chips are needed to build the detector. The strip pitch is 25 μm for L0. It is 37.5 μm for the axial and 40 μm for the stereo sensors of L1–L5

Object	Inner	Radius (cm)	Outer	Ladders/ Supermodules	Sensors	Hybrids	SVX4 Chips
Beampipe			1.25	–	–	–	–
L0 inner	2.10 (0°)		n/a	6	36	18	36
L0 outer	2.50 (0°)		n/a	6	36	18	36
L1 inner	3.55 (0°)		4.00 (0°)	3	36	18	72
L1 outer	4.35 (0°)		4.80 (0°)	3	36	18	72
L2 inner	5.95 (0°)		6.40 (1.2°)	6	72	36	144
L2 outer	7.48 (0°)		7.93 (1.2°)	6	72	36	144
L3 inner	9.08 (1.2°)		9.53 (0°)	9	108	54	216
L3 outer	10.45 (1.2°)		10.90 (0°)	9	108	54	216
L4 inner	11.93 (1.2°)		12.38 (0°)	12	144	72	288
L4 outer	13.30 (1.2°)		13.75 (0°)	12	144	72	288
L5 inner	14.75 (0°)		15.20 (0°)	15	180	90	360
L5 outer	16.15 (0°)		16.60 (0°)	15	180	90	360
Inner screen		2.98					
Bulkhead	3.1		17.50				
Spacetube	17.70		18.50				
ISL	19.00		32.00				

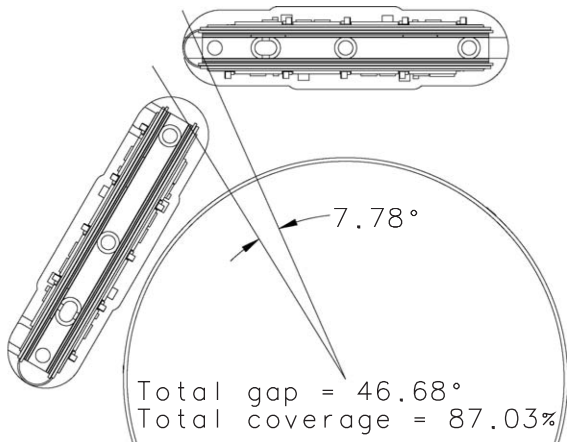

Fig. 3. End view detail showing the 7.8° gap between adjacent L1 supermodules.

Table 2
Impact parameter resolutions σ_d in the r–ϕ plane for all axial layers (L0, SVXIIb and ISL) and for configurations in which the tracks miss L1 and/or L0. The numbers are given for 90° and 30° track incidence on L1

90° incidence	Asymptotic σ_d (μm)	σ_d (μm) at $P_T = 2\,\text{GeV}$
All layers	6	25
L1 missed	7.5	27
L0 missed	9	51
L0 and L1 missed	15	79
30° incidence	**Asymptotic σ_d (μm)**	**σ_d (μm) at $P_T = 2\,\text{GeV}$**
All layers	7.2	26
L0 missed	13	58

scattering term (not shown). Another price of placing the wide supermodule structure at a small radius is an increased number of tracks at large incident angles and a corresponding loss of resolution. This effect is small if all layers are functional (see Table 2). Thus a dedicated L1 design, with reduced sensor width in either L0 or supermodule style, was not chosen.

The single-sided sensors on the top and bottom of a supermodule are separated by 4.5 mm. In a supermodule with axial sensors on both sides (double-axial), line segments (stubs) can be reconstructed with a pointing resolution of ≈ 3.5 mrad, comparable with the pointing resolution of the Central Outer Tracking chamber (COT) [30] of the CDFII detector. Tracking algorithms can exploit this information by requiring the reconstructed stub slope to be consistent with the projected track slope.

Double-axial supermodules are placed in L1 and L5. In L1, this strengthens pattern recognition in the crowded environment near the beampipe. In L5 the connection between COT tracks and the silicon system is strengthened, which protects against possible performance degradation of the COT due to overlapping hits. Double-axial layers add redundancy and the mentioned pointing resolution. The later effects were quantified with Monte-Carlo simulations of $t\bar{t}$ events, which contain dense high energy jets. COT tracks were extrapolated to L5 and L1, and the slopes of the double axial stubs for L1, L5 and the COT track slope were compared. In L5, 72% of the track stubs can be rejected by requiring a 3σ agreement with the COT track slope. This eliminates $\frac{3}{4}$ of the pattern searches into the inner layers and reduces the rate of pattern recognition failures. Similarly 40% of the track stubs can be eliminated at L1.

L0 is an important layer in the Run IIb detector. While the impact parameter resolution for a single track improves when L0 is closer to the collision point and multiple scattering effects are smaller, the number of nearby tracks increases as well. The latter leads to shared hits and decreased resolution. In order to determine the optimum L0 radial position, $t\bar{t}$ and $b\bar{b}$ events were simulated and processed through a stand-alone version of a standard CDF secondary vertex finding algorithm (SECVTX). The secondary vertex tagging efficiencies were determined for typical selection criteria, and the different resolutions of shared and unshared hits were considered. The procedure was repeated for radial locations of L0 between 1.5 and 3 cm.

The simulation results for $b\bar{b}$ events are shown in Fig. 4. The L0 is best placed at 1.5 cm, but the efficiency to tag at least one b-hadron is only marginally reduced at 2 cm (reduction by $\approx 1\%$ for $t\bar{t}$ events and $\approx 4\%$ for $b\bar{b}$ events). The reduction is stronger for $b\bar{b}$ events due to the lower momenta of the b-hadrons and increased multiple-scattering. Positioning L0 at 3 cm leads to a prohibitive reduction of the single-tag efficiencies by $\approx 5\%$ for $t\bar{t}$ events and $\approx 20\%$ for $b\bar{b}$ events. We decided to place the inner L0 layers at 2.1 cm. This presents fewer mechanical difficulties, offers good performance, and decreases the radiation dose by an additional factor of ≈ 1.8. (The radiation dose approximately falls off with radius proportional to $1/r^{1.7}$. The deviation from a $1/r^2$ dependence is due to the creation of secondary particles in the detector and beam pipe material.)

Different studies were performed to optimize the number and position of the stereo layers and the sensor strip angle. While 90° stereo layers offer the best track resolution along the beam direction, they make the association of hits to tracks in a multiple track environment more difficult due to random combinations of axial and stereo hits (“ghosts”). Emphasizing robustness, optimum pattern recognition, and resolution in the r–ϕ plane, we opted for 1.2° stereo layers. The track resolution and reconstruction efficiency depend on the number of stereo layers. The favored design with three supermodule stereo layers (and the ISL) gives an impact parameter resolution of $\sigma_z \approx 1.3$ mm, which is sufficient to separate primary vertices from multiple interactions. The track finding efficiency is approximately 90%. A fourth stereo layer would barely improve resolution and efficiency, while a system with only two stereo layers is not very efficient and provides no redundancy.

Lastly, the pattern recognition efficiency of the Run IIb design was investigated, again using simulated $t\bar{t}$ events. Pattern recognition errors can arise due to cluster merging and due to lack of pointing resolution to discriminate among nearby hits. A typical “outside-in” tracking algorithm will successively form a track by associating hits layer by layer, starting from a COT/ISL hit, and refit the track parameters at each stage. To understand the differences between the Run IIa and Run IIb detector designs, it was investigated in which layer wrong hits are first included in the track fit, and how frequently this happens. The results are displayed in Fig. 5.

The Run IIb detector has a significantly smaller wrong hit association probability at L5, the algorithm entry point, since L5 is placed at a larger radius compared with the Run IIa detector. This increased efficiency carries through to the inner layers, where the occupancy increases and errors due to merged hits are more frequent. Only for the outer Layer 1 and for Layer 2, are the failure rates of the Run IIb design worse than the Run IIa design at the same radius. This is in part due to the larger average incident angle in the Layer 1 Run IIb design and due to the larger pitch of the Run IIb sensors. For Layer 2, this is mostly due to the larger distance to the next outer layer in the Run IIb design. The overall performance is obtained by summing

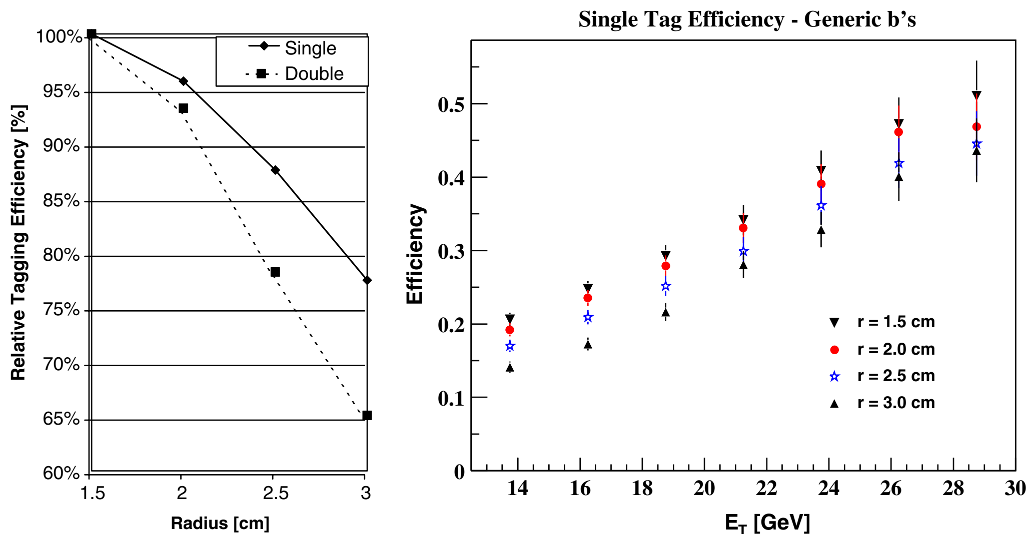

Fig. 4. Left: single and double tagging efficiencies in simulated $b\bar{b}$ events as a function of the Layer 0 radial position. The tagging efficiency at 1.5 cm radius is normalized to be 100%. Right: single tagging efficiency in $b\bar{b}$ events as a function of b—jet transverse energy E_T.

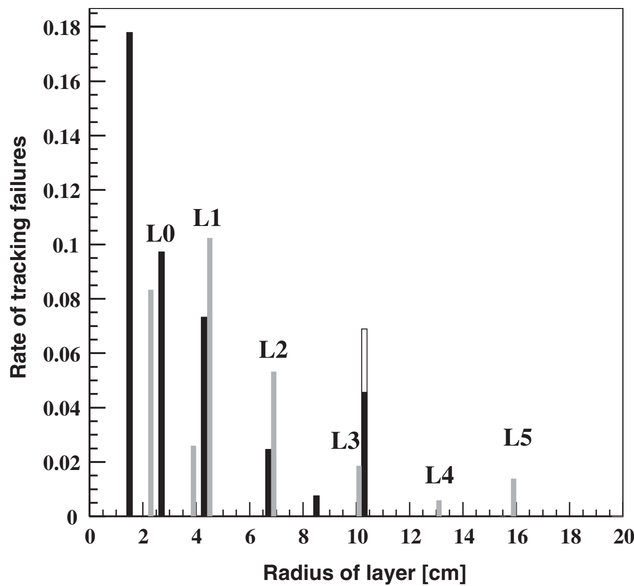

Fig. 5. The rate and point of origin (axial layer) of tracking failures in the r–ϕ plane. Effects of both merging (solid) and pointing inadequacy (open) for Run IIa (black) and Run IIb (gray) designs are shown. The labels L1 to L5 refer to the Run IIb average layer positions. Only the axial layers are shown. Note that the tracking failure rate in the inner axial sensors of L5 is zero for the Run IIb design and is not visible in the plot (unlike the inner axial sensor of L1).

the failure rate at each layer. In this particular study the rate for potential tracking failures is 31% in the Run IIb design and 45% in the Run IIa design. With a real tracking algorithm some of the "failures" would be recoverable, while others would lead to decreased detector performance and a non-Gaussian component to the impact parameter resolution.

These studies indicate that despite the strong emphasis placed on production and assembly issues, the Run IIb silicon detector was a powerful and robust tracking device, optimized to function well in a complex multi-track environment and to compensate possible loss of efficiency of the innermost COT layers.

5. Supermodules

5.1. Layout

The supermodule is the main building block and readout unit of the Run IIb silicon detector. It forms a 66 cm long, highly integrated mechanical, thermal and electrical structure. The top view and end view of a supermodule are shown in Figs. 6 and 7.

The core of the supermodule is composed of carbon fiber composite skins on a Rohacell [31] foam core with built-in cooling tubes. The cooling tubes are formed from 0.1 mm thick Polyetheretherketone (PEEK). The tubes follow a U-shaped path along the supermodule core with the inlet and outlet beyond the active detector region.

A flexible circuit bus cable, which provides all electrical connections, is glued to the top and bottom carbon fiber skins. Three silicon modules, each carrying a beryllia hybrid, are glued on the top bus cable, and three are glued to the bottom one. The mini-port card (MPC), a power distribution and repeater circuit, is located at the top side of the supermodule.

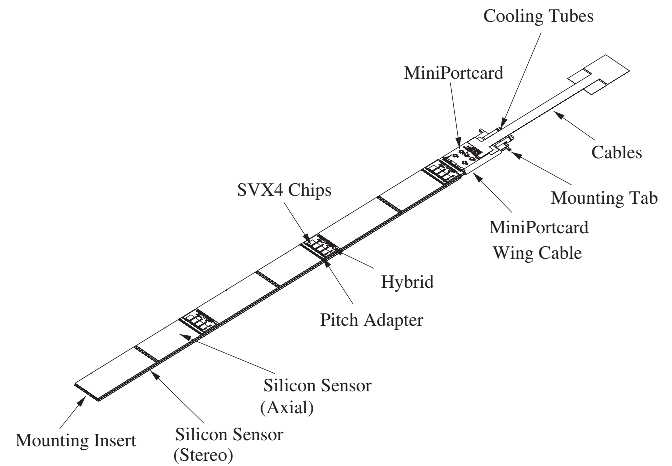

Fig. 6. Schematic drawing of a supermodule.

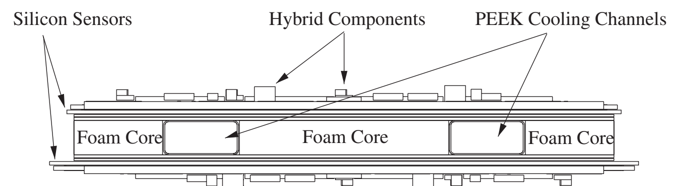

Fig. 7. Supermodule cross section. Note that the stereo sensors (bottom) and pitch-adapters are slightly wider than the axial ones (top).

Electrical connections from the hybrids to the bus cables are made with wire bonds through 3 mm wide gaps between silicon modules. This is illustrated in Fig. 8. The MPC and the top bus cable are connected with wire bonds as well. The connection between the mini-port card and the bottom of the supermodule is made with a short flexible circuit called the "wing cable". This cable is attached to the MPC and wraps around one edge of the supermodule to the bottom bus cable. Apart from the MPC, wing cable, and possibly the sensor type (axial or stereo), the top and bottom sides of the supermodule are identical.

The dense packing of the supermodule has a series of advantages. First, it allows many supermodule layers to be packed in the available space. One set of cooling tubes serves both the top and the bottom silicon sensors and the MPC. The installation and alignment of the supermodules in the bulkhead is straightforward compared with a system consisting of many independent modules, as is the construction of the supermodules themselves. The supermodules are so long that two barrels with supermodules easily cover the interaction region of the CDF detector. Electrical services and cooling only connect to the MPC end of the supermodules. This end points away from the

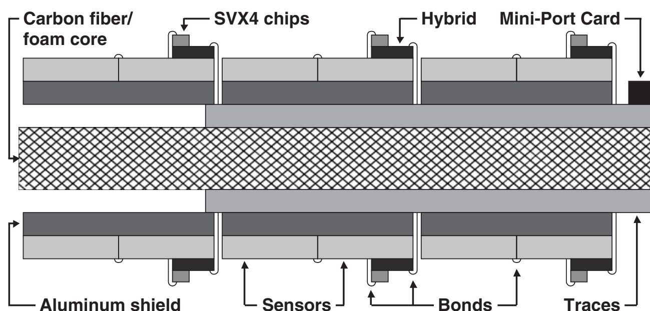

Fig. 8. Schematic and simplified side view of a supermodule. The horizontal and vertical scales are different. The pitch adapter is not shown.

interaction point, is relatively accessible, and is located outside the active detector region.

The dense packaging makes deadtime-less operation of the supermodule more challenging since electrical coupling of bus cable activity into the silicon sensors must be efficiently suppressed. This challenge was successfully met by careful design of the bus cable and its aluminum shield layer. The bus cable design and the supermodule electrical performance are described in Sections 7.3 and 10.

5.2. Thermal and mechanical properties

The silicon sensors were designed to operate in a harsh radiation environment. They must be cooled in order to limit their leakage current and associated noise increase and reverse annealing. The maximum operating temperatures are estimated to be $-5\,^{\circ}\mathrm{C}$ for L1, $+10\,^{\circ}\mathrm{C}$ for L2 and L3, and $+15\,^{\circ}\mathrm{C}$ for L4 and L5.

The dominant heat sources in the system are the SVX4 chips, which contribute $\approx 10\,\mathrm{W}$ per supermodule and half of the heat load of the Run IIb silicon detector. Other sources are convection from the outer detector walls to the cold supermodules, the MPC transceiver chips, and the sensor leakage current. The heat generated in the SVX4 chips is transported through the beryllia hybrid, the silicon sensor, the bus cable, the carbon fiber skins, and various adhesive layers to the cooling tubes. A finite element thermal model of the supermodule was developed to simulate its thermal performance. The sensors are warmest near a hybrid, and the warmest location on a supermodule is close to the hybrid next to the mini-port card, which is another heat source. For $-15\,^{\circ}\mathrm{C}$ coolant temperature (see Section 4.1), this point is $\approx 0\,^{\circ}\mathrm{C}$. The leakage current is determined by the average temperature over a strip, which is $\approx -10\,^{\circ}\mathrm{C}$ for axial strips, and $\approx -4\,^{\circ}\mathrm{C}$ for the short stereo strips under a hybrid. These temperatures are well below the above specifications.

Supermodule bowing due to gravitational forces and thermal effects were simulated and measured in order to verify compatibility with the SVT silicon track trigger mechanical requirements. For supermodules with sensor faces oriented horizontally in the barrel, sagging effects of the order of $150\,\mu\mathrm{m}$ can be observed. This is a natural consequence of the supermodule length and weight. The maximum radial variation ΔR along a strip within a given module is largest for the modules at the end of the supermodule. Typical values are $\Delta R \approx 120\,\mu\mathrm{m}$. If the supermodule sensor faces are oriented vertically in the barrel, radial variations of $\Delta R \approx 60\,\mu\mathrm{m}$ are more typical. No particular efforts were made to optimize module flatness on the supermodule core.

5.3. Material breakdown

Minimizing detector material is crucial for a vertex detector because multiple scattering limits the achievable impact parameter resolution. Particle interactions with detector material also create secondary charged particles, which increase occupancy and complicate track finding.

A breakdown of the supermodule material is given in Table 3. Overall the supermodule corresponds to $\approx 1.7\%$ of a radiation length. The single-sided sensors contribute 39% to the total supermodule radiation length, the supermodule core (including carbon fiber, adhesive and coolant) contributes 36%, the bus cables 12%, and the hybrids 12%. A supermodule including coolant was weighed at 152 g; its calculated weight is 150.6 g.

The material traversed by a track depends on its impact position. In Fig. 9, the average material seen by hypothetical tracks at normal incidence to the supermodules is shown as a function of position along the beam line. The material thickness in radiation lengths of the Run IIb detector is comparable to that of the Run IIa detector, despite the use of single-sided sensors. This was achieved for one by placing the Run IIb mini-port card at the end of the supermodule, whereas the Run IIa port cards and cables are inside the tracking volume. Moreover the Run IIb hybrids are smaller and more compact due to the use of advanced printing technologies (see Section 7.2) and the compactness of the supermodule design.

The supermodule radiation length compares favorably with other high luminosity hadron collider detectors. This is in part due to the supermodule being a self-supporting structure that is anchored by bulkheads, rather than being supported by a closed carbon-fiber cylinder. Further reduction of the supermodule material, for example in the context of a different detector, is conceivable. Starting points could be variation of the bus cable and hybrid layout, and the cooling system.

5.4. Supermodule construction

Supermodule production and assembly proceeds in the following steps.

First, silicon modules are constructed by butt-gluing two silicon sensors together at their front edges. The gluing and alignment fixture is shown in Fig. 10. The alignment process is straightforward. The adhesive is brought into the 0.1 mm gap between the adjacent fronts of the two sensors by exploiting capillary forces. The fixture has a removable

Table 3
Breakdown of the supermodule material. The material is averaged over the supermodule area covered by sensors, which is 244.55 cm^2

Part name	Material	X_0 (mm)	Qty	$\%X_0$	% total
Sensors	Silicon	93.6	12	0.676	39.11
Supermodule structural elements					
Carbon fiber facing	CF	230	2	0.234	13.55
Foam	Rohacell	13800	1	0.023	1.36
PEEK tubing	PEEK	319	2	0.017	1.00
Coolant	Water/Glycol	372	2	0.192	11.13
Epoxy (total)	Epoxy	320	22	0.153	8.87
Structural elements subtotal				0.621	35.91
Hybrids					
Hybrid substrate	BeO	144	6	0.049	2.85
Dielectric planes	Glass	100	42	0.050	2.87
Gold planes	Au	3.35	30	0.069	3.99
SVX4 chips	Silicon	93.6	24	0.018	1.06
Conducting epoxy	Silver	8.54	24	0.002	0.10
Components	various	35	174	0.021	1.20
Resistor chip	Silicon	93.6	6	0.0002	0.01
Hybrid subtotal				0.209	12.09
Bus cable					
Bus kapton	Kapton	287	6	0.038	2.18
Bus Cu traces	Copper	14.3	2	0.060	3.48
Bus Al plane	Aluminum	89	2	0.071	4.09
Interlayer glue	Glue	320	2	0.033	1.93
Bus cable subtotal				0.202	11.68
Pitch adapter substrate	Al_2O_3	75.5	8	0.021	1.21
Pitch adapter traces	Aluminum	89	8	0.0001	0.01
Mini-port card					
MPC substrate	BeO	144	1	0.022	–
Dielectric planes	Glass	100	8	0.025	–
Gold planes	Au	3.35	5	0.039	–
XCVR chips	Silicon	93.6	10	0.001	–
Conducting epoxy	Silver	8.54	10	0.000	–
Components	various	var.	45	0.002	–
Mini-port card subtotal				0.089	–
Mini-port card wing cable					
Wing copper traces	Copper	14.3	1	0.035	–
Wing Kapton	Kapton	287	1	0.007	–
Wing G10	G10	194	1	0.012	–
Wing cable subtotal				0.053	–
Supermodule total (not including MPC)				1.729	100

center plate such that the wet assembly can be removed after alignment and gluing. This makes it possible to assemble several modules per hour on the same fixture. The module axis is defined as the line connecting the outer fiducials on each side of a module. The module "misalignment" is defined as the maximum deviation of a point on a strip from the module axis. The average misalignment of the preproduction modules is $\approx 1\,\mu m$.

A different fixture is used to glue the hybrid and pitch adapter on the modules, and it requires the alignment of the hybrid pitch adapter with the sensor bond pads. Much less mechanical precision is needed compared with the sensor alignment for module gluing discussed above. A set of three modules is typically glued in less than 2 h. After curing, the modules are bonded. There are four sets of bond connections: silicon-to-silicon, silicon-to-pitch adapter, pitch adapter-to-hybrid, and hybrid-to-test card. Together there are ≈ 1600 bond connections. All connections are made with ultra-sonic aluminum bonds with a wire diameter of $25\,\mu m$. Loading, bonding and unloading of the modules typically takes less than 1 h per module.

Construction of the supermodule core requires laminating, curing, and cutting of the carbon fiber skins; laminating the bus cables on the cut carbon fiber skins; cutting sheets of Rohacell foam; bending and heat forming the PEEK cooling tubes; and laminating these ingredients together. A number of additional finishing steps are described elsewhere [32]. None of the core construction

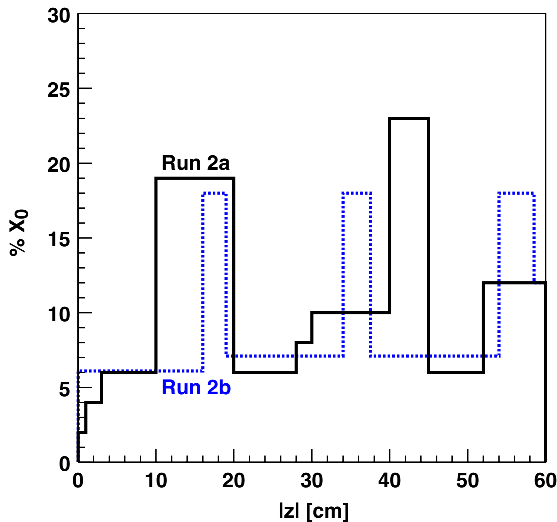

Fig. 9. The average material of the Run IIa and Run IIb silicon detector designs is compared for normal incidence trajectories as a function of position along the beam line ($|z|$). The black curve corresponds to Run IIa, and the light curve to Run IIb. The three peaks at $|z| = 18$, 36, and 56 are caused by the Run IIb hybrids.

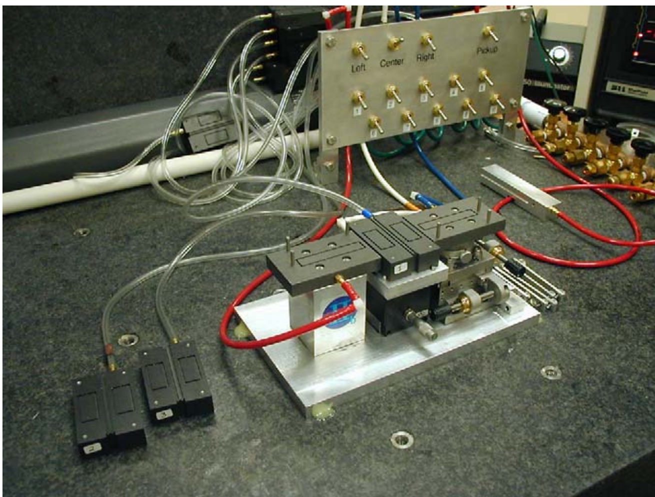

Fig. 10. Fixture to align and glue two sensors to a module.

steps is exceptionally challenging or time consuming. Curing time and the number of available fixtures determine the production rate.

After supermodule core assembly, the mini-port card and the sensors are mounted. Precision alignment of the axial modules on the core is crucial due to the use of the axial information in the secondary vertex trigger (SVT). The axial strip to beam axis angle is specified to be less 180 μrad, and the axial module should be aligned with the supermodule axis to 39 μrad. This was achieved for 42 of the 45 axial modules mounted on the supermodules. The average (absolute) deviation from the nominal position is 21 μrad. The stereo sensors hits are not used in the SVT so less precision is required.

6. Silicon sensors

The silicon sensors for the Run IIb detector are single-sided p^+-doped microstrips on n-doped bulk silicon, manufactured by Hamamatsu Photonics [33]. The supermodule sensors' main specifications are given in Table 4.

The sensors must withstand high particle fluences and are designed to operate at high bias voltages. Therefore, they can be fully depleted and have high charge collection efficiency even after type inversion of the n-bulk. To delay high voltage operation and to increase the lifetime of the detector, the substrate resistivity was chosen to be relatively low, with a minimum initial depletion voltages of ≈ 100 V. All sensors are AC coupled and biased through a polysilicon resistor. Between neighboring readout strips, one biased intermediate strip is placed, which is not connected to a preamplifier. The presence of the intermediate strips improves the position resolution without increasing the number of readout channels. This arrangement is made possible by the good noise performance of the SVX4 chip.

Three different sensor designs are used. The L0 sensors are identical to the L00 sensors of the Run IIa detector and are described elsewhere [34]. The design of the supermodule sensors is similar to those developed for the LHC detectors, and therefore required minimal R&D.

The supermodule sensors are produced on 150 mm wafers with two sensors per wafer. The wafer thickness varies by 15 μm about its nominal 320 μm thickness. The crystal orientation is ⟨100⟩. There is only one guard-ring. The distance between the scribed edge and the sensitive sensor area is 1 mm. The bowing of the sensors due to the different thermal expansion coefficients of silicon and silicon dioxide is less than ≈ 75 μm.

The supermodule sensors have 512 AC coupled readout strips, which have a pitch of 75 μm or 80 μm. The strip width is 8 μm and is fully covered by a 15 μm wide

Table 4
Main specifications of the supermodule sensors

Parameter	Axial	Stereo
Overall dimensions	$40.6 \times 96.4\,mm^2$	$41.1 \times 96.4\,mm^2$
Strip pitch	37.5 μm	40 μm
Readout strip pitch	75 μm	80 μm
Number of strips	512 readout and 513 intermediate strips	
Depletion voltage	100 to 250 V	
Sensor leakage current	<2 μA at 20 °C and 500 V	
Poly resistor values	1.5 ± 0.5 MΩ	
Passivation	0.5–1 μm thick SiO_2	
Strip width	8 μm implant and 14 μm aluminum strip	
Implant	depth >1.2 μm doping $>1 \times 10^{18}$ ions/cm^3	
Aluminum strip	Thickness >1 μm, resistivity <30 Ωcm	
Coupling capacitor	capacitance >120 pF breakdown voltage >100 V	
Interstrip resistance	>1 GΩ	
Total interstrip capacitance	<1.2 pF/cm	
Bad channels	<1%	

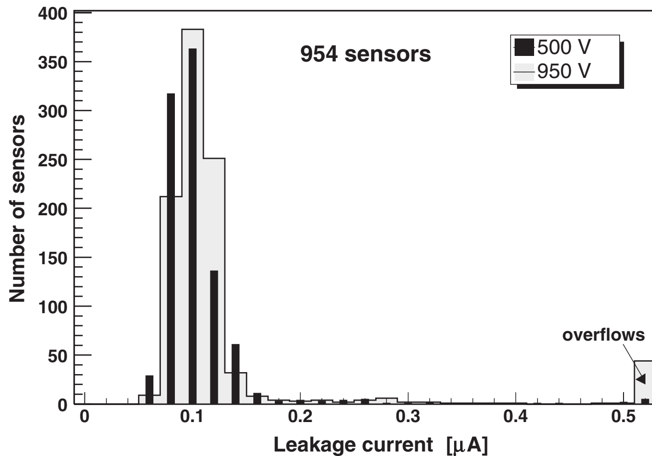

Fig. 11. Leakage currents before irradiation at 500 and 950 V. Leakage currents exceeding 0.5 μA are displayed in the overflow bin at the right of the figure.

aluminum layer. The supermodule sensors come in two flavors, either with axial strips to measure the radial track position or with strips in a 1.2° stereo angle allowing moderate (<1 mm) resolution of the coordinate along the beam axis. To build the Run IIb detector, 1512 axial and 648 stereo supermodule sensors, and 144 L0 sensors are needed.

A sample of 954 sensors have been inspected for their electrical and mechanical properties and were found to be well within their specifications. A comprehensive summary of the test results is given in Ref. [35]. The sensor leakage currents for two different voltages well above the operating voltage are displayed in Fig. 11. The sensor leakage at 500 V is typically 0.100 μA at 20 °C. No sensor has a leakage current above 2 μA, and 97% of the sensors have leakage currents below ≈ 0.5 μA even at 950 V.

A sample of five sensors was irradiated with neutrons up to a fluences of 1.4×10^{14} neutrons/cm^2. Leakage currents of ≈ 6 mA are typically measured for these fluences (at 500 V bias voltage and 20 °C). Due to the type inversion and charge accumulation in the oxide layer, interstrip capacitance, resistance, and bias resistor resistance are degraded. However, the measured electrical properties remain within the specifications, when the detectors are biased with voltages of 250–300 V, well above the full depletion voltage. The measured detector performance after irradiation is thus very satisfactory.

7. Front-end electronics

7.1. The SVX4 integrated circuit

The SVX4 readout chip is a mixed-signal custom integrated circuit, fabricated in a 0.25 μm CMOS commercial process by Taiwan Semiconductor Manufacturing Company (TSMC) [36]. The chip architecture is similar to that of the SVX3 chip [18] currently in use at the CDF experiment.

The chip contains 128 parallel charge-integrating preamplifiers, each with a 46-cell-deep analog pipeline capable of buffering up to four samples; an 8-bit Wilkinson type analog-to-digital converter (ADC); a digital readout sparsification circuit with differential transceivers; a 192-bit deep configuration register, including a 128-bit deep channel mask; and a shadow register, a single-event upset (SEU) resistant copy of the configuration register excluding the channel mask.

A conceptual schematic and block diagram of the SVX4 are shown in Figs. 12 and 13, and basic chip properties are listed in Table 5. A correlated double sample of the input charge, performed by the pipeline, extracts the signal and reduces low-frequency noise and offsets. The programmable risetime of the preamplifier stage in turn limits high-frequency noise. The preamplifier was designed to achieve an equivalent noise charge of less than 2000 e^{-} for an input capacitance of 40 pF and a nominal integration time of 132 ns. Typical noise values are shown in Fig. 14 for different loads. A valuable feature of the SVX4 preamplifier is a programmable "black-hole" elimination circuit. If activated, a selected preamplifier channel is able to shunt a current beyond 1 mA from a shorted detector strip (pinholes) while the neighboring channels are properly read out [23]. The digital section of the chip is fully synchronous with an externally supplied clock. (The nominal clock frequency at the Tevatron is 53 MHz to be synchronous with the accelerator radio frequency). The Wilkinson ADC counter runs at double the external clock frequency and has been tested to operate properly up to an effective rate of 500 MHz. Detailed descriptions of chip operation and properties are given in Refs. [24–26].

Features of the SVX4 design include optional data sparsification, deadtime-less operation, and real-time pedestal subtraction. (The latter features were introduced in the SVX3 chip and reproduced in the SVX4.) Deadtime-less performance, i.e. continuous data acquisition also during digitization and readout, can increase trigger bandwidth substantially and thus offer great physics advantages. The low resistivity substrate of the bulk CMOS process is exploited to carry all analog ground currents and effectively decouple the low noise analog section from the digital section of the chip. Deadtime-less performance of the chip is excellent as is discussed in Ref. [25] and Section 10 of this paper. Sparsification of channels with a signal exceeding a programmable sparsification threshold is a feature of the SVX4 and all CDF designs going back to the original SVX [27]. The chip can perform real-time pedestal subtraction (RTPS) to suppress common-mode effects.

A large number of programmable parameters and features makes the chip very flexible. Programmable chip parameters include integrator bandwidth, preamplifier and pipeline current, pipeline delay, sparsification threshold and modes, real-time pedestal subtraction, a charge

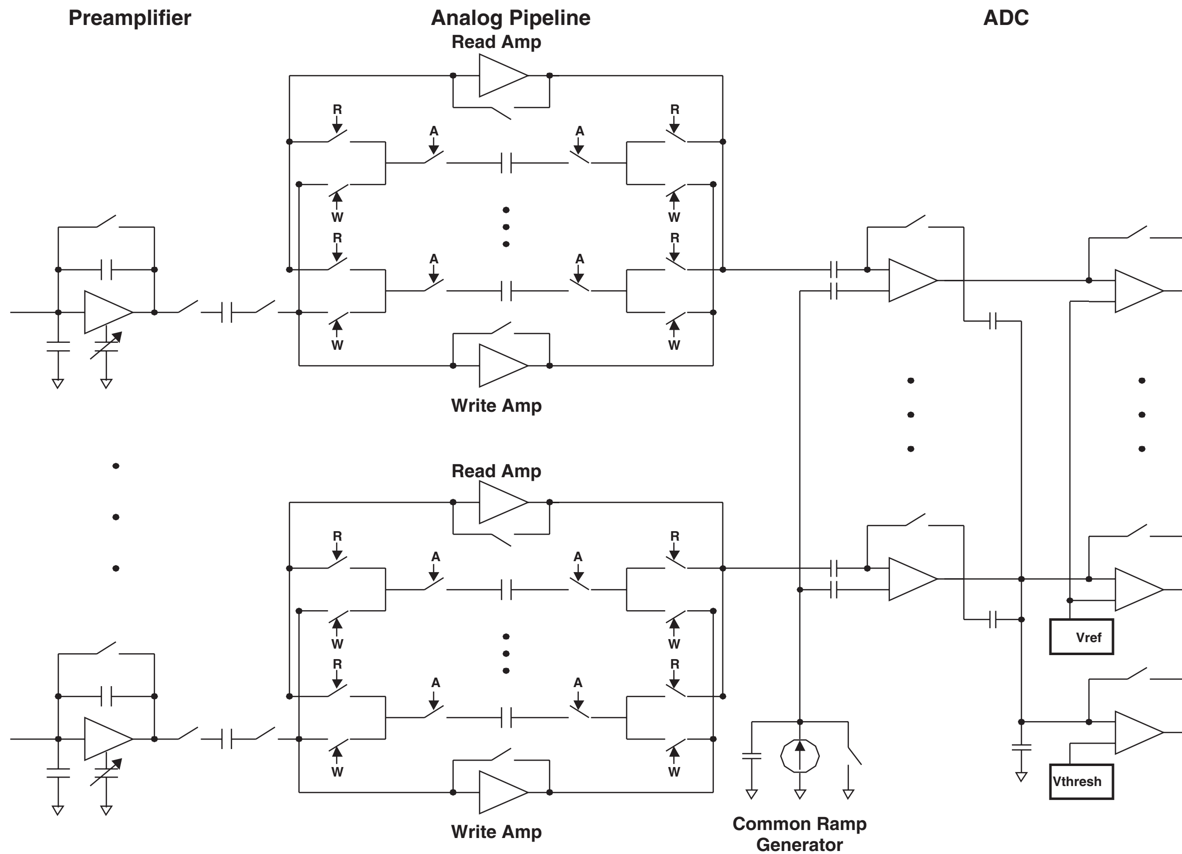

Fig. 12. Block diagram illustrating the functional units of the SVX4 chip.

calibration and bad channel mask, ADC ramp slope, pedestal level, and data driver currents.

The main improvement over the SVX3 chip is the much-increased radiation tolerance. This is a consequence of the thin gate oxide layer of the 0.25 μm CMOS process and of the enclosed N-MOS transistor topologies developed by the RD-49 collaboration [22]. The chip has substantially lower noise than its predecessors, in particular after irradiation. Extensive irradiation measurements on a number of chips and hybrids were performed with different sources: up to 20 MRad at a 19,000 Cu^{60} Co γ-ray source; up to a fluence of 2×10^{14} 63 MeV protons/cm^2 at the UC Davis cyclotron; and up to a fluence of 9×10^{8} Si, Cl, Va, Ni, Ag and iodine ions at the SIRAD beam line of INFN Legnaro.

The SVX4 chip does not show a relevant change in noise, gain, pedestal, or the like, and functions well up to ≈ 25 MRad, which is well above the design specification. This is illustrated in Fig. 15. Single-event upset (SEU) rates were determined for the configuration register, shadow register, and data memory cells [37] and are shown in Fig. 16.

We find that the linear energy transfer (LET) threshold for SEU exceed $\approx 20\,\mathrm{MeV\,cm^2\,mg^{-1}}$ and that SEU cross sections are an order of magnitude lower than for the SVX3 chip. The chip is thus very well suited for particle physics applications in an intense radiation field. The SEU cross section for a $1 \rightarrow 0$ bit flip is significantly higher than for a $0 \rightarrow 1$ bit flip, as was observed elsewhere for this technology [38]. The shadow register uses an early version of the DICE cell [39] developed by the ATLAS Pixel group. As expected, it is found to be several orders of magnitude more radiation-tolerant than the configuration register. Lastly, we observe a significant increase of the SEU cross section by a factor 3–5 for a 45° incidence compared with normal incidence.

While the CDF Run IIb silicon detector will not be built, the SVX4 chip is used in other particle physics experiments [40,41].

7.2. The beryllia hybrids

The purpose of the hybrid is to carry the SVX4 chips, to receive and distribute analog and digital power, with various control and clock signals, and to send the combined digitized data stream back to the DAQ system. The hybrid also filters the high voltage bias line and carries a temperature sensor.

The design requirements of the hybrid and the overall system are closely intertwined. The hybrid must be compact and lightweight in order to minimize its contribution to the supermodule radiation length. It must perform well in deadtime-less operation despite being glued directly on top of the silicon sensors. The heat of the chips must

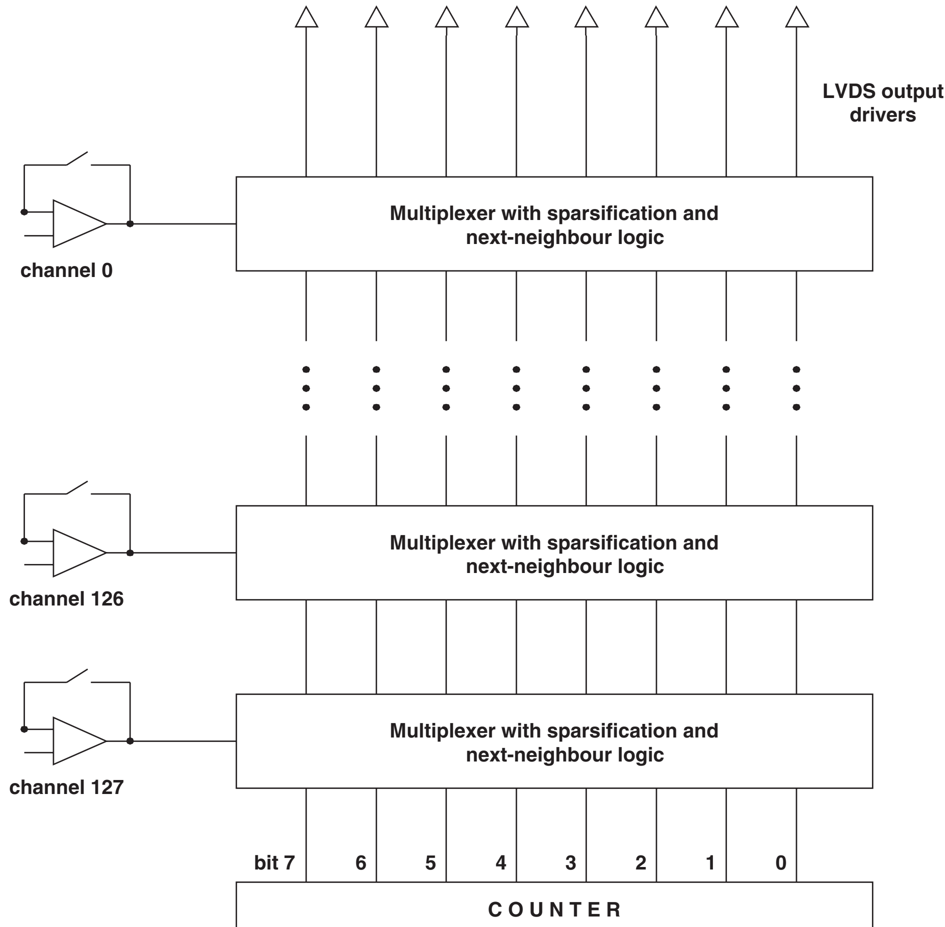

Fig. 13. Sketch of the SVX4 readout unit. The comparators of the ADC section of the chip are shown on the left side of the figure.

Table 5
Parameters of the SVX4 chip

Parameter	Value
Die size	6.3 mm × 9 mm
Analog/digital voltage	2.5 V/2.5 V
Current consumption analog/digital	50–100 mA/10−30 mA
Preamplifier gain	5 mV/fC
Pipeline voltage gain	3
Total gain	15 mV/fC
Preamplifier dynamic range	$>$200 fC
Pipeline dynamic range	$>$100 fC
Pipeline depth	46 cells
Risetime (10–90%) at 10 pF load	20–70 ns
Reset time	20 ns
Max. digitization/readout rate	$>$250 MHz/$>$8 × 50 Mb/s
Max. radiation dose/fluence	$>$20 MRad/1.5 × 10^{14} p/cm^2

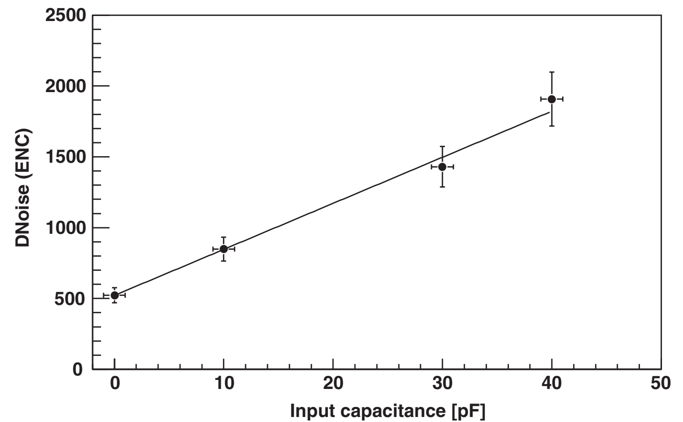

Fig. 14. Best noise performance of the SVX4 chip achieved with the maximum preamplifier risetime settings. The fitted line corresponds to the formula ENC $= 521.5\,e^- + 32.5\,e^- * C/$ [pF] rms. The integration time is ≈ 125 ns.

flow efficiently through the sensors and the bus cable into the cooling pipes. Of course, the hybrid should also be robust and reliable. Finally, technological risks and significant R&D must be minimized to keep a tight schedule.

These requirements were satisfied by choosing a photo-imageable thick film process (Fodel technology) [42,43] on a beryllia (BeO ceramic) substrate. CDF has gained substantial experience with these materials and processes [44] for previous silicon detector projects. The beryllia

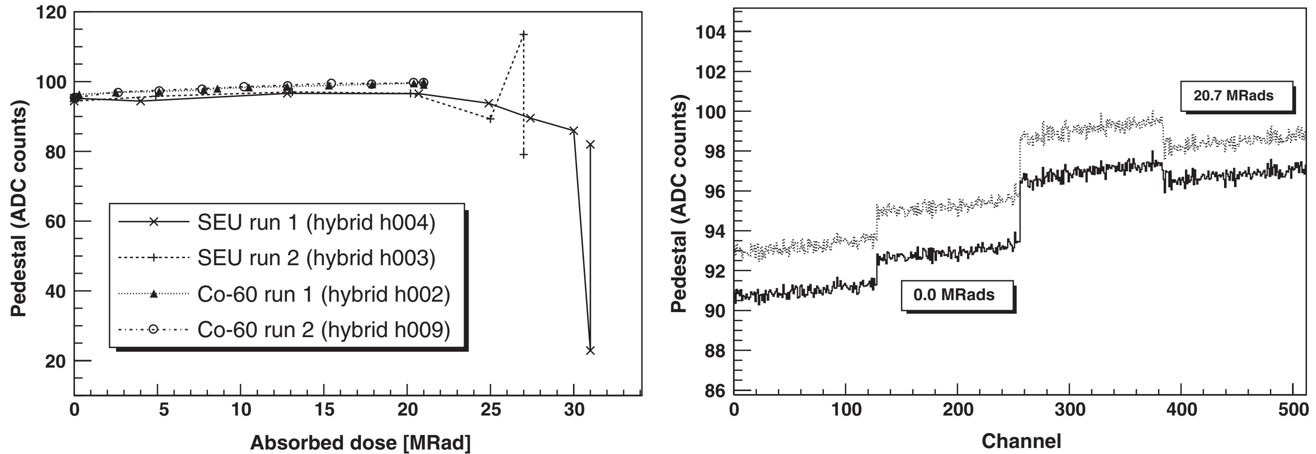

Fig. 15. Left: pedestal average over all channels of four SVX4 chips of a CDF Run IIb hybrid versus absorbed dose. Two of the hybrids were irradiated in a ^{60}Co γ-ray source, and two in the UC Davis proton cyclotron. Right: pedestal versus channel number for a hybrid before (bottom curve) and after proton beam irradiation (top curve). The pedestal is averaged over 10 consecutive events.

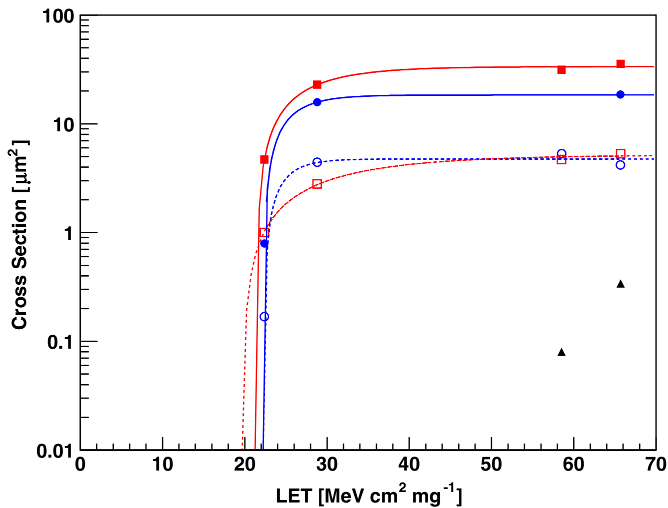

Fig. 16. Single bit SEU cross sections of the initialization shift register (circles), shadow register (triangles), and output FIFO (squares). The solid symbols are the cross section for a 1 → 0 bit flip, the open symbols for a 0 → 1 bit flip.

substrate offers excellent heat conductivity and long radiation length. By using photo-imageable thick film materials, printing and pattern generation are separated and can be optimized independently, which leads to an increased resolution and density compared with "traditional" thick film technology.[3] The minimum trace width, space width, and via size used on the hybrid are 125 μm, 75 μm, and 150 μm, respectively. These are conservative choices for this process which helped increase the hybrid yield and reduce costs.

Details of the Run IIb hybrids are summarized in Ref. [45]. The schematic of the supermodule hybrid is shown in Fig. 17. This circuitry is realized in a compact layout with only four gold conductor layers and a total size of $38 \times 20 \times 0.380\,\mathrm{mm}^3$. The hybrid carries four SVX4 chips, which cover 30% of its area, and 30 passive components. Resistors are used for control signal and clock terminations, and to set currents. Two ceramic decoupling capacitors (100 nF each), one for analog and one for digital power, are located near (≈ 1 mm) each SVX4 chip in the small gap between adjacent chips. The hybrid also contains an RC bias voltage filter and a thermistor (RTD) to monitor hybrid temperature. A picture of a hybrid mounted on a sensor is shown in Fig. 18. A separate alumina thin-film pitch-adapter glued next to the hybrid is also visible.

The hybrid material corresponds to 0.21% of a radiation length and contributes 12% to the total radiation length of a supermodule. The substrate, dielectric, and gold conductor layers contribute 24%, 24%, and 33%, respectively to the hybrid total. Three of the seven dielectric layers are located at the back side of the hybrid, to minimize bowing and to improve the flatness of the hybrid.

For the innermost layer (L0), a second hybrid type was designed and produced using the same process. The L0 hybrid is narrower ($22.5 \times 33 \times 0.380\,\mathrm{mm}^3$) than the supermodule hybrid and carries only two SVX4 chips. The hybrid is not served by a mini-port card and receives differential control signals only. A custom 0.25 μm CMOS transceiver chip [46] is placed on the hybrids and generates the eight single-ended CMOS control signals the SVX4 chips require (when operated in CDF mode). Four flexible circuit cables are connected to the L0 hybrid. Two fine-pitch cables that carry the analog detector signals are glued to the top side of the hybrid. The cables are connected electrically with wire bonds. On the other end of the hybrid, two more cables are soldered and provide analog and digital power, high voltage, clock, control and data

[3]The Fodel process is reported to resolve 40 μm wide traces and 50 μm wide spaces over significant areas [42]. The minimum resolved via diameters are 75 μm for a 150 μm pitch.

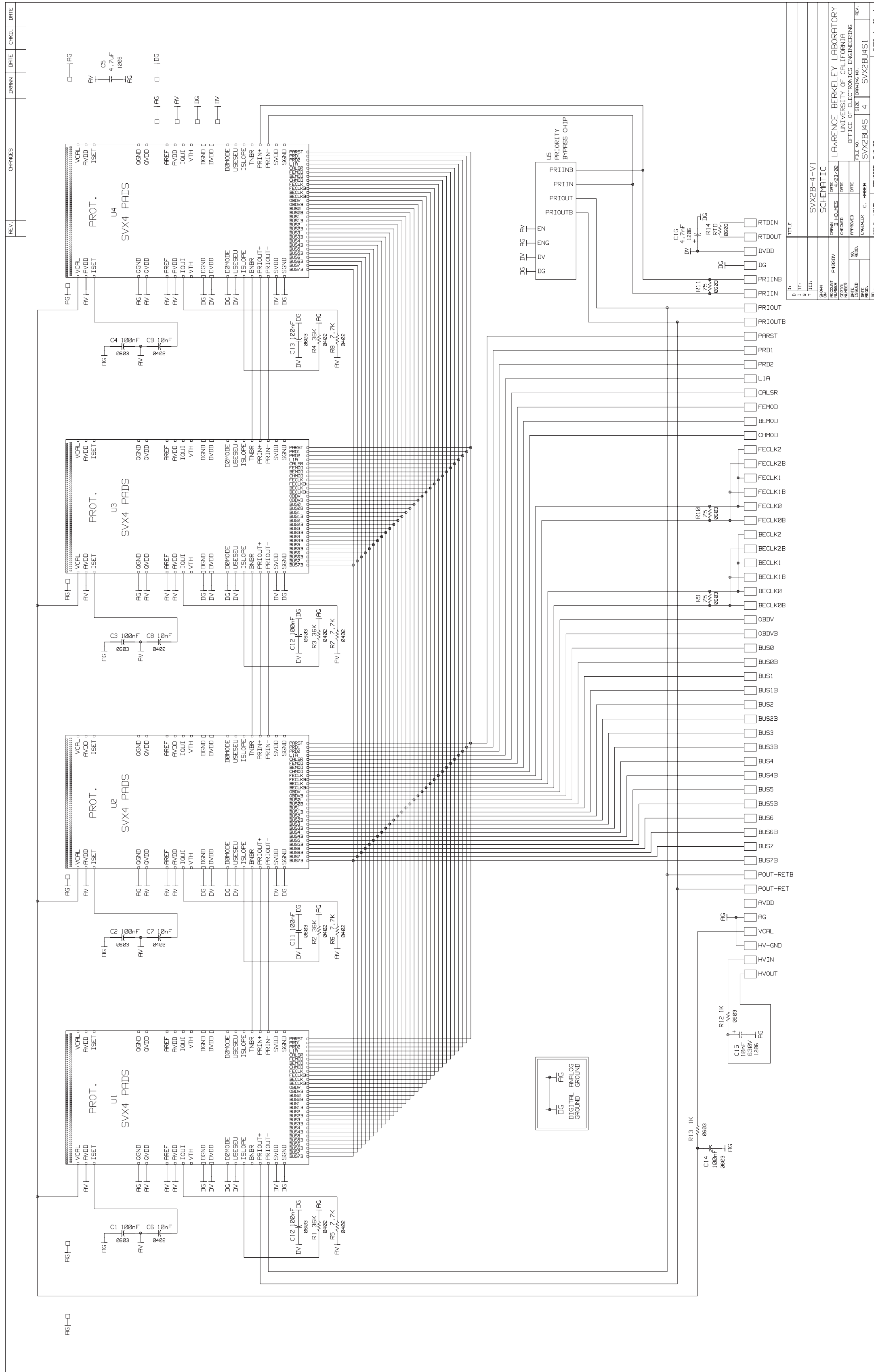

Fig. 17. Schematic of the supermodule hybrid. Note that the capacitor C5 shown here was eliminated due to space constraints. The termination resistor chip for the eight pairs of bus lines (BUS0-BUS0B through BUS7-BUS7B), which is only needed for the last hybrid on a supermodule, is not shown.

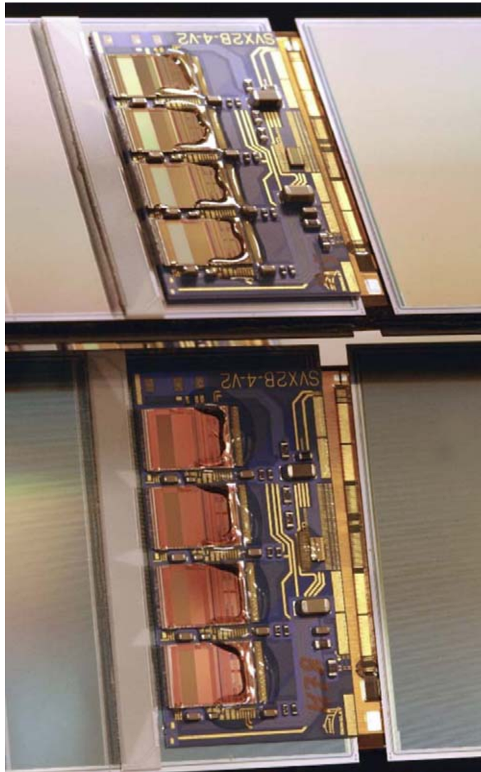

Fig. 18. Photograph of two hybrids on adjacent supermodules installed in the barrel. The pitch adapter, sensors, and the bus cable bond pads are also visible.

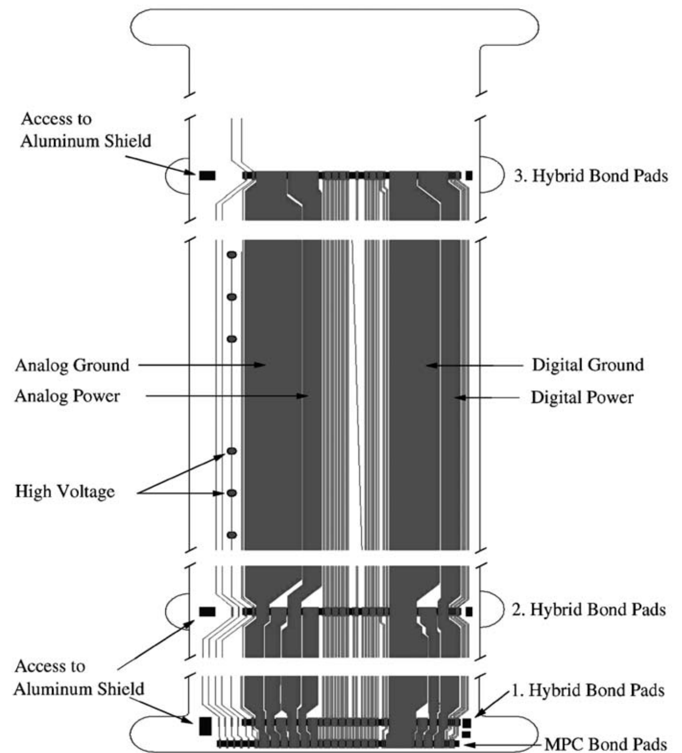

Fig. 19. Sketch of the bus cable layout with cutouts. The horizontal axis of the cable is stretched and much of the straight trace sections outside the bonding regions for the mini-port card (bottom) and the three hybrids are not shown. The middle section shows six openings on the left side, which serve as the high voltage connections to the sensor backplane. This section also contains the front-end clock trace that is tilted to minimize capacitance to any individual sensor strip.

signal connections. More details on the L0 hybrid are given in Ref. [45].

7.3. The bus cable

Two identical 59-cm-long copper/polyimide/aluminum flexible circuit laminates (“bus cables”) are mounted on the supermodule, one on each side, directly under the silicon sensors. The bus cable has the following electrical functions: it provides high voltage to the sensors; supplies analog and digital power, and clock and control signals to the hybrids; it transmits the data to the MPC; and it reads out the hybrid thermistors.

The cable has a simple mechanical structure with consecutive polyimide/copper, polyimide, aluminum, and polyimide layers interleaved with adhesive layers. The copper layer is 18 μm thick[4] and contributes ≈ 3.5% to the supermodule radiation length. This makes the use of more than one trace layer undesirable. The 50 μm thick aluminum layer, which contributes a similar amount to the material budget, serves as a shield between the copper trace layer and the silicon sensor high voltage backplane. (A cable version with a 25 μm thick aluminum layer was also produced but has slightly inferior electrical shielding efficiency, as is shown in Section 10.) The aluminum layer is split in three parts along the length of the cable, each shielding one module. Each part is connected with the corresponding hybrid ground through multiple bond connections (see Fig. 8). The cable is ≈ 220 μm thick.

A detailed view of the bus cable layout is shown in Fig. 19. The wide traces distribute power and the narrow traces carry clock, control, and data signals. The minimum copper trace width is 75 μm, and the minimum space width between traces is 100 μm. There are no vias within the cable. High voltage is provided to the back of the sensors through openings in the polyimide and aluminum layers of the bus cable. After reaching the last hybrid, all traces stop with the exception of the bias voltage traces which serve the last module.

Due to the proximity of the bus cable and the sensor, care must be taken to suppress electromagnetic coupling of bus cable activity into the silicon sensors. Voltage or current variations of millivolts or milliamperes can cause pedestal fluctuations that are a fraction of a MIP or larger, which increase fake occupancy, therefore increase readout time, and eventually compromise hit resolution. Common mode effects, which affect all channels equally, can be suppressed by the SVX4 real-time pedestal subtraction [19]. However, local interference effects, e.g. from a control line below a strip, cannot be removed in this way.

[4]Corresponding to $\frac{1}{2}$ oz of copper per square foot.

Various electromagnetic interference effects were studied in prototype supermodules and were successfully suppressed by optimizing the cable layout. These effects, measurements, and performance are discussed in more detail in Ref. [47]. Capacitive interference is suppressed by the grounded aluminum shield, while conductive interference is suppressed by minimizing resistance of the power traces. The latter is achieved by maximizing the width of the bus cable power traces. Analog power and ground and digital power of the hybrids are all kept separate. Power traces end at their destination hybrid and the freed space on the bus cable is taken by the power traces for the remaining hybrids. A wide digital ground trace is common to all three hybrids. Keeping digital power separate makes possible switching off the digital circuitry of a hybrid in case of a major chip malfunction, in order to limit power consumption and to prevent a broken chip from blocking hybrid readout.

7.4. The mini-port card

The mini-port card (MPC) is located at the top side of supermodule. It is responsible for signal translation and repetition from the SVX4 readout chips to the data acquisition system and vice versa. The MPC also distributes high voltage to the silicon sensors, as well as analog and digital power to the six supermodule hybrids. The active components of the MPC are five identical transceiver chips [46]. The custom chips are produced in the same radiation-hard 0.25 μm CMOS process that is used for the SVX4 chips. The MPC also carries 45 surface-mount resistors and capacitors. A picture of the MPC is given in Fig. 20. Details on the MPC are available from Ref. [48].

The MPC serves both sides of the supermodule. It is connected to the top bus cable with wire bonds. A flexible circuit ("wing") cable is soldered to one edge of the MPC. This cable is folded over to the bottom of the supermodule where it is glued to the bus cable. The electrical connections between the wing and the bottom bus cable are again through wire bonds. Two further flexible cables, the data/HV pigtail and the low voltage (LV) pigtail, are attached to the MPC and connect it to the Junction Port Card (JPC) outside the detector volume.

Fig. 20. A photograph of the top side of the beryllia mini-port card.

The MPC was fabricated in two alternative technologies, based on a beryllia or a polyimide substrate. The electrical function of the two versions are identical. They cover the same area ($50.8 \times 39.4\,\mathrm{mm}^2$), have a similar thickness (780 and 750 μm), and are realized in a six metal layer layout. The signal integrity of both MPC versions is excellent. The electrical and noise performance of modules driven with an MPC are identical to that obtained in dedicated bench measurements without an MPC.

The minimum gold trace width and space of the beryllia MPC are 75 μm each, while those of the polyimide copper traces are 100 μm each. The material of the beryllia MPC averaged over the supermodule area corresponds to $\approx 0.089\%$ of a radiation length while that of the polyimide is $\approx 0.067\%$. A nice feature of the polyimide MPC is the integration of the three flexible cables into the MPC substrate. This reduces the number of solder connections from 159 to 32, simplifying MPC assembly significantly.

Heat conduction of the beryllia MPC is superior to that of the polyimide one. The main heat sources are the transceiver chips which produce ≈ 0.5 W each. The temperature profile of the MPCs was simulated and measured. In order to optimize thermal performance of the polyimide MPC, nine thermal vias are placed under each transceiver chip. The vias connect to a copper strip at the bottom layer of the MPC, which is in good thermal contact with the supermodule cooling pipes. This limits the transceiver temperature to $\approx 13\,^\circ$C for a coolant temperature of $-10\,^\circ$C. The typical transceiver temperature on the beryllia MPC is $\approx 6\,^\circ$C. A choice between these designs would have been the next step but would have primarily reflected perceived manufacturing and scheduling issues.

8. The innermost layer (L0)

The innermost silicon layer, L0, is similar to L00 of the Run IIa detector. The L0 sensors are 1.485 cm wide and 7.85 cm long. They are single-sided AC-coupled p-on-n microstrip sensors as are the supermodule sensors. The L0 strip pitch is 25 μm, and every other strip is read out. Pairs of sensors are glued and bonded together, and each pair is read out by one (L0) hybrid. The sensors are supported by a castellated carbon fiber structure. The r–ϕ view of L0 is given in Fig. 2. Unlike L00, the L0 of Run IIb is supported by the supermodule barrel and not by the beam pipe.

Due to the limited space in the center of the detector, the hybrids are located at larger radii at the end of the interaction region at $\eta \approx 3.7$ (see Fig. 21). This reduces the material in the detector and decreases the hybrid radiation dose. On the negative side, the sensor strips and the hybrids are connected with fine-pitch flexible cables up to 60 cm long. This increases the capacitive load of the SVX4 chip, causing noise performance of L0 to be worse than that of the supermodule layers. The same cables also provide high voltage and ground.

Two fine-pitch cable designs, produced by different vendors, were investigated. Both designs have 100 μm trace

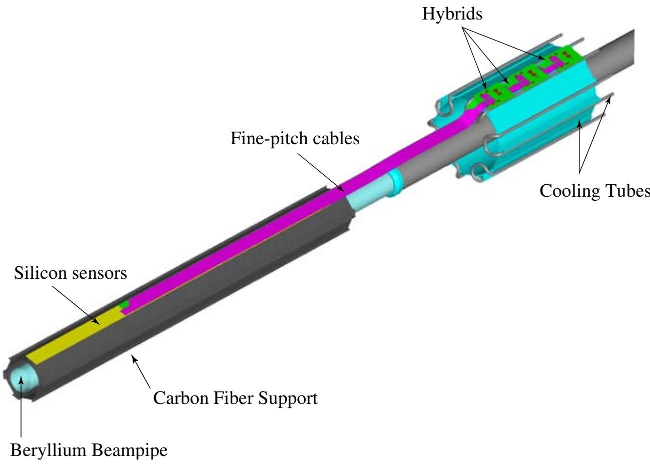

Fig. 21. The innermost layer, L0. The sensors on the left are not covered by the fine-pitch cable, while all other sensors are. The hybrids are located on the right side of the picture. Only one of the twelve ladders (the top one) is shown in the picture.

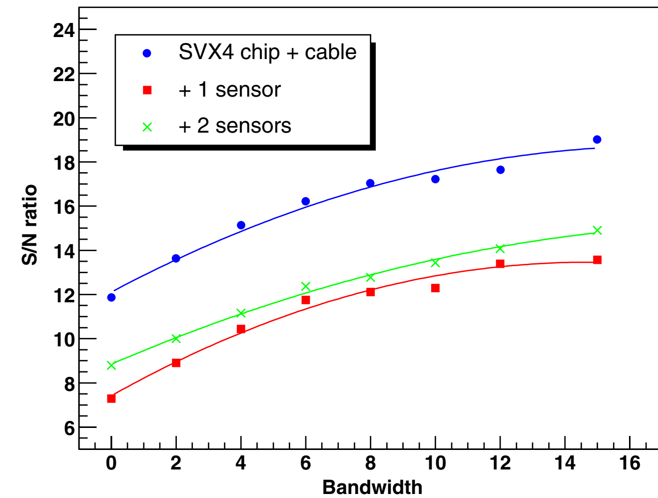

Fig. 22. Signal-to-noise ratio of a L0 prototype for different bandwidths (BW). A large value of the bandwidth bits (at the right of the plot) corresponds to maximum preamplifier risetime and vice versa. Three configurations are shown: the bare chip and cable not being connected to a silicon sensor (SVX4 chip + cable); the same wire-bonded to one sensor (+1 sensor) or to two sensors (+2 sensors). The latter case is the nominal configuration.

pitch over most of their length. One design necks down to 47 μm pitch at both the hybrid and the sensor end. This design turned out to be very challenging, and the yield was low even for an increased trace width of 35 μm. The design selected for L0 keeps the trace pitch of 100 μm constant over the full cable length, while the trace width is only 15 μm. Two overlapping cables, staggered by 50 μm with respect to each other, are needed to readout all strips. This design requires a more complicated bonding scheme, but cable capacitance is reduced, and the yield is acceptable.

With this arrangement, a signal-to-noise ratio (S/N) up to 13 has been obtained in L0 prototypes (see Fig. 22), which is sufficient for reliable track reconstruction.

Unlike the other Run IIa layers, once installed, the pedestal of the L00 layer was not sufficiently uniform to operate the detector in deadtime-less mode. All channels are read out and the pedestal is determined by offline fits in order to identify particle hits. Unfortunately this procedure increases the data volume and the readout time, and prevents use of the precision L00 hits in the secondary vertex trigger. To avoid this situation in Run IIb, the pedestal uniformity of a L0 prototype was studied in detail [49]. The pedestal was found to be sufficiently flat, and no relevant pickup "noise" is present in the system if the carbon fiber structure carrying L0 is well grounded.

9. Prototyping and preproduction experience

Prototyping and preproduction of the CDF Run IIb silicon project was smooth and essentially proceeded on or ahead of schedule. An overview of preproduction numbers and yields is given in Table 6. A summary of the preproduction experience, which focuses on practical issues and explicitly emphasizes things which did not go so well initially, is given below.

The sensor quality was excellent and no change of the prototype layout was required for preproduction. None of the sensors showed break-down below 500 V. Approximately 8% of the sensors failed the wafer resistivity specifications which led to a depletion voltage below 100 V. These sensors were still usable for the supermodules

Table 6
Number and yield of preproduction supermodules and components. The quantities needed to build the full detector are also given. The L0 components, which reached the prototype stage only, are not included. Due to the limited number of MPCs and supermodules, statistically significant yield cannot be determined

Component	Built in preproduction	Needed in Total	Yield	Most likely number of bad channels
SVX4 chips	782	4464	79%	0
Sensors	953	2160	>92%[a]	0
Hybrids	117	1080	89%	0
Modules	92	1080	83%	0
MPCs	25	180	n/a	n/a
Bus cables	70	360	77%	n/a
Supermodules	$11+\frac{1}{2}$	180	n/a	≈ 10

[a]The remaining sensors are fine for use at the outer radii.

at the outer radii. The fraction of bad readout strips measured on a subsample of sensors was found to be 0.04%.

The use of a commercial 0.25 μm CMOS technology for the SVX4 chip and the availability of reliable design tools led to a high yield. During chip design, two test chips with preamplifier and/or pipeline circuits and two full designs including the final chip were submitted. All of them were fully functional. The main design and testing process was completed in two years. Although essentially all subcircuits of the SVX3 chip had to be redesigned, the functionality of the chip was already well defined and precise specifications were available from the start of the project.

Three of the SVX4 wafers were probed during preproduction. The most frequent cause for rejecting an SVX4 chip in preproduction was bad pipeline capacitors. (Each chip has $128 \times 46 = 5888$ pipeline capacitors.) Of the 782 chips with probing data, 500 had no defects. For preproduction, only chips with at most one bad pipeline cell were accepted, which resulted in a yield of 79%. Accepting two bad capacitors would have given an 85% yield. Chips with an entire dead channel were rejected. Failure of a few pipeline capacitors is a relatively minor defect and much less stringent criteria have been used for other projects. The correlation of SVX4 wafer probing data and the data taken for the same chip when assembled on a hybrid is excellent.

CDF has gained considerable experience with beryllia hybrids, and hybrid production was smooth and did not pose significant technical difficulties. Several batches of patterned beryllia substrates were received during prototyping and preproduction. All were of high quality and less than 3% of the substrates were rejected due to shorts or opens between power traces. Hybrid yield after component placing, die attach, and bonding was 89%. Hybrids with one bad channel or more than one bad pipeline capacitors were rejected. The cause for half of the rejected hybrids was incorrect labeling of probed SVX4 chips and poor encapsulation craftsmanship on a small number of hybrids.

Hybrid testing was largely based on sophisticated automated tools, which were developed for the SVX3 chip wafer probing and hybrid testing [50]. Approximately 40 hybrids could be assembled and tested per week, which is the nominal rate. Doubling this rate seems conceivable. After initial acceptance, the hybrids were subjected to a 72 h automated burn-in procedure; a repetitive cycle of data acquisition, digitizing and readout, complemented by periodic data integrity tests as well as current and voltage measurements. The full series of hybrid quality checks also used for initial testing is applied at the beginning and end of the burn-in period. Thirty-two hybrids could be run in parallel on the burn-in test-stand. All 101 hybrids submitted to the burn-in process passed [51].

In the process of optimizing the deadtime-less performance of the Run IIb silicon detector, various bus cable versions were submitted to two different vendors. Overall, cable manufacturing was straightforward and provided excellent quality and high yield with the exception of a few initial difficulties due to the length of the cable and its integrated aluminum shield. The cables were on average ≈ 250 μm shorter than specified. Compensating the layout by the appropriate amount led to cables of the desired length. The alignment of the laser-cut aluminum foil with the other cable layers turned out to be poorly controlled. This was addressed by generous distances (> 250 μm) between open copper and aluminum areas in the layout of the cable. During manipulation the cables tend to bend in the bond area region, which is substantially thinner than the rest of the cables due to openings in the polyimide layers. Care in handling and temporary reinforcement tabs outside the genuine cable cross section solved this problem.

Module yield was 83%. In the early stages of module assembly some sensors were broken during handling. After refinement of the module frames, wire bonding fixtures and test fixtures, the most likely reason for module rejection became bad channels. This was largely related to defects on the aluminum-on-alumina pitch adapter (PA). After more careful inspection of the PA for shorts, opens, scratches, and discolorization of the deposited aluminum, the bad channel rate dropped. Only modules with fewer than six bad strips (out of 512 strips) were accepted for supermodule construction. Most of the modules did not have a single bad strip.

During preproduction both mini-port card versions were used for supermodule construction and performed well electrically. Due to the cancellation of the project the final version was not yet selected, and the fixture to mount the MPC to the supermodule was not yet finalized. The bending of the wing cable, which connects the MPC to the back side of the supermodule, turned out to be more complicated than anticipated for the beryllia MPC and led to some broken traces. This effect, which was not present in prototyping, could have been cured by varying the wing cable copper thickness, or by optimizing the geometry of the solder pads. The polyimide MPC did not show this problem. It should be noted that despite the significant advantages of using a polyimide technology in terms of radiation length, lead time and price, several vendors had to be utilized before a workable product emerged.

Efficient and expedient testing of chips, hybrids, module, and supermodules was crucial for the technical success of the project. As part of the CDF Run IIb project, the VME-based Run IIa DAQ system was upgraded successfully. The Run IIb VME-based DAQ, while capable to read out the complete future Run IIb detector, turned out to be impractical for quick evaluation and debugging of Run IIb prototypes. Instead a simple, flexible, and relatively inexpensive DAQ system, the PCI Test Stand (PTS) was developed [52,53].

The PTS consisted of a Linux host computer and two specialized boards, a PCI Test Adapter (PTA) and a Programmable Mezzanine Card (PMC). Exploiting on-board field-programmable gate arrays (FPGAs) [54] which could run with clock speeds up to 50 MHz, command

sequences were clocked into SVX4 chips and data were read out at the same speed they would be in the finished detector. Data acquisition with the PTS was performed through a custom ROOT-based [55] graphical user interface software package (ROOTXTL). The test features implemented included pedestal read-back, noise measurement, a charge injection scan for SVX4 gain measurement, a bandwidth scan, and a deadtime-less scan. Multiple PTS stations were deployed during the preproduction phase; they were used to test many different hardware configurations, from single SVX4 chips to five supermodules read out simultaneously.

During preproduction, 11 supermodules were fully assembled. Another supermodule was only loaded with modules on the top side.

10. Electrical performance

Crucial for the electrical performance of the Run IIb silicon detector are the supermodule signal-to-noise ratio (S/N), the functioning of data sparsification, and the ability to run in deadtime-less operation. All supermodules were fully tested and excellent electrical performance was achieved.

A compilation of the noise and pedestals of the five supermodules installed in the barrel is shown in Figs. 23 and 24.

The average noise is 2 ADC counts which corresponds to an ENC of ≈ 1000 electrons. The typical S/N is ≈ 24. The noise distribution shows a little shoulder at ≈ 1.5 ADC counts. This structure is mostly due to the small number of stereo sensor strips which have a reduced strip length and are correspondingly less noisy. Also shown in Fig. 23 is the differential noise (dnoise). Differential noise is the standard deviation of the difference between the instantaneous pedestals of two adjacent channels divided by $\sqrt{2}$. A comprehensive discussion of the differential noise is given in Ref. [56]. In the absence of coherent noise effects, e.g. high or low frequency effects common to several channels, differential noise and noise are similar. The figure shows that this is the case, with mean noise being only $\approx 4\%$ larger than mean differential noise.

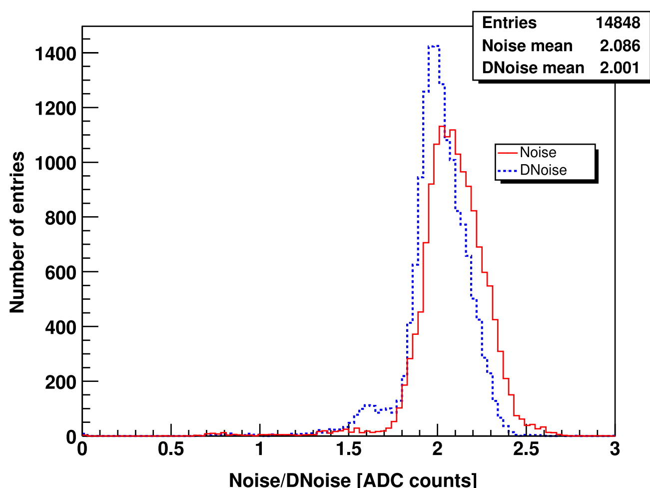

Fig. 23. Noise and differential noise distribution of the five supermodules installed in the barrel.

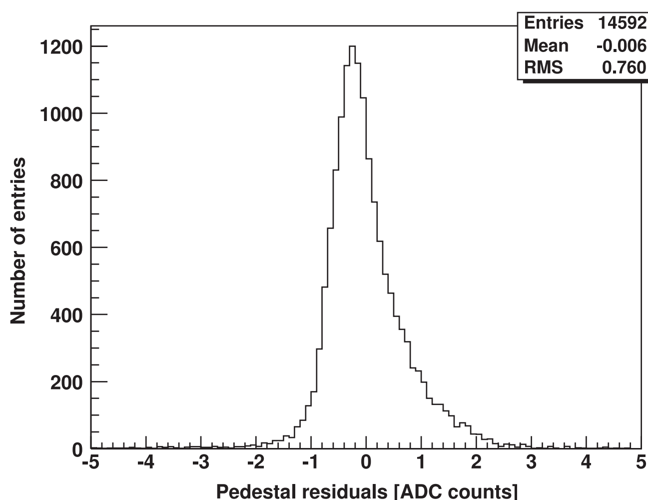

Fig. 24. Pedestal distribution of the same supermodules. The quantity plotted is $(\text{ped}(i) - \langle\text{ped}\rangle_i)$, where $\text{ped}(i)$ is the pedestal of channel i and $\langle\text{ped}\rangle_i$ is the mean pedestal of the corresponding chip.

Data sparsification is required in order to minimize the readout time, which will then depend on occupancy rather than the total number of channels. The SVX4 chip has an 8-bit adjustable sparsification threshold common to all channels. One requirement for proper functioning of data sparsification is pedestal uniformity across all channels of a given chip. In Fig. 24 the distribution of pedestals is shown. The pedestals are referred to the average pedestal of a given chip, since a possible variation of average pedestal can be compensated by a corresponding chip sparsification level. The distribution of normalized pedestals in this plot is narrow. Note that also the average chip pedestals differ by only a few ADC counts (not shown).

The performance in deadtime-less mode is illustrated in Fig. 25, where pedestals of different channels are shown for different modes of chip operation: acquire only; acquire while digitizing; and acquire while reading out. This sequence of chip modes is also representative of supermodule operation within the CDF experiment. A bucket corresponds to the time between colliding bunches, here assumed to be 120 ns,[5] and the clock frequency was set to 50 MHz. In each case the pedestal is quite flat and pedestals vary, with few exceptions, within 2 or 3 times the strip noise. This performance is excellent and entirely satisfactory for operation of supermodules in the experiment. This performance is even achieved without using the real-time pedestal subtraction (RTPS) feature of the SVX4 chip.

[5] The Tevatron Run II bunch crossing is 396 ns. The nominal Run IIb bunch crossing was first assumed to be 132 ns, but then revised to 396 ns.

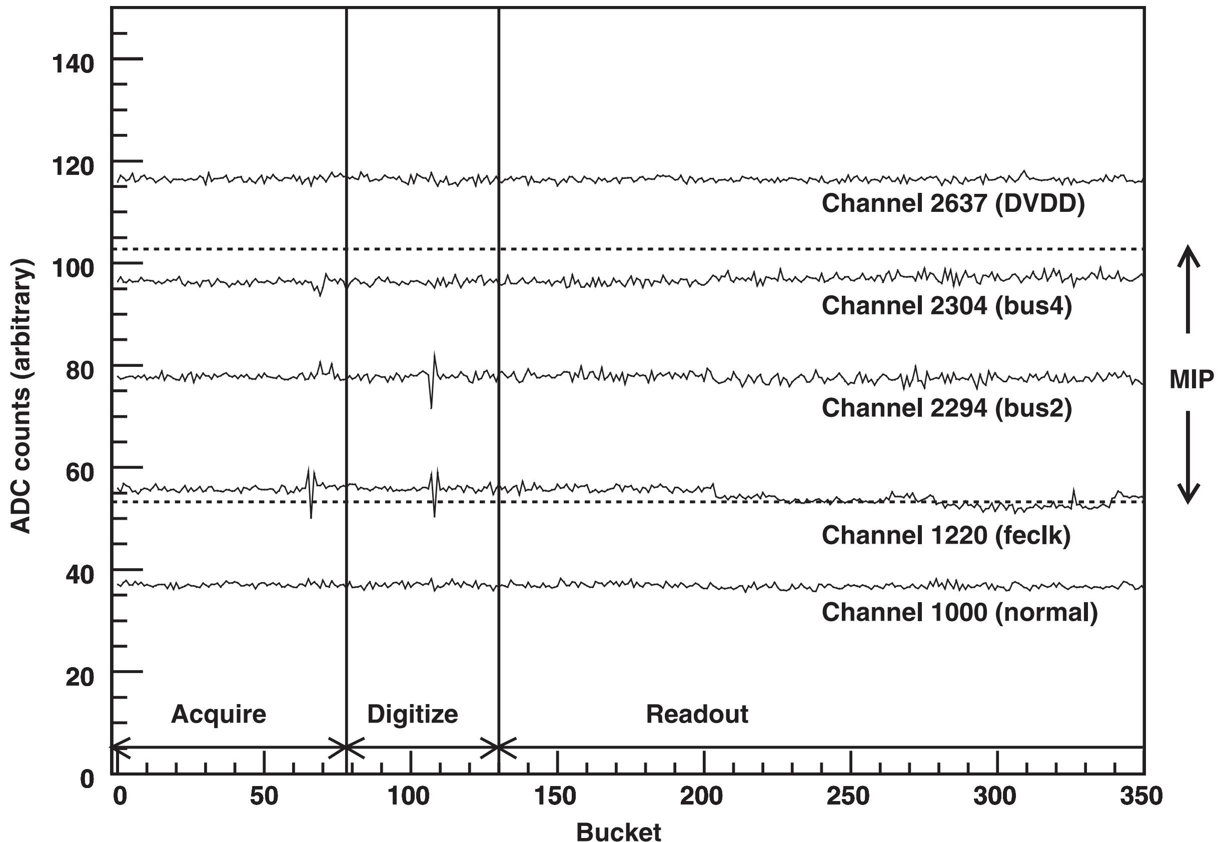

Fig. 25. Pedestal distribution as a function of time (bucket) and different modes of chip operation (see text). The curves show different channels which correspond to strips located above the digital power traces (DVDD), above different data bus traces (bus2 and bus4), and above the front-end clock trace (feclock). A strip that does not run above a bus cable trace (normal) is shown as well. The vertical position of the curves is arbitrary. The signal of a minimum ionizing particle corresponds to ≈ 50 ADC counts.

In Fig. 26 all channels are displayed for an arbitrary bucket. The bus cable traces running below the strips are indicated in the figure as well. The curve labeled "thin shield" shows a distinct pick-up structure above the front-end clock trace. The structure is present in every bucket (not shown). A detailed explanation of the interference effects causing the structure is given in Ref. [57], together with simulations and comparison to measurement. The effect is present if the magnetic fields, associated with the front-end clock signal, are not sufficiently suppressed by the aluminum shield. The time-dependent magnetic fields induce an electromagnetic force (emf) in the loops formed by pairs of strips, and their interconnections through the preamplifier and interstrip capacitance. This emf in turn leads to a net charge integration in the preamplifier.

No such effect is seen for any of the stereo sensor modules where the strips are tilted by 1.2° or for the modules at the end of the supermodule that are not located on bus cable traces other than the high voltage lines. For the sensors with stereo strips, the magnetic flux induced by the clock signal is distributed over a substantially larger number of strips, and a strong suppression of the interference signal seen in individual strips is expected. The easiest and safest way to remove all clock interference effect was by increasing the shield thickness to $50\,\mu$m (see the bottom curve of Fig. 26). The penalty in material increase is acceptable. With the final design, using a $50\,\mu$m shield, the electrical performance of the supermodules is excellent. An alternative would have been to tilt the bus cable traces with respect to the strip orientation (rather than tilting the strips as is the case for the stereo sensors). This idea is implemented in the middle section of the bus cable layout shown in Fig. 19.

11. Conclusions

In order to cope with the increased radiation levels of the Tevatron's Run IIb, the CDF collaboration designed a new silicon tracking detector. The detector is optimized to operate reliably in a high radiation and high luminosity environment and to ensure maximum sensitivity for Higgs boson and new particle searches.

Due to the much reduced Tevatron luminosity projections and funding difficulties, the project was canceled after reaching the preproduction stage.

In the design of the Run IIb detector, great care was taken to minimize risk, and involved R&D activities. Novel but simple design solutions, which emphasize robustness and ease of production, were found. These include an unconventional layer arrangement and the introduction of

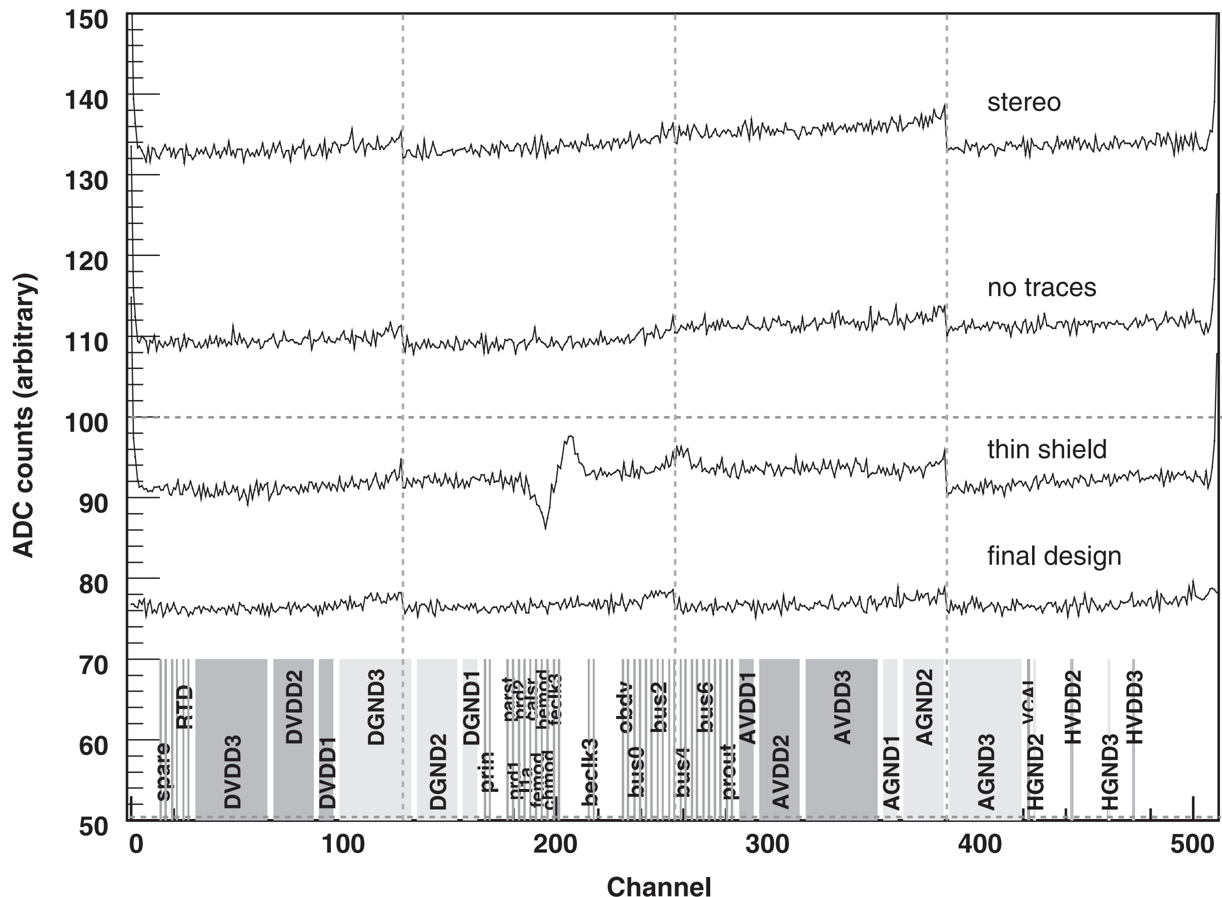

Fig. 26. Pedestal distribution for different channels for a fixed bucket. The curves show the channels of different supermodules. The dashed vertical lines separate different chips. The vertical lines and shaded areas at the bottom of the plot indicate the bus cable traces which run below the respective strips. The wide traces (DVDD, DGND, AVDD, AGND) are power traces. Most of the narrow traces are clock, control, and data. The top curve corresponds to a module with 1.2° stereo strips (stereo). The next curve (no traces) shows an axial module at the end of the supermodule. At this position there are only the high voltage bus cable traces. The third curve (thin shield) shows an axial module near the mini-port card. The aluminum shield of this and the above supermodules is 25 μm thick. The bottom curve shows an axial module at the same position for a 50 μm thick aluminum shield (final design). Again the vertical position of the curves is arbitrary and a MIP signal corresponds to ≈ 50 ADC counts.

a long, compact, low-mass "supermodule", which is used for all but the innermost detector layer. The SVX4 chip, a radiation-hard readout chip in 0.25 μm CMOS technology, was successfully designed and tested in only two years time. Also the development of all other detector components—silicon sensors, hybrids, mini-port cards—was successful. The preproduction experience shows that complex, large silicon detector systems can be built on a short time scale if construction and assembly issues are emphasized early in the design process.

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