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M. Bash

R. R. Chan

J. Crider

C. Harianto

J. Lian

See next page for additional authors

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A Medium Voltage DC Testbed for Ship Power System Research

M. Bash, R. R. Chan, J. Crider, C. Harianto, J. Lian, J. Neely, S. D. Pekarek,
S. D. Sudhoff and N. Vaks
School of Electrical and Computer Engineering
Purdue University, West Lafayette, IN 47907-2035, USA

***Abstract*— Medium voltage dc distribution systems are currently of interest for future naval warships. In order to provide hardware validation for research associated with the development of these systems, a low power Medium Voltage DC Testbed (MVDCT) is being constructed. This paper documents the system being constructed and provides some initial test results.**

I. Introduction

Medium voltage dc power distribution systems are being considered for future naval warships. As with any power distribution architecture, there are numerous design considerations which need to be addressed. In the case of medium voltage dc systems, of these considerations of particular interest include the effective paralleling of dc sources, stability in the presence of numerous constant power loads, and fault-protection.

In order to provide hardware validation of research results relevant to these issues, a Medium Voltage DC Testbed (MVDCT) is being constructed. The goal for this testbed is to provide a fully and publically documented system which can be used by the entire research community. This paper will provide an overview of the MVDCT, as well as initial control algorithms and parameters. Subsequent publications will provide finalized design and parameter values.

A one-line diagram of the MVDCT is depicted in Fig. 1. The system includes two generation systems (GS-1 and GS-2), a ship propulsion system (SPS), a pulsed power load (PPL), as well as lower-power zonal dc distribution system.

The dc voltage on the scaled medium voltage busses are denoted v_{mvx} where "x" is the bus number. Port and starboard zonal bus voltages are denoted v_{pty} and v_{sby}, respectively, where "y" is the zone number.

Generation system GS-1 includes a 59 kW wound rotor synchronous machine designated SG-1 connected to a passive rectifier R-1. Voltage regulator VR-1 adjusts the field so as to regulate the output voltage. Generation system GS-2 is based on an 11 kW permanent magnet synchronous machine denoted SG-2, which is connected to the system via an inverter. The voltage regulator VR-2 controls the inverter so as to regulate the output voltage. Both VR-1 and VR-2 have provisions for load sharing. The nominal output voltage of GS-1 and GS-2 is 750 V. Both generators are driven by four-quadrant dynamometers which will emulate prime movers. These are labeled PM-1 and PM-2 in Fig. 1.

The ship propulsion system SPS-1 in Fig. 1 is the dominant load at 37 kW peak power. The second largest load is the pulsed power load PPL, which emulates a rail gun system and draws a peak power of 18 kW.

The power supply PS-1 is utilized to step down the 750 V dc to 500 V dc and to distribute the power to the dc zonal systems via the port-side dc distribution bus. Power supply PS-2 provides power for the dc zonal systems via the starboard side dc distribution bus. It is intended to represent the effects of additional generation systems (which are physically not present) supporting the starboard distribution bus. PS-2 receives a three-phase 480 Vll-rms power from the utility grid. Using a line-commutated rectifier and the appropriate control, PS-2 converts the ac power into 500 V dc.

In the dc zonal system, six converter modules CM-1 through CM-6 are utilized to step the 500 V dc down to 420 V dc. These converter modules also provide protection to the port and starboard side distribution bus in the case of zonal faults. Note that in Fig. 1, there are two CMs in each zone. The two CMs operate in parallel to provide power to the inverter module (InM). In the case of a fault to one of the converter module or the distribution bus, the other converter module is able to pick up the load and continue services to the inverter module (InM)-load bank (LB) system. The InMs are utilized to convert the 420 V dc into a three-phase 230 Vll-rms ac, which is the form required by the 5 kW load banks (LB). The mathematical model for the InMs are set forth in [1], while the models, controls, and parameters for PS-2 and the CMs are set forth in [2].

II. Generation System GS-1

The majority of the power supplied to the MVDCT originates from generation source GS-1, which is depicted in Fig. 2. For the moment, the prime mover PM-1 is a dynamometer which regulates the speed of generator SM-1 to 1800 RPM [3]. However, the dynamometer will eventually emulate a gas turbine or some other prime mover.

The generator itself is a wound rotor synchronous machine with a brushless excitation system. The mathematical model and parameters of this machine and its brushless excitation system are set forth in [4]-[5].

The output of GS-1 includes rectifier R-1 which consists of an uncontrolled rectifier and a passive filter. The parameters for the passive elements are listed in Table I. Although uncontrolled rectifier is currently used, it is envisioned that a thyristor based rectifier will be utilized for future work, primarily for fault mitigation.

In this system, the desired dc voltage is approximately 750 V. The one line diagram for the control is depicted in Fig. 3. Therein, v^{**}_{mv1} denotes the reference (or commanded) dc voltage, $\hat{v}_{mv1}$ denotes the filtered dc bus voltage, and $\hat{i}_l$

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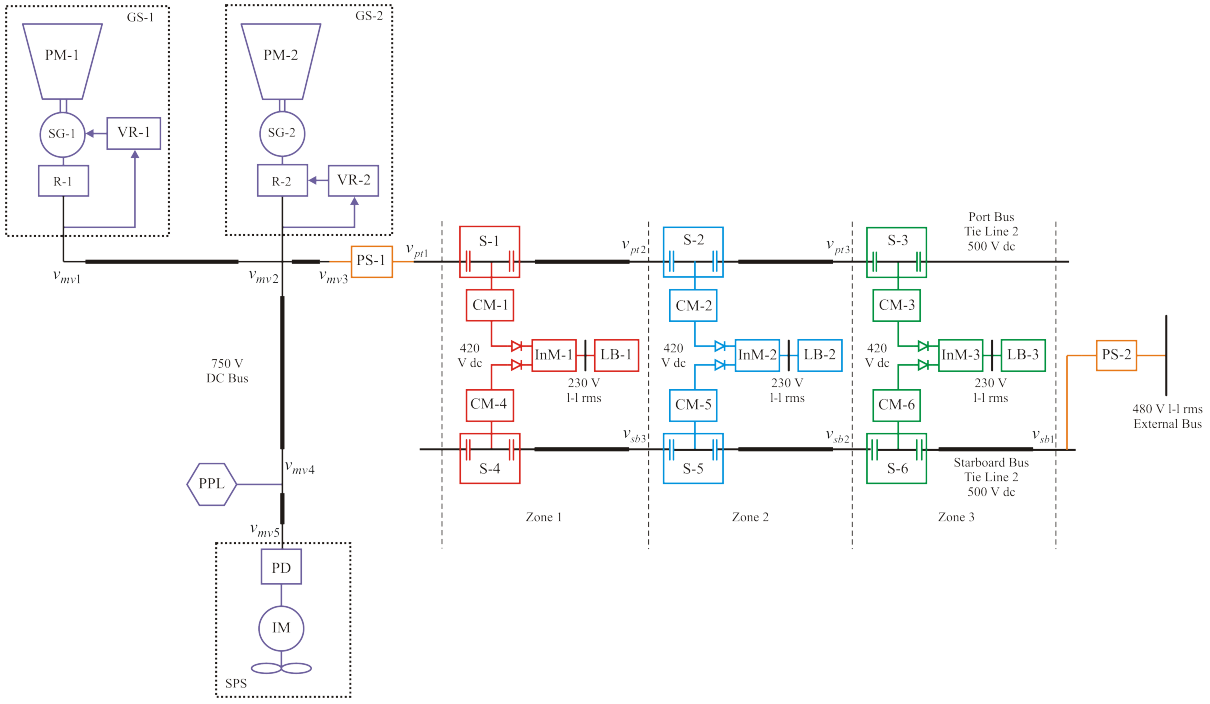

Fig. 1. Medium Voltage DC Testbed (MVDCT).

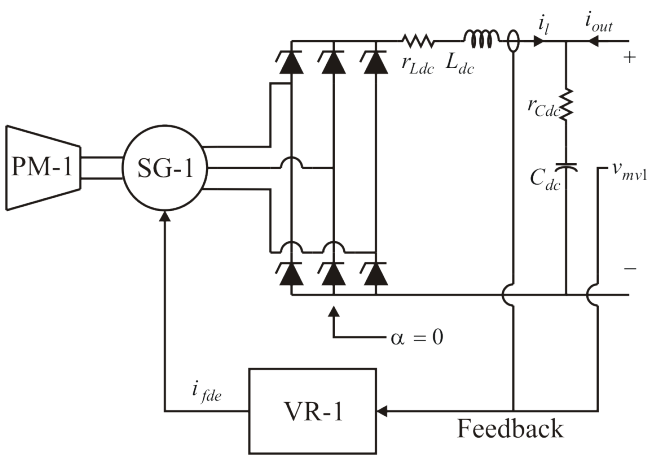

Fig. 2. Generation System GS-1.

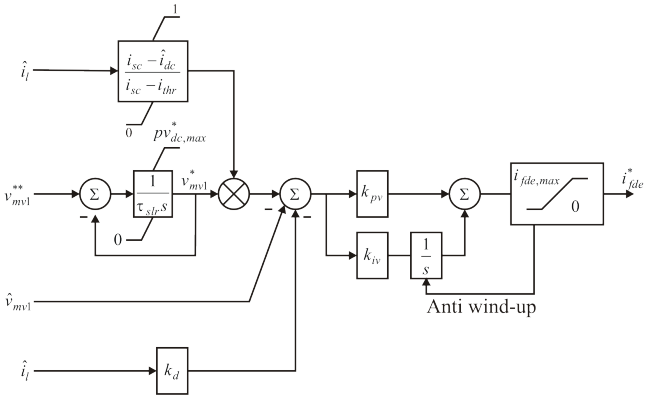

Fig. 3. GS-1 Control Block Diagram.

TABLE I
GS-1 PASSIVE COMPONENT PARAMETERS

Parameter	Value	Description
L_{dc}	7.5 mH	DC link inductor inductance
r_{Ldc}	0.075 Ω	DC link inductor resistance
C_{dc}	1.4 mF	DC link capacitor capacitance
r_{Cdc}	0.075 Ω	DC link capacitor series resistance

denotes the filtered inductor current. Both filters are of the first-order low-pass variety and have time constants τ_{fv} for the voltage and τ_{fi} for the current. The reference dc voltage is slew-rate limited to prevent excessive capacitor inrush currents on startup.

Short circuit protection is also included by sharply reducing the voltage command when the current exceeds a threshold i_{thr}. The droop term, k_d, allows the two generators to share the load. Voltage regulation utilizes a PI control with anti wind-up. The proportional and integral gains of the PI control are denoted as k_{pv} and k_{iv} respectively. The output of the control is the commanded field current into the brushless exciter, i^*_{fde}, which is then used in the hardware-based hysteresis control to

TABLE II
GS-1 CONTROL PARAMETERS

Parameter	Value	Description
$i_{fde,max}$	3 A	Brushless exciter maximum field current
i_{sc}	92 A	Short circuit current protection
i_{thr}	84 A	Threshold current
τ_{slr}	0.1 s	Slew rate limit time constant
k_d	0.59 Ω	Droop term
k_{pv}	7.5 mA/V	Proportional gain
k_{iv}	10 mA/V-s	Integral gain
τ_{fv}	28.5 ms	Bus voltage filter time constant
τ_{fi}	28.5 ms	Inductor current filter time constant

TABLE III
GS-2 PARAMETERS

Parameter	Value	Description
r_s	0.45 Ω	Stator winding phase resistance
L_q	2.6 mH	Q-axis inductance
L_d	2.6 mH	D-axis inductance
λ'_m	0.1723 V-s	Magnetic flux linkage
n_p	8	Number of poles
r_{Cdc}	20 mΩ	Output capacitor series resistance
C_{dc}	4 mF	Output capacitance
r_{Ldc}	20 mΩ	Output inductor series resistance
L_{dc}	0.3 mH	Output inductance

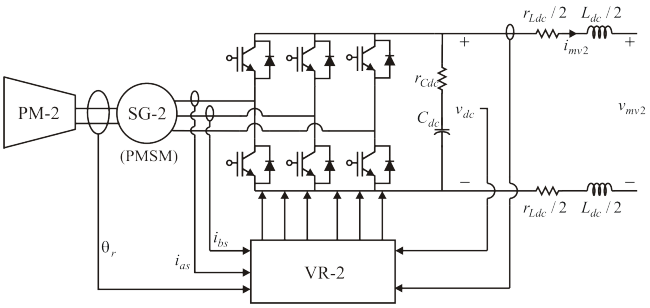

Fig. 4. GS-2 Topology.

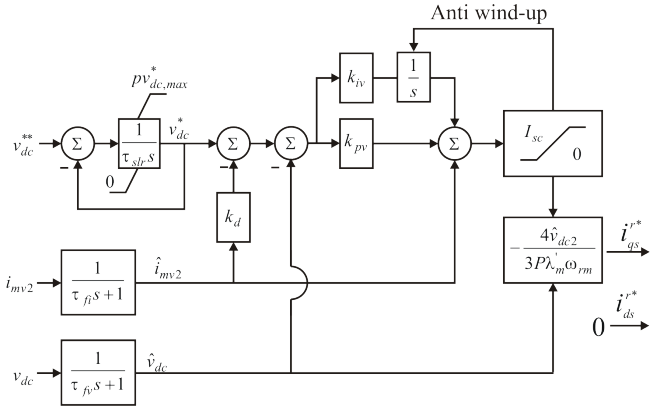

Fig. 5. GS-2 Voltage Controller.

obtain the desired brushless exciter field current. The control parameters are listed in Table II.

III. GENERATION SYSTEM GS-2

In Fig. 4, generation source GS-2 is depicted, which consists of a four-quadrant dynamometer acting as a prime mover (PM-2), a permanent magnet synchronous machine operating as a generator (SG-2), a three-phase bridge inverter serving as a rectifier (R-2), and a filter. This generation source is rated for 11 kW at 3600 rpm. As in the case of generation source GS-1, at this point in time the dynamometer simply attempts to regulate the speed, in this case at 3600 rpm. In the future, the dynamometer may be programmed to emulate a turbine or other prime mover. The three phase bridge inverter is current controlled and performs the ac-dc conversion. The filter prevents high-frequency current harmonics from entering the distribution system. The model of the PMSM is as set forth in [6]. Parameter values of the machine and passive filter elements are listed in Table III.

The voltage regulator consists of two parts, a voltage control and current control. The voltage control diagram is depicted in Fig. 5. In this diagram, v^{**}_{dc} denotes the commanded dc voltage, v_{dc} denotes the dc bus voltage, i_{mv2} denotes the inductor current, and $\hat{v}_{dc}$ and $\hat{i}_{mv2}$ denote the low-pass filtered values of v_{dc} and i_{mv2}, respectively.

The commanded dc voltage is slew-rate limited to prevent over currents due to capacitive inrush on startup. The voltage control consists of a PI control with anti wind-up. The output of the voltage controller is the commanded qd-axis phase currents referred to the rotor reference frame, $\mathbf{i}^{r*}_{qds}$, which will be used in the current controller. The voltage controller also includes a droop term to facilitate power sharing with GS-1.

The current controller diagram is depicted in Fig. 6. In this diagram, $\mathbf{i}_{abs}$ denotes the phase currents of the generator, $\mathbf{K}^r_i$ denotes the current transformation from $\mathbf{i}_{abs}$ to $\mathbf{i}^r_{qds}$, and $\mathbf{K}^r_s$ denotes the transformation from machine variables to the rotor reference frame [6]. In particular,

$$\mathbf{K}^r_i = \sqrt{3}\begin{bmatrix} \cos\left(\theta_r - \frac{\pi}{6}\right) & \sin\theta_r \\ \sin\left(\theta_r - \frac{\pi}{6}\right) & -\cos\theta_r \end{bmatrix} \tag{1}$$

and

$$\mathbf{K}^r_s = \frac{2}{3}\begin{bmatrix} \cos\theta_r & \cos\left(\theta_r - \frac{2\pi}{3}\right) & \cos\left(\theta_r + \frac{2\pi}{3}\right) \\ \sin\theta_r & \sin\left(\theta_r - \frac{2\pi}{3}\right) & \sin\left(\theta_r + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2}$$

The output of the current controller is the commanded phase currents for the generator, $\mathbf{i}^*_{abcs}$, which is then used in the hysteresis control of the current modulated inverter to obtain the appropriate switching signals. Parameter values are listed in Table IV.

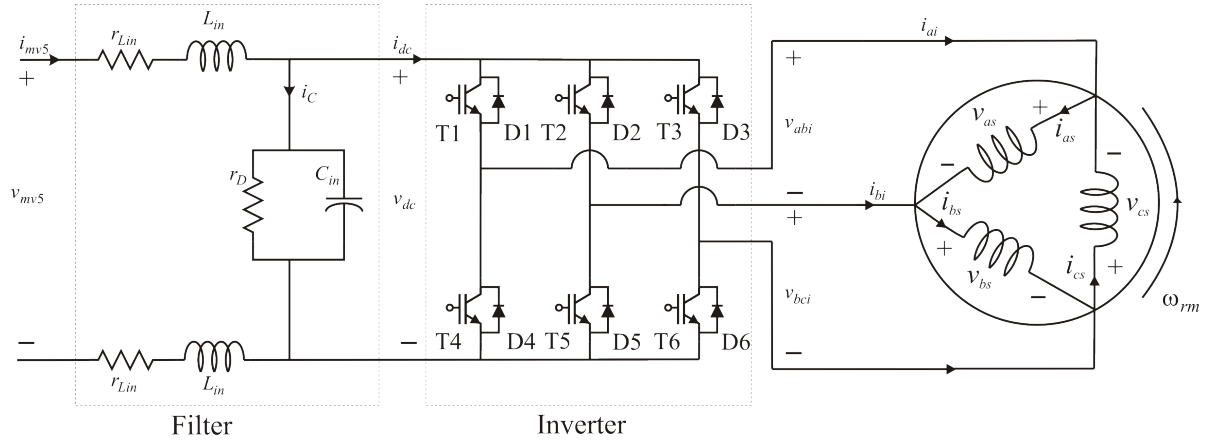

Fig. 7. SPS Topology.

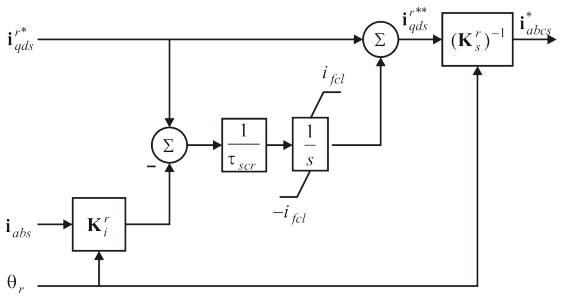

Fig. 6. GS-2 Current Control.

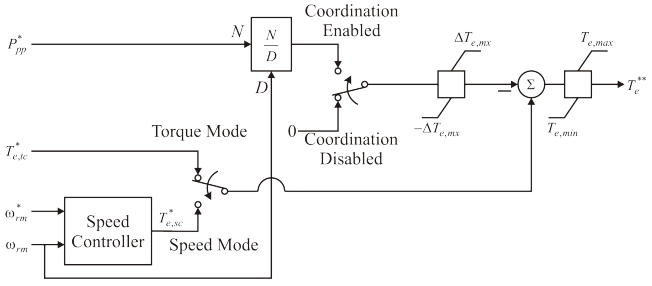

Fig. 8. SPS Control.

TABLE IV
GS-2 VOLTAGE REGULATOR PARAMETERS

Parameter	Value	Description
τ_{fv}	4.421 ms	Bus voltage filter time constant
τ_{fi}	4.421 ms	Inductor current filter time constant
τ_{slr}	0.1 s	Slew-rat limiter time constant
$pv^*_{dc,max}$	7500 A/V	Maximal ramp up rate
k_d	3.5 Ω	Droop term
k_{pv}	0.3 A/V	Proportional gain
k_{iv}	7.58 A/V-s	Integral gain
I_{sc}	15.71 A	Short circuit protection current
τ_{scr}	1.59 mA	Current regulator time constant
i_{fcl}	0.25 A	Integral feedback current limit
h	0.125 A	Hysteresis level of modulator

IV. SHIP PROPULSION SYSTEM (SPS)

The ship propulsion system (SPS) consists of the propulsion drive (PD) and an induction machine (IM) connected to a dynamometer which can be used to emulate hydrodynamics.

The one-line diagram of the SPS is depicted in Fig. 7. It consists of a filter and an inverter. The filter is designed to reduce the high frequency voltage ripple at the input terminals to the inverter and to prevent high frequency switching ripple from propagating into the distribution system. The values of the components of the filter are chosen such that the cut-off frequency of the filter is at 1 kHz.

Variables in Fig. 7 include the input voltage and current, denoted as v_{mv5} and i_{mv5}, respectively, the capacitor current i_c, the inverter input voltage and current, denoted as v_{dc} and i_{dc}, respectively, and the a-phase and b-phase inverter current, i_{ai} and i_{bi}.

The propulsion drive is connected to 4-pole delta-connected squirrel cage induction machine rated at 37 kW, 460 Vll-rms, and 60 Hz. The machine model and parameters are set forth in [7]. The control diagrams of the SPS is depicted in Figs. 8-9. Therein, two primary control modes are considered, namely the torque mode and the speed mode. In the torque mode, the desired torque $T^*_{e,tc}$ is specified directly.

In speed mode, a torque command $T^*_{e,sc}$ is computed based on a speed command ω^*_{rm} and the measured speed ω_{rm} . The speed control consists of a PI control with anti-windup protection as depicted in Fig. 9. The output of the speed control is the torque command $T^*_{e,sc}$.

The SPS control also coordinates with the pulsed power load (PPL) such that the net power demand of the SPS and the PPL is approximately constant when coordination is enabled. Such coordination can be achieved by considering P^*_{pp}, which denotes the instantaneous power flow into PPL. The torque command, $T^*_{e,tc}$ or $T^*_{e,sc}$, is adjusted so as to approximately reduce the power flow into the drive by P^*_{pp}. The maximum adjustment is limited to $\Delta T_{e,max}$. The final net

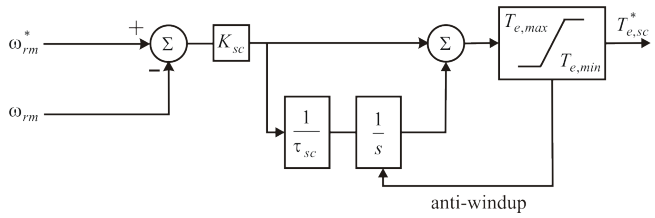

Fig. 9. SPS Speed Control.

TABLE V
SPS PARAMETERS

Parameter	Value	Description
L_{in}	0.113 mH	Input filter inductance
r_{Lin}	0.25 Ω	Input filter inductor resistance
C_{in}	1.4 mF	Input filter capacitance
r_D	40 kΩ	Capacitor drain resistance
K_{sc}	5 Nms/rad	Speed control gain
τ_{sc}	1 s	Speed controller time constant
$T_{e,min}$	0 Nm	Minimum allowed torque
$T_{e,max}$	250 Nm	Maximum allowed torque
$\Delta T_{e,mx}$	200 Nm	Maximum torque adjustment

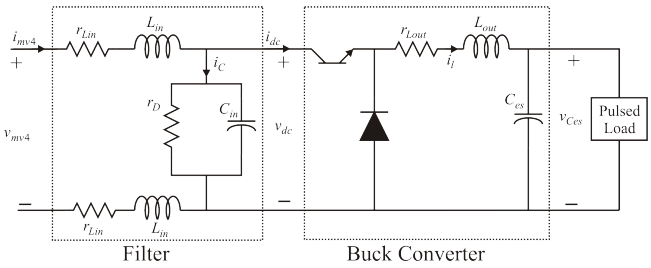

Fig. 10. PPL Topology.

TABLE VI
BUCK CIRCUIT AND INPUT FILTER PARAMETERS

Parameter	Value	Description
L_{in}	0.113 mH	Input filter inductance
r_{Lin}	0.25 Ω	Input filter inductor resistance
C_{in}	1.4 mF	Input filter capacitance
r_D	40 kΩ	Capacitor drain resistance
L_{out}	3 mH	Output inductance
r_{Lout}	0.1 Ω	Output inductor series resistance
C_{es}	0.2 F	Energy storage capacitance

torque command is T_e^{**}.

An adaptive maximum torque per amp control strategy set forth in [7]–[9] then utilizes the torque command T_e^{**} to determine the commanded inverter current in the synchronous reference frame $\mathbf{i}_{qdi}^{e*} = [i_{qi}^{e*} \;\; i_{di}^{e*}]^\top$ and the commanded slip frequency ω_s^*. This strategy minimizes the loss in both the inverter and the motor. The SPS parameters are listed in Table V.

As a protection feature, the input bus voltage is monitored. The drive will go off-line if the input voltage leaves the range 650-850 V.

V. PULSED POWER LOAD (PPL)

The MVDCT Pulsed Power Load (PPL) is designed to place a load on the MVDCT which is representative of a pulsed-power weapon such as a rail gun. The circuit topology of the PPL is depicted in Fig. 10. It has a peak power draw of approximately 18 kW. Fig. 10 depicts the charging circuit which includes a filter and a buck converter. The filter is designed to reduce the high frequency voltage ripple at the input to the buck converter. The buck converter regulates the current i_l so as to charge the energy storage capacitor C_{es} according to the desired profile. The passive component parameter values are listed in Table VI.

The controls for the PPL are depicted in Figs. 11-13. Therein, a supervisory control to formulate the charge/discharge command signals is depicted in Fig. 11. The inputs to the supervisory control include a commanded charging signal, e_c^*, a commanded discharging signal, e_d^*, the filtered energy storage capacitor voltage, $\hat{v}_{Ces}$, and the minimum capacitor voltage threshold at which discharging is allowed, v_{c2}^*. The outputs of this control are the logical charging status, e_c (logical 1 to charge) and the logical discharge status, e_d (logical 1 to discharge).

Provided that a discharge sequence is not underway, enabling e_c^* will enable the charge status e_c, whereupon the capacitor will be charged. If the capacitor voltage is greater than the threshold voltage and e_d^* is enabled, a discharge sequence is enabled. The charge-discharge supervisory control also considers a time delay between the charge and discharge cycles for protection.

The charge enable signal is used in the capacitor current control command synthesizer in Fig. 12. Therein, a capacitor current command i_c^* is computed as a function of the commanded capacitor voltage v_{c1}^*, a measured capacitor voltage v_{Ces}, and the charge signal e_c. A dynamic limit i_{climit} is introduced to limit the capacitor current command, where i_{climit} is formulated as a function of the peak capacitor current limit i_{cmax} and a peak power limit of P_{cmax}. In the PPL control, the capacitor voltage first-order low-pass filter time constant is τ_{inf}.

Note that K_{sf} is selected to be sufficiently large such that the capacitor current command is at its limit until the filtered

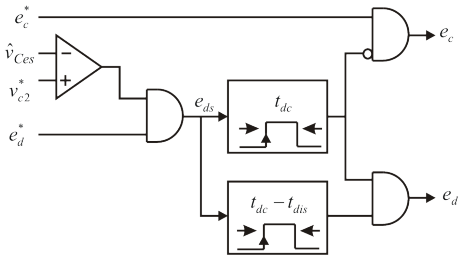

Fig. 11. PPL Charge/Discharge Supervisory Control.

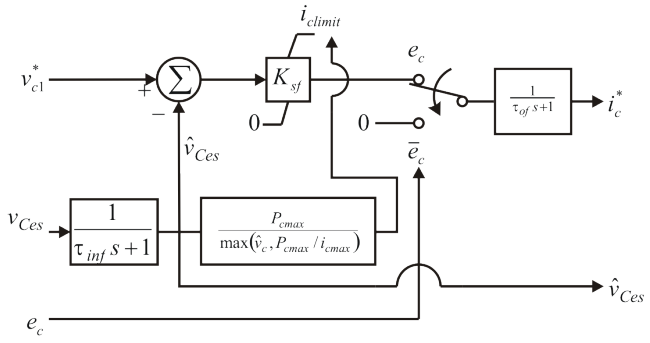

Fig. 12. PPL Capacitor Current Control Command Synthesizer.

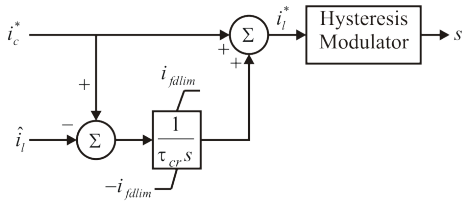

Fig. 13. PPL Buck Circuit Hysteresis Current Control.

component of the capacitor voltage $\hat{v}_{Ces}$ reaches v_{c1}^*. At this point, the capacitor voltage charging decreases asymptotically. For this reason, the target voltage v_{c1}^* is set slightly higher than the minimum voltage to discharge, v_{c2}^*.

The capacitor current command i_c^* is then utilized in the buck circuit hysteresis controller, depicted in Fig. 13, to formulate the inductor current command i_l^*. The hysteresis current control also considers the integral feed forward term of the error between the capacitor current command and the filtered component of the inductor current $\hat{i}_l$. The purpose of the integral term is to remove any tracking error in the hysteresis modulator. The output of the hysteresis control is the switching signal s to control the switching of the transistor in the buck circuit.

The last component of the pulsed power system is the energy storage capacitor. In an actual system, this would represent a physical capacitor. However, in the PPL, the majority of the energy storage capacitance is emulated to allow rapid charge and discharge without a true pulsed power event and to reduce space requirements. The specifications, component values, and the control strategy for the capacitor emulator circuit are defined in [9]. The control parameters are listed in Table VII.

VI. Power Supply PS-1

Power supply PS-1 interfaces the 750 V dc bus with the 500 V dc port bus. PS-1 has a physical rating of 25 kW but has parameters which are adjusted to reduce the ratings to appropriate values for the system (since all zonal loads sum to 15 kW).

In Fig. 14, the PS-1 topology is depicted. It consists of an input filter with inductor L_{in} and capacitor C_{in} with

TABLE VII
PPL Control Parameters

Parameter	Value	Description
v_{c1}^*	350 V	Target capacitor charging voltage
v_{c2}^*	345 V	Minimum capacitor firing voltage
P_{cmax}	10 kW	Maximum allowed power into storage capacitor
i_{cmax}	25 A	Maximum allowed current into storage capacitor
t_{dis}	0.2 ms	Time over which storage capacitor is discharged
t_{dc}	0.25 ms	Time of discharge cycle
τ_{inf}	0.79 ms	Input filter time constant
τ_{of}	5 ms	Output filter time constant
K_{sf}	13.35 A/V	Current forward gain
τ_{cr}	1 ms	Integral feedback time constant
i_{fdlim}	2.62 A	Integral feedback current limit
h	2.62 A	Hysteresis level of modulator

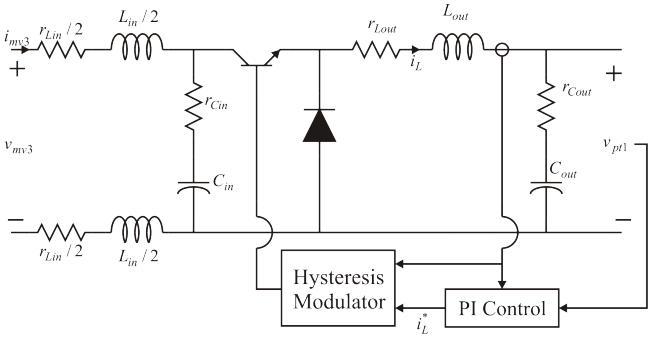

Fig. 14. PS-1 Circuit Topology.

parasitic resistances r_{Lin} and r_{Cin}, a buck converter with inductor L_{out} and a parasitic resistance of r_{Lout}, and finally a capacitive output filter with capacitance C_{out} and parasitic series resistance of r_{Cout}. Parameter values for the circuit are listed in Table VIII.

The PS-1 output voltage is regulated using a current-mode feedback control. A PI controller determines the commanded output inductor current from output voltage error. Measurement of the output voltage v_{pt1} is filtered using a low-pass filter with time constant τ_{vpt1}, denoted as $\hat{v}_{pt1}$, and the voltage error is determined by comparing $\hat{v}_{pt1}$ with the commanded output voltage v_{pt1}^*. The commanded current is maintained by a delta-modulation hysteresis current controller that limits the switching frequency to 25 kHz. The output inductor current to capacitor voltage transfer function describes the open loop system to be controlled, and the proportional and integral gains of the PI control k_{pv} and k_{iv} are selected to place the closed-loop poles at -200. The PS-1 controller is illustrated in Fig. 15; the control parameters are listed in Table IX.

TABLE VIII
PS1 CIRCUIT PARAMETERS

Parameter	Value	Description
L_{in}	0.361 mH	Input filter inductance
r_{Lin}	138 mΩ	Input inductor series resistance
C_{in}	1.8 mF	Input filter capacitance
r_{Cin}	60 mΩ	Input capacitor series resistance
L_{out}	1.99 mH	Output inductance
r_{Lout}	26 mΩ	Output inductor series resistance
C_{out}	1.8 mF	Output capacitance
r_{Cout}	60 mΩ	Output capacitor series resistance

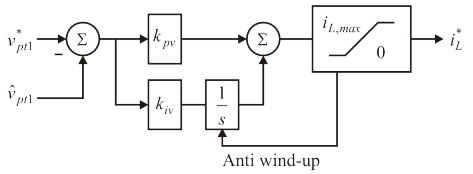

Fig. 15. PS-1 Voltage Control.

VII. PRELIMINARY TEST RESULTS

In this section, some preliminary test results will be provided. At the time this paper is written, GS-1, SPS, and PPL are operational. The first study demonstrates the performance of GS-1 and SPS at full load in steady-state. The SPS control is configured in a torque mode with the commanded torque $T^*_{e,tc} = 200$ Nm and $\omega_{rm} = 1800$ rpm. The waveforms associated with GS-1 are depicted in Fig. 16. Therein, v_{mv1} is the voltage at medium voltage dc bus 1, i_a denotes the GS-1 a-phase current, i_l denotes the GS-1 inductor current, and i_{out} denotes the GS-1 output current, which is negative due to the sign convention used in Fig. 2. The waveforms for the SPS are depicted in Fig. 17. Therein, v_{mv5} denotes the input voltage to the SPS, v_{dc} denotes the filtered dc voltage, v_{abi} denotes the line-to-line ac voltage out of the inverter, and i_{ai} denotes the a-phase stator current into the induction machine.

A transient study involving the charging and discharging of the PPL is depicted in Fig. 18. In this study, the output voltage of GS-1 has reached steady-state at 750 V dc before the PPL is enabled. The SPS is off-line. In Fig. 18, v_{Ces} denotes the PPL capacitor voltage, v_{mv4} denotes the PPL input dc voltage, i_{mv4} denotes the input dc current, and i_a denotes the a-phase current of GS-1. From these results, it can be observed that the capacitor voltage of PPL is charged to approximately 350 V before it was discharged. During the discharge, the dc bus voltage v_{mv4} was slightly perturbed.

TABLE IX
PS1 CONTROL PARAMETERS

Parameter	Value	Description
k_{pv}	0.744 A/V	Proportional gain
k_{iv}	75.20 A/V-s	Integral gain
τ_{vout}	0.15915 ms	Voltage filter time constant
$i_{L,max}$	55 A	Maximum inductor current
v^*_{pt1}	500 V	Commanded output voltage

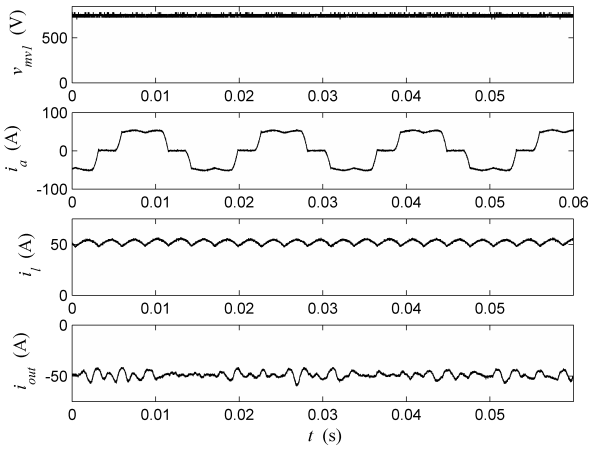

Fig. 16. GS-1 Steady-State Waveforms.

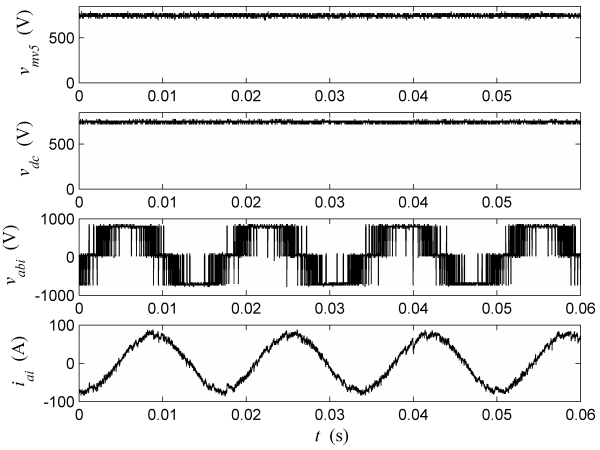

Fig. 17. SPS Steady-State Waveforms.

VIII. CONCLUSION

In this paper, the medium voltage dc (MVDC) testbed is described. The diagrams of each component as well as the associated controls are documented. Preliminary experiment results have shows the behavior of the system during steady state and transient conditions. Future work will include control and parameter refinements and comprehensive system studies.

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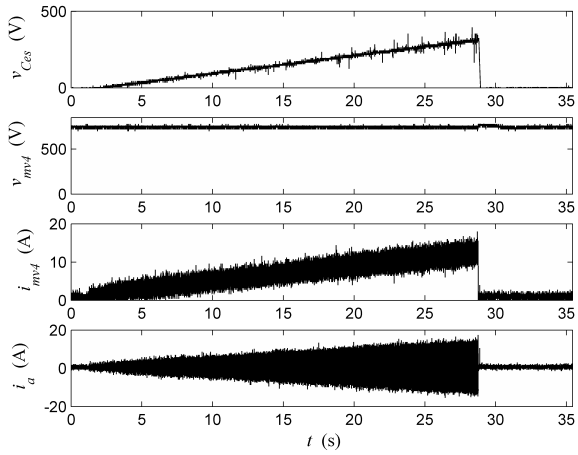

Fig. 18. PPL Transient Waveforms.

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