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15.4 A Digital Driving Technique for an 8b QVGA AMOLED Display Using ΔΣ Modulation

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Active-matrix organic LED (AMOLED) is one of the most promising contenders for next-generation displays. However, the V_T-shift issue in thin-film transistors (TFT) has to be addressed to enable wide deployment [1]. Voltage programming and current programming are well-known V_T-shift-compensation techniques for analog driving. However, they all need more than 4 TFTs per pixel, which increases the panel complexity and decreases yield and aperture ratio. Recently, a V_T-shift compensation technique that uses a 2TFT-1C pixel in an analog driving AMOLED has been reported [2]. However, it requires OLED supply voltage programming, and shows a 14% variation in OLED current after V_T-shift compensation, which is not enough for high-definition applications. Digital driving has been proposed as an alternative to mitigate the V_T-shift issue with a simple pixel structure and to provide flexibility to the driver design. Figure 15.4.1 shows the pixel structures for voltage programming, current programming and digital driving. While the gate of the driving TFT (M2) is in the high state, the voltage across M2 is very small due to the large current-driving capability of a TFT as compared with an OLED. Hence, the current through the OLED is dominated by the supply voltage (PVDD), and minimally affected by the variations in TFT characteristics [3]. Digital driving is also useful for true dark-level expression since the OLED can be completely turned off for black gray levels.

Previous digital driving techniques for AMOLEDs have been focused on PWM due to the compatibility with the traditional frame-based refreshing method. However, PWM suffers from a false-image-contour problem caused by an incompatibility with the human visual system. Several approaches have been proposed to alleviate the issue [4], but all of them cause increased system complexity or grey-level reduction. We propose a non-frame-refreshing digital-driving technique based on pulse-density modulation (PDM) using a ΔΣ modulator that effectively suppresses false image contours without increasing the system complexity, while providing the same or better resolution and relaxed gate-scan time as compared with PWM.

Figure 15.4.2 shows example pulse waveforms of PWM and PDM signals with their integrated values that are actually perceived by the human visual system, and the simulated ramp outputs. A 2nd-order LPF model is used for the human visual system [5]. Due to the clear frame boundary of PWM, the human visual system can perceive incorrect integrated values causing a false image contour when the relative location between the human visual system and the display is not stationary. In the PWM ramp output graph, gray-level transition points responsible for the false image contour are marked with dashed lines. Since the current output is affected by the previous values in the ΔΣ modulator, the PDM waves do not have a clear frame boundary. The non-refreshing characteristic makes it free from the false-contour problem, and the simulated PDM ramp output in Fig. 15.4.2 shows no distortion, demonstrating its effectiveness in suppressing false image contours.

Figure 15.4.3 shows the block diagram of the implemented system. The 24b RGB video signals are converted to transition-minimized differential signals and fed into an FPGA that implements the proposed digital driver using ΔΣ modulation. X(Z) is an 8b input, E(Z) is quantization noise, and Y(Z) is the PDM 1b output stream. Its RTL implementation consists of one 8b adder and one frame buffer for each RGB input. The output PDM waves are fed to four source drivers that drive the data lines of the OLED panel. Each source driver is composed of a 64b shift register that drives 240×3 (RGB) data lines. Scan lines are driven by an integrated scan driver with 4-phase clocks. The tested range of the operating frequencies in the FPGA is from 32 to 80MHz, whose corresponding oversampling ratios (OSRs) range from 7 to 17. The PDM signal fed to the panel is then lowpass-filtered by the human visual system [5]. A 1st-order ΔΣ modulator is used because the human visual system is closely related to a 2nd-order LPF.

Figure 15.4.4 shows the simulated resolutions and gate scan times in the face of different OSR values. The resolutions are estimated by measuring the peak output SNRs with triangle-wave inputs. The gate scan time is the time period allowed for charging and discharging each scan line for the minimum-length sub-field, and calculated for the (320×240×RGB) QVGA panel with 2-TFT-1-Cap pixels. As shown in Fig. 15.4.4, PDM easily achieves more than 8b resolution because of its oversampling and noise-shaping properties. More importantly, its minimum gate scan time is much longer than that of PWM, which makes it a promising candidate for high-definition applications.

A digital driver needs to charge and discharge each pixel more frequently than an analog one, and requires higher power consumption for panel driving. On the other hand, the proposed digital driver only needs a simple SRAM buffer, three 8b adders, and shift registers, while analog driving requires additional complex DAC array and buffer amplifiers that consume considerable power. An example QVGA AMOLED analog driver with a power consumption of 13.3mW is reported [6]. The proposed digital driver consumes 5 to 6mW of extra power for panel driving. The example shows the effectiveness of the proposed digital driving technique for low power design.

The idle tone issue is a typical drawback of a ΔΣ modulator. The PDM output from the ΔΣ modulator generates periodic tones when the input is held constant. If the idle tone magnitude outweighs the output margin, the human visual system can recognize the deviation from the ideal gray level, causing flicker for constant or stationary inputs. Figure 15.4.5 shows the simulated normalized idle-tone magnitude for 256 gray levels with OSR of 7 and 13. For the 8b resolution including idle tones, the normalized maximum idle tone magnitude has to be less than LSB/2 = $1/(2^8 \times 2)$. With an OSR of 7, the idle tones of some gray levels outweigh the margin, limiting the practical resolution. With an OSR of 13, the idle-tone amplitude is reduced below the margin, while having some DC offset, which can easily be removed by DC-offset cancellation.

Figure 15.4.6 shows a still image capture of the panel with the proposed PDM digital driver. The system is tested with a maximum operating frequency of 80MHz, where the OSR equals 17. No false image contour is observed. Figure 15.4.7 shows a die micrograph of the pixel array. The panel size is 2.2 inch with 320×240×RGB resolution.

A new PDM digital driving technique for AMOLED is reported that uses ΔΣ modulation and is applied to a 2.2-inch QVGA AMOLED panel with a 2TFT-1C pixel structure. The technique provides all advantages of digital driving techniques such as insensitivity to V_T-shift, programmable gamma correction, and an excellent dark level expression. In addition, PDM using ΔΣ modulation provides an effective solution for false image contour, and for high-resolution design without excessive limitations on the gate scan time, which is a significant advantage for high-definition display applications.

Acknowledgements:
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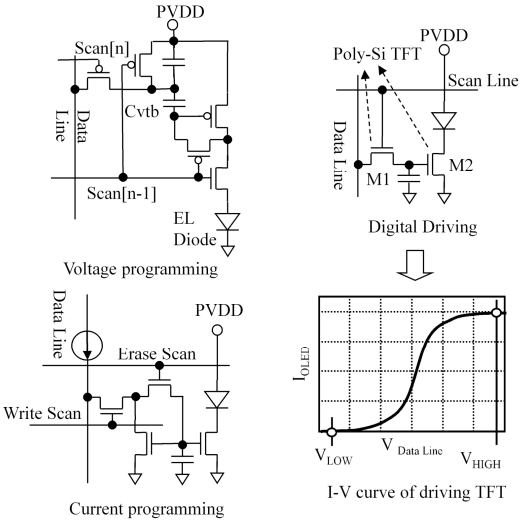

Figure 15.4.1: Panel structure schematics with different driving techniques. Digital driving needs a simple 2TFT-1C structure.

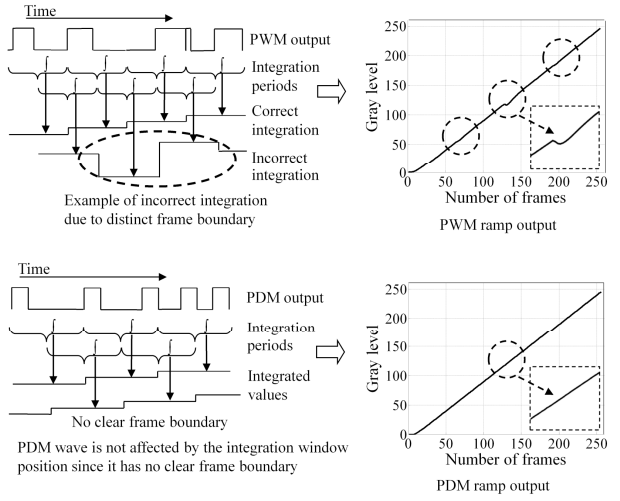

Figure 15.4.2: Comparison between the conventional PWM and the proposed ΔΣ modulation schemes. The simulated PWM ramp output shows distortion responsible for the false image contour.

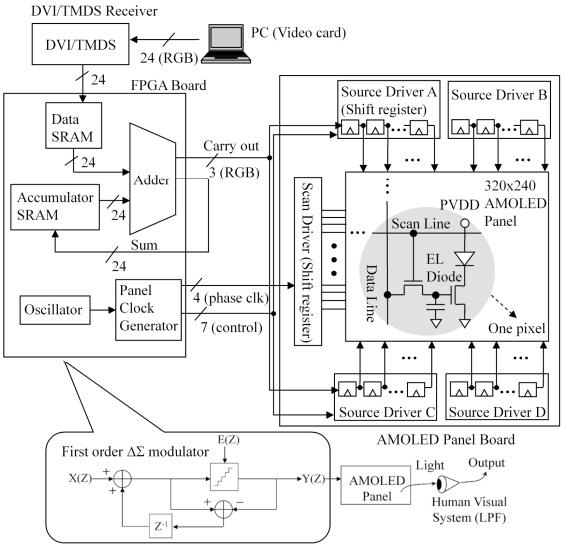

Figure 15.4.3: Block diagram of the implemented system.

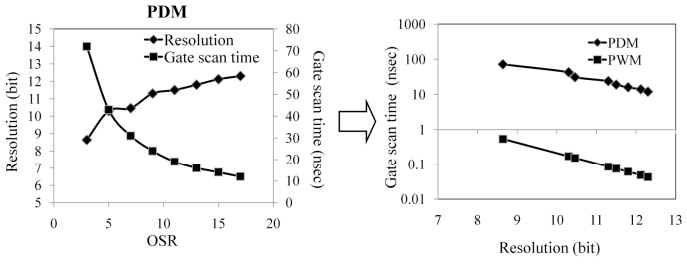

Figure 15.4.4: Resolution and gate scan time comparison graphs. PDM shows more relaxed gate scan time than PWM with the same resolutions.

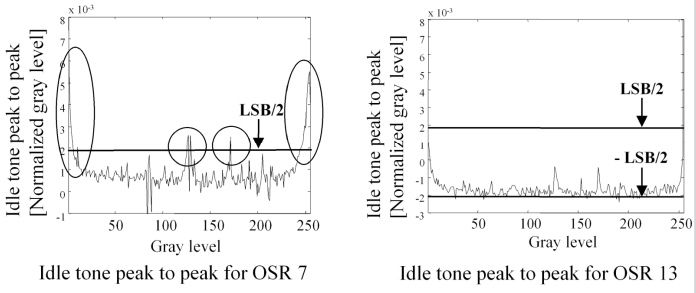

Figure 15.4.5: The maximum output level difference between the modulated value and the ideal value for OSR of 7 and 13. The output level difference is mainly caused by the idle tones.

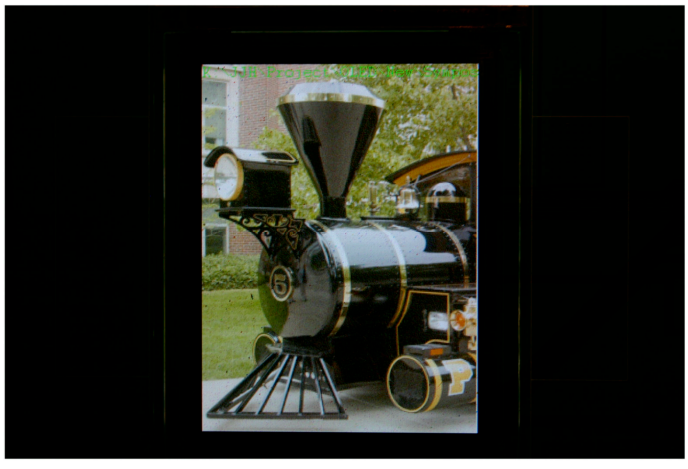

Figure 15.4.6: A still image capture where no false contour is observed.

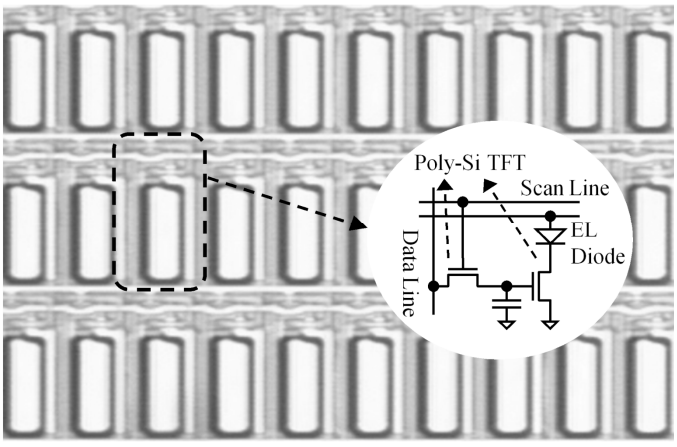

Figure 15.4.7: AMOLED pixel micrograph and schematic.

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