Process-level Power Estimation in Multi-core Architectures

Maxime Colmant, Romain Rouvoy, Lionel Seinturier

Process-level Power Estimation in Multi-core Architectures *

Maxime Colmant, Romain Rouvoy, Lionel Seinturier

* Published article: Colmant (M.), Kurpicz (M.), Huertas (L.), Rouvoy (R.), Felber (P.) et Sobe (A.). – Process-level Power Estimation in VM-based Systems. – In *European Conference on Computer Systems (EuroSys)*, Bordeaux, France, avril 2015

Motivation

Problem

- Hard to identify the largest power consumers
- Power meters are not fine-grained enough
- Limited number of processor-agnostic solutions
- Limited number of power-aware interfaces

Vision

- Software-defined power meters
- Support for all CPU features
- Provide critical indicators

Metrics

Hardware (HW) Performance Counters

- Representative and accurate metrics
- Mostly available on modern processors

Criteria selection

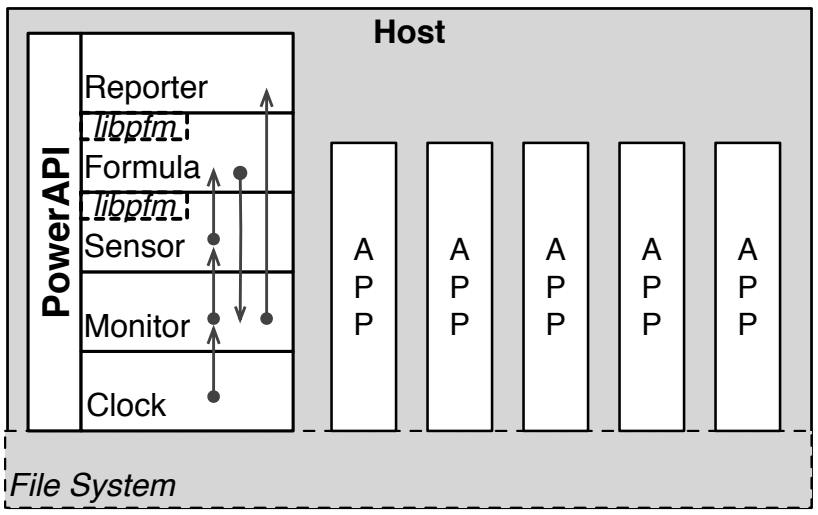
- Counter availability per CPU
- Monitoring overhead
- Best fit under several workloads

Selected HW Performance Counters

- CPU_CLK_UNHALTED:THREAD_P (*uc*)
- CPU_CLK_UNHALTED:REF_P

PowerAPI

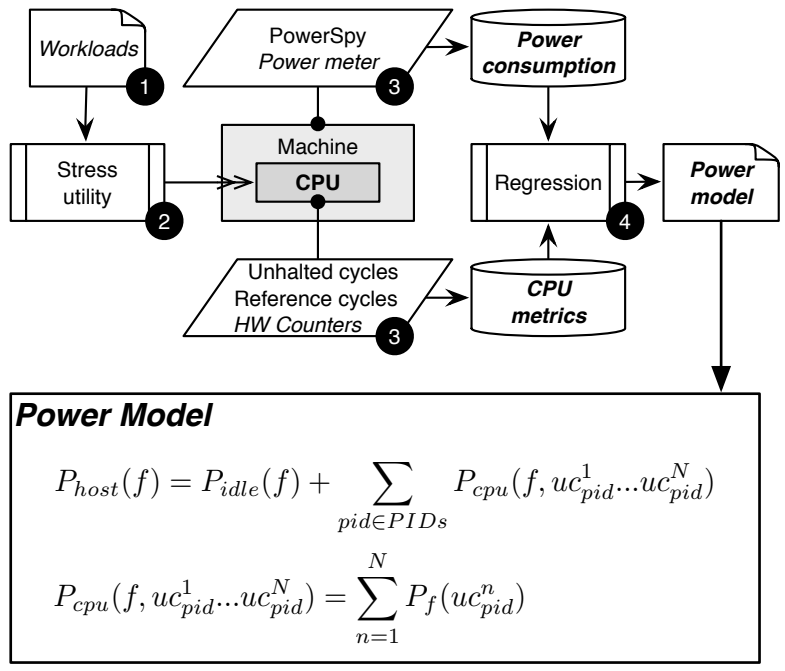
Implementation



PowerAPI

Available online:
http://powerapi.org

Learn the CPU power model

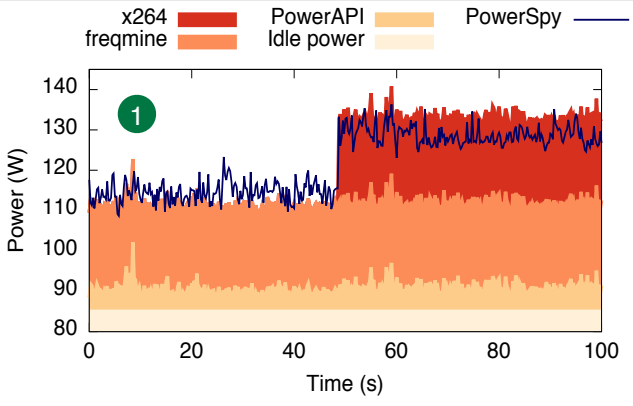


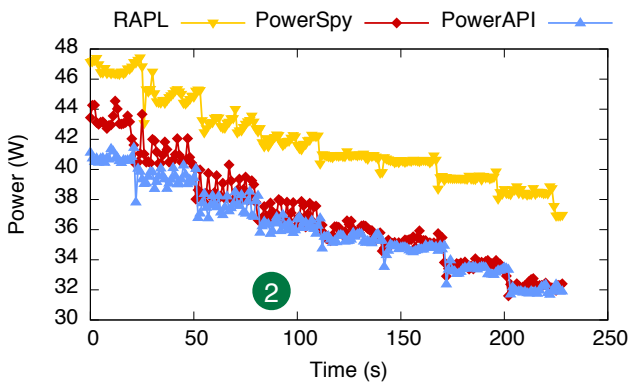
Power Model

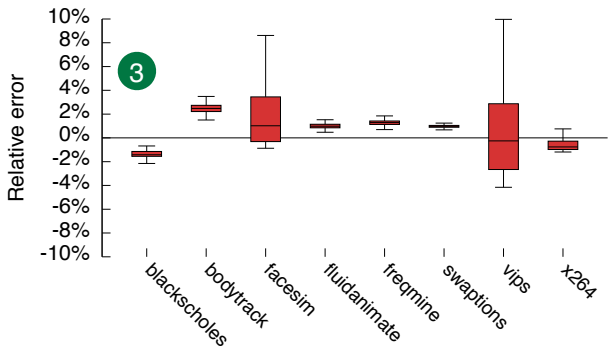
$$P_{host}(f) = P_{idle}(f) + \sum_{pid \in PIDs} P_{cpu}(f, uc^1_{pid} ... uc^N_{pid})$$

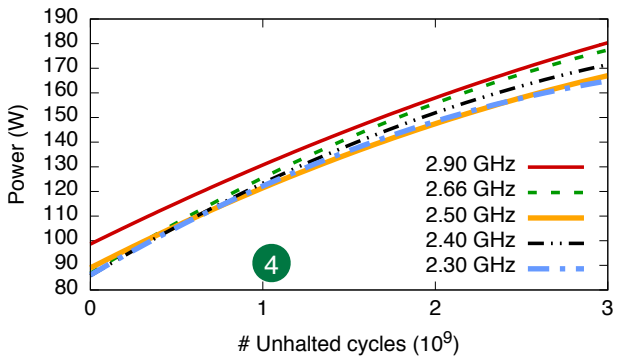
$$P_{cpu}(f, uc^1_{pid} ... uc^N_{pid}) = \sum_{n=1}^{N} P_f(uc^n_{pid})$$

Validation









1. Process-level power consumption of PowerAPI, x264, and freqmine on a Xeon W3520 processor
2. Decreasing load of stress on a i3 2120 processor, compared to RAPL
3. Relative error distribution of the PARSEC benchmarks on a Xeon W3520 processor
4. Power models for the highest frequencies on a Xeon W3520 processor

ADEME Agence de l'Environnement et de la Maîtrise de l'Energie · Inria Inventeurs du monde numérique · Université de Lille · PARA DIME · IIUN Institut d'informatique Université de Neuchâtel · unine Université de Neuchâtel