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MICROMECHANICAL SENSORS USING MERGED EPITAXIAL LATERAL OVERGROWTH OF SILICON

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ABSTRACT

A novel technology for manufacturing thin silicon diaphragm structures is presented. Controllability of thin silicon diaphragm is one of the most important issues in fabricating silicon micromechanical sensors whose sensitivity depends on the diaphragm thickness. This can be accomplished by epitaxial lateral overgrowth (ELO) of single crystal silicon on a patterned layer of masking material, typically SiO_2, combined with crystallographic etching of which etching rate depends on the crystal plane. With recent improvement of ELO material, good quality of 10µm thick, 200µm x 1000µm single crystal silicon was obtained with its thickness being precisely controlled by growth rate (≤ 1µm/min.). The junction leakage of the p-n junction diodes fabricated on merged ELO silicon indicated the material quality is comparable to the substrate silicon. Using this technology, a bridge-type piezoresistive accelerometer with four beams and one proof mass was fabricated successfully. Its sensitivity and resonant frequency were comparable to the accelerometers made by other methods. They were analyzed by comparing the experimental results to a simple analytical solution as well as ANSYS stress simulator using a finite element: methods. The experimental results showed a potential application of the new technology to silicon sensor fabrication but some further refinement is remaining.

Free-standing single crystal cantilever beams were fabricated using, MELO and RIE, of over 1000µm long and 5pm by 10µm in cross section. These beams were very short, straight, indicating little residual stress. Wide, short beams were .fabricated using ELO which were also free standing. Special treatment of MELO indicated that diodes and bipolar transistors fabricated on top of the oxide stripes showed nearly ideal characteristics, hence the quality of the MELO was improved. With MELO of thicker than 5µm, no voids were observed. Test structures significantly with all surface micromachining, were designed for further development of silicon membranes.

CHAPTER 1
INTRODUCTION

1.1 Background

In the last four decades, silicon has been the core material in the area of microelectronics due to its semiconductor electrical properties and fabrication technology. The continuing progress in microelectronics, with the advent of the microprocessor, has made the very large scale integration of circuits possible and tremendously improved the areas of system control and signal processing. In addition, the batch fabrication made the cost of silicon integrated chips fall dramatically and hence the cost of discrete mechanical sensors became a considerable portion in the whole system. That was the time when the mechanical property of silicon began to draw people's attention in the pursuit of cheaper and more versatile sensors. Silicon sensors, if manufactured by batch fabrication which was well developed in microelectronics, could then replace expensive hand-assembled sensors, reduce the whole system price, and give several additional advantages.

With the introduction of the silicon stress sensor in the 1950's, numerous silicon micromechanical sensors such as pressure sensors or accelerometers have been actively developed in the 1970's. In virtually every field of application sensors that transform real-world input into (usually) electrical form of output can be found. Sensor classification schemes can in general range from the very simple to the complex. Figure 1.1 shows an example of the category of mechanical sensor area, which is the most related to the silicon sensor, selected from a sensor classification scheme proposed by White [1].

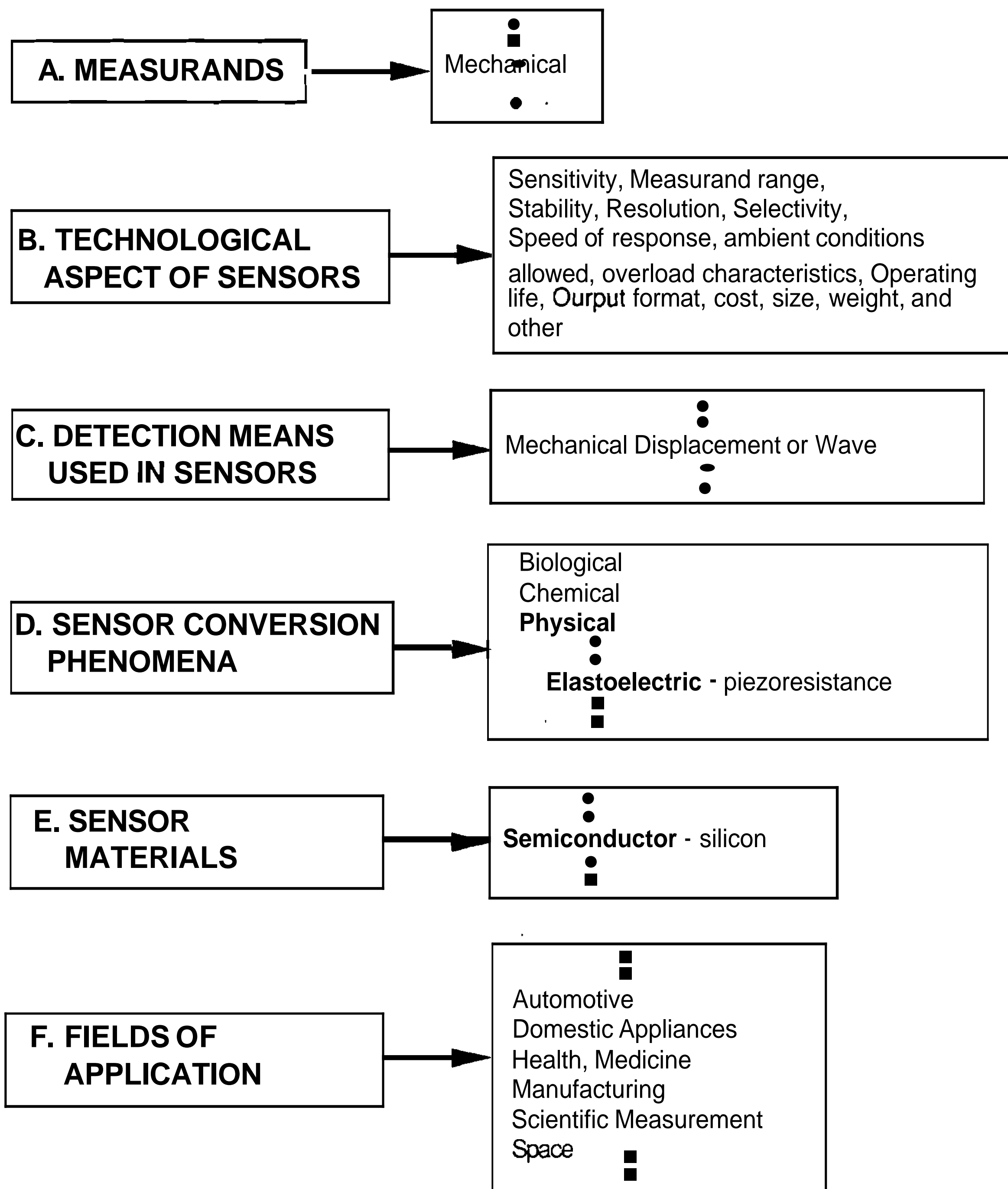

Figure 1.1 The list of possible sensor characteristics - measurands, technological aspects of sensors, detection means, conversion phenomena, sensor materials, fields of application [1].

1.2 Silicon as a mechanical material

Silicon has been increasingly employed in the area of micromechanical sensors because of its excellent mechanical properties. It is rugged, inexpensive.,chemically inert in a corrosive ambient, and superior to metal strain elements in the piezoresistance effect. It also responds to external stimuli with a large sensitivity, makes batch fabrication possible, and permits the integration of the sensing element and the signal-processing circuit in one chip. The important physical effects of silicon in sensor applications are summarized in Table 1.1 [2]. Silicon has shown sufficient effects including the Hall effect, the Seebeck effect, and the piezoresistance effect, all of which are rather large. One problem with silicon is that its sensitivities to strain, light, and magnetic field show a rather large variation with temperature changes. The offset due to temperature sensitivity needs to be eliminated or controlled and it has been shown that the temperature sensitivity of resistors can be eliminated either by signal conditional circuitry or by laser trimming.

In mechanical sensor applications, because silicon is not piezoelectric, only the piezoresistance effect is used. This effect is rather large because the average mobility of electronics and holes in silicon is strongly affected by the application of strain. Depending on the structure and the location of the piezoresistors, this effect can be applied to make micromechanical sensors for pressure, force, acceleration, displacement, torque, or stress.

Table 1.1 Physical effects of silicon sensors to various signals [2].

Signals	Physical effects
Radiant signals	photovoltaic effect, photoelectric effect, photoconductivity, photomagneto-electric effect
Mechanical signals	piezoresistivity, lateral photoelecmc effect, lateral photovoltaic effect.
Thermal signals	Seebeck effect, temperature dependence of conductivity and junctions, Nernst effect
Magnetic signals	Hall effect, magnetoresistance, Suhl effect
Chemical signals	ion-sensitive field effect

1.3 Silicon micromachining

Micromachining is a technology which incorporates miniaturized and mechanical devices with elecmcal devices, using the already-existing and advanced integrated circuit fabrication techniques. Silicon micromachining is usually performed by wet chemical etching to form three-dimensional shapes such as pits, pyramids, trenches, hemispheres, cantilevers, diaphragms, needles, and walls. A wide variety of micromechanical devices can be constructed from combinations of these structural elements [3]. To make a certain physical structure, silicon needs to be either added or removed only at some desired locations. The processing techniques for this include chemical and electrochemical etching, epitaxial growth processes, thermomigration, and field-assisted thermal bonding [4]. Among the mentioned processes, chemical etching is considered as the most versatile processing tool due to the etchant's varying degree of selectivity to silicon material. Key parameters, in controlling micromachining, are crystallographic orientation, etchant, etchant concentration, starting semiconductor material, temperature, and time.

Accelerometers and pressure sensors, two typical examples of integrated silicon sensors, utilize a thin semiconductor diaphragm structure. The thin diaphragm, which is formed by selective etching of the silicon, is used as a stress magnifying device. A piezoresistive sensor, which utilizes the piezoresistive effect of silicon, is the most widely employed type of sensor using the thin diaphragm. This is due to its easier fabrication, smaller area consumption, larger dynamic response, and more linear response than other types of sensors. For the piezoresistive sensors, a full bridge of diffused resistors is usually formed in a (100) oriented silicon diaphragm to detect the physical stimulus by an electrical output. The piezoresistive effect is a change in resistivity with applied pressure due to the change of the carrier mobility in a resistor. Although silicon pressure sensors have been developed for many years, there are problems which have not been adequately solved. One of the most important problems has been the lack of controllability and reproducibility in forming the thin diaphragm by .etching of silicon, resulting in low device yields. Several different diaphragm thickness control and monitoring techniques and their limitations will be discussed and a new single crystal silicon diaphragm fabrication technique using merged epitaxial lateral overgrowth (MELO) of silicon with SiO_2 etch-stop is the topic of this thesis.

1.4 IC compatible micromechanical sensors

When the substrate material for both the sensor and the electronic circuits is silicon, the integration on the sensor and circuits on one chip is possible and profitable. Some of the additional advantages are as follows:

(1) Better signal-to-noise ratio.

(2) Improvement of characteristics in non-linearity, cross-sensitivity, offset, parameter drift, and frequency response.

(3) Signal conditioning and formatting capability: analog-to-digital conversion, impedance matching, output formatting, conditioning.

(4) Speculative applications in future for sophisticated measurement and control systems.

The popular image of a future intelligent sensor is an integrated device combining the sensor with the microcomputer, which is yet to be realized. Figure 1.2 [5] illustrates development stages of such an intelligent sensor. Four separate functional blocks including sensor, signal conditioner, A/D converter, and microprocessor are gradually coupled on a single chip, then turned into a direct coupling of sensor and microprocessor.

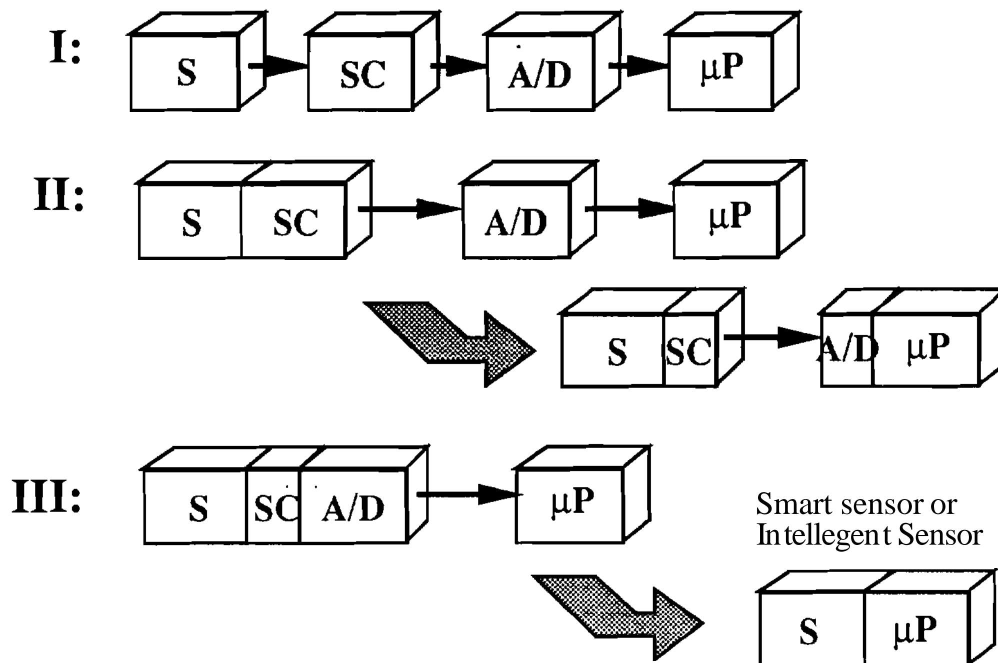

Figure 1.2 Development trends of silicon sensors in integration with microprocessors. (S: Sensor, SC: Signal Conditioner, A/D: A/D Converter, and μP: microcomputer) [5].

1.5 Overview of thesis

The development of a single crystal silicon diaphragm fabrication technology is described and its application to the fabrication of a bridge-type piezoresistive accelerometer is presented. This new diaphragm forming technique utilizes a merged epitaxial lateral overgrowth (MELO) of silicon combined with an SiO_2 etch-stop and a crystallographic self-limiting etching by V-grooves; resulting in high-quality silicon membrane with well-controlled dimensions. The MELO is an extension of the Selective Epitaxial Growth (SEG) and Epitaxial Lateral Overgrowth (ELO) technologies which already have been employed in development of novel devices such as three dimensional MOS and bipolar transistors. This indicates that the new diaphragm forming technique is IC-compatible.

Chapter 2 explores a mechanical properties of silicon and the piezoresistive effect which is employed in silicon micromechanical sensor applications. Chapter 3 reviews the present silicon micromachining technologies and addresses a new silicon diaphragm fabrication technique utilizing MELO-Si and SiO_2 etch-stop and a crystallographic self-limiting etching by V-grooves. Chapter 4 presents the fabrication procedure and its development for a bridge-type piezoresistive accelerometer using the new diaphragm fabrication technique. Chapter 5 describes the performance of the MELO-Si bridge-type piezoresistive accelerometer. This chapter includes the experimental results of the fabricated accelerometer as well as the sensitivity of the accelerometer performance to the applied acceleration in terms of structural parameters. Also discussed is the theoretical static and dynamic response of a bridge-type piezoresistive accelerometer using simple beam theory and the finite element method (FEM). Finally, Chapter 6 summarizes the significance of the new diaphragm technology and discusses the future direction in the development of monolithic IC-compatible silicon micromechanical sensors.

1.6 References

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CHAPTER 2
PIEZORESISTANCE EFFECT OF SILICON

2.1 Introduction

There are various types of silicon rnicromechanical sensors among which two types of sensors are of the most interest nowadays; the accelerometer and the pressure sensor. When the mechanical energy is to be transformed into electrical signals, piezoresistive [1-3] and capacitive sensors [4-6] are two most common sensors used presently. Piezoresistive type devices are considered in this thesis because they are more easily fabricated in smaller dimensions, show better linear sensitivity, and have a somewhat larger dynamic range than capacitive devices [2].

A conventional silicon pressure sensor uses the diaphragm structure shown in Fig. 2.1(a). Particularly in piezoresistive pressure sensors, resistors are implanted or diffused into the front (or top) side which will become the thin diaphragm. Anisotropic etching from the backside creates the characteristic rectangular cavity and leads to a die with a thin diaphragm. A silicon accelerometer typically includes a silicon mass in addition to the beam diaphragm structure which is similar to that of the pressure sensor. Here, the diaphragm structure is utilized in creating sensitive thin beams which would contain stress-sensitive resistors, called piezoresistors. A Bridge-type accelerometer shown in Fig. 2.1(b) and a cantilever-type accelerometer shown in Fig. 2.1(c) are the two most typical accelerometer structures.

When the diaphragm deforms with applied pressure or acceleration, the resistance of a resistor varies accordingly. The resistance change depends on both the change of resistivity with stress, which is the piezoresistive effect, and on the dimensional changes of the resistor due to the stress. The piezoresistors are placed at the locations of peak stresses for the best sensitivity. These resistors are used to form a half or full bridge circuit. Converting the change in the resistance into a voltage change, using the Wheatstone bridge circuit, the output can be measured as a change in voltage. Using this relation, the overall response of a sensor to a physical stimulus can be determined.

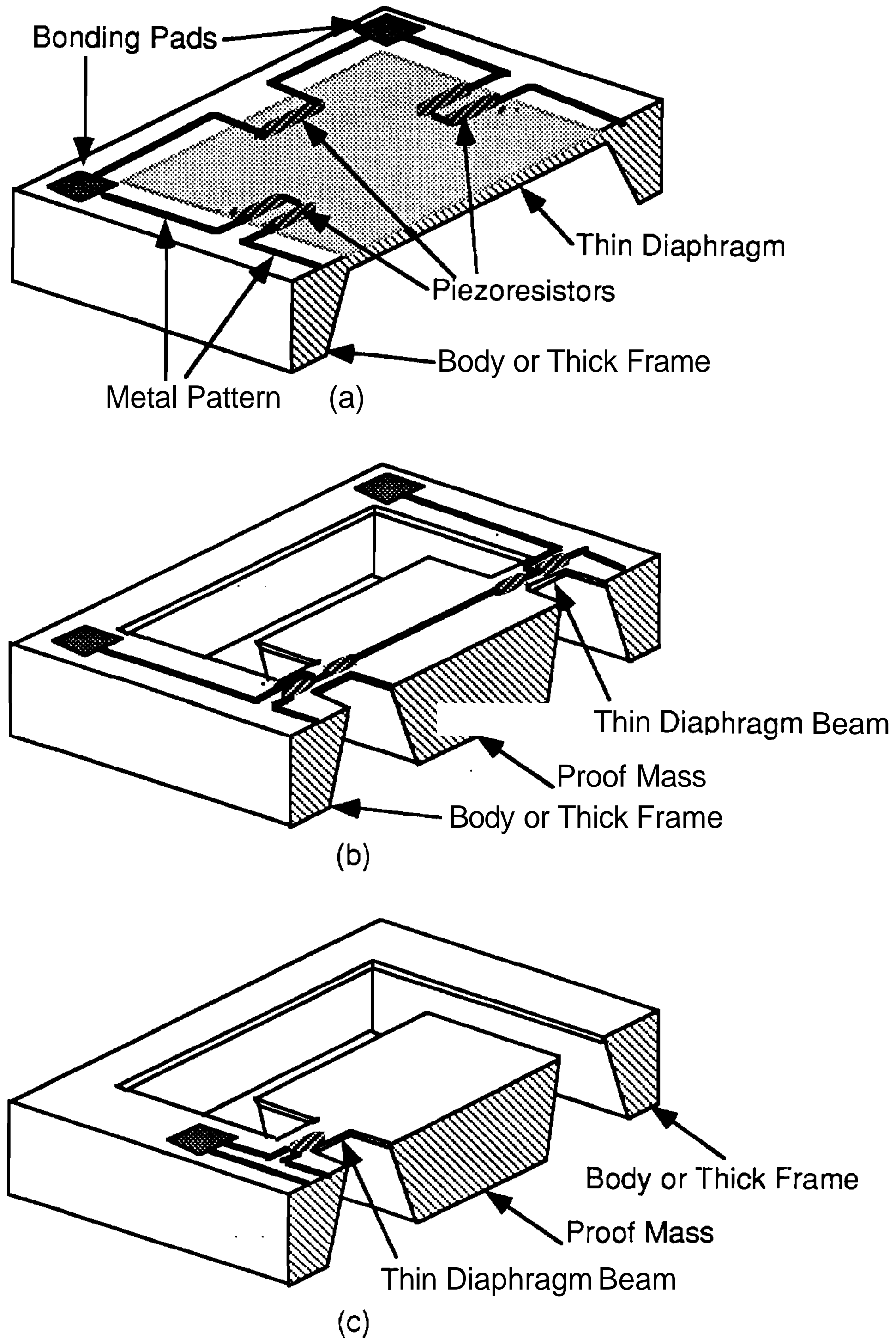


Figure 2.1 Silicon micromechanical sensors utilizing a thin diaphragm: (a) pressure sensor, (b) bridge-type accelerometer, (c) cantilever-type accelerometer.

This chapter describes the piezoresistivity of silicon which is the main reason why silicon started to be recognized as a sensor material. First, the general theory of piezoresistivity of a solid material is considered. 'The phenomenological description of the piezoresistivity and its notation simplification are reviewed. Next, the description of the piezoresistivity in silicon, which is further simplified due to material symmetry, is presented. Finally, the physical explanation of the piezoresistivity in silicon is discussed followed by an evaluation of the piezoresistive coefficients in silicon.

2.2 Theory of Piezoresistivity

Piezoresistivity is defined as the change in the electrical resistivity of a material due to an applied stress. This effect was first investigated by Bridgman [7], who studied the effect of mechanical tension on the electrical resistance of several materials. Later, he also measured the resistivity changes for a number of semiconducting materials under hydrostatic pressure [8]. The symmetry of the second order resistivity tensor for electrically anisotropic materials was demonstrated by Onsager [9]. After that, the specific form of piezoresistive tensor has been developed for all known crystal classes, with the observations about the effects of crystal symmetry on physical properties made by Nye [10], Bhagavantam [11], arid Juretschke [12]. An early theory of the piezoresistance effect in silicon and germanium was developed by Smith [13], who described the physical background of the effect and measured the piezoresistive coefficients experimentally. The theoretical physics of the piezoresistive effect in silicon was addressed by Paul and Pearson [14], and Hemng and Vogt [15].

The application of the piezoresistive effect to strain gages was made by Mason and Thurston [16], who provided the first thorough presentation of the theory of piezoresistivity and who developed the equations describing the resistance change along a uniform conductor subjected to various states of plane stress. These ideas were further developed by Phann and Thurston [17], and by Thurston [18]. The temperature dependence of the piezoresistive coefficients was investigated by Morin, et al. [19], and Tufte and Stelzer [20], shortly after that Keyes investigated the temperature dependence of the elastoresistive coefficients of n-type germanium. General discussions of piezoresistivity were provided by Mason [16], and Bir and Pikus [21] while the piezoresistive characteristics of a diffused layer on a cubic semiconductor were investigated by Kerr and Milnes [22]. The properties and performance characteristics of semiconductor strain gages have been discussed by Padgett and Wright [23], and by Dally and Riley [24].

The nonlinearity of the piezoresistive effect, neglected by most researchers, was addressed by Yamada, et al. [25], and in the same year Kanda [26] represented the piezoresistive coefficients of n-type and p-type silicon graphically, including their dependence on the impurity concentration and temperature.

2.2.1 Phenomenological Description

Assume that the electric field components, E_i, are functions of the current density components, J_j, and the stress components, σ_{kl}. That is, assume

$$E_i = E_i(J_j, \sigma_{kl}). \tag{2.2.1}$$

When E_i is developed in a McLaurin series about the state of zero current and stress, eqn (2.2.1) can be rewritten as

$$dE_i = \frac{\partial E_i}{\partial J_j} dJ_j + \frac{\partial E_i}{\partial \sigma_{kl}} d\sigma_{kl} + \frac{1}{2!}\left[\frac{\partial^2 E_i}{\partial J_j \partial J_m} dJ_j dJ_m + \frac{\partial^2 E_i}{\partial \sigma_{kl}\partial \sigma_{no}} d\sigma_{kl} d\sigma_{no} + 2\frac{\partial^2 E_i}{\partial J_j \partial \sigma_{kl}} dJ_j d\sigma_{kl}\right] + \ldots \tag{2.2.2}$$

Now the derivatives $\partial E_i/\partial \sigma_{kl}$, $\partial^2 E_i/\partial J_j \partial J_m$, and $\partial^2 E_i/\partial \sigma_{kl}\partial \sigma_{no}$ are components of tensors of ranks 3, 3, and 5 respectively and vanish for silicon because all odd rank tensors vanish when there is a center of symmetry. The remaining derivatives are designated as follows:

$$\frac{\partial E_i}{\partial J_j} = \rho_{ij}^o = \text{resistivity components for the unstressed material}$$

$$\frac{\partial^2 E_i}{\partial J_j \partial \sigma_{kl}} = \pi_{ijkl} = \text{piezoresistance components.}$$

Equation (2.2.2) becomes

$$dE_i = \rho_{ij}^o dJ_j + \pi_{ijkl} dJ_j d\sigma_{kl} + \ldots$$

or by replacing the differential increments by the variables themselves,

$$E_i = \rho_{ij}^o J_j + \pi_{ijkl} J_j \sigma_{kl} + \ldots \tag{2.2.3}$$

For sufficiently low levels of stress, this expression can be truncated so that the resistivity change components are linearly related to the stress components, the second term, and it becomes

$$E_i = \rho^o_{ij} J_j + \pi_{ijkl} J_j \sigma_{kl} = (\rho^o_{ij} + \pi_{ijkl}\sigma_{kl}) J_j \qquad (2.2.4)$$

where the subscripts for stress, k and l are variables having a range from 1 to **3.** The piezoresistance coefficient π_{ijkl} is characterized not only by the direction of the electric fields component, i, and the current density component, j, but also by the direction of the stress. The stress σ_{kl} corresponds to a tensile stress along the crystal axes if k=l and represents a shear stress if $k \neq l$.

2.2.2 Notation Simplification

The equation relating resistivity change to the state of applied mechanical stress is written as

$$\rho_{ij} = \rho^o_{ij} + \pi_{ijkl}\sigma_{kl}. \qquad (2.2.5)$$

Because $\rho_{ij}=\rho_{ji}$, which can be shown using the Onsager Reciprocity Principle [9] based on the theory of thermodynamics of irreversible processes, only six of the nine equations are unique in eqn.(2.2.5). In addition, for the piezoresistance components, the first two subscripts can be interchanged with each other, as can the last two subscripts, that is

$$\pi_{ijkl} = \pi_{jikl} = \pi_{ijlk} = \pi_{jilk}. \qquad (2.2.6)$$

Applying the relation $\rho_{ij}=\rho_{ji}$ and eqn.(2.2.6) to eqn.(2.2.5) leads to the following six unique relations:

$$\begin{bmatrix} \rho_{11} \\ \rho_{22} \\ \rho_{33} \\ \rho_{23} \\ \rho_{13} \\ \rho_{12} \end{bmatrix} = \begin{bmatrix} \rho_{11}^o \\ \rho_{22}^o \\ \rho_{33}^o \\ \rho_{23}^o \\ \rho_{13}^o \\ \rho_{12}^o \end{bmatrix} + \begin{bmatrix} \pi_{1111} & \pi_{1122} & \pi_{1133} & \pi_{1123} & \pi_{1113} & \pi_{1112} \\ \pi_{2211} & \pi_{2222} & \pi_{2233} & \pi_{2223} & \pi_{2213} & \pi_{2212} \\ \pi_{3311} & \pi_{3322} & \pi_{3333} & \pi_{3323} & \pi_{3313} & \pi_{3312} \\ \pi_{2311} & \pi_{2322} & \pi_{2333} & \pi_{2323} & \pi_{2313} & \pi_{2312} \\ \pi_{1311} & \pi_{1322} & \pi_{1333} & \pi_{1323} & \pi_{1313} & \pi_{1312} \\ \pi_{1211} & \pi_{1222} & \pi_{1233} & \pi_{1223} & \pi_{1213} & \pi_{1212} \end{bmatrix} \begin{bmatrix} \sigma_{11} \\ \sigma_{22} \\ \sigma_{33} \\ \sigma_{23} \\ \sigma_{13} \\ \sigma_{12} \end{bmatrix} \quad (2.2.7)$$

The conventional shorthand notation for the above subscripts are as follows:

$$11\rightarrow1 \qquad 22\rightarrow2 \qquad 33\rightarrow3 \qquad 23\rightarrow4 \qquad 13\rightarrow5 \qquad 12\rightarrow6.$$

According to this reduced index notation scheme, the resistivity and stress components are relabeled in the following manner:

$$\rho_1 \equiv \rho_{11} \qquad \rho_2 \equiv \rho_{22} \qquad \rho_3 \equiv \rho_{33} \qquad \rho_4 \equiv \rho_{23} \qquad \rho_5 \equiv \rho_{13} \qquad \rho_6 \equiv \rho_{12}$$
$$\sigma_1 \equiv \sigma_{11} \qquad \sigma_2 \equiv \sigma_{22} \qquad \sigma_3 \equiv \sigma_{33} \qquad \sigma_4 \equiv \rho_{23} \qquad \sigma_5 \equiv \rho_{13} \qquad \sigma_6 \equiv \sigma_{12}$$

The piezoresistivity components in eqn.(2.2.7) are renumbered, as shown by Mason and Thurston [16], according to the reduced index notation scheme, except that a two is factored out of the stress elements which relate to the three shear stresses.

The piezoresistivity equations then can be rewritten in the reduced index notation:

$$\begin{bmatrix} \rho_1 \\ \rho_2 \\ \rho_3 \\ \rho_4 \\ \rho_5 \\ \rho_6 \end{bmatrix} = \begin{bmatrix} \rho_1^o \\ \rho_2^o \\ \rho_3^o \\ \rho_4^o \\ \rho_5^o \\ \rho_6^o \end{bmatrix} + \begin{bmatrix} \tilde{\pi}_{11} & \tilde{\pi}_{12} & \tilde{\pi}_{13} & \tilde{\pi}_{14} & \tilde{\pi}_{15} & \tilde{\pi}_{16} \\ \tilde{\pi}_{21} & \tilde{\pi}_{22} & \tilde{\pi}_{23} & \tilde{\pi}_{24} & \tilde{\pi}_{25} & \tilde{\pi}_{26} \\ \tilde{\pi}_{31} & \tilde{\pi}_{32} & \tilde{\pi}_{33} & \tilde{\pi}_{34} & \tilde{\pi}_{35} & \tilde{\pi}_{36} \\ \tilde{\pi}_{41} & \tilde{\pi}_{42} & \tilde{\pi}_{43} & \tilde{\pi}_{44} & \tilde{\pi}_{45} & \tilde{\pi}_{46} \\ \tilde{\pi}_{51} & \tilde{\pi}_{52} & \tilde{\pi}_{53} & \tilde{\pi}_{54} & \tilde{\pi}_{55} & \tilde{\pi}_{56} \\ \tilde{\pi}_{61} & \tilde{\pi}_{62} & \tilde{\pi}_{63} & \tilde{\pi}_{64} & \tilde{\pi}_{65} & \tilde{\pi}_{66} \end{bmatrix} \begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \\ \sigma_6 \end{bmatrix} \quad (2.2.8)$$

The tildes over the reduced index piezoresistivity coefficients indicate that they are intermediate results. The piezoresistive coefficients $\pi_{\alpha\beta}$ are then defined by the following relation:

$$\pi_{\alpha\beta} \equiv \frac{\tilde{\pi}_{\alpha\beta}}{\bar{\rho}} \quad (2.2.9)$$

where the hydrostatic resistivity $\bar{\rho}$ is defined as

$$\bar{\rho} = \frac{1}{3} \text{trace} (p^{o}_{rj}) = \frac{\rho^{o}_{11} + \rho^{o}_{22} + \rho^{o}_{33}}{3} \tag{2.2.10}$$

Equation (2.2.8) can be expressed very compactly using indicial notation:

$$\rho_\alpha = \rho^{o}_{\alpha} + \tilde{\pi}_{\alpha\beta}\sigma_\beta \tag{2.2.11}$$

where α,β range from 1 to *6*. It is important to note that the coefficients $\tilde{\pi}_{\alpha\beta}$ are not tensor components, and that the (6x6) matrix of reduced index piezoresistive coefficients expressed in eqn.(2.2.8) is not symmetric.

Equations (2.2.9) and (2.2.11) can be combined to write the piezoresistive equations in terms of the standard piezoresistive coefficients $\pi_{\alpha\beta}$:

$$\rho_\alpha = \rho^{o}_{\alpha} + (\bar{\rho}\pi_{\alpha\beta})\sigma_\beta \tag{2.2.12}$$

or

$$\frac{\Delta\rho_\alpha}{\bar{\rho}} = \pi_{\alpha\beta}\sigma_\beta. \tag{2.2.13}$$

This can be expressed in mamx form as follows:

$$\begin{bmatrix} \Delta\rho_1 \\ \Delta\rho_2 \\ \Delta\rho_3 \\ \Delta\rho_4 \\ \Delta\rho_5 \\ \Delta\rho_6 \end{bmatrix} = \bar{\rho} \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{13} & \pi_{14} & \pi_{15} & \pi_{16} \\ \pi_{21} & \pi_{22} & \pi_{23} & \pi_{24} & \pi_{25} & \pi_{26} \\ \pi_{31} & \pi_{32} & \pi_{33} & \pi_{34} & \pi_{35} & \pi_{36} \\ \pi_{41} & \pi_{42} & \pi_{43} & \pi_{44} & \pi_{45} & \pi_{46} \\ \pi_{51} & \pi_{52} & \pi_{53} & \pi_{54} & \pi_{55} & \pi_{56} \\ \pi_{61} & \pi_{62} & \pi_{63} & \pi_{64} & \pi_{65} & \pi_{66} \end{bmatrix} \begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \\ \sigma_6 \end{bmatrix} \tag{2.2.14}$$

It is important to note that the piezoresistive coefficients $\pi_{\alpha\beta}$ are also not tensor components, and the relation $\pi_{\alpha\beta}=\pi_{\beta\alpha}$ is not valid for general classes of materials.

2.3 Piezoresistive Effect of Silicon

The phenomenological notation and its simplified form of piezoresistance coefficients can be even further simplified in a cubic material like silicon due to its symmetry condition.

In this section, the material symmetry of silicon is considered and resistance change in silicon due to applied stress is expressed in terms of piezoresistance coefficients. Then, the physical explanation of the piezoresistance effect is exploited and the evaluation of the coefficients is described.

2.3.1 Material Symmetry Considerations in Silicon

The general equations of piezoresistivity can be simplified for certain materials, particularly cubic materials such as silicon and germanium, by taking into account material symmetry. The equations produced will be considerably simpler in form, but they will be valid only for type m3m cubic crystalline materials. If a rotation and/or reflection of the lattice leaves it in a position indistinguishable from its original position, the crystal is said to possess symmetry, and the rotation and/or reflection is called a symmetry operation. Such a coordinate transformation is also referred to as a symmetry elements. Symmetry elements play a large role in determining the material properties of a crystal.

The basis of the study of the effect of a crystal's symmetry on its physical properties is Newmann's principle, which states that the symmetry elements of any physical property of a crystal must include all the symmetry elements of the point group of the crystal. A point group is defined as the entire set of symmetry elements possessed by the crystal lattice structure. Due to the restrictions imposed by lattice structure on the directional symmetry of a crystal, only 32 point groups exist. These have been grouped into seven crystal systems, according to their implications on the shape of the unit cell. Silicon falls into point group 32, which is one of five point groups in the cubic crystal system. This point group has the Schoenflies symbol O_h and the Hermann-Mauguin symbol m3m. The symmetry elements of this point group, when written out, are as follows:

$$E \; 8C_3 \; 3C_2 \; 6C_4 \; i \; 8S_6 \; 3\sigma \; 6\sigma \; 6S_4$$

where $E \equiv 2\pi$ rotation about an axis (identity)

$C_p \equiv \frac{2\pi}{P}$ rotation about an axis

$i \equiv$ center of inversion

$S_p \equiv \frac{2\pi}{P}$ rotation about an axis followed by a reflection in a plane normal to that axis

$\sigma \equiv$ plane of reflection.

There is a subset of the set of symmetry elements of a crystal which forms a basis for the set of symmetry elements for that crystal's point group. This subset is called the generating elements for that point group. When the coordinate transformations described by the generating elements are applied to a material property, that property is affected in the same way as if the entire set of transformations described by all the symmetry elements had been applied to it. The coordinate transformations described by the generating elements are applied successively to the set of tensor equations describing the material property of interest. It is required that the equations remain invariant under each generating element transformation. As the generating elements are applied, relationships between the constants representing the property begin to emerge. After all the generating elements have been applied, a set of non-vanishing independent coefficients will remain. These simplified coefficients completely describe the material property of interest for a crystal of a given symmetry and are valid for all members of that point group.

In the case of silicon, the generating elements have been given by Juretschke [12] to be as follows:

$$[a_{ij}] = \begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & -1 \end{bmatrix} \equiv i \tag{2.3.1}$$

$$[a_{ij}] = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix} \equiv C_3 \tag{2.3.2}$$

$$[a_{ij}] = \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \equiv C_4 \tag{2.3.3}$$

The components of the unstressed resistivity tensor, ρ_{ij}, must satisfy the generating element transformation in eqn.(2.3.4),

$$[\rho^o] = [a][\rho^o][a]^t. \tag{2.3.4}$$

Applying each of the generating elements in eqns.(2.3.1) - (2.3.2) to eqn.(2.3.4) yields the following result for the unstressed resistivity components:

$$\begin{bmatrix} \rho_{11}^{o} & \rho_{12}^{o} & \rho_{13}^{o} \\ \rho_{12}^{o} & \rho_{22}^{o} & \rho_{23}^{o} \\ \rho_{13}^{o} & \rho_{23}^{o} & \rho_{33}^{o} \end{bmatrix} = \begin{bmatrix} \rho_{o} & 0 & 0 \\ 0 & \rho_{o} & 0 \\ 0 & 0 & \rho_{o} \end{bmatrix} \tag{2.3.5}$$

This result means that unstressed silicon, or any other unstressed crystal of the same point group is electrically isotropic. The piezoresistive coefficient matrix in eqn.(2.2.14) can also be simplified for cubic crystal materials by applying the generating elements to the invariant transformation rule.

$$[\pi] = [T][\pi][T]^{-1} \tag{2.3.6}$$

The transformation matrix, [T], has been defined as

$$[T] = \begin{bmatrix} l_1^2 & m_1^2 & n_1^2 & 2m_1n_1 & 2l_1n_1 & 2l_1m_1 \\ l_2^2 & m_2^2 & n_2^2 & 2m_2n_2 & 2l_2n_2 & 2l_2m_2 \\ l_3^2 & m_3^2 & n_3^2 & 2m_3n_3 & 2l_3n_3 & 2l_3m_3 \\ l_2l_3 & m_2m_3 & n_2n_3 & m_2n_3+m_3n_2 & l_2n_3+l_3n_2 & l_2m_3+l_3m_2 \\ l_1l_3 & m_1m_3 & n_1n_3 & m_1n_3+m_3n_1 & l_1n_3+l_3n_1 & l_1m_3+l_3m_1 \\ l_1l_2 & m_1m_2 & n_1n_2 & m_1n_2+m_2n_1 & l_1n_2+l_2n_1 & l_1m_2+l_2m_1 \end{bmatrix} \tag{2.3.7}$$

where the reduced index notation for the direction cosines is defined as

$$\begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} = \begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} \tag{2.3.8}$$

Applying the transformation matrix of eqn.(2.3.7), after substituting each of the generating elements of eqns.(2.3.1)-(2.3.3) to eqn.(2.3.6) gives the following result for the piezoresistive coefficients:

$$[\pi] = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{22} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \tag{2.3.9}$$

This is the on-axis piezoresistive coefficient matrix. It is valid for silicon, or any other crystal possessing m3m point group symmetry, when the coordinate system is aligned with the principal crystallographic directions. The form of the piezoresistive coefficient matrix in an off-axis coordinate system can be obtained by substituting eqn.(2.3.9) into the transformation relations:

$$\pi'_{\alpha\beta} = T_{\alpha\gamma}\, \pi_{\gamma\delta}\, T^{-1}_{\delta\beta}. \tag{2.3.10}$$

2.3.2 Resistance Change Equations

Now that the symmetry effects of silicon have been taken into account, the equations of conduction for a stressed material can be considerably simplified. In a three-dimensional medium with orthogonal axes 1, 2, and 3, the electric field components, E_i, and current density components, J_j, can be related as

$$E_i = \rho_{ij}\, J_j. \tag{2.3.11}$$

Here, each of the subscripts i and j have a range from 1 to 3, and ρ_{ij} is the resistivity component which relates the electric field component in the i-direction to the current component in the j-direction. This expression can be expanded in the single subscript notation:

$$\begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} = \begin{bmatrix} \rho_{11} & \rho_{12} & \rho_{13} \\ \rho_{21} & \rho_{22} & \rho_{23} \\ \rho_{31} & \rho_{32} & \rho_{33} \end{bmatrix} \begin{bmatrix} J_1 \\ J_2 \\ J_3 \end{bmatrix} = \begin{bmatrix} \rho_1 & \rho_6 & \rho_5 \\ \rho_6 & \rho_2 & \rho_4 \\ \rho_5 & \rho_4 & \rho_3 \end{bmatrix} \begin{bmatrix} J_1 \\ J_2 \\ J_3 \end{bmatrix} \tag{2.3.12}$$

For a cubic crystal like silicon, under no stress, the resistivity becomes isotropic and the second order resistivity tensor components can be represented as

$$\rho_{ij} = \rho_o \delta_{ij} \text{ where } \delta_{ij} = 1 \text{ if } i=j \quad = 0 \text{ if } i \neq j \tag{2.3.13}$$

Therefore, the overall relation between mechanical stress and **electrical** resistivity for silicon can be expressed as

$$\begin{bmatrix} \rho_1 \\ \rho_2 \\ \rho_3 \\ \rho_4 \\ \rho_5 \\ \rho_6 \end{bmatrix} = \begin{bmatrix} \rho_o \\ \rho_o \\ \rho_o \\ \rho_o \\ \rho_o \\ \rho_o \end{bmatrix} + \rho_o \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{22} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \begin{bmatrix} \sigma_{11} \\ \sigma_{22} \\ \sigma_{33} \\ \sigma_{23} \\ \sigma_{13} \\ \sigma_{12} \end{bmatrix} \tag{2.3.14}$$

In the piezoresistive coefficient matrix, the first subscript denotes the relative directions of the electric field and current density vectors, and the second subscript denotes the stress direction. Thus, π_{11} is the piezoresistance coefficient coupling for the elecmc field and the current density vectors along the same crystallographic direction with the tensile stress applied in that same direction. Similarly, π_{12} represents coupling between coincident electric field and current density vectors and a tensile stress applied normal to the direction of current flow. Finally, π_{44} represents coupling between elecmc field and current density vectors (which are normal to each other) and an applied shear stress. In this notation the three equations of Eqn. (2.3.12) become

$$\begin{aligned} \frac{E_1}{\rho_o} &= J_1[1 + \pi_{11}\sigma_1 + \pi_{12}(\sigma_2 + \sigma_3)] + \pi_{44}(J_2\sigma_6 + J_3\sigma_5) \\ \frac{E_2}{\rho_o} &= J_2[1 + \pi_{11}\sigma_2 + \pi_{12}(\sigma_1 + \sigma_3)] + \pi_{44}(J_1\sigma_6 + J_3\sigma_4) \quad . \\ \frac{E_3}{\rho_o} &= J_3[1 + \pi_{11}\sigma_3 + \pi_{12}(\sigma_1 + \sigma_2)] + \pi_{44}(J_1\sigma_5 + J_2\sigma_4) \end{aligned} \tag{2.3.15}$$

A much simpler equation can be used when we are concerned with an electric field component E, current density component J, and a longitudinal tensile stress σ_l all along the same direction. A simplified expression can be written as

$$\frac{E}{\rho_o} = J\,[1 + \pi_l\sigma_l] \text{ or } + \frac{E}{J} = \rho_o\,[1 + \pi_l\sigma_l] \tag{2.3.16}$$

where π_l is a longitudinal piezoresistance coefficient and σ_l is a longitudinal, or uniaxial tensile stress. The ratio of E/J, which is the longitudinal resistivity under a longitudinal tensile stress σ_l, will be denoted by

$$\frac{E}{J} = \rho_o + Ap. \tag{2.3.17}$$

Then, from Eqns. (2.3.16) and (2.3.17), the fractional change in resistivity due to a longitudinal tensile stress is

$$\frac{\Delta\rho}{\rho_o} = \pi_l\sigma_l. \tag{2.3.18}$$

Similarly, when a longitudinal tensile stress is perpendicular to an electric field and current density components, the fractional change in resistivity due to the stress can be expressed as

$$\frac{\Delta\rho}{\rho_o} = \pi_t\sigma_t \tag{2.3.19}$$

where π_t is a transverse piezoresistance coefficient and σ_t is a tensile stress perpendicular to the current flow.

The actual resistance change will be the result of the combined effects of this resistivity change and dimension changes. A tensile stress always results in an increase in length and a decrease in cross-sectional area and thus tends to increase the resistance in that direction and to decrease in the perpendicular direction. In many cases, the small effect of dimension changes can be neglected in comparison with the higher effect due to the change in resistivity [13, 16].

In a typical application of the piezoresistance effect to micromechanical sensors, π_l and π_t are two piezoresistance coefficients which need to be considered. The expression for these coefficients along arbitrary axes can be expressed in terms of fundamental coefficients π_{11}, π_{12}, and π_{44}. The simplest case is that when a uniaxial tensile stress is applied along one of the crystal axes, like [100] direction in silicon. In this case, π_l is simply π_{11} and π_t is π_{12}. For a more general case, the expression for π_l and π_t can be obtained by the transformation of the crystal axes. For an arbitrary coordinate system (1',2',3') which is rotated respect to the crystallographic axes (1,2,3) as shown in Fig. 2.2, the direction cosines l, m, and n for this transformation are

$$\begin{array}{cccc|ccc} & 1 & 2 & 3 & 1 & 2 & 3 \\ 1' & m_1 & l_1 & n_1 & \cos\theta\cos\phi & \cos\theta\sin\phi & -\sin\theta \\ 2' & m_2 & l_2 & n_2 & -\sin\phi & \cos\phi & 0 \\ 3' & m_3 & l_3 & n_3 & \cos\phi\sin\theta & \sin\phi\sin\theta & \cos\theta \end{array} \tag{2.3.20}$$

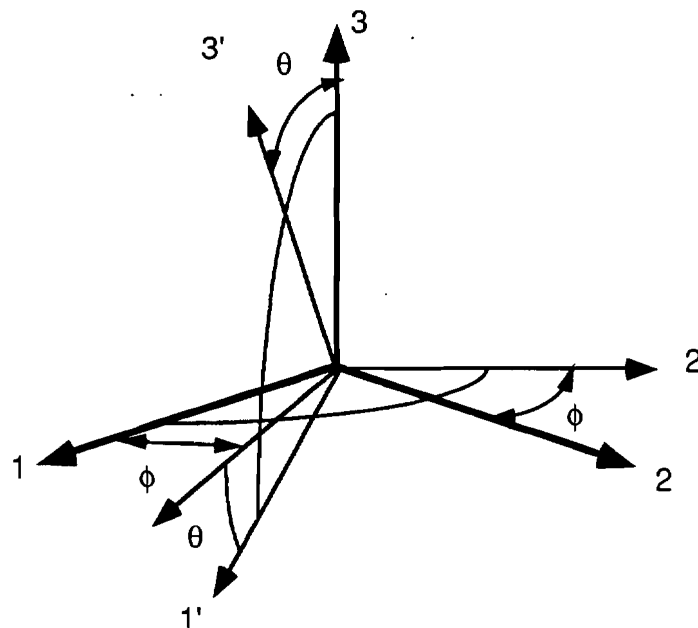


Figure 2.2 An arbitrary coordinate system (1',2',3') referred to the crystallographic axes.

To obtain a new expression of Eqn. (2.3.15) in the new coordinate system, the transformation of the components of Eqn. (2.3.15) is necessary. First, the stress components need to be expressed in terms of new stress components in the new coordinate system. The same procedure needs to be done for the current density components J and J'. Also, an expression for the electric field components for the new coordinate system needs to be written in terms of the electric field components along the major crystallographic axes. Finally, combining all the previous equations, a complete set of expressions relating the electric fields, current densities, and stresses in the arbitrary coordinate system (1',2',3') are obtained [17]. If only E'_1 and J'_1 exist and E'_2, E'_3, J'_2, and J'_3 are zero and if stress components σ'_1 through σ'_6 are applied as shown in Fig. 2.3, it results in

$$\frac{E'_1}{\rho_0} = J'_1(1 + \pi'_{11}\sigma'_1 + \pi'_{12}\sigma'_2 + \pi'_{13}\sigma'_3 + \pi'_{14}\sigma'_4 + \pi'_{15}\sigma'_5 + \pi'_{16}\sigma'_6). \quad (2.3.21)$$

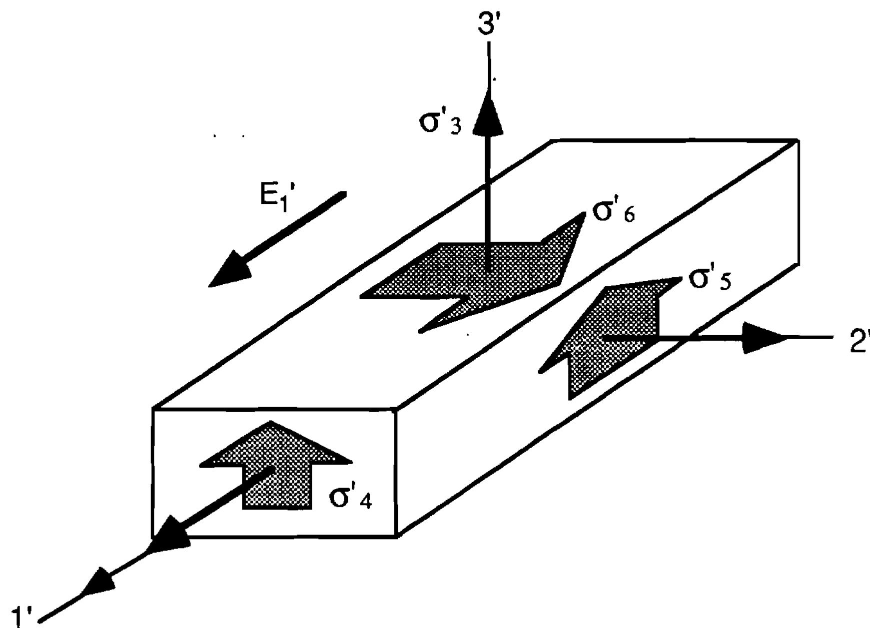


Figure 2.3 Three tensile stresses σ'_1, σ'_2, and σ'_3, and three shear stresses σ'_4, σ'_5, and σ'_6 for colinear field component E'_1 and current density component J'_1.

The expressions for the piezoresistance coefficients are shown in Table 2.1. As an example, for <110>-oriented resistors on (100)-oriented silicon, $\phi=45°$ and $\theta=0°$. Substituting these angles into the direction cosines and inserting the resulting direction cosines in the expression of the piezoresistance coefficients in Table 2.1 results in

$$
\begin{aligned}
\pi'_{11} &= \frac{1}{2}(\pi_{11} + \pi_{12} + \pi_{44}) \\
\pi'_{12} &= \frac{1}{2}(\pi_{11} + \pi_{12} - \pi_{44}) \\
\pi'_{13} &= \pi_{12}
\end{aligned}
\qquad (2.3.22)
$$

and all the piezoresistance coefficients for the shear stresses (π'_{14}, π'_{15}, and π'_{16}) become zero. Then, Eqn. (2.3.22) can be rewritten as

$$
\begin{aligned}
\frac{E'_1}{J'_1} &= \rho_o(1 + \pi'_{11}\sigma'_1 + \pi'_{12}\sigma'_2 + \pi'_{13}\sigma'_3) \\
&= \rho_o + \Delta\rho \\
&= \rho_o\left(1 + \frac{\Delta\rho}{\rho_o}\right)
\end{aligned}
\qquad (2.3.23)
$$

Table 2.1 Expressions for the piezoresistance coefficients for an arbitrarily rotated coordinate system [17].

$$
\begin{aligned}
\pi'_{11} &= \pi_{11} - 2(\pi_{11} - \pi_{12} - \pi_{44})(l_1^2 m_1^2 + l_1^2 m_1^2 + l_1^2 m_1^2) \\
\pi'_{12} &= \pi_{12} + (\pi_{11} - \pi_{12} - \pi_{44})(l_1^2 l_2^2 + m_1^2 m_2^2 + n_1^2 n_2^2) \\
\pi'_{13} &= \pi_{12} + 2(\pi_{11} - \pi_{12} - \pi_{44})(l_1^2 l_3^2 + m_1^2 m_3^2 + n_1^2 n_3^2) \\
\pi'_{14} &= 2(\pi_{11} - \pi_{12} - \pi_{44})(l_1^2 l_2 l_3 + m_1^2 m_2 m_3 + n_1^2 n_2 n_3) \\
\pi'_{15} &= 2(\pi_{11} - \pi_{12} - \pi_{44})(l_1^3 l_3 + m_1^3 m_3 + n_1^3 n_3) \\
\pi'_{16} &= 2(\pi_{11} - \pi_{12} - \pi_{44})(l_1^3 l_2 + m_1^3 m_2 + n_1^3 n_2)
\end{aligned}
$$

If we let $\pi'_{11}=\pi_l$, $\pi'_{12}=\pi_t$, $\pi'_{13}=\pi'_t$, $\sigma'_1=\sigma_l$, $\sigma'_2=\sigma_t$, and $\sigma'_3=\sigma'_t$, where the subscript I stands for the longitudinal component and t stands for the transverse component relative to the current flow direction, then Eqns. (2.3.22) and (2.3.23) results in

$$\frac{\Delta\rho}{\rho_o} = \pi_l\sigma_l + \pi_t\sigma_t + \pi'_t\sigma'_t = \frac{1}{2}(\pi_{11} + \pi_{12} + \pi_{44})\sigma_l + \frac{1}{2}(\pi_{11} + \pi_{12} - \pi_{44})\sigma_t + \pi_{44}\sigma_t \quad (2.3.24).$$

The transformation from the crystal axes to a Cartesian system of arbitrary orientation can be done by direction cosines between the two axes, which can be expressed in terms of Euler's angles. Usually, two typical piezoresistance effects are considered when uniaxial stress is applied in the material. One is a longitudinal piezoresistance coefficient when the current and field are in the same direction of the stress noted by π_l, the other is a transverse piezoresistance coefficient when the current and field are perpendicular to the stress noted by π_t.

2.3.3 Physics of Piezoresistivity in Silicon

Silicon is one of the best known materials showing a strong piezoresistance effect [3, 18] and several attempts have been proposed to explain the piezoresistance effect in silicon. Based on the work of Herring [15], two mechanisms were generally considered to be responsible for this effect in silicon. First, the change in the energy gap, E_g, in response to the applied stress was considered. The stress causes a volume change which in turn causes a change in the energy gap between the valence and conduction bands. Therefore, the number of carriers changes resulting in the resistivity change. This energy gap effect appears to be too small to explain the large piezoresistance effects measured, and it gives zero contribution to the shear coefficients [13].

Second, changes in carrier mobility [13, 15] due to the effect of strain has been suggested. The energy band structure of n-type silicon shown in Fig. 2.4(a) indicates that the band structure is not spherical but has six minima along the <100> axes. Fig. 2.4(b) shows the structure of the constant energy surfaces which consist of six ellipsoids of revolution located on the cube axes in momentum space. The electrons are located in the energy minima which are centered at the ellipsoid centers. Because the energy surfaces are ellipsoidal, the effective mass of an electron in a given group is anisotropic. Hence, the mobility associated with a group is anisotropic although the overall mobility, or conductivity, is isotropic. In the absence of strain, the energy valleys are equally populated with electrons.

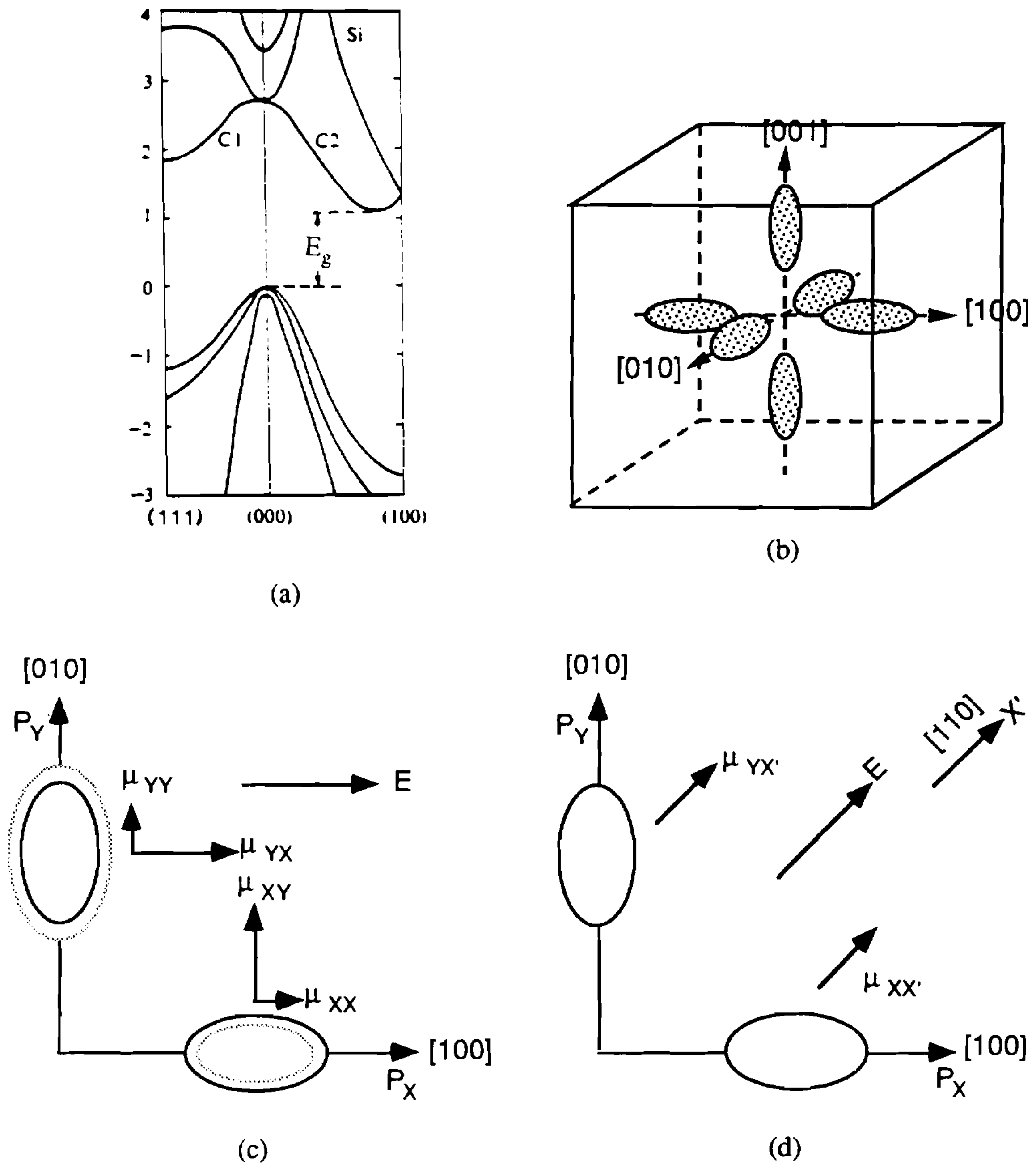


Figure 2.4 Energy diagram versus wave vector for silicon. (a) A picture of electron energy versus wave vector along <100> and <111> axes. (b) Constant energy surfaces characterizing the conduction-band structure in silicon. (c) and (d) describes schematic diagram of constant energy surfaces and the effect of stress on the valley energies when the stress is applied (c) along [100] and (d) along [110] direction.

When the crystal is strained by a tension in the [100] direction, the two energy minima shift in opposite directions. This is indicated by the shift of a given constant energy surface from the solid line to the dashed positions in Fig. 2.4(c), where the value of the energy surface along the stress direction is raised and that at right angles to the stress direction is lowered. The mobility of the charge carriers in different directions are roughly indicated by the arrows. Electrons then transfer from the high-energy x valley to the lower-energy y valley. There will be more electrons that have high mobility and fewer electrons of low mobility in the x direction. Hence there are more electrons with the higher mobility in the [100] direction and the conductivity will become anisotropic in <100> directions. The results have shown that, for an n-type silicon sample, a tensile stress along a crystallographic axis, when the direction of current flow is same, produces a large negative change in the resistance while a stress in a perpendicular direction produces a positive change of about half the value. Also it can be seen that tensile forces applied in a [110] direction will not change [100] and [010] valleys and will not cause the electron transfer mechanism between x and y valleys. The mobility of the x and y groups are the same in the [110] direction and the strain shifts the energy of those two valleys identically, i.e. not at all, as shown in Fig. 2.4(d). Therefore, no piezoresistance effect should be observed.

However, when the tensile force is applied in a [110] direction, small conductivity change is observed. Kanda [27], in his recent review, explained this by the change of effective mass of electron in the [001] energy valleys as shown in Fig. 2.5(b) due to the special character of the conduction band. Therefore, only a small piezoresistance effect will be produced, which is reflected in the low value of the corresponding piezoresistance coefficient for n-type silicon in <110> direction. These mechanisms, camer-transfer between intravalleys and mobility change, seem applicable particularly to n-type silicon and there is a good agreement with experimental results.

It has been shown experimentally that the hole mobility is also strongly dependent on strain [13]. However, the valence band structure for p-type silicon is very complex since the energy surfaces are not of the multivalley type, but rather of the degenerate type illustrated in Fig. 2.4(a) and 2.6(a). Thus, the origin of the large piezoresistance effect in the p-type silicon requires a different explanation. The band edge, the upper $P_{3/2}$ state, consists of a pair of two-fold degenerate bands at $k=0$, usually designated as the 'light' and 'heavy' hole bands. These energy surfaces are warped spheres. The spin-orbit split-off band, the lower $P_{1/2}$ state, has a spherical energy surface. When a uniaxial tensile stress is applied parallel to the <111> direction, the degeneracy of the valence band is lifted and two bands of prolate and oblate ellipsoidal energy surfaces with anisotropic mass parameters are

formed as illustrated in Fig. 2.6(b) [28, 29]. Consequently, the resistivity change comes from both the mass change and hole transfer. Although several qualitative explanations were considered for the main source of the piezoresistance in the degenerate bands, the calculation of the piezoresistance coefficients from the energy distortion is more difficult due to the three energy surfaces found for p-type silicon.

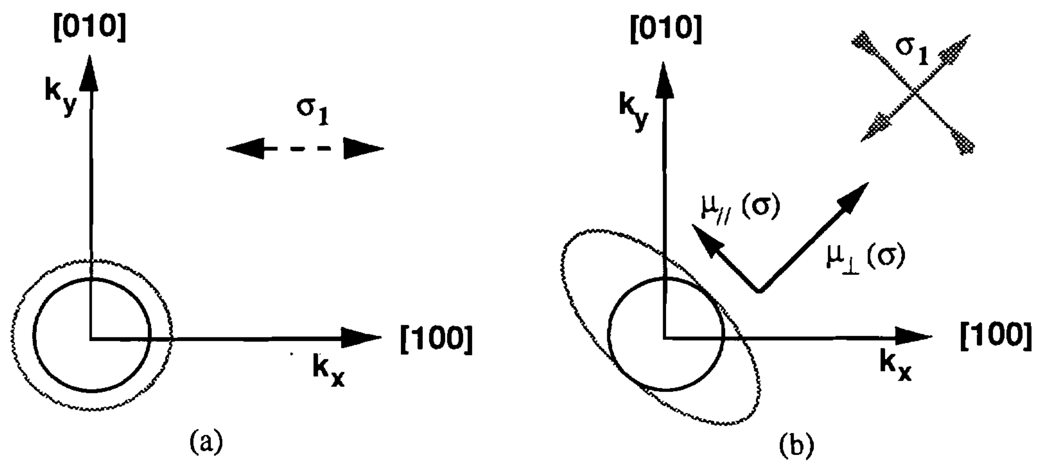
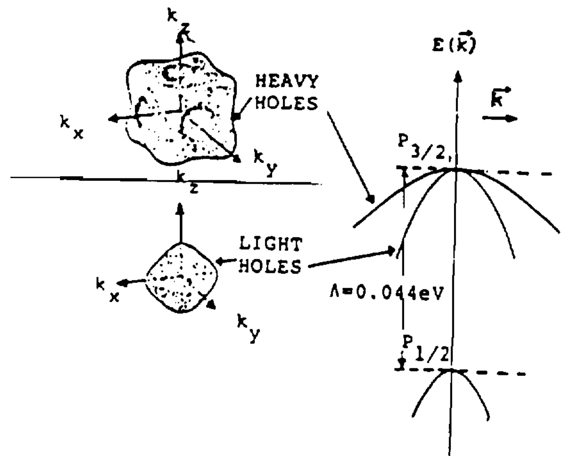
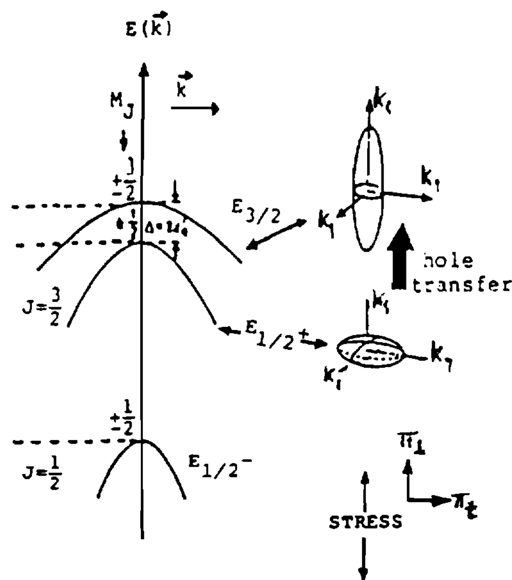


Figure 2.5 Schematic diagram of the <001> valley in k-space for n-type silicon. Dotted lines show effect of stress. (a) corresponds to stress σ_1 and (b) to σ_6 [26].



(a)



(b)

Figure 2.6 **Schematic diagram of the valence band energy surfaces in k-space near k=0 for p-type silicon [29]. (a) Warped and degenerate structure under no stress. (b) The split band valence bands of uniaxially stressed silicon at k=0, denoted by A, for a compressive stress σ//[001].**

2.3.4 Evaluation of Piezoresistive Coefficients in Silicon

The values of the piezoresistance coefficients have been investigated by many authors. Smith [13] published experimental data for π_{11}, π_{12}, and π_{44} in bulk material both for n- and p-type silicon and germanium. The data by Smith were obtained from materials having an impurity concentration of the order of 10^{15} cm^{-3}, which is too low to be implemented using standard impurity diffusion technology. Also, it can be questioned whether or not the piezoresistance coefficients measured from the bulk material can be considered to be identical to those from diffused resistors. Tufte, Chapman, and Long [30] reported the first example of an integrated device utilizing both the longitudinal and transverse piezoresistive effects. In their work, using diffused resistors on a circular silicon diaphragm, they found the dependence of the piezoresistance coefficient on surface impurity concentration shown in Fig. 2.7. Their data revealed linearly decreasing piezoresistance coefficients with increasing doping. Shortly after this, Kerr and Milnes [22] presented a theoretical analysis of the piezoresistance coefficients as a function of surface concentration for diffused resistors. About the same time, Tufte and Steltzer [30] published experimental data showing the independence of the piezoresistance coefficients of the diffused layer thickness. Table 2.2 shows the typical values of π_{11}, π_{12}, and π_{44} at room temperature for n- and p-type silicon both in bulk material and in diffused layers based on the work of the above researchers.

Recently, Kanda [26] published the graphical representation of calculated piezoresistance coefficients in silicon as shown in Fig. 2.8. Figure 2.8(a) and (b) show the room temperature piezoresistance coefficients π_l and π_t in the (100) plane of both n- and p-type silicon. Figure 2.8(a) and (b) indicate that the best piezoresistance effects that can be obtained depends on the type and the direction of the resistors. When n-type resistors are used, they should be aligned to <100> directions, and when p-type resistors are used, they should be aligned to <110> directions for the best sensitivity.

Multiplication of these coefficients by a piezoresistance factor, P(N,T), which summarizes the effects of surface concentration and temperature, determines the actual coefficients for a given surface concentration and temperature. Figure 2.9(a) and (b) show the piezoresistance factor, P(N,T), as a function of impurity concentration between $10^{15}cm^{-3}$ and $10^{20}cm^{-3}$ with temperature varying from -75" to +175° for n- and p-type silicon. These calculations are in good agreement with previously reported experimental data for the variations of π with both impurity concentration and temperature. However, more accurate calculations that include various scattering mechanisms can be made for further improvement.

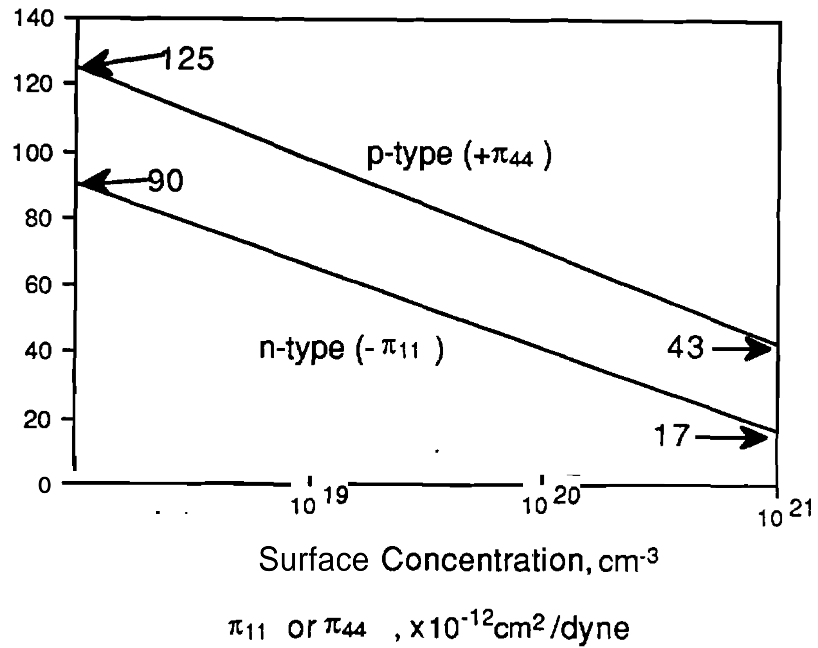
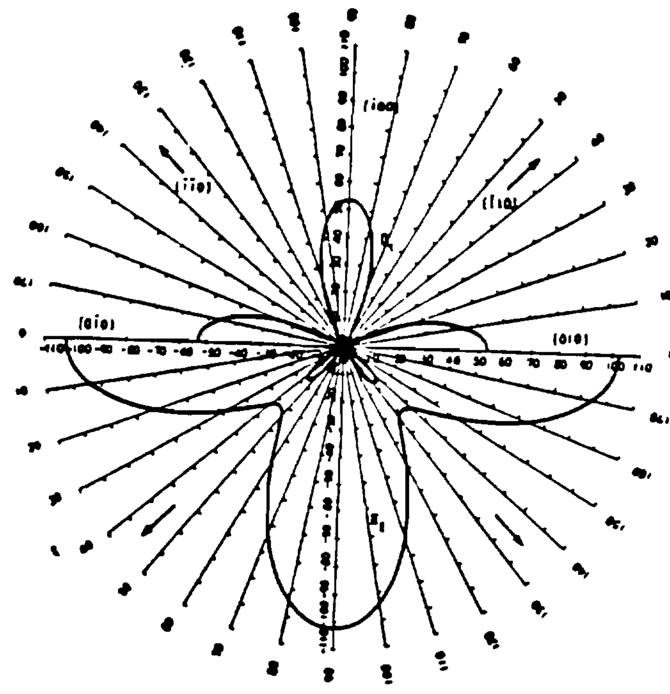


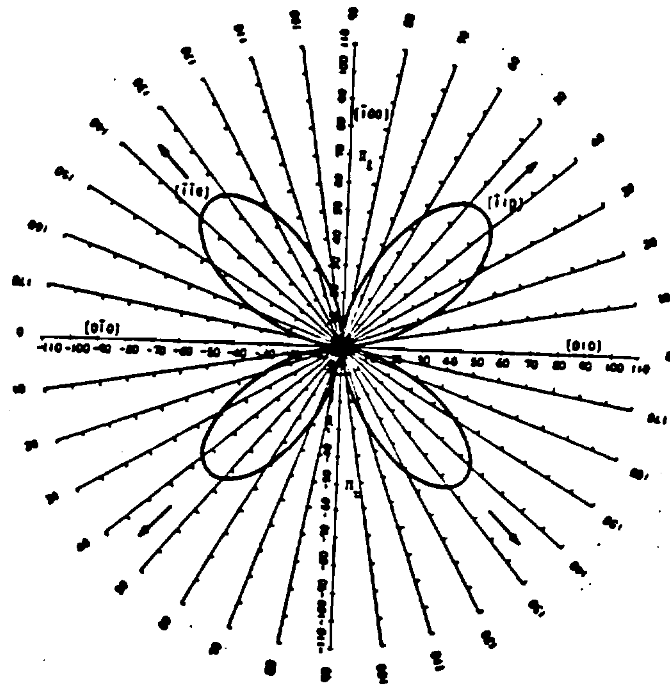
Figure 2.7 Piezoresistance coefficients vs. surface impurity concentration in silicon diffused layers [30].

Table 2.2 Typical piezoresistance coefficients in silicon [13, 20, 30] (x 10^{-12} cm^2/dyne).

	Impurity Concentration	π_{11}	π_{12}	π_{44}
Bulk Material	p-type (1.6 x $10^{15}cm^{-3}$)	. 6.6	-1.1	138
	n-type (4 x $10^{14}cm^{-3}$)	-102	53.4	-14
Diffused Layer	p-type ($10^{19}cm^{-3}$)	4	-1	100
	n-type ($10^{19}cm^{-3}$)	-65	32	-12

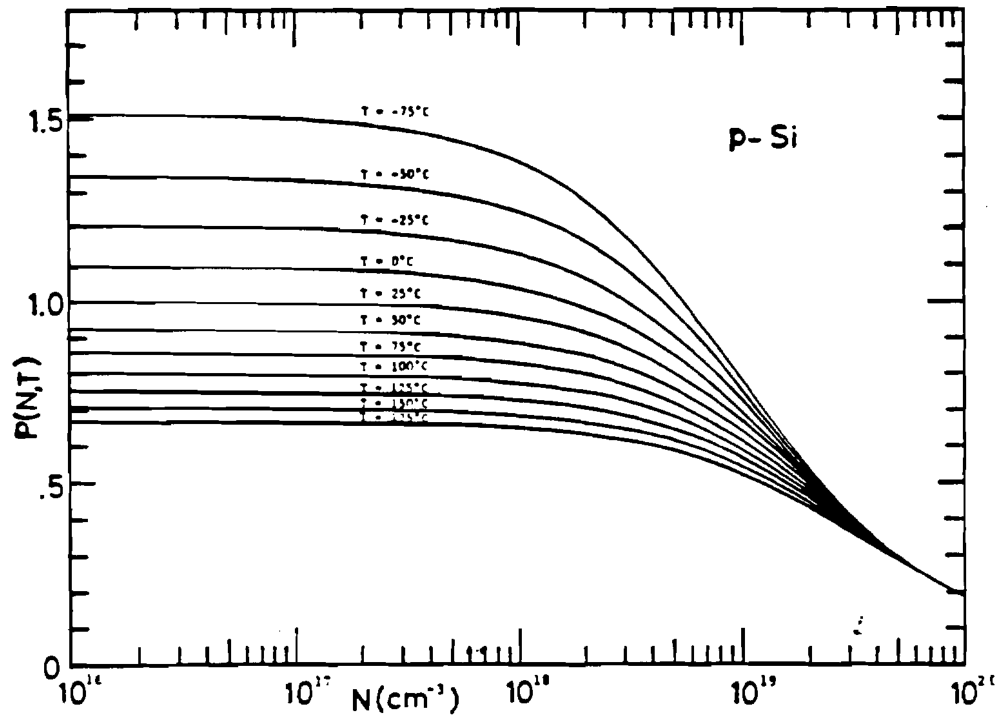


(a)



(b)

Figure 2.8 Theoretical piezoresistance coefficient in n- and p-type (100) silicon [26]: (a) Graphical representation of piezoresistance coefficients in the (100) plane of p-Si ($10^{-12}cm^2$/dyne). (b) Graphical representation of piezoresistance coefficients in the (100) plane of n-Si ($10^{-12}cm^2$/dyne).



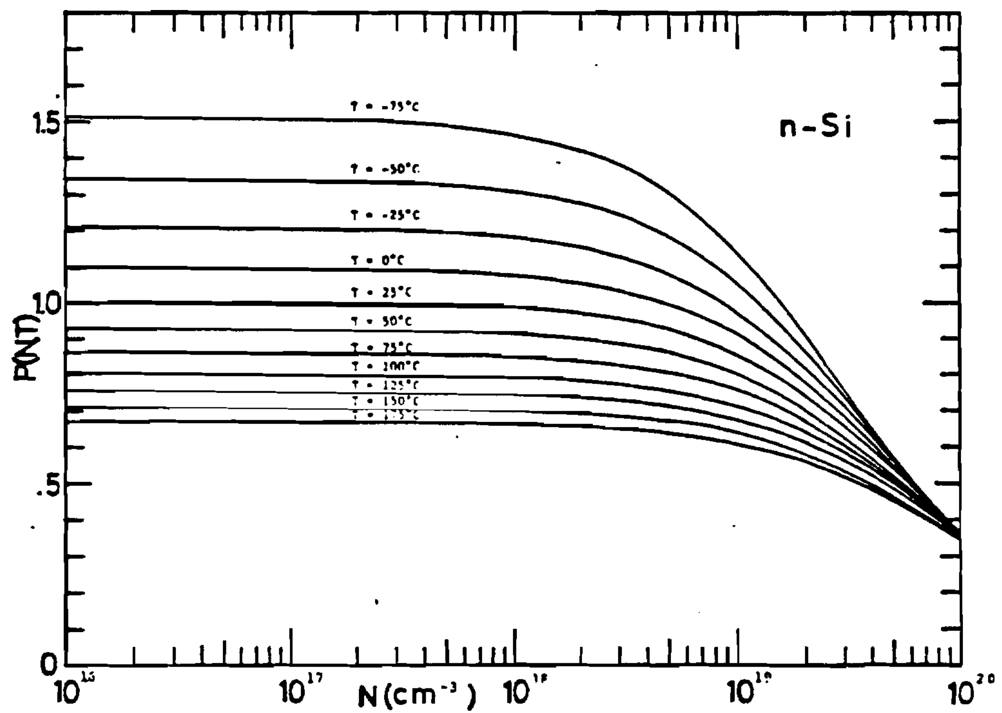


Figure 2.9 Piezoresistance factor, P(N,T), in the theoretical piezoresistance coefficient in n- and p-type (100) silicon [26]: (a) Piezoresistance factor P(N,T) as a function of impurity concentration and temperature for p-Si. (b) Piezoresistance factor P(N,T) as a function of impurity concentration and temperature for n-Si.

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CHAPTER 3
PROPOSED SILICON DIAPHRAGM FABRICATION

3.1 Introduction

A basic requirement in silicon sensor fabrication is the formation of three dimensional shapes in silicon. Particularly a thin silicon diaphragm has been one of the most frequently employed as a stress magnifying structure in micromechanical sensors. Accelerometers and pressure sensors, two most popular examples of integrated silicon sensors, utilize a thin silicon diaphragm structure. One of the key issues in the development of the silicon micromechanical sensor has been the controllability and reproducibility of an IC compatible silicon diaphragm with a good material quality. This chapter reviews existing silicon diaphragm control and monitoring techniques. It also presents a new silicon diaphragm fabrication technique using MELO-Si technology combined with an SiO_2 etch-stop and a crystallographic self-limiting etch-stop. This technique resulted in a high-quality silicon diaphragm with well-controlled dimensions and device quality material. The fabrication technique improves the controllability and reproducibility of the silicon diaphragm thickness as compared to existing techniques.

3.2 Silicon Bulk Micromachining

The successful realization of practical integrated sensing structures during the past several years has been due in part to the continuing progress being made in integrated circuit (IC) process technology [1]. More directly it has been the result of the successful development of additional processes specifically required for sensors fabrication [2-4]. The most important process has been silicon micromachining, i.e. selective precision etching of the silicon substrate. This ability to etch silicon, with high accuracy in an IC-compatible batch process has.made silicon solid-state sensors to be realized as commercial products. This section presents current silicon rnicromachining technologies and their characteristics, particularly silicon diaphragm fabrication techniques for application in pressure sensors and accelerometers.

3.2.1 Silicon Anisotropic Etching

Silicon etching can be divided into two categories depending on its directionality: isotropic and anisotropic. Isotropic etchants etch the silicon crystal at the same rate in all directions and makes gently rounded shapes at the edges as shown in Fig. 3.1(a). On the other hand, anisotropic etchants etch silicon at different rates in different directions depending on the crystal orientation, doping concentration, or etching condition. The anisotropic etchants can form well-defined shapes with sharp edges and comers and hence micromachining makes more extensive use of the anisotropic etchants than of the isotropic ones. Figure 3.1(b) and (c) are examples of orientation dependent anisotropic etching on (100) and (110) silicon wafers respectively.

In typical applications of micromechanical sensors, the silicon wafer must be selectively thinned from a starting thickness of 300-500μm to form a diaphragm or thin beam having a thickness of 5-30μm with well-controlled vertical and lateral dimensions. This was quite difficult to achieve accurately with isotropic etchants, but became much more possible with the development of anisotropic etchants such as potassium hydroxide (KOH) [5], hydrazine [6, 7], and ethylenediamine pyrocatechol [8, 9]. All of these anisotropic etchants, which are also known as orientation-dependent or crystallographic etchants, etch at different rates in different directions in the crystal lattice. All of them attack the {100) planes at typically 1-2μm/min, depending on the temperature, but attack the {110) and the {111) planes at a considerably slower rates. More specifically the order of the etch rate follows (211)-(100)-(110)-(331)-(111}, highest along the (211) plane and the lowest along {111) planes [lo-121.

The precise mechanisms underlying the nature of chemical anisotropic (or orientation-dependent) etches are not yet well understood. Since (111) silicon surfaces exhibit the highest density of atoms per unit area, it has been inferred that this density variation is responsible for anisotropic etching behavior. In particular, the screening action of attached H_2O molecules, which is more effective at higher densities, i.e. on (111) surfaces, decreases the interaction of the surface with the active molecules. This screening effect has also been used to explain the slower oxidation rate of (111) silicon wafers over (100). Another factor involved in the etch-rate differential is the energy needed to remove an atom from the surface. Since (100) surface atoms have two dangling bonds on each, while (111) surfaces have only one dangling bond, (111) surfaces are again expected to etch more slowly. On the other hand, the differences in bond densities and the energies required to remove surface atoms do not differ by much more than a factor of two among the various planes. Hence it is difficult to use these factors alone to explain etch rate

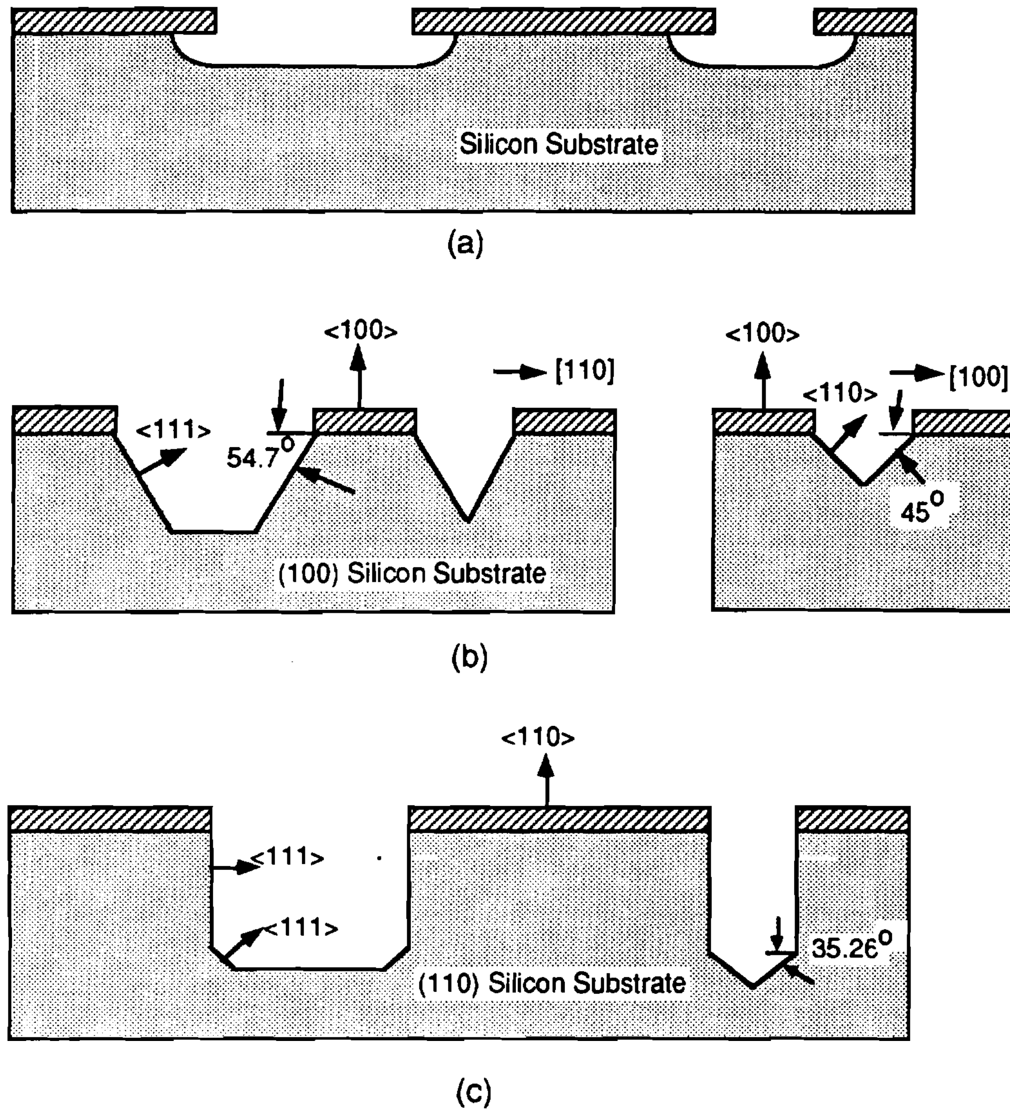


Figure 3.1 Typical wet etching techniques which are commonly used in micromachining. (a) Isotropic etching. (b) Anisotropic etching on (100) silicon substrate with oxide pattern aligned to either <110> or <100> directions. (c) Anisotropic etching on (1 10) silicon substrate with <110> oxide pattern orientation.

differentials in the range of 100 or more, which is maintained over a relatively large temperature range. This implies that some screening effects must also play a role. It appears that the full explanation of orientation-dependent etching behavior is a combination of all the above factors [3].

3.2.2 Present Silicon Diaphragm Fabrication Technology

A thin silicon diaphragm, which is one of the most important structures for silicon micromechanical sensors, can be formed by using one of the previously mentioned anisotropic etchants and using a suitable etch-stop technique. The silicon diaphragm thickness control is dependent on how accurately these etch-stop techniques can terminate etching. Controlling the diaphragm thickness is crucial in silicon micromechanical sensor technology as it will dictate the proper performance of the sensors, in particular its sensitivity is inversely proportional to the square of the diaphragm and beam thickness of pressure sensor and accelerometer respectively. Some of the common techniques for diaphragms formation for micromechanical sensor applications are discussed in the following sections.

3.2.2.1 Time-Controled Etch-Stop

This is the simplest etch-stop technique, in which the etching is stopped just short of what it would take to etch through a wafer. It is a very crude method and hence causes a large variation in the resultant diaphragm thickness because of the thickness variation across a wafer and/or between wafers. Also, a slight difference in etching rate, depending on temperature and the composition of the etching solution, can make a large difference after a long etching time. This method can be used for a quick rough estimates of the etched cavity depth.

The time-controlled etch technique can be improved by diaphragm thickness monitoring techniques such as the V-groove technique shown in Fig. 3.2(a) [13]. This monitoring technique makes use of the property that the etch rate for the (111) planes is negligible. When the mask, SiO_2 or Si_3N_4, is aligned with the <110> direction on (100) silicon, two (111) sidewalls meet during the etching of the (100) plane and the subsequent etching virtually stops by forming a V-shaped groove. Since the angle between (111) plane and (100) plane is 54.74°, the mask width of this V-groove is about 1.4 times the depth of the groove. If a series of lines of different widths are patterned on the front side of the

wafer and a corresponding diaphragm pattern is defined on the back, then a series of V-grooves of different depths are produced on the front and the bottom of some V-grooves will meet the back etching. By monitoring the V-groove with the desired depth to be opened, etching can be terminated and the diaphragm thickness is determined. Although the degree of mask undercutting is ideally none, the mask undercutting becomes considerable in actual processing of long etching and causes the thickness variation (>5μm) across a wafer resulting low yields [14]. For thin diaphragms, this becomes a serious problem.

3.2.2.2 Boron Etch-Stop

During early 1970's, it has been observed that the anisotropic etchants etch a silicon wafer at different rates depending not only on crystal orientation but also on the impurity concentrations. Particularly, the etch rate of p-type silicon by EDP etchant falls as the boron doping level in silicon increases above $10^{18}cm^{-3}$ and reaches effectively zero at $5x10^{19}cm^{-3}$ [12, 15]. Also the etch rate by KOH etchant was shown to be about 0.3 μm/min. for $N_A = 5x10^{19}cm^{-3}$ and down to 0.02μm/min. for $N_A = 10^{20}cm^{-3}$ [5].

Although the boron etch-stop behavior has not yet been adequately explained, several mechanisms have been suggested. The atomic concentrations at these doping levels correspond to an average separation between boron atoms of 20-25Å, which is also near the solid solubility limit ($5x10^{19}cm^{-3}$) for boron substitutionally introduced into the silicon lattice. Silicon doped with boron is placed under tension as the smaller boron atom enters the lattice substitutionally, thereby creating a local tensile stress field. At high boron concentrations, the tensile forces became so large that it is more energetically favorable for the excess boron (above $5x10^{19}cm^{-3}$) to enter interstitial sites. Presumably, the strong B-Si bond tends to bind the lattice more rigidly, increasing the energy required to remove a silicon atom high enough to stop etching altogether. Alternatively, in KOH and EDP etchants, high enough surface concentrations of boron, converted to boron oxides and hydroxides in an intermediate chemical reaction, would passivate the surface and prevent further dissolution of the silicon [3]. Making use of this fact, the boron etch-stop was developed during the 1970s [15, 16].

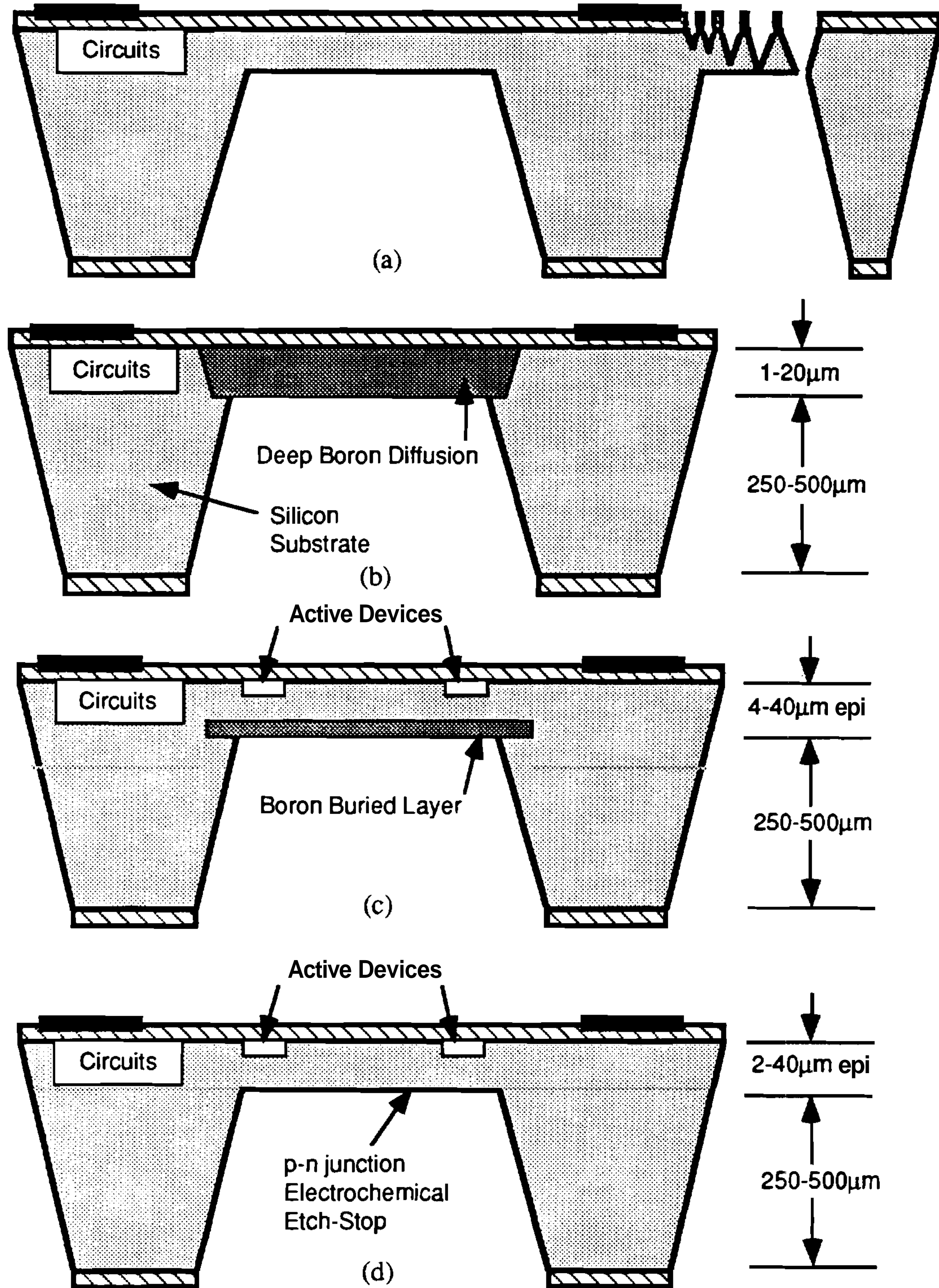


Figure 3.2 Present etch-stop techniques for fabricating a thin silicon diaphragm. (a) V-groove etch-stop. (b) Boron diffusion etch-stop. (c) Boron buried layer etch-stop. (d) P-N junction etch-stop.

The boron doping concentration of $5x10^{19}cm^{-3}$ or higher can be introduced by a simple diffusion or ion implantation for an etch-stop in order to fabricate a thin diaphragm as illustrated in Fig. 3.2(b). This etch-stop technique, called boron diffusion etch-stop, is quite simple and finds many applications in fabricating various thin structures like cantilever beams, bridges, diaphragms, and microprobes [4]. However, the drawback of this technology is that the doping level of the silicon diaphragm is too high to allow the formation of electronic devices within it, and hence it was not appropriate for fabricating piezoresistive silicon sensors.

As an alternative, the boron buried layer can be placed underneath an epitaxial layer which can be more lightly doped and suitable for devices, as shown in Fig. 3.2(c). With a heavily doped p^+ layer formed between lightly doped substrate and epi-layer, when the silicon is etched from the backside to form diaphragms, the etching rate will significantly decrease and will practically stop when the buried layer, with N_A concentration greater than $5x10^{19}cm^{-3}$, is exposed. However, this technique has its own limitations which are as follows. First, the concentration of boron in silicon required to stop etching is so large that the resultant lattice strain is greater than the maximum that the silicon lattice can accommodate without the formation of defects [10, 17, 18]. For thicker diaphragms (2 25μm) these defects do not severely affect the device performance but in the case of thin diaphragms they result in adverse effects. Also, a tensile stress is created through the thickness of the diffusion layer because the boron distribution is non-uniform and because the atomic radius of boron (0.88Å) is smaller than that of silicon (1.17Å). This non-uniform tensile stress causes plastic deformation of thin diaphragms [19-21], and puts a severe limitation on its use as a stress sensitive membrane. Therefore, fabrication of sensitive (or thinner) diaphragms with good quality single crystal silicon is very difficult. Secondly, the out-diffusion of boron from the heavily doped p^+ buried layer into the lightly doped n-type epi-layer, as well as into the substrate, during epi-layer growth and further high temperature steps changes the diaphragm epitaxial doping level. Also, if the out-diffusion is such that the peak buried-layer doping level falls below the critical value of $5x10^{19}cm^{-3}$, the etch-stop will be perturbed, resulting in the loss of thickness control during etching.

3.2.2.3 P-N Junction Etch-Stop

Another etch-stop technique, the electrochemical etch-stop, has been developed since its first introduction by Waggener [22] in 1970. He observed that either n- or p-type

silicon can be selectively removed from material of opposite conductivity when they are properly biased in a KOH solution, which is an electrochemically controlled silicon thinning method. At the same time, Meek [23] reported that n+-type silicon can be dissolved while n-type silicon is not when they are properly biased in a HF solution. Recently, Jackson et al. [24] presented a similar result obtained with EDP solution.

This technique combines the well known anodic passivation characteristics of silicon [25, 26] with a reverse-biased p-n junction to provide an etching selectivity of p-type silicon over n-type in anisotropic etches such as KOH and EDP. With a sufficient potential applied to the silicon, silicon passivates electrochemically as a result of anodic oxide formation and the silicon ceases to dissolve resulting in the structure in Fig. 3.2(d). This potential is defined as the passivation potential. This effect can be used to produce self-limited semiconductor etch by selectively passivating a thin silicon surface layer (n-type epitaxial layer) of the semiconductor by maintaining it at a potential above the passivation potential while the bulk of the semicanductor (p-type substrate) is at a potential below the passivation potential. The etching apparatus is illustrated in Fig. 3.3. Ohmic contact to the entire top surface of the n-type epitaxial layer is made and a positive potential slightly greater than the passivation potential is applied between it and cathode. Since the passivation potential applied to the n-type layer is positive relative to the cathode, the p-n junction is reverse biased and the majority of the potential drop is across the p-n junction. Therefore, the p-type silicon remains essentially at open circuit potential and its relative potential to the cathode is less than the passivation potential, resulting in its etching. With the complete removal of the p-type silicon, the diode is destroyed and the n-type silicon becomes directly exposed to the etchant. Since the potential of the n-type silicon relative to the cathode is equal to or greated than the passivation potential, etching terminates and leaves the n-type epitaxial layer. Therefore, the microstructure morphology is determined by the definition of the n-type silicon under anodic bias [10, 17, 24, 27, 28].

The silicon diaphragms produced by this technique have excellent crystalline and electrical quality as they are lightly doped. In addition, unlike the boron etch-stop technique, there is no heavy boron diffusion involved at high temperature, hence reducing the problems concerning built-in stress and outdiffusion. A recent reported thickness variation of the membranes in this technique is excellent ($\approx$2%) [27]. However, the requirement of individual wafer contact during etching hinders its use in large batch fabrication processes. Also the membranes produced using this technique tend to become thicker at the center than at the edges. This trench effect was describe by Palik et al. [28]. For practical implementation of this technique, it is very difficult to make and protect good

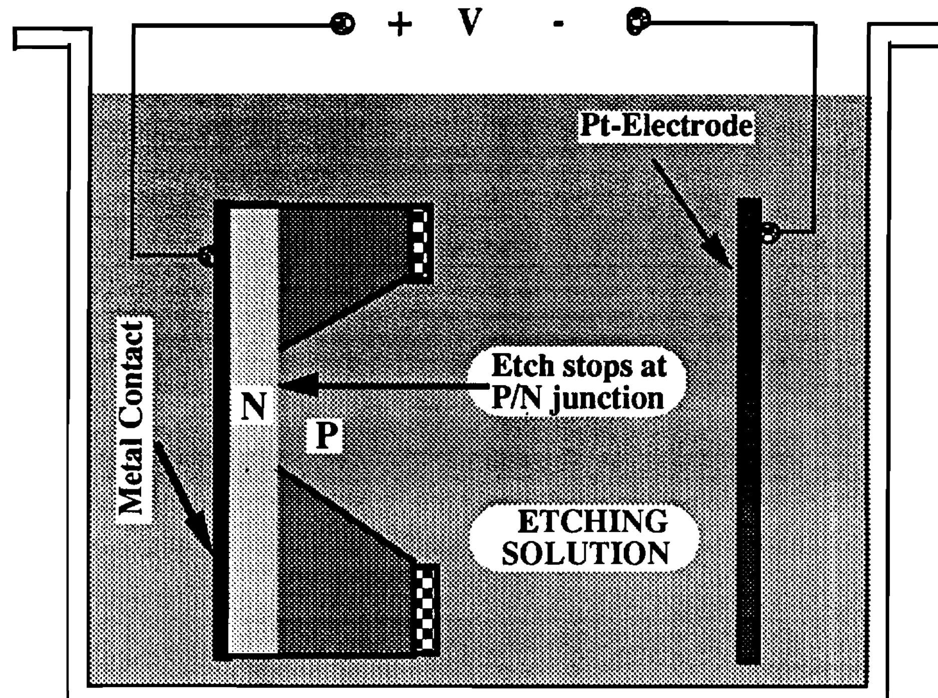


Figure 3.3 A schematic illustration of the P-N junction electrochemical etch-stop.

electrical contacts to the wafers to be passivated from the highly corrosive etching solutions at higher temperatures (60°C-120°C). Special apparatus may need to be invented for good passivation because protecting the contact metal by existing passivation techniques is very difficult during the required long back-side etch and it will make this process expensive to mass produce.

3.2.2.4 Wafer Bonding and Etch Back

The capability of bonding the silicon wafer became an important part of silicon micromechanical sensor fabrication. Starting with glass-to-silicon bonding with a glue for producing a sealed cavity [29], various wafer bonding processes have been developed including eutectic bonding, anodic bonding, field-assisted bonding, and silicon fusion bonding. Among those above bonding techniques, silicon fusion bonding technique is the most recently developed technique and it provides some advantages over the other bonding techniques. Silicon fusion bonding fuses silicon wafers together at the atomic level without the need for a 'glue' layer or an applied electric field [30, 31]. Figure 3.4 shows the

processing steps in this technique. The bottom constraint substrate is first anisotropically etched to define the dimensions of the membrane. A second silicon wafer with a lightly doped epitaxial layer is brought into face-to-face contact with the substrate wafer. The resulting wafer sandwich is annealed at 1100°C for a long time without external force. This bonds the two wafers together mechanically. A doping-selective silicon etch, again through most of the wafer, removes all of the capping wafer, leaving the epitaxial layer. This process can overcome some of the problems faced by other techniques such as thermal expansion mismatches, fatigue, and creep of the bonding layer, complex and difficult assembly methods, unreliable bonds, and the large expense of same processes

However, the wafer bonding and etch-back technique has some drawbacks associated with it. The doping-selective silicon etching uses solutions that are similar to a Dash [32] defect etch solution which composed of 1 part of HF to three parts HNO_3 to ten parts glacial acetic acid. The etch solution has 2 more parts of glacial acetic acid than the Dash defect etch. Therefore, the lightly doped epitaxial layer must be absolutely defect free, otherwise any crystallographic defects in the layer will rapidly dissolve, resulting in large irregular holes in the membrane. It is very difficult to grow a lightly doped epitaxial layer from a heavily doped substrate wafer without any dislocation faults. Even under the best conditions, 10-15% thickness variation occurs in a membrane 3pm thick [17]. Also the membrane using this doping-selective etching tends to have etch pits. An alternative way of thinning the bonded wafer could be the use of chemical mechanical polishing. Since the present silicon fusion bonding scheme can not provide any local etch-stops during the planarization, the membrane thickness variations will still be a major problem in the wafer bonding and etch back process.

Four etch-stop techniques can be compared in several areas: diaphragm film quality, diaphragm thickness control, ease of etch-stop utilization, and suitability for circuit fabrication. Table 3.1 illustrates this comparison.

3.3 MELO-Si Technology for Silicon Diaphragm Fabrication

In this section, a novel silicon diaphragm fabrication technique utilizing merged epitaxial lateral overgrowth of silicon (MELO-Si) and SiO_2 etch-stop is presented. Single crystal silicon can grow from the patterned seed regions of an oxidized wafer, first selectively only from the open seed regions (SEG) and then laterally over the oxide pattern (ELO) as well as vertically. Two laterally grown silicon fronts from opposite sides of an

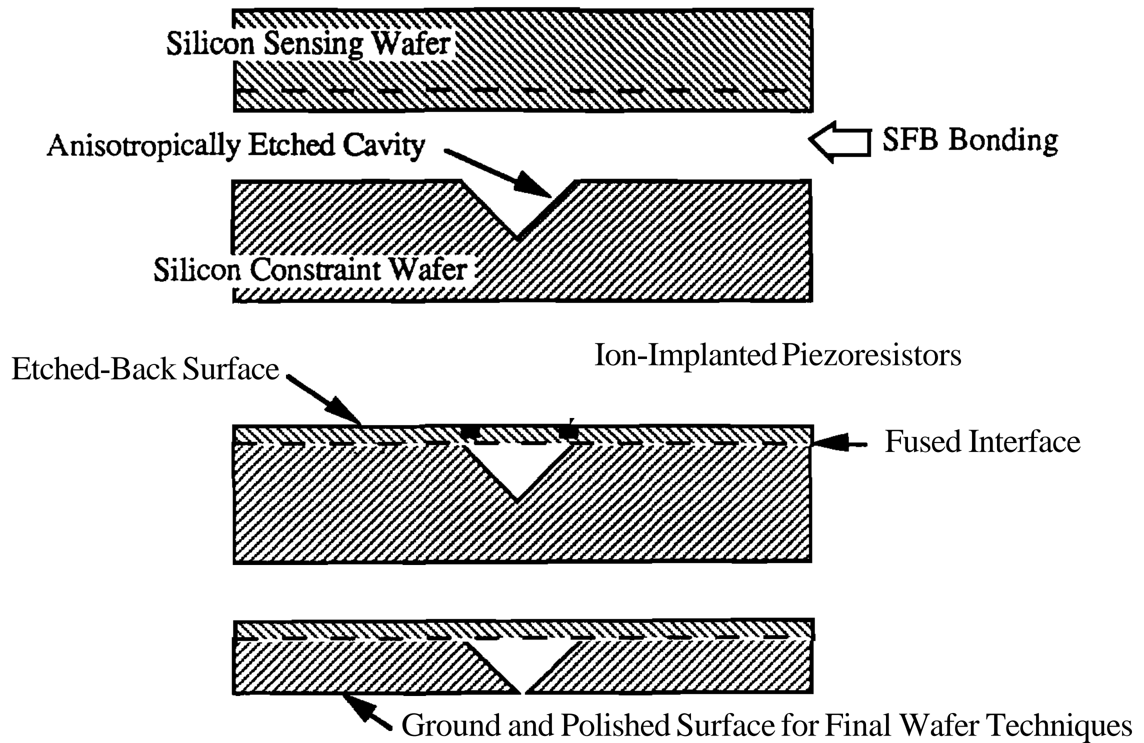


Figure 3.4 Fabrication process of silicon fusion bonding for a low pressure sensor [30].

Table 3.1 Comparison of the four different etch-stop methods as applied to thin silicon diaphragm fabrication.

Etch-Stop Method	Diaphragm Fabrication	Thickness Controllability	Remarks
V-grooves	Series of V-grooves	Fair	Large Error (≥5μm) for a long etching
Boron Diffused	Heavy Boron Deep Diffusion	Good	Too High Doping Conc. for Device Fabrication
Boron Buried	Epi-Layer on Boron Buried Layer	Good	High Defect Density in Epi-Layer
Electrochemical p-n Junction	P/N or N/P Epi-Layer	Excellent	Complicated, Inconvenient Apparatus

oxide pattern will meet on the oxide layer and forms a local silicon-on-insulator (SOI) structure as shown in Fig. 3.5(a). This local SOI structure can provide several advantages in silicon micromechanical sensor applications over other silicon micromachining techniques. First, SiO_2 is a virtually perfect etch-stop when EDP or KOH etchant is used for etching. Hence the epitaxial silicon on the SiO_2 pattern is completely protected from etching as shown in Fig. 3.5(b). Secondly, the thickness of the silicon diaphragm can be controlled more accurately than the boron etch-stop techniques since it is controlled by the ELO growth rate which is approximately 0.1μm/min or less. The growth rate can be adjusted by the amount of source gas, hydrogen, HCl, and temperature of the silicon epitaxy reactor. Thirdly, the laterally overgrown epitaxial silicon (ELO-Si) film is of good quality and hence fabrication of devices, including piezoresistors, is possible in ELO-Si. Finally, the complex apparatus, which is necessary for the electrochemical p-n junction etch-stop, can be eliminated since the etching procedure is very simple.

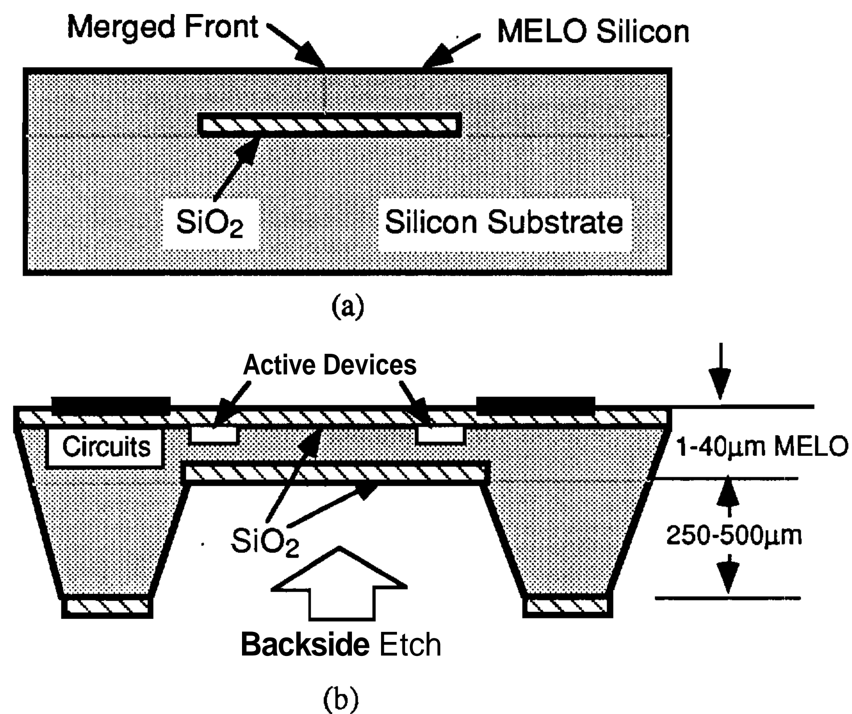


Figure 3.5 A schematic illustration of a novel silicon diaphragm fabrication technique. (a) MELO silicon fabricated on silicon dioxide. (b) Silicon diaphragm produced by SiO_2 etch-stop.

3.3.1 Silicon Epitaxy

The fundamentals of silicon selective epitaxy, effect of process parameters, and the experimental results of the MELO-Si structure are described in this section since silicon selective epitaxy plays an important role in the new diaphragm fabrication technology. The word 'epitaxy' is derived from the Greek words 'epi'(on) and 'taxis'(arrangement). In semiconductor technology, epitaxy refers to the growth of a single crystal semiconductor upon a single crystal substrate. When the grown material and substrate are of the same type, the growth is referred to as 'homoepitaxy', and when they are of different type, the growth is referred to as 'heteroepitaxy' [33]. The substrate acts as a seed crystal and the source of the growing crystal is provided externally. Epitaxy can be divided into four categories depending on the state of the source supplied; vapor phase epitaxy (VPE), liquid phase epitaxy (LPE), solid phase epitaxy (SPE), and molecular beam epitaxy (MBE). VPE is the most common form of epitaxy and utilized in conventional full-wafer silicon epitaxy.

Silicon epitaxy is to grow a single crystal silicon layer upon a single crystal silicon substrate. Silicon epitaxial growth has been developed and widely used in device fabrication processes such as bipolar [34], MOS [35-37], discrete power devices, and CCD technology [38-40]. Silicon epitaxy can be achieved in various systerns, among which chemical vapor deposition (CVD) is by far the most important. Silicon CVD has been accomplished with four different source gases; silane (SiH_4), dichlorosilane (SiH_2Cl_2), trichlorosilane ($SiHCl_3$), and silicon tetrachlorine ($SiCl_4$).

3.3.1.1 Fundamentals of Epitaxy

CVD epitaxy of silicon film can be represented as shown in Fig. 3.6 [41]. There are five basic steps involved; (1) the transport (or diffusion) of reactants to substrate through the carrier gas, (2) the adsorption of reactants to the substrate surface, (3) the chemical reaction on the surface resulting in the film formation and the reaction products, (4) the desorption of the reaction products from the surface, (5) the transport of the reaction products from the surface.

A simple model developed by Grove [42] is often used to study the kinetics of epitaxial film growth. This model is based on only steps (1) and (3) above but it forms the basis of epitaxy. There are two fluxes F_1 and F_2 associated with steps (1) and (3) respectively. Assume the flux F_1 can be written as being linearly proportional to the difference in the concentration of the gas species at the surface and in the medium away from the surface. Then it can be written as,

$$F_1 = h_g (C_g - C_s) = (D_g, \delta) (C_g - C_s) \quad (3.3.1)$$

where C_g and C, are he concentration of the reactant species in the bulk of the gas and surface of the substrate respectively, and h_g is the gas phase mass transfer coefficient. h_g can be expressed as a ratio of the effective diffusion constant, D_g, to the distance *6*, called stagnant film region, over which diffusion takes place. Defining h_g as such is called the stagnant film model and then the above equation is essentially an expression of Fick's first law. In the stagnant film region, it is assumed that the gas velocity is zero and the transport is diffusion limited. This model of F_1 shows a good approximation even though in reality the stagnant film region is different from the definition.

The flux F_2 is assumed to be linearly proportional to C, and it can be expressed as,

$$F_2 = K_s C_s \quad (3.3.2)$$

where K, is the surface reaction rate constant controlling the first order kinetics. At steady state, $F_1 = F_2 = F$, and thus

$$C_s = \frac{C_g}{1 + \frac{K_s}{h_g}} \, . \quad (3.3.3)$$

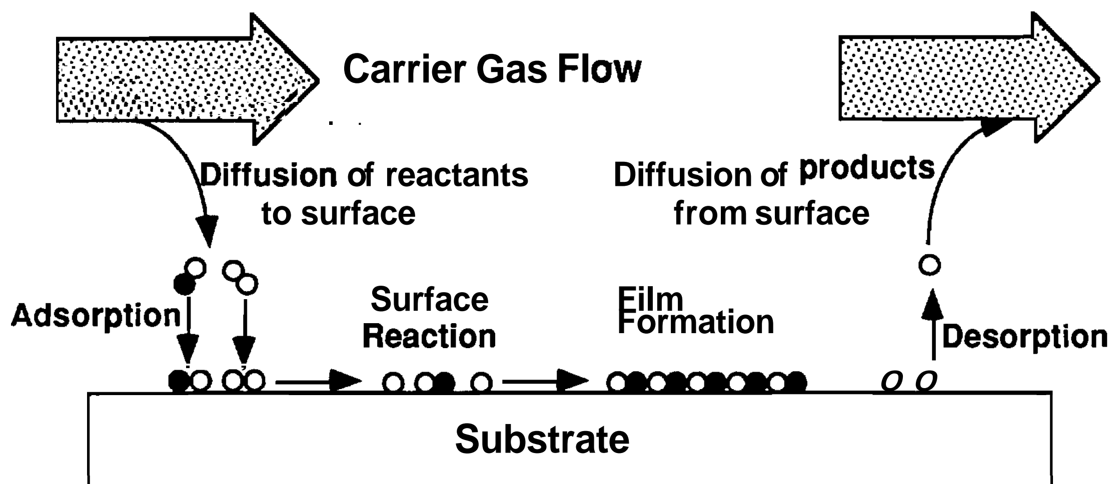


Figure 3.6 Schematic of CVD reaction steps [41].

The growth rate, GR, is given by the ratio of the flux to the number of atoms per unit volume incorporated into the crystal, N_i, which is $5x10^{22}/cm^3$ for silicon. Since C_g = YC,, where Y is the mole.fraction of the reactant species and C_t is the total number of molecules per unit volume in the gas, the expression for the growth rate becomes

$$GR = \frac{F}{N_i} = \frac{K_s h_g}{K_s + h_g}\left[\frac{C_g}{N_i}\right] = \frac{K_s h_g}{K_s + h_g}\left[\frac{C_t}{N_i}\right] Y. \qquad (3.3.4)$$

According to Eqn.(3.3.4), the growth rate is proportional to the mole fraction of the reactant species, Y. The growth rate at a given mole fraction is determined by the smaller value between K_s and h_g, which correspond to the limiting cases of mass-transfer controlled and surface reaction controlled conditions. In these two cases, the growth rates can be expressed as,

$$GR = K_s \text{ — } Y \quad \text{[surface reaction-controlled]} \qquad (3.3.5)$$

or

$$GR = h_g\left[\frac{C_t}{N_i}\right] Y \quad \text{[mass transfer-controlled]} \qquad (3.3.6)$$

This simplified model neglects the flux of reaction products and assumes a linear proportionality of the growth rate to the mole fraction of the reactant species, which is true only for low mole fractions of the reactant species. As an example, for silicon epitaxy, one of the reaction products is HCl which starts to etch the silicon as its mole fraction increases. Therefore, the linear approximation of this model deviates from the experimental results because the reaction products were not considered.

The temperature dependence of silicon epitaxy growth rates for various silicon gas sources is shown in Fig. 3.7 [43]. Here h_g is relatively temperature independent and hence the growth rate is more temperature dependent in the surface reaction region than in the mass transfer controlled region. At higher temperatures, in region B, $K_s \gg h_g$ and the growth rate is limited by mass transfer which is rather temperature independent. At lower temperatures in region A, $K_s \ll h_g$ and the growth rate is surface reaction limited and is dependent exponentially on temperature, i.e. proportional to $\exp(-E_a/kT)$ where E_a is an activation energy.

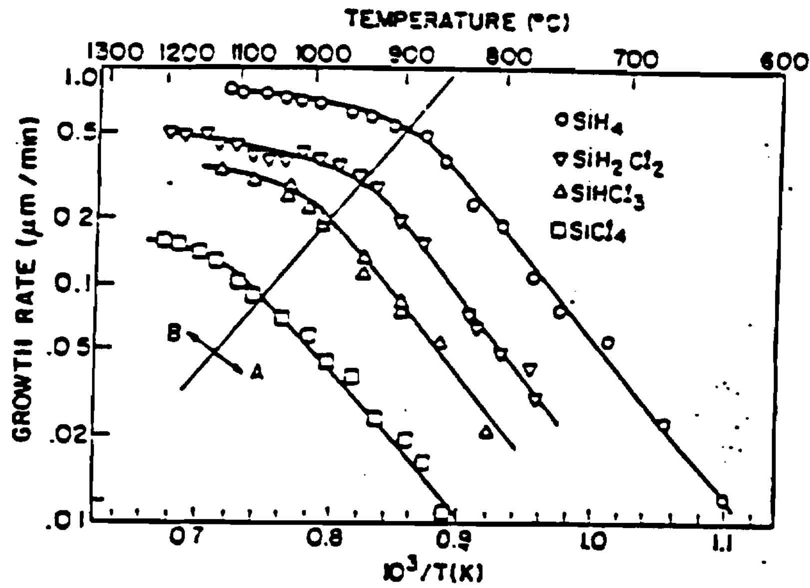


Figure 3.7 Silicon epitaxy growth rate as a function of temperature for various gas sources.

3.3.1.2 Selective Epitaxy

Selective epitaxial growth has been accomplished in a standard commercial low pressure (LP) CVD epitaxial reactor. $SiCl_4$, $SiHCl_3$, SiH_2Cl_2, and SiH_4 are four major gas sources that have been used for silicon selective epitaxy. $SiCl_4$ has been widely used in the past for silicon epitaxial growth because it is chemically stable, has a rather low vapor pressure, and it usually leaves very little silicon coating on the reactor walls. The disadvantage of using $SiCl_4$ is that it requires a high deposition temperature (1100 - 1300°C). The overall reaction is a hydrogen reduction of the gas as,

$$SiCl_4 + 2H_2 \rightarrow Si + 4HCl. \quad (3.3.7)$$

SiH_2Cl_2 and $SiHCl_3$ have similar characteristics to that of $SiCl_4$ except that they can be used at lower deposition temperatures for comparable growth rates and crystal quality. Due to its lower deposition temperature and hence reduced autodoping and diffusion, SiH_2Cl_2 is widely used in low temperature silicon epitaxy. Also, it has been shown that SiH_2Cl_2 has the highest efficiency of the reaction, i.e. the ratio of the amount of deposited silicon to the amount of reactant gas entering the reactor, while $SiCl_4$ has the lowest.

Compared to chlorosilane chemistries, silane (SiH_4) is not widely used for silicon epitaxy even with its lower deposition temperature. The disadvantages of using the SiH_4 are that homogeneous gas phase reactions could occur and no HCl is produced in the decomposition of the silane. SiH_4 is not a stable gas and reduces in the gas phase and forms silica dust which can contaminate the wafers and the reactor walls. The addition of HCl is necessary to maintain growth selectivity over oxide when using SiH_4. Silicon is deposited by the pyrolytic decomposition of SiH_4 as,

$$SiH_4 \rightarrow Si + 2H_2 \qquad (3.3.8)$$

while the reactions using DCS are

$$SiH_2Cl_2 \rightarrow SiCl_2 + H_2 \qquad (3.3.9)$$

$$SiCl_2 + H_2 \rightarrow Si + HCl \qquad (3.3.10)$$

where HCl is a decomposition by-product. HCl prevents the nucleation by etching silicon atoms on the oxide surface by the reaction

$$Si + HCl \rightarrow SiCl_2 + H_2. \qquad (3.3.11)$$

After numerous experiments by several research groups, SiH_2Cl_2 has become the preferred source for selective silicon epitaxy for the following reasons [44]: (1) lower growth temperature, (2) higher conversion rate of silicon, (3) more reduced pressure selective growth, and (4) lower or no nucleation density on the oxide. At Purdue University in the Solid State Epitaxial Laboratory a Gemini-1 pancake-type reactor uses SiH_2Cl_2 as the silicon source.

Maintenance and control of selectivity of the silicon growth on silicon over that on the oxide is the key to selective silicon growth. The nucleation of silicon on a dielectric material like oxide or nitride needs a higher supersaturation than nucleation on a clean silicon surface because the adsorption energy of silicon to the dielectric material is higher. Once the silicon adatoms start to nucleate on the insulator surface they start to form clusters. If the cluster exceeds a critical size (supercritical size), then further growth is favorable. Clusters that are smaller than the critical size do not grow and eventually get etched. Therefore, the nucleation can be reduced by increasing the HCl content which will etch the clusters before they grow above the critical size. Also decreasing the reactor

pressure, which increases the critical size needed for further growth, improves the selectivity. In addition, the onset of nucleation on the mask is a function of temperature, the mask material, and its cleanliness.

3.3.2 SEG, ELO, and MELO

The selective epitaxial growth (SEG) of silicon has brought much attention for small device isolation [45-47] and the development of various novel device structures [48-51]. In SEG, the epitaxial deposition conditions are adjusted to prevent silicon deposition on the mask regions, usually oxide, while epitaxial growth occurs on the exposed silicon in the seed windows as shown in Fig. 3.8(a). Once the silicon grows vertically above the mask level, it then grows laterally over the oxide mask as it continues its vertical growth. This is referred to as epitaxial lateral overgrowth (ELO), and it starts to construct a locally silicon-on-insulator (SOI) structure of Fig. 3.8(b). The epitaxial process can be continued even further until growth fronts seeded from different windows meet, forming a continuous film of silicon, or merged ELO (MELO) illustrated in Fig. 3.8(c). Figure 3.8(d) illustrates a rather unique extension of SEG technology and its structure that is controlled by growing vertically and laterally in a cavity or tunnel consisting of dielectric material walls, which is called confined lateral SEG or CLSEG.

3.3.2.1 Effect of Process Parameters

There are several process conditions to be considered in order to achieve a good quality MELO silicon film, to be used for silicon micromechanical sensors. Since MELO is just a continuation of ELO, the process conditions considered to improve ELO/SEG are also applied to the MELO process. For the SEG and ELO processes, the selectivity of silicon growth is the first concern, i.e. the nucleation of polysilicon on the masking material must be limited. The nucleation depends on the masking material, deposition temperature, pressure, and the carrier gas. It has been found experimentally that nucleation generally occurs less on silicon dioxide than on silicon nitride [52, 53]. In addition, the nucleation can be suppressed by using reduced pressure [54, 55], lowering the deposition temperature [44, 55], and adding HCl gas in the silicon process gas [56, 57].

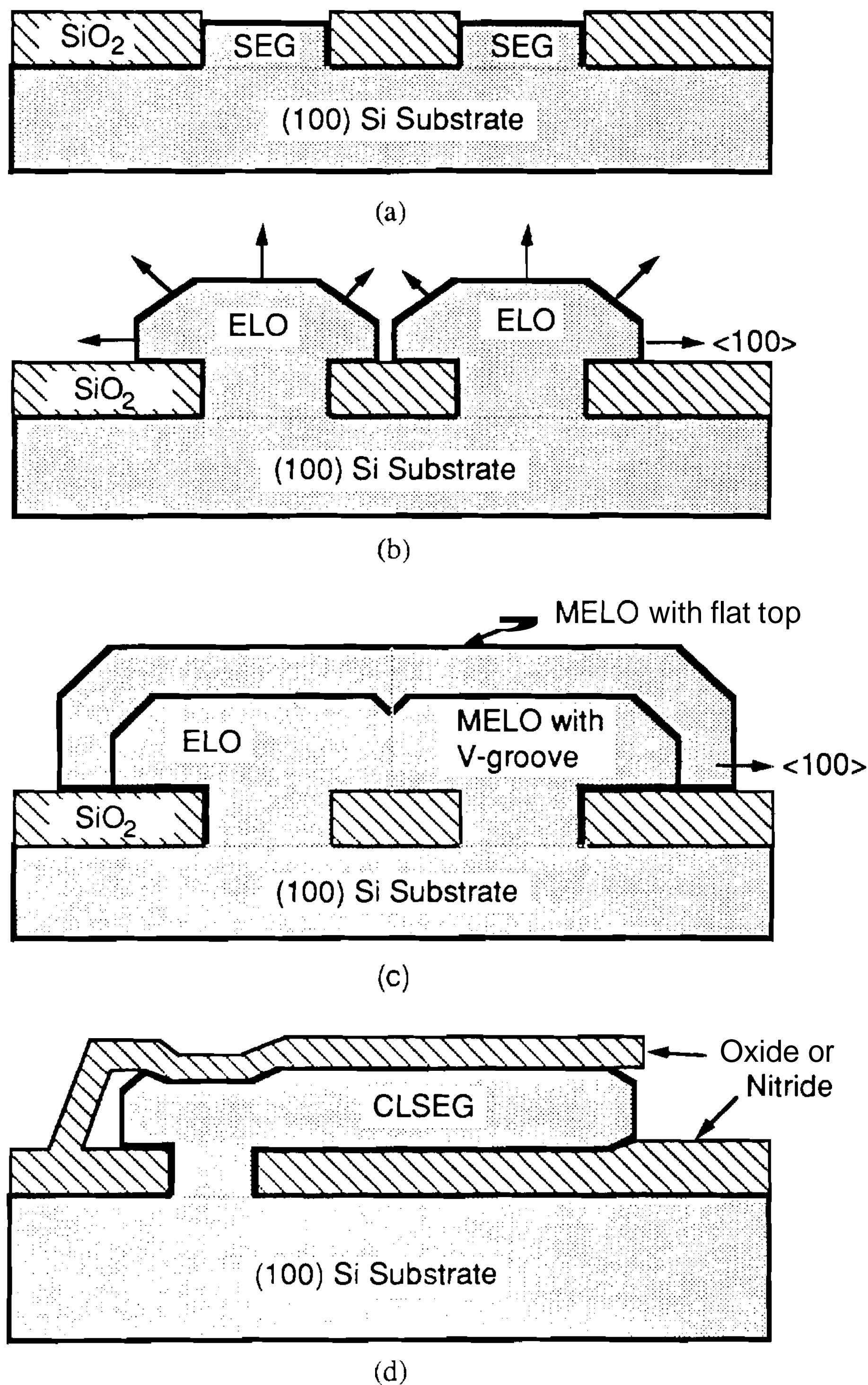


Figure **3.8** (a) Selective epitaxial growth (SEG) of silicon. (b) Epitaxial Lateral overgrowth (ELO). (c) Merged ELO (MELO). **(d)** Confined lateral SEG (CLSEG).

The crystal quality of SEGELO depends on several deposition conditions such as deposition temperature, pressure, seed surface condition, seed orientation, masking material, and contaminants in the reactor. First of all, oxide has been proved to be the better masking material than nitride, since nitride generates more stacking faults along SEG sidewalls than oxide [55, 58]. Also, leakage currents along the SEG/sidewall interfaces are the lowest if the sidewalls are a thick oxide [59, 60]. Therefore, oxide is generally used as the masking material. Typical defects generated by interaction between oxide edges and ELO silicon are edge dislocations and stacking faults [61, 62]. These effects are believed to be a result of the stress relief caused by the difference in the thermal expansion between the silicon and the oxide during the high temperature growth [62]. The density of these defects in SEG/ELO can be reduced by lowering the growth temperature.

The seed window orientation also has an effect on the SEG material quality. Films grown on the seed windows aligned to <110> directions exhibits a higher density of defects than those grown on seed windows aligned to <100> [61, 63-65]. Another important factor in the process is the surface condition of seeds. SEG material grown on (100) substrates shows superior quality to that grown on (111) substrates because of their lower probability of stacking fault nucleation [54]. An in-situ precleaning with hydrogen to remove the substrate's native oxide before epitaxy is critical to SEG material quality. It is believed that H_2 at high temperature acts as a reduction agent and remove:; chemical species that interfere with perfect single crystal formation. Low pressure also enhances the H_2 reduction process by encouraging the removal of other foreign atoms from the surface [47, 66].

The use of HCl also decreases defect density on SEGELO films. However, if too much of HCl is used in the cleaning step, the undercut between silicon and mask may occur [47, 54, 59]. Recently, the effects of water vapor and oxygen levels in the epitaxy environment were investigated [67]. At the same temperature and pressure, the quality of SEG/ELO improves with the reduction of water vapor and oxygen level:in the reactor. It was determined experimentally that the critical temperature, above which deposition of good critical quality epitaxy is possible, is governed by the moisture and oxygen partial pressure during preclean and growth.

The method of etching the masking oxide also affects quality of the SEG material since the sidewall angle of the oxide is related to defect generation at the interface. It was found that the vertical sidewalls tend to yield the best SEG [59]. Wet etching of the oxide never achieves a vertical sidewall due to its isotropic etching characteristics. The anisotropic reactive ion etching (RIE) should ideally create the vertical sidewall, but it often

creates radiation damage to the seed surface, leading to defects in SEG [47]. In order to maintain the vertical sidewalls and to heal the surface damage, RIE followed by a sacrificial oxide, which is then wet etched, is an alternative [59].

Uniformity of SEGELO film on a wafer is quite important for the consistent results between devices from the same wafer. The local growth rate of SEG/ELO can be different depending on the ratio of the exposed silicon seed area to oxide covered area [68, 69]. It appears that growth rates increase locally as the exposed silicon area decreases. This phenomenon can occur on a device scale or wafer scale depending on process conditions. This is called a "loading effect" and is not desirable since it causes non-uniformity in a wafer and even within a die. Loading effects can be reduced at low temperatures [70], at reduced pressure [44], and with higher HCl concentrations during growth [44, 68]. Also, it is less significant at a larger Si/SiO_2 surface ratio [44, 68] where most wafer area is exposed.

The shape of SEGELO films and facet formation are determined by the difference of the growth rates between growing crystal planes. The formation of a facet can be reduced by making seeds oriented along <100> directions [47, 71], lowering the deposition temperature [72], reducing the pressure [45, 55, 59, 73], and increasing HCl concentration [65, 74]. The morphology of SEG films is highly dependent on the orientation of the oxide sidewall with respect to the orientation of the oxide [47, 54]. When the sidewall is parallel to {110} planes, the SEG film typically exhibits {311} facets adjacent to the sidewalls. As the film continues to grow over the oxide, then {111} facets appear on the ELO film as shown in Fig. 3.9(a) [71]. When the sidewall is parallel to {100) planes, less faceting is observed on the SEG and {110) planes are often observed after overgrowth begins as shown in Fig. 3.9(b) [65]. When the oxide mask is thin, sometimes no facet is observed on the SEG film. However, the relationship between oxide thickness and the facet formation is not clear.

Adding HCl, in addition to suppressing polysilicon nucleation on the oxide, changes the growth rate of the {100} planes relatively to that of the (110) planes [65]. A high HCl partial pressure increases the growth rate of the {110) planes with respect to that of the {100) planes so that the slow-growing (100) planes remain to bound the deposit, and vice versa as shown in Fig. 3.10. Controlling the HCl partial pressure during deposition allows the possibility of varying the shape of the ELO growth fronts and consequently obtaining satisfactory coalescence of two growth merging fronts. When a high HCl partial pressure is used, the lateral growth planes become nearly vertical and they may meet together so as to generate a perfect MELO structure without any groove on the

top. However, if they meet first near the upper edge of the vertical {100} planes, they may leave a void below the point where the growth fronts first meet as shown in Fig. 3.10(c). On the other hand, if a lower HCl partial pressure is used, faceted growth fronts with only a small vertical {100} plane will be developed and consequently minimize or eliminate the void when they coalesce. In this case, a V-groove will appear on the top MELO structure and longer epitaxy is necessary to obtain a flat top MELO. The V-groove can be quickly removed by changing the HCl partial pressure after the first meeting of the ELO growth fronts.

For the growth of high quality SEG/ELO material, low temperature, reduced pressures, and addition of HCl in the process gas are generally preferred even though the growth rates are reduced. These conditions give advantages such as: (1) enhanced selectivity, (2) better SEG planarity, (3) fewer stacking faults at the SEG sidewalls, (4) less loading effects, (5) reduced faceting, and (6) fewer crystal defects and nucleations.

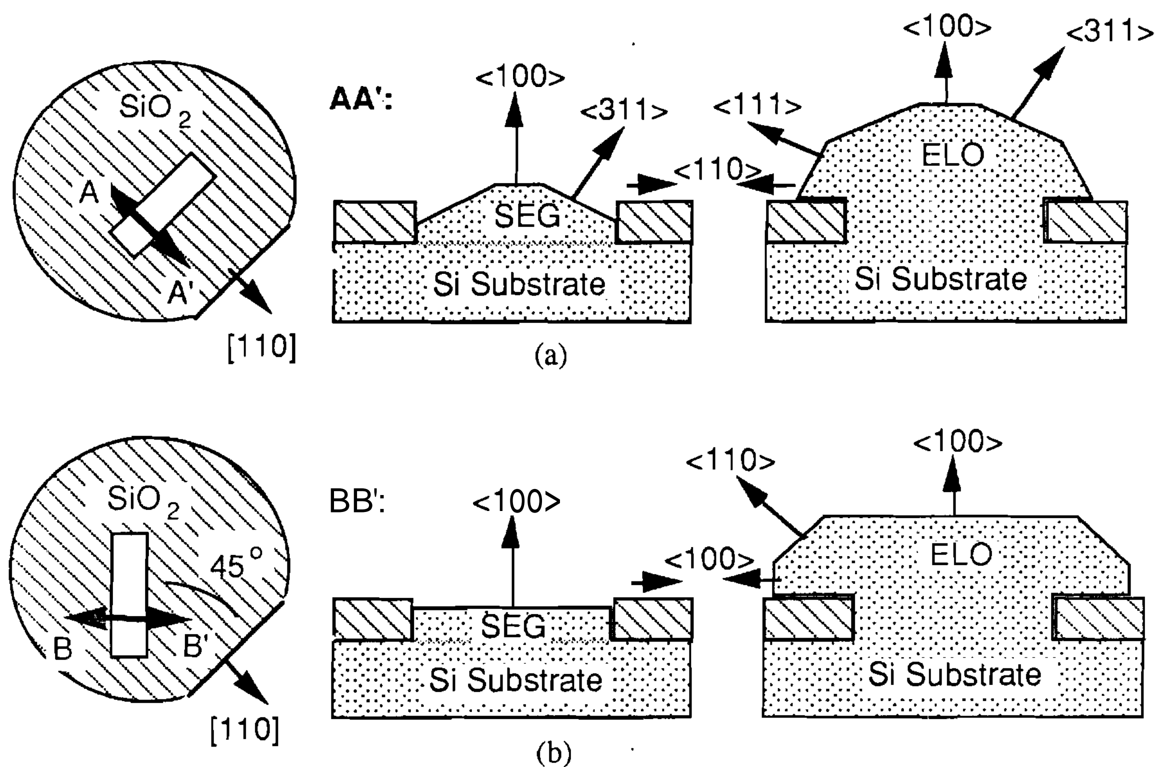


Figure 3.9 Facet formation depending on the seed window orientation [71]. (a) When oxide pattern is aligned to <110> directions. (b) When oxide pattern is aligned to <100> directions.

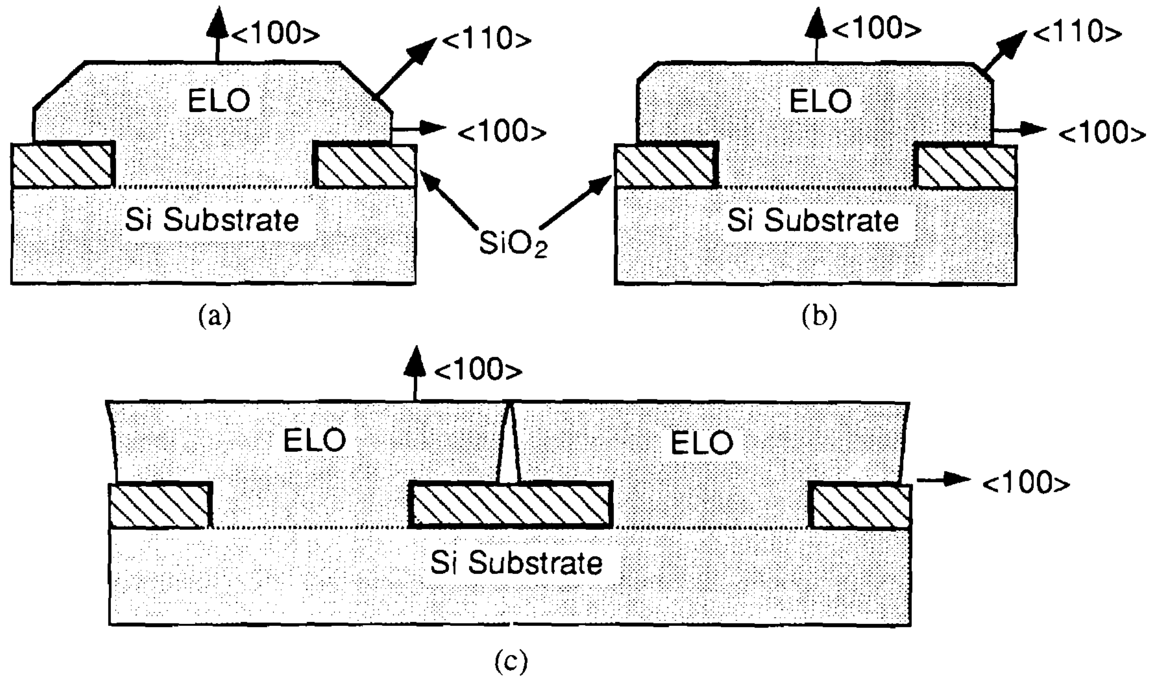


Figure 3.10 Facet formation depending on the HCI partial pressure [65]. (a) With little HCl into the process gas. (b) With more HCl into the process gas. (c) When too much HCI is used, the top of ELO fronts meet first and a void may occur.

3.3.2.2 Initial Experimental Results

The first test mask was designed and implemented to study ELO merging characteristics and to verify the feasibility of the proposed new silicon diaphragm fabrication technique for both small and large beam dimensions of accelerometers. Figure 3.11 illustrates the test mask for MELO and etch-stop experiments. It comprises array of oxide strips with various widths and spacings in order to examine the growth and merging characteristics. Four variations were applied to the seed window width as 1µm, 1.5µm, 2µm, and 3µm. The oxide strips also have four different widths of 5µm, 10µm, 15µm, and 20µm. The oxide strips are made into groups and each group includes strips of four different lengths as 500 µm, 1000µm, 1500µm, and 2000µm. The selected values for seed window widths, oxide widths, and lengths resemble those that would be used in accelerometer beam fabrication. Nine big squares of 250 µm by 250µm and four L-shaped structures are for ELO thickness measurement. They are so large that they won't be completely covered by ELO and the ELO thickness can be measured non-destructively way using a surface profilometer.

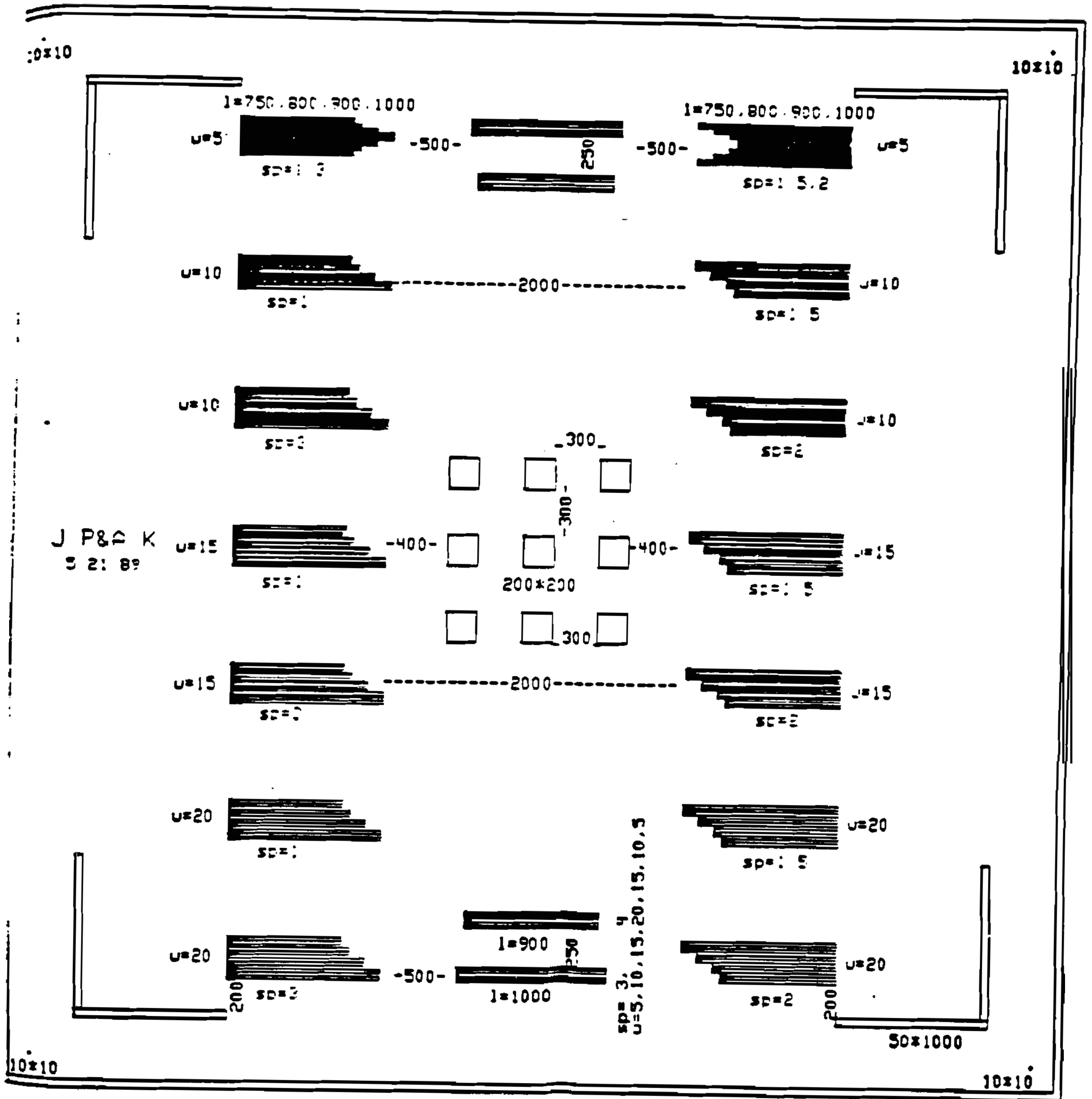
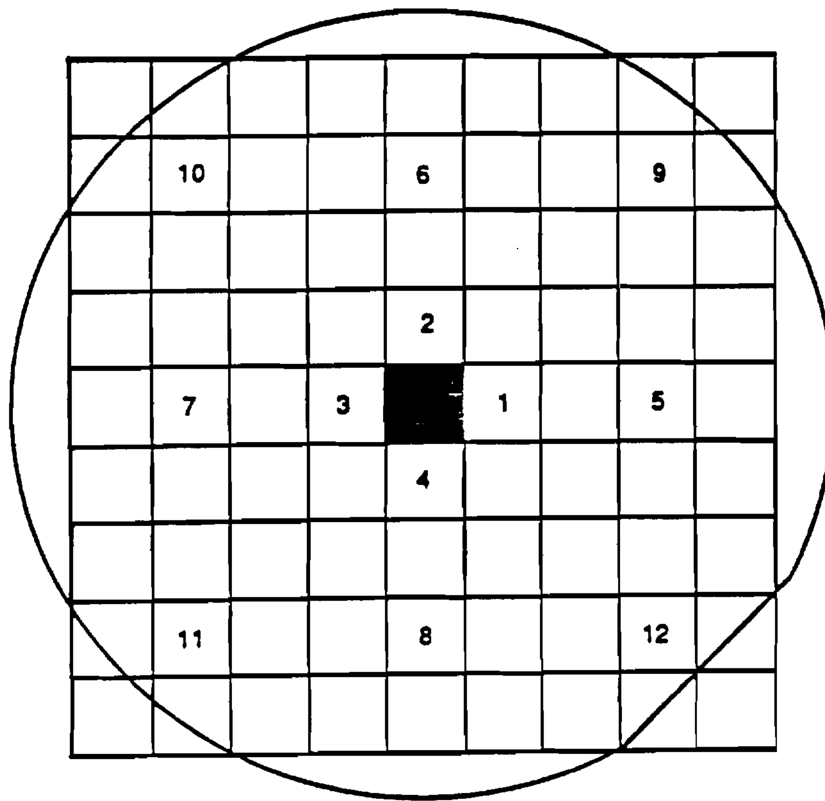


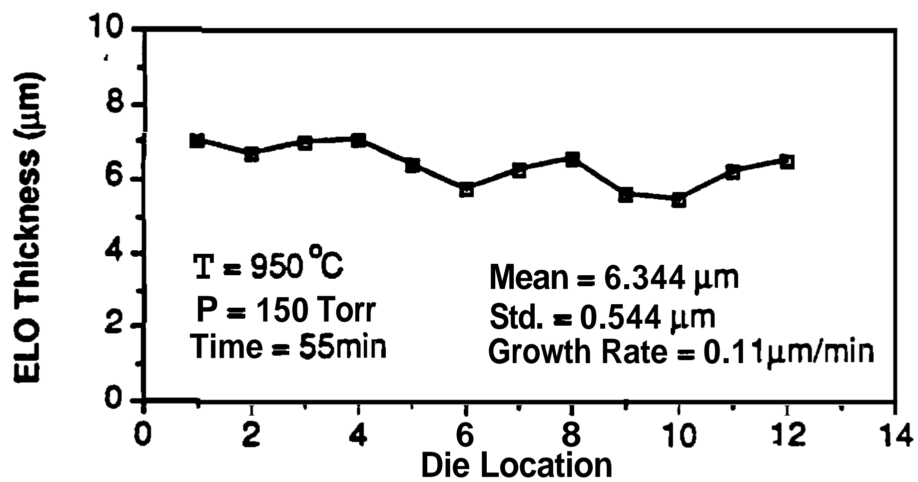
Figure 3.11 The first test mask layout for MELO and etch-stop experiment.

The SEG/ELO experiments started with (100) n-type silicon substrates. The wafers were initially cleaned in a hot $H_2SO_4 + H_2O_2$ solution. After the rinse in deionized (DI) water and blown dry with N_2, they were oxidized in a wet O_2 ambient. Approximately 1500Å of thermal oxide was grown in a steam atmosphere and it was subsequently patterned for opening seed windows. The seed windows were opened by wet etching in buffered hydrogen fluoride (BHF) solution. After patterning the seed windows, the wafers were cleaned again in a hot $H_2SO_4 + H_2O_2$ solution. The wafers were rinsed in DI water and dipped in a BHF solution for 10 seconds to remove any native oxide. Just prior to the silicon epitaxy, the wafers were rinsed very thoroughly in DI water and dried with N_2, since the epitaxial silicon quality is greatly affected by the cleanliness of the wafer. For (100) oriented wafers, the edges of the oxide pattern were placed parallel or perpendicular to the <100> directions, and all wafers were placed in the reactor such that the major flat of the wafers would make 45° to the radial direction of the round reactor susceptor.

Selective growth was carried out in Gemini I LPCVD reactor, an inductively heated pancake reactor, in the Purdue University Solid State Epitaxial Laboratory. After the wafers were placed on the susceptor, the reactor was heated to 950°C, the deposition temperature. Then they were subjected to a 5 minute bake in a hydrogen ambient at 150 Torr or 40 Torr which is the deposition pressure, to remove any remaining native oxide from the wafer surface. Subsequently, HCl was introduced and the substrates were etched for a short time, typically 30 seconds or 1 minute. Thereafter dichlorosilane was added as a silicon source gas to initiate the deposition and HCl gas was added to enhance the selectivity. ELO growth rates of approximately 0.1 µm/min were accomplished. These parameters led to planar SEG with good selectivity and minimum visible defects. The thorough investigation of SEG/ELO parameters of Gemini I LPCVD reactor at Purdue University were previously performed experimentally by Kastelic and Friedrich [75].

For each of the wafers SEG/ELO growth thickness measurements were taken at five positions in each of 12 different dies, as marked in Fig. 3.12(a), using a Tencor Alpha-Step profilometer and averaged for each die. The absolute experimental error for growth measurements using this instrument was estimated to be 10nm. The seed window geometries and locations within each die measured for growth rate comparison were identical. The typical measurement results are shown in Fig. 3.12(b), which resembles the previously reported result [48].





(b)

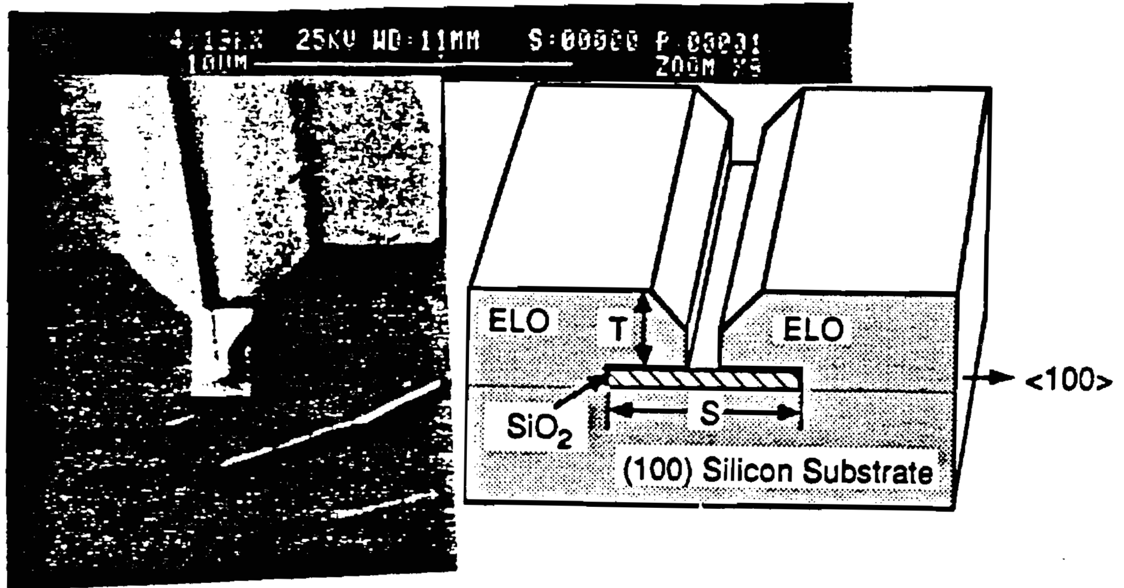
Figure 3.12 (a) The die locations on a wafer for ELO thickness measurement. (b) ELO growth variation over a 3" wafer.

When the ELO fronts start to meet, they form a groove at the top surface due to the facets on the ELO fronts. Fig. 3.13(a) shows a typical morphology of two ELO fronts just prior to merging on the 10μm wide oxide after 4.5μm growth. This V-groove between the growth fronts gets smaller and smaller and finally vanishes as the growth progresses. Therefore, additional growth is necessary to obtain a flat top MELO film even after merging. It has been observed that there is approximately a linear relationship between the total growth thickness needed to merge and form a flat top MELO surface and the seed hole separation as shown in Fig. 3.12(b). Equation (3.3.12) was derived empirically [76], showing these relationships to facet growth rates as

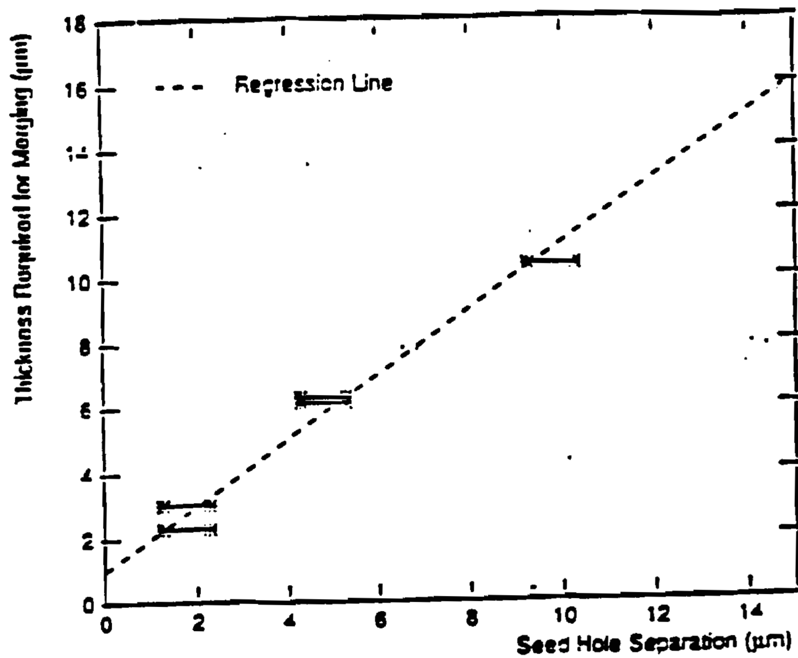
$$T = \frac{S}{2(\sqrt{2}r - 1)} + T_o \tag{3.3.12}$$

where T is the growth thickness above the mask, T_0 is the growth thickness needed before the ELO starts, S is the seed hole separation, and $r = g_{110}/g_{100}$ is the ratio of the growth rates along {110) and {100} planes. The thickness has been a problem when ELO has been considered as an alternative silicon-on-insulator(SO1)for dielectrically isolated CMOS or bipolar technology because a very thin SOI film (≈1μm) is required. This, however, does not limit the application of the MELO structure to silicon micromechanical sensors since the thickness of diaphragm in sensor applications is not usually that thin but typically 10 to 30 pm. The V-groove also can be reduced by increasing the HCl in the process gas during ELO growth [65].

The ELO silicon previously showed higher defect densities than SEG or in bulk semiconductor [56, 63, 77]. However, recent results of R. Zingg and G. Neudeck demonstrated the bulk-quality characteristics of majority carrier MOS devices fabricated in ELO silicon [78]. This verifies the applicability of ELO to the silicon micromechanical sensor where only majority carrier devices are required. Also, crystallographic defects such as void formation or twins in the MELO structure has been reported in the earlier work [63, 65]. The void appears when the upper parts of ELO fronts merge first and trap some gas in the vicinity of the oxide surface. The void formation can be avoided either by decreasing the overall growth rate or by reducing the HCl concentration until the ELO fronts merge [65].



(a)



(b)

Figure 3.13 (a) SEM photograph showing a morphology of ELO prior to merging. (b) The thickness required for complete merging vs. seed-hole separation [76].

Simple MELO structures on (100) substrate silicon over <100> oriented 5μm wide oxide smps have been produced to examine its crystallographic quality as grown in the Gemini I LPCVD reactor in the Purdue Solid State Epitaxial Laboratory. A scanning electron microscopy (SEM) photograph of the cleaved cross section is shown in Fig. **3.14.** Optical observations indicated that there are no voids on the buried masking oxide or any other visible crystal defects after merging.

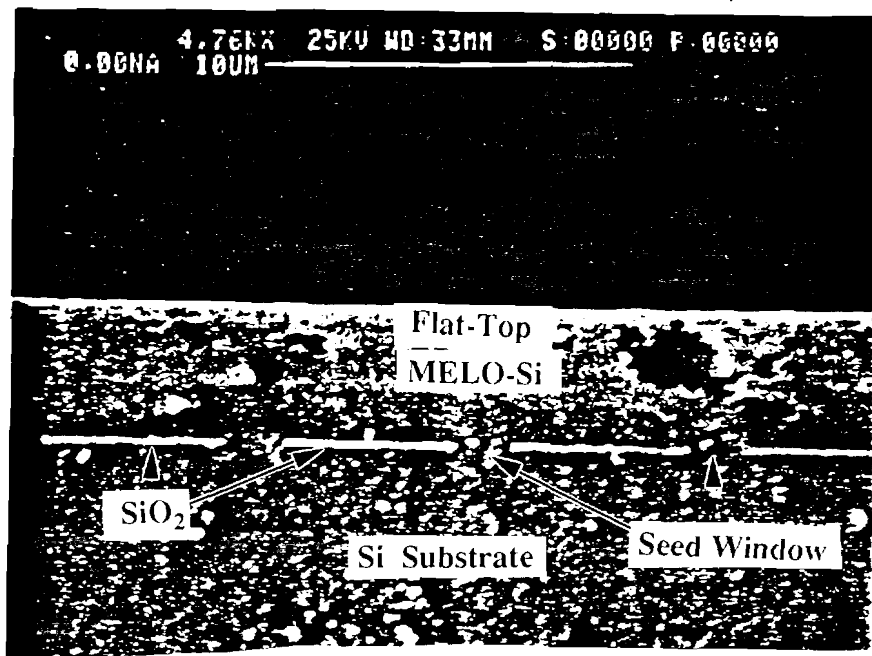


Figure **3.14** SEM photograph of MELO silicon cross section.

3.4 Wide and Thin MELO-Si Diaphragm Fabrication Process

Using MELO silicon and the new SiO_2 etch-stop technique illustrated in Fig. 3.5, a novel single crystal diaphragm can be produced. For a small accelerometer, which would have very small seismic mass and beams of less than 5μm thickness, only one oxide strip can be used to manufacture a thin diaphragm beam. In this case, only oxide would participate in the etch-stop mechanism and both sides of a beam are formed by slowly etched crystallographic planes as shown in Fig. 3.15(a). Therefore, a perfect etch-stop with an excellent control of the beam thickness would be expected.

For reasonably large devices such as an accelerometer with beams whose dimensions are in the range of 10 to 25μm thick, 100μm wide, and 1000μm long, a modified beam structure needs to be employed. If one wide oxide strip is used for a wide beam structure, then the desired thin MELO silicon on SiO_2 for a diaphragm structure can not be achieved. Instead the thickness will be about half of the width of the oxide when the MELO silicon takes place because the aspect ratio, the ratio of lateral to vertical growth, of ELO silicon is close to unity. However, the wide and thin diaphragm can be constructed by MELO silicon on several oxide strips, between which several narrow seed holes are formed, and SiO_2 etch-stop combined with V-groove self-limiting etch-stops as shown in Fig. 3.15(b).

This section presents design, fabrication development, and experimental results of a large area, thin MELO-Si diaphragm with an SiO_2 etch-stop combined with crystallographic self-limiting V-groove etching. The V-groove self-limiting process, the anisotropic etching has been described in section 3.1. The etching will then be limited by the oxide strips and the slowly etched crystallographic planes exposed between oxide strips. First is discussed the anisotropic etching of the silicon substrate and MELO-Si film that was performed with a KOH-based solution for the verification of V-groove self-limiting etch-stop. Then the thickness uniformity of the MELO-Si film is presented over a wafer and by location on a wafer-to-wafer basis. The thickness of the MELO-Si diaphragm is controlled by the MELO growth rate which is approximately 0.1μm/min. In addition, the material quality of MELO-Si film was examined by a crystallographic defect etch and by device fabrication and characterization.

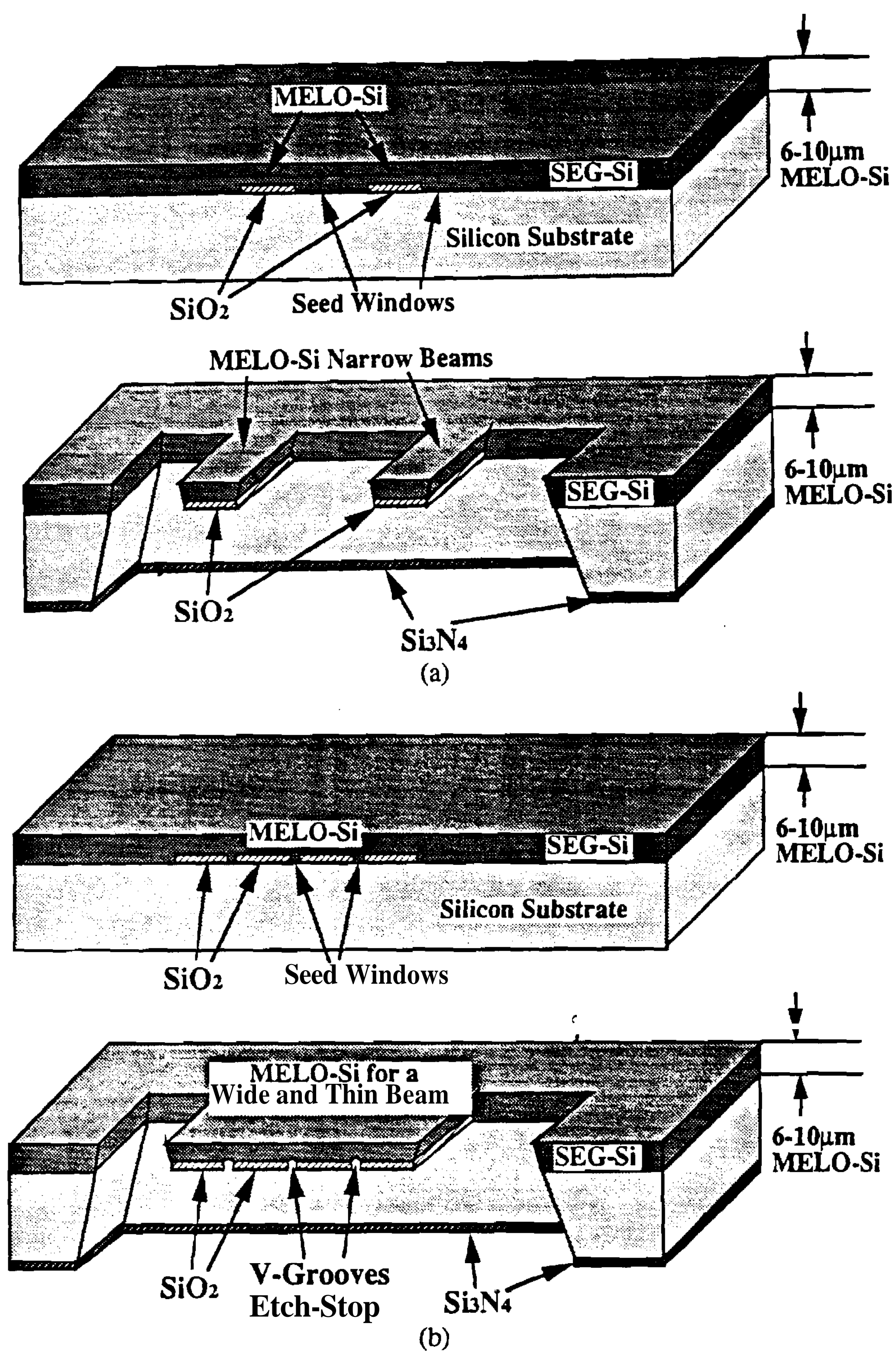
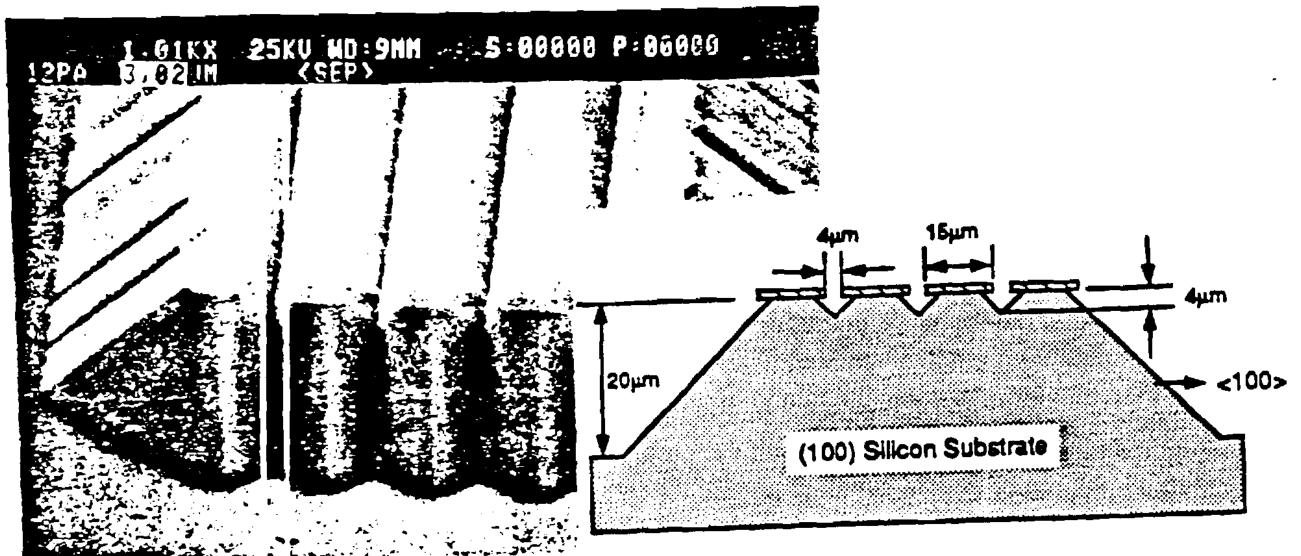


Figure 3.15 MELO-Si diaphragm fabrication technique by SiO_2 etch-stop combined with V-groove self-limiting etch. (a) A narrow beam with a single oxide. (b) A wide and thin diaphragm or beam with a group of oxide smps.

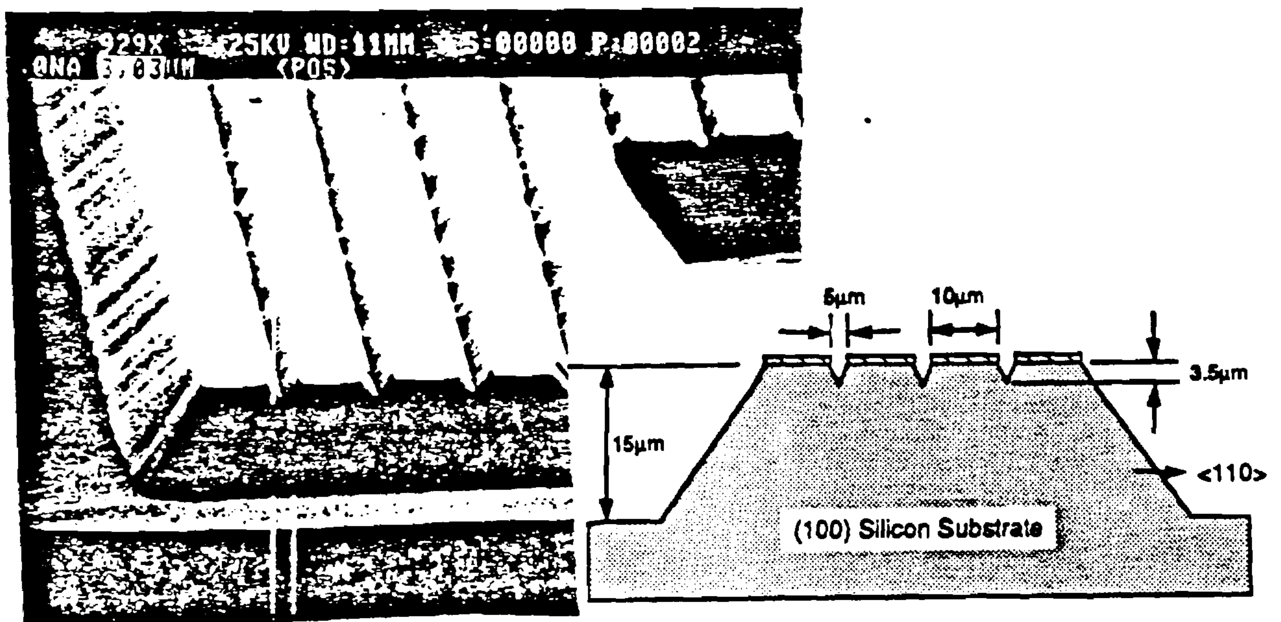
3.4.1 Examination of the Etch-Stop by Self-Limiting V-grooves

The anisotropic etching and etch-stop experiments were performed on (100) n-type silicon wafers which were the same as those used for SEG/ELO experiments. First, SiO_2 patterns were aligned to <100> directions which would result in the better ELO quality than other directions. With the oxide aligned to <100> directions, the etched structure is bounded by convergent {110} planes which make an angle of 45° with the surface plane as shown in Figure 3.16(a). Actually, this (110) plane is not a single plane but a group of (110} edges, each of which resulted from the intersection of a couple of {111} planes. Therefore, the real etch-stop planes are {111} planes even though the macroscopic view indicates the etch-stop is realized by {110} planes. This result agrees with the observation of Lee [7]. After a long etching time with the KOH-based etching solutions, it revealed that the V-grooves formed between the oxide smps sustained their shapes with some lateral undercut. The undercut, with the oxide edges aligned to <100> directions, is more noticeable than with those aligned to <110> directions due to the (110} edges exposed. However, the etched depth is somewhat compensated for because the angle made by (110) edges with the surface plane is smaller (45") than that made by (111) planes (54.74').

Next, SiO_2 patterns were aligned to <110> directions for the purpose of comparison. When the masking oxide is aligned to <110> directions, the etching shows better etch-stop characteristics with less undercut than when the oxide edges are aligned to <100> as shown in Figure 3.16(b). It has been found experimentally that when the oxide opening is precisely aligned to <110> directions, etching can conform exactly to the oxide mask with the negligible undercut [79]. However, when the oxides are aligned to <110> directions, the angle between one of the slowly etched planes, {111) planes, and the top is about 54.7° resulting in deeper grooves than when the oxides are aligned to <100> directions, provided the etch windows are identical. For a self-limiting V-grooves etched for a long time, the oxides aligned to <110> directions will have less undercut than those aligned to <100> directions. However, as mentioned earlier, the ELO material quality grown on the oxide aligned to <110> directions usually shows more crystallographic defects and larger facets on the growth fronts [54, 63, 71].



(a)



(b)

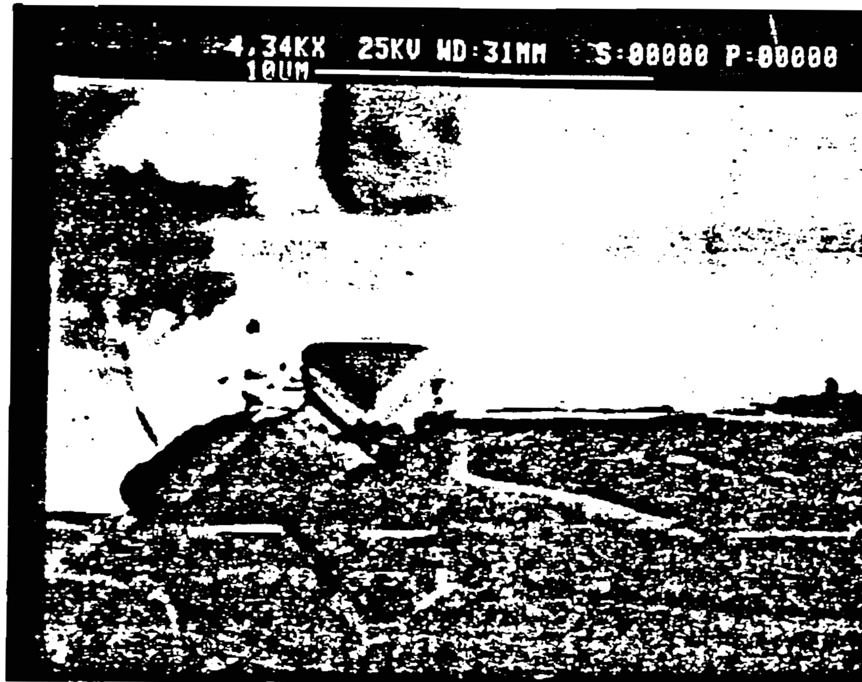
Figure 3.16 (a) SEM photograph of V-groove self-limiting etch-stop after long anisotropic KOH etch with oxides aligned to <100> directions. (b) SEM photograph of V-groove self-limiting etch-stop after long anisotropic KOH etch with oxides aligned to <110> directions.

Finally, the anisotropic etching was performed on the MELO-Si film. A thin diaphragm is normally fabricated by etching a silicon substrate from the back to the desired thickness, which usually takes several hours. For simplicity, however, etching was performed from the top MELO surface, assuming the MELO silicon is identical to the substrate silicon, even though actual etching needs to be done from the back of the wafer. The legitimacy of this approach was verified by etching the MELO film surface anisotropically and comparing it with the results obtained from the anisotropic etching of the substrate silicon. A SEM photograph of the top etched MELO film is shown in Fig. 3.17(a) which illustrates the V-grooves formed by the slowly etched {110) planes resulting in the self-limiting etch-stop like the substrate. It indicates the MELO film has the identical orientation and the same crystallographic strength as the substrate silicon.

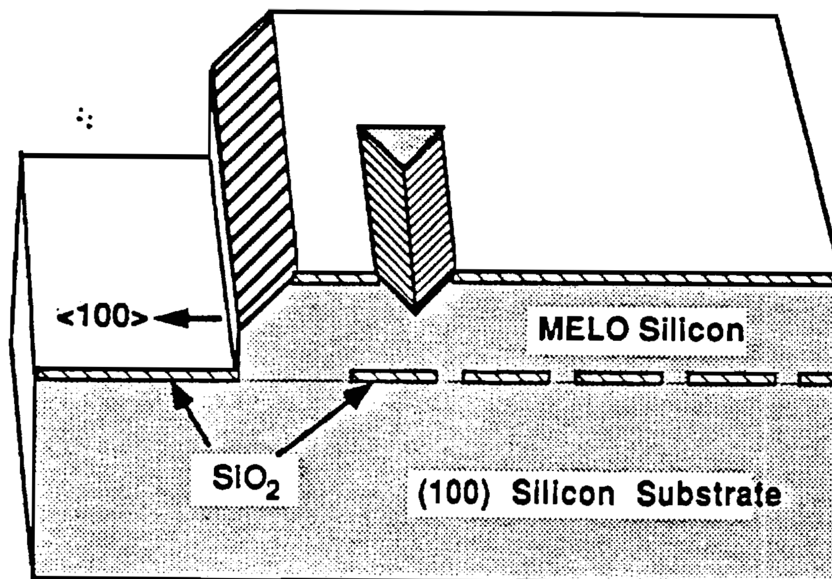
From these etch-stop experiments, it has been shown that the new etch-stop technique is applicable to form a wide thin diaphragm beam. A beam structure can be formed with the minor variation in the thickness due to the V-grooves formed between the oxide strips for the crystallographic etch-stop. The depth of those grooves mainly depends on the seed window width between two neighboring oxides and the lateral undercut associated with the exposed planes during the anisotropic etching.

3.4.2 Design and Development

The second test mask, shown in Fig. 3.18, was designed and implemented for realizing a wide and thin diaphragm using the MELO technology and with an SiO_2 etch-stop combined with crystallographic self-limiting etching. It was also used for MELO growth rate and its uniformity characterization. The growth rate of the MELO films was evaluated by measuring the ELO film thickness over the large oxide regions, wider than 100μm, with an Alpha-Step profilometer. Figure 3.19 shows the places on the wafer where the measurement was taken. Positions 1 through 8 correspond to the large oxide islands in quadrant #3. These islands are clearly shown on the mask layout in Fig. 3.18(a). Each vertical bar in quadrant #1 of Fig. 3.18(a) consists of a set of 5x1200 μm^2 rectangular oxide islands separated by 2pm wide seed holes; this is magnified and illustrated in Fig. 3.18(b).



(a)



(b)

Figure 3.17 (a) SEM photograph of V-groove self-limiting etch-stop on the MELO film. (b) Schematic view of the SEM photograph.

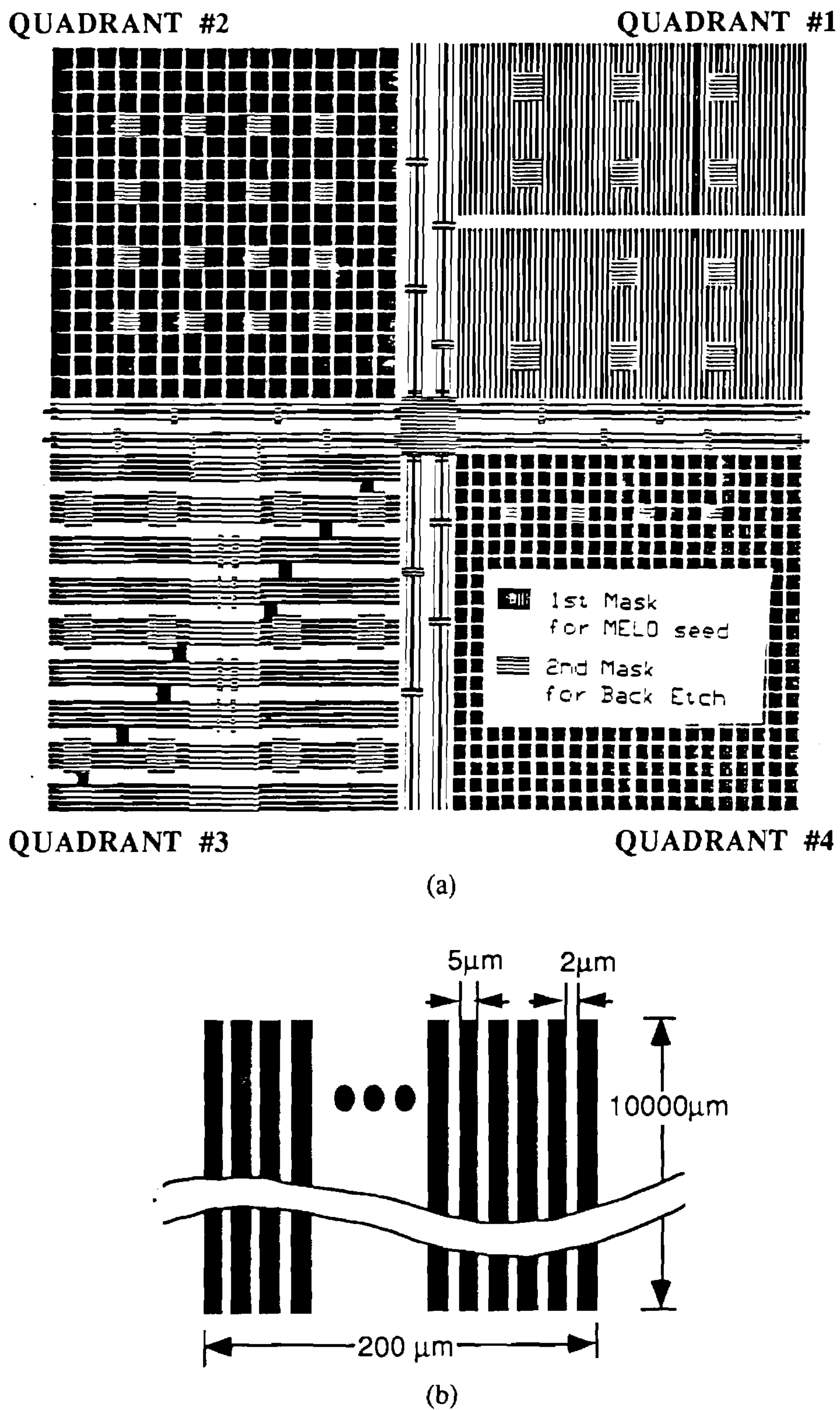


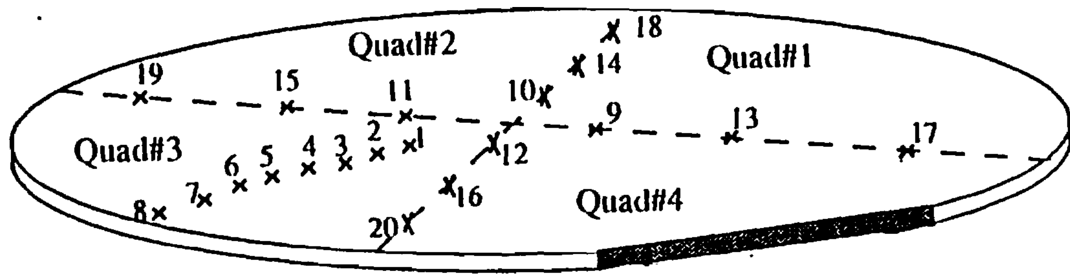
Figure 3.18 Layout of the second test mask. (a) The 4 quadrants cover a whole 3" wafer. (b) Magnified view of one vertical bar in Quad. #1.

3.4.3 Uniformity of MELO Silicon

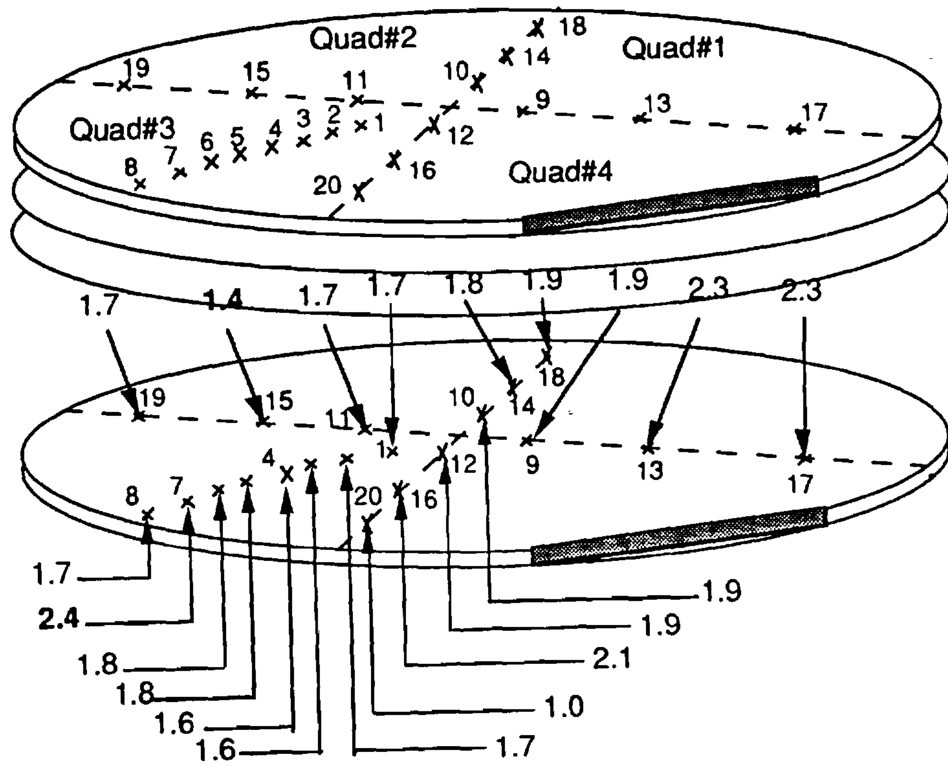
Tables 3.2 summarizes the statistical results of the MELO silicon growth on the wafers over four different epitaxial (epi) runs. All wafers in each run used the same pattern and orientation. The MELO-Si film thickness analysis was performed across the wafer by measuring twenty different positions across each wafer as shown in Fig. 3.19. To further understand the summary tables, consider the original data sheet of the first epi run given in Table 3.3. Statistical parameters, such as the average growth, the standard deviation, and the percent variation, are calculated across a wafer (down a column) over twenty different locations. The percent variation is obtained by a hundred times the standard deviation divided by the average growth value. Thus, the last three rows in Table 3.3 are the values listed in the middle three columns under average growth rate, standard deviation, and % variation of Table 3.2. In addition, the same parameters were calculated and added in the last three columns for a particular location (on the wafer) over all wafers as shown in Fig. 3.19. These parameters have a wafer to wafer basis and are not listed in the summary tables. To better visualize the wafer to wafer parameters per run, the ELO thickness for all wafers has been plotted against position (Figures 3.20, 3.22, 3.24, and 3.26; also known as growth profile), and the standard deviation and the percent variation of all wafers are graphed versus position as well (Figures 3.21, 3.23, 3.25, and 3.27). The significance between the parameters within a wafer and the parameters with a wafer to wafer basis will become apparent in the following discussion.

In the first run, the growth temperature was 1020°C at 150 Torr. The variation of growth across a wafer is within 6% for all six wafers, the lowest being 2.9% for wafer #GT5. For the second run at 970°C, 40 Ton, the growth variation in a wafer is within 6.4%, very similar to the first run. Analogously, the percent variation in a wafer is within 4.1% and 6% for the third run at 1020°C, 150 Torr and forth run at 970°C, 150 Torr, respectively. Thus, at either high or low growth temperature, it is possible to attain less than 10% growth variation (the accepted range) across a wafer, as listed in Tables 3.2 and 1.3.

The growth profile of each run (Figures 3.20, 3.22, 3.24, and 3.26) illustrates that the epitaxial thickness at any given position on a wafer deviates very little from that at the same position on other wafers in the same run. This can be further verified by the corresponding bar graphs (Figures 3.21, 3.23, 3.25 and 3.27) that display the standard deviation and the percent variation at any given wafer location per run.



(a)



(b)

Figure 3.19 MELO thickness measuring positions over each wafer and wafer to wafer with the second test mask.

Table 3.2 Statistical results and uniformity of ELO growth

Growth Condition		Wafer	Avg. total Growth(μm)	Std. Dev. (μm)	% Var.	Avg. GR (μm)
RUN **#1**						
Temperature	1020°C	GT5	10.43	0.30	2.90	0.130
Pressure	150 Torr	GT6	10.48	0.59	5.65	0.131
Ox.thickness	0.5 μm	GT4-tn	10.08	0.44	4.32	0.126
Dep. time	80 min.	GT5-tn	10.11	0.45	4.44	0.126
		GT6-tn	10.37	0.40	3.84	0.129
		GT7-tn	10.17	0.60	5.87	0.127
RUN #2						
Temperature	970°C	gt1	11.95	0.52	4.32	0.108
Pressure	40 Torr	gt2	11.20	0.45	4.32	0.102
Ox.thickness	0.5 μm	gt3	11.70	0.70	4.02	0.106
Dep. time	110 min.	gt4	11.01	0.56	6.01	0.100
		gttn1	11.36	0.72	5.05	0.103
		gttn2	11.34	0.55	6.35	0.103
		gttn3	11.66	0.51	4.86	0.106
RUN #3						
Temperature	970°C +	gr10tn	8.181	0.334	4.08	0.128
	1020°C	gr22tn	8.334	0.326	3.92	0.130
Pressure	150 Torr	gr12tn	8.467	0.249	2.94	0.132
Ox.thickness	0.9 μm	gr14tn	8.403	0.347	4.13	0.131
Dep. time	5+66 min.					
RUN #2						
Temperature	970°C	gr15tn	9.135	0.54	5.86	0.083
Pressure	150 Torr	gr16tn	8.56	0.49	5.78	0.078
Ox.thickness	0.9 μm	gr17tn	8.28	0.494	5.96	0.075
Dep. time	110 min.	gr18tn	7.87	0.34	4.29	0.073

Table **3.3** MELO run sheet of run #1

Position	GT5 (µm)	GT6 (µm)	GT4-tn (µm)	GT5-tn (µm)	GT6-tn (µm)	GT7-tn (µm)	Avg. W to W (µm)	Std. Dev (µm)	% Var
1	10.34	10.49	10.06	9.985	10.26	10.22	10.23	0.18	1.72
2	10.29	10.33	9.905	9.845	10.09	10.02	10.08	0.17	1.68
3	10.22	10.16	9.77	9.745	10.05	9.89	9.97	0.16	1.61
4	10.25	10.07	9.685	9.66	9.905	9.68	9.88	0.16	1.64
5	10.06	9.725	9.4	9.405	9.73	9.355	9.61	0.17	1.75
6	10.01	9.59	9.34	9.35	9.69	9.235	9.54	0.17	1.79
7	9.74	9.39	9.135	9.2	9.68	9.06	9.37	0.22	2.37
8		9.28				8.975	9.13	0.15	1.67
9	10.67	11.04	10.52	10.46	10.61	10.67	10.66	0.20	1.91
10	10.71	11.14	10.57	10.65	10.91	10.85	10.81	0.20	1.86
11	10.74	11.05	10.58	10.56	10.85	10.78	10.76	0.18	1.69
12	10.86	11.15	10.59	10.61	10.8	10.74	10.79	0.20	1.87
13	10.64	11.07	10.38	10.44	10.57	10.6	10.62	0.24	2.29
14	10.52	10.94	10.41	10.57	10.78	10.8	10.67	0.19	1.75
15	10.71	10.8	10.43	10.47	10.75	10.71	10.65	0.15	1.43
16	10.8	11.03	10.42	10.47	10.68	10.51	10.65	0.22	2.08
17	10.55	10.89	10.2	10.27	10.4	10.41	10.45	0.24	2.31
18	10.1	10.37	9.94	10.28	10.43	10.47	10.27	0.19	1.85
19	10.36	10.35	10.06	10.13	10.56	10.34	10.30	0.18	1.72
20	10.62	10.65	10.19	10.08	10.37	10.11	10.34	0.21	2.04
Avg. Growth (µm)	10.43	10.48	10.08	10.11	10.37	10.17			
Std. Dev (µm)	0.30	0.59	0.44	0.45	0.40	0.60			
% Var.	2.90	5.65	4.32	4.44	3.84	5.87			

In the high temperature runs (Runs #1 and #3), the percent variation at a specific location is less than 2.5% whereas, in the low temperature runs (Runs #2 and #4), the same variation is less than 9%. The nearly constant thickness among the wafers in the same run at higher growth temperature indicates that any thickness of the diaphragm beam can be repeatedly grown in the reactor at Purdue University. However, the corresponding growth profiles show a decrease of growth radially outward in quadrant #3. This is merely an indication that the susceptor in the reactor has a temperature gradient, which has been verified by Ge dot melts. The same growth reduction is observed for the low temperature runs. Correction can be made to the reactor by adjusting the RF heating coils such that more uniformity may be ensured during growth. Lastly, it will be explained that the slight increase in the percent variation at a reduced growth temperature is a trade off for a better silicon quality, which is always desired in the semiconductor technology.

As mentioned before, the percent variation from wafer to wafer at high temperature 1020°C) is slightly less than that at lower temperature (970°C). This rnay be explained from a growth rate point of view. In Tables 3.2 and 3.3, note that the growth rates at high temperature runs are always larger and more consistent among the wafers in a run than those at low temperature runs. This is duly to the increase in the reaction rate of the reactants at high temperature, which ultimately increases the overall growth. Thus, at low temperature, low reaction rates across the wafer results in less consistent growth rates among the wafers in a run; therefore, an increase in the percent variation from wafer to wafer is observed in the data analysis. Yet, better quality of silicon was obtained at low temperature.

From the above discussion for four different growth runs, the following conclusions are made.

1. Temperature gradient across the susceptor is evident in all growth profiles and has been verified by Ge dot melts.
2. Repeatability of the growth in the reactor is very consistent
   a. for within a wafer average and
   b. for at a given position average.
3. Uniformity is improved for high temperature runs.
4. Increased temperature yields higher growth rate due to the increase in the reaction rate of the reactants.
5. Lowering of the temperature has slightly increased the percent variation of the growth from wafer to wafer; however, the surface topology appears excellent.

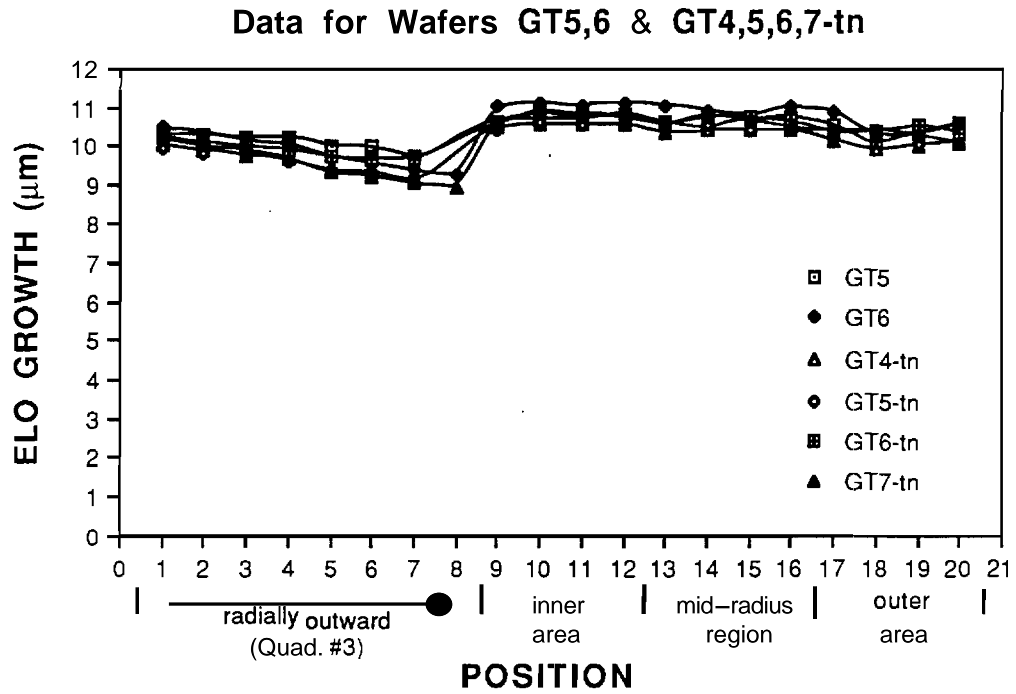


Figure 3.20 Growth profiles of the first run (at 1020°C and 150 Torr).

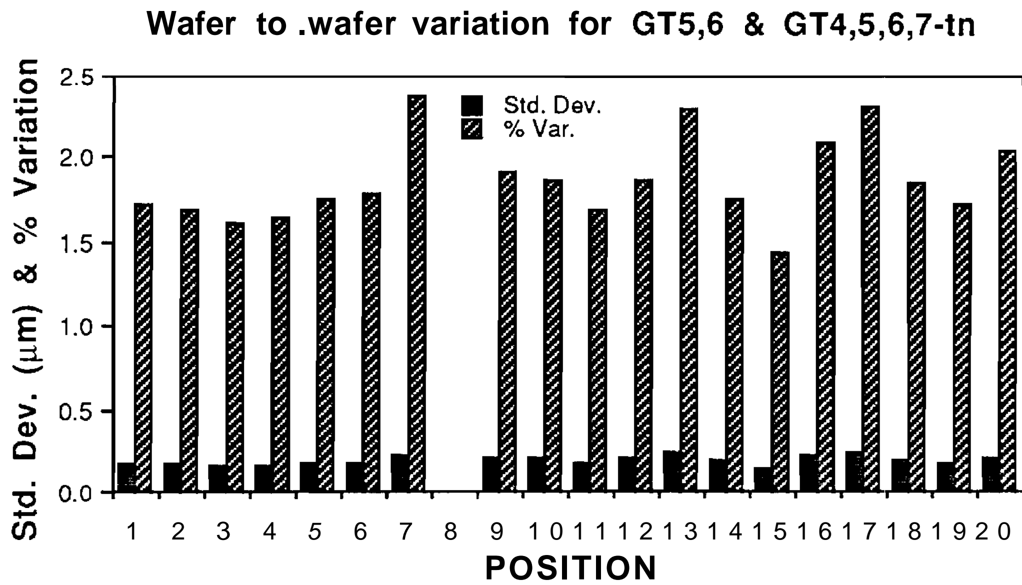


Figure 3.21 Wafer to wafer standard deviation and % variation of the ELO silicon thickness at different test points for the first run (at 1020°C and 150 Torr).

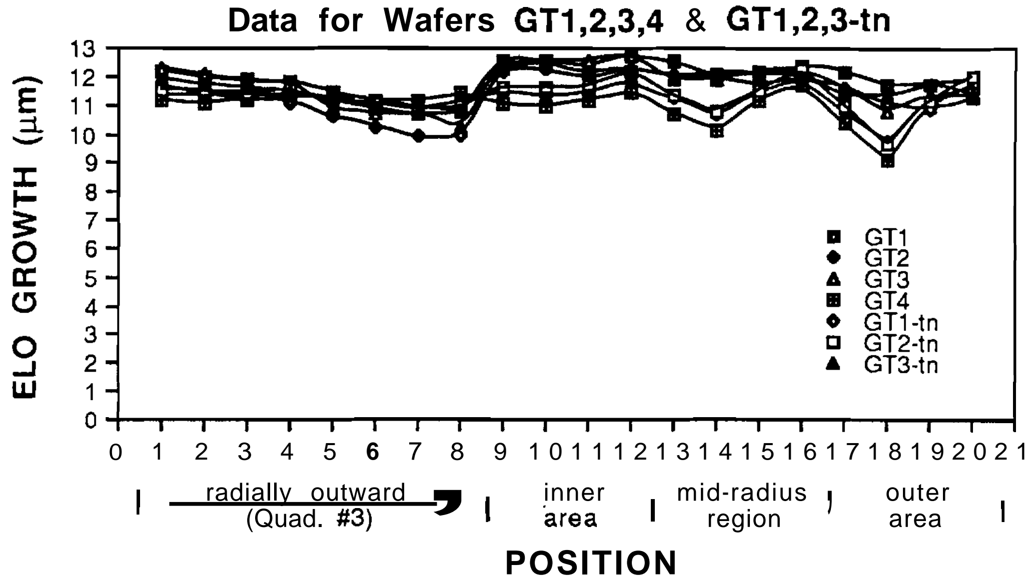


Figure 3.22 Growth profiles of the second run (at 970°C and 40 Torr).

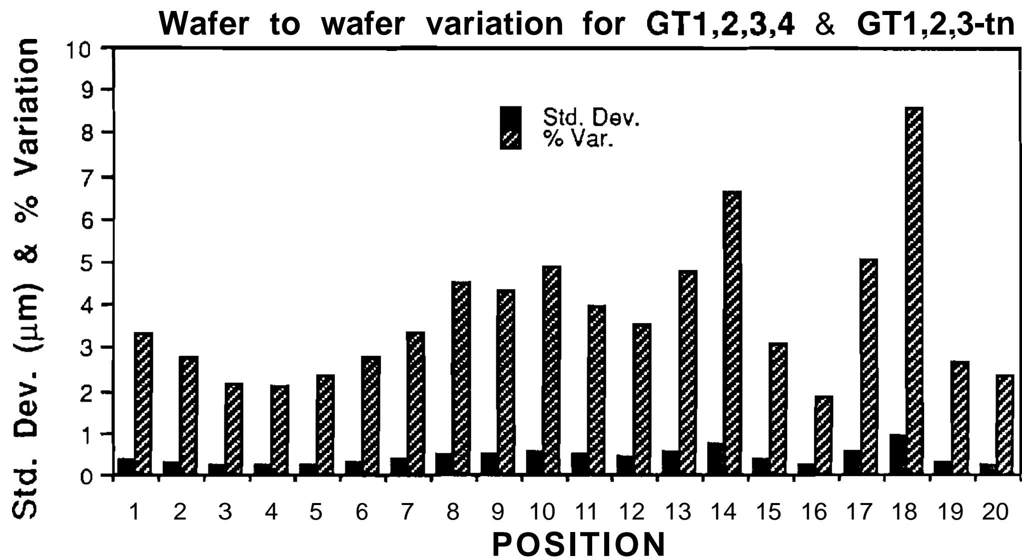


Figure 3.23 Wafer to wafer standard deviation and % variation of the ELO silicon thickness at different test points for the second run (at 970°C and 40 Torr).

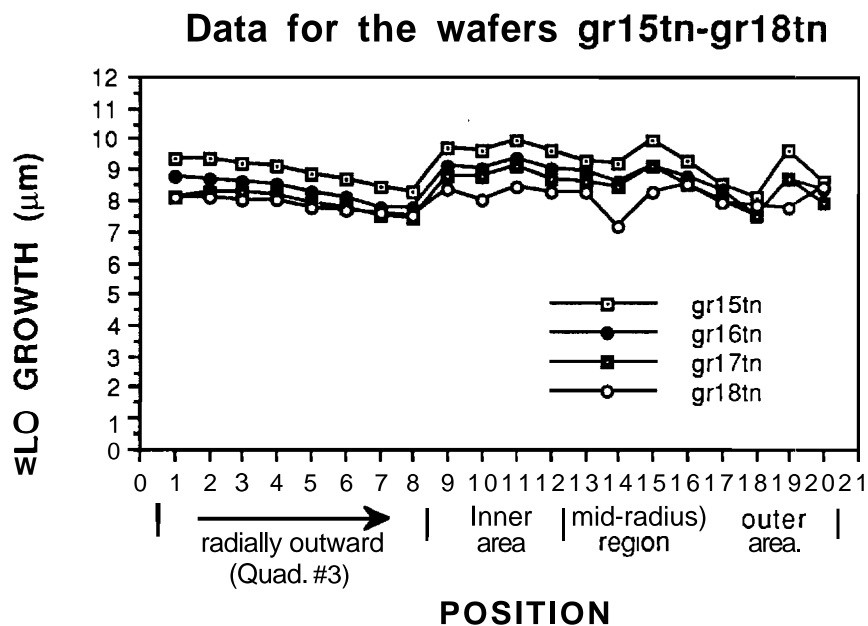


Figure 3.24 Growth profiles of the third run (at 1020°C and 150 Torr).

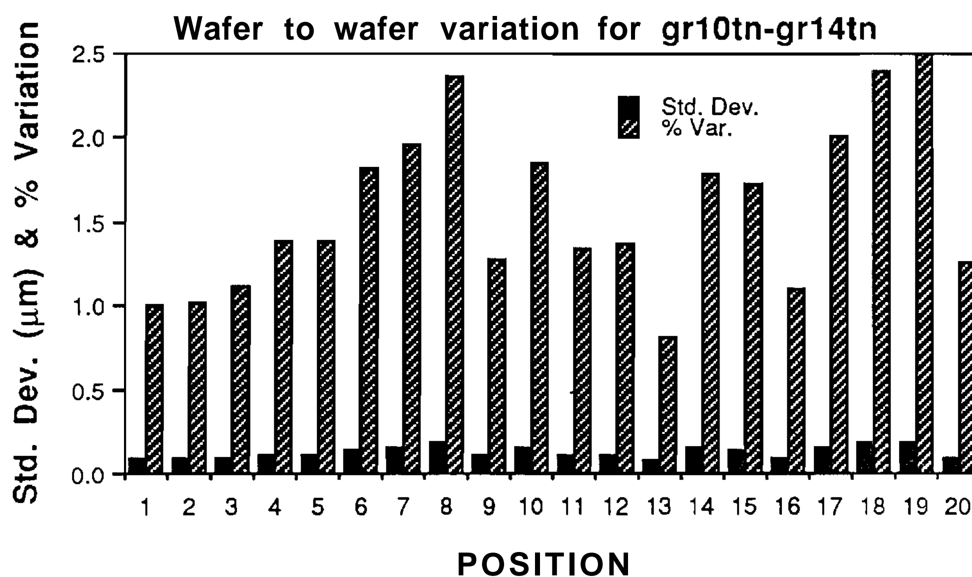


Figure 3.25 Wafer to wafer standard deviation and % variation of the ELO silicon thickness at different test points for the third run (1020°C).

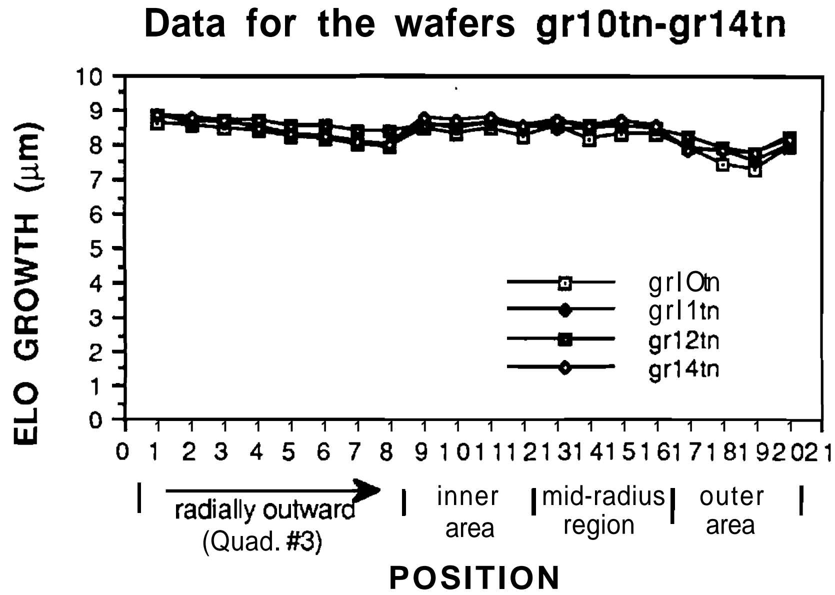


Figure 3.26 Growth profiles of the forth run (at 970°C and 150 Torr).

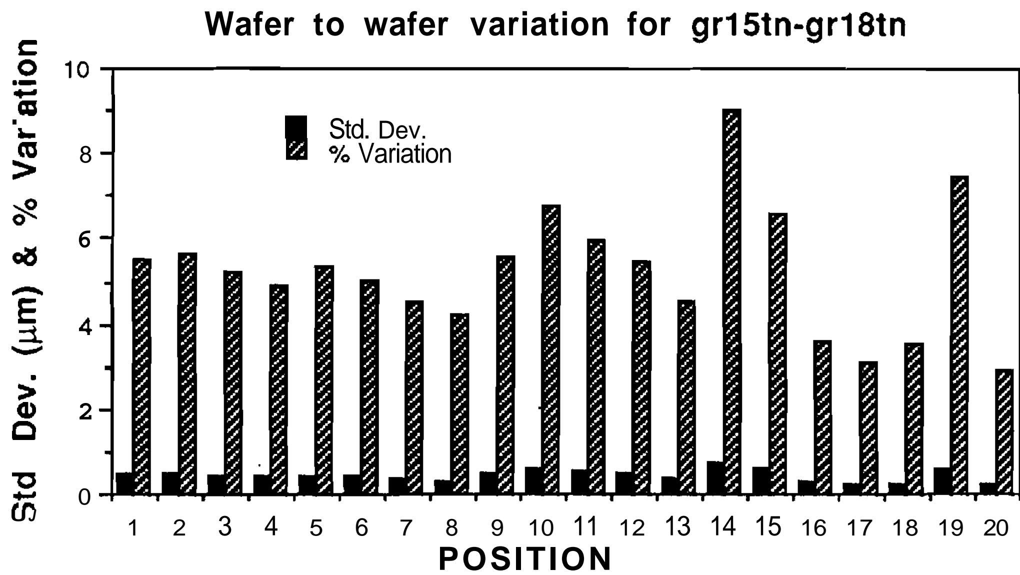


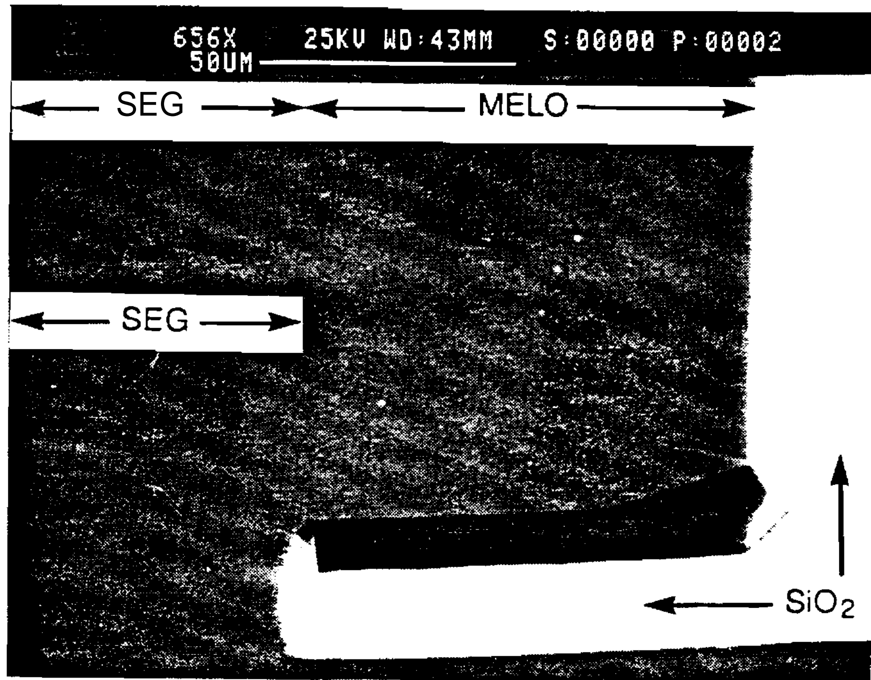
Figure 3.27 Wafer to wafer standard deviation and % variation of thickness at different test points for the forth run (at 970°C and 150 Torr).

3.4.4 MELO-Si Diaphragm Fabrication by SiO_2 Etch-Stop and Self-Limiting V-grooves

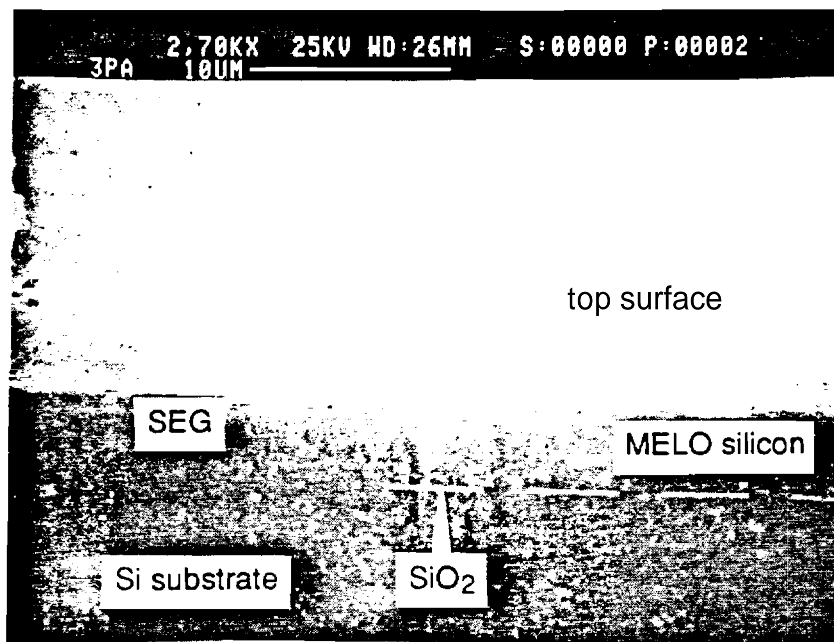
The merged ELO silicon grown on oxide islands in the Gemini-I reactor shows a very uniform and smooth surface topology. Although SEG growth and MELO growth are two different processes, the wafer topology of the silicon grown by the two processes in a given run shows no visible difference under SEM. Figure 3.28 displays an SEM photograph of the MELO and SEG silicon grown on the same wafer in the same run. Note that the MELO silicon shown covers approximately 5pm wide oxide islands alternatively patterned next to the seed holes (refer to Fig. 3.18) and has a thickness of 9µm. Because the merged part has a very uniform surface topology, it is difficult to distinguish the MELO silicon from the neighboring SEG silicon as demonstrated in Fig. 3.28.

The thin diaphragm structure shown in Fig. 3.29 was achieved by etching the back side of the wafer using the anisotropic KOH etch. Note that the flat top surface reveals a completely merged ELO, approximately 9µm thick, while the backside was defined by the V-grooves which resulted from self-limiting crystallographic etch. Backside etching was performed at a constant temperature of 80±1°C. The etch solution used contains 47gm of KOH in 127ml of DI water and 39ml of Propanol. Note the formation of the 2pm deep V-groove etch stops between the oxide islands. Due to the precise temperature control of the etch at 80±1°C and due to thorough cleaning of the wafer, the undercut across the oxide islands was minimized. As mentioned earlier, Figure 3.29(b) is a close-up view of the diaphragm beam of Fig. 3.29(a), but the beam has been stripped of the protective nitride layer and the oxide islands.

A protective silicon nitride mask was required on both sides of the wafer during the silicon etch. Plasma enhanced vapor deposition (PECVD) technique was used to form the silicon nitride film even though low pressure chemical vapor deposition (LPCVD) technique could have been used just as well. In either case, the nitride film must be able to sustain itself in the KOH solution for as long as it takes to etch from the backside of the wafer to the oxide islands near the top of the wafer. One of the advantages of PECVD nitride over LPCVD nitride is that PECVD nimde is deposited at a lower temperature than Al-Si melting point while LPCVD nitride is deposited at a higher temperature. Therefore, in the accelerometer fabrication process, PECVD nitride can be employed after Al-Si deposition but LPCVD cat not. In addition, the PECVD nimde can be patterned by etching with Buffered Hydrogen Fluoride (BHF) solution. SiO_2 cannot be used as the mask because the backside etching takes more than five hours and SiO_2 is considerably damaged after one to two hours in the KOH solution.

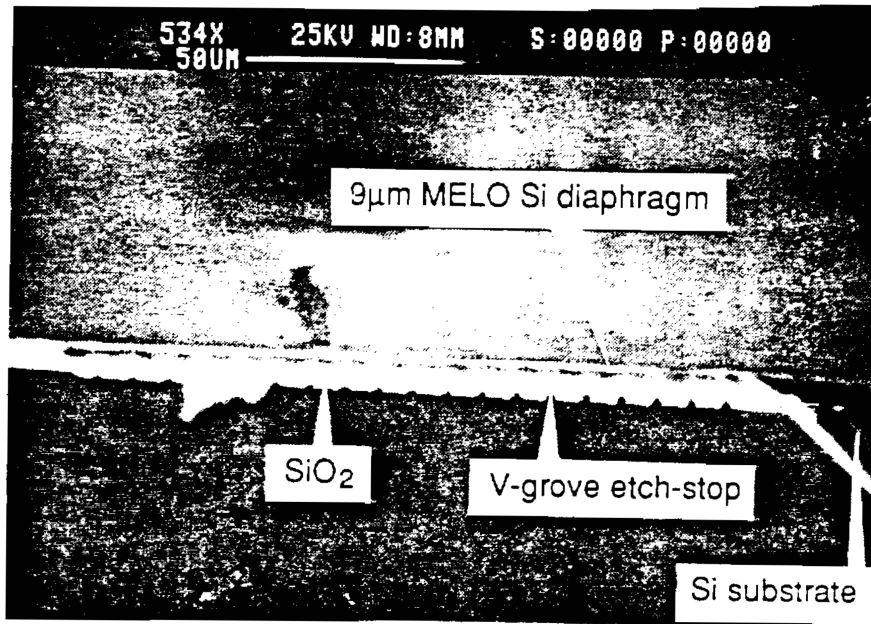


(a)

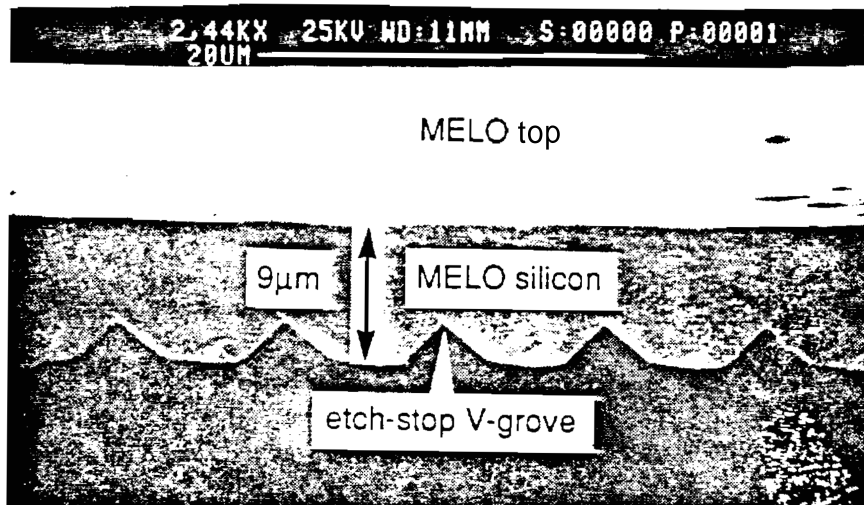


(b)

Figure 3.28 SEM photograph showing the MELO and SEG silicon on the wafer grown at 970°Con a silicon substrate. (a) Top view of SEG and MELO which can not be distinguished from the top. (b) Cross section and top view showing no voids and visible defects at the merging plane on SiO_2.



(a)



(b)

Figure 3.29 SEM photograph showing the thin diaphragm beam with flat MELO (top) and etch stop V-grooves (bottom). (a) A 200µm wide, 9pm thick MELO silicon diaphragm. (b) Enlarged view of the diaphragm after etching SiO_2 strips and nitride protection layer.

Figure 3.30 shows the deep basin formation after five hours of etching from the back side of the wafer. The etched surface and the edges remain very smooth with no sign of etch pits. Figure 3.31 is an SEM picture of the cross section of the. deep basin after seven hours of etching. Here, the picture clearly shows the thin MELO silicon diaphragm hanging at the top of the substrate. Again, it can be reemphasized that the etch stop V-grooves are well defined and the MELO surface remains flat at the merging seam. Overall, the critical issues concerning the formation of thin silicon membrane with a large surface area have been successfully demonstrated.

Evaluation of the cross-sections of MELO films in the scanning electron microscope reveals the following characteristics.

(1) The aspect ratio, lateral to vertical growth ratio, of the ELO film is close to unity. Therefore, ELO growth must continue across at least half of the SiO_2 width before the two ELO fronts merge.

(2) The MELO films do not show any visible voids or crystal defects along the merging plane. .

(3) The merging fronts make V-groove facets when they start to coalesce and become a planar MELO surface with additional growth time.

3.4.5 MELO-Si Material Evaluation

As shown in Fig. 3.10, when the two ELO fronts merge on the SiO_2 mask the MELO silicon film may have voids or defects along and near the merging seam. By optimizing the silicon epitaxy condition, the voids can be minimized or eliminated. The defects induced by the merging mechanism can be physically examined with a defect decorating etch such as Secco etch or Wright etch. It is, however, more intriguing to find out if those defects would play a significant role in the electronic device characteristics. In order to evaluate whether the MELO technology is suitable for electrical devices such as resistors, diodes, or transistors, it is important to build devices on the MELO film and examine the device electrical characteristics. The device structure used for testing was designed to include bipolar junction transistors (BJT), which is one of the most sensitive devices to the material defects. With this design, both base-to-emitter (B-E) diodes and base-to-collector (B-C) diodes can be evaluated in addition to the BJT device. By fabricating such devices on both SEG and on the MELO silicon and testing them, the electrical characteristics such as diode ideality factor, junction leakage current, can be compared.

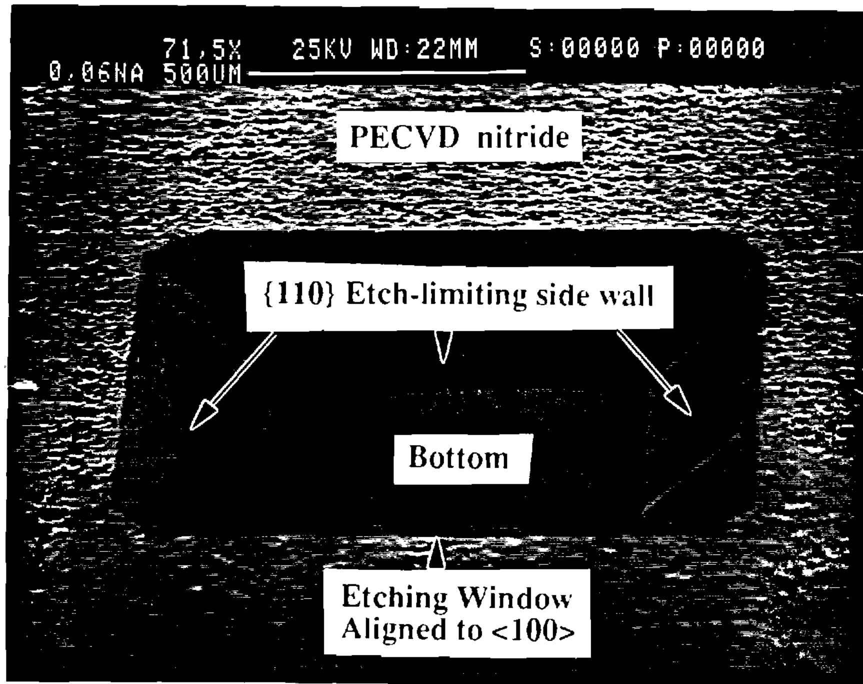


Figure 3.30 SEM photograph of the deep basin formed by the back side etch.

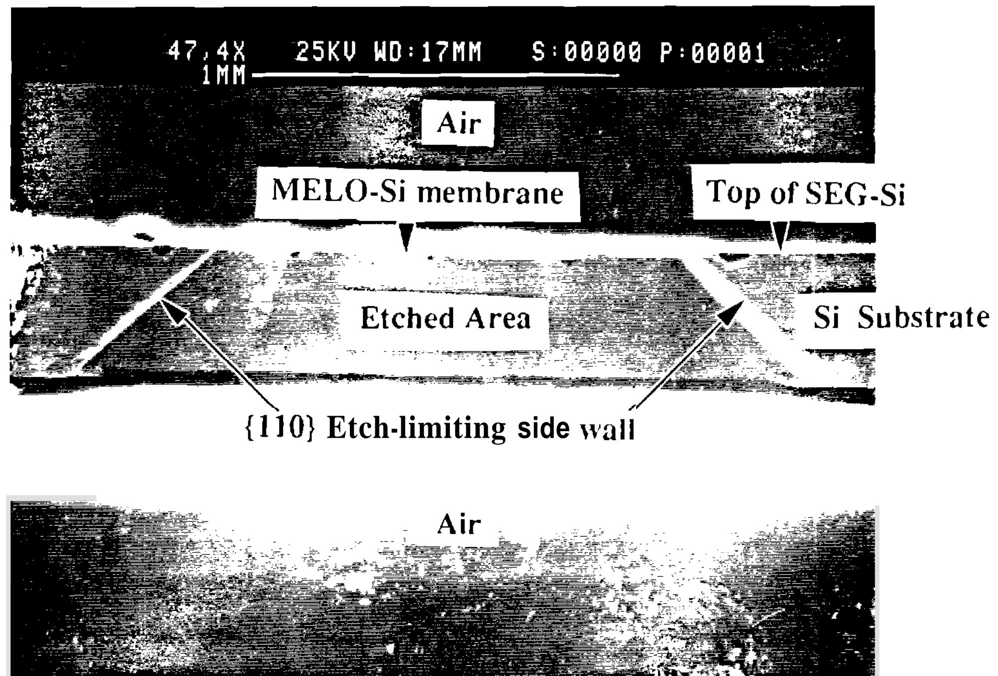


Figure 3.31 SEM photograph showing the cross section of the deep basin shown in Fig. 3.24 after completion of the etch.

3.4.5.1 Device Fabrication - Diode and Bipolar Junction Transistor

The bipolar junction transistor layout is shown in Fig. 3.32. These BJT devices are placed in each die so that the MELO silicon material can be evaluated across the wafer. The fabrication of BJT devices can be incorporated into the MELO-Si accelerometer fabrication by adding only two more masking steps. The additional two masking steps are base (mask #4) and emitter (mask #5) implant pattern. The full MELO accelerometer fabrication procedures, including BJT fabrication steps, are described in chapter 4.

The devices were fabricated on three types of silicon crystal material for comparing the material quality between SEG and MELO silicon: SEG, MELO-I., and MELO-m. Figure 3.33 illustrates the cross section diagram of BJT device fabricated on those three types of film. SEG silicon of Fig. 3.33(a) is a single crystal grown on a large seed window (or silicon field area) selectively. Since the SEG silicon is grocvn far away from the SiO_2 mask, its growth is hardly affected by the SiO_2 mask. The quality of the SEG silicon can be compared to the substrate silicon and hence the devices fabricated on the SEG silicon have repeatedly shown the electrical characteristics comparable to those on the substrate silicon. Therefore, other types of the devices can be compared to the SEG device for the evaluation of the devices as well as the material. MELO-1 of Fig. 3.33(b) represents the MELO silicon grown over a single oxide strip whereas MELO-m of Fig. 3.33(c) represents the MELO silicon grown over multiple oxide strips, here 13 oxide strips. Consequently, MELO-1 silicon has a single merging seam, and MELO-m silicon has several merging seams. The devices were fabricated on these two types of MELO silicon in order to examine the influence of the oxide strips and the corresponding merging seams above them.

The testing results of BJT devices averaged over a number of dies are summarized in Table 3.4. As mentioned earlier, the SEG devices are showing excellent electrical characteristics. The ideality factors from base-emitter and base-collector p-n junction diodes are almost unity and the reverse biased junction leakage current density from those diodes are also very low. The electrical testing results of the MELO-1 and MELO-m devices are not as good as the SEG devices. The ideality factor of the base-collector diodes are still comparable to the SEG devices and it indicates that the material quality of the MELO silicon can become as good as the SEG silicon. Also the leakage current of all three types of devices are comparable. This indicates the MELO silicon is good enough for the majority carrier dominant devices such as piezoresistors and MOSFETs as well as diodes and BJT devices. The measured BJT I, vs. V_{ce} plots from three types of devices are illustrated in Fig. 3.34.

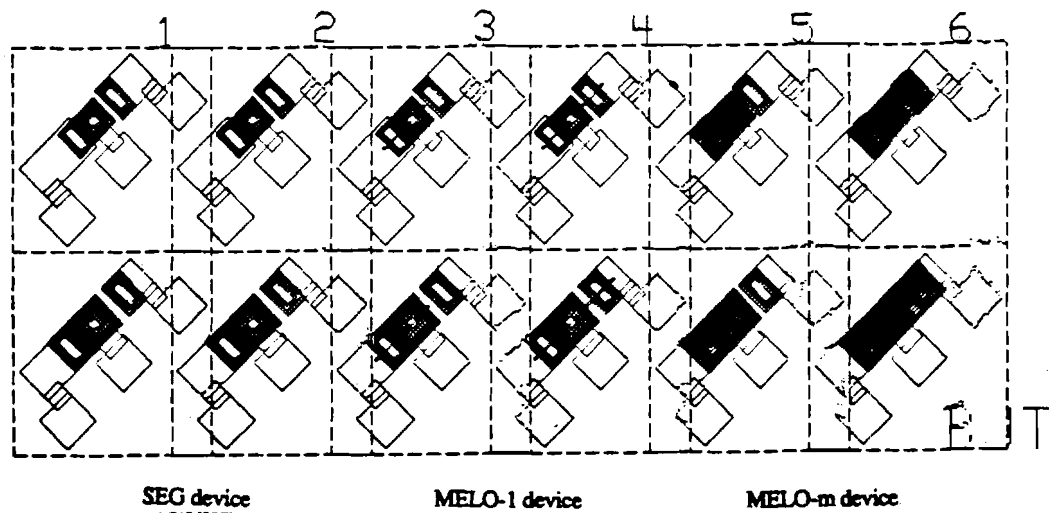


Figure **3.32** Top view of the BJT device for **MELO** silicon material evaluation. The devices under the number 1 and **2** are devices fabricated in SEG silicon, the devices under **3** and 4 are in **MELO** silicon with one oxide strip, and those under *5* and 6 are in **MELO** silicon with multiple oxide strips.

Table **3.4** The testing results of BJT devices fabricated on SEG and MELO-Si

material types	η (ideality factor)		leakage current (A/cm^2)		β_{peak}
	BE diode	BC diode	BC diode	BE diode	
SEG	1.01	1.00	9.70x10^{-8}	5.63x10^{-6}	95
MELO-1	1.35	1.12	4.98x10^{-6}	6.25x10^{-5}	72
MELO-m	1.23	1.11	1.85x10^{-6}	1.16x10^{-5}	~72

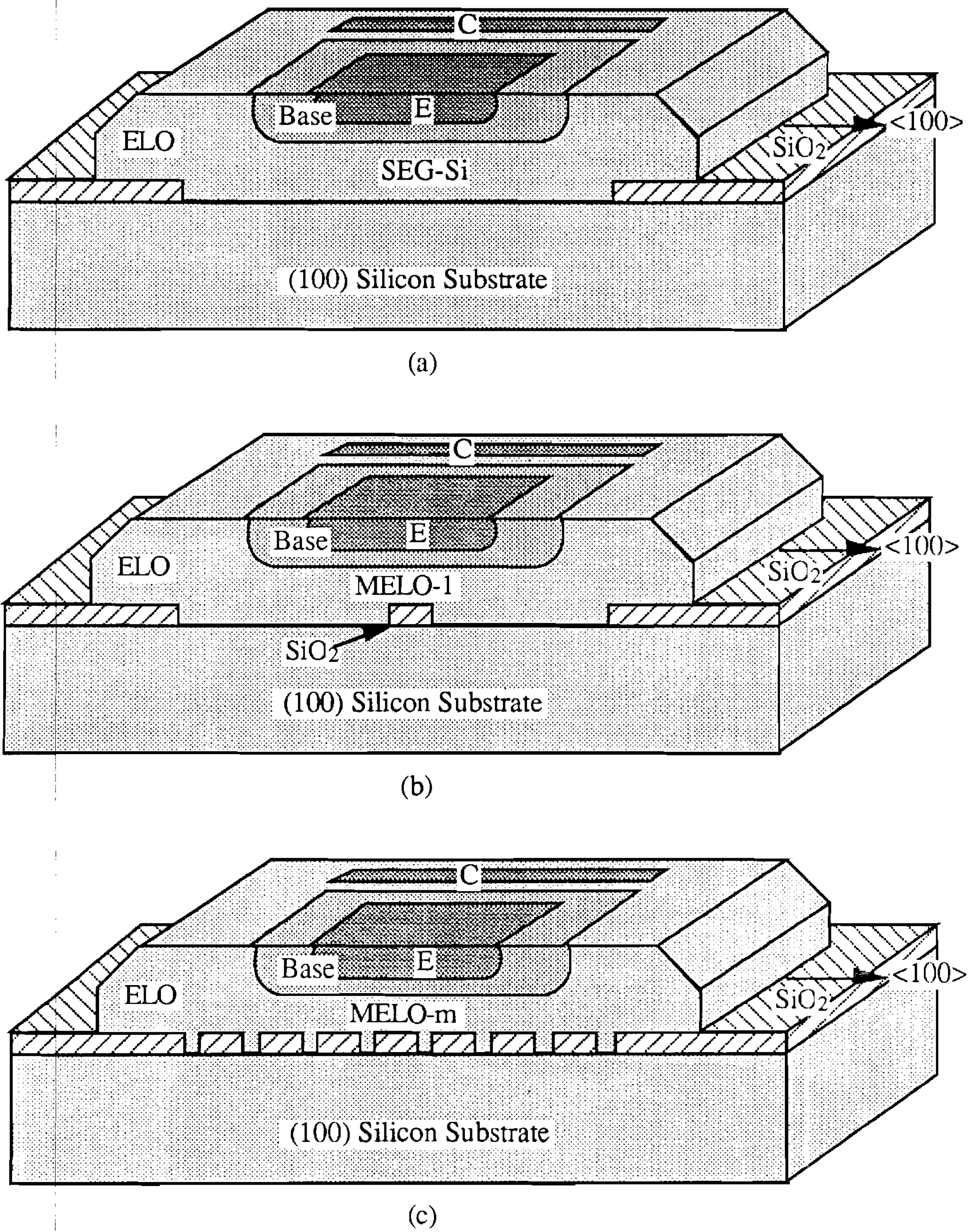


Figure 8.33 Cross section diagram of BJT devices on three different types of material. (a) SEG device, (b) MELO-1 device, (c) MELO-m device

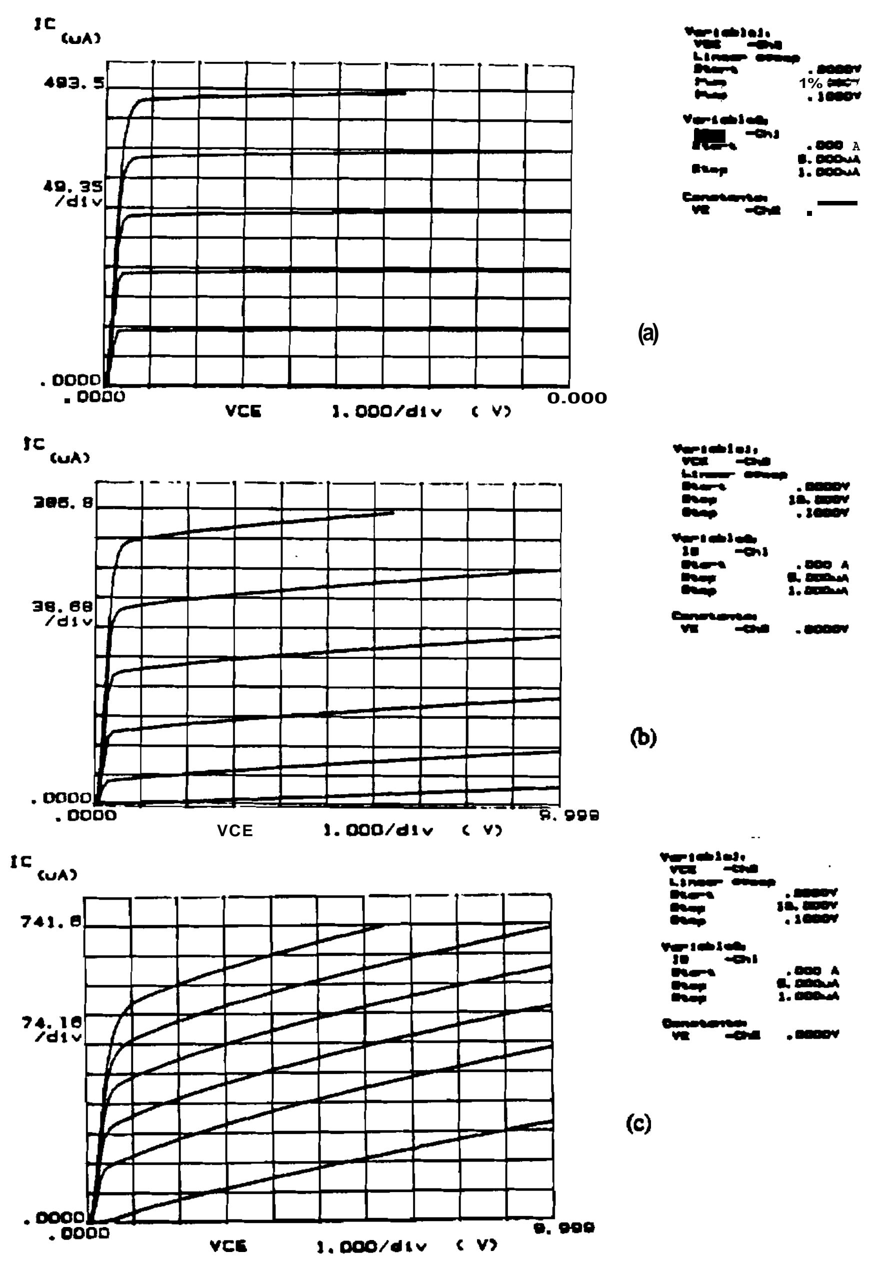


Figure **3.34** Typical I, vs. V_{ce}plots from BJT device of Fig. 2.11. (a) SEG device. (b) MELO-I device. (c) MELO-m device.

3.4.5.2 Crystallographic Defect Etch

The conventional Secco defect etch (one part of 0.15 molar solution of $K_2Cr_20_7$ plus 2 parts of HF) has been executed on MELO silicon for examining crystallographic defects. Preliminary results show that oval shaped etch pits occurred around the merging seam of the MELO silicon. When two advancing ELO fronts merge at the middle of the oxide island, they produce a thermomechanical stress along the merging seam and thereby induce dislocation faults. Also the temperature gradient in the reactor and the difference of thermal expansion coefficient between silicon and silicon dioxide (SiO_2) may play a role in inducing these dislocation faults.

The test mask has different oxide widths starting from 5pm up to 10μm as shown in Fig. 3.35. MELO silicon was grown over these oxide islands on a wafer in a same run. As illustrated in Fig. 3.35 merging will occur on the 5μm wide oxide island first and finally on the 10μm wide strips. Figure 3.36 shows the variation number of etch pits and the etch pit densities which resulted from a 90 second Secco defect etch on MELO silicon grown on different width oxide islands. Both the number of defects and the defect densities are increasing with the wider oxide islands as shown in Fig. 3.36 while having the identical MELO silicon. Since the MELO silicon forms on narrower oxide islands earlier than on wider oxide islands, the merging seam area on the narrow oxide is covered by thicker single crystal silicon. While the MELO silicon is forming on wider silicon islands, the defects around the merging seam on the narrower oxide islands gets healed during the subsequent film growth. Therefore, fewer defects propagate to the top of the MELO silicon where the Secco etch has decorated the defects.

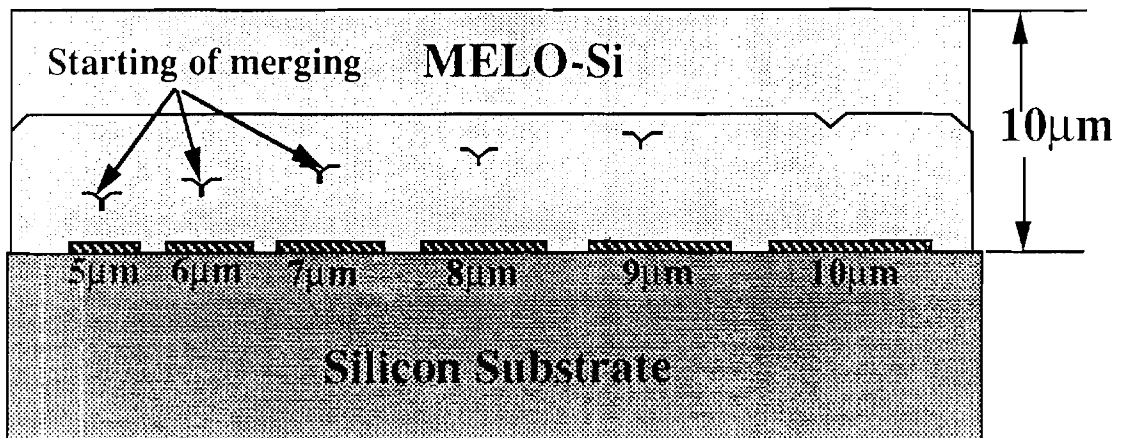
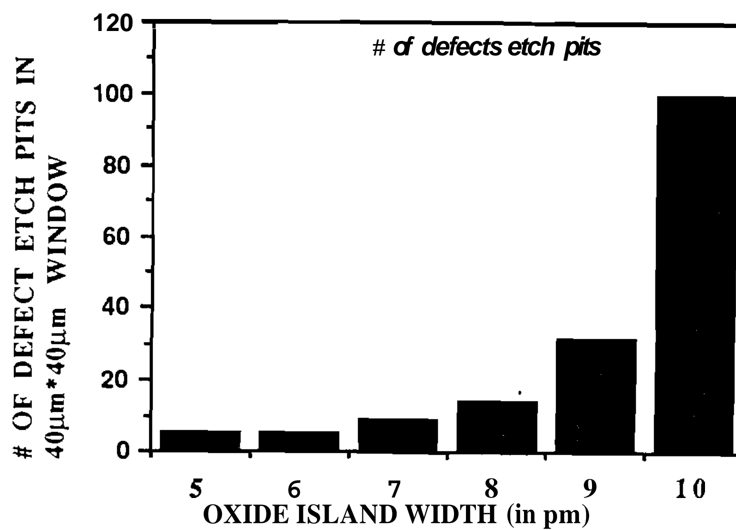
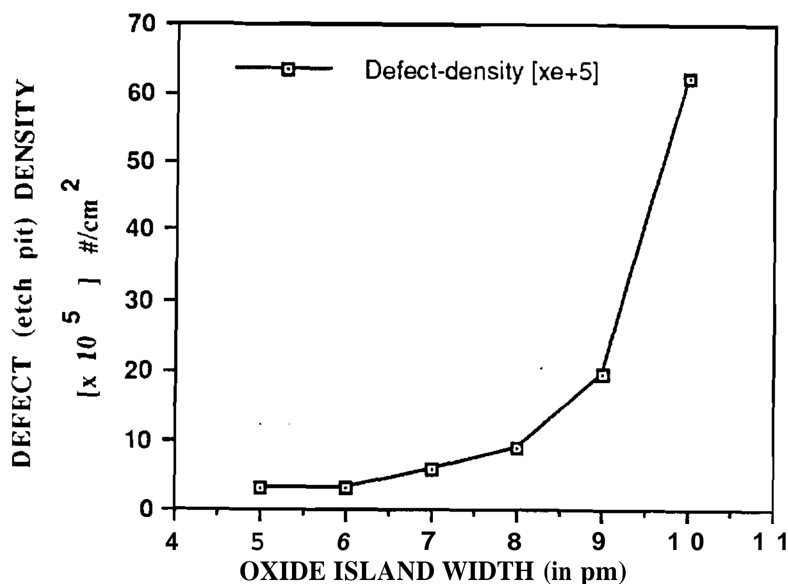


Figure 3.35 Merging on Oxide islands with different width in test mask.

In the accelerometer design, piezoresistors are fabricated on the top 1 μm out of a 10 μm thick MELO silicon film grown over a group of 5 μm wide oxide islands. As shown in Fig 3.36, both the number of defects and the defect densities over 5 μm wide oxide islands are minimum and are within a reasonable range. The test results of the p-n junction leakage current densities from the diodes fabricated on the 10 μm thick MELO film showed reasonable leakage. In fact it is lower than the leakage current data of the resistor on much thicker (≈25μm) epitaxial silicon grown on P^+ layer [80]. Therefore, for thick MELO film the dislocation faults resulting from merging are not playing a critical role in device performance. However for thinner MELO film a further research to reduce defect counts is recommended.



(a)



(b)

Figure 3.35 Results of Secco etching. **(a)** Graph showing # of etch pits vs. width of oxide islands. (b) Graph showing the variation of defect density with the width of the oxide island.

3.5. References

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CHAPTER 4
FABRICATION OF MELO-SI ACCELEROMETER

4.1 Introduction

This chapter details the structure and fabrication sequence of an IC compatible, bridge-type piezoresistive accelerometer utilizing the MELO-Si diaphragm fabrication technique described in Chapter 3. Standard circuit photolithography and diffusion processes provide pattern definition capabilities and stress-sensitive piezoresistors for the accelerometer output. Producing the mechanical structure, including its seismic mass and four supporting bridges (or beams), requires special masking and etching techniques in silicon. A description of the entire accelerometer precedes sections detailing the fabrication of its parts and the final assembly, and discussing difficulties along with solutions.

4.2 Structure of MELO-Si Accelerometer

The essential components of a bridge-type piezoresistive accelerometer are a seismic mass with supporting bridges, a mechanical-to-electrical transducing device, electrodes, and protection plates. The key process features which are unique to the accelerometer fabrication are front-to-back alignment, metal passivation during KOH etching, and reactive ion etching (RIE) for the front delineation, in addition to the diaphragm fabrication for the beams. All the above process features must be IC compatible in order for the accelerometer to be fabricated with other electrical devices on the same chip.

The picture of the Purdue MELO-Si accelerometer from the top is shown in Fig. 4.1. The center portion is the heart of the accelerometer, a seismic mass and the four very thin supporting MELO-Si diaphragm beams, completely surrounded by a thick rim. The rigid rim provides the "built-in" end condition at one end of the beams, a region for metal routing and contact pads, and this surrounding rim is a main part of the starting silicon wafers. The thin silicon diaphragm structure for four supporting bridges are fabricated by MELO-Si diaphragm technique described in Chapter 3. The seed windows and SiO_2 etch-stop layers were patterned on the area around the middle seismic mass for the MELO-Si formation. On the MELO-Si film, where the bridges will be delineated, stress-sensing

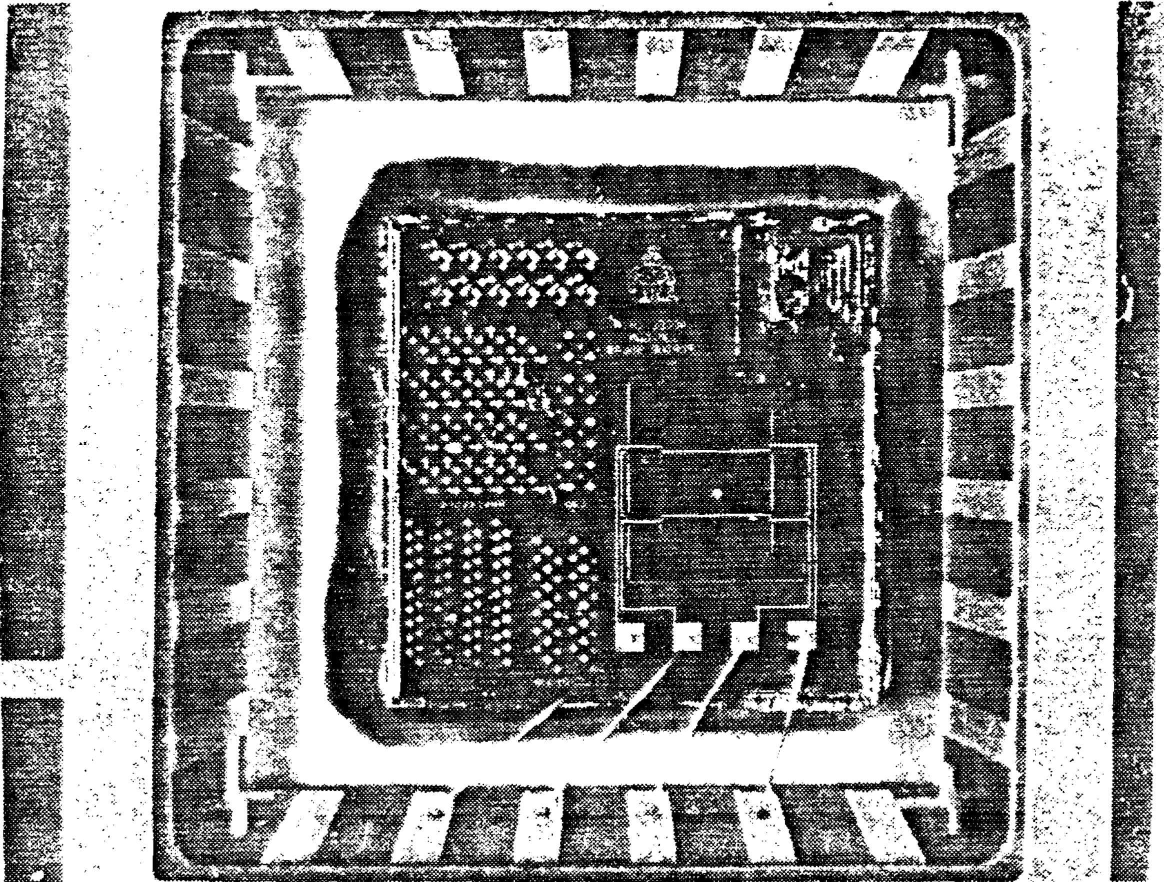


Figure 4.1 A photograph of the final packaged MELO-Si accelerometer from the top.

piezoresistors are fabricated and a Wheatstone full bridge circuit is configured by metallization and its patterning. At the same time, other electrical devices can be fabricated on the same die of the wafer. The circuit components on the front and the back side of the wafer are protected by a passivating film such as plasma enhanced chemical vapor deposition (PECVD) of nitride during the anisotropic etching. Then the back side of the wafer is patterned and the anisotropic etching is performed to complete the MELO-Si diaphragm formation. The diaphragm is first fabricated all around the middle seismic mass and the final four bridge structures are delineated by RIE from the front side of the wafer. The seismic mass was defined by anisotropic etching from the back side of the wafer at the same time when the MELO-Si diaphragm is produced.

4.3 Fundamental Principle of Operation

The basic behavior of the bridge-type accelerometer can be understood using an analysis of an ideal elastic straight beam whose left end is fixed and right end is guided as shown in Fig. **4.2.** The general differential equation of elastic curve has the following form for the system shown in Fig. **4.2;**

$$EI\frac{d^2y(x)}{dx^2} = M\ ;\ I = \frac{wt^3}{12} \tag{4.1}$$

where E is Young's modulus, I is the moment of inertia of the cross section in the yz plane about z axis, t is the beam thickness, w is the beam width, y(x) is the beam deflection along the x direction, and M is the bending moment in terms of x. The effect of an accelerometer on the beam and mass is modeled as a point load (or force), F, equal to the product of the mass and the applied acceleration perpendicular to the plane of the beam. The stress in this model of the accelerometer assumes that the beam thickness is much less than its length, that the load acts in a plane of symmetry of the beam, and that the normal stresses due to bending are not affected much by the presence of shearing stresses. Under those conditions, the deflection of the beam can be expressed as

$$y(x) = \frac{F}{12EI}(3lx^2 - 2x^3) \tag{4.2}$$

where F is applied force and I is the beam length. The stresses at the surface are

$$\sigma(x) = \frac{F}{I}(\frac{l}{2} - x)\ y(x). \tag{4.3}$$

For a rectangular cross section, the area moment of inertia about the centroid axis of the beam cross section is

$$I = \frac{1}{12}wt^3 \tag{4.4}$$

giving

$$y(x) = \frac{l^3}{wEt^3}\left[3\left(\frac{x}{l}\right)^2 - 2\left(\frac{x}{l}\right)^3\right] \tag{4.5}$$

$$\sigma(x) = \frac{12F}{wt^3}\left(\frac{l}{2} - x\right)y(x). \tag{4.6}$$

The placement of the sensing resistor affects the resistance change observed due to the variation of stress along the beam. Since the maximum stresses and hence maximum resistance change occur at $y=\pm\frac{t}{2}$, $x=0$ and l, the most advantageous placement of the resistors is on the surface of the beam at or near the fixed end and the guided end where the force is applied. The maximum stress, σ_o at $y=\frac{t}{2}$, $x=0$, can be expressed as

$$\sigma_o = \frac{12F}{wt^3}\left(\frac{l}{2}\right)\left(\frac{t}{2}\right) = \frac{3lF}{wt^2} \tag{4.7}$$

and $\sigma(x)$ becomes

$$\sigma(x) = \sigma_o\left[1 - 2\left(\frac{x}{l}\right)\right]. \tag{4.8}$$

With a shallow resistor ion implant or diffusion the stress acting to change the value of the resistor is

$$\sigma(x) = \sigma_o\left[1 - 2\left(\frac{x}{l}\right)\right] = \frac{3lF}{wt^2}\left[1 - 2\left(\frac{x}{l}\right)\right]. \tag{4.9}$$

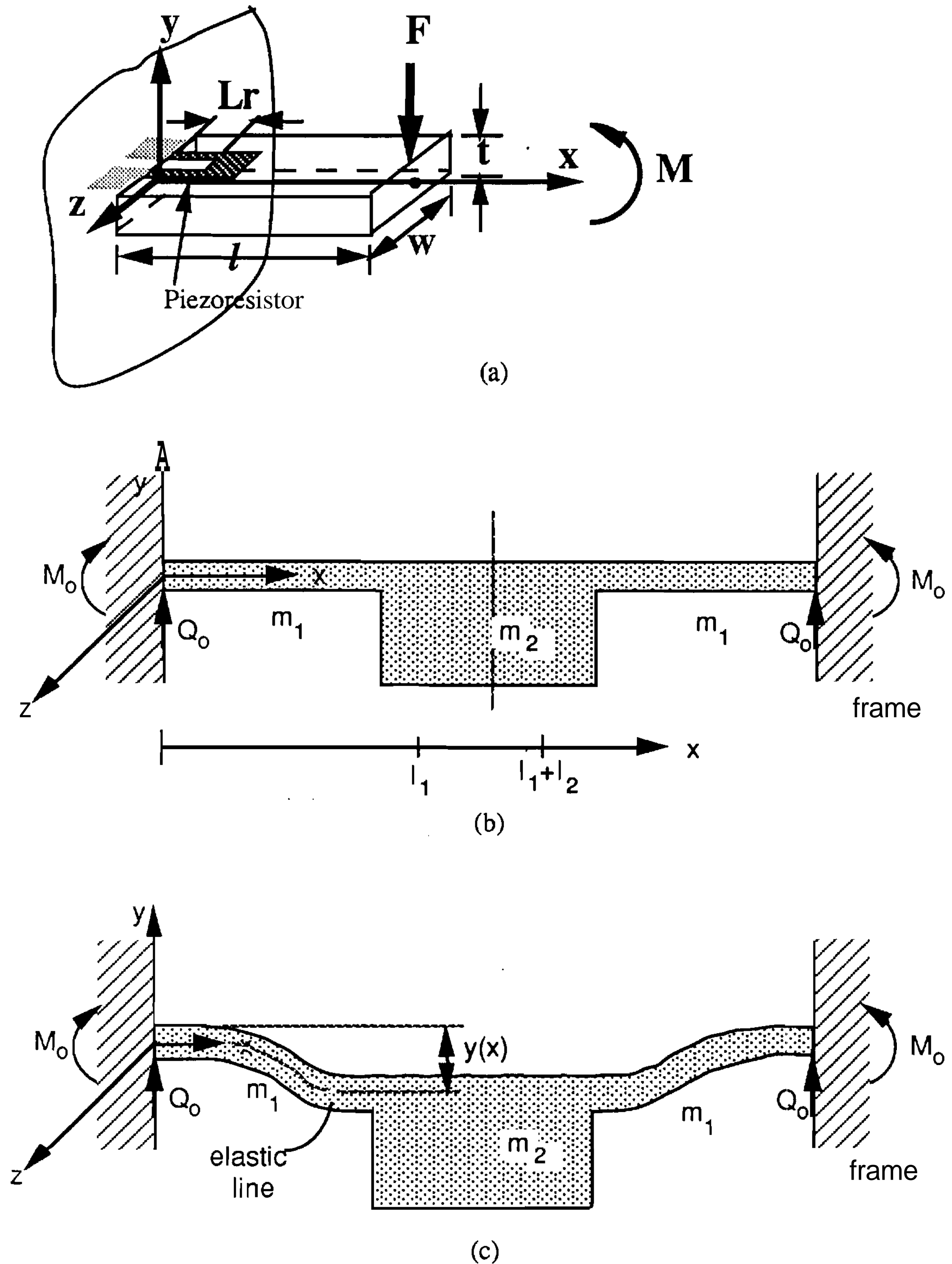


Figure. 4.2. Idealized model of a bridge-type accelerometer. (a) Ideal elastic straight beam with a bending moment at the end. (b), (c) are two-dimensional structure of a bridge-type accelerometer before and after deflection respectively.

The next step in driving the response to acceleration is to examine how the resistance varies with stress. The basic equation for the resistance R of a diffused resistor with resistivity p (in Ω-cm), length L(cm), and cross sectional area A(cm^2) is given by

$$R = \frac{\rho L}{A} \tag{4.10}$$

assuming the resistivity is uniform in the diffused region. The differential change in R with applied stress can be expressed as

$$dR = \frac{\rho}{A}dL - \frac{\rho L}{A^2} + \frac{L}{A}d\rho \tag{4.11}$$

and the fractional resistance change is

$$\frac{\Delta R}{R} = \frac{\Delta L}{L} - \frac{\Delta A}{A} + \frac{\Delta \rho}{\rho}. \tag{4.12}$$

The first two terms represent its dimensional changes of the resistor due to the applied stress and the last term represents the change of resistivity with stress, or piezoresistivity. Generally, however, the piezoresistive effect is much more significant than the dimensional changes in semiconductor and the first two terms can be neglected. Again, neglecting shearing stresses, the variation can be written as

$$\frac{\Delta R}{R} = \Pi_{//}\,\sigma_{//} + \Pi_{\perp}\,\sigma_{\perp} \tag{4.13}$$

where $\sigma_{//}$ and $\sigma_{\perp}$ are the stress parallel and perpendicular to the direction of the resistor in the plane of the resistor, respectively, and $\Pi_{//}$ and $\Pi_{\perp}$ are the corresponding piezoresistance coefficients, coupling stress and resistance change. For a p-type resistor oriented along <110> direction of the silicon lattice, it has been shown that

$$\Pi_{//} = \frac{1}{2}\Pi_{44} \tag{4.14}$$

and hence

$$\frac{\Delta R}{R} = \frac{1}{2}\Pi_{44}\,\sigma(x). \tag{4.15}$$

The stress, $\sigma(x)$, is not a constant along the length of the resistor and its average value needs to be found from the stress distribution along the length of the resistor and used in order to simplify the Eqn. (4.15). Integrating along the length of a resistor near the fixed end,

$$\bar{\sigma}(x) = \frac{\int_0^{L_r} \sigma(x)dx}{\int_0^{L_r} dx} = \frac{3F(l-L_r)}{wt^2} \quad (4.16)$$

where L_r is the length of the piezoresistor that was extended out on the bridge from the beam edge. Substituting into Eqn. (4.15), one finds

$$\frac{\Delta R}{R} = \frac{3\Pi_{44}}{2} \frac{(l-L_r)}{wt^2}. \quad (4.17)$$

The above resistance change can be converted to a voltage change using a Wheatstone bridge circuit configuration. Figure 4.2 shows that the elastic curve of the beam consists of both concave-down and concave-up curves which indicate both expansion and compression occur with the applied force. Therefore, by placing two resistors at or near both ends of the each beam, both positive and negative piezoresistive effects can be obtained with a stress. In a bridge-type accelerometer with four beams, eight equal resistors are placed. If the Wheatstone bridge circuit is driven by a voltage source, V_{cc}, for example, then the output voltage, V_o, would be

$$V_o = \pm\left(\frac{2R-2\Delta R}{4R} - \frac{2R+2\Delta R}{4R}\right)V_{cc} = \pm\frac{\Delta R}{R}V_{cc} \quad (4.18)$$

assuming $R_1 = R_2 = R_3 = R_4 = R_5 = R_6 = R_7 = R_8 = R$. Using this expression, the overall response of the accelerometer to an acceleration a can be obtained as

$$V_o = \pm\frac{3}{2}\Pi_{44}\frac{(l-L_r)}{wt^2}V_{cc}\,M\,a. \quad (4.19)$$

This equation indicates that the output is linear with applied acceleration and bridge supply voltage. The response to the acceleration is determined and varied by physical dimensions of the beam width, thickness, length, piezoresistor location, and doping concentration of piezoresistor. Particularly, the thickness control is more important that other parameters since it is only the squared term in the equation. The well controlled geometry is necessary for getting the desired output range.

4.3 Layout Design of MELO-Si Accelerometer

The MELO-Si accelerometer fabrication process, including BJT device fabrication, consists of 9 masking steps as listed in Table 4.1. Each masking step and its design are described in this section.

Table 4.1 Description of MELO-Si accelerometer mask levels.

Mask #1	Alignment Marks after MELO process
Mask #2	Seed Window Patterns for MELO Silicon
Mask #3	Piezoresistors Pattern
Mask #4	Base (in BJT device) Pattern
Mask #5	Emitter (in BJT device) Pattern
Mask #6	Contact Definition
Mask #7	Metal Pattern
Mask #8	Back Etch Pattern
Mask #9	Front Delineation for Beams and Proof Mass

The size of the designed MELO-Si accelerometer is 3 mm x 4 mm including the frame for the metal bonding pads and the beam is 10 μm thick, 420 μm long, and 170 μm long. However, the die size is 7 mm x 7 mm and the rest of the area is for the fabrication of other electrical devices such as resistors, diodes, BJT devices, capacitors, and gate-controlled diodes on the same die for evaluating the MELO-Si material quality as well as process procedures. The layout of the whole die is illustrated in Fig. 4.3.

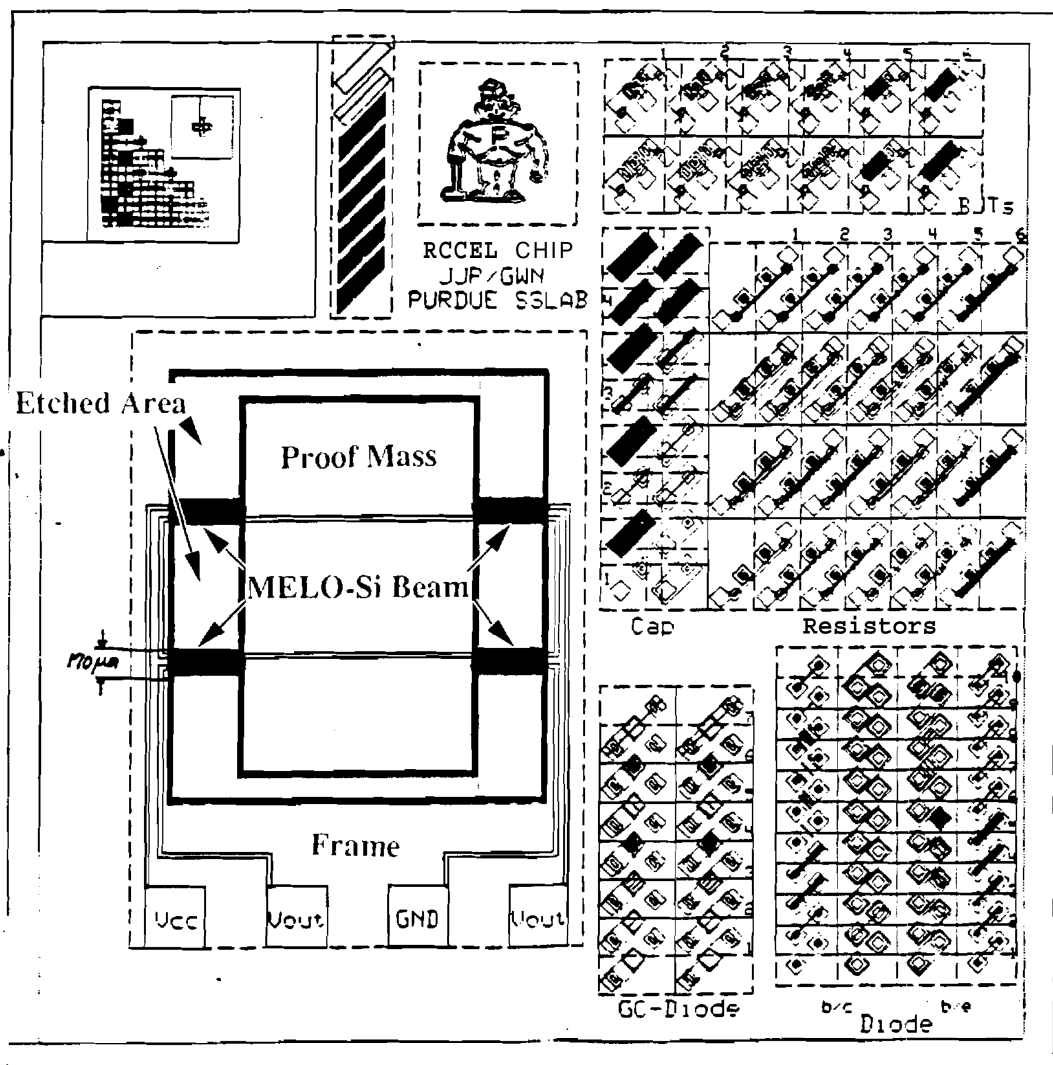


Figure 4.3 Layout of Purdue MELO-Si accelerometer die. The die size is 7 x 7 mm² (272 x 272 mil²) and accelerometer size is 3 x 4 mm². There are other electrical devices, in addition to the accelerometer, for evaluating the MELO material and process procedures.

The first step is to make alignment marks on the top that will maintain their shapes after the MELO process. Ideally the ELO process grows silicon equilaterally over the adjacent oxide masks from the seed window. However, if the lateral growth rate of silicon varies in different directions, then the oxide alignment pattern will be covered differently according to the different lateral silicon growth. This tends to shift the alignment marks and the subsequent alignment won't be properly registered. When the width of the alignment marks is so narrow that the ELO silicon merges on the alignment marks, then the alignment marks will be washed out and further alignment will be impossible. Therefore, in this process, the first alignment marks were made with PECVD nitride and they were designed to be covered by the large oxide area in the next level. PECVD nitride alignment marks then won't be affected by the subsequent MELO process and maintain their original shapes through the whole process. This is illustrated in Fig. 4.4.

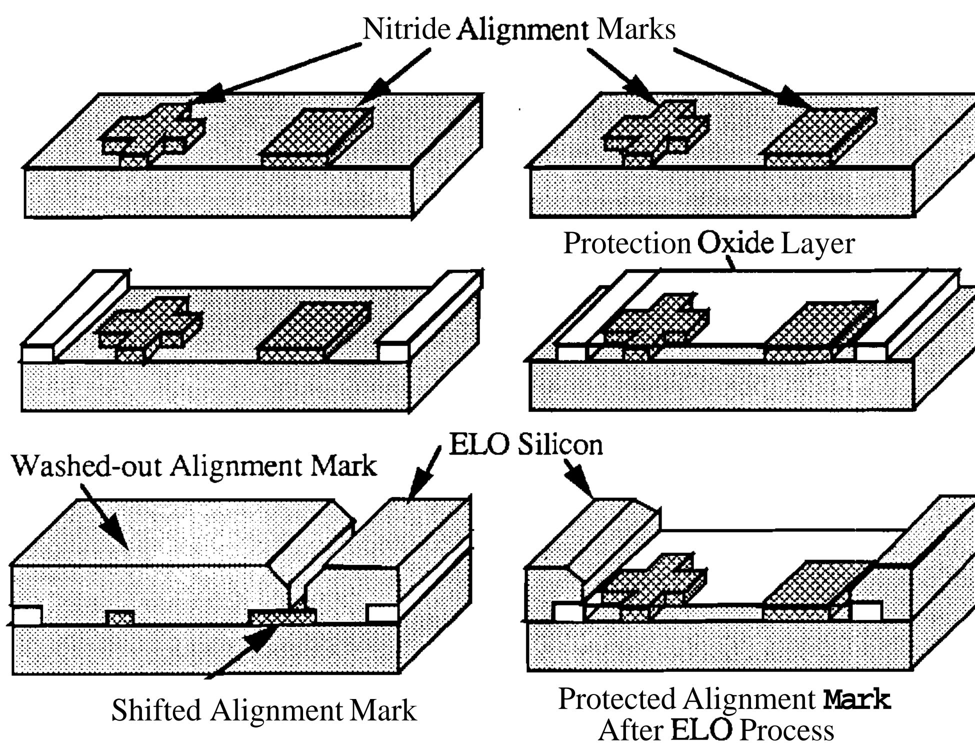


Figure 4.4 Schematic diagram of the washed-out and shifted alignment marks caused by the ELO process and the protection of the alignment marks with an additional mask step.

The MELO process, after the front alignment pattern definition, starts with thermal oxidation of the (100) silicon. The oxide smps were then patterned along the <100> direction for the thin MELO-Si diaphragm formation in the area surrounding the proof mass. The oxide smps were extended into the mass area in one direction and into the rim in the other so that it allows tolerance for the misalignment. When the MELO-Si diaphragm is fabricated around the proof mass by KOH back etch, the whole diaphragm provides more mechanical strength until the bridges are defined by the front delineation. The width of the silicon dioxide smps was determined as 5 μm and the space between them as 2 μm in order to work comfortably in the Purdue University Solid State Laboratory. The thickness of the oxide was chosen as 1 μm so that oxide smps effectively stop KOH back etch when the KOH solution reaches the oxide under the MELO-Si diaphragm. Seed windows are aligned to the <100> direction for the best quality MELO silicon. MELO silicon growth was performed with a Gemini I reduced pressure RF heated epitaxial reactor. An in-situ precleaning cycle of a 5-min hydrogen bake and a 30 sec. HCl etch at 970 °C or 1020 °C and at 150 Torr or 40 Torr were performed just prior to the silicon growth. The HCl-to-SiH_2Cl_2(DCS) gas flow ratio was set to produce a silicon growth rate of about 0.1 μm/min. at a certain temperature and pressure. For an example, at 970 °C and at 40 Torr, the growth rate of 0.2 μm/min was obtained at the HCl and DCS flow rate of 0.64 *l*/min and 0,22 *l*/min respectively.

The following steps are piezoresistor definition, the base and emitter definition of BJT devices, contact definition, and metal deposition and patterning. All of these are considered as standard IC fabrication technologies. The p-type piezoresistors are aligned to the <110> direction for their highest resistivity; i.e. the most resistance change induced by the applied stress. Their junction doping concentration and junction depth were designed to have a sheet resistance of 212 Ω/square and a junction depth of 1 pm. The general rule is to make the junction depth of the piezoresistors less than or equal to 10% of the silicon diaphragm thickness. Since the ion implant is done without an oxide buffer layer, the ion implant had to be done at the lowest possible energy available at Purdue University Solid State Laboratory, 25 KeV, in order to achieve a shallow junction depth. The resistance value of one resistor was determined such that the stress sensitivity of the piezoresistors is reasonably good while the 'temperature sensitivity is low. SUPREM III process simulator was employed to determine the ion implant dose and drive-in time for the desired junction depth and sheet resistance at 25 KeV. The dose of the boron as $1 \times 10^{15}/cm^2$ and wet oxidation drive-in at 1000°C for 30min were selected. As shown in Fig. 4.5, the peak carrier concentration and junction depth of a piezoresistor become $1 \times 10^{18}/cm^3$ and 1.0 μm

after 30 min drive-in. Its corresponding sheet resistance is 212 Ω/square and the resistance of each piezoresistor would be 3 kΩ since 15 squares were employed in one piezoresistor. The U-shape piezoresistors were selected for an easy metal connection and higher sensitivity as compared to the I-shape. Two resistors were fabricated on each bridge and each resistor was placed such that the end of the beam crosses the resistor lengthwise since the both ends produce the maximum absolute stress values as shown by Eqn. (4.6). The drive-in time was divided into two parts so that BJT devices can be fabricated at the same time.

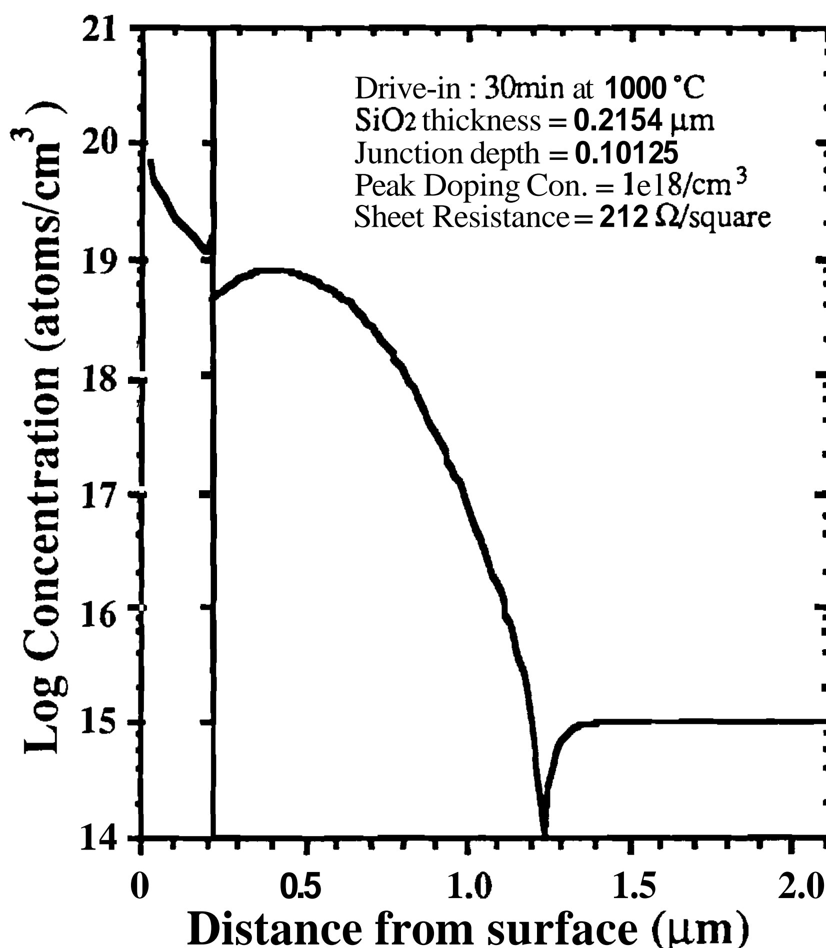


Figure 4.5 SUPREM III process simulator output plot for determining the boron ion implant dose, energy, and drive-in parameters. The resulting junction depth and sheet resistance of a piezoresistor become 1.0µm and 212 Ω/square respectively.

The thickness of the thermal oxide mask for the boron and arsenic ion implant was also determined by SUPREM 111 process simulator. The value was chosen such that 95% of the implanted boron will be masked by the oxide. For the piezoresistors, the boron dose is 1 x $10^{15}/cm^2$ and 4000 Å of thermal oxide is necessary. By the same token, for 1 to 3 x $10^{13}/cm^2$ of base dose and 1 to 3 x $10^{15}/cm^2$ of emitter dose, 1500Å and 1000Å of thermal oxide are needed respectively. The drive-in for the piezoresistors was divided into two; the first 15 min. with the base drive-in after both boron implant and the next 15 min. with the arsenic drive-in. The collector contact region was patterned and implanted with the emitter with the same mask level (mask #5) so that an ohmic contact can be made to the collector. The test devices were fabricated on SEG and MELO silicon for silicon material characterization. The number and location of the silicon dioxide smps under the MELO silicon are varied such that their effect on the device character can be analyzed. After the emitter drive-in, the contacts were defined (mask #6) and metal deposition was performed. Al-1%Si was deposited using a Perkin-Elmer Sputtering System at 100 Watts, 8 mTorr, for 30min, resulting in 2500Å thick metal. The effect of the metal deposition and the following processes on the passivation layer will be discussed later in this chapter in more detail. The metal is then patterned by wet etching and annealed at 400°C for 20min. At this stage, the devices are ready to be tested but the accelerometer needs further processing steps.

The next step is the fabrication of a thin MELO silicon diaphragm by KOH back etch. The front circuits and metal pattern need to be protected during a lengthy KOH etch. Plasma enhanced chemical vapor deposition (PECVD) of nitride was deposited on both sides of the wafer as a protection on the front side and as a mask on the back side. The problems associated with metal passivation and their solutions are discussed in the following section. The back-etch windows were patterned (mask #8) for KOH etch using a thick (~6µm) A24620 photoresist as a mask. They were patterned by reactive ion etch, but they also can be patterned by BHF wet etch, or combination of both. The front side was also protected by AZ1350 photoresist, or AZ4620 photoresist when only BHF etch is used, while patterning the back side. It is important to pattern the etch windows without damaging other passivation areas because the damage on the passivation layer would be attacked during a long KOH etch, resulting in the etched metal and silicon. It is also important to remove the nimde or oxide layer completely from the patterned area for a uniform KOH etch over a wafer. If a thin nitride/oxide layer is left in some patterns, then it will cause a considerable non-uniform etch over a wafer. Also additional KOH etching

time is required for removing the silicon under the MELO-Si diaphragm. This longer etch time will enlarge the etch window by having more lateral undercut and result in a low yield.

The front side wafer delineation can be done either before or after KOH back etch. At first, The front delineation was designed to be done before KOH etching in order to make the KOH etching as the very last step since any further photolithography seemed improper due to the weakness of the thin silicon diaphragm. However, by attaching the accelerometer wafer, after KOH etch, to another back plate wafer it became possible to have an additional photolithography step due to its enhanced mechanical strength and hence the front delineation after KOH etch became possible as well. In addition, the front delineation before KOH etching creates a big step on the front of the wafer and results in a poor passivation during KOH etching. Therefore, the order the front delineation was changed to be the very last step in the accelerometer fabrication process.

4.4 Process Development

In fabricating the MELO-Si accelerometers, there were some obstacles in the fabrications. In this section, some of the critical fabrication issues and their developments are presented. They include front-to-backside alignment, piezoresistor fabrication parameters, metal passivation during KOH anisotropic etching, corner compensation in KOH anisotropic etching, and front delineation. .

4.4.1 Front-to-Backside Alignment

MELO-Si diaphragm was fabricated by etching silicon from the back side of the wafer, and hence a front-to-back alignment technique was required. This alignment is important since the piezoresistors need to be placed on precise locations over the diaphragm to take advantage of the stress pattern of loaded diaphragm beams. Misalignment of the piezoresistors from the right locations of the beams will result in the reduced sensitivity or the functional failure of the accelerometer.

Front-to-backside alignment of silicon wafer has been investigated along with silicon micromechanical sensor development as it is often necessary to carry out bulk micromachining accurately. Several techniques have been developed including the use of special mechanical jig [1, 2], etching of several alignment mark holes by anisotropic etching completely through the wafer [3], and infra-red mask aligner. The use of the special jig and the alignment holes will suffer alignment error due to a mechanical misfit

and lateral etch of the anisotropic etch respectively. In this MELO-Si accelerometer fabrication, KARL SUSS double-sided mask aligner was utilized to align the front and back of the wafer. Using a double-sided mask aligner is non-destructive method since it avoids making holes in the wafer and can improve the alignment of both sides.

4.4.2 Piezoresistors

The piezoresistors are produced with standard IC techniques. Their patterns were defined by a photolithography in a SiO_2 masking layer and the doping impurities are introduced by ion implant for a good control of shape and concentration. Resistance values are set by the length to width ratio of the doped region and its resistivity in Ω/square which depends on the implanted dose and high temperature drive-in process. As described in chapter 2, a single piezoresistive coefficient, π_{44} for p-type silicon and π_{11} for n-type silicon, dominates silicon's behavior for applied stress [4]. The resistor must therefore be oriented on the beam in a direction which gives a large coupling coefficient between the longitudinal stress in the beam and the resistance. In effect, the orientation of the beams is determined as well, because the components of stress parallel and perpendicular to the axis of the resistors are determined by the longitudinal axis of the beams. In (100) silicon, the beam and resistor axes should coincide with <110> directions for maximum piezoresistive effect with p-type resistors, and with <100> directions for n-type resistors.

While the orientation and resistivity type are major factors in achieving a large coupling coefficients, other factors need to be considered for the piezoresistors doping concentration. The piezoresistive coefficients are a function of impurity concentration, as are the temperature coefficients of resistance [5]. The dominant piezoresistive coefficient increases with decreasing surface impurity concentration of the diffused layer, reaching its limiting value at a surface concentration of 10^{17} cm^{-3}. However, the temperature variation of the piezoresistive coefficients has the opposite dependence on concentration. The impurity concentration also determines the range of resistance which can be achieved, given constraints on resistor length, width, and junction depth. The optimum impurity concentration for p-type piezoresistors, in order to make its temperature coefficient of resistance to be canceled. by temperature coefficient of the gage factor, are around $N_A \approx 10^{18}$ or 10^{20} cm^{-3} [5]. At these impurity concentrations, theoretically, the piezoresistance coefficients are least influenced by the temperature change. Therefore, the impurity concentration and final resistance of the piezoresistors were designed as described in section 4.3.

4.4.3 Fabrication of MELO-Si Diaphragm and Proof Mass by KOH Etching

After the circuit fabrication and metal pattern are completed, the next step is the fabrication of a thin MELO-Si diaphragm and a proof mass at the same time by KOH etching. In this section, the development of KOH etching system, the passivation layer for KOH etching, MELO-Si diaphragm fabrication, and the comer compensation design of the proof mass are discussed.

4.4.3.1 Development of KOH Etching System

Controlling the etch rates of various crystallographic planes are important because they are used to determine the pattern dimensions and the final structure of the etched silicon. The etch rates of different crystallographic planes vary depending not only on the concentration ratio of the etchant components but also on the etching temperature. According to Price's work [6], the anisotropic ratio of (100) to (111) etch rates appears to be at a maximum for 30 weight percent (w%) KOH without isopropyl alcohol (IPA) and 40 w% KOH with IPA. For (110) to (111) planes, the anisotropic ratio peaks around 35 to 45 w% KOH without P A and reaches a constant value beyond 50w% KOH with IPA. Price indicated that IPA acts as an additive that enhances preferential selectivity of the crystal. For a KOH etchant without IPA, the etch rate of (110) place can be greater than that of (100) plane while for a KOH etchant with IPA the (100) etch rate is always greater. In general, the etch rate decreases as IPA concentration increases for all crystallographic planes. Palik [7] suggested after the Raman spectroscopy experiments that IPA does not participate in the etching process but perhaps acts as a coating, thereby reduces the etch rate

The morphology of the etched silicon surface also varies depending on the etchant components. The bottom surface etched by KOH etchant is usually smooth for KOH concentration below 30w% [8] provided that the starting wafer surface is smooth and clean. However, at higher KOH concentration, pyramids tend to form more frequently. The pyramids, once they appear during the KOH etching, will continue to keep their shapes and cause the KOH etching non-uniformity during diaphragm formation.

For the fabrication of MELO-Si diaphragm and proof mass, high vertical etch with low lateral etch rate at the same time is desirable to reduce undercuts on the mask for a good control of the lateral dimensions. Therefore, alcohol (n-propanol) plays a significant role in the KOH etching because it reduces the severity of the undercuts as described before. Increasing the temperature beyond 80 °C will confound the functionality of the n-propanol since it may evaporate away during the etch due to its boiling point, –97.3 °C. If

an azeotropic effect is occurring between water and n-propanol within the KOH solution, then the azeotropic boiling point is lower, ~87°C [9]. Hence, even if the temperature is below the boiling point of the n-propanol, the increase of the temperature above 80 °C may cause severe undercut which was initially prevented by the n-propanol. Also, when the n-propanol evaporates, so does water, and the solution concentration will vary accordingly, Therefore, choosing 80 °C as the operating temperature is for having a high vertical etch rate without changing solution concentration substantially.

For consistent etching results, it is desired to minimize the temperature variation of the KOH etching solution, preferably less than or equal to ± 1°C. Therefore, a chemical etching system was designed as illustrated in Fig. 4.6. There are two objectives of the chemical etching system: (1) the precise controllability of the operating temperature, and (2) the preservation of the n-propanol during etching. First, a stable etching temperature will reduce the fluctuation in the etch rate because the etch rate increase with the temperature. Therefore, a temperature controller, monitoring the etching system, was required to maintain a steady temperature. Secondly, a semi-enclosed system prevents the n-propanol from escaping too quickly since the n-propanol condenses at the top cover and drips back to the etching solution. This helps to sustain the content of the n-propanol in the etchant and to reduce excessive n-propanol vapor out of the system, which can be a potential danger.

The KOH etching system consists of a temperature controller, a j-type Teflon coated thermocouple as a temperature probe, a quartz wafer holder, 1 liter Pyrex beaker for water bath, 800 ml Pyrex beaker for KOH solution, and a hot plate. A thermocouple is placed in the water bath instead of the KOH solution because the water bath acts as a constant heating source as well as a buffer between the KOH etchant and both the cool air and the hot plate. To keep a steady temperature, the temperature controller adjusts the cycling of the hot plate and the magnetic stirrer according to the measured water bath temperature. To let the heat flow throughout and around inner beaker,,the inner beaker must be slightly raised; this also allocates a space near the hot plate for stirring. Hence, the feature promotes constant heating along the side and bottom of the inner beaker. Therefore, when the system is at equilibrium, the etchant will be heated close to the temperature of the bath water. To be certain that the etchant would reach close to the water bath temperature, a mercury thermometer is placed inside the etchant through an opening in the lid. A vent is built into the lid to sustain pressure equilibrium. The KOH etchant is agitated by the hydrogen released while silicon is being etched. With this design KOH etching system, it became possible to achieve ± 1°C temperature variation during normal etching conditions.

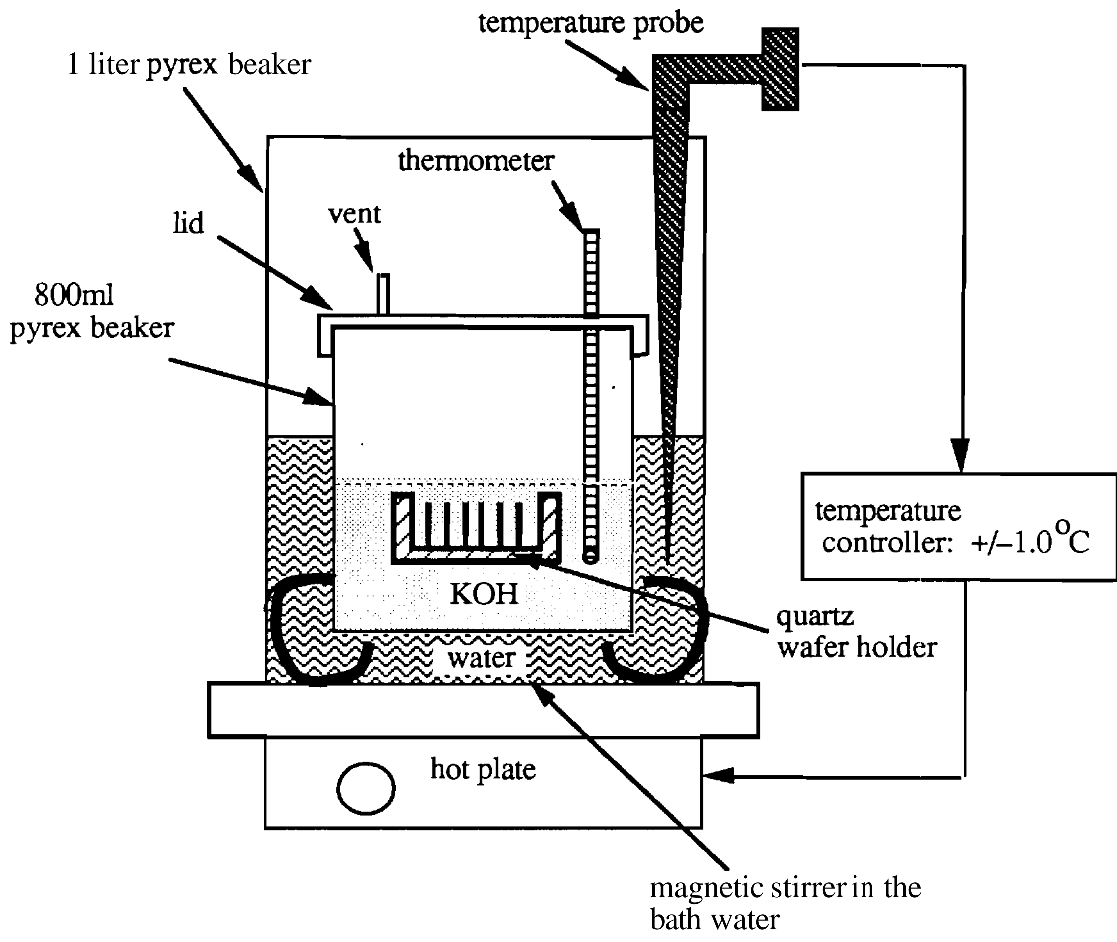


Figure 4.6. KOH etching system using beaker-within-beaker arrangement and Omega temperature controller [10].

4.4.3.2 Passivation Layer for KOH etching

In order to define the etching region, a protective layer must be used to cover the silicon wafer. The most popular masking films are silicon dioxide (SiO_2) and silicon nitride (Si_3N_4). In KOH solution, however, Si_3N_4 is a preferred passivating layer than SiO_2 because Si_3N_4 has a lower etch rate and SiO_2 tends to be damaged after a while by the KOH etchant. Plasma Enhanced Chemical Vapor Deposition (PECVD) or Low Pressure Chemical Vapor Deposition (LPCVD) techniques can be used to form Si_3N_4.

From the etching experiments without deposited metal, silicon nitride deposited by low pressure chemical vapor deposition (LPCVD) at 800°C served as the best passivation layer with a minimum lateral undercut. Also, LPCVD nitride can be deposited more

conformally and hence should be able to protect the metal edge better than PECVD nimde. However, LPCVD nitride can not be used with Al-Si metal pattern due to its high temperature requirement. The passivation layers available with Al-Si metal pattern are silicon nitride(SiN_x) and silicon oxide (SiO_x) deposited by plasma enhanced chemical vapor deposition (PECVD) due to their low deposition temperature. The low temperature process required for the passivation layer is due to the choice of the metal, Al-Si, which is easily available and good for silicon IC processing. Table **4.2** shows the differences between PECVD and LPCVD nimde film characteristics.

Table **4.2** Comparison of PECVD and LPCVD nitride film characteristics.

	PECVD Nitride	LPCVD Nitride
Deposition Temperature	- 300 °C	- 750 °C
Surface Coverage	Less Conformal	Conformal
Required Thickness	≥ 3 µm	- 0.2 µm
Cracks appear	≥ 5 µm	2 0.4 µm
Lateral Undercut	more than LPCVD	small

PECVD nitride, instead of oxide, was deposited on the Al-Si layer as the passivation layer and examined its endurance in the KOH etchant. A thick (> **3** µm) PECVD nitride protected the silicon surface and AL-Si metal pattern quite well as shown in Table **4.3.** However, too thick of a passivation film applies stress to the silicon wafer and may result in cracking during the KOH etch. PECVD $SiN_x/SiO_x/SiN_x$ multiple layer was also examined instead of one thick passivation layer so that PECVD oxide can act as stress relief material between the nitride sandwich. According to the results in Table 4.3, the multiple layer seems to work the best thus far, but the whole deposition takes a much longer time than a single passivation layer deposition because the PECVD chamber and electrodes need to be cleaned before each deposition. Also, removing those three passivation layers will require three different etching steps whereas it takes only one reactive ion etching (RIE) step to remove the thick PECVD nitride.

Table 4.3 Number of good MELO accelerometer dies after 5-hour KOH etch with different Al-Si deposition pressure and different passivation layers for comparison.

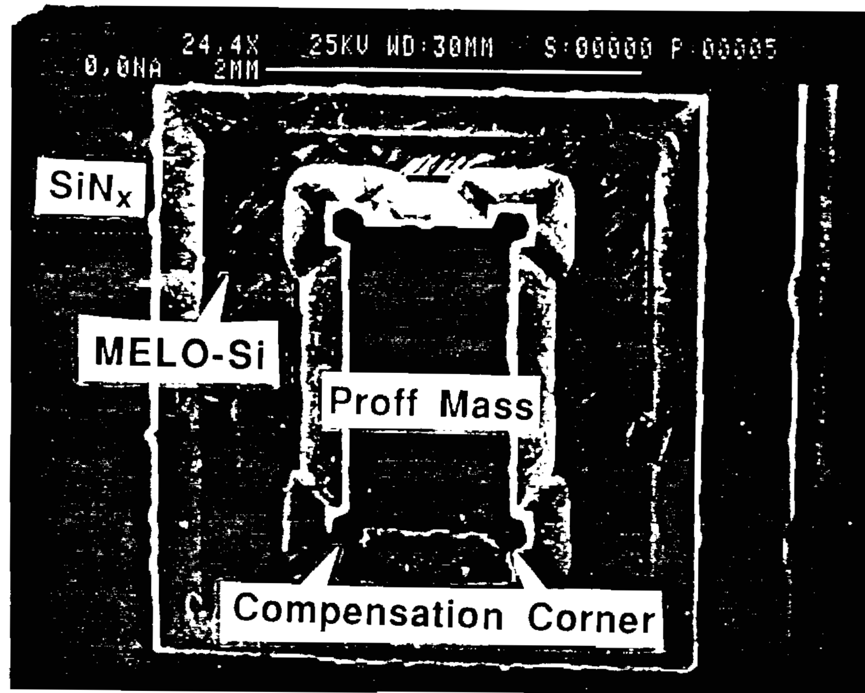
Sputter Deposit Base Pressure (Torr)	Single PECVD SiN_x (about 3 μm)	PECVD $SiN_x/SiO_x/SiN_x$ (2μm/1μm/0.7μm)
2 x 10^{-7}	10 out of 26	40-47 out of 50
3 x 10^{-7}	< 15 out of 50	< 25 out of 50

4.4.3.3 MELO-Si diaphragm fabrication

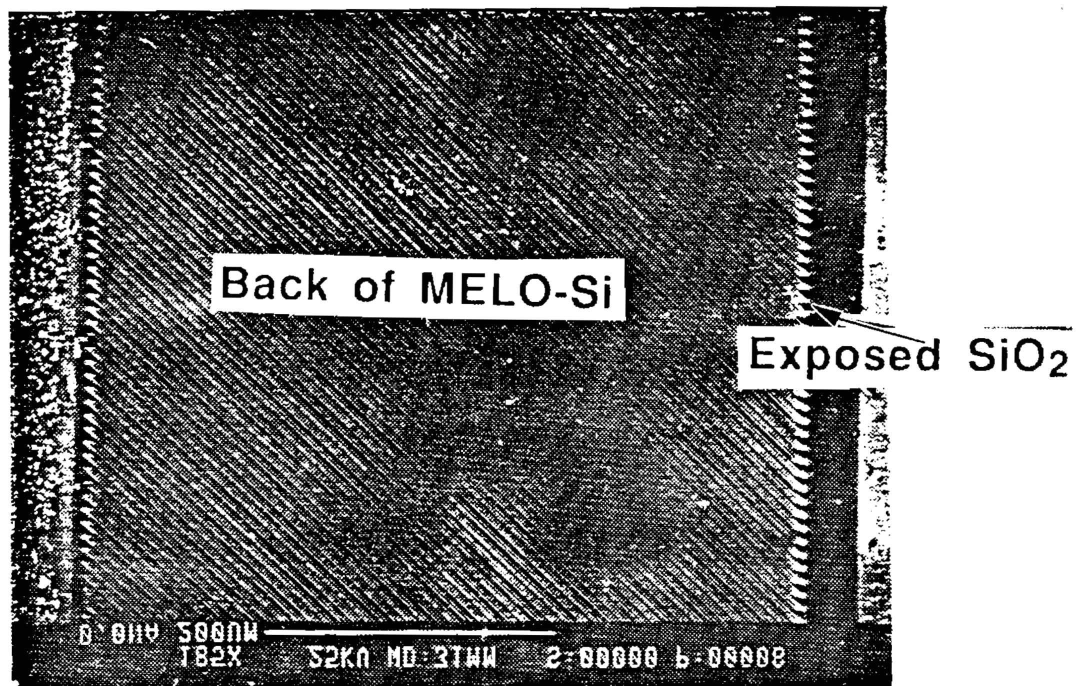
The KOH etchant which was used for MELO-Si diaphragm formation consists of 63.25w% deionized (DI) water, 13.34 w% n-propanol, and 23.41 w% KOH pallets. They correspond 127 ml DI water, 39 ml n-propanol, and 47 mg KOH pallets, respectively. The entire etching takes 5 to 6 hours depending on the KOH etchant temperature fluctuations, the original wafer substrate thickness, and the number of wafers (loading effect). The etching was performed in the chemical etching system which was described before, by controlling the temperature with the temperature controller. Figure 4.7 illustrates the SEM pictures of (a) the back of the MELO-Si diaphragm surrounding the proof mass and (b) the enlarged view of the back of the MELO-Si diaphragm in the bridge area.

Because the oxide islands used to create SEG are sandwiched between the epitaxial layer and the substrate silicon, etching for a period of time from the substrate silicon would mean that the oxide islands are exposed before continual etch into the epitaxial layer. There are two properties that accounts for the successful use of the oxide islands as the etch-stop layer: (1) the etch rate of the oxide layer is much lower than silicon and the oxide layers can be differentiated from the silicon by visual inspection and (2) the small seed windows have a lower etch rate due to the limiting crystal planes.

Since the oxide film colors under white light and has a low etch rate (relative to silicon) in the KOH solution, the strips of oxide islands can be easily observed during KOH etching and do not quickly dissolve into the KOH etchant once the substrate silicon is etched away. A concern, at this point, is the effect of the KOH solution on the SEG seed windows aligned across the beam. On the (100) wafers, V-grooves can be formed during concave etching (Section 3.2.1). This is especially true if the etching windows are kept to small dimensions. Since a seed hole between the oxide islands has a small width, V-grooves are serially formed across the length of the beam from backside KOH etching. However, since the long rectangular SEG windows are aligned to <100> direction, striated



(a)



(b)

Figure 4.7. SEM pictures of the rear view of a resultant MELO-Si diaphragm after a long KOH etching. (a) MELO-Si diaphragm surrounding the proof mass. (b) Enlarged view of the MELO-Si diaphragm in the bridge area.

planes will bound the V-grooves instead of the smooth (111) planes, as illustrated in Figure 3.16(a). Yet, since the striated planes forming the V-grooves consist of both (110) and (111) planes and since the width of the seed window is small, lateral undercutting would not be severe. If KOH etching is allowed to continue, the V-grooves can deepen into the epitaxial beam. In this case, a very thin epitaxial silicon beam can be punched through. Therefore, it is important that during the last few minutes of KOH etching, visual inspection for the oxide color is done periodically.

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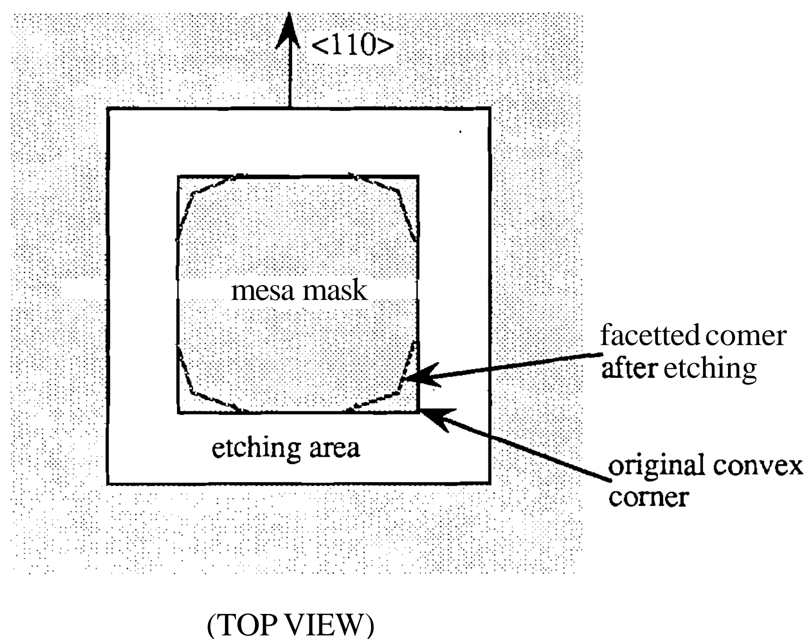
4.4.3.4 Corner Compensation of the Proof Mass

Although the beam is crucial to the accelerometer, the mass suspending from the beams is just as important because it plays a role in the sensitivity of the accelerometer. In a batch processing of the accelerometers, repeatability in the mass size is desired. So, the behavior of mesa etching is a necessary knowledge to determine the mesa shape. Therefore, from being able to determine the mesa shape, the weight of the accelerometer mass can be repeated from run to run. Therefore, convex etching of the mass or mesa will be discussed.

The anisotropic etching for fabricating a MELO-Si diaphragm described in chapter 3 is called a concave anisotropic etching, or a basin etch, since the etched shape is a trench on

the wafer surface. In concave etching, the etched shape is controlled by the most slowly etching planes. However, the accelerometer proof mass exposes a mesa shape after the anisotropic etching, and hence it is called a convex etching or a mesa etch. In convex etching, the etched shape is controlled by the fastest etching planes [11-13], particularly at the convex comers. Therefore, the convex corner undercutting ultimately reduce the size of the mesa which is the back of the proof mass. In addition, the faceting phenomenon of the convex comers basically creates two extra traces on the wafer surface for each convex corner encountered in a geometry. For example, if a rectangular pattem is used to create a mesa, each comer on the rectangle may have two extra faceting planes connected to the side walls of the rectangle, shown in Fig. 4.8. Therefore, the convex comers of a rectangular mesa will not be lines created from the intersections of the side wall planes. The possibility of having comer facets at each convex comer depends on the direction of the wafer surface as well as the orientation of the pattem relative to the wafer surface.



(TOP VIEW)

Figure 4.8 Faceting of convex comers after anisotropic etching, with mask aligned to <110> flat on a (100) wafer.

The convex comer undercutting is associated with the depth of the etch [11, 12]. Several researchers have presented their experimental results and theoretical analyses about the convex corner undercutting and tried to control the convex corner shapes during anisotropic etching process. The convex comer facets are different depending on the wafer orientation, the direction of the pattem relative to the wafer surface, and etching solution. However, under the same conditions, the facets have been identified differently. The facets which were generated by KOH etchant with IPA on a (100) wafer with a rectangular shape mesa aligned to the <110> direction were identified as (331) planes by Bean [11], and {212} by Wu and Ko [14]. It was also presented that different etching solutions such as KOH etchant without IPA and Ethylenediamine-based solution expose different facets [12, 15-17]. Nevertheless, all authors agree that corner faceting is inevitable for sharp corners and can be corrected to a certain extent.

Since an absolute agreement about the corner facets orientations has not been reached, likewise the suggested correction techniques of the corner undercutting are different [11, 12, 14, 16, 17]. However, the ideas, in general, can be classified into two categories: (1) addition of a compensation mask to protect the convex comers from undercutting and (2) alignment correction of the mesa pattem relative to the wafer flat or to <110> direction. The first idea is considered as the better choice because it can be applied into any orientation of the mesa. The corner compensation mask would act as a buffered area for undercuts to occur and the resultant corner becomes a sharp 90" convex corner trace on the (100) wafer surface. Further etching of a given compensation mask would result in comer undercuts again. Therefore, the ability to identify the convex comer facets is important in obtaining the most effective comer compensation pattern. The general approach to determining the shape and the dimension of the compensation mask is to estimate the plane of facets, the ratio of comer undercut relative to the etched depth, and then the relative dimension of the mask based on crystalline geometry.

The criterion to designing a compensation mask by superimposing an additional shape is that the receding peaks of the convex comers under the compensating pattern have to reach the main mesa tip simultaneously when the specified etched depth is reached. K. E. Bean proposed a square mask that overlaps each comer of a mesa for compensating the effects of corner undercuts [11]. Abu-Zeid attempted to modify the square corner compensation mask by superimposing rectangles and creating various shapes of the design [12]. Neither Bean nor Abu-Zeid designed a comer compensation specifically based on the corner faceting planes, though. A novel corner compensation design made by X. Wu and W. H. Ko [14] is the first design which utilized the corner faceting planes. They defined

the trace line of the fastest etched plane on (100) wafer experimentally and described the extent of comer undercutting by normalizing the etched distance of this trace line by the etched depth. Then, by crystalline geometry, a triangular pattem defined by the equivalent trace lines is designed to surround the convex comer as illustrated in Fig. 4.9. One disadvantage of this method is that its length takes up a large space and its improved version was introduced by B. Puers and W. Sansen [17]. They incorporated rectangles and flat triangles in order to reduce the space that the whole triangle takes as shown in Fig. 4.9. Recently, R. Buser et al. introduced an alternative comer compensating method for pure KOH etchant, called <100> oriented compensation mask . This method utilizes a rectangular strips oriented 45" relative to the mesa pattem, which overlaps the convex comer, and introduced a perfect convex comer from top to bottom.

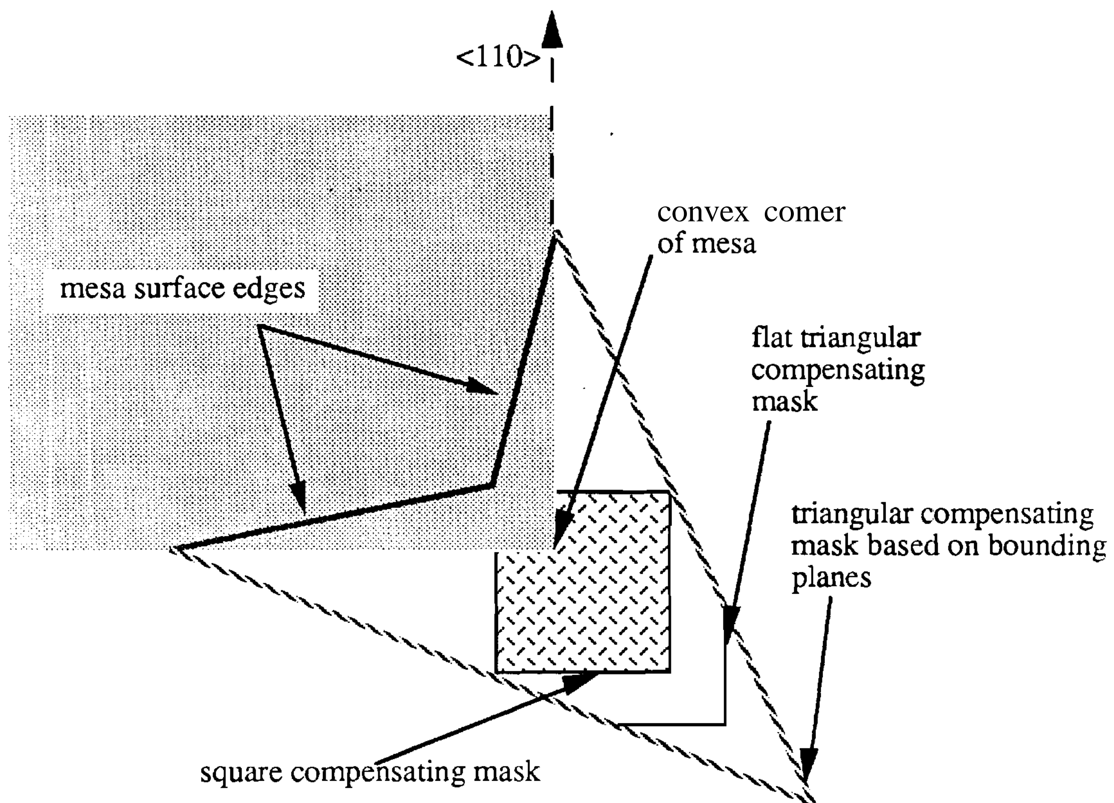


Figure 4.9. Different compensation designs based on bounded, fastest etching planes.

A test pattern mask was designed, as illustrated in Fig. 4.10, in order to characterize the KOH etching behavior and to estimate the comer compensation mask. It was also designed such that it can somewhat simulate the structural design of the accelerometer. The mask covers two directions of alignment, <100> and <110> in order to check the KOH etching characteristics in two interesting directions simultaneously. The mask also includes both the concave and convex comers and hence a comparison can be made on those comers between the <100> and the <110> alignment. The inner boundary of the "C" shape models what may be an accelerometer mass with only one beam. The width of the shaded region, which is the open area for KOH etching, is chosen as 500µm that is approximately the actual accelerometer beam length. Therefore, the test pattern covers most aspects of interest so that a compensation pattern can be developed.

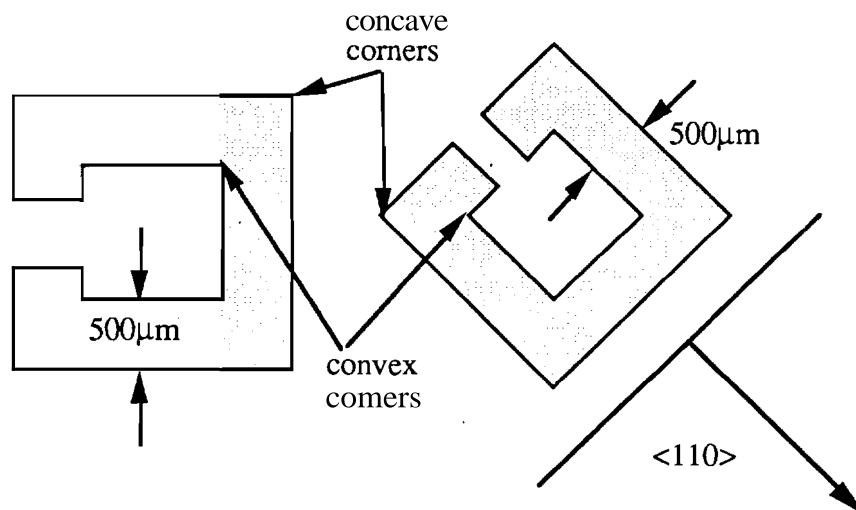


Figure 4.10. Test pattern (top view) for concave/convex anisotropic etching analysis, where the shaded region is unprotected and, therefore, etched.

To determine the dimensions of the corner compensation mask for the accelerometer, an experimental etch was performed using a KOH etchant whose contexts are 63.25w% DI water, 13.34w% n-propanol, and 23.41w% KOH. Tencor alpha-step profilometer was used to measure the vertically etched depth, and an SEM was used to measure the lateral etch. Also, some qualitative observations, such as surface morphology, were made by using the SEM. The comer compensation mask is used for the undercuts at the convex comers of a mesa aligned to the <110> direction. The comer compensation

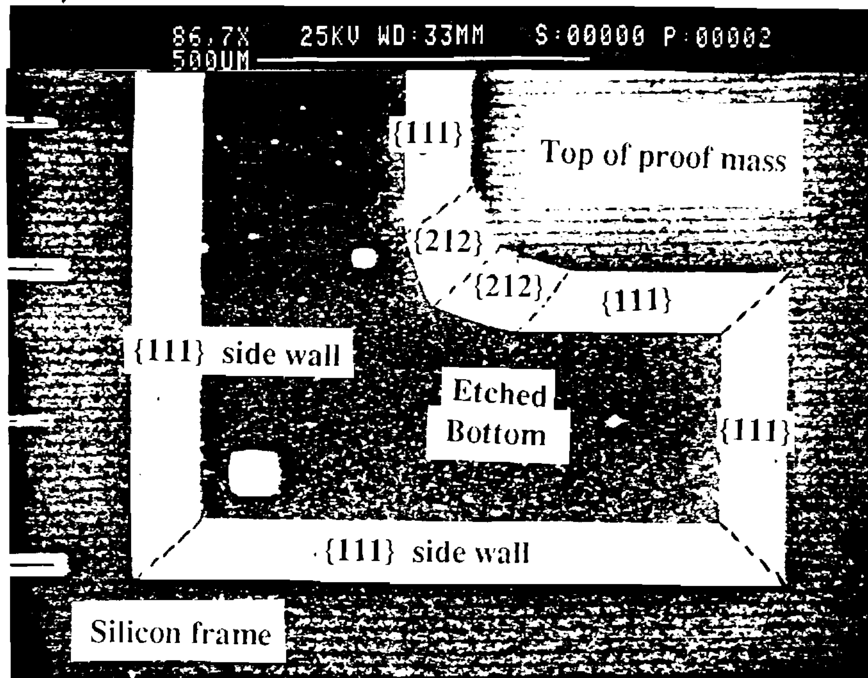
mask design is based on the techniques published by Puers and Sansen [17]. The design is calculated based on the desired final etched depth. Therefore, ratios should be used to describe the comer undercutting characteristics. Figure 4.11(a) is a SEM photograph illustrating the top view of the etched testing mask pattern whose edges are aligned along the <110> directions. First of all, the trace line of the fastest etching plane on (100) wafer must be identified experimentally and described the extent of corner undercutting by normalizing the etched distance of this trace line by the etched depth. Figure 4.11(b) is a schematic figure of the SEM photograph of Fig. 4.11(a) in order to identify the corner facets. The trace line of the fastest etching plane on (100) wafer can be determined by examining the angle made by the facet plane and the top (100) plane. The angle θ between two planes $[h_1k_1l_1]$ and $[h_2k_2l_2]$ can be obtained by

$$\theta = \cos^{-1} \frac{(h_1h_2 + k_1k_2 + l_1l_2)}{[(h_2^1 + k_2^1 + l_2^1)\,(h_2^2 + k_2^2 + l_2^2)]^{1/2}} \tag{4.20}$$

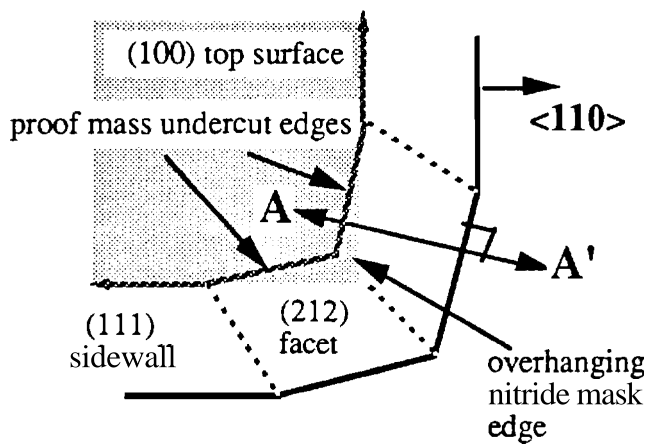
After 2 hours of KOH etching, the vertical etched depth was 127μm and the lateral etching was 105μm. Using the Eqn. (4.20), the angle between the comer facet and the top (100) plane became 50°. Since the corner facets suggested by several researchers are (211}, (331}, {221}, and {411}, the angle made between those planes and the: top (100) plane were examined and summarized in Table 4.4. From the table 4.4, the (221) plane made the almost identical result as the etching experiment and therefore the comer facet plane was determined as {221} plane. The direction of the intersecting line of the (221} plane and (100) plane is <210>.

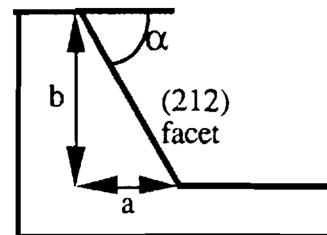
Table 4.4 The angle made by comer facets and (100) top plane.

	{211}	{221}	{331}	{411}
The angle made with (100) plane	35.26' or 65.9'	48.2" or 70.5"	46.5' or 76.7'	19.5" or 76.4"



(a)





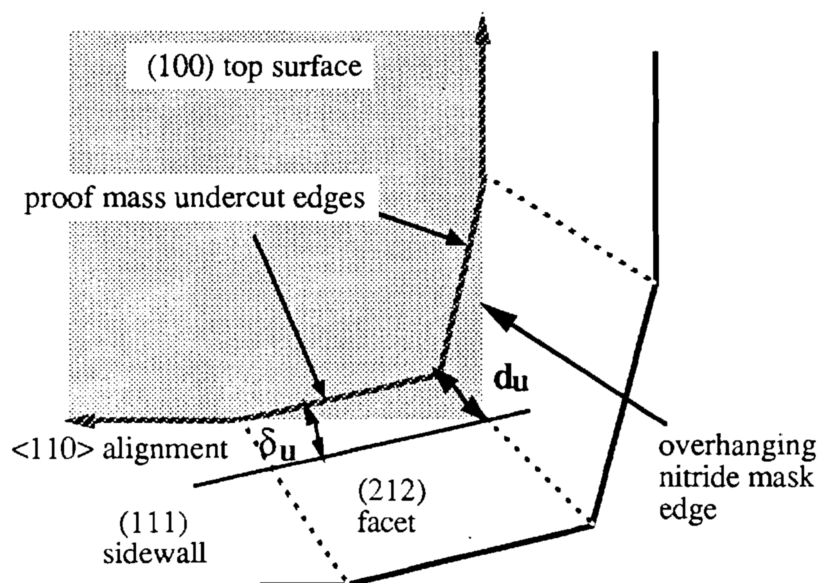
From the measurement,
a = 105 μm
b = 127 μm
a = $\tan^{-1}$(b/a) ≈ 50°

(b)

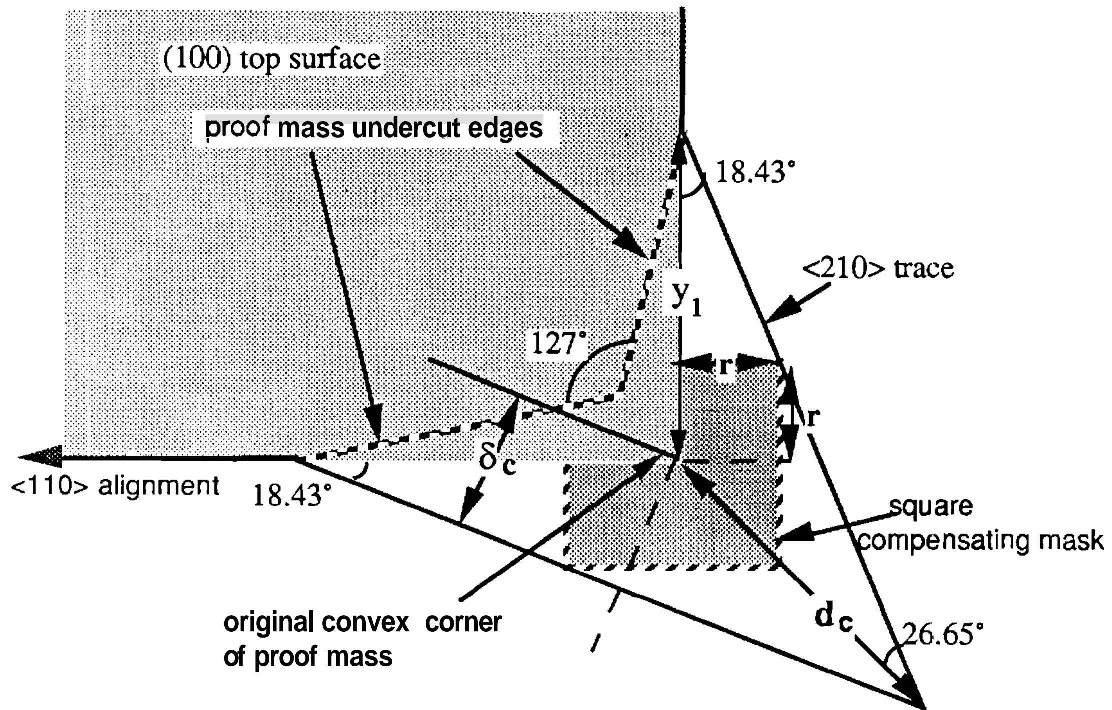
Figure 4.11. Top view of a convex comer etching result of the testing mask whose mesa edges are aligned along the <110> direction. (a) SEM photograph. (b) A schematic drawing of the SEM and cross section of the (212) side facet.

There are two parameters in Fig. 4.12 that are used for calculating the corner compensation pattern: d, and 6, The parameters d, and 6, are ratioed to the etched depth in the experimental etch, also called tip undercut and relative facet undercut, respectively. Relative facet undercut can be used to determine the dimension of the triangular corner compensation mask. Relative tip undercut will determine the diagonal.extension of the square compensation mask to the corner of the mesa. Then, by geornetry, the square dimension of the corner compensation is determined. One example of corner compensation mask and its geometry calculation is illustrated in Fig. 4.13. The corner compensation mask dimension can be obtained by using other geometrical parameters as discussed by J. Chang in her thesis [10].

The first comer compensation mask was large enough to protect the comer from the undercutting but it turned out to be larger than necessary as illustrated in Fig. 4.14. Even though the comers are bigger than the original convex corner, since the silicon diaphragm is exposed between the proof mass and the frame, the accelerometer still can function as designed. The variation of the mass will have some effect an the measured sensitivity and resonant frequency. In order to refine the corner compensation mask, a series of KOH experiments were performed and the improved comer compensation mask was obtained and its improved etching result is illustrated in Fig. 4.15.



4.12. Top view of a convex corner with parameters used to design corner compensation mask.



$$d_u = \frac{\sqrt{5}}{2}\,\delta_u$$

6, = 6,

$$d_c = \sqrt{5}\,\delta_c = 2\,d_u\ .$$

After 2-hours KOH etching: etched depth = d_e = 127μm

d, = 50μm, 6, = 45μm

Therefore, $d_c = \sqrt{5}\,\delta_u$ = 100.6μm

For 15 mil. (381μm) thick wafer etching:

(Assuming that all the etching is proportional to the vertical etching)

Required etched depth = 381μm = 3 x 127 μm

$$d_c = \frac{381\mu m}{127\mu m} \times 100.6\mu m = 300\mu m$$

$\delta_c = 135\mu m = y_1 \sin 18.43° \rightarrow y_1 = 427\mu m$

$x_1 = d_c \cos 26.65" = 300\ \mu m \cos 26.65" = 268\mu m$

For a square comer compensation with each edge length of' 2r,

$r = (y_1 - r)\tan 18.43° = (y_1 - r) \times 0.3332$

<u>r = 106.72μm</u>

Figure 4.13 Top view a square corner compensation mask using <210> traces and the calculation of the square compensation mask dimension.

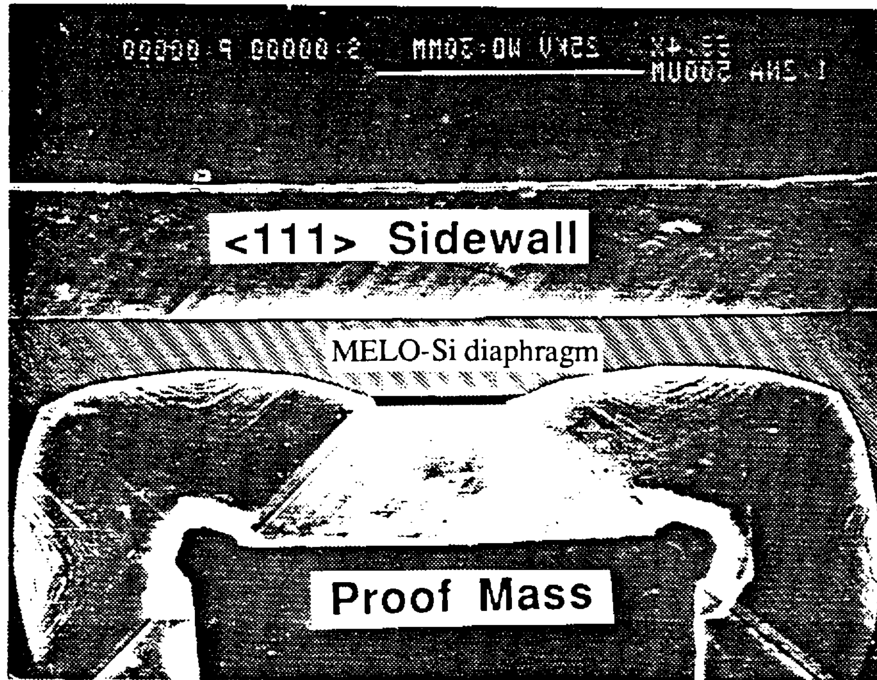


Figure 4.14 An SEM picture of the experimental result of the initial comer compensation comer mask after 6-hour KOH etching at 80±1°C.

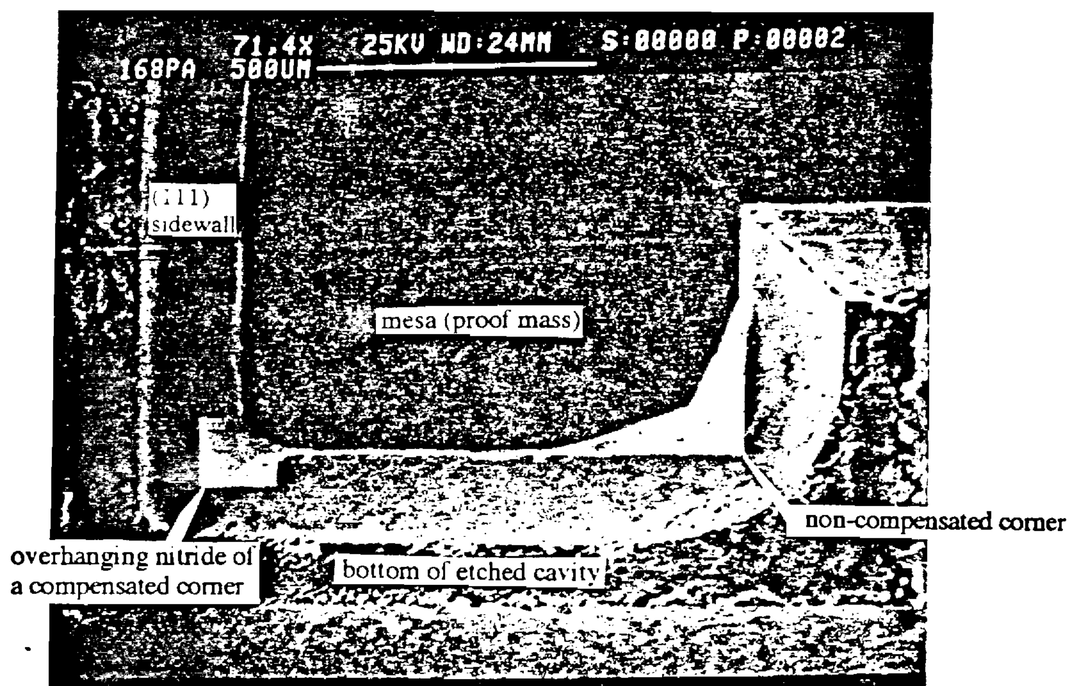


Figure 4.15 An SEM picture of the improved comer compensation mask after about 4 hours KOH etching at 80±1°C.

4.4.4 Metal Passivation in KOH Etch

After the circuit fabrication and metal pattern are completed the front circuit and metal pattern need to be protected during KOH etching. Front-side passivation of Al-Si, during 6-hour long back-side KOH etch, turned out to be one of the critical steps in fabricating MELO accelerometer successfully unless metal deposition and patterning can be performed after KOH etching. The strength and durability of the passivating layer depend on the metal deposition, metal pattern, surface cleaning, passivating material and its thickness, etching solution, and the etching temperature. A series of experiments were performed in order to improve the metal (Al-Si) passivation and the etching results are described in this section.

4.4.4.1 Al-Si Lift-off vs. Wet Etch

It has been known that the metal lift-off procedure can cause sharp spikes at the metal edges when the lithography is not done. carefully. Nevertheless, Al-Si lift-off procedure is often preferred in device fabrication over wet etching for metal pattern definition because of its simplicity and fine geometry capability. In addition, Al-Si passivation is usually not required for device fabrication unless the device faces a harsh environment. The electrical devices on a wafer or a die can be tested on a probe station regardless of the possible existence of the spikes at the Al-Si line edges. Therefore, the importance of avoiding the spikes at the Al-Si edges and difficulties of Al-Si metal passivation were not realized until a complete accelerometer was fabricated.

Metal lift-off is normally performed by soaking the metal deposited wafer in acetone until the underlying photoresist gets dissolved and the top unwanted metal is lifted off leaving a metal pattern. In order to speed up the process, the wafer is sometimes placed in the ultrasonic cleaner (USC). This USC treatment turned out to make the spikes even worse because it breaks the Al-Si edges more abruptly than that of simple acetone soaking. The USC process also can produce small particulate of the lifted Al-Si and these particulate can cause micrometer range bumps by sticking on the patterned Al-Si surface as shown in a SEM photograph (Figure 4.16). Figure 4.17(a) illustrates the Al-Si metal surface roughness at the edge as well as on the metal layer caused by lift-off process even after plasma nitride/oxide deposition. The measurement was performed by Tencor Alpha-step surface profilometer after Al-Si sputter deposition at 8 mTorr (with the starting base pressure of 3 x 10^{-7} Torr) on the patterned photoresist, lift-off, and plasma oxide/nitride deposition. Unfortunately, these spikes caused by the Al-Si lift-off process continue to

maintain their sharpness even after a thick passivation layer deposition. Figure 4.17(b) illustrates a 1μm high spike on the Al-Si metal layer after passivation layer deposition. The height could be as high as few micrometers

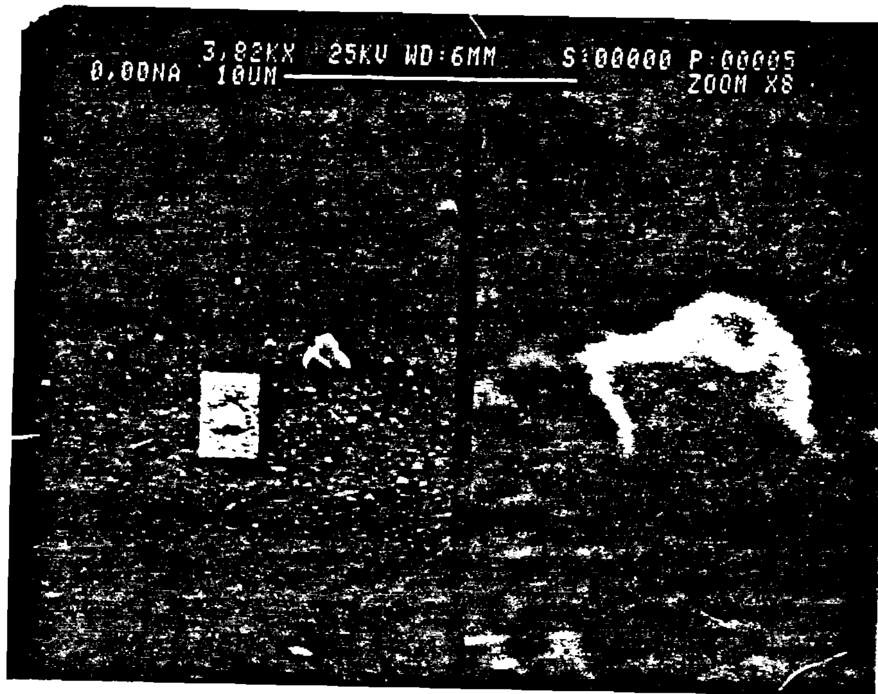
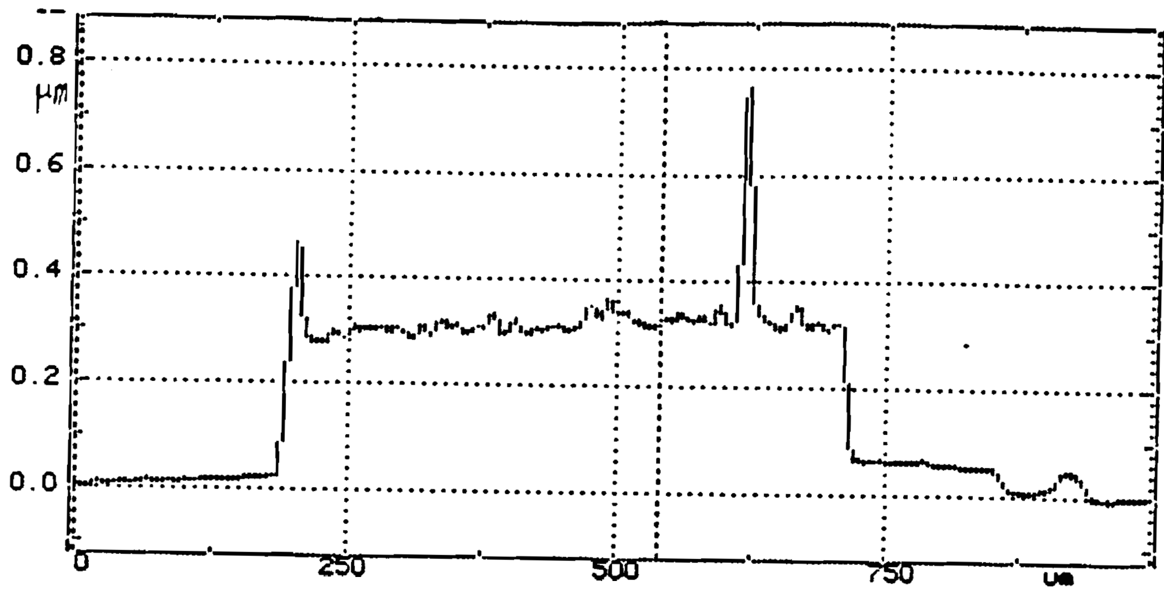
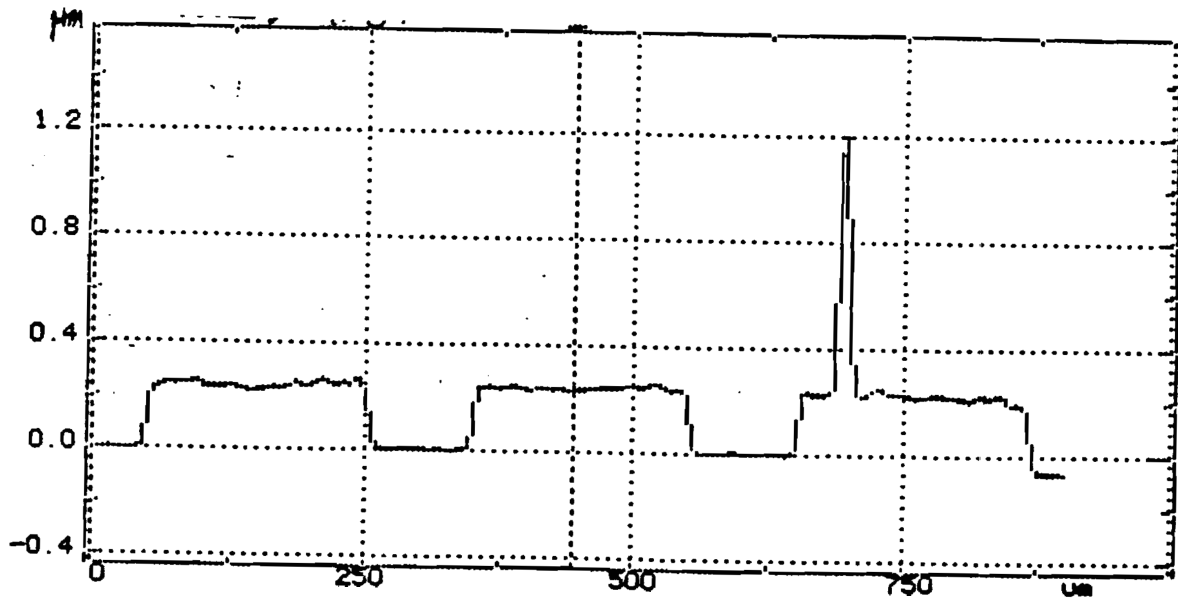


Figure 4.16 A SEM photograph of Al-Si particulate sitting on the metal layer after lift-off.

Even when the spikes are covered by the passivation layer, they are not covered conformally and a pin hole or break-through can occur from the side of the spikes faster than on the passivated surface. In this case, during KOH etch, the weaker passivation layer is damaged by the KOH etch solution and Al-Si becomes exposed. Once the Al-Si is exposed to KOH etch solution through the damaged passivation layer, Al-Si is then etched rather fast by the KOH etchant. Figure 4.18 illustrates couple of examples of the etched Al-Si metal pattern by KOH etch solution after deposition of plasma oxide and nimde as passivation layers. Therefore, Al-Si wet etching was employed instead of lift-off.

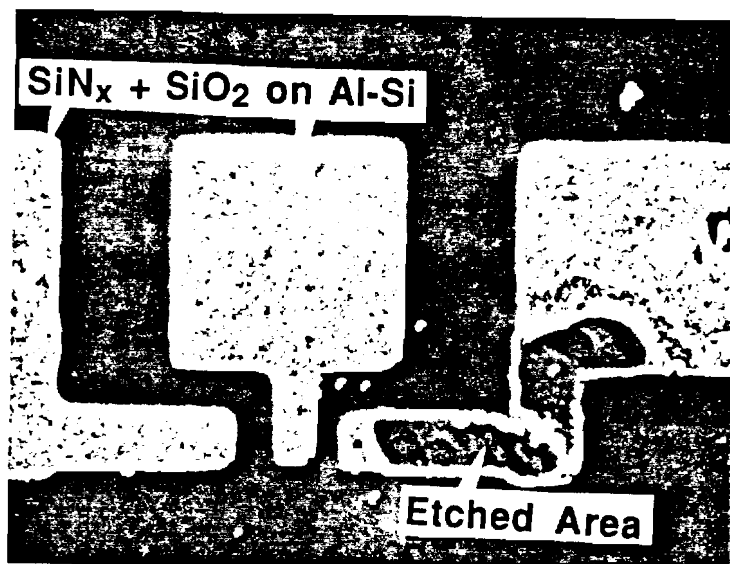


(a)

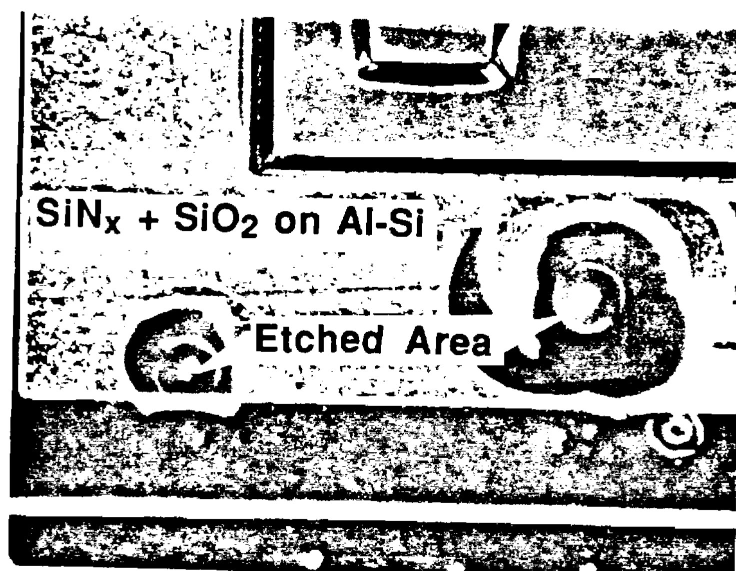


(b)

Figure 4.17 **Al-Si Metal spikes caused by a lift-off process. After Al-Si sputter deposition at 3 x 10^{-7} Torr, lift-off, plasma oxide deposition, and plasma nimde deposition. (a) spikes on the metal layer as well as at the edge.** (b) 1 μm size spike.



(a)



(b)

Figure 4.18 Example of the etched Al-Si metal layer by 15 min KOH etch after passivation. (a) etch starting from a comer. (b) etch starting from an metal edge as well as from the top.

4.4.4.2 Chamber Base Pressure Before Al-Si Deposition

The original quality of the sputter deposited Al-Si is important as it is related to the degradation of the passivation layer. Previously Al-Si was deposited by sputtering the Al-Si source target at 8 mTorr with a base pressure of $3x10^{-7}$ Torr and the deposited Al-Si was good enough for electrical testing of the devices. Argon gas was used for making a plasma. However, Al-Si deposited at the above condition resulted in a rough surface and later caused a degradation of the passivation layer. Whereas sputtering of the Al-Si layer at lower base pressures (< $2x10^{-7}$ Torr) yielded a better, very smooth and shinny surface which made the subsequent passivation layer hold much longer during KOH etch using the same passivation layers. Therefore, the Al-Si deposition base pressure was set as low as possible and a pressure near $2x10^{-7}$ Torr was. usually obtained. Table 4.3 shows an improvement in yielding good accelerometer dies with a lower base pressure of the Al-Si deposition chamber.

As illustrated in Table 4.3, the lower base pressure in the Al-Si deposition chamber improved the accelerometer fabrication yield considerably. Even though the number (from $3x10^{-7}$ Torr to $2x10^{-7}$ Torr) doesn't seem to indicate a big difference in the pressure, the lowering of the base pressure takes 8 to 10 hours of extra pumping time. This longer pumping would remove the water and oxygen contents from the sputtering chamber and the quality of the deposited Al-Si metal might have improved with this lower base pressure due to lower oxygen and water contents. Degradation of the Al-Si layer deposited at near $3x10^{-7}$ Torr became obvious after the Al-Si annealing at 400°C which is a moderately high temperature process. In fact, this annealing process have participated in making the Al-Si metal surface rough and resulting in a degradation of the passivation layer during KOH etch. However, a very recent surface measurement of the Al-Si layer deposited at $2.2x10^{-7}$ Torr followed by annealing at 400°C for 20 min. revealed that the surface does not become very rough after the annealing step. Therefore, the original Al-Si layer quality from the deposition seems to affect the,surface roughness more than the following annealing step.

4.4.4.3 Al-Si + Chrome Double Metal Layer

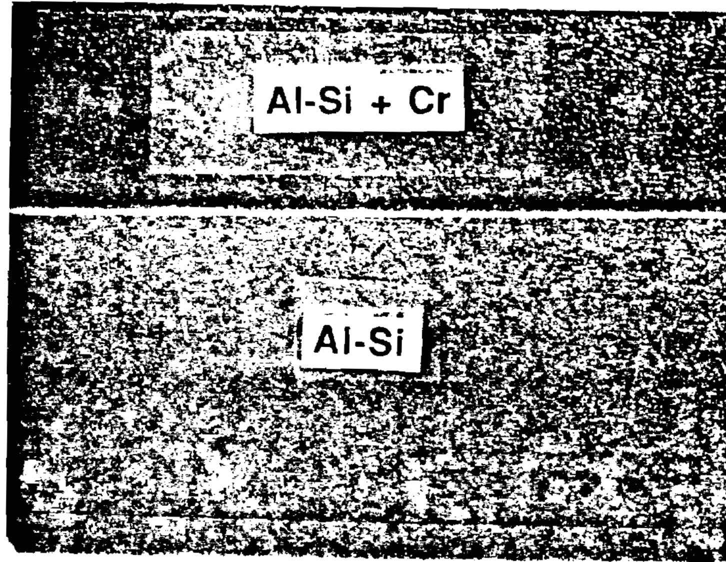
Al-Si deposited with the base pressure of $3x10^{-7}$ Torr, which was the typical base pressure, seemed very difficult to passivate with plasma oxide or nimde in the early stages. Chrome(Cr) was employed to examine if the passivation could be improved since Cr has been known to have a smoother surface than AI-Si. The different smoothness between Al-Si layer and Al-Si+Cr layer is shown in Figure 4.19. Particularly, after plasma oxide

deposition the Al-Si surface clearly became rougher than the Chrome surface deposited over the Al-Si layer as shown in Figure 4.19(b). Since Cr has a smoother surface, it was protected better with the same passivation layer than Al-Si in a KOH etch solution. However, Al-Si was not replaced by Cr because of the following reasons. First, Cr is known to make a poor ohmic contact with the silicon substrate and hence only used as a gate metal for MOSFET devices instead of contact metal. Secondly, Cr is known to have a higher resistance than Al-Si with a metal path, which is the case with MELO accelerometer layout. At last, it was difficult to bond Al wire on the Cr bonding pads. Therefore, Cr was chosen as a metal layer but as a protection layer on Al-Si during the KOH etching.

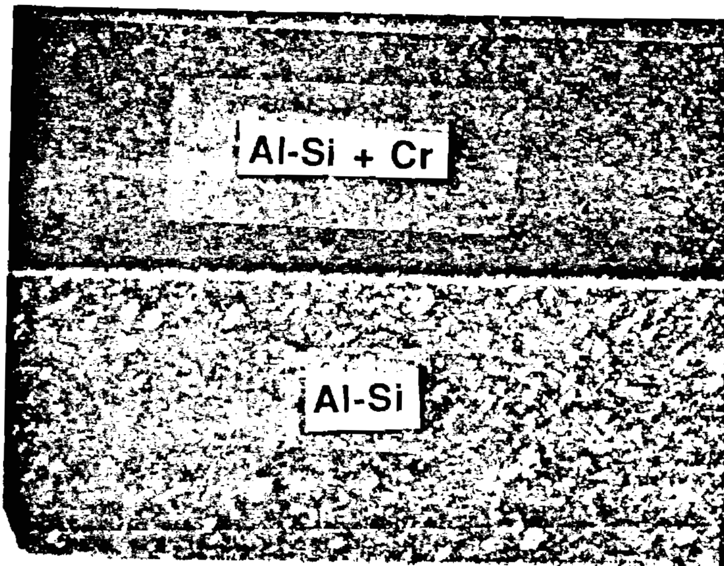
Next, Cr was employed for covering the Al-Si pattern. Al-Si and Cr were deposited consecutively and patterned with a negative photoresist for a wet etch process. Then Cr and Al-Si were etched in that order for patterning, resulting in the structure shown in Figure 4.20(a). Cr on the Al-Si layer can be easily removed by a wet Cr etch without damaging the underneath Al-Si layer after the KOH back etch is finished. However, Cr deposited on the Al-Si and patterned using the same mask did not have perfect coverage and any exposed Al-Si, particularly at edges, was attacked by KOH etch. Figure 4.20(b) is a picture the Al-Si layer covered by the identically patterned Cr layer with the plasma nitride passivation layer on it. Figure 4.20(c) shows the Al-Si layer being etched by KOH etchant starting from the edge.

A slight modification in the mask, by making the Cr patter slightly larger than Al-Si pattern, will resolve the exposed Al-Si edge by covering the Al-Si edges; better. With the identical mask, Al-Si edge coverage was tried by patterning Al-Si and overetching Al-Si to make it narrower followed by depositing and patterning Cr. Figure 4.21 (a) depicts the cross section diagram of the resulting structure. This method somewhat improved the Al-Si coverage but it was difficult to cover all the Al-Si edges without losing the original Al-Si dimension considerably. Figure 4.21 (b) and (c) show the top view of this structure where most of Al-Si was covered by Cr except one edge. After a long KOH back etch, some of the uncovered Al-Si edges were etched and it depends on the alignment error.

From the above results, it became evident that a Cr protecting layer over Al-Si pattern can enhance the passivation during KOH etching. Therefore Cr deposition step was added in the process. In this case, Cr can be deposited over the patterned Al-Si on the whole front side of a wafer, without being patterned, and passivation layer can then be deposited. This will not only protect the surface better but also provides more mechanical strength after the KOH back-etch is completed.



(a)



(b)

Figure 4.19 **Comparison of Al-Si and Al-Si + Cr metal layer. (a) Before plasma oxide deposition. (b) After plasma oxide deposition.**

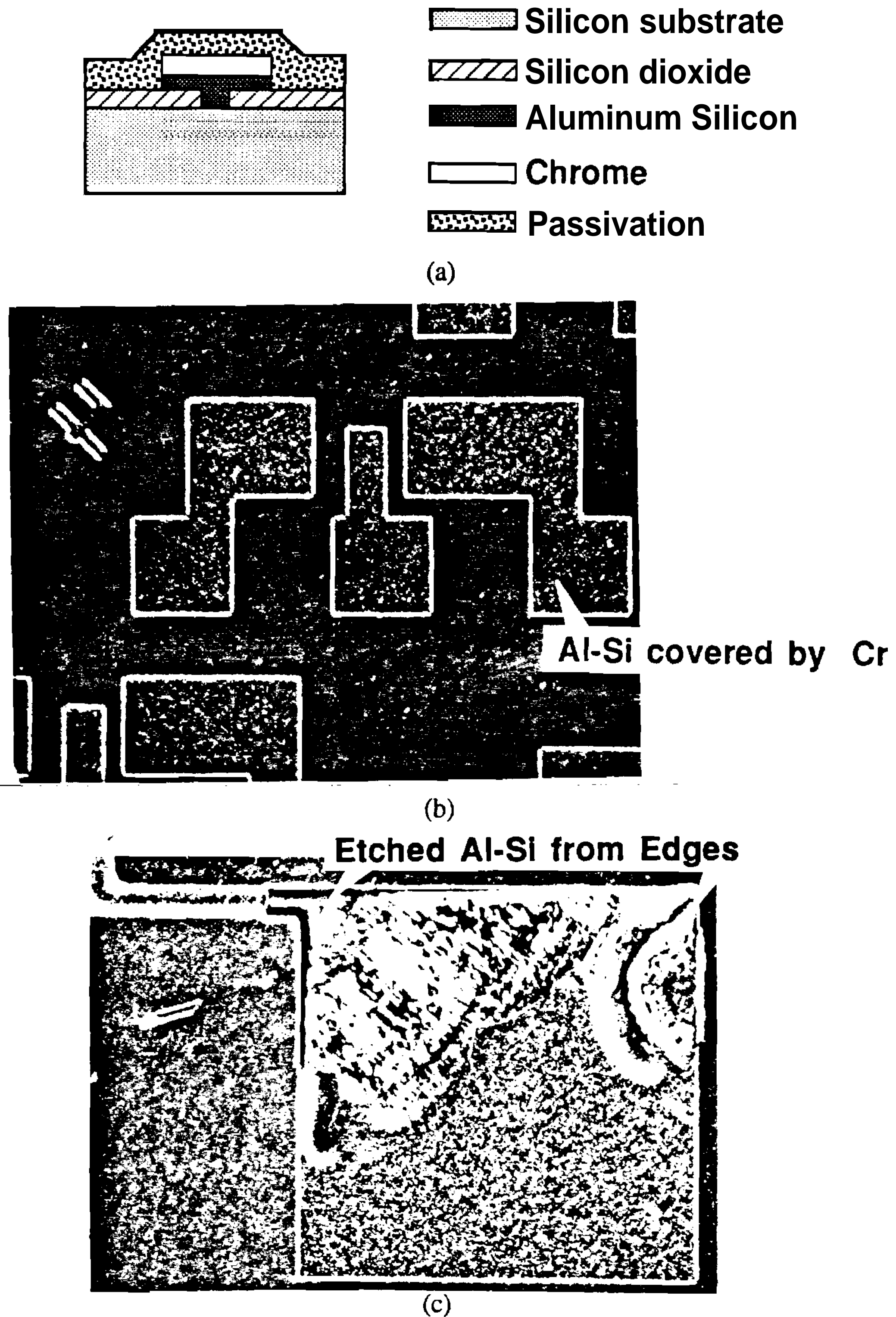
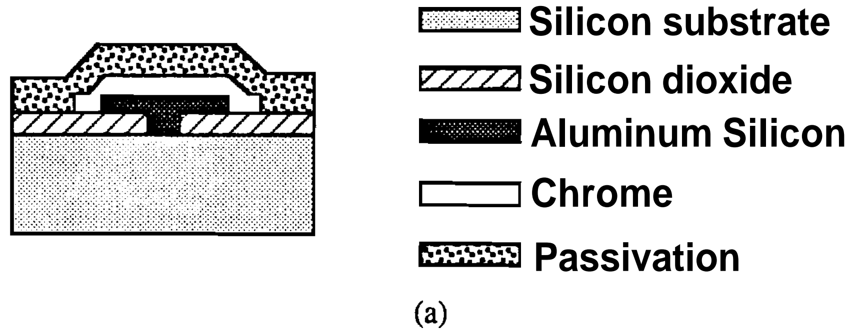
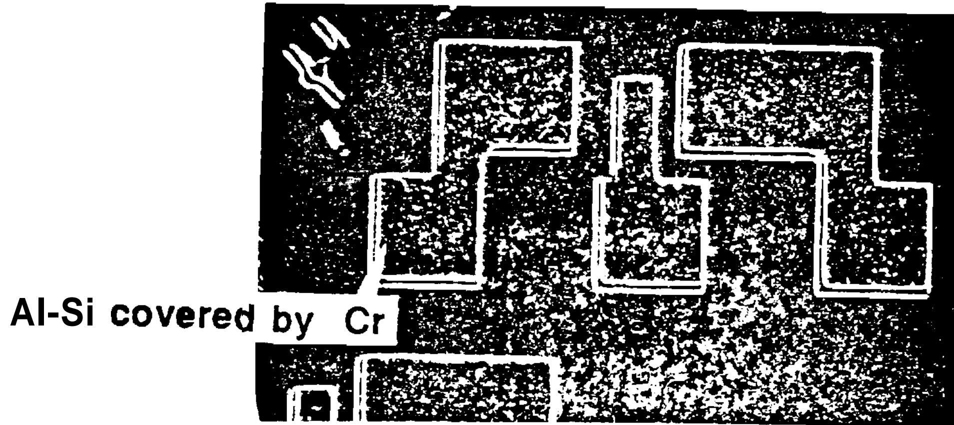


Figure 4.20 Al-Si plus Cr double metal layer with identical dimension. (a) A cross section diagram. (b) Al-Si and Cr are deposited and patterned together. (c) Al-Si exposed at the edge gets etched by KOH etch.



(a)



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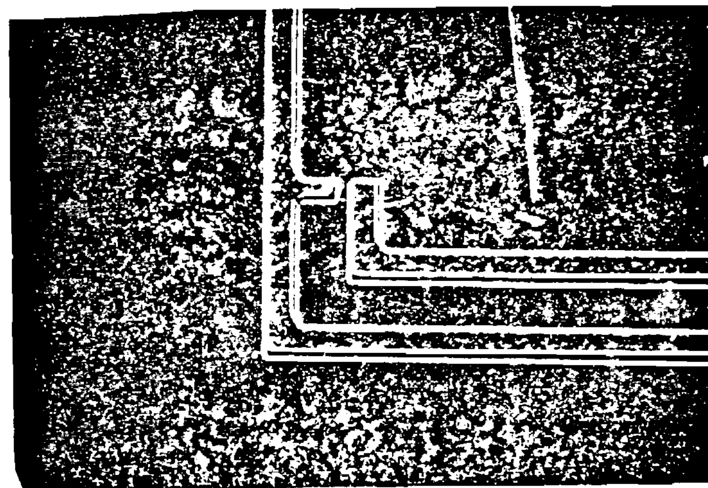


(c)

Figure 4.21 Al-Si plus Chrome double metal layer in which Al-Si is deposited and patterned by overetching first then Chrome is deposited and patterned. (a) A cross section diagram. (b),(c) A top view showing that most edges were covered by Cr layer except one direction.

4.4.4.4 Wafer Surface Roughness

The wafer surface morphology is another important aspect that needs to be considered because the surface roughness can bring a catastrophic result by degrading the passivation layer during KOH etching. The surface roughness can be caused anytime through the fabrication process, between the initial cleaning and the passivation deposition, and once the surface becomes rough it will likely stay rough. Cleaning the wafer is very important throughout the whole fabrication process because surface uncleanness will cause an unexpected roughness. Cleaning is very important particularly for the following steps: before oxidation, before and after photolithography, before silicon epitaxy, before Al-Si deposition, after Al-Si pattern, before PECVD nitride deposition, and after nitride pattern. Handling wafer with a dirty tweezers can also make the wafer dirty and rough.

In general, Piranha (1 H_2SO_4 + 1 H_2O_2) cleaning is one of the best methods for cleaning the wafer during the device fabrication. Therefore, right before high temperature process such as thermal oxidation, chemical vapor deposition, silicon selective epitaxy, and after photolithography. It is very difficult to remove the defects and roughness generated in a high temperature process. Therefore, it is required to clean not only the wafers but also the tweezers and glassware carefully. Photolithography is another major source of the surface roughness because the unwanted photoresist may stay on the wafer after the lithography. The surface roughness is more often caused indirectly by mask uncleanness, imperfectly defined and patterned photoresist, and badly defined lithography. These bad lithography will induce the surface roughness during the next step, such as oxide or nitride etching, metal deposition, and silicon epitaxy. In short, it is desirable to maintain the wafer surface smoothness like the starting wafer until the KOH etching.

Recently, the wafer surface roughness, which appeared after the MELO process, was reduced by chemical mechanical polishing (CMP) and it improved the KOH etching characteristics considerably. Figure 4.22(a) illustrate the step reduction on the front surface and (b) illustrates the improvement of the back surface morphology, afier CMP process. Both the front and back polishing was done at 25 lbs and 150 rpm. The front surface MELO step reduced from 1μm to less than 0.2μm after 3 min CMP and helped the AL-Si step coverage. The original one side polished wafer showed ±1μm roughness but this back side also became mirror-like smooth with about ±200Å roughness after 12 min CMP. The smooth back surface also improved the KOH etch characteristics by generating less number of black pyramids, etching uniformity, and enhanced accelerometer yield from each wafer.

The photolithography process was difficult because of the back surface roughness of the original wafer. Therefore, the back surface roughness caused a non-uniform etching and generated black pyramids during the KOH etching.

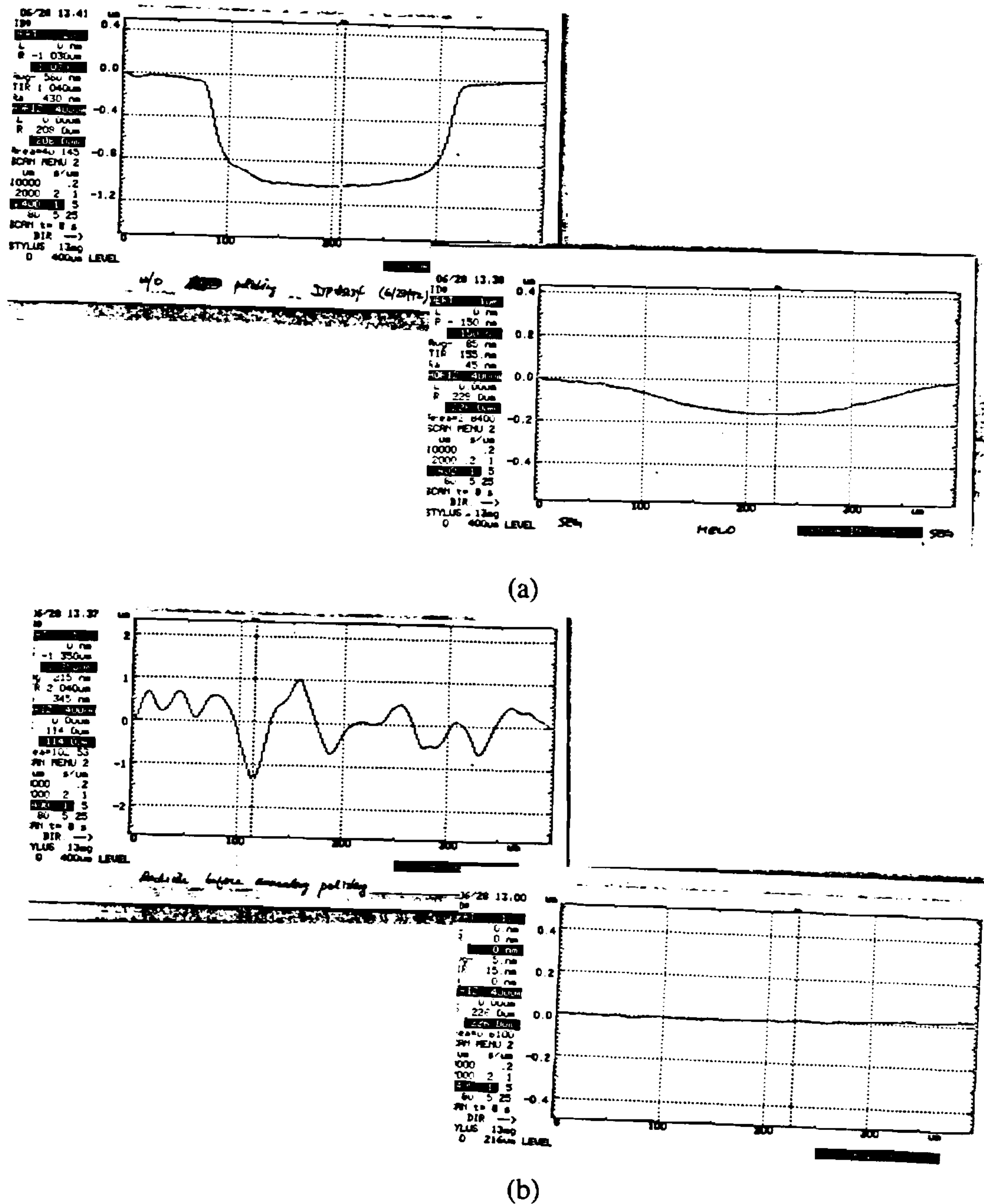


Figure 4.22 Surface profile of (a) the step reduction on the front of the wafer, (b) the improvement of the back surface morphology after chemical mechanical polishing at 25 lbs, 150 rpm with Nalco 2350 + DI water (1:15)

Even though the piranha solution is one of the best cleaning solution, it can not be used after Al-Si deposition because it attacks the Al-Si layer. After the metal layer is patterned by negative photoresist and wet etched, the negative photoresist can not be removed by acetone (ACE) rinse. It can be removed by warm Nophenol followed by rinsing in tetrachloroethane (TCA), ACE, methanol (METH). During this rinse, Nophenol needs to be cleaned thoroughly from the wafer front to achieve a clean surface before depositing a passivation layer. When Nophenol is exposed to water, it will make foam and may leave some residue even after a long rinsing with deionized (DI) water. Any residue before depositing a passivation layer can cause a degradation of the passivation layer. Cleaning the wafer and apparatus is also important because KOH etch is sensitive to the cleanness of them. After depositing PECVD nitride and patterning back etch window, cleaning with piranha was avoided in order to minimize any possible damage to the surface of the passivation layer. The wafer was cleaned only by soaking and rinsing with a mild agitation in solvents. This cleaning with only solvents may contribute to generating pyramids on the back of the etched diaphragm after the KOH etch since KOH etch is quite sensitive to the cleanness.

PECVD chamber must also be cleaned very well in order to obtain a stoichiometric plasma nitride passivation layer without many defects. Typically, PECVD deposition chamber is cleaned by $CF_4 + O_2$ plasma etch after each deposition run. However, $CF_4 + O_2$ plasma etch is not enough to remove the residue from the electrodes and scrubbing the electrodes is often necessary particularly to remove the carbon deposited during $CF_4 + O_2$ plasma etch. Scrubbing the electrodes and wiping the electrodes with solvents improved the PECVD nitride quality as a passivation layer.

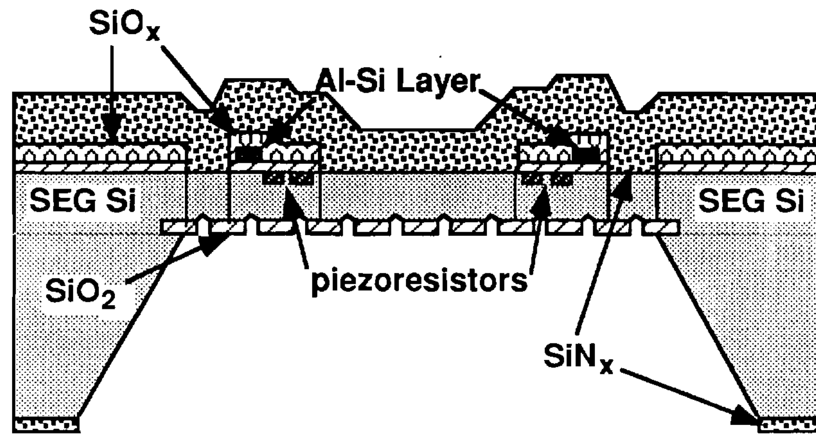
4.4.5 Front Delineation and Final Assembly

Two different methods were considered and tried for the passivation and the front delineation. The first design was made such that all lithography steps would be completed before KOH back-side etching. Figure 4.23(a) illustrates the cross section diagram of the structure just before the front delineation is performed. In this first design, a PECVD oxide layer was deposited on the front side and patterned using the front delineation mask (mask #8) after Al-Si metal patterning. Then a PECVD nitride layer was deposited on both sides of the wafer. While protecting the front nitride with a photoresist, the back etch pattern was defined. When the back-etch was completed using KOH, the wafer was placed in the reactive ion etch (RIE) chamber for the front delineation.

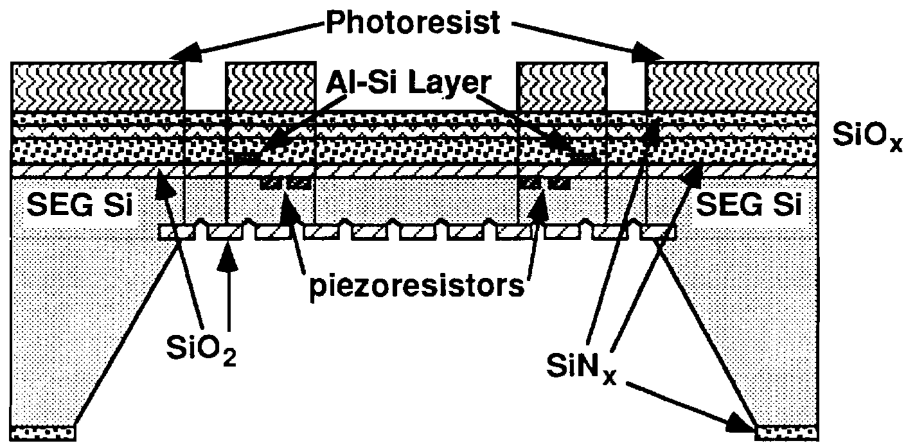
As the front PECVD nitride is etched away, the patterned PECVD oxide is exposed and used as a mask while etching silicon for front delineation. The etch rate of, PECVD oxide, PECVD nitride, and silicon with sulfur hexafluoride (SF_6) at 500watts was found to be 0.02µm/min, 0.1µm/min, and 1.0µm/min respectively. The PECVD oxide thickness can be optimized such that top Al-Si bonding pads will be exposed when the silicon etching is completed. If the PECVD oxide is thicker than desired and left after front delineation, then it can be etched with a BHF wet etch. This way, when the back-etch is done, the front delineation can be completed without any further lithography process. Therefore, no photolithography step would be necessary after the thin silicon diaphragm is fabricated since the thin diaphragm can be easily damaged. However, with this design some accelerometers were damaged during KOH etch because of the thick steps introduced by the patterned PECVD oxide and nitride passivation was not thick enough to protect sides of those steps. The PECVD nimde deposited after patterning the oxide became weak at those steps and was damaged during a long back-side KOH etch. This design would work better if the oxide step was reduced.

The second method is to perform the back-side KOH etch before the front delineation. Figure 4.23(b) shows the cross section diagram when the wafer is ready for the front delineation. In this approach, single thick layer of PECVD nitride was deposited on the front of the wafer after the metal was patterned. Without patterning the front layer, the back of the wafer was passivated and patterned for KOH etch. When the KOH etch was completed, the wafer was then attached to a back-plate wafer for an additional mechanical support as illustrated in Fig. 24. With the back plate wafer attached, the accelerometer wafer can proceed photolithography steps even though it still requires much care.

The PECVD nitride was then etched by RIE using SF_6 followed by Cr etching before the front delineation lithography. The front delineation was patterned with a thick (AZ4620) photoresist such that the photoresist can be used as a mask during front delineation by RIE using SF_6. After the front delineation is completed, the photoresist on the top can be removed by either ACE soak or a plasma ash without damaging the wafer. The front lithography worked quite well with the back plate wafer intact and the front delineation has been successful as long as the top photoresist stays intact during the front delineation by RIE. The front lithography can still be avoided if the PECVD oxide can be patterned after the first nitride deposition



(a)



(b)

Figure 4.23 Cross section diagram of two different approaches for the front delineation. (a) Front delineation is patterned on PECVD oxide before the KOH back etch. No lithography step is performed after the KOH etch. (b) KOH etch is performed followed by a front lithography step for the front delineation.

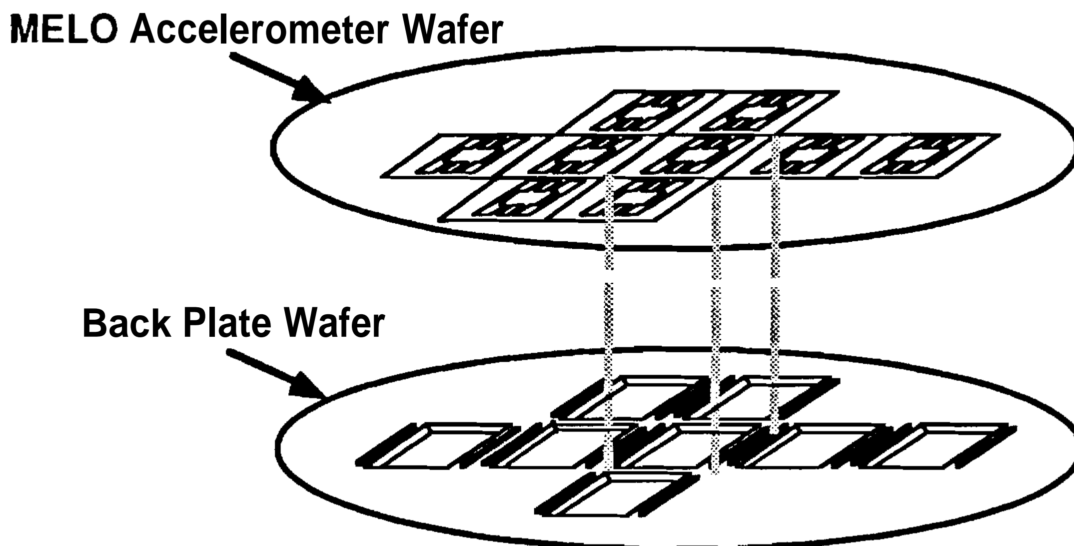


Figure 4.24 A schematic picture showing MELO accelerometer (AP-1) wafer is attached on the Delco Electronics ASD back-plate.

4.5. Final Process Flow and Results

The resulting final structure of MELO-Si accelerometer is shown in Fig. 4.25 and the one of the thin MELO silicon diaphragm beams and its close-up view are illustrated in Fig. 4.26. The final fabrication procedure is briefly described in Figure 4.27 and its across section diagrams are illustrated in Figure 4.28. A complete fabrication procedure is described in Appendix A.

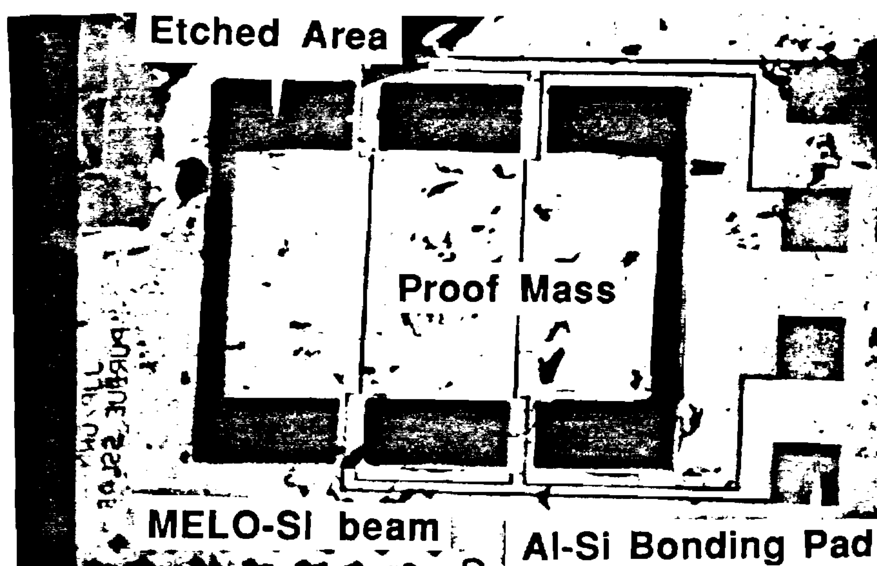
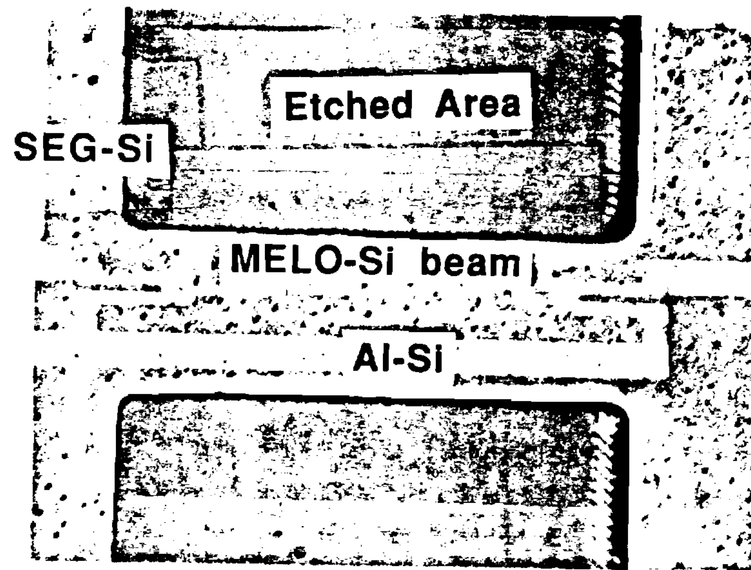
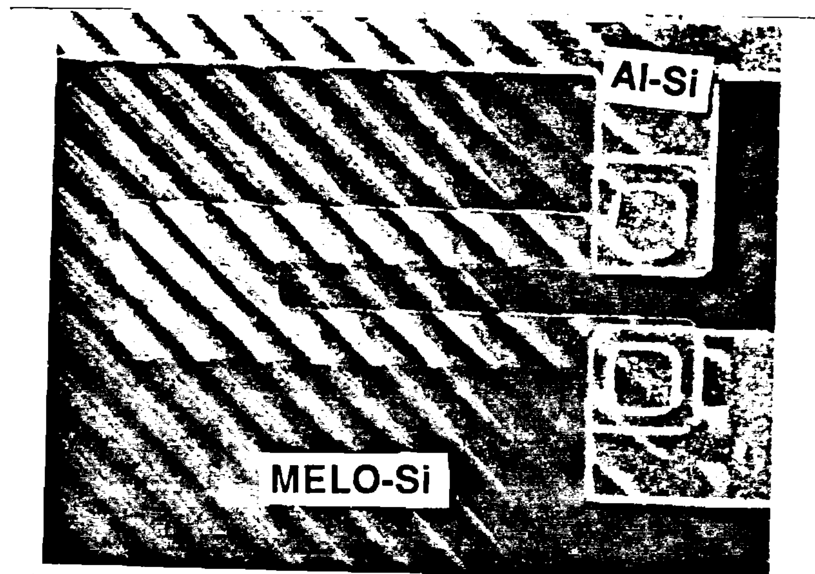


Figure 4.25 SEM photograph of top view of the resulting final structure.



(a)



(b)

Figure 4.26 The close-up view of the final thin MELO silicon diaphragm beam (a) One bridge with piezoresistor (b) an enlarged view of the piezoresistor by Nomarski microscope. The seed window lines are shown by shadow.

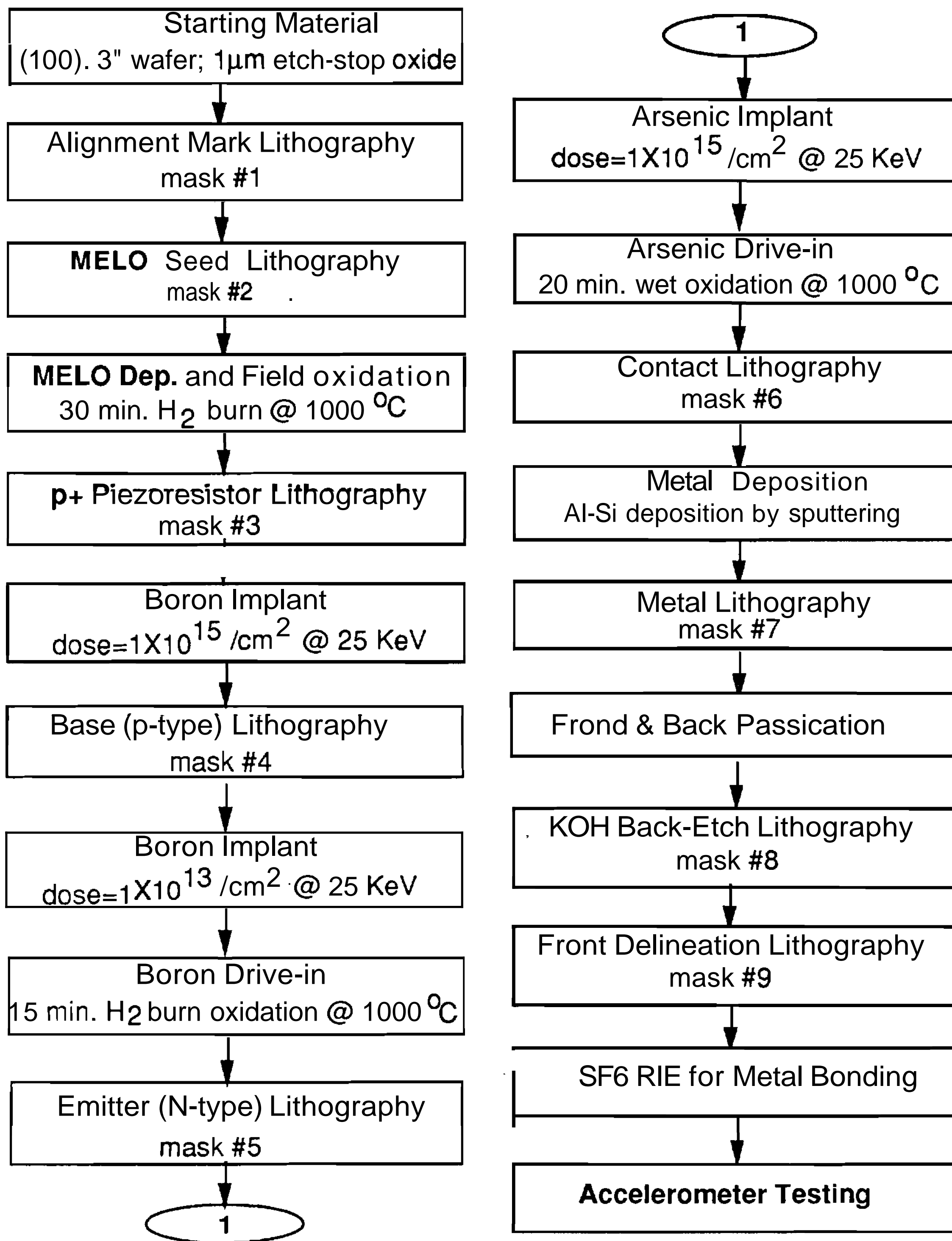
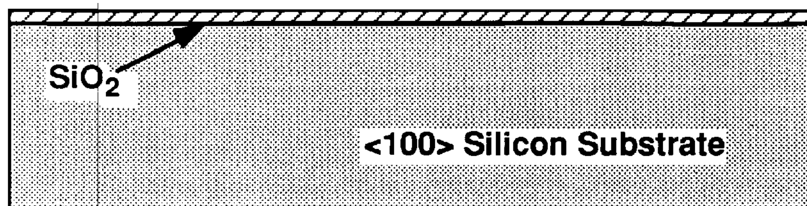
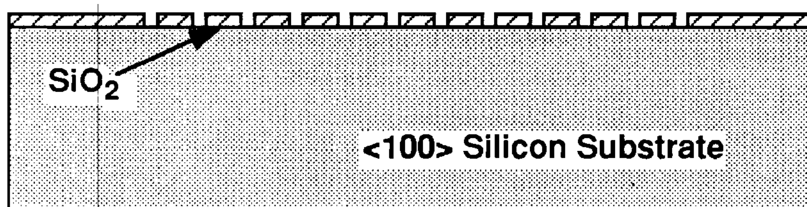


Figure 4.27 Final fabrication procedure of MELO-Si accelerometer including BJT device fabrication



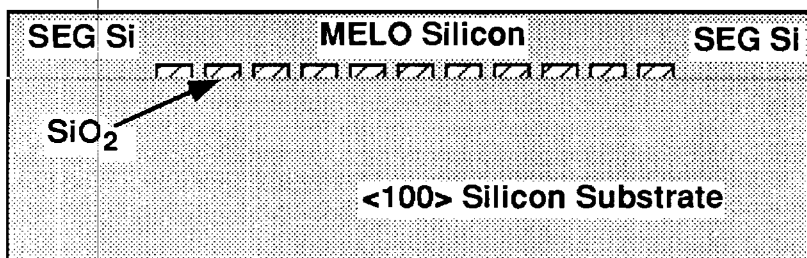
PECVD OxideDep.
Pattern Alignment Marks
- mask #1
Field Oxidation

(a)



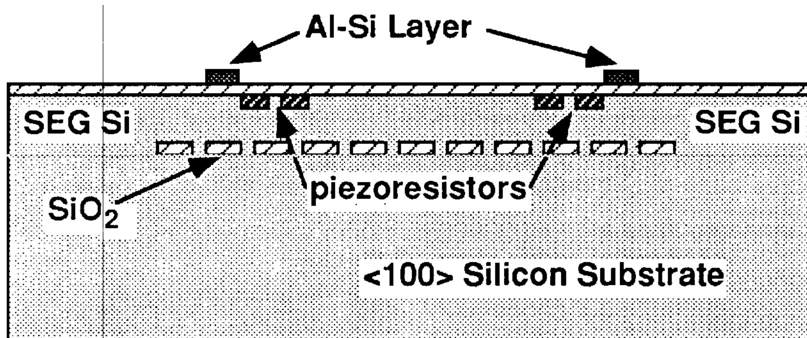
Pattern Seed Window
Along <100> Direction
for MELO silicon Process
- mask #2
2 μm seed width,
5 μm oxide width

(b)



Selective Silicon Epitaxy
for 10 μm MELO silicon
Growth Rate:
- 0.1 μm/min.

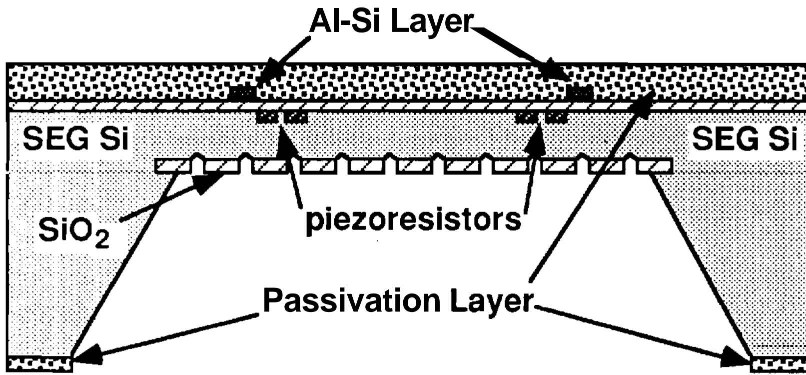
(c)



Piezoresistor fabrication
- mask #3
Base and Emitter Pattern
- mask#4 and 5
Contact Pattern - mask #6
Al-Si Metal Pattern
- mask #7

(d)

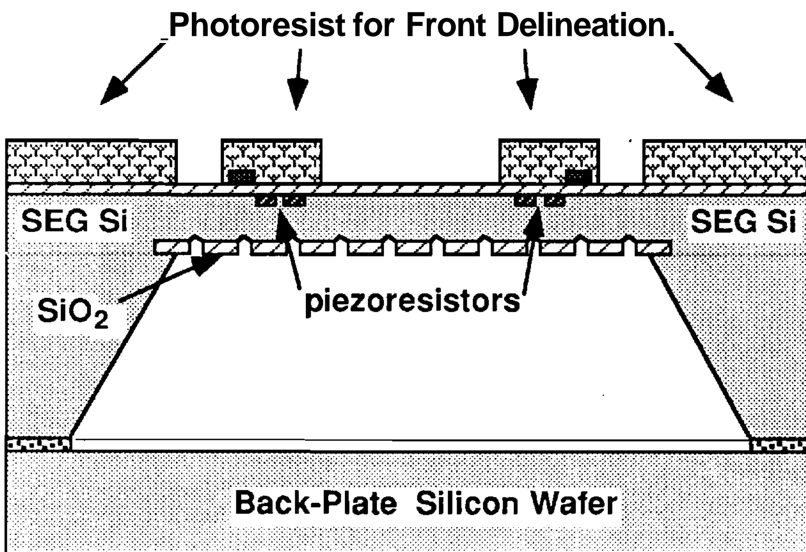
Figure 4.28, Continued



PECVD Nitride dep.
as a Passivation layer
on the frontand the back

Pattern Back for
KOH Back-Etch
- mask # 8

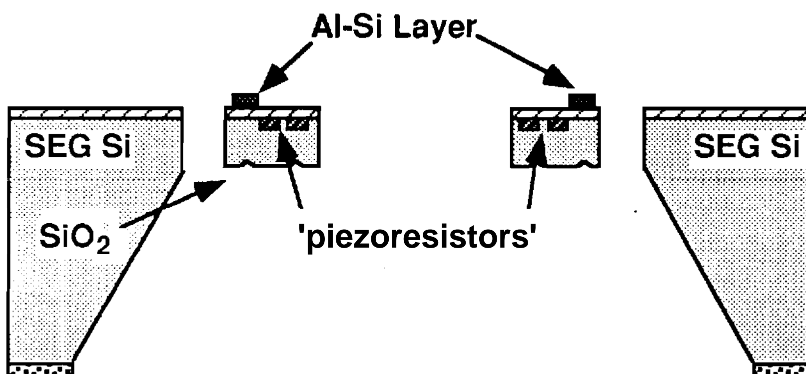
KOH Back-Etch
for MELO Silicon
Diaphragm Formation



Attach to the Back-Plate
for a Mechanical Support

Pattern Front Delineation
- mask #9

A24620 Thick (~6 μm)
Photoresist is
Uaed as a Front Mask



Fornt Delineation by
(RIE) with SF6

Photoresist Removal by
Plasma Ash

Removal of Seed Oxide

Attach to the Back-Plate
and Test Accelerometer

Figure 4.28 Cross sectional diagram of the MELO accelerometer fabrication procedure.

4.6 References

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CHAPTER 5
PERFORMANCE OF MELO-SI ACCELEROMETER

5.1 Introduction

The MELO-Si accelerometer performance is examined in detail in this chapter. The theoretical understanding, initially developed in chapter 4, of the static response to the applied stress will be extended. In addition, the theoretical analysis of the dynamic response will be presented. Their analytical results are compared with the simulation results, solved by finite element methods, for stress and strain along the beams. The testing results of the MELO-Si accelerometers are included and are compared with the theoretical analysis and the simulation results. Sensitivity, resonant frequency, and output linearity are three criteria that need to be considered for evaluating the performance of an accelerometer. Also, the effects of the processing tolerances on the performance of the MELO-Si bridge-type piezoresistive accelerometers, such as front-to-back misalignment, dimensional change due to overetching, etc. are discussed.

5.2 Static Response of the MELO-Si Piezoresistive Accelerometer

The static response of a bridge-type piezoresistive accelerometer was described in Chapter 4 using an ideal elastic beam with a boundary condition at one end being fixed and the other end being guided. A force was assumed to be concentrated at the end of the beam where the momentum was applied. A fabricated MELO-Si accelerometer, though, consists of four deflection beams with a stiff central section representing a seismic mass. To make the theoretical analysis closer to the real accelerometer, the two dimensional structure shown in Fig. 4.2(b) was employed. In this analysis, assuming symmetry in the z direction, the structure was simplified as two bridges with half of the original seismic mass. The forces acting on the bridges result from an acceleration of the distributed mass of seismic mass and the beams in the y direction, P_1 and P_2 as shown in Fig. 4.2(b).

From the elastic beam theory [1], assuming the deflection is very small, the differential equation for the deflection curve of a beam of Eqn.(4.1) is valid. By differentiating Eqn.(4.1) with respect to x and substituting the relationship between the load

P, the shear force Q_o, and the bending moment M ($P = -dQ_o/dx$ and $Q_o = dM/dx$), the following equations are obtained.

$$\frac{d^3y}{dx^3} = \frac{Q_o}{EI} \tag{5.1}$$

$$\frac{d^4y}{dx^4} = -\frac{P}{EI} \tag{5.2}$$

The deflection y(x) can be obtained by solving any one of Eqns.(4.1), (5.1), and (5.2), depending upon whether M, Q_o, or P is known and also depending upon mathematical convenience.

For the static analysis of the MELO-Si bridge-type accelerometer with four bridges, Eqn.(5.1) is the convenient one since the load Q_o can be directly obtained from the structure as

$$2Q_o = \frac{(m_1 + m_2)}{2} a_y \tag{5.3}$$

where a_y is the acceleration in the y direction, and m_1 and m_2 are the mass of the beam and the seismic mass respectively. If $m_2 >> m_1$, which is the case of the MELO-Si accelerometer, then $Q_o \approx m_2 a_y/4$ can be assumed. A general solution of Eqn.(5.1) can be written as

$$y(x) = a_0 + a_1 x + a_2 x^2 + a_3 x^3 \tag{5.4}$$

and the boundary conditions of this structure are

$$y(0) = 0,\ \left.\frac{dy}{dx}\right|_{x=0} = \left.\frac{dy}{dx}\right|_{x=l_1} = 0,\ EI \left.\frac{d^3y}{dx_3}\right|_{x=l_1} = \frac{m_2}{4} a_y = F_y \tag{5.5}$$

From these boundary conditions the coefficients of the general solution can be found as

$$a_0 = 0,\ a_1 = 0,\ a_2 = -\frac{F_y}{4EI} l_1,\ a_3 = \frac{F_y}{6EI} \tag{5.6}$$

Therefore, the equation for the deflection, after few calculations, becomes

$$y(x) = \frac{F_y l_1^3}{12EI}\left[2\left(\frac{x}{l_1}\right)^3 - 3\left(\frac{x}{l_1}\right)^2\right] \quad (5.7)$$

which agrees with **Eqn.(4.5)**. The force F_y in **Eqn.(5.5)** is from a quarter of the seismic mass because the seismic mass is supported by four beams. The expression of the strain along the x direction at $y=y_0$ is

$$\varepsilon(x) = y_0 \frac{d^2y}{dx_2} = y_0 \frac{F_y}{2EI}(2x-l_1) \quad (5.8)$$

and on the surface, $y = \frac{t}{2}$,

$$\varepsilon(x,y=\frac{t}{2}) = \frac{F_y t}{4EI}(2x-l_1) \quad (5.9)$$

It exhibits that the mechanical strain has a linear distribution along the length of a beam when the mass of the supporting beam is negligible. The stress distribution is obtained by multiplying Young's modulus to the strain as

$$\sigma(x,\frac{t}{2}) = \frac{F_y t}{4I}(2x-l_1) \quad (5.10)$$

which is identical to Eqn. (4.8). The sensitivity of an accelerometer is defined as the output voltage divided by the source voltage and applied acceleration. The sensitivity S of a bridge-type accelerometer, including the longitudinal piezoresistance coefficient π_l along the length of the resistors, can be represented using Eqn.(4.19) as

$$S = \frac{V_o}{V_{cc}}\frac{1}{a_y} = \alpha\frac{\pi_l l_1 m_2}{4nI} = \alpha\frac{3\pi_l l_1 m_2}{wnt^2} \quad (5.11)$$

where V_{cc} is the supply voltage for a full Wheatstone bridge circuit, n is the number of the supporting beams. The factor ***a*** ranges between zero and one depending on the location of the piezoresistors. A value of ***a=1*** indicates that the placement of the resistor is placed on one of the two maximum stress points, x=0 and $x=l_1$ from the analytical solution, and that the sensitivity becomes the maximum. When the piezoresistor is placed on a region where

no stress or a very small stress is generated, like on the frame, then a value α=O is used. The theoretical analysis of the static response is summarized in Table 5.1.

5.2.1 Static Response to the off-axis stress

The theoretical analysis of the previous section considered the accelerometer's response to accelerations only in the y direction. However, the device may face the accelerations in the x or/and z directions in real applications and the response to those accelerations needs to be examined for a full understanding of the device performance. Therefore, the sensitivity of the accelerometer response to the off-axis accelerations is evaluated. In addition, once these responses are known, the response to an arbitrary acceleration can be extracted from the principle of superposition provided that the response is linearly dependent to the applied acceleration.

Table 5.1 A summary of static response of a bridge type accelerometer.*

Beam Deflection Formula	$y(x) = y_o\left[3\left(\frac{x}{l_1}\right)^2 - 2\left(\frac{x}{l_1}\right)^3\right]$
Center Deflection	$y_o = \frac{l_1^3 F}{12EI}$
Stress at Surface	$\sigma(x) = \sigma_o\left[1 - 2\left(\frac{x}{l_1}\right)\right]$
Maximum Stress	$\sigma_o = \frac{F l_1 t}{4I}$
Maximum Sensitivity	$S_o = \pi_l\left[\frac{m_2(l_1-L_r)t}{4nI}\right] = 3\pi_l\left[\frac{m_2(l_1-L_r)}{wnt^2}\right]$
Moment of Inertia	$I = \frac{1}{12}wt^3$

*beam of a length l_1, L_r is the length of the piezoresistor that extended out on the bridge assuming that it starts from the frame edge, width w, thickness t, number of beams n, coordinate along beam axis x with origin at frame end, load distributed on the beam and mass P, seismic mass m_2, Young's modulus E, and acceleration a_y, and $F=m_2a_y/n$.

Again assuming that the forces act through the centroid of the beam cross section and that the center of mass exists on the xz plane, the response to an acceleration in the z direction can be determined by an analogous analysis as the previous one. By interchanging y and z in Eqn.(4.3), the stress along the x direction becomes

$$(x) = \frac{12F}{wt3}\left(\frac{l}{2} - x\right) z(x). \qquad (5.12)$$

The average stress $\overline{\sigma}_x$ in the resistor is zero if the resistor is placed symmetrically on the beam with respect to the center line in the x direction since the average value of z in the expression for the stress is zero for any value of x. It is due that half of each resistor is under expansion and the other half is under compression with the applied stress and they cancel the resistance change of each other. This holds for either a single resistor stripe or for a U-shaped resistor positioned anywhere along the beam in x. Once the resistors are placed off the centerline of the beam along the x-direction, the resistance change in each resistor is not canceled any more but is proportional to the applied stress. The ratio of percent resistance change per unit acceleration a, in the z direction to that in the y direction is

$$\frac{\left(\frac{\Delta R}{R}\right)_{a_z=a_u}}{\left(\frac{\Delta R}{R}\right)_{a_y=a_u}} = \frac{\frac{1}{2}\pi_{44}(\overline{\sigma}_x)_z}{\frac{1}{2}\pi_{44}(\overline{\sigma}_x)_z}$$

$$= \frac{2tz_r}{w^2} \qquad (5.13)$$

where z_r is the value of the offset. This quality is negligible for the very small value of z_r/w which can be obtained with proper process control and for $\frac{t}{w}$ <<1. For the MELO-Si accelerometer design, w = 0.017 cm, t = 0.001 cm, and a value for z_r of 0.0005 cm as a probable maximum misalignment error are the values that can be used and the value of Eqn (5.13), $2tz_r/w^2$, becomes less than 0.004 which is negligible.

For accelerations in the x direction the beam can be modeled as a long column with the load applied uniformly over the cross section of the beam. The stress distribution then becomes

$$\sigma(x) = \frac{F_x}{A} = \frac{F_x}{tw'} \tag{5.14}$$

The corresponding resistance change is then

$$\frac{\Delta R}{R} = \frac{\Pi_{44}F_x}{2tw} \tag{5.15}$$

giving a ratio of sensitivities of

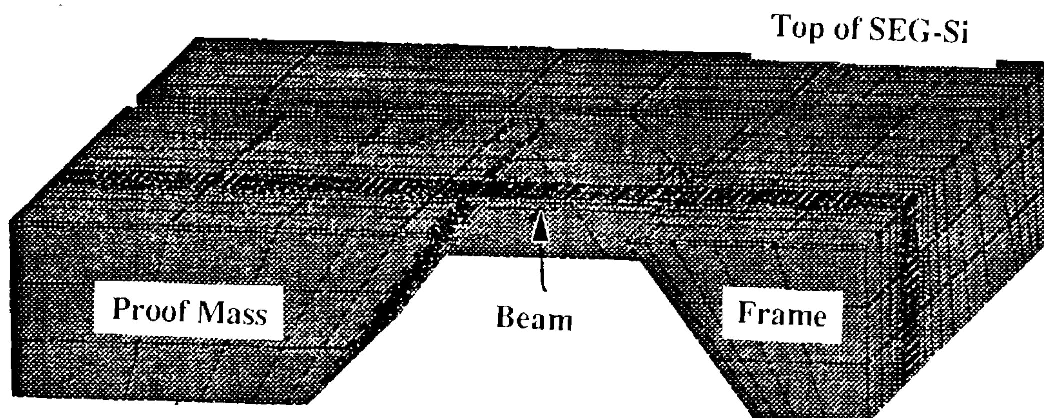
$$\frac{\left(\frac{\Delta R}{R}\right)_{a_x=a_u}}{\left(\frac{\Delta R}{R}\right)_{a_y=a_u}} = \frac{t}{3(l-L_r)} \tag{5.16}$$

The device will not be sensitive to accelerations in the x direction provided $t/(l-L_r) \ll 1$. This condition is easily met since $t/(l-L_r)$ is typically 0.03 which is the same with the MELO-Si accelerometer. Thus the device can be assumed to react in only in one direction, to a good approximation.

5.2.2 Static Response Simulation by ANSYS

The static response of the MELO-Si accelerometer was also analyzed by a commercially available 3-dimensional simulator called ANSYS. The ANSYS is a finite element analysis program used in a variety of fields including mechanical stress analysis [5]. For the finite element method, first the solid needs to be divided into several finite elements, then the variation of fields within each element is described by using interpolating polynomials. Finally, related physical rules and the boundary conditions are applied in order to get the solutions for each node, and the field between nodes is approximated by interpolation [2].

In the simulation of the MELO-Si accelerometer, only one quarter of the entire structure was modeled and its symmetry property was applied in both directions to simulate the entire structure, as shown in Fig. 5.1. The element type used for this solid modeling is stiff 45, 3-dimensional isoparametric solid in which each element is defined by eight points having three degrees of freedom at each node: translation in the nodal x, y, and z directions.



(a)

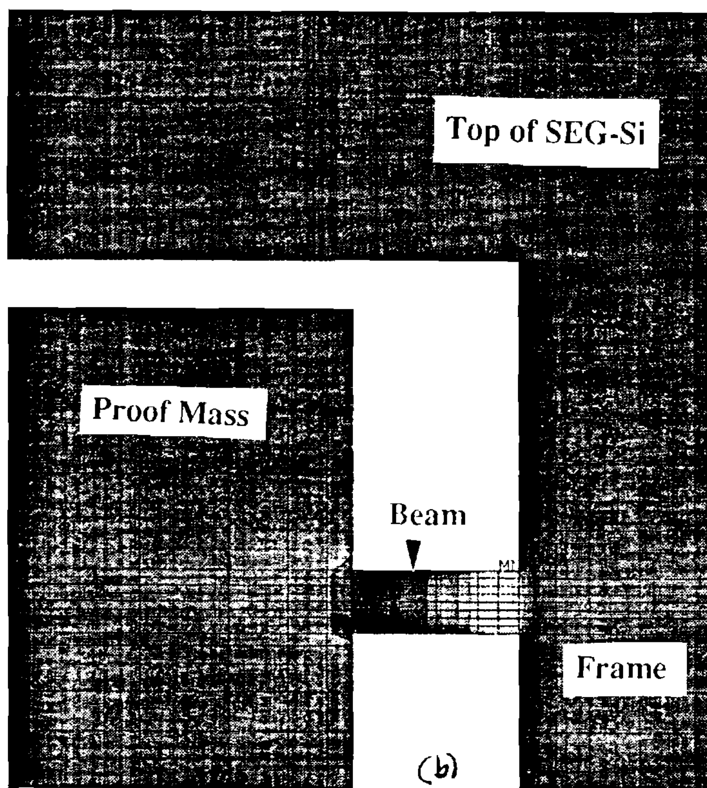
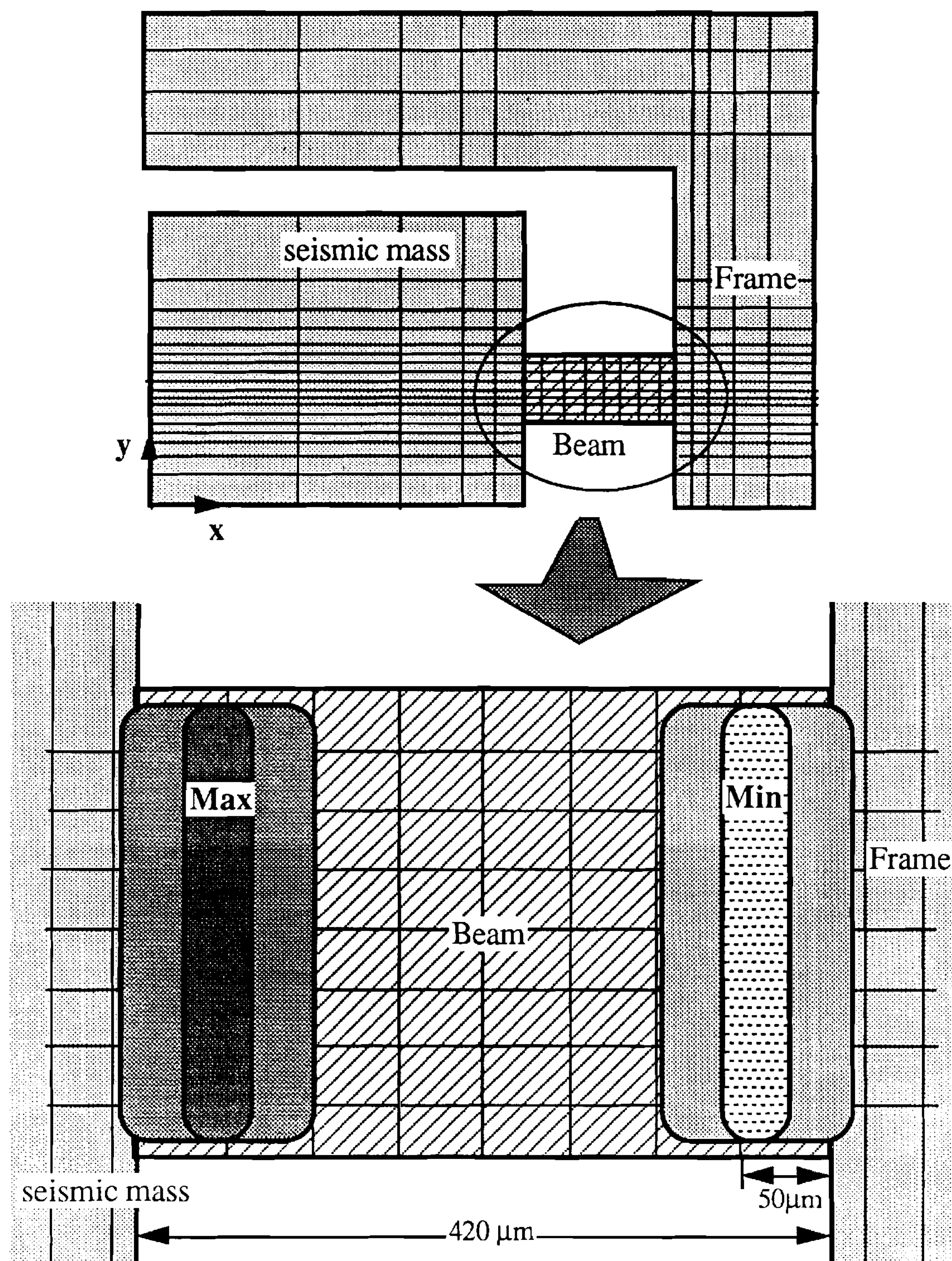


Figure 5.1 A plot of elements generated for ANSYS stress simulator on one quarter of the bridge-type accelerometer. (a) Side View. (b) Top view with stress contours generated by acceleration in the positive z direction (out of the paper).

The meshes were divided smaller on and near the beam area and larger in the seismic mass and frame in order to get a better simulation results. The beam is much thinner (≈10µm) than the seismic mass and the frame(= 350µm) and hence most of the stress generated by the applied force is distributed on and near the beam. Also the stress values change more rapidly than in any other region.

The letter 'MN' in the top view of the ANSYS plot of Fig. 5.1(b) indicates the place where the minimum stress along the x direction is generated on the top surface by the applied force in the positive **x** direction which is out of the paper. In this case the minimum stress means the most compressing force because the compressing force is indicated by the negative value. The maximum stress area is the area where the most expanding force is applied. The darkest region represents the area where the most stress is generated. Figure 5.2 is a schematic picture of the ANSYS plot for a clearer view. When the acceleration is reversed to the negative z direction, the maximum and minimum locations will be interchanged. Therefore, those two places are where the piezoresistors should be placed for a largest sensitivity of the accelerometer. The stress values obtained from the ANSYS analysis showed that the stress is positive from one side to the mid region of the beam in the x direction and is negative in the rest, which indicates that there is a zero stress point somewhere in the middle of the beam. Also, the maximum stress does not occur right at the frame edge but on the beam a little toward the mass from the frame edge. The stress on the frame edge is still shown to be quite large from the ANSYS results and hence the piezoresistors will be effective as long as their active region crosses the frame edge. The best placement would be to put the resistors over both the frame edge and maximum stress area. According to the ANSYS simulator, the maximum point exists approximately within 50 µm from the beam edge for the presently designed MELO-SI accelerometer.

Figure 5.3 shows the cross sectional view along the length of the beam. Both maximum and minimum stress points are indicated by 'MX' and 'MN' as shown in Fig. 5.3(b) and (c). This indicates that when the top surface of the beam expands the back of the beam compresses. This property has been employed in strain gage applications. The variation of the induced stress on the beam was examined by comparing the stress values on the nodes of the top surface. Each nodes are 50 µm apart and hence if the stress values are significantly different between the two nodes then the element defined by those two nodes can be divided again for a finer examination.



igure 5.2 A schematic drawing of the **ANSYS** simulation model. (a) Top view showing elements and nodes (b) **An** enlarged view of beam area showing maximum and minimum stress resulted from an applied stress.

First, the stress variation across the beam (along the beam width) was examined by comparing the stress at the maximum stress region. They ranged from 10.83 x 10^6 dyne/cm^2 to 11.2 x 10^6 dyne/cm^2 and its percent variation from the center to the edge is only 3.6%. Therefore, the misplacement of the piezoresistors along the beam width, or in the y direction, should not affect the sensitivity very much. The variation of the stress along the beam length, or in the x direction, is a little more significant. The stress varies from 10.83 x 10^6 dyne/cm^2 at the maximum location to 7.04 x 10^6 dyne/cm^2 on the frame edge and its percent variation was 35%. This indicates that sensitivity will be affected by 35% if the active region of the piezoresistors are misplaced from the frame edge. This result is somewhat different from the analytical solution due to the simplification of the analytical solution. However, if all the active part of the piezoresistor is placed further into the frame, the sensitivity variation becomes drastic. For example, if the stress level moves from 10.83 x 10^6 dyne/cm^2 at the maximum location to 0.54 x 10^6 dyne/cm^2, the percent variation becomes 95 percent and the resistance change from that particular piezoresistance will be almost zero. The ANSYS program, node and element numbers on the top of the beam, and their stress values can be found in Appendix B.

5.3 Dynamic Response of the MELO-Si Piezoresistive Accelerometer

For the dynamic response analysis, the idealized two-dimensional structure shown in Fig. 4.2(b) is again utilized to model the MELO-Si accelerometer. It is assumed that the frame and central section, which represents the seismic mass are rigid, that the deflections are small, and that the deformations are limited to the beams. The transverse vibrations of the accelerometer structure are considered only in the x-y plane, which is assumed to be a plane of symmetry for any cross section. When the beam is vibrating transversely, the dynamic equilibrium condition for forces in the y direction combined with the moment equilibrium condition produces the equation

$$\frac{\partial^2 M}{\partial x^2} dx = - \rho A \, dx \frac{\partial^2 y}{\partial t^2} \qquad (5.17)$$

where ρ is the material density of the and A is the area in the yz plane. By substituting the relationship $M = EI \frac{\partial^2 y}{\partial x^2}$ into Eqn.(5.17), the general equation for transverse free vibrations of a beam can be obtained as [3]

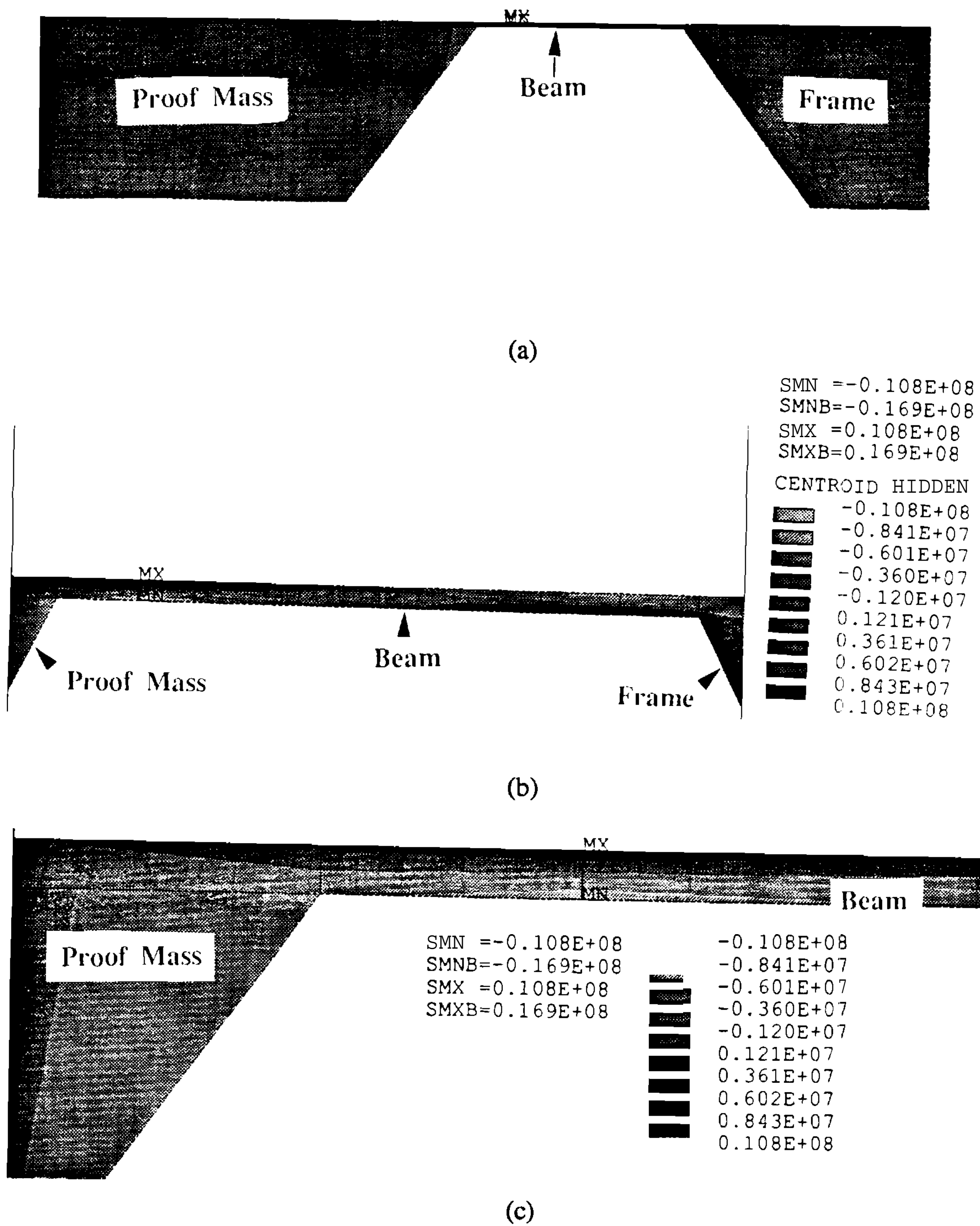


Figure 5.3 A cross section of elements generated for **ANSYS** stress simulator on quarter of the bridge-type accelerometer. (a) Side View. (b) Enlarged view showing the two maximum and minimum points at each end of the beam. *(c)*Enlarged view of the beam with the maximum stress.

$$EI\frac{\partial^4 y}{\partial x^4}dx = -\rho A\, dx\frac{\partial^2 y}{\partial t^2} \tag{5.18}$$

This equation may be rewritten, using the accelerometer structure geometry, as

$$EI\frac{\partial^4 y(x,t)}{\partial x^4} = -\frac{m_1}{l_1}\frac{\partial^2 y(x,t)}{\partial t^2} \tag{5.19}$$

When a beam vibrates transversely in one of its natural modes, the deflection at any location varies harmonically with time. Therefore, the solution of the Eqn.(5.19) can be written, by separation of variables, as

$$y(x,t) = X(x)\,T(t) = X(x)\,e^{jwt} \tag{5.20}$$

where $e^{j\omega t} = \sin\omega t + j\cos\omega t$. Substituting Eqn.(5.20) into Eqn.(5.19) results in

$$EI\frac{\partial^4 X(x)}{\partial x^4} - \frac{m_1}{l_1}\omega^2 X(x) = 0 \tag{5.21}$$

or

$$\frac{\partial^4 X(x)}{\partial x^4} - \left(\frac{\lambda}{l_1}\right)^4 X(x) = 0; \quad \left(\frac{\lambda}{l_1}\right)^4 = \frac{m_1\,\omega^2}{EIl_1} \tag{5.22}$$

Then the general form of the solution becomes

$$X(x) = C_1\cos\left(\frac{\lambda}{l_1}\right)x + C_2\sin\left(\frac{\lambda}{l_1}\right)x + C_3\cosh\left(\frac{\lambda}{l_1}\right)x + C_4\sinh\left(\frac{\lambda}{l_1}\right)x \tag{5.23}$$

where C_1, C_2, C_3, C_4 are constants to be determined and λ is a notation introduced for convenience as

$$\lambda^4 = \frac{48\pi^2}{E}\frac{m_1 l_1^3}{tw^3}f^2 \tag{5.24}$$

The constants can be determined from the following boundary conditions: (1) the deflection and the bending at the fixed end of the beam are zero, (2) the bending of the beam at $x=l_1$ is zero due to the solid connection of the beam with the stiff seismic mass, and (3) the

transverse force must be continuous. From these boundary conditions, the following equations are obtained.

$$X\big|_{x=0} = \frac{dX}{dx}\bigg|_{x=0} = \frac{dX}{dx}\bigg|_{x=l_1} = 0$$

$$EI\ \frac{\partial^3 y(x,t)}{\partial x^3}\bigg|_{x=l_1} = \frac{m_2}{4}\ \frac{\partial^2 y(x,t)}{\partial t^2}\bigg|_{(x=l_1)} \tag{5.25}$$

Form those boundary conditions and the relationship of Eqn.(5.24), the following equation results in:

$$\frac{m_1}{m_2} = \frac{\lambda}{4}\,\frac{1-\cos(\lambda)\cosh(\lambda)}{\sin(\lambda)\cosh(\lambda) + \cos(\lambda)\sinh(\lambda)} \tag{5.26}$$

For a given mass ratio m_1/m_2, an infinite number of h-roots exist which satisfy Eqn.(5.26). These roots are coupled with possible harmonic modes of the system as shown in Eqn.(5.24). The first seven roots, λ_i, are shown in Table 5.2.

The first lowest non-zero root, λ_1, corresponds to the first resonant frequency and it shows a strong dependence on m_1/m_2 while the higher resonant frequencies are relatively independent of this ratio. Its value for the MELO-Si accelerometer is 3.816kHz assuming the beam dimension is 10μm thick, 420μm long, 170μm wide, and the seismic mass is 2.71mg. Further λ values can be approximated by the relationship $\lambda_{i+1} = \lambda_i + \pi$ for i 22, as shown in Table 5.2. Their frequency values can be obtained from the relationship expressed in Eqn.(5.24). The first resonant frequency also can be obtained by a series expansion of the right hand side of Eqn.(5.26), by expanding each sinusoidal function and taking the lowest order term [4]. It results in the equation

$$f_1 = \frac{1}{2\pi}\sqrt{\frac{4Ewt^3}{l_1^3 m_2}} \tag{5.27}$$

Table 5.2 The first seven roots of the dynamic response differential equation.

ith root	1	2	3	4	5	6	7
λ_i	0.4142	4.7305	7.8535	10.9958	14.1373	17.2789	20.4045

It is desirable to make the sensitivity of the accelerometer as large as possible without incurring limitations on the bandwidth. Since the resonant frequency mainly depends on the structural geometry, the sensitivity can be adjusted using the same resonant frequency by optimizing other parameters such as orientation of the piezoresistors, doping type and concentration of the resistors, and so on.

5.3.1 Dynamic Response to the off-axis movement

The accelerometer generally has a number of response modes. One fundamental mode exhibits motion in the acceleration axis of interest while there are numerous secondary modes. Some relate to minor spring-mass pairs such as the resonance of the mass itself. When the secondary modes appear to affect the off-axis sensitivity, they need to be considered with care. One of the major advantages that the four bridge accelerometer structure has over the double bridge or cantilever-type accelerometer structure is a substantial reduction in off-axis sensitivity and unwanted resonant frequency modes. Figure 5.4 shows the three major secondary modes for the four bridge accelerometer structure [5]. Each of them has a resonance associated with it. For the four bridge accelerometer, is was indicated that the ratio of the resonant frequencies of those modes is 1:2:1.6 respectively [5]. Particularly the third mode will depend on the effective spacing between the pair of beams on one side of the seismic mass and can be minimized by controlling their spacing.

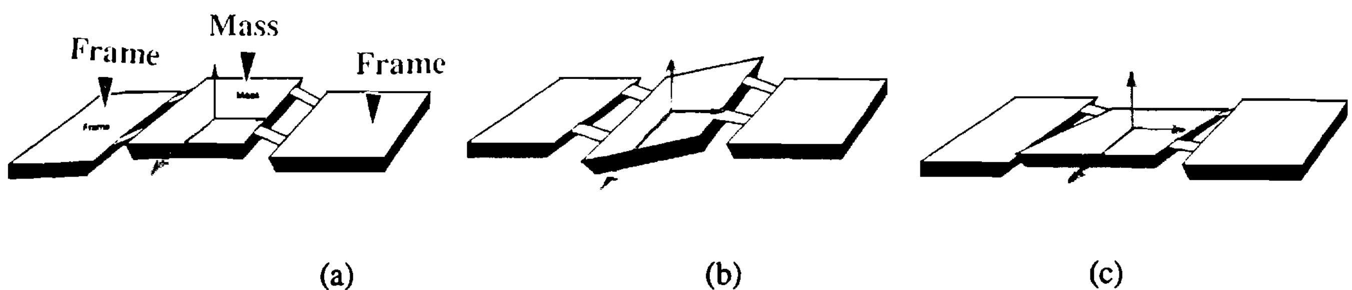


Figure 5.4 Three principle modes of motion for a bridge-type accelerometer with four beams. (a) Vertical (desired) mode. (b) Lateral mode. (c) Perpendicular mode.

For a bridge-type accelerometer, even if the off-axis sensitivity can not be eliminated, the third mode of Fig. 5.4(b) can be compensated and minimized. When the seismic mass happens to tilt up on one side, as shown in Fig. 5.4(b), the opposite side tends to tilt down and this in fact can compensate the first motion. The careful placement of the piezoresistors can effectively cancel this off-axis component because opposite sides of the structure are in opposite bending modes. This compensation can not be obtained from a cantilever-type accelerometer because there is no such symmetry.

5.3.2 Dynamic Response Simulation by Finite Element Methods

The dynamic response was simulated by a one dimensional finite element method because the simulation of dynamic response by ANSYS simulator requires much larger computer storage space and memory. In addition, since the structure is simple and syrnmemcal, the interesting answer is the resonant frequency of the entire system, not the stress distribution on the surface like static response, a one dimensional response can provide the desired solution. The structure was simplified as a beam with a bigger mass dismbutor in the middle like Fig. 4.2(b) and the elements were divided in the x direction only. Since this is a one dimensional simulation, only the first mode and third mode resonance of Figs. 5.4(a) and (b)are considered. The first mode resonant frequency for the accelerometer of this work was 2.805kHz whereas the third mode resonant frequency as 6.909kHz. Their corresponding cross section curves are shown in Fig. 5.5.

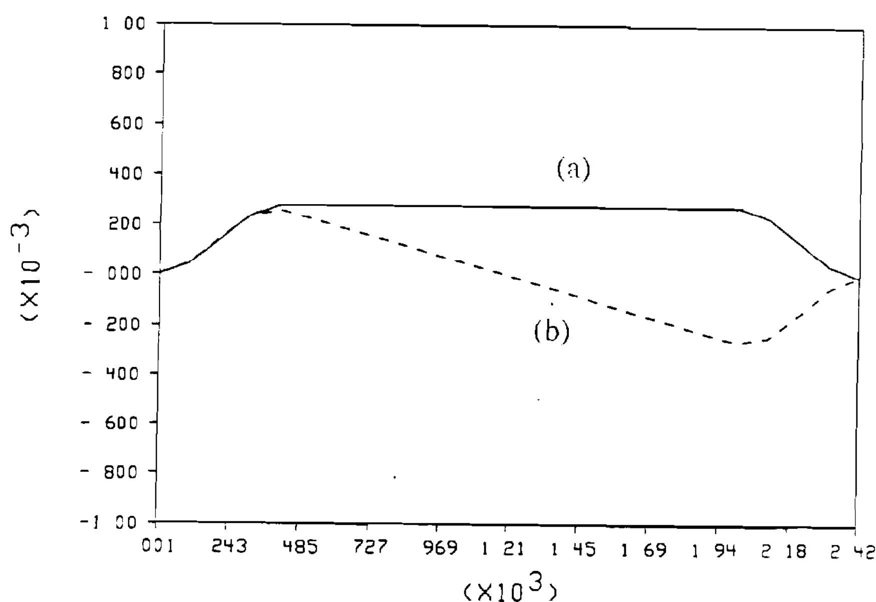


Figure 5.5 The cross section curve of the (a) first and (b) third resonance modes obtained from one dimensional simulation using a finite element method.

5.4 Experimental Results

The MELO-Si accelerometers were successfully fabricated and tested for evaluating the MELO-Si diaphragm fabrication technology and the accelerometer performance. In this section, their experimental results are presented. The accelerometers were designed to have good linearity up to 30g, thirty times gravitational acceleration, which is one of the specifications for automobile air-bag actuation [6]. First, the testing measurement system is described then the sensitivity, resonant frequency from the dynamic response, and the linearity of the fabricated accelerometer are presented. The experimental results are compared with the theoretical results and the effects of tolerances on the results are discussed.

5.4.1 Accelerometer Measurements System

Once fabrication of the MELO-Si accelerometers was completed, the wafer was cleaved into dies and each die was placed on the back-plate die. Each-back plate has a basin pattern aligned so that for each accelerometer the seismic mass was limited to the displacement of the mass in the transverse direction when the shock or overforce was applied to the accelerometer. The back-plate not only protects the accelerometer from the shock but also gives a mechanical support to the device after the thin MELO-Si diaphragm was fabricated around the seismic mass for the last lithography step of front delineation. The mask was designed to open narrow paths along the die boarder on the back at the same time with back-etch patterning so that the exposed silicon is etched by KOH etchant. The purpose is to separate each die easily without sawing and damaging the fragile MELO-Si diaphragm. However, if the MELO-Si diaphragm is strong enough, then the whole wafer can be processed, attached to the back-plate, and cut into die using a diamond saw. Each die is then packaged and bonded with aluminum wire.

Both static and dynamic testing were performed on the same testing system which is schematically illustrated in Fig. *5.6.* The testing system consists of an electrodynamic shaker, a mount fixture, signal generator, oscilloscope, charge amplifier, power amplifier, and bridge conditioning amplifier. The sinusoidal signal generator has a capability of a programmable sweep generation for continuous frequency response testing. Sweep limits, rate, type (linear or log), and number of sweeps can be programmed. A desired signal is generated by the signal generator and becomes an input to the power amplifier. The signal is then amplified by the power amplifier and sent to the electrodynamic shaker which applies acceleration to the accelerometer under test. A shaker provides a vibrating motion at

various acceleration levels depending on the signal amplitude, between 0 and 1 (root mean squared) RMS volts from the power amplifier. The frequency of the input signal is changed by the signal generator. A reference accelerometer was mounted in the same shaker fixture and its output was calibrated by the charge amplifier so that the applied acceleration can be identified from the output of the reference accelerometer. The output signal of the reference accelerometer was calibrated to provide 10mV per every 'g' of acceleration. Output from the MELO-Si accelerometer was amplified by the bridge conditioning amplifier in order to observe the magnitude of the output signal on the oscilloscope since the original output voltage is usually less than 1mV. The voltage gain of the bridge amplifier was set at 100.

5.4.2 Theoretical Evaluation of the Sensitivity and Resonant Frequency

The sensitivity and resonant frequency of the MELO-Si bridge-type accelerometer are estimated in this section in order to explain the performance of the fabricated accelerometers. The theoretical sensitivities were obtained from the analytical solution compiled in Table 5.1 and the frequency was calculated from Eqn.(5.27). Table 5.3 shows the sensitivity and resonant frequency values of not only the ideal structure but also the structure with varied beam dimensions. The beam dimension can vary if the process was not carefully controlled when the KOH etching or the RIE was performed. Particularly, since the RIE is used for the front delineation and its etching is isotropic, the lateral etching becomes the same as the vertical etching which will change the beam length, width, and even the thickness while delineating the beams. Therefore, the narrower and longer beams were considered in this calculation. Also, the doping concentration of the piezoresistors can vary between 1 x $10^{18}/cm^3$ and 1 x $10^{19}/cm^2$ depending the boron ion implantation. Therefore, the second group in the table contains the calculated values using the piezoresistors corresponding to the doping concentration of 1 x $10^{18}/cm^2$.

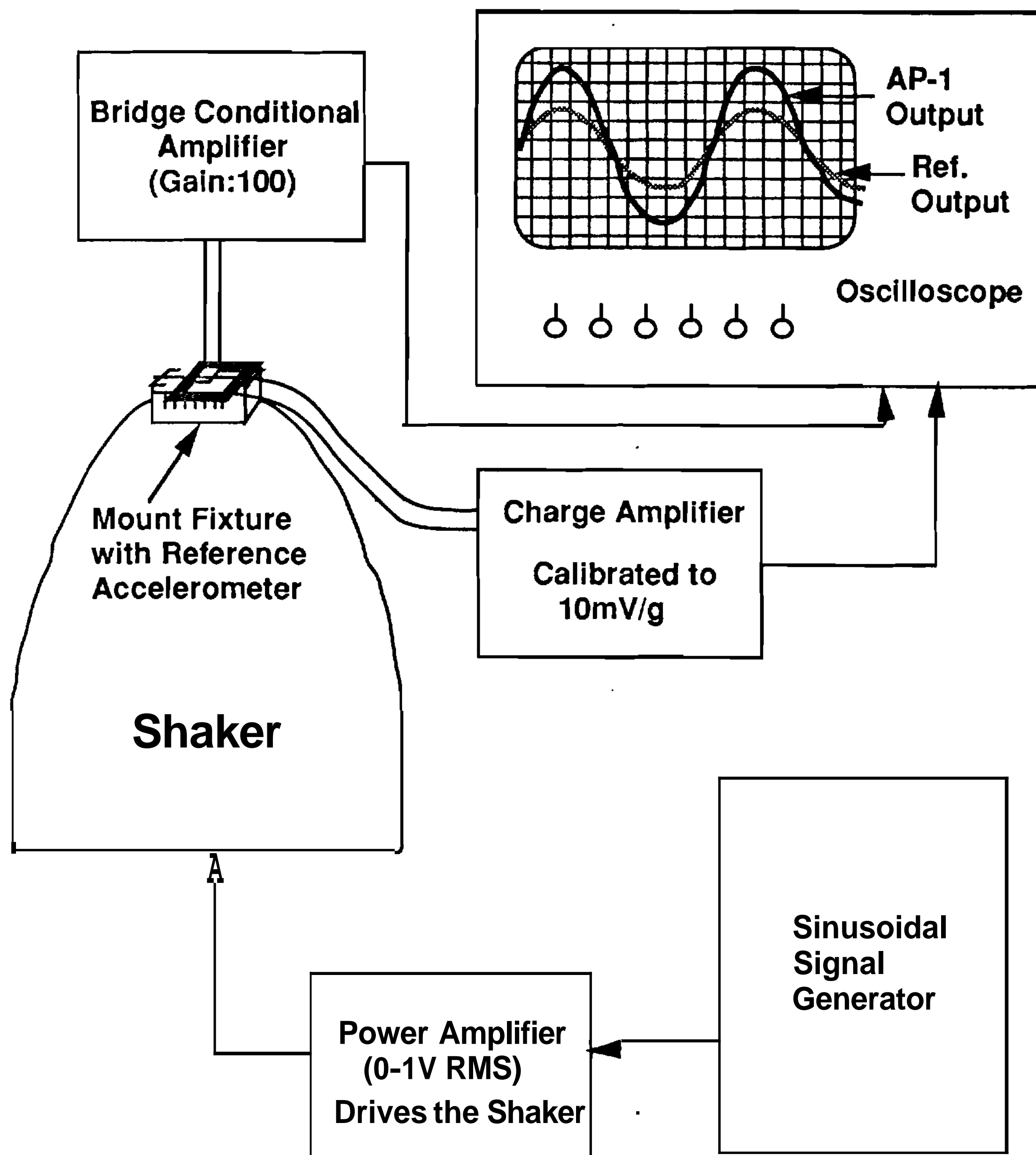


Figure 5.6 Testing measurement system for accelerometer characterization.

Table 5.3 Sensitivity and resonant frequency obtained by the analytic solution for two different piezoresistance coefficient value: 70 x 10^{12} cm^2/dyne and 50 x 10^{12} cm^2/dyne corresponding to the piezoresistor doping concentration of 1 x 10^{18} /cm^3 and 1 x 10^{18} /cm^3 respectively.

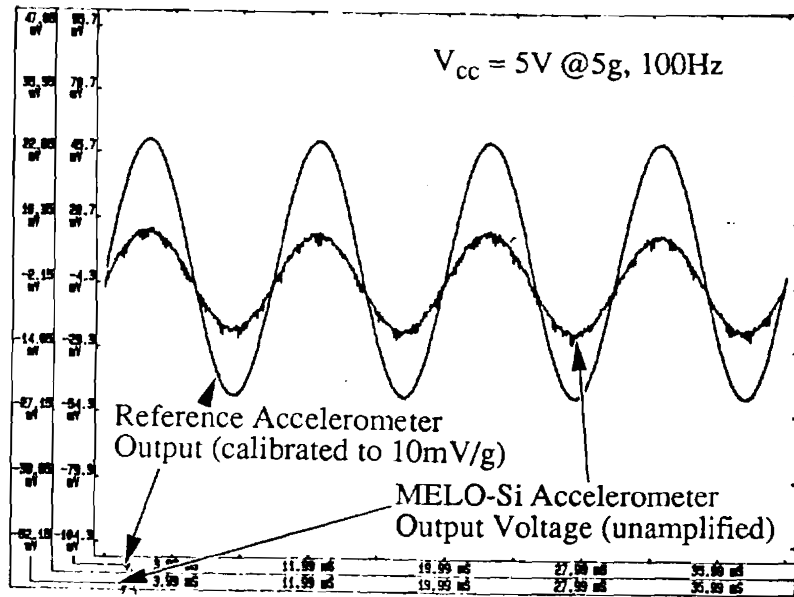
	Ideal Case (10μm)	10μm Lateral Etch	Ideal Case (20μm)	20μm Lateral Etch
Beam Thickness (cm)	0.001	0.001	0.002	0.002
Beam Width (cm)	0.017	0.015	0.017	0.011
Beam Length (cm)	0.042	0.044	0.042	0.046
Seismic Mass (gram)	0.00271	0.00271	0.00271	0.00271
Young's Modulus (dyne/cm^2)	1.7E+12	1.7E+12	1.7E+12	1.7E+12
Gravitational Acceleration (g/cm^2)	980	980	980	980
Number of Beams	4	4	4	4
Extension of Piezoresistor (cm)	0.0028	0.0028	0.0028	0.0028
Piezoresistance coefficient (cm^2/dyne) @ dose=1x10^{18}/cm^3	7E-11	7E-11	7E-11	7E-11
Maximum Sensitivity (μV/V-g)	321.5	382.97	80.38	136.89
Resonant Frequency (kHz)	3.819	3.345	10.8	7.58
Piezoresistance coefficient (cm^2/dyne) @dose=1x10^{19}/cm^3	5E-11	5E-11	5E-11	5E-11
Maximum Sensitivity (μV/V-g)	229.65	273.55	57.4	97.78
Resonant Frequency (kHz)	3.82	3.345	10.8	7.58

5.4.3 Sensitivity of the MELO-Si accelerometers

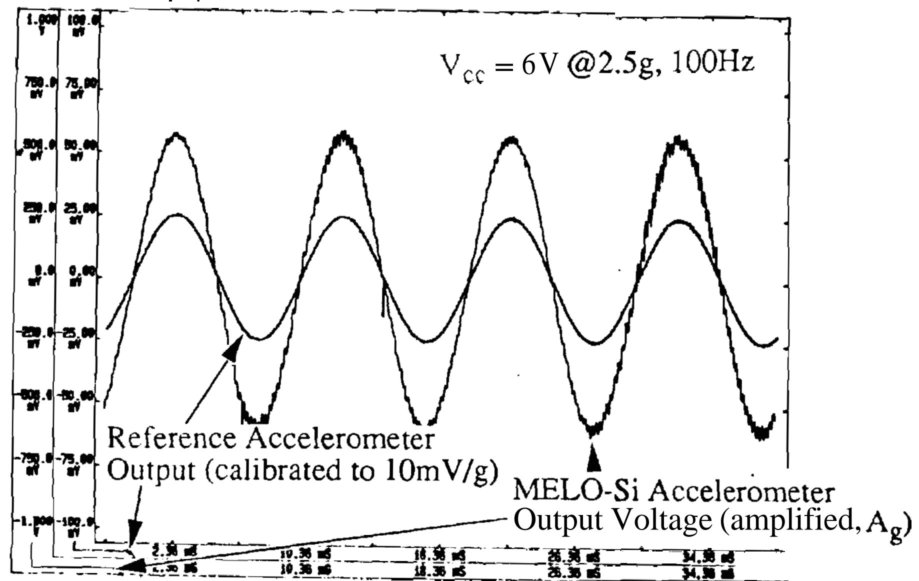
Figure 5.7(a) illustrates the unamplified output voltage (AV) of an accelerometer with 10μm thick beam and the reference accelerometer at 5g and 100Hz. The maximum RMS (root mean squared) output voltage of the reference accelerometer was approximately 50mV which corresponds to the applied acceleration because the charge amplifier was calibrated for 10 mV/g as described in the previous section. Accelerometer sensitivity was obtained by dividing the maximum output voltage by the input supply voltage and the applied acceleration. In this measurement, the supply voltage was 5V DC and the applied acceleration was 5g. The resulting sensitivity was 286.88 μV/V-g. The small oscillating characteristics superimposed on the output signal was caused by the resonant frequency. This phenomenon becomes more obvious in the amplified output signal as shown in Fig. 5.7(b), where the applied acceleration was 2.5g, the frequency was 100Hz, and the applied voltage source was 6V DC. Here, the output signal was amplified by the bridge conditioning amplifier. Table 5.4 shows all the sensitivity and resonant frequency results from the MELO-Si accelerometers including the accelerometers, with 20μm thick beams.

Table 5.4 Sensitivity and resonant frequency measured from the MELO accelerometers with both 10μm and 20μm thick MELO- Si beams.

		Sensitivity (μV/V/g)	Resonant Frequency (kHz)
10μm thick MELO-Si beam	Test #10-1	286.88	2.026
	Test #10-2	168.19	3.052
20μm thick MELO-Si beam	Test #20-1	152.79	1.384
	Test #20-2	101.78	2.5
	Test #20-3	50.88	4.19
	Test #20-4	47.76	4.128
	Test #20-5	37.52	4.2
	Test #20-6	34.67	4.0
	Test #20-7	21.51	4.4



(a)



(b)

Figure 5.7 The test output of a MELO-SI accelerometer with 10μm thick beam. (a) Unamplified MELO-Si accelerometer output overlaid with the reference accelerometer output at 5g and 100 Hz. (b) Amplified MELO-Si output with the reference accelerometer at 2.5g and 100 Hz.

5.4.4 Linearity of the MELO-Si Accelerometer Output

The linearity of the MELO-Si accelerometer was examined by two different methods. First, the linearity was compared with the linearity of the reference accelerometer as shown in Fig. 5.8. The linearity of the both accelerometers are quite close to each other and is excellent up to 30g. Secondly, the maximum RMS output voltage of the accelerometer was measured from 1g to 30g with an increment of 1g and then these output voltage data were plotted with respect to the applied acceleration. Figure 5.9(a) shows a plot of the output voltage versus acceleration of Test #10-1. Figure 5.9(b) illustrates that the nonlinearity, calculated from the data, for the Test #10-1 accelerometer up to 30g which was less than ±4%. Once the output voltage data are obtained, the linear curve-fit can be applied in order to get the linearity of the output curve as shown in Fig. 5.10. The linear curve-fit was applied to all the measured data and it was found that all the data are within 5% error bar from the curve-fit. This also relates to the linearity of the data.

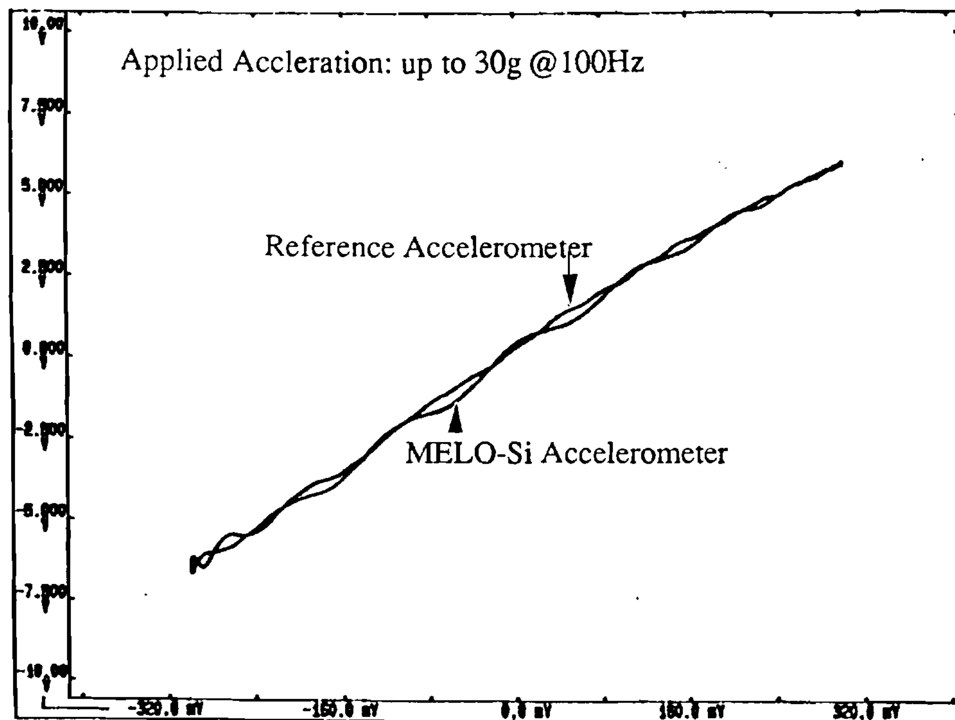
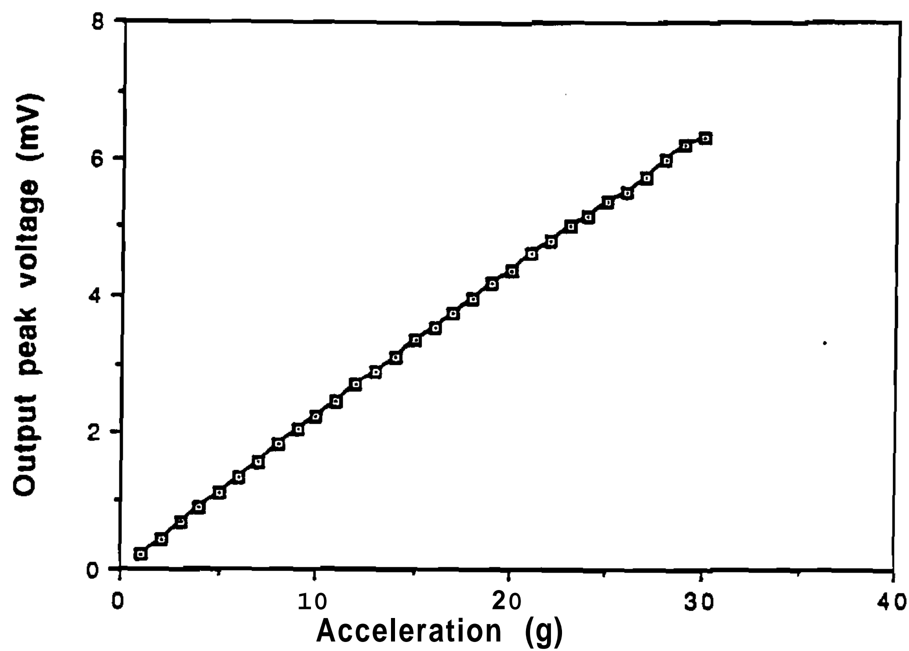
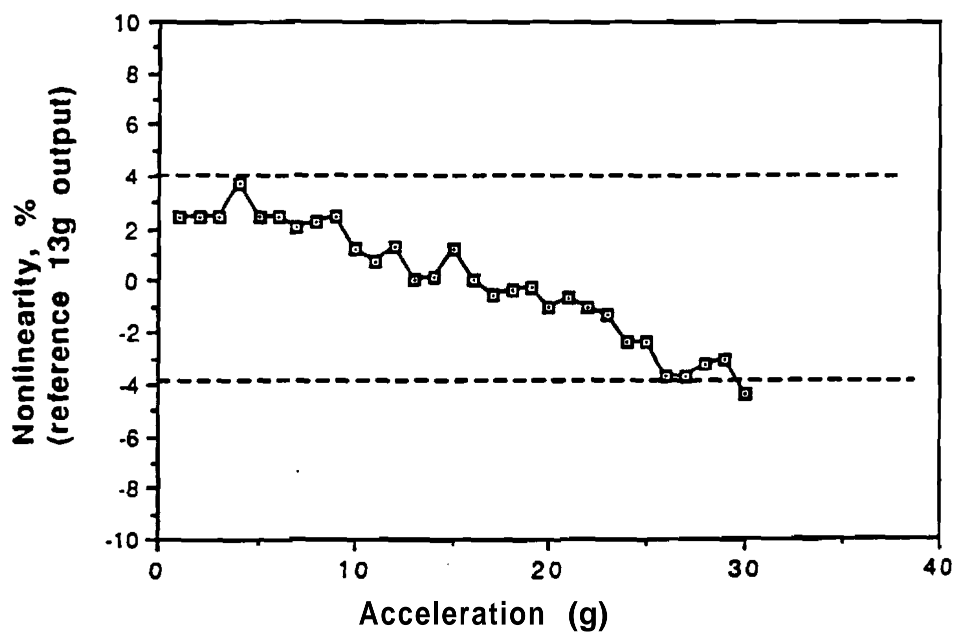


Figure 5.8 The relative linearity comparison between the reference accelerometer and the MELO-Si accelerometer Test #10-1 from 1g to 30g acceleration.

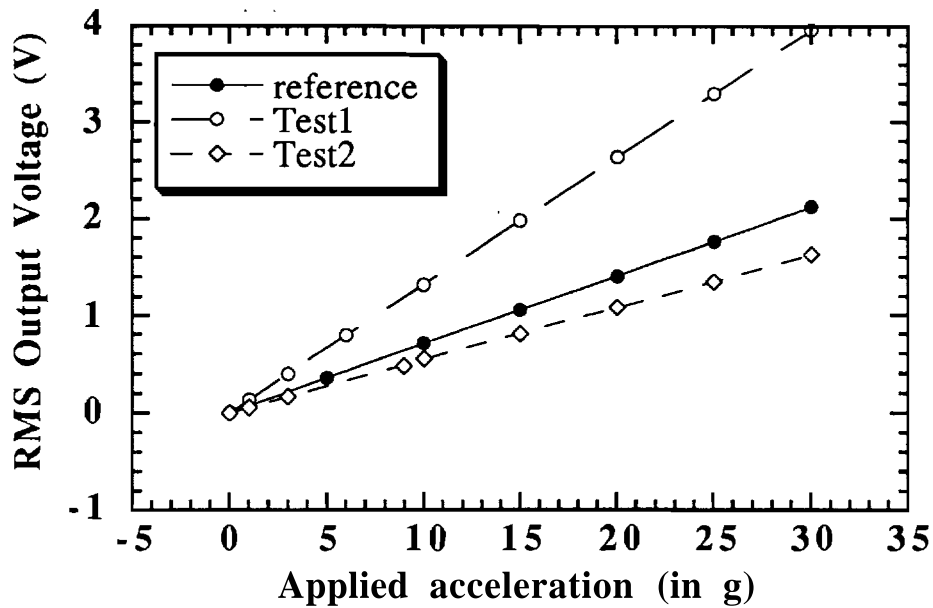


(a)

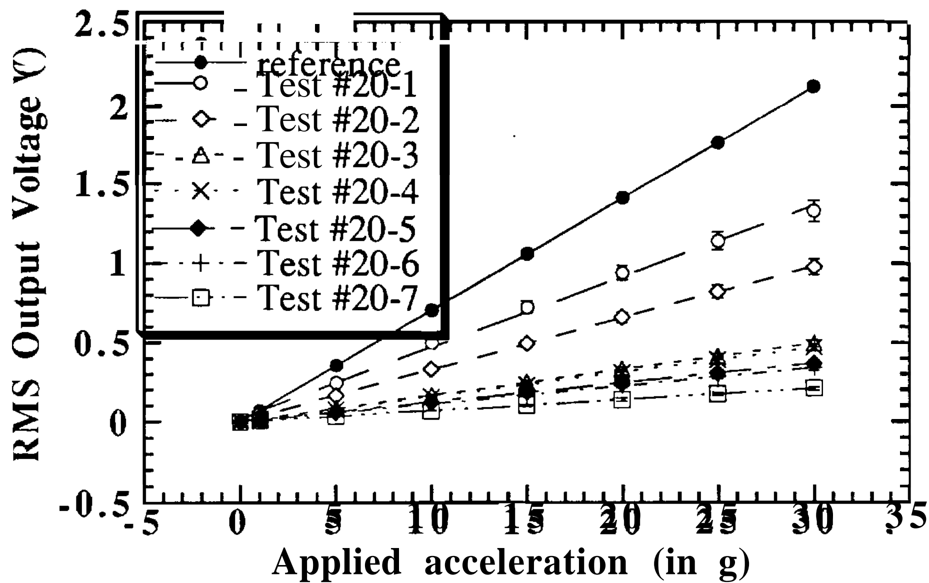


(b)

Figure 5.9 The linearity of the MELO-Si accelerometer Test #10-1. (a) The output voltage versus applied acceleration up to 30g. (c) percent non-linearity curve up to 30g acceleration.



(a)



(b)

Figure 5.10 The curve-fit of the measured output voltage for the linearity of (a) Test #10-1,2 and (a) Test #20-1 to 7 up to 30g acceleration.

5.4.5 Resonant Frequency of the MELO-Si Accelerometers

The resonant frequency of the MELO-Si accelerometer was measured by the natural vibration which can be obtained on the testing floor. It also could be measured from an impulse response of an accelerometer, as illustrated in Fig. 5.11, from which the period of the sinusoidal signal and hence the resonant frequency can be calculated by inverting the period. The best method is, however, to use the transfer function gain plot and the phase plot simultaneously since a 90° phase shift should appear when the resonant frequency is reached. Figure 5.12(a) and (b) illustrate a typical transfer function which was obtained from Test #20-1. The resonant frequency is obvious when the phase plot curve crosses the 90" shift and the gain reaches the peak value.

The resonant frequency is supposed to be a function of the beam dimensions and the proof mass but independent of the dose, shape, and the location of the piezoresistors. Therefore, the resonant frequency is sometimes used to extract the beam thickness of the accelerometers and evaluate the thickness variation between dies or wafers assuming other parameters such as beam length, width, and proof mass are precisely controlled. However, with the MELO-Si accelerometer, the resonant frequency may vary with the shape of the V-grooves etch-stop on the back of the beams. For example, even though the beam thickness was designed to be 20μm, the resulting effective thickness for the resonant frequency may become 18μm or even smaller depending on the V-groove depth.

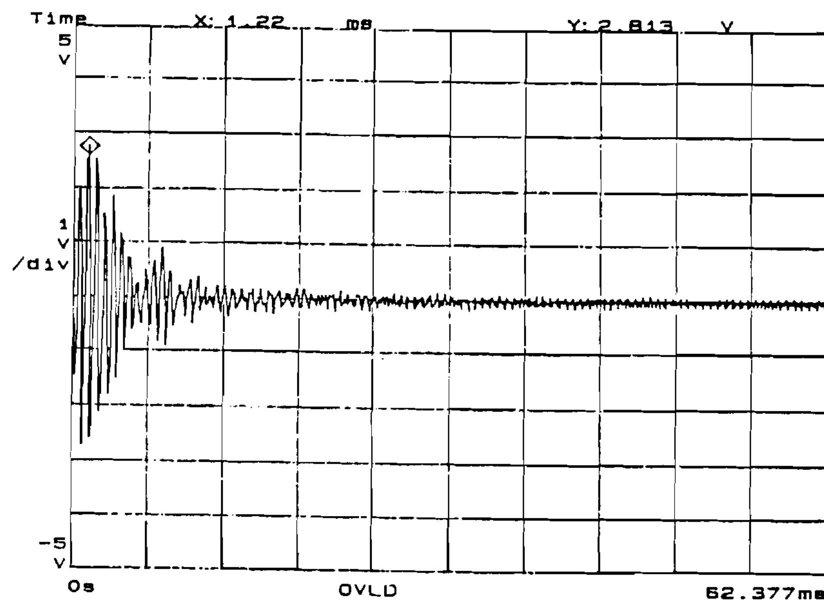
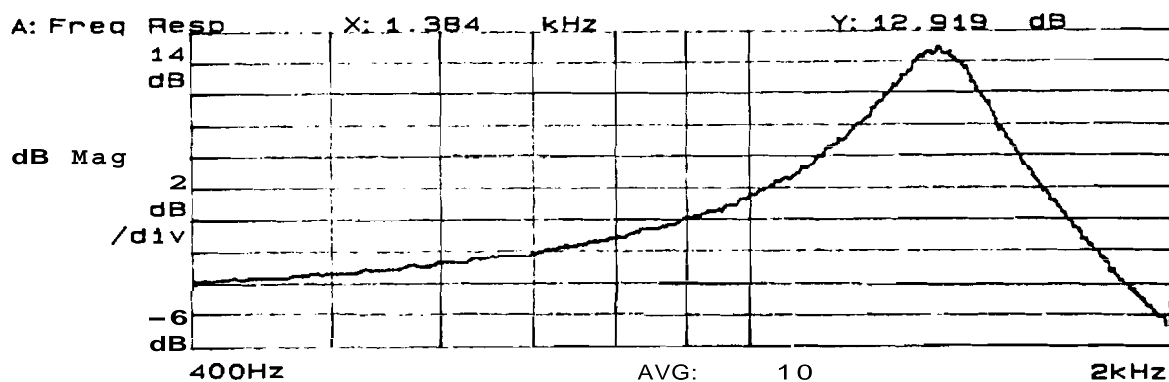
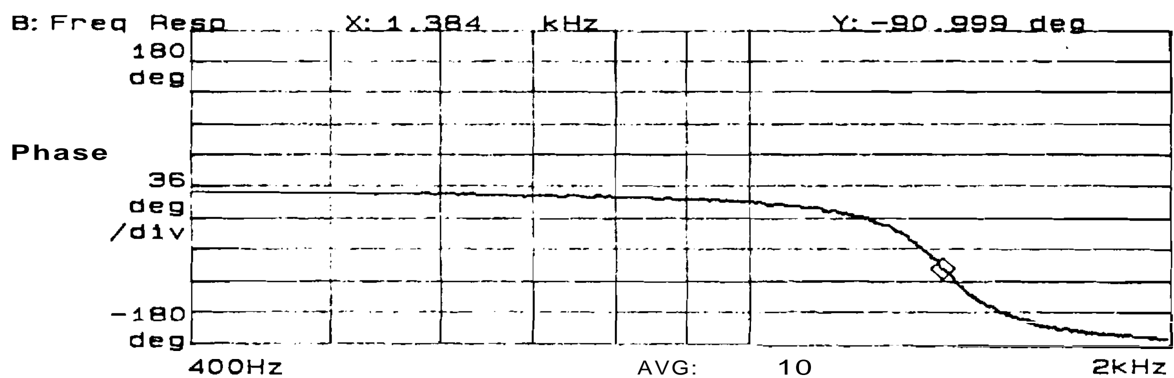


Figure 5.11 A typical impulse response of the MELO-Si accelerometer, which can be used for calculating its resonant frequency. This was from Test #10-1.



(a)



(b)

Figure 5.12 The plot the transfer function obtained from the MELO-Si accelerometer Test #20-1. (a) Gain. (b) Phase

5.5 Effect of front-to-back misalignment

The experimental results from Test#10-1 and #10-2 somewhat agreed with the theoretical results since the sensitivity might vary from 200 to 400 μV/V-g without considering the variation of the beam thickness. The piezoresistors placement on the beam was examined and they were on the desired locations. The resistance of the each piezoresistor can range from 3KR to 10KΩ on a 3 inch wafer depending the beam current distribution during boron ion implantation. However, the accelerometers with 20μm thick MELO-Si beam had an additional problem. During the front-to-back mask alignment, the mechanical arm of the SUSS double sided mask aligner holds the wafer during the mask alignment step When the alignment is done, the arm releases the wafer on the bottom mask for exposure. The mechanical arm tends to slide the wafer when it releases the wafer and causes a misalignment. It occurred with the Test#20 dies and varied the sensitivity of the accelerometers into a wide range. Therefore, in this section, the effect of the front-to-back misalignment on the sensitivity and resonant frequency of the MELO-Si accelerometer is presented.

It is assumed that if the active part of the piezoresistors are residing on the frame edge or the proof mass then all those resistors experience the identical resistance change and that the resistance change is much smaller compared to the original resistance value. When the misalignment is severe enough to cause the half number of the piezoresistors to be insensitive to the applied stress, the output voltage becomes half of the normal case. The detail calculations of the analysis are shown in Figs. 5.13 and 5.14. When the experimental data of Test#20 accelerometers were compared to the analytical results, including the effect of ion implant dose variation, and the beam dimension variation by RIE, the sensitivity and resonant frequency didn't correlate with each other. However, adding the effect of the misalignment, the analytical results and the experimental results correlated better. This correlation will improve if the stress distributes along the frame and the mass as well as the beam can be expressed more accurately because the stress was assumed to be localized only on the beam in the current analytical solution.

Table 5.5 shows the misalignment values for each MELO-Si accelerometers by measuring them under an optical microscope but the thickness, which would be the most important parameter, was not measured because the non-destructive measurement methods was not available. Also, the optical microscope pictures of the accelerometer top views are illustrated in Figs. 5.15 and 5.16. For more accurate analysis of the measurement results, the thickness and the proof mass (or volume) also need to be measured accurately.

With Perfect Alignment:
All 8 resistors will change their resistances due to applied stress

Assuming all Ri's (i=1 to 8) are same as R

$$Vout = ((2R-2\Delta R)/4R - (2R+2\Delta R)/4R))*Vcc$$
$$= (\Delta R/R)*Vcc$$

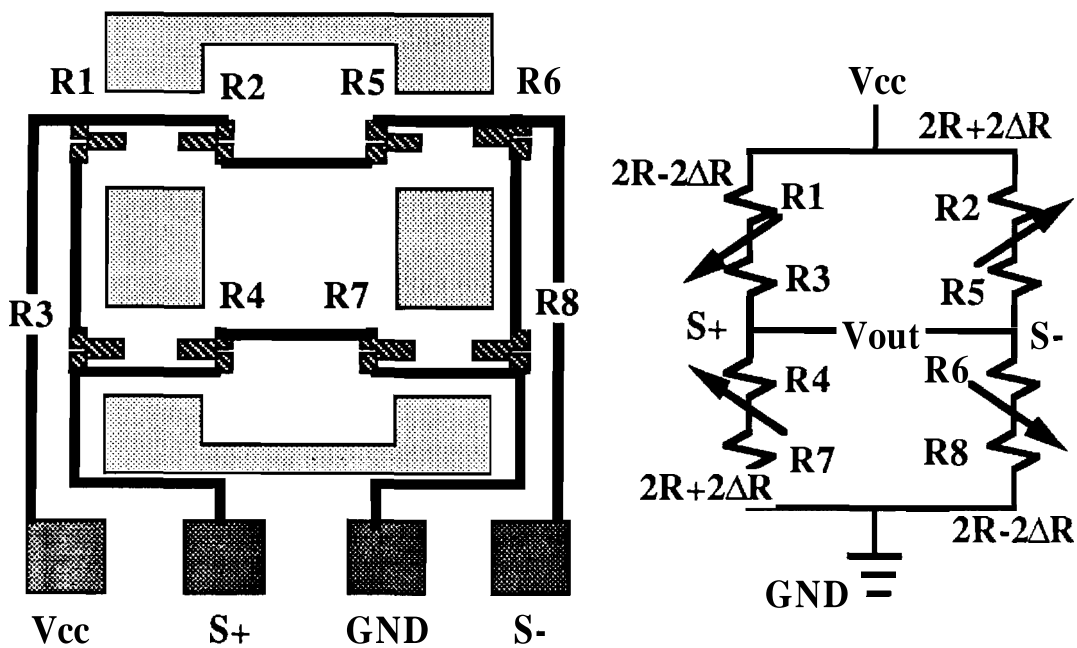


Figure 5.13 Theoretical V_{out} value from a bridge-type accelerometer with four bridges and eight piezoresistors from a resistance change due to the applied stress with a perfect front-to-back alignment.

With Backside Misalignment:
Only 4 resistors will change their resistances due to applied stress
In this example, R1,R3,R5, and R7 are not changing their resistance
Only R2, R4, R6, and R8 are changing their resistances.

Assuming all Ri's (i=1 to 8) are same as R

$$Vout = ((2R+\Delta R)/(4R+\Delta R) - (2R-2\Delta R)/(4R-\Delta R))*Vcc$$
$$= (\Delta R(8R+\Delta R)/(4R*4R-\Delta R*\Delta R))*Vcc$$

Assuming $\Delta R << R$,

$$Vout = (\Delta R*8R/(16R*R))*Vcc = (\Delta R/2R)*Vcc$$

Therefore, the sensitivity will become half of the ideal case
if that is the only difference. However, the linearity still holds.

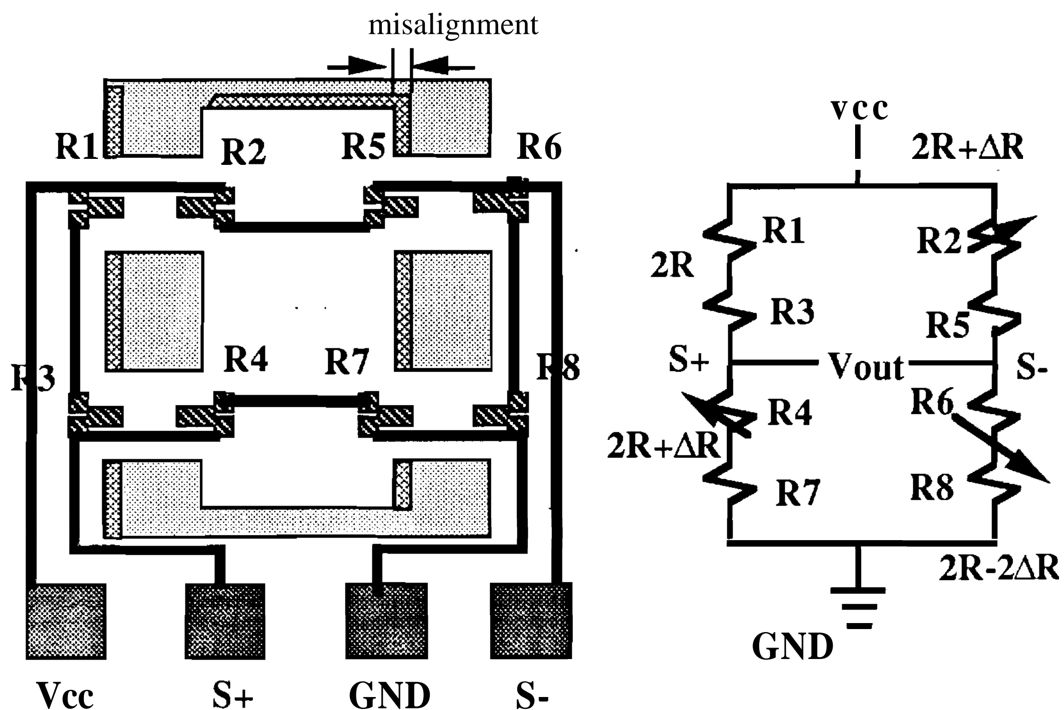


Figure 5.14 Theoretical V_{out} value from a bridge-type accelerometer with four bridges and eight piezoresistors from a resistance change due to the applied stress with a front-to-back misalignment.

Table 5.5 The misalignment along the beam direction in each MELO-Si accelerometer.

Accelerometer	#10-1	#10-2	#20-1,2	#20-3	#20-4,5,7	#20-6
misalignment (μm)	19.2	0	48.0	overetched	60	43.2

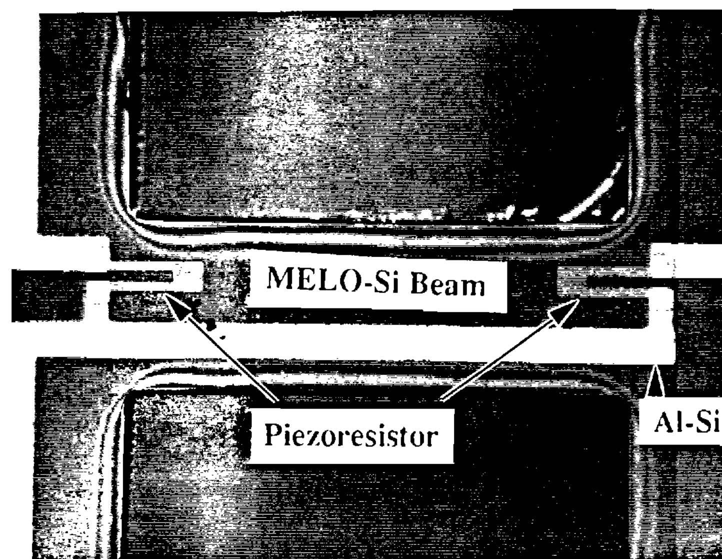
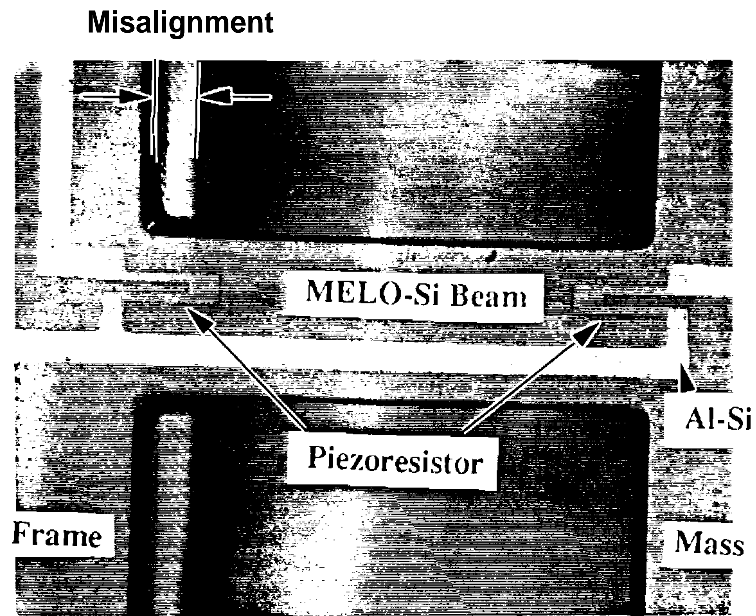
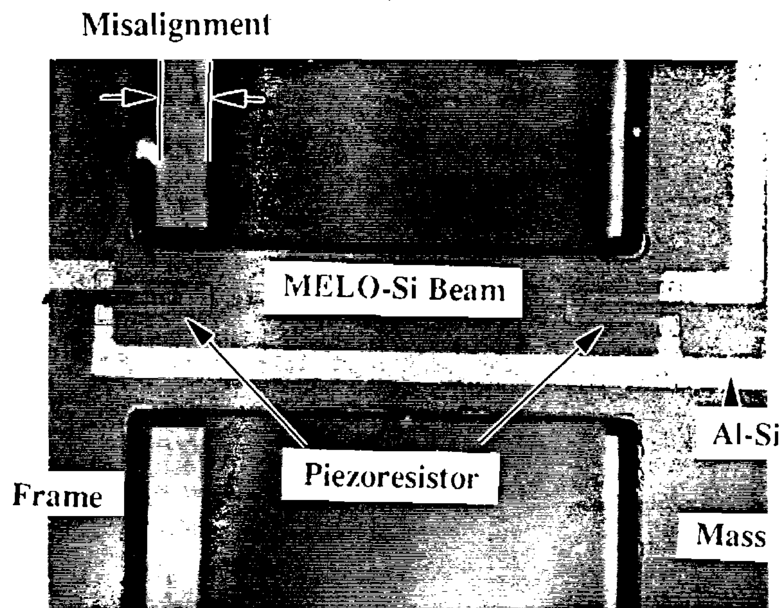


Figure 5.15 A top view of the MELO-Si accelerometer beam with zero misalignment shown from Test#10-2.



(a)



(b)

Figure 5.16 A top view of the MELO-Si accelerometer beam. (a) A minor misalignment shown from Test#10-1 and Test#20-1,2,6 (b) A major misalignment shown from Test#20-4,5,7

5.6 References

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CHAPTER 6
SURFACE MICROMACHINED MICROMECHANICAL STRUCTURES

6.1 Introduction

Over the last three decades, the rapid progress in the area of microelectronics has facilitated the successful implementation of large scale integration of many circuits on a single chip. The number of transistors integrated on a chip of silicon has been increased at the rate of two orders of magnitude per decade with sharp decrease in functional cost. The continuing progress in micro-electronics has tremendously improved the areas of system control and signal processing. As a result, the smart micro-computer has found its way to enter into our everyday life. For further expansion of the field of application of the smart VLSI systems, better interfacing and comparatively low cost sensors for sensing the signals from non-electronic hosts are necessry. A microprocessor is virtually blind, deaf, and dumb without suitable sensors to provide input from mechanical and physical variables. Without smart actuators the microcomputer is powerless to carry out control functions. Today, sensors hold the key to the successful entry of VLSI into a variety of new market areas, including those in health care, consumer products, automated manufacturing, and the automotive industry [1-3,7].

Historically, much effort has been applied to produce integrated sensors using bulk micro-machining [4-9,14,18]. Usually, the bulk micromachined silicon diaphragm dimensions are larger than 1x1 mm^2 with a thickness of approximately 5 - 20 μm. It is difficult to make micro size diaphragms less than 100μm on a side using these techniques. Bulk micromachining severely limits device density and weakens the mechanical integrity of the wafer during manufacturing. Front-to-back side wafer alignment is another added complication to the process. Furthermore, anisotropic silicon etchants (KOH or EDP) require a long etch time and potentially lower the yield of working circuits and sensors on the wafer.

The mechanical characterization of thin film micro-structures critically depends on the average residual stress in the film. The commonly used heavily boron-doped Si diaphragms have sufficient internal tensile stress that their pressure sensitivity is substantially reduced when compared with lightly doped diaphragms [3]. Hence, the search for low doped single crystal silicon diaphragms has become a very important issue in sensor technology. Again, for further miniaturization of sensors, the need for a IC compatible, one sided process, is very important. Surface micro-machining is a rapidly developing technology which extends the range of micro-mechanical materials and

structures that can be fabricated using only a planar technology. Recently, with the introduction of surface micro-machining techniques polysilicon/nitride membranes, using laterally-undercut sacrificial layers, have been fabricated for piezoresistive type sensors [23,25,27,29,33]. Both polysilicon and silicon nitride films are plagued with higher residual stress and not suitable in forming very thin diaphragms [3,10-12,31]. Surface micromachined capacitive transducers, have recently been shown to offer larger pressure sensitivity and lower temperature sensitivity than their piezoresistive counterparts. However, they also require a larger dia area, are more nonlinear, and demand sophisticated on-chip circuitry along with a somewhat more difficult process [14-16,19,32]. **A** very small parasitic in the signal conditioning circuitry can adversely affect the linearity of the sensor response [20,21]. Therefore, it requires close coupling to relatively carefully designed analog electronics to minimize the effects of the stray capacitances. Most of the surface micro-machined capacitive and resonant transducers use finger like structures formed from the 2pm thick polysilicon slab by removing the underneath sacrificial layers. It is quite impossible to deposit polysilicon films with small grain size more than 10μm thick. Particularly when the sensing axis is set along the plane of the chip. Thicker resonant structures are required as they will increase the active area and reduce the effect of fringing fields and thereby increase the capacitive sensing considerably. With polysilicon thicker resonant structures are quite impossible.

Merged Epitaxial Lateral Overgrowth (MELO) of silicon combined with laterally-undercut sacrificial layers has the potential to overcome these difficulties and open up possibilities for making ultra-miniature diaphragms and micro actuators. Particularly for fabricating single crystal silicon resonant structures MELO and SEG silicon are quite suitable. Using surface micromachining and MELO-silicon, resonant structures such as free standing beams with different thickness (from less than 1μm to greater than 10μm) can be fabricated. This new surface micromachined process is compatible with present day IC processing, since it uses conventional fabrication equipment, techniques, materials, and chemicals. Another advantage of this technique is that it can easily integrate micro-sensors and circuitry onto a single chip and thereby reduce power consumption and signal paths. Also the requirement for an extra back-side protecting plate for packaging, which is essential for bulk micromachined sensors, is eliminated.

Furthermore, a by product of using the MELO techniques will result in local silicon on insulator (SOI) structures on the same chip, which is an important technology for device isolation and for special devices. Successful implementation of this technique will introduce to today's micro-electronic industries the emergence of broader array of

solid state sensors and open the door for exploring the feasibility of applications of these new micro sensors/actuators into different areas.

6.2 Surface Micromachining

Top-side surface micro-machining is a rapidly developed technology which extends the range of micro-mechanical materials and structures which can be fabricated using planar a technology. Figure 6.1 illustrates the simple process of surface micromachining. The silicon substrate is first coated with an isolation layer, then a sacrificial layer is deposited on it. Windows are opened in the sacrificial layer and micro structural thin film is deposited and patterned by a proper etchant to define the diaphragm structures. The free standing micromechanical structure is formed by selectively etching out the sacrificial layer as illustrated in Figure 6.1(b).

This simple concept was first applied in the 1960s at Westinghouse Research Laboratories with metal films [22]. In the early 1980s, researchers at the University of California at Berkeley used polycrystalline silicon as the structural material and oxide as a sacrificial layer. Most of the related work was confined to study the mechanical properties of the LPCVD polysilicon [11]. Researchers at University of Wisconsin, Madison, in mid 1980s [23-25], have pioneered a method for making sealed cavities by depositing additional films over the free standing micromechanical structures. Thermal oxidation of the polysilicon and silicon substrate or CVD of oxide or nitride films are used for sealing the cavity as shown in Figure 6.2. Using this technique, a polysilicon micro-diaphragm of 125x125 μm^2 size with thickness varying from 1-4pm were realized by Guckel, et al.[23] in 1986.See Figure 6.3. They successfully fabricated a piezoresistive polysilicon pressure sensor using surface micromachining. At the same time Sugiyama, et al,[27] fabricated a micro-diaphragm pressure sensor with silicon nitride diaphragm of 80μm x 80μm using polysilicon piezoresistors, as illustrated in Figure 6.4.

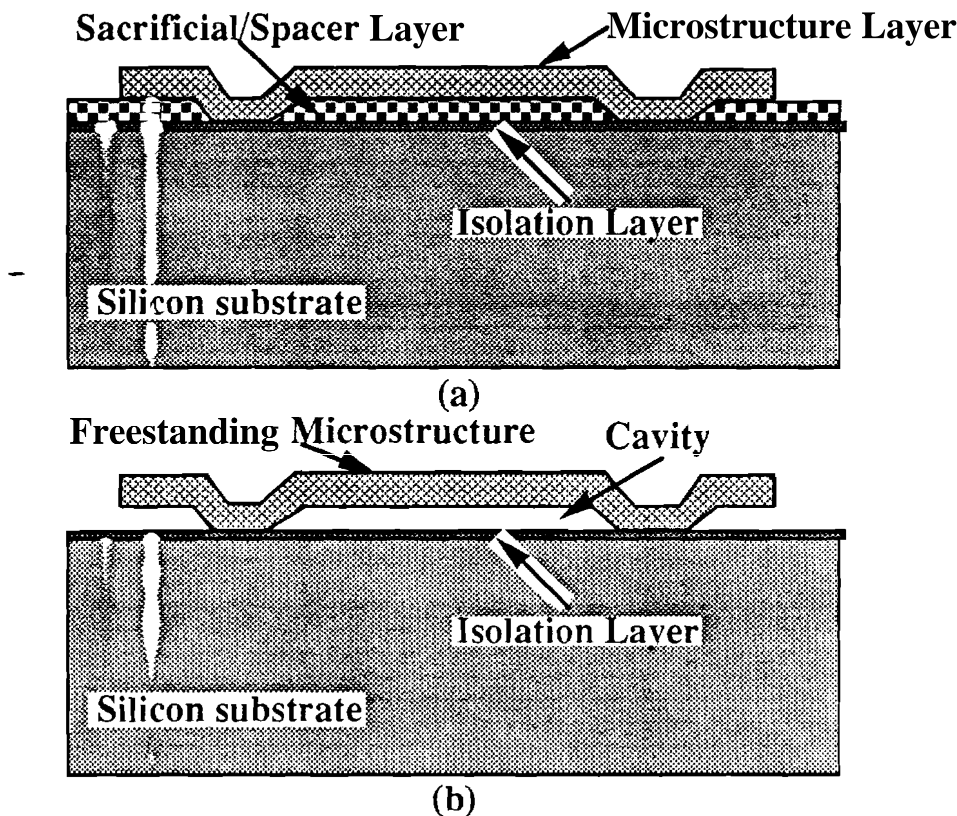


Figure 6.1 Surface microstructure fabrication process. (a) Patterning the sacrificial layer and depositing the microstructure layer. (b) Releasing the freestanding microstructure by etching out the underneath sacrificial layer.

Surface micromachined polysilicon pressure sensors using capacitive sensing has also been reported [17,32]. In addition to a nonlinear pressure response and the requirement of additional sophisticated signal sensing circuitry, the circuit noise for smaller diaphragms has severely limited the resolution of this type of transducers [21,26]. Hence, miniaturization using capacitive sensing has a serious problem, although they offer higher pressure sensitivities. Additional sensing circuitry also increases the size of the die. Particularly, most of the capacitive accelerometers are cantilever type which are more prone to off axis problems which produces unwanted response during operation. Very recently (1991) a highly symmetrical capacitive micro-accelerometer using bulk micromachining was reported to solve the off axis problem [28]. However this technique required a very large structure measuring 36mm x 3.6mm x 1.7mm and has a four layer

sandwich structure (glass/si/si/glass). Alignment of all four layer is an additional problem along with the already existing difficulties with bulk micromachining.

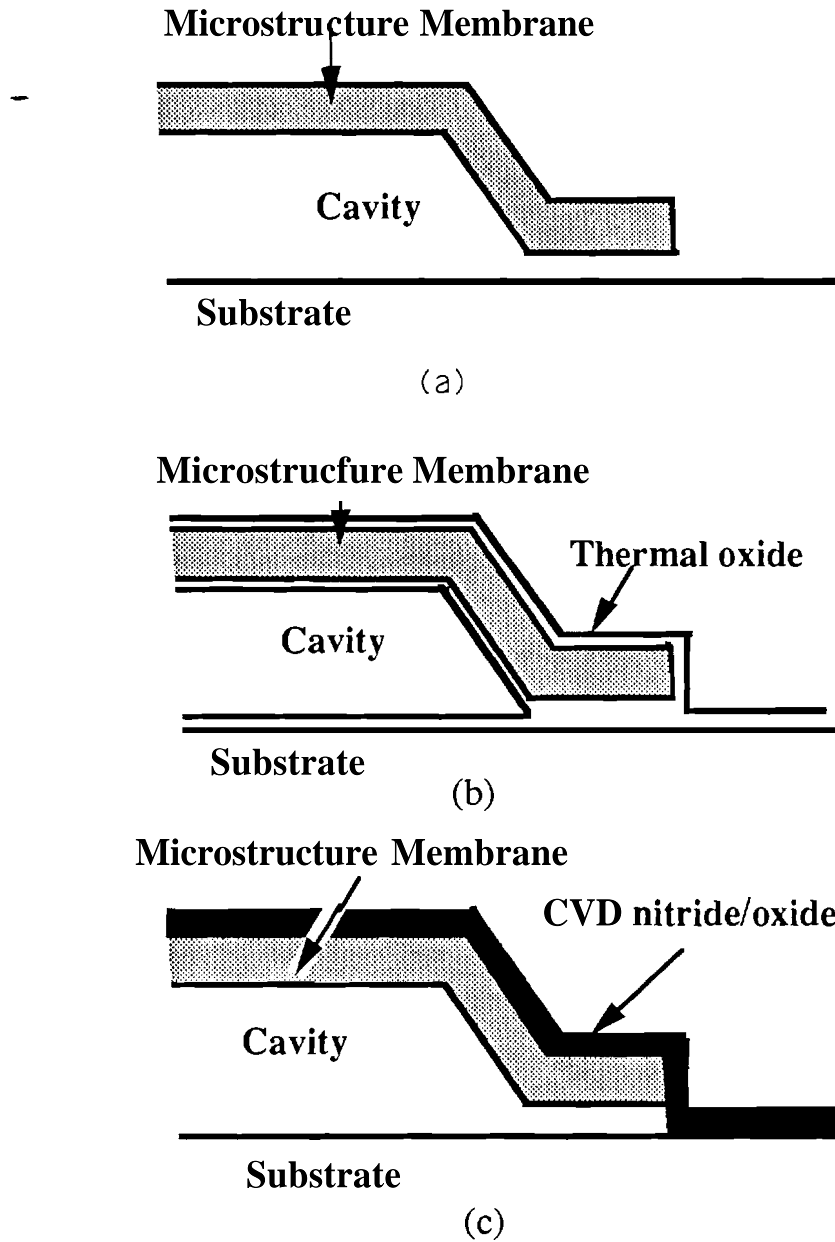


Figure 6.2 Sealing of the cavity. (a) The cavity (b) Reactive sealing (c) CVD sealing

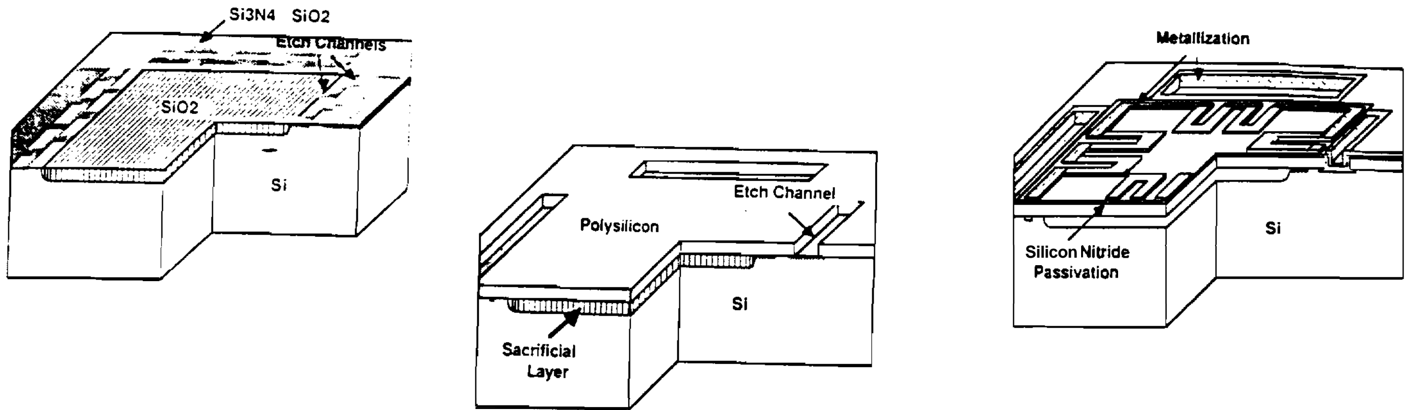


Figure *6.3* Surface micro-machined polysilicon pressure sensor [23].

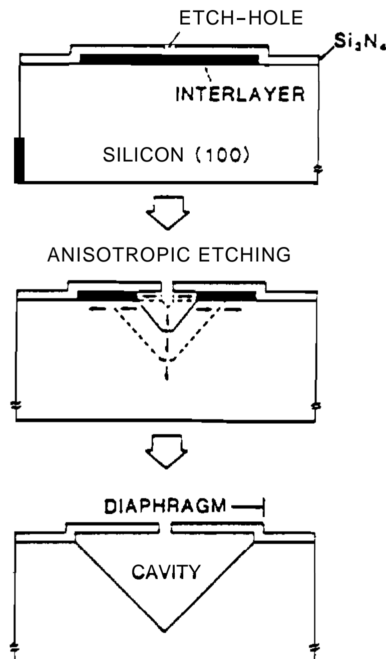


Figure 6.4 Surface micromachined pressure sensor using Nitride membrane [27].

The main advantage of surface micromachining is its ability to scale down the existing sensors by using completely planar single-sided processing, solely on the top surface of the silicon wafer. Using polysilicon or SiN_x as the structural material has put some limitations on miniaturization. The mechanical characteristics of thin-film microstructures critically depend on the average residual stress in the film and the stress variations in the direction of film growth or deposition. Both polysilicon and silicon nitride films are plagued with higher residual stress, and not suitable for making very thin diaphragms [3,10,31]. Thin membranes using polysilicon usually buckle due to the residual stress. Using annealing reported to be a cure for this problem, a fairly good mechanical material can be obtained after the stress relieving annealing cycle [24]. In addition to the residual stress, the doping concentration of piezoresisters on polysilicon are much higher ($10^{18}/cm^3$-$10^{20}/cm^3$). This high doping concentration reduces the piezoresistive coefficients, hence reduces the sensitivity as a whole [13,30]. Furthermore, electronic devices made in polysilicon show poor electronic properties. Therefore, a need of single crystal silicon based surface micro-machined process is a key for successful miniaturization of sensor technology.

Most recently (June 1991) Peterson, et al.[30] , from Nova Sensor has demonstrated the use of silicon fusion bonding to fabricate single crystal silicon membranes using surface micro-machining [Fig. 6.51. This technique shows much promise. However, the nonuniform membrane thickness control (>10 - 15%) introduced by doping and selective back etching possess a serious problem to this technique. Unless a better etch-stop technology evolves, making thin diaphragms repeatability with precise thickness control will be a major drawback of this fabrication system.

Engineers at Analog Devices [32] has introduced a force-balance surface micromachined accelerometer chip which claimed to offer many advantages over conventional accelerometers [Fig.6.6]. The sensor consists of a variable, differential, air capacitor whose plates are cut (etched) through one, 2pm thick slab of polysilicon. The fixed capacitor plates, Y and Z, are simple cantilever beams supported 1µm above the chip, in the free space by polysilicon anchors as shown in Figure 6.6 (b). The accelerometer's proof mass consists of 50-odd polysilicon fingers [X plates in Fig. 6.6(a)] which form the movable plate of the variable capacitor [Fig. 6.6(c)]. The two plates of fixed capacitor plates (Ys and Zs) are electrically connected in parallel within the chip. This forms a pair of independent capacitors, X-Y and X-Z, with the moving plate X consisting of all of the fingers extending from the proof mass. Here the X moving fingers

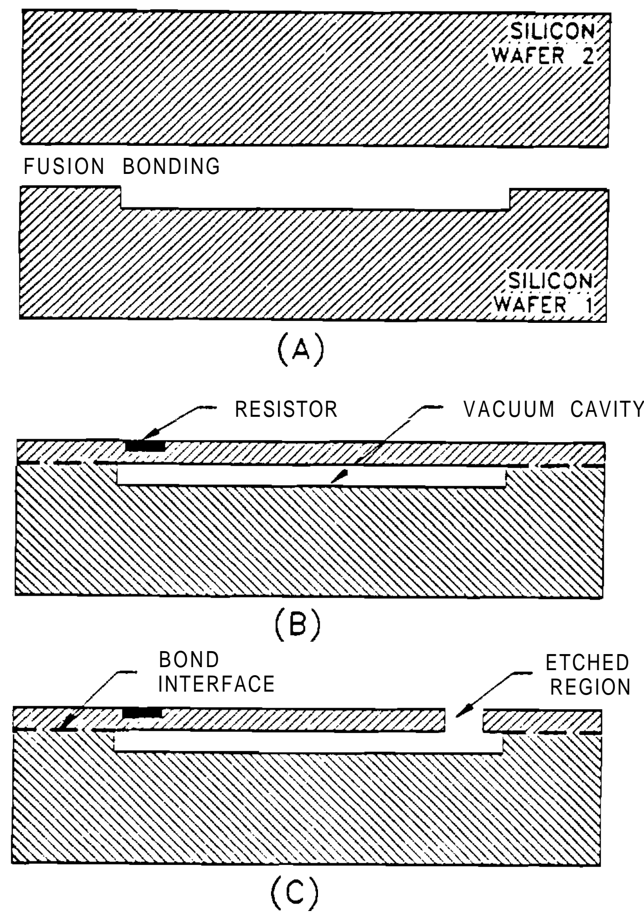


Figure 6.5 Surface micro-machining using Silicon Fusion Bonding [30].

moves along the plane of the chip with acceleration. As these plates move the distance between X-Y and X-Z plates changes and produces a differential capacitor output. In a open loop operation the differential output voltage due to the change of capacitance is feed into a buffer amplifier, which drives a phase-sensitive demodulator. The demodulator contains a low-pass filter and provides a low-frequency analog voltage representing the signature of the acceleration. The air bag system digitizes the signature, and applies to a special-purpose digital signal processor circuits, which makes the decision to deploy. In the closed loop version, the dc voltage at the output of the preamplifier is applied to the moving capacitor plates via a feedback path. It creates an electrostatic force between the fixed and moving plates that opposes the inertial force of the mass and restores the the mass to the neutral position. The preamplifier output signal is thus a direct function of the inertial force, and therefore of the acceleration. Figure 6.7 shows a photograph of the top view of the complete accelerometer chip. Although this technique offers promise, the

actual sensing of the acceleration requires an extensive amount of high quality precise on-chip active signal-conditioning circuitry. Also the Y and Z fixed plates are cantilever type beams. Hence off axis stimulation will result in unwanted sensor output. Since the capacitor plates are made of polysilicon membranes they can buckle due to intrinsic residual stress in these thin films and effect the yield adversely. Furthermore, introduction to any noise in the circuit will severely limit its performance. Also due to the extensive amount of on chip circuitry, the die area became relatively large (3mm x 3mm), which in fact is larger than some of the existing bulk micro-machined devices.

Polysilicon resonant structures such as free standing beams are fabricated and used to estimate the mechanical properties of the material including the strain in the deposited film [34]. But non repeatability of polysilicon deposition process and poor electrical device performance in polysilicon hinders its widespread use. A need for single crystal silicon micro-mechanical structures in the sensor technology still prevails. Therefore, a surface micromachined single-crystal silicon process using MELO has the potential to open the door for broader array of solid state sensors.

±50-g IC ACCELEROMETER
WITH SIGNAL ONDITIONING

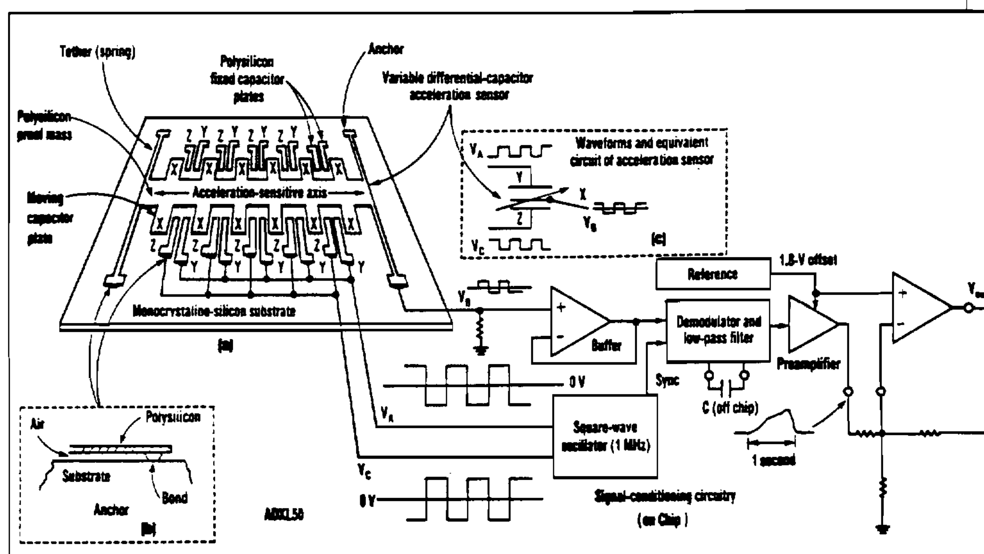


Figure *6.6* Schematic of the Analog Devices' IC accelerometer [32]. (a) Surface rnicromachined variable capacitor module. (b) The Y and Z fixed capacitor plates. (c) The differential output scheme.

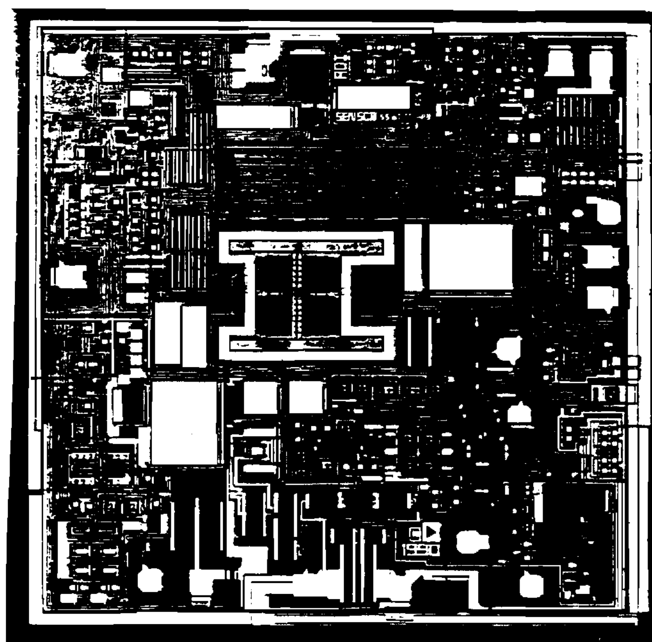


Figure 6.7 Top view of the Analog Devices' accelerometer die [32].

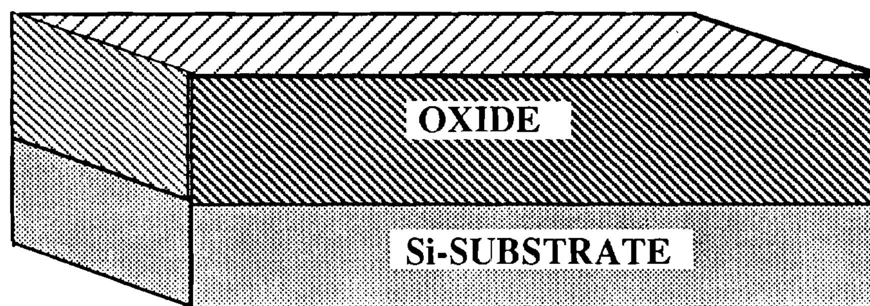
6.3 Single Crystal Silicon Cantilever Beams

Two different techniques for fabricating surface micromachined single crystal silicon cantilever beams will be presented below. The first technique is suitable for fabricating thin, very wide but short beams. A second technique will be presented that is very versatile and very suitable for fabricating thin or thick, narrow but extremely long free standing single crystal silicon beams.

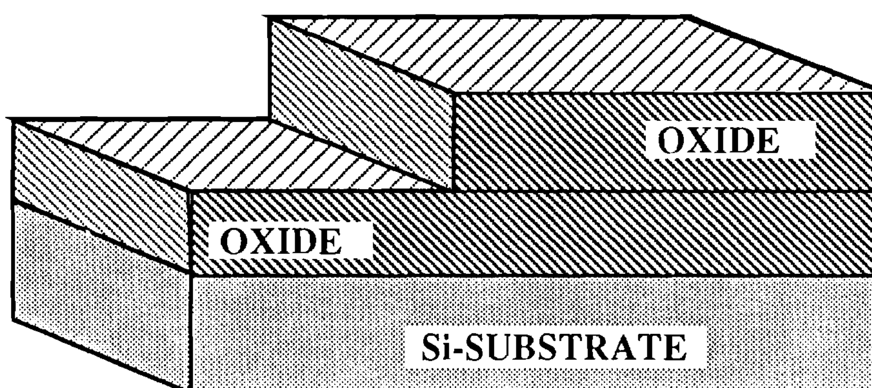
6.3.1 First Technique :Fabrication of Thin but Short and Wide Cantilever Beams

The process sequence for fabricating the thin single crystal silicon cantilever beams using surface micromachining is illustrated in Figure 6.8. Starting with n-type Si substrate, a thick oxide was grown and patterned to produce an oxide step [Figure 6.8(a)]. Then using another mask, patterns were defined on the thicker oxide and the oxide was etched to define beam thickness [Figure 6.8(b)]. Notice the remaining oxide between the adjacent beams, which will act as the etch-stop oxide during the later Chemical Mechanical Polishing (CMP).

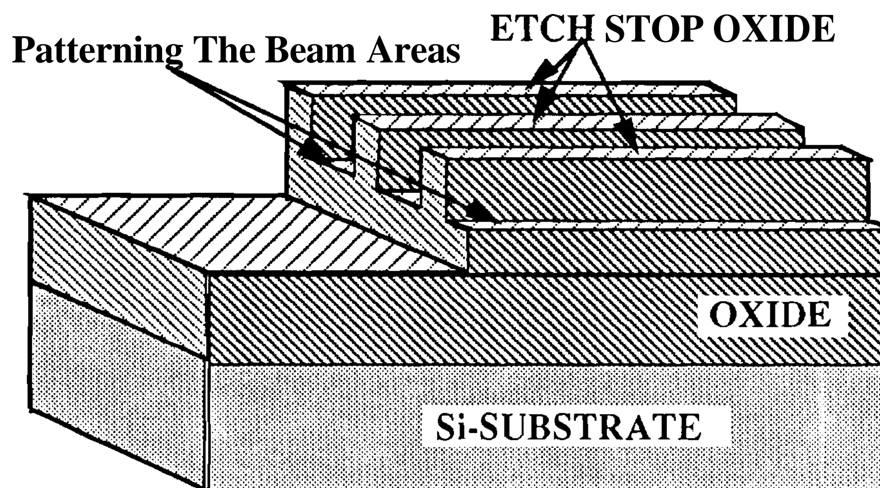
In the next step the SEG/ELO seed hole was patterned using another mask as shown in Figure 6.8(c). Now selective epitaxially grown silicon is grown from the seed hole and allowed to fill in the cavities in the etch-stop oxide [Figure 6.8(d)]. Using Chemical Mechanical Polishing (CMP) and the etch-stop oxide the thickness of the beams are defined as shown in Figure 6.8(e). Finally, the etching of the sacrificial oxide layer by HF results in the thin single crystal silicon free-standing cantilever beams [Figure 6.8(f)].The length of the beam is limited by the amount of ELO. However the thickness and width have few limits, mainly photolithography and oxide etching.



(a) Thermal oxidation of the Substrate

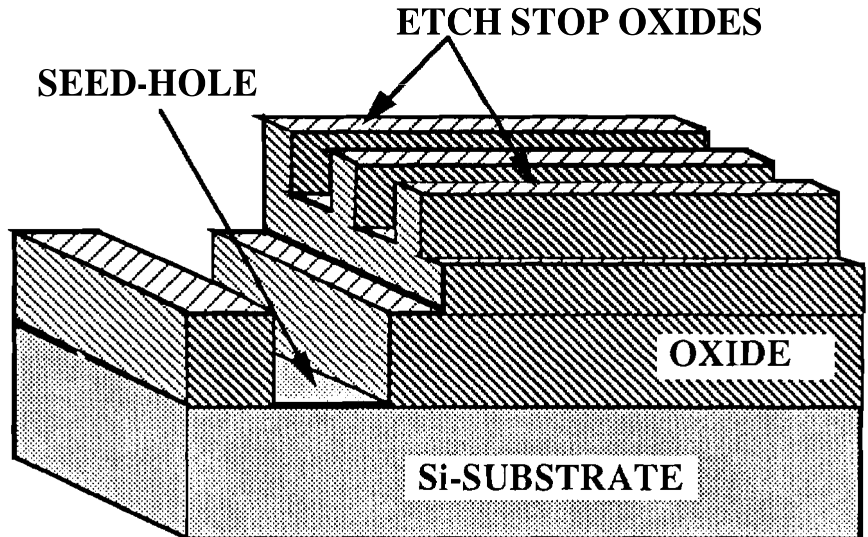


(b) Mesa Etch to form step in oxide

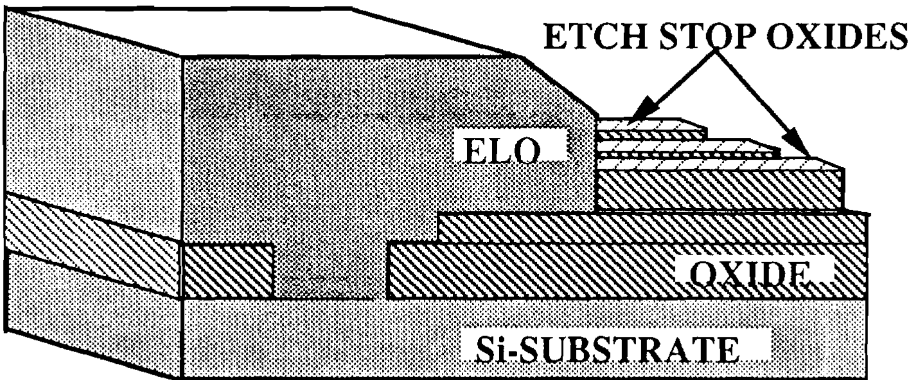


(c) Delineation of beam thickness

Figure 6.8 Process flow of thin but short and wide cantilever beam fabrication.

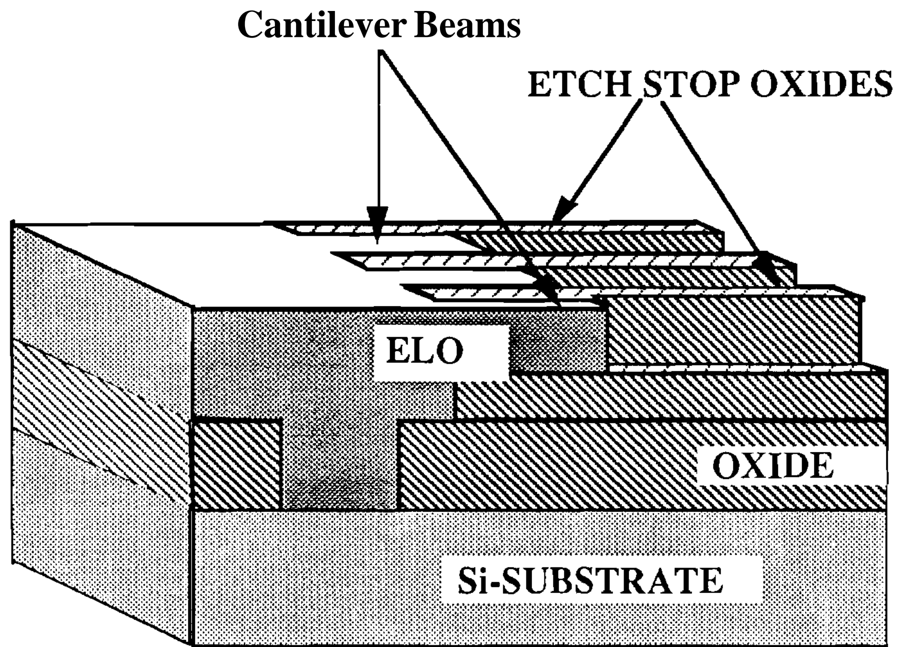


(d) Seed Hole patterning

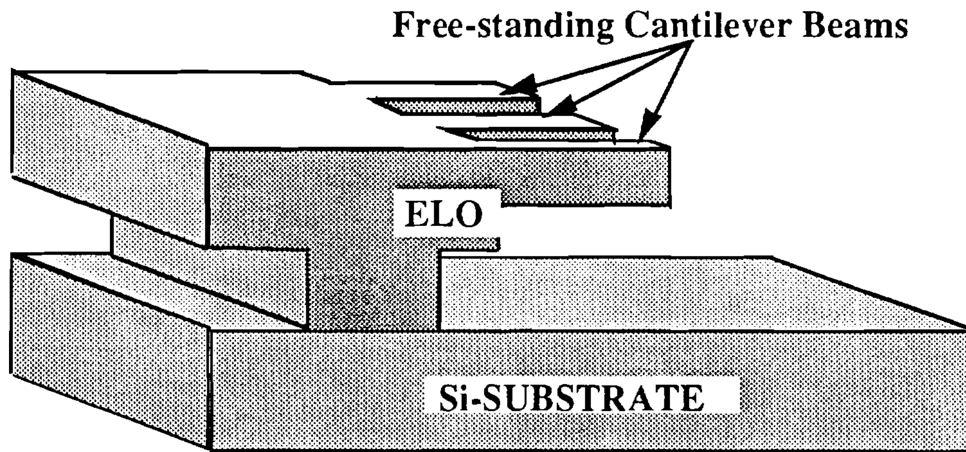


(e) Epi Growth: Cavities are filled with single crystal Silicon

Figure 6.8 Process flow contd.



(f) Chemical Mechanical Polishing and formation of Thin Beams

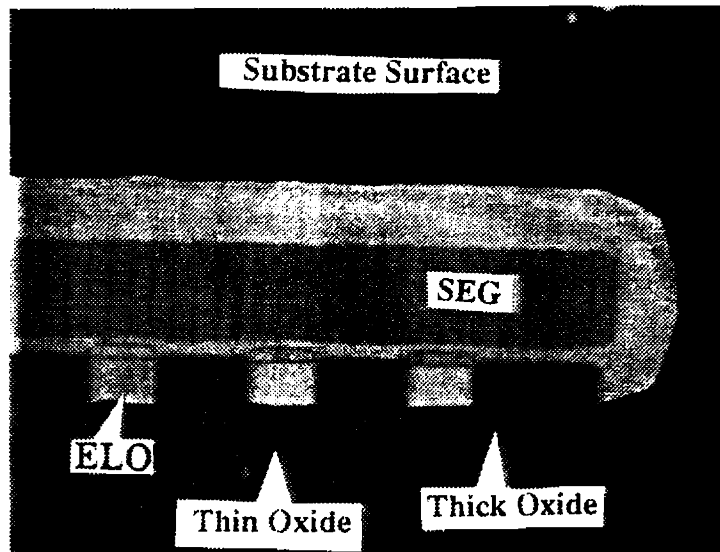


(g) Formation of Free Standing Cantilever Beams.

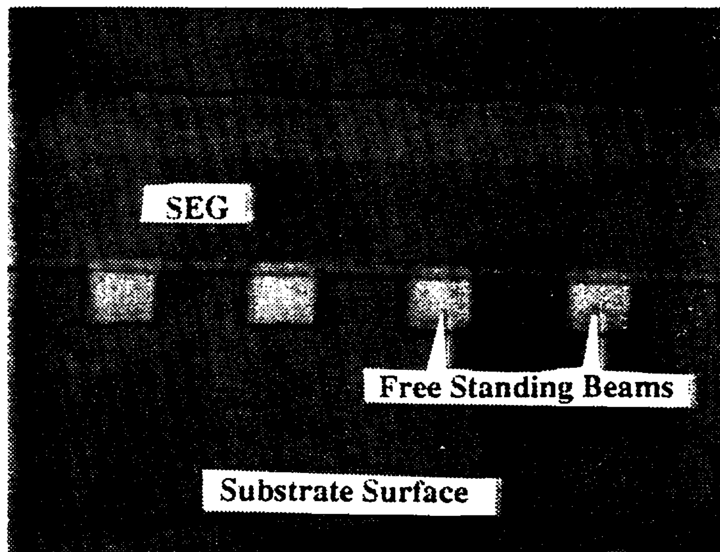
Figure 6.8 Process flow contd.

6.3.2 Results :

Using the above technique, 0.5μm thick, 8μm long and 12 micron wide single crystal silicon cantilever beams have been successfully fabricated. The clearance of the beams with the substrate was 0.7μm. Figure 6.9(a) shows the photograph of the top view of the beams after CMP. It clearly shows the single-crystal silicon is preserved in the cavities between the etch-stop oxides. Figure 6.9(b) shows the photograph of the free standing cantilever beams after the underneath sacrificial and the etch-stop field oxides are removed by etching in HF for 10 minutes. Figure 6.10(a) shows the SEM photograph of the beams after the sacrificial layer etch. **A** closer view of the SEM photograph in Figure 6.10(b) shows the free standing 0.5μm thick cantilever beam.

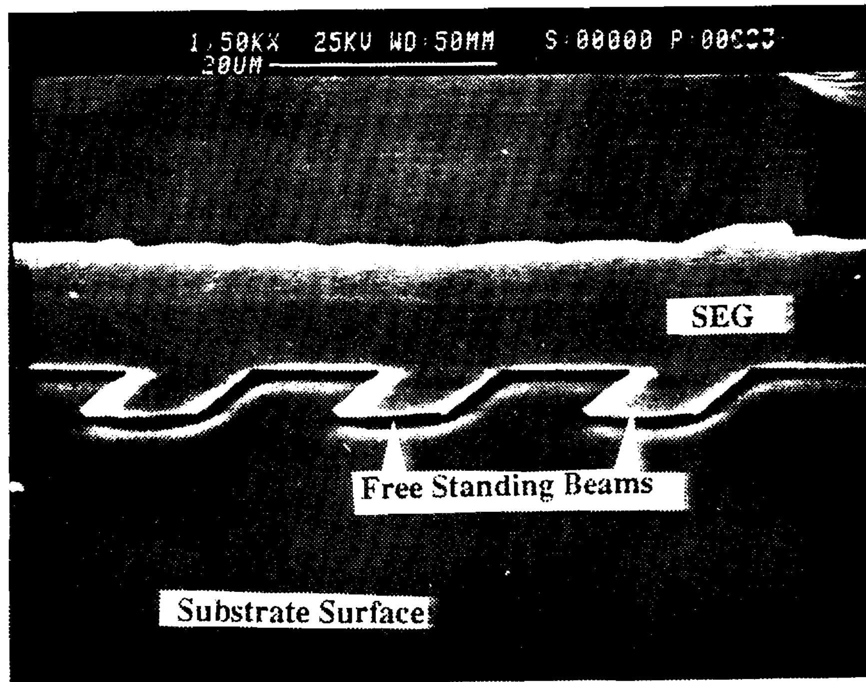


(a)

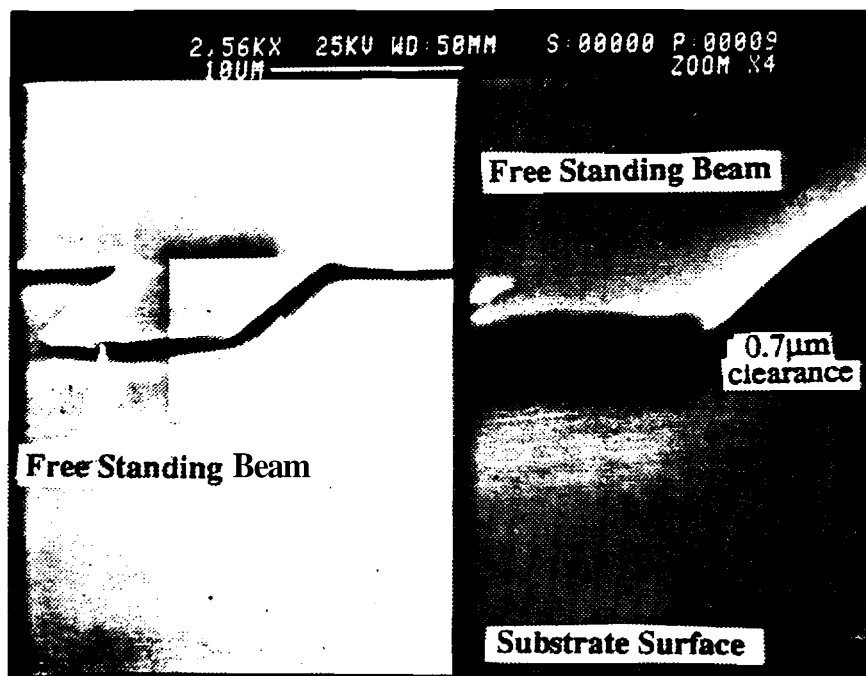


(b)

Figure 6.9 (a) Photograph showing the top view of the single crystal silicon beams after CMP (b) Photograph showing the Free Standing Cantilever Beams



(a)



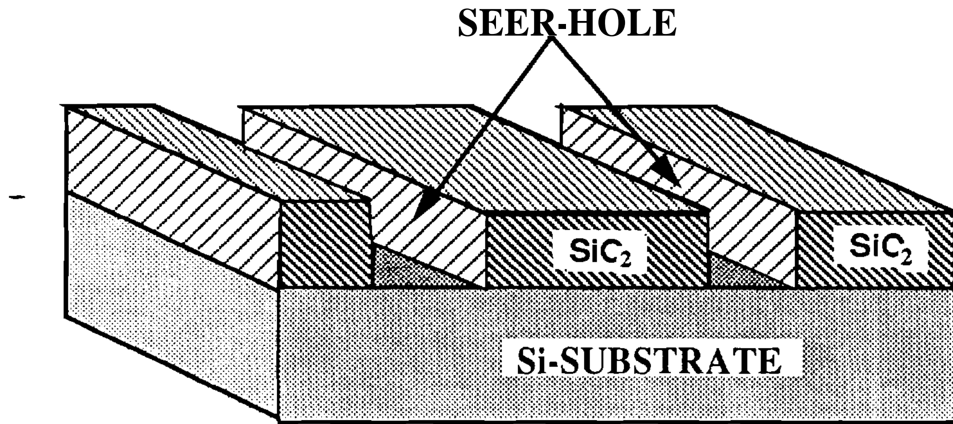
(b)

Figure 6.10 SEM Photographs (a) Showing The Free Standing Single Crystal Silicon Cantilever Beams (b) A more closer view of the Beam.

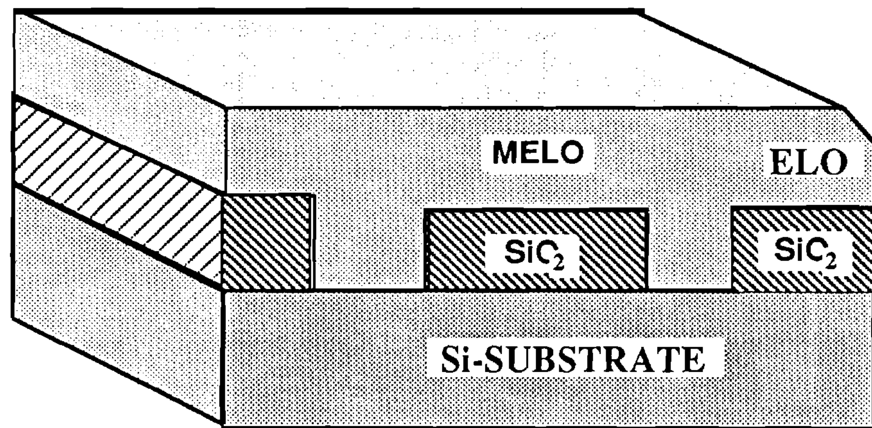
6.3.3 Second Technique : Fabrication of Long-Narrow Cantilever Beams

The process sequence for fabricating single crystal silicon resonant structures using surface micromachining is illustrated in Figure 6.11. Starting with n-type silicon substrate, a thick oxide was grown and patterned to open the seed holes as shown in Figure 6.11(a). Then selective epitaxially grown silicon, from the seed holes, is allowed to merge in the middle of the oxide island. [Fig 6.11(b)]. Using a thick photoresist (AZ4620) as a masking material, a pattern was defined photolithographically and reactive ion etching was used to etch out the silicon from the seed holes to define the beam as shown in Figure 6.11(c). After removing the photoresist and etching the sacrificial oxide layer with HF or BHF results in free standing single crystal silicon cantilever beams as shown in Figure 6.11(d). They can be of any length. However, the width is limited by the amount of ELO material; as is the thickness.

The process sequence for fabricating thin but long cantilever beams is shown in Figure 6.12. The first two processing steps are common in both processes. After growing the MELO-silicon [Fig 6.11(b)] a layer of CVD polysilicon was deposited as shown in Figure 6.12(a). Now a very thin LPCVD nimde layer is deposited on top of the poly-layer [Fig. 6.12(b)] which will work as an etch stop during chemical mechanical polishing. The combined thickness of this nitride and the poly-layer will define the thickness of the beam. Using Chemical Mechanical Polishing (CMP) and the etch-stop nitride, the thickness of the beams is defined as shown in Figure 6.12(c). A second mask is used to photolithographically enable RIE etching of the silicon from the seed holes and hence define the beam width as shown in Figure 6.12(d). Finally, the etching of the sacrificial oxide layer with HF or BHF resulted in the thin single crystal silicon free-standing cantilever beams as shown in Figure 6.12(e). Notice that the whole process sequence for fabricating thin or thick single-crystal silicon resonant structures of any length, only requires two masking steps; one for seed hole openings and other for RIE etch window openings.

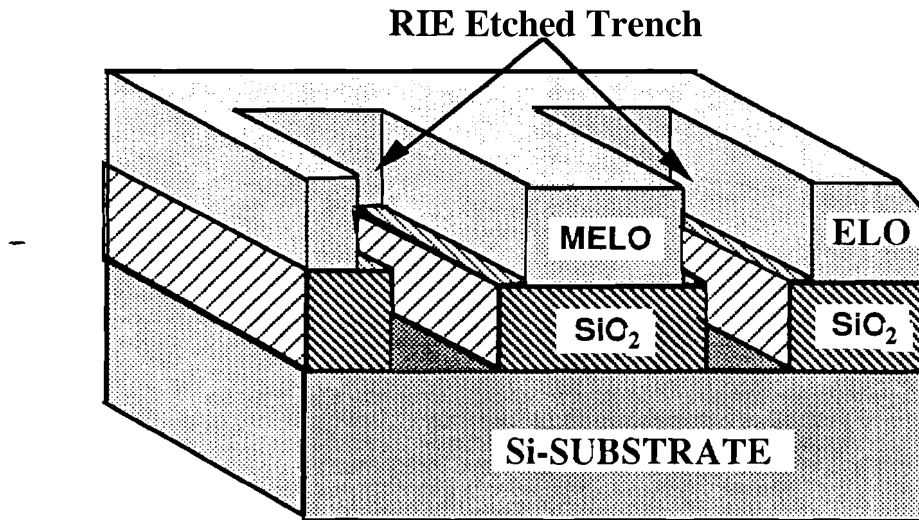


(a) Seed Hole patterning

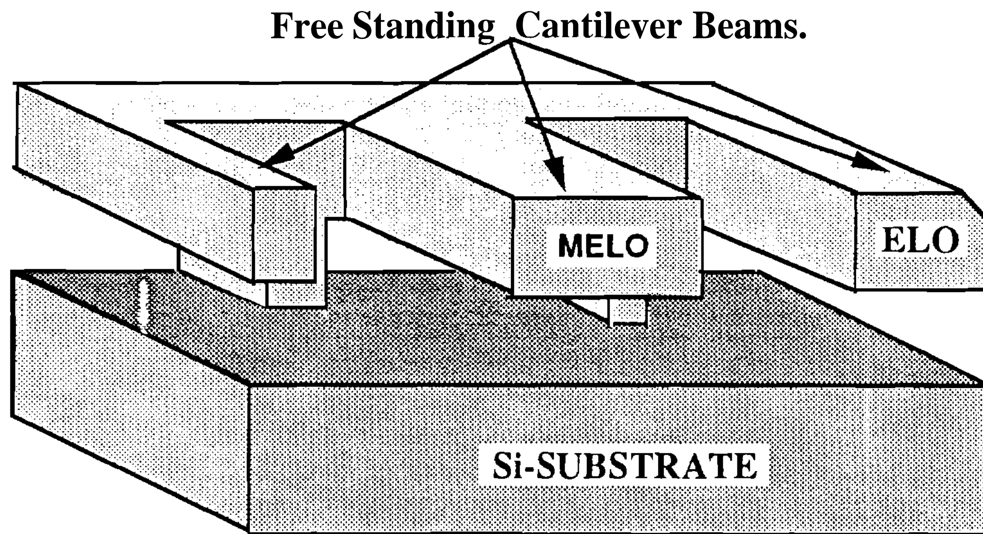


(b) Epi Growth: Formation of ELO and MELO-Silicon

Figure 6.11 Process Flow of Thick but Long-Narrow Cantilever Beam Fabrication.

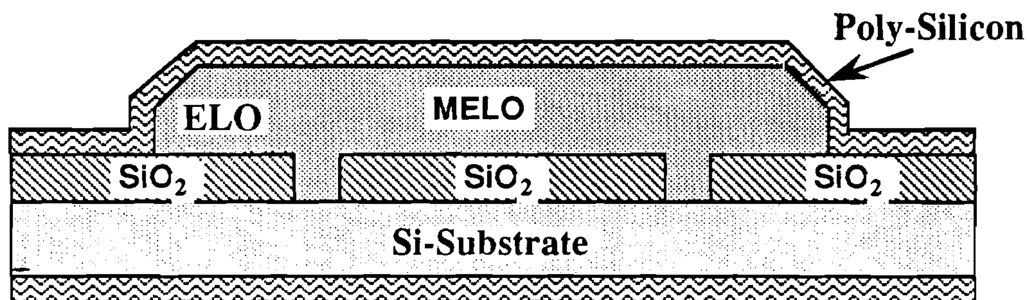


(c) Delineation of beams by RIE

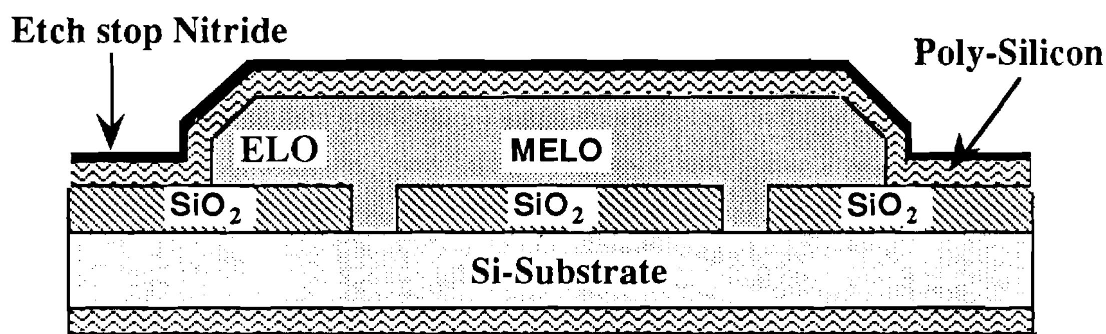


(d) Formation of Free Standing Thick but Long-Narrow Cantilever Beams.

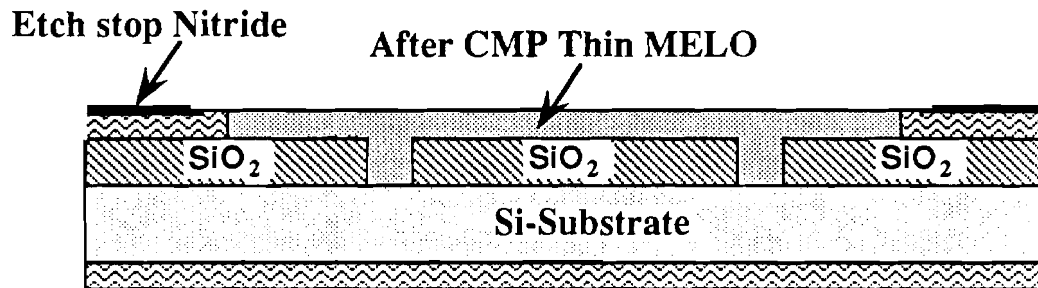
Figure 6.11 Process flow contd.



(a) Deposition of Poly-Silicon layer on MELO-silicon

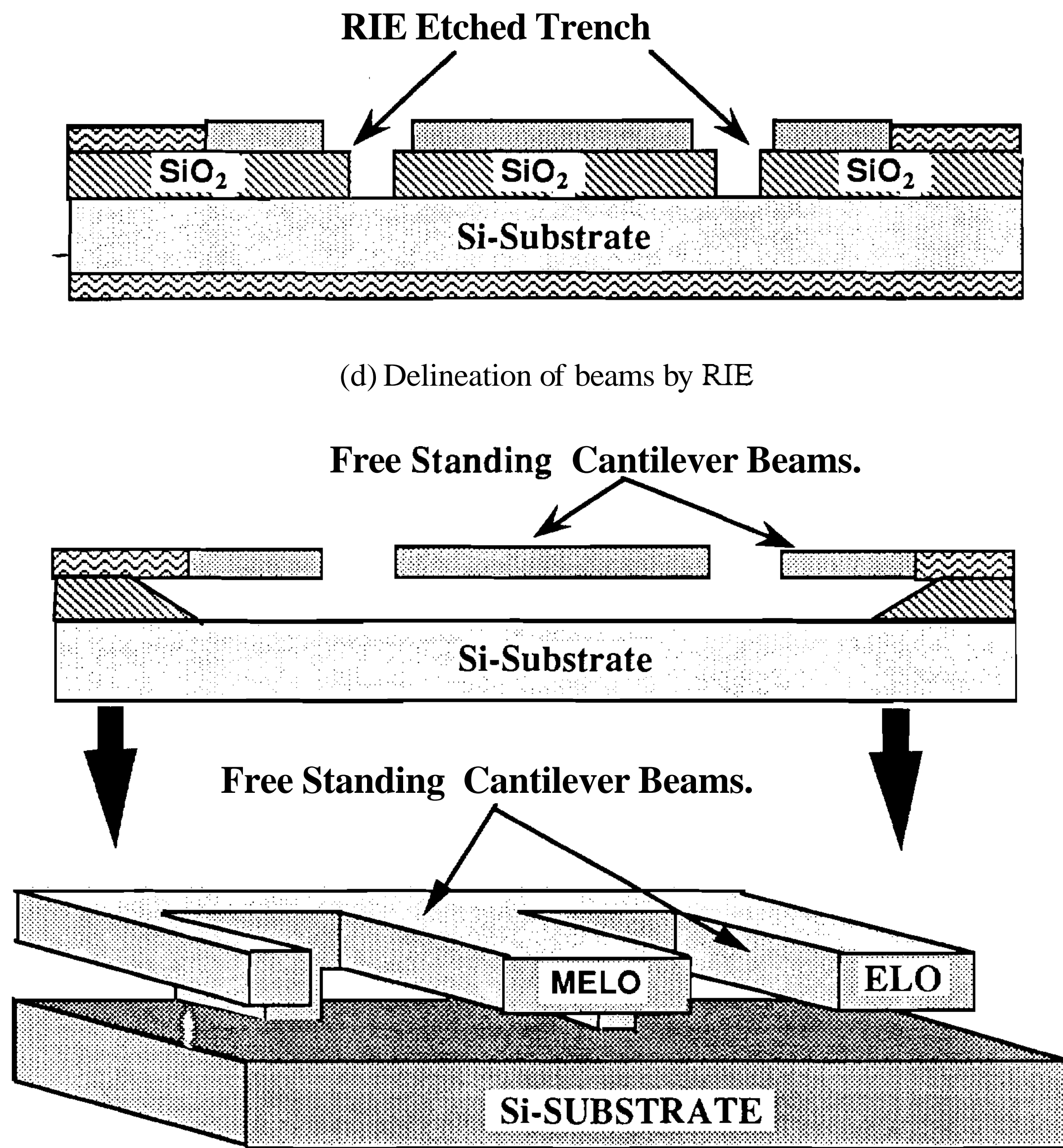


(b) Deposition of Etch Stop CVD Nimde



(c) Chemical Mechanical Polishing and formation of Thin Si Membranes

Figure 6.12 Process Flow for Thin but Long-Narrow Single Crystal Silicon Cantilever Beams



(d) Delineation of beams by RIE

(e) Formation of Free Standing Thin Cantilever Beams.

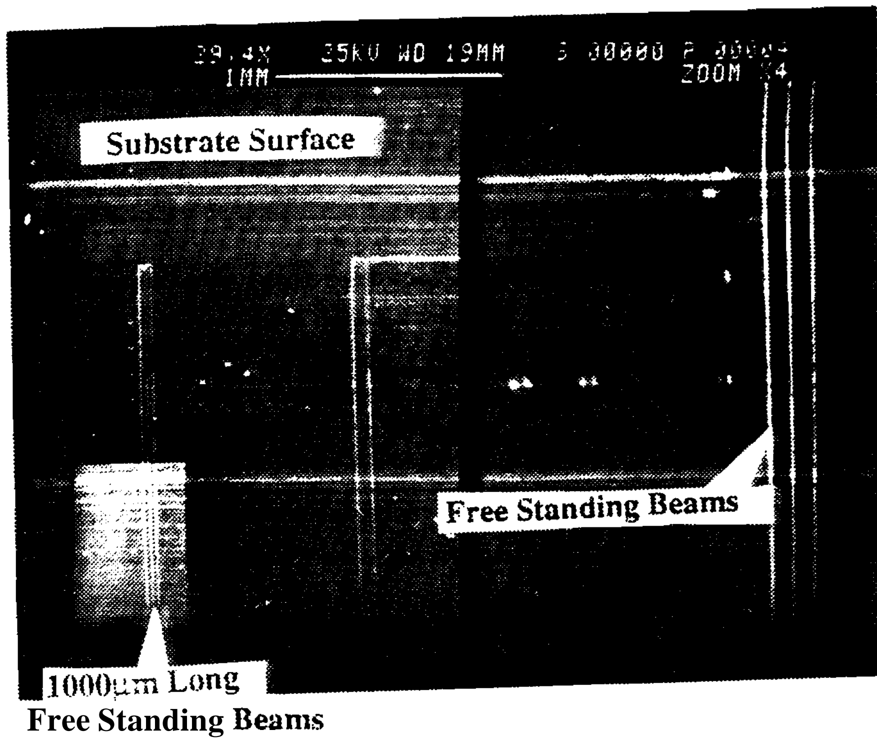
Figure 6.12 Process flow contd.

6.3.4 Results :

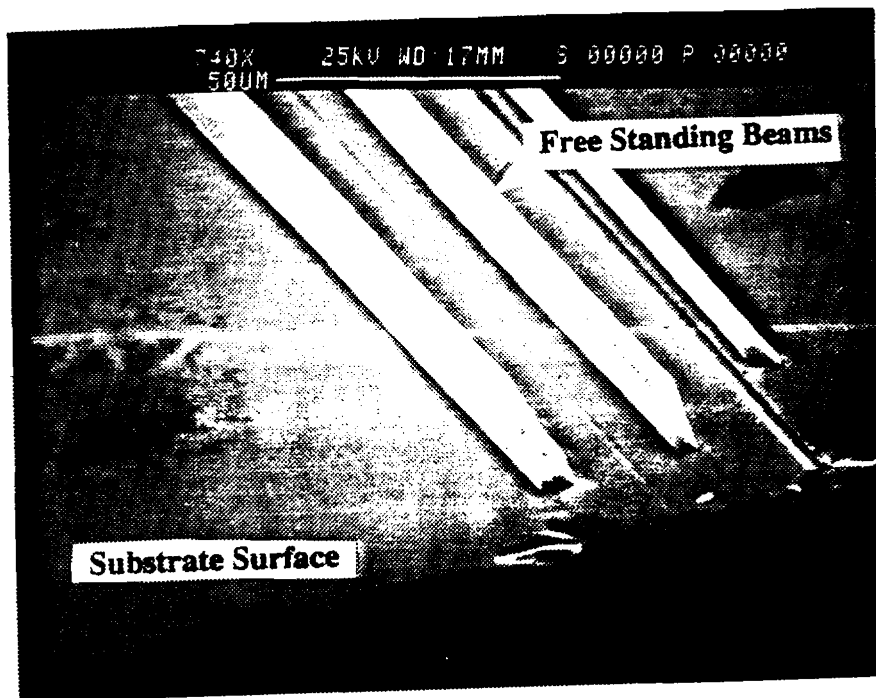
Using the above technique, 10μm thick, 1000μm long and 5pm wide single crystal silicon cantilever beams have been successfully fabricated. The clearance of the beams with the substrate was 1.2μm. The sacrificial layer was etched in BHF wet etch and rinsed in DI water and methanol. Figure 6.13(a) shows the SEM photograph of the beams after the sacrificial layer etch. A closer view is shown in the SEM photograph in Figure 6.13(b), which clearly shows the tips of the free standing cantilever beam. The beam ends are irregular due to purposely fracturing the wafer to get the cross sectional view in the SEM photograph.

6.3.5 Mask layout for other resonant structures

A test mask set for fabricating different resonant structures is presently underway. This mask is designed to study the built-in stresses or strains in the single crystal silicon free standing structures. Usually internal stresses are originated due to the thermal mismatch between different materials with varied thermal expansion coefficients. To evaluate the compressive strain fields, the doubly supported beam structures shown in Figure 6.14 are used. The beams can either be connected or isolated from the substrate as shown in Figure 6.14(a) and (b). To estimate the tensile strain fields free standing cantilever with or without the merge seam are considered as shown in Figure 6.15(a) and (b). Also a ring and square structures are considered for estimating the tensile strain fields [Figure 6.16(a) and (b)]. Table 6.1 lists some of the variation of different dimensions of the above mentioned structures in the layout. Both capacitive and piezoresistive sensing modes were considered for estimating the resonant frequency of the beams.

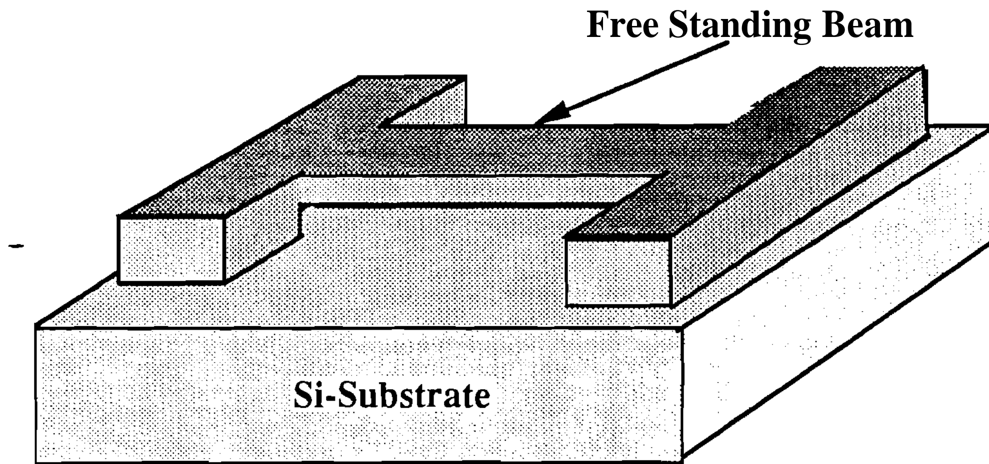


(a)

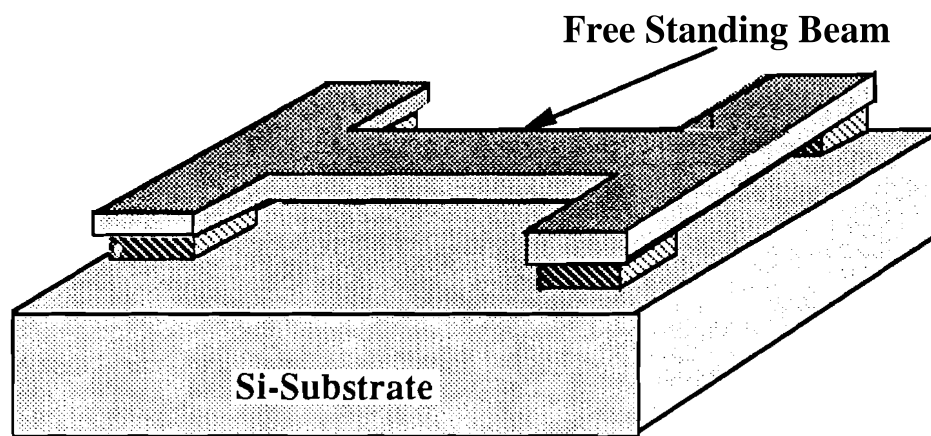


(b)

Figure 6.13 SEM Photographs (a) Free standing Single Crystal Silicon Cantilever Beams (b) A closer view at the Tip of the Beams

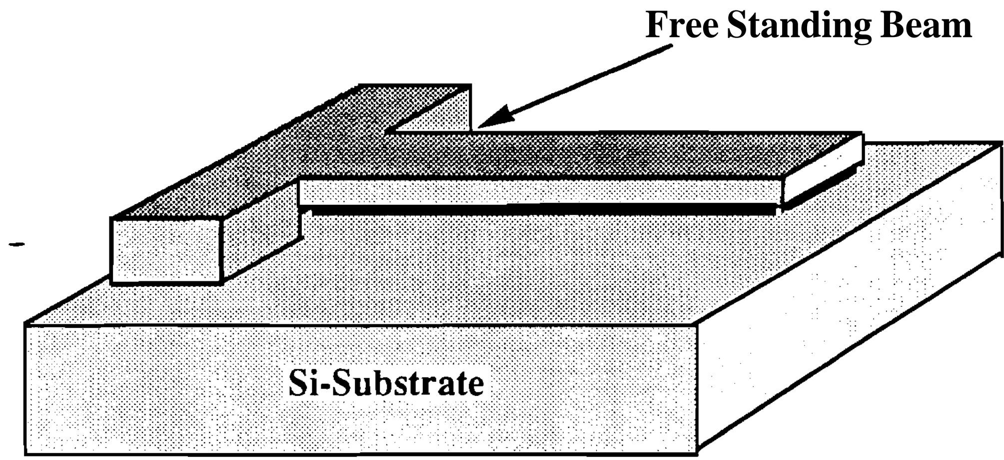


(a)

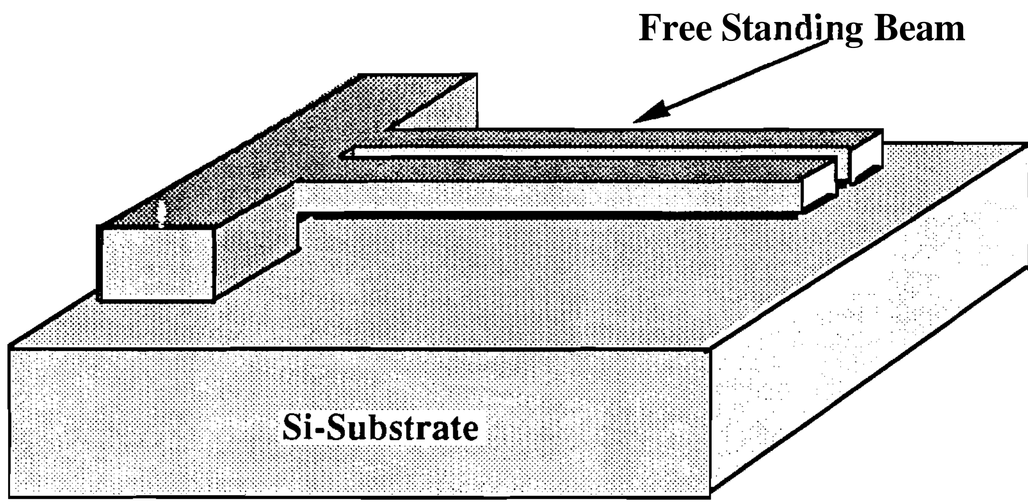


(b)

Figure 6.14 Free standing doubly supported beams (a) Beams are connected to the substrate (b) Beams are isolated from the substrate.

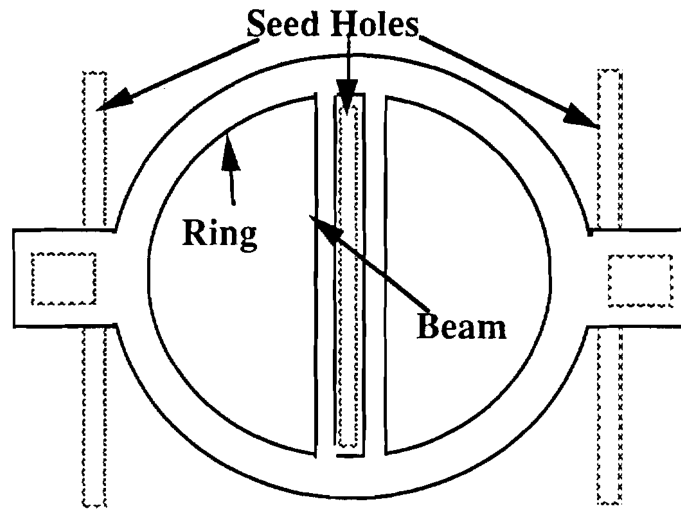


(a)

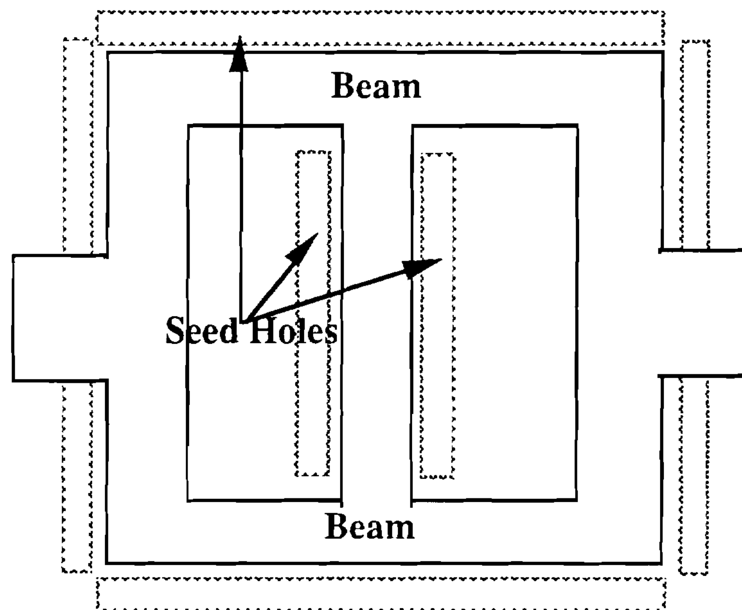


(b)

Figure 6.15 Free standing single crystal silicon Cantilever beams. (a) Merged seam included in the beam (b) Without the merged seam.



(a)



(b)

Figure 6.16 Tensile stress realizing structures (a) Ring Structure (b) Square Structure.

Table 6.1 :Variation of Dimensions in The Mask Layout

Beam Structures :		
Length 10 to 100μm--- 20μm Step 100 to 500μm--- 50μm Step 500 to 1000μm--- 100μm Step	**Width** 2μm to 20μm	**Thickness** <1μm to >10μm
Separation of Electrode From Beam : 2μm to 10μm		
Ring Structures :	Inner Radius 5μm to 15μm Ring width 5 to 10μm	
Square Structures :	Length-- 50 to 500μm in 50 μm Steps Width-- 2 to 20μm	

6.4 Electrical Properties of MELO-Silicon

Diodes were the primary measuring tool used for MELO material characterizations. The slope of the forward bias curve determines the junction ideality factor, η. This easily measured device parameter (η) is a practical barometer of crystal quality. Eta (η) is numerically about equal to 2.0 in poor material, and approaches unity (1.0) in high-quality material. Also reverse leakage currents (both at room temperature and at 115°C) are measured to estimate the leakage through the junctions.

Figure 6.17 shows the cross sectional diagram of the diodes fabricated on the three different types of material, namely SEG, MELO and the substrate silicon. The SEG, MELO and substrate diodes were fabricated in the same process on the same die in order to make a reasonable comparison of their performances.

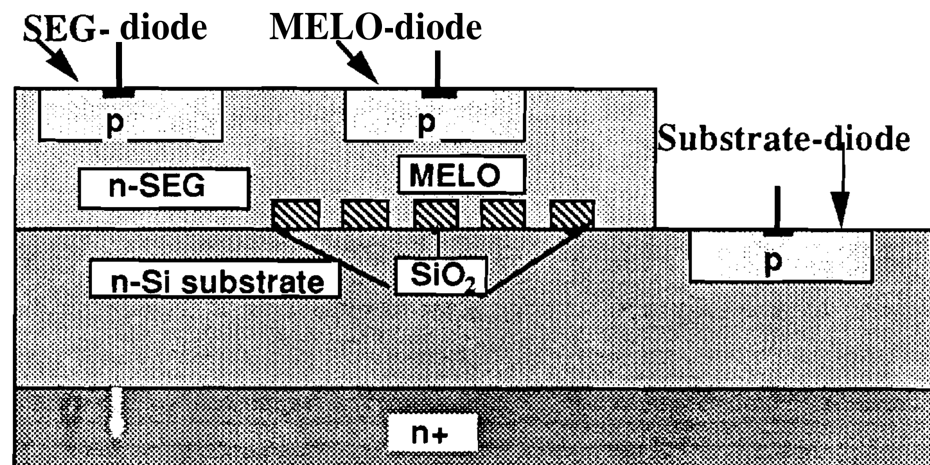


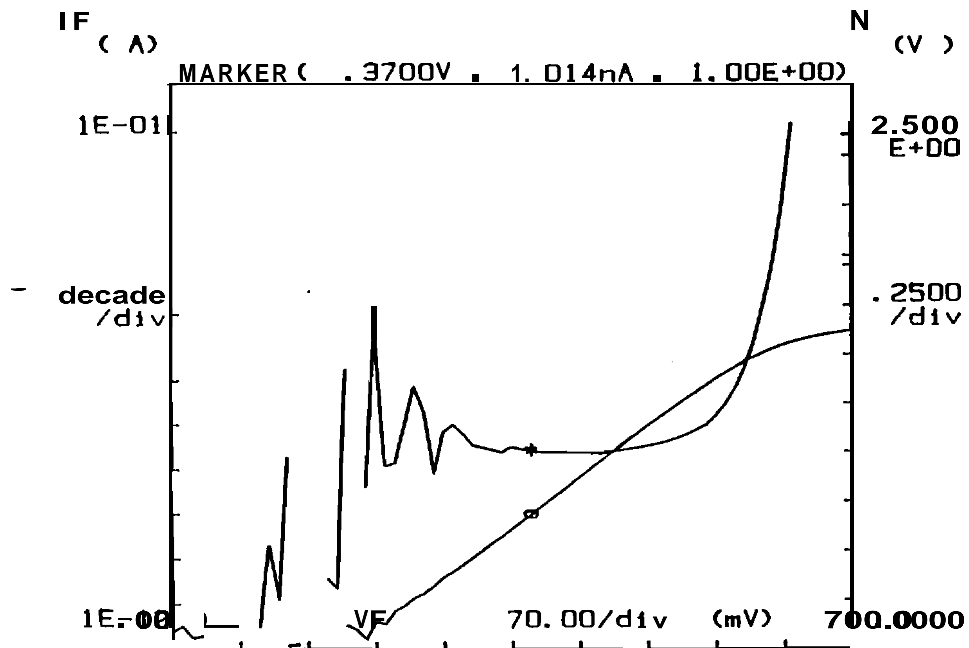
Figure 6.17 Cross-sectional diagram of three different diodes.

In addition to normal diode fabrication processing steps, two extra steps prior to the diode fabrication were introduced. The first additional processing step was a 2 min. Chemical Mechanical Polishing of the MELO. This polishing step removed any non uniformity on the surface of the MELO-film due to merging facets. Then, the wafer was annealed in a oxidation environment for 45 min. at 1100°C and the oxide grew from this step was completely removed by BHF etching. A second oxide (–2500 Å) was grown at 1000°C and the normal diode processing steps were carried out on this oxidized wafer. For the p type junction boron was implanted at the dose of $3x10^{13}/cm^2$ at 27 kev and a 21 min. drive-in step at 950°C in oxidation environment was performed. Arsenic was implanted at the dose of $2x10^{15}/cm^2$ at 25 kev for the back-side contact.

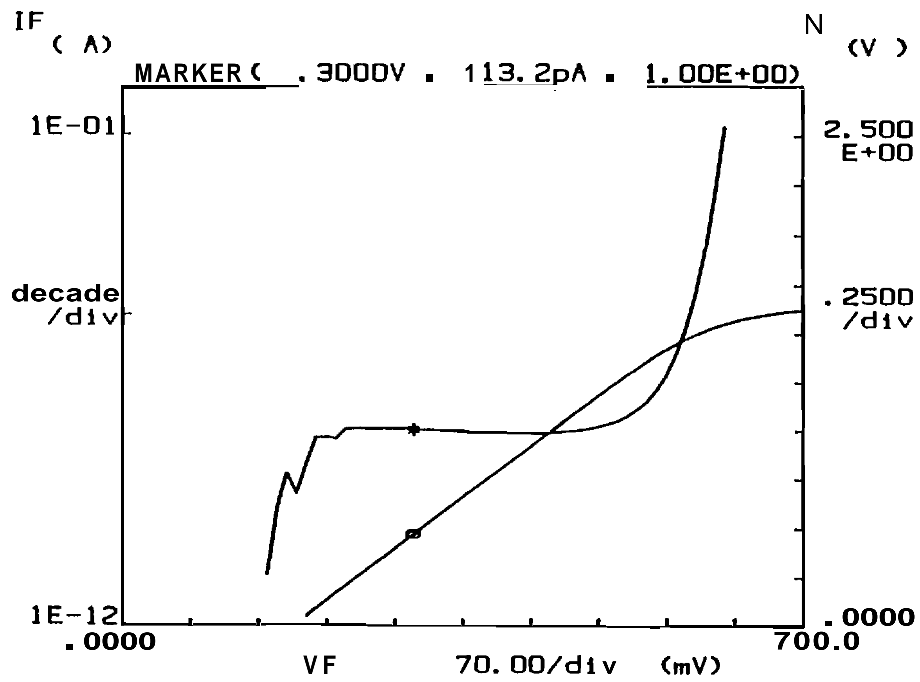
Figure 6.18 shows the forward bias characteristics of the diodes fabricated on SEG, MELO, and substrate silicon. In all devices the ideal regions (where η = 1.00) were measured over four to five decades of diode current which indicates excellent quality of the materials. Table 6.2 lists the average ideality factor of the 20 different measurements. The ideality factor for MELO diodes varied from 1.00 to 1.04 in all 20 devices and all of them have the ideal region spread over more then four to five decades of diode current. The similarity between MELO, SEG and substrate values indicates excellent quality in the MELO and SEG materials.

Table 6.2 : Ideality factor of different diodes

	Substrate-Diode	SEG-Diode	MELO-Diode
Ideality Factor η (avg. of 20 devices)	1.01	1.01	1.013

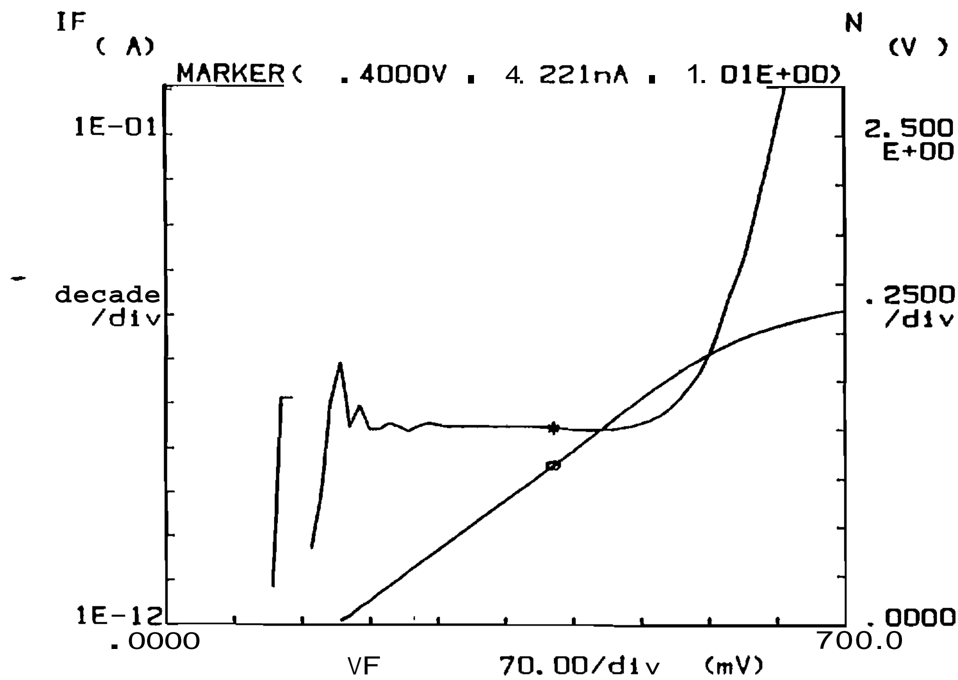


(a) Substrate Diode



(b) SEG Diode

Figure 6.18 Forward bias characteristics of the diodes.



(c) MELO Diode

Figure 6.18 Forward bias characteristics of the diodes contd.

To estimate the leakage through the diodes on MELO, reverse leakage current was measured both at room temperature and at 115°C. Table 6.3 lists the average of the leakage current density of 10 different measurements. These results show very low leakage current through the junction which indicates excellent quality of the MELO silicon. Figure 6.19 shows the breakdown characteristic of the MELO diodes, which shows breakdown characteristics.

Although there exists some defects in the merged seam, the test results indicate that they have negligible contribution in device performance when the MELO film thickness is about 10µm. To investigate whether the oxidation annealing step has a greater role in improving the device performance, diodes were fabricated in a same run with and without this annealing step but keeping the same CMP step. The average ideality factor of devices with oxidation treatment is 1.01 (average of 20 devices) whereas without oxidation treatment the average ideality factor became 1.07 (average of 20 devices). The test results show that the oxidation treatment prior to the diode fabrication is helping in removing some of the defects in the merged seam. The repeatable excellent device

performance of the MELO-diodes has established MELO-silicon (10μm thick) as an excellent quality single crystal silicon material.

Table **6.3** : Diode leakage currents

	Substrate-Diode	SEG-Diode	MELO-Diode
Room temp. Leakage amp/cm2	$< 1x10^{-08}$	$< 1x10^{-08}$	$< 1x10^{-08}$
Leakage at 115° C amp/cm2	—	$3.6x10^{-07}$	$2.8x10^{-06}$

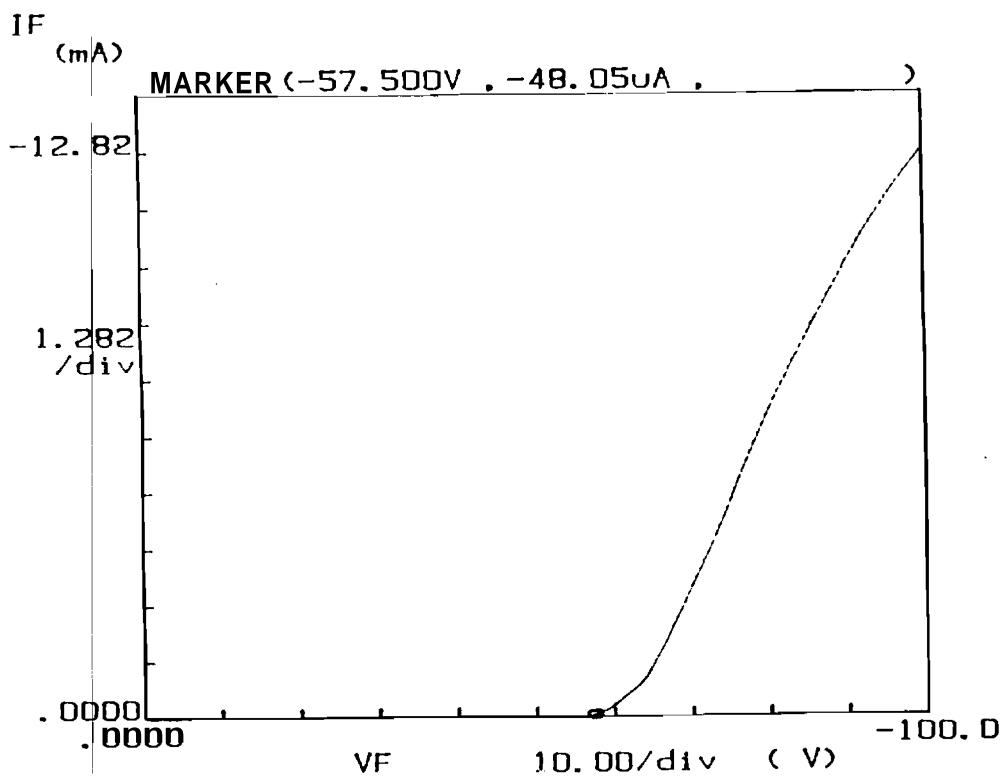


Figure 6.19 Breakdown characteristics of MELO diodes

6.5 Controlling the V-Groove Depth into The Membrane

The relatively wide and thin single crystal silicon diaphragms are formed by exploiting the advantages of merging of advancing ELO fronts and the formation of V-groove self limiting etch-stop during the back side etch. Controllability of the depth of the V-groove etch stops is essential when forming the beams from backside etching. Figure 6.20 illustrates two cases where the V-groove is terminated. Two factors are considered when controlling the V-groove etch depth; interfacial bond strength at the SEG/SiO_2 interface and the SEG seed hole width. In the first case, a weak bond at the SEG/SiO_2 interface will increase the etch rate of silicon around the oxide in the anisotropic KOH etchant and not stop at bottom edge of the oxide. Therefore the depth of the V-groove etch stop will increase. In the second case, a large seed hole defines the opening size of the V-groove and, therefore, the depth of the etch stop. Reduction of the etched V-grooves can be accomplished by strengthening the interfacial bond and by tightening the width of the seed hole.

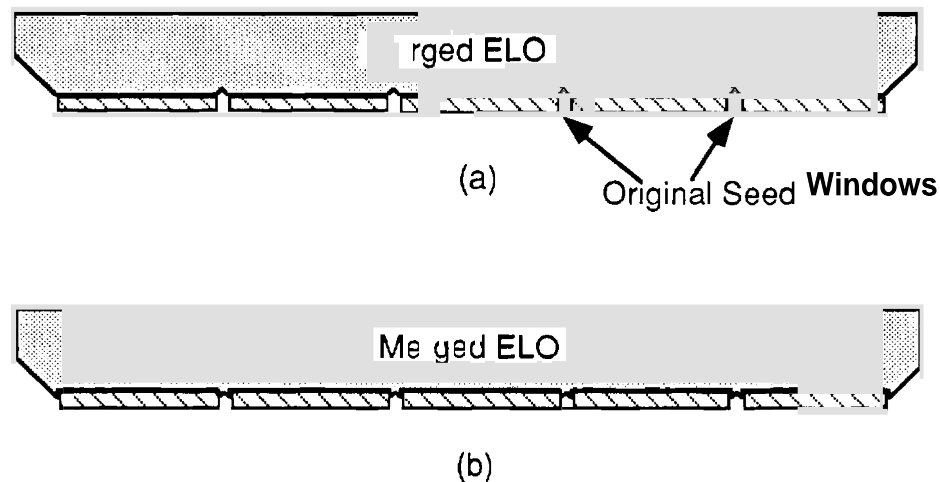
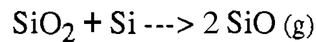


Figure 6.20. A wide thin diaphragm formation using MELO silicon combined with V-groove self-limiting etch stop: (a) with normal MELO silicon; (b) with the improved SEG/SiO_2 interface.

An attempt was made to minimize the effects of the V-grooves on the topology of the beam. First, to limit the depth of the V-grooves into the membrane we need to ensure a stronger bonding between the SEG silicon and the oxide sidewall so that. while etching we can expose the etch limiting <110> planes earlier along the oxide edges. Secondly, since the V-groove depth is proportional to the width of the seed window, a reasonably narrow (2μm) seed windows were selected.

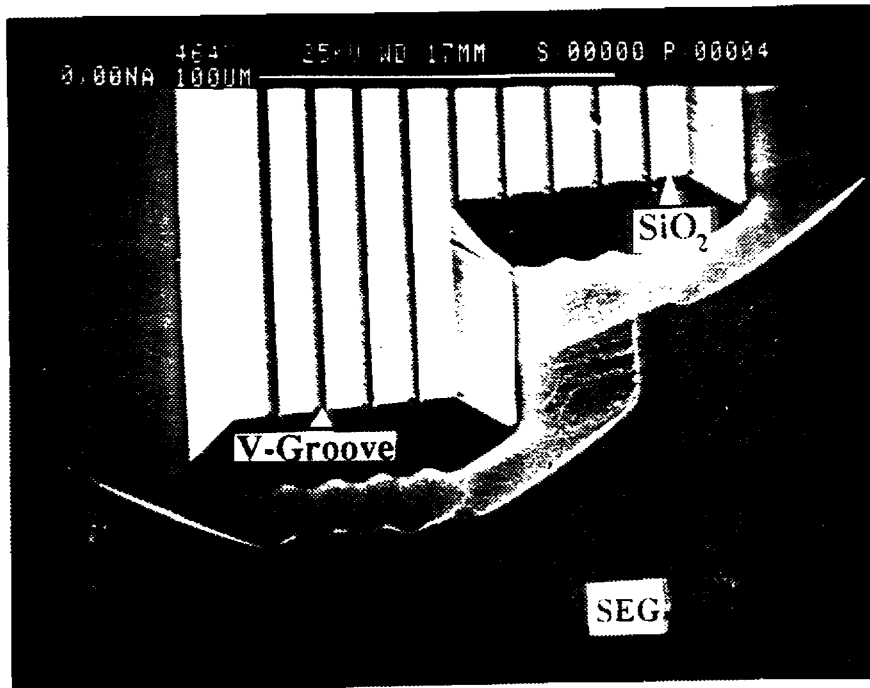
SEG/SiO_2 interface has been investigated due to the large interfacial leakage current observed in the SEG/ELO IC fabrication. The increase in the interfacial states is a result of the weak atomic bonding formed between the SEG silicon and the oxide wall. Evidence of the weak bonding includes the enhancement in the impurity diffusion down the sidewall and the silicon etch rate increases along the SEG/SiO_2 side walls. Possible explanation for the existence of the weak bond can be based on the following reaction, occurring at the interface during the epitaxial growth.



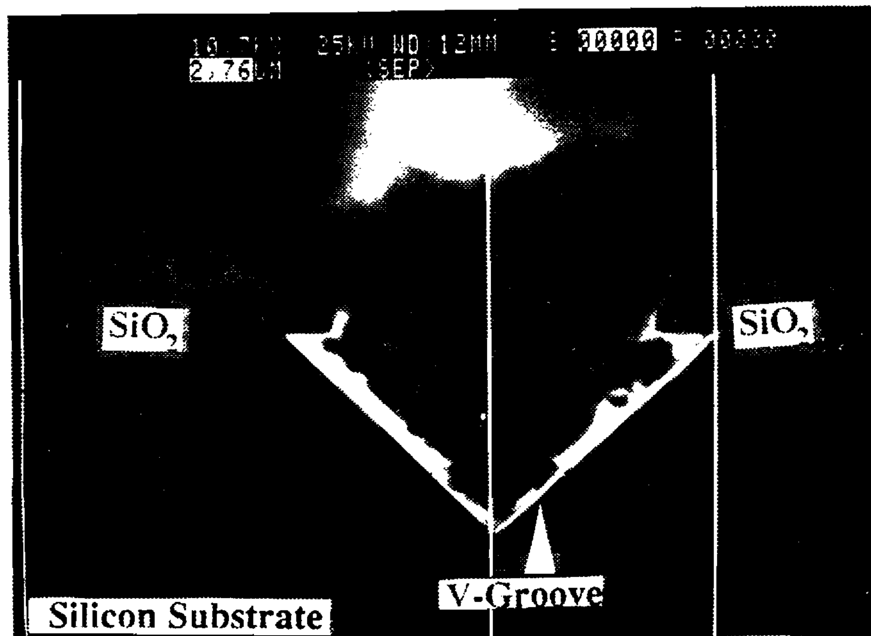
$$SiO_2 + Si \text{ ---> } 2\,SiO\,(g)$$

This reaction etches away both the silicon atoms and the oxide atoms at the interface, which, in effect, leaves a sheet of atomic voids and therefore results in a weak bonding from incomplete bond formation. Figure 6.21(a) shows the silicon near the SiO_2 strips etched faster, hence deeper than other parts of the SEG. Figure 6.21(b) shows how this causes the undercut of the SiO_2 and therefore deeper V-grooves.

Recent articles have stated that the interface shows improvement after a post epitaxial oxidation treatment (PEOX). This indirectly implies that the interface can be healed by normal post-epitaxial re-oxidation. During the re-oxidation, the interface becomes oxygen-rich and close to a thermally oxidized silicon surface which typically shows complete and strong bonding with few interface states. Taking advantage of this improvement, the PEOX process can be included into the normal ELO/MELO film process without further complexity.



(a)

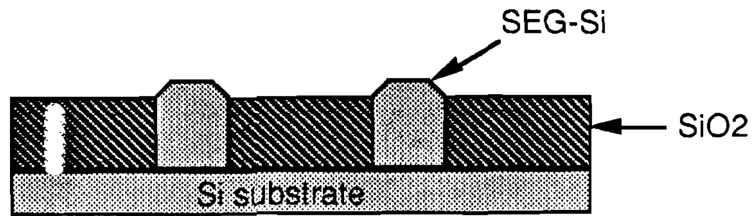


(b)

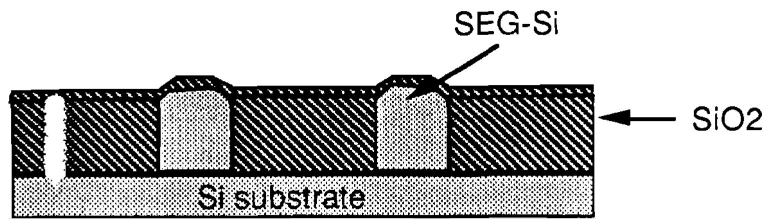
Figure 6.21 KOH etching of MELO to from V-grooves (a) SEM photograph showing enhancement of etching of silicon near silicon /oxide interface (b) SEM photograph showing the cross-section of the v-grooves having considerable amount of undercutting.

To incorporate this PEOX process into the SEG/ELO and MELO process the following approach illustrated in Figure 6.22, was attempted. Seed holes were patterned by wet etch followed by SEG growth. The duration of EPI growth was set such that the SEG coming out of the seed hole just begins to spread laterally over the oxide [Figure 6.22(a)]. Then, a layer of thermal oxide was grown on the SEG/ELO [Figure 6.22(b)]. At this step, the oxygen molecules will diffuse down the SEG/SiO_2 interface, fill the atomic voids created by the above mentioned reaction, and at the same time, completing the interfacial bonds. The thermal oxide was removed by BHF and then the ELO islands were planarized by chemical mechanical polishing (CMP) to remove any planes other than the <100> exposed on the top surface of the remaining SEG inside the seed hole [Figure 6.22(c)]. Finally MELO was grown from these post epitaxial oxidation treated seed holes [Figure 6.22(d)] To investigate the effect of PEOX treatment on limiting the V-groove depth while etching, the wafer was put into KOH etchant for a short period of time after removing the thermal oxide from the top of the ELO islands. Finally the wafer cross section was examined under SEM to investigate whether there was an early exposure of the etch limiting <110> planes at the sidewall of the oxide islands.

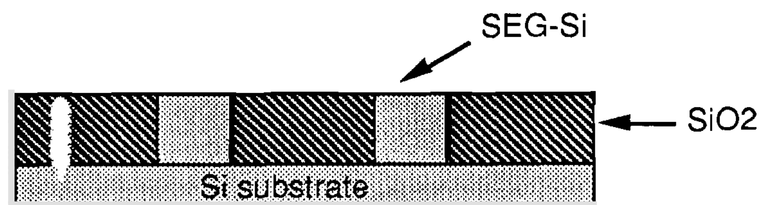
Thicker oxide was chosen so that the etch can be stopped while the silicon is still left in the oxide step of the seed hole. Since the etch rate of silicon in KOH is about 1μm/min., it was very difficult to stop the etch so that silicon was left in the oxide step. When the oxide side wall is slanted either by wet etch or RIE, early exposure of the etch limiting <110> planes at the side wall of the oxide step was not noticed even though the SEG/ELO grown from these seed holes were subjected to PEOX treatment [Figure 6.23(a)]. Even a 60 second KOH etching has resulted in a small amount of undercutting [Figure 6.23(a)]. However the etching characteristics of silicon near the oxide interface showed considerable improvement. As shown in Figure 6.23(b), the equal etch of both SEG silicon away from oxide and SEG silicon near the oxide strips was observed. This indicates that the SEG/oxide bonding at the interface has been improved by this PEOX process.



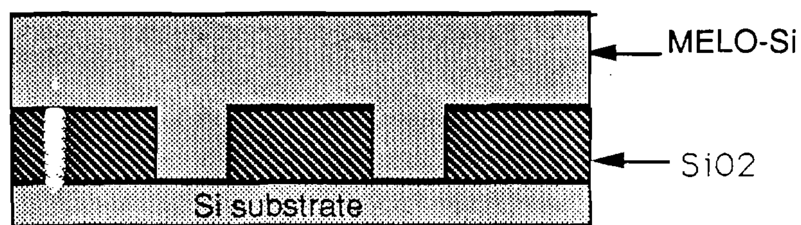
(a) SEG/ELO growth to top surface of oxide islands



(b) Oxidation to strength SEG-Si/SiO2 side walls.

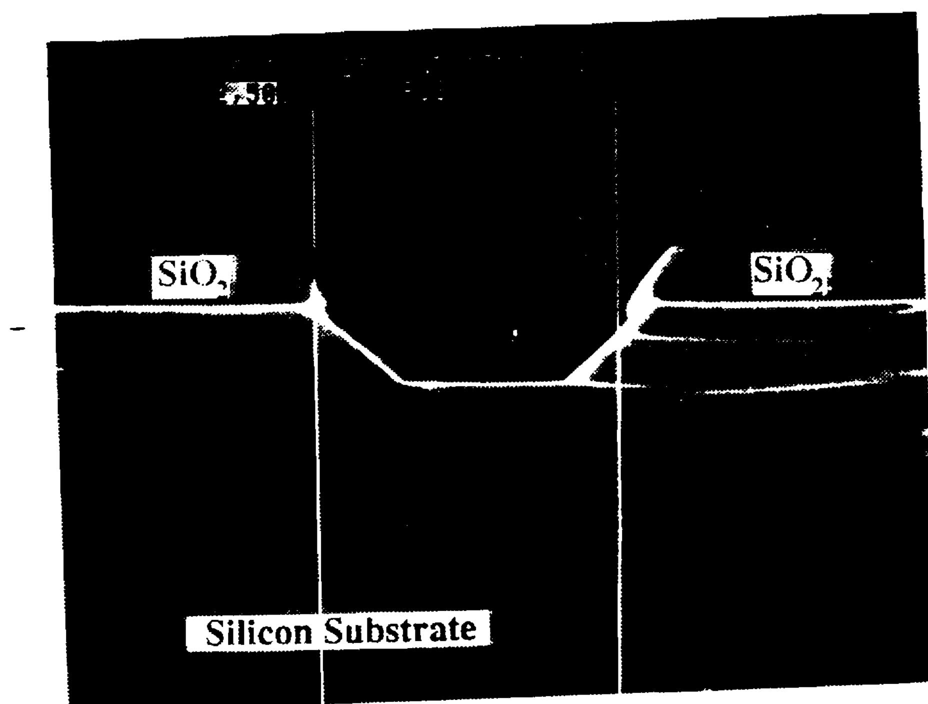


(c) Removal of oxide layer in BHF and after CMP



(d) Continuation of ELO/MELO growth to flat top

Figure 6.22: The SEG/ELO/MELO process including PEOX process.



(a)

(b)

Figure **6.23** KOH etching on PEOX treated seed holes.(a) SEM photograph showing the cross-section of the v-groove formation in Freon 115 etched seed hole.(b). SEM photograph showing equal etching of silicon in KOH near and away from oxide interface.

An attempt was made to investigate the effect of PEOX treatment on V-groove formation on SEG/ELO grown from more vertical oxide side walls. An 1μm thick thermal oxide was grown on (100) n-type wafers. The seed windows were etched by RIE with Freon 116 gas plasma for 200min at 1000W and 300 mT (about 500Å of oxide was left and removed in BHF dip). Positive photoresist AZ 1350 was used as a masking material during-this etch. Figure 6.24 shows the SEM photograph of the etched seed hole cross-section. Here the oxide side walls are almost vertical and the masking photoresist remained intact.

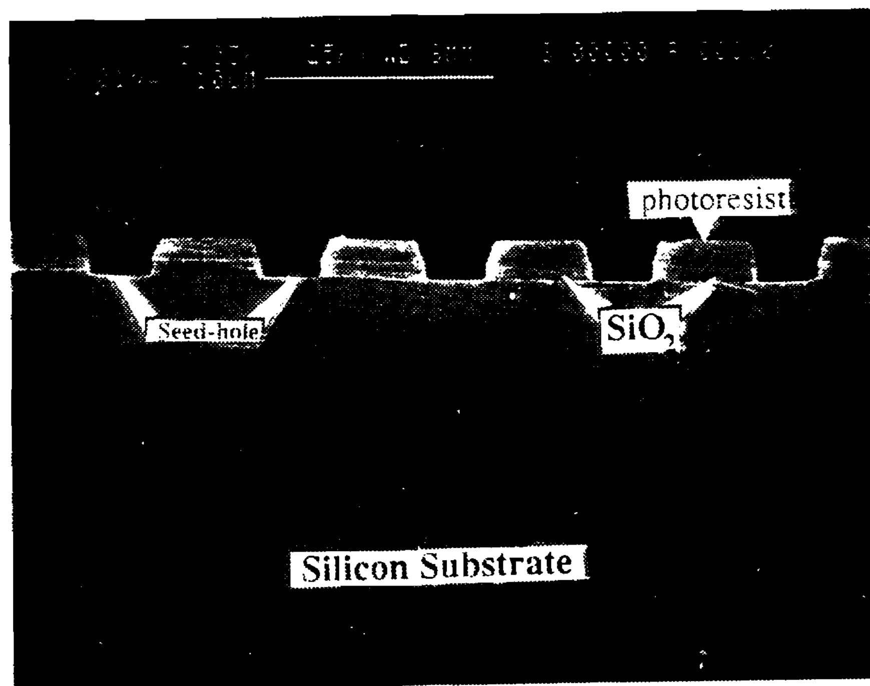


Figure 6.24. SEM photograph showing the cross-section of the RIE (Fr 116) etched seed holes.

The SEG/ELO used for these tests was grown for 20 min at 920° C, 150 Torr with 1.76 slpm HCl and 0.44 slpm DCS, resulting in 1.4 μm of growth. Figure 6.25 shows an SEM photograph of the top view of the ELO island grown from the RIE etched seed windows. The ELO spread was about 0.2μm over the oxide surface. The wafer was put into a wet oxidation tube for an hour at 1000' C. After this oxide was removed in a BHF dip, the wafer was thoroughly cleaned in piranha. Then the wafer was put into anisotropic KOH etchant for a shot time (40sec). The cross section under SEM analysis shows the starting of the V-groove formation inside the oxide step [Figure 6.26(a)]. But a longer etch (3 min. long) has propagated the V-grooves to the bottom of the oxide sidewall without any undercutting [Figure 6.26(b)]. With further narrowing the seed hole width and using PEOX treatment on seed holes with vertical side walls will eventually keep the V-grooves inside the oxide side walls.

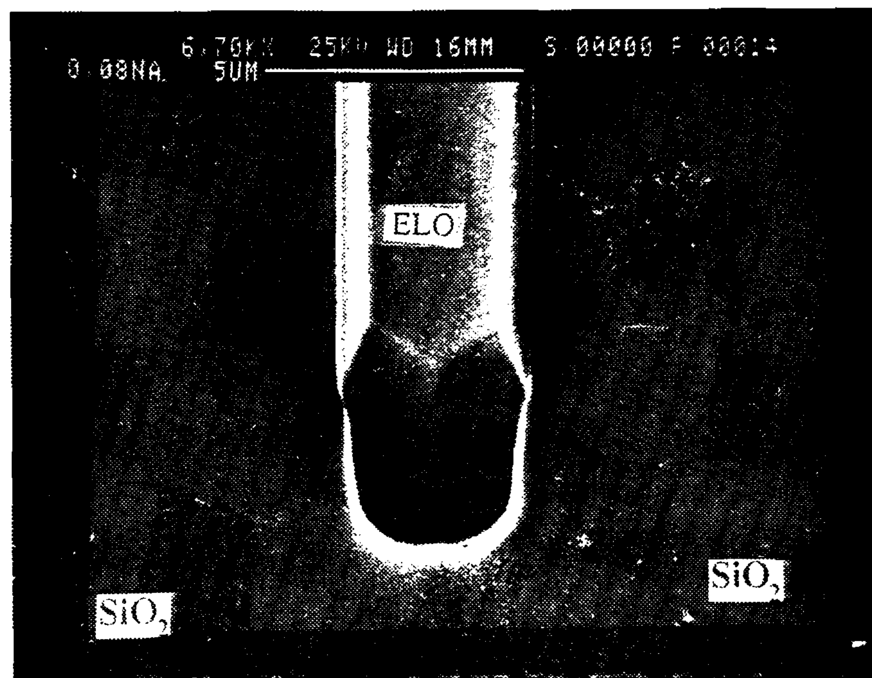
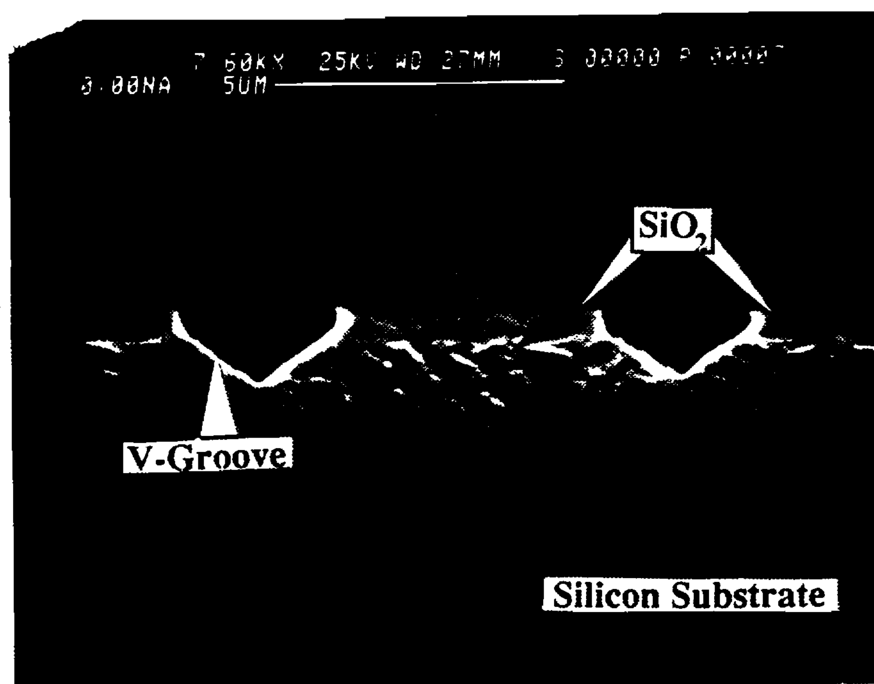
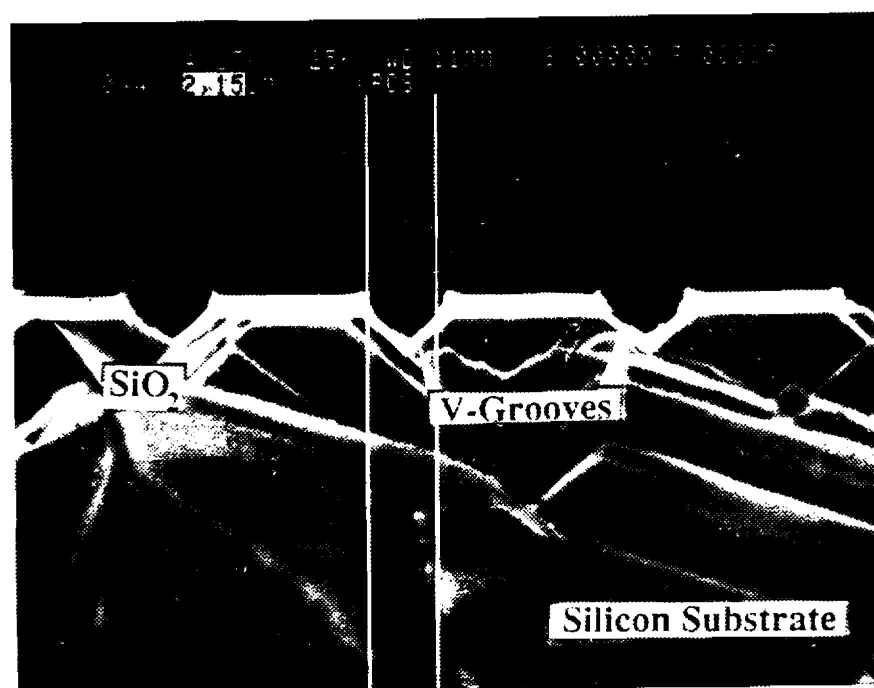


Figure 6.25. SEM photograph showing the top view of the ELO island grown from the RIE etched seed holes.



(a)



(b)

Figure 6.26. SEM photographs showing the cross-section of the V-grooves formed in the seed holes (etched by Freon 116) during KOH etching. (a) Cross-section after 40 second of etching. (b) After **3** minutes of etching.

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APPENDIX A

MELO-Si ACCELERPMETER FABRICATION PROCESS FLOW

(mask set JJP-MA1)

Wafer Set______________________________

Time/Date

1. Starting material
   a. Date process flow started ________
   b. Lot #____________; # of wafers____________
   d 3 inch n-type; (100) with flat on <110>
   d. Resistivity:____________R-cm
   e. Comments:

2. Alignment mark nimde
   (Include monitor wafers!)
   a. Piranha clean (H_2SO_4:H_2O_2 = 1:1), DI rinse, dry
   b. Plasma nimde dep. - 5000Å ________
   @ 650 mTorr, 300 °C, 50 Watts, w/ 5 sccm SiH_4, 50 sccm NH_3, 50 sccm N_2
   Resulted thickness: ____________
   Comments:

3. Nitride alignment lithography
   a. Clean the mask plate w/ piranha, DI rinse, Dry, Hardbake for 10 min.
   b. Mask #MA-1: Light Field!
   -- Apply HMDS, AZ4620 resist spin @ 6000rpm for 40sec.
   -- Softbake @ 90°C for 30min.
   -- Expose @ 23Watt/cm^2 w/ SUSS mask aligner for 30sec.
   -- Develop w/ AZ developer + DI water (1:1) for 2min., DI rinse, Dry
   -- Inspection: ____________
   -- Hardbake @ 110°C for 30 min. ________
   c. Etch plasma nimde in BHF until the etched area dewets: time ________ ________
   d. Strip resist w/ solvents and then piranha clean for 20 min. ________
   -- Inspection: ____________
   e. Comments:

4. Field oxidation (or Etch-stop oxide growth)
   (Include monitor Wafers!)
   a. Piranha clean, DI rinse, Dry.
   b. H_2 burn oxidation @ 1100 °C w/ 90sccm H_2, 60sccm O_2 for 150 min. ________
   c. Oxide color/thickness: _________/_________ (10251Å from SUPREM3)

Time/Date

5. MELO seed lithography
   a. Clean the mask plate w/ piranha. DI rinse, Dry. Hardbake for 10 min.
   b. Mask #MA-2: Light Field!
      -- Apply HMDS, AZ1350 resist spin @ 4000rpm for 30sec.
      -- Softbake @ 90°C for 15min.
      -- Expose @ 23Watt/cm^2 w/ SUSS mask aligner for 7.5sec.
      -- Develop w/ AZ developer + DI water (1:1) for 2min., DI rinse, Dry
      -- Inspection: ____________
      -- Hardbake @ 110°C for 20 min. __________
   c. Etch with BHF until the etched area dewets: time ________
   d. Strip resist w/ solvents __________
      -- Inspection: ____________
   e. Comments:

6. MELO-Si growth
   (Include monitor wafers!)
   a. Piranha clean for 15 min., DI rinse
   b. BHF dip for 10 sec., DI rinse, Dry
      -- Thorough rinse with DI water is an ABSOLUTE condition for good MELO-Si
      -- Avoid any contamination while drying with nitrogen gun.
   c. MELO process parameters:
      run#: ________
      prebake: time_____, H_2 _____, HCL ______, DCS ______.Temp ______,Pressure ______
      HCL etch: time ______, H_2 ______,HCL ______, Temp ______, Pressure ______
      Dep.: time_____, H_2 ______, HCL ______, DCS ______, Temp ______, Pressure ______
   d. Inspection: __________
      -- ELO thickness with profilometer: average ______, std. dev. ______.
      -- Nucleation (subjective): ______
      __ Sheet resistivity with four point probe: ______
   e. Comments:

7. MELO-Si field oxidation
   (Include monitor wafers!)
   a. Piranha clean, DI rinse, Dry.
   b. H_2 burn oxidation @ 1100 °C w/ 90sccm H_2, 60sccm O_2 for 30 min. __________
      -- Oxide color/thickness: _________/_________ (3125Å from SUP3)
   c. Comments:

8. Piezoresistor lithography
   a. Clean the mask plate w/ piranha, DI rinse, Dry, Hardbake for 10 min.
   b. Mask #MA-3: Dark Field!
      -- Apply HMDS, AZ1350 resist spin @ 4000rpm for 30sec.
      -- Softbake @ 90°C for 15min.
      -- Expose @ 23Watt/cm^2 w/ SUSS mask aligner for 7.5sec.
      -- Develop w/ AZ developer + DI water (1:1) for 45- OW., DI rinse, Dry
      -- Inspection: ____________
      -- Hardbake @ 110°C for 20 min. __________
   c. Etch with BHF until the etched area dewets: time ________
      -- Rinse, dry, and use the photoresist as an additional ion implant mask.
      -- Inspection: ____________

Time/Date

9. Piezoresistor (p-type) implant
   a. Boron implant @25keV, $1.0x10^{15}/cm^2$ __________
      -- Implant with the beam line pressure below $1x10^{-6}$ Torr
      -- Beam current: _________
   b. Strip photoresist with solvents and then piranha clean.
   c. Comments:

10. Baselithography
   a. Clean the mask plate w/ piranha. DI rinse. Dry. Hardbake for 10 min.
   b. Mask #MA-4: Dark Field!
      -- Apply HMDS. AZ1350 resist spin @ 4000rpm for 30sec.
      -- Softbake @ 90°C for 15min.
      -- Expose @ $23Watt/cm^2$ w/ SUSS mask aligner for 7.5sec.
      -- Develop w/ AZ developer + DI water (1:1) for 45-60sec., DI rinse. Dry
      -- Inspection: _____________
      -- Hardbake @ 110°C for 20 min. __________
   c. Etch with BHF until the etched area dewets: time _________
      -- Rinse, dry, and use the photoresist as an ion implant mask.
      -- Inspection: _____________
   d. Comments:

11. Base (p-type) implant
   a. Boron implant @25keV, $3.0x10^{13}/cm^2$ __________
      -- Implant with the beam line pressure below $1x10^{-6}$ Torr
      -- Beam currenr _________
   b. Strip photoresist with solvents and then piranha clean.
   c. Comments:

12. Base drive-in
   a. Piranha clean. DI rinse, dry
   b. Wet oxidation @1000°C w/ 90sccm H_2, 60sccm O_2 for 15 min. __________
      -- Oxide color/thickness: SEG/MEMO:__________/__________
      piezoresistor:__________/__________
      base: __________/__________
   c. Comments:

13. Emitter lithography
   a. Clean the mask plate w/ piranha. DI rinse. Dry. Hardbake for 10 min.
   b. Mask #MA-5: Dark Field!
      -- Apply HMDS. AZ1350 resist spin @ 4000rpm for 30sec.
      -- Softbake @ 90°C for 15min.
      -- Expose @ $23Watt/cm^2$ w/ SUSS mask aligner for 7.5sec.
      -- Develop w/ AZ developer + DI water (1:1) for 45-60sec., DI rinse. Dry
      -- Inspection: _____________
      -- Hardbake @ 110°C for 20 min. __________
   c. Etch with BHF until the etched area dewets: time _________
   d. Strip photoresist with solvents and piranha clean, DI rinse, dry.
      -- Inspection: _____________
   e. Comments:

Time/Date

14. Emitter implant
    a. Arsenic implant @25keV, $3.0 \times 10^{15}/cm^2$ __________
       -- Implant with the beam line pressure below 1×10^{-6} Torr
       -- Beam current. __________
    b. Strip photoresist with solvents and then piranha clean.
    c. Comments:

15. Emitter drive-in
    a. Piranha clean, DI rinse, dry
    b. Wet oxidation @1000°C w/ 90sccm H_2, 60sccm O_2 for 15 min. __________
       -- Oxide color/thickness: SEG/MEMO:__________/__________
       piezoresistor:__________/__________
       base: __________/__________
       emitter: __________/__________
    c. Comments:

16. Contact lithography
    a. Clean the mask plate w/ piranha, DI rinse. Dry, Hardbake for 10 min.
    b. Mask #MA-6: Dark Field!
       -- Apply HMDS, AZ1350 resist spin @ 4000rpm for 30sec.
       -- Softbake @ 90°C for 15min.
       -- Expose @ $23 Watt/cm^2$ w/ SUSS mask aligner for 7.5sec.
       -- Develop w/ AZ developer + DI water (1:1) for 45-60sec., DI rinse, Dry
       -- Inspection: __________
       -- Hardbake @ 110°C for 20 min. __________
    c. Etch with BHF until the etched area dewets: time __________
    d. Strip photoresist with solvents and piranha clean, DI rinse, *dry*.
       -- Inspection: __________

17. Metal (AI-Si) deposition
    a. Load the wafers in the Al-Si dep. chamber and Wait till Pressure$<3 \times 10^{-7}$ Torr.
    b. Sputter deposit Al-Si(1%) @ 100 Watt, 8 mTorr for 30min. __________
    c. Inspect the metal surface smoothness
    d. Comments:

18. Metal Anneal
    a. Anneal in Nitrogen @ 400 °C for 20 min. __________
    b. Comments:

19. Metal lithography
    a. Clean the mask plate w/ piranha, DI rinse, Dry, Hardbake for 10 min.
    b. Mask #MA-7: Dark Field!
       -- Apply HMDS, KTI 747 negative resist spin @ 3000rpm for 40sec.
       -- Softbake @ 90°C for 15min.
       -- Expose @ $23 Watt/cm^2$ w/ SUSS mask aligner for 3sec.
       -- Develop w/ KTI developer, Rinse w/ KTI rinse, Dry w/ Nitrogen
       -- Inspection: __________
       -- Hardbake @ 110°C for 20 min. __________

Time/Date

c. Etch w/ (25ml DI + 100ml Acetic Acid + 25ml Nimc Acid + 100ml Phosphoric Acid)
   -- Do not overetch the metal!
   -- DI rinse.
d. Strip photoresist with warm Nophenol with mild agitation ________
   -- Rinse with TCA. ACE, METH with agitation, DI rinse, dry.
   -- Inspection: ____________
e. Comments:

20. Chrome (Cr.) deposition
    a. Load the wafers in the Cr. dep. chamber and Wait till Pressure<3×10^{-7} Torr.
    b. Sputter deposit Cr. @ 100 Watt, 8 mTorr for 60min. ________
    c. Inspect the metal surface smoothness
    d. Comments:

21. Passivation nitride deposition
    a. PECVD nitride deposition @ 350 mTorr, 300 °C, 50 Watt, ________
       w/ 50sccm w/ 5 sccm SiH_4, 50 sccm NH_4, 50 sccm N_2
    b. Front deposition- 1 hour + 2 hours (total 3 hours)
       Back deposition- 1 hour
    c. Comments:

22. Back-etch pattern lithography
    a. Clean the mask plate w/ piranha, DI rinse, Dry, Hardbake for 10 min.
    b Mask #MA-8: Dark Field!
       -- Apply HMDS, A24620 resist spin @ 6000rpm for 40sec. on the back.
       -- Softbake @ 90°C for 30min.
       -- Apply HMDS, A24620 resist spin @ 6000rpm for 40sec. on the front.
       -- Softbake @ 90°C for 30min.
       -- Expose the back side with SUSS double sided mask aligner for 3min.
       -- Develop w/ AZ developer + DI water (1:1) for 3-5min., DI rinse, Dry
       -- Inspection: ____________
       -- Hardbake @ 110°C for 20 min. ________
    c. Etch w/ SF_6 @ 500 watts (PECVD nimde etch rate: ≈ 0.5μm/min)
       -- Need a visual inspection
       -- Etched time: ________
       -- Inspection: ____________
    d. Strip photoresist with warm Nophenol with mild agitation ________
       -- Rinse with TCA, ACE, METH with agitation, DI rinse, dry.
       -- Inspection: ____________
    e. Comments:

23. MELO-Si diaphragm formation
    a. KOH anisotropic etching
       -- Etching solution: 127ml DI, 47gm KOH, 39ml n-propanol (or their multiples).
       -- Temperature: 80±1°C
       -- Time: 5-7 hours. After 5 hours, the manual inspection is recommended.
       -- DI soak (overnight is recommended).
    b. The diaphragm is very fragile after the KOH etching. Therefore, extreme caution
       is necessary during rinsing and drying.
       -- Inspection: ____________

Time/Date

24. Assemble to the back plate
    a. Apply glue on the back plate dies, next to the etched basin edges, parallel to the accelerometer bridges direction and attach the MELO-Si accelerometer wafer (or dies) on the back plate aligning the beck of the middle mass to the basin
    b. Hardbake @ 110 °C for 1 hour or more. __________
    c. IF the MELO-SI accelerometer dies become separated into dies, then the wafer *can* be diced and each accelerometer die *can* be attached to each back plate die individually.
    c. Comments:

25. Front passivation nitride removal
    a. Etch the front nitride w/ SF_6 @ 500 watts __________
       -- Need a visual inspection until Cr. is completely exposed.
       -- Etched time: __________
       -- Inspection: ____________
    b. Comments:

26. Front Cr. removal
    a. Etch Cr. w/ (500ml DI + 20ml Acetic Acid + 50gm $(NH_4)_2Ce(NO_3)_6$) __________
       -- Need a visual inspection until Cr. is completely etched.
       -- Etched time: __________
       -- Inspection: ____________
    b. Comments:

27. Front delineation lithography
    a. This lithography step *can* be performed on either a whole wafer or individual dies. In the case of individual dies, they *can* be amounted on another wafer and can be processed.
    b. Clean the mask plate w/ piranha, DI rinse, Dry, Hardbake for 10 min.
    c Mask #MA-9: Dark Field!
       -- Apply HMDS, AZ4620 resist spin @ 6000rpm for 40sec.
       -- Softbake @ 90°C for 30min.
       -- Expose @ 23Watt/cm^2 w/ SUSS mask aligner for 30sec.
       -- Develop w/ AZ developer + DI water (1:1) for 90-120sec., DI rinse. Dry
       -- Inspection: ____________
       -- Hardbake @ 110°C for 20 min. __________
    d Etch w/ SF_6 @ 500 watts (PECVD nitride etch rate: ≈ 1μm/min)
       -- Need a visual inspection
       -- Etched time: __________
       -- Inspection: ____________
    e. Etch the seed window oxides with BHF. __________
       -- DI soak (overnight is recommended).
       -- Inspection: ____________
    f. Strip photoresist by soaking in solvents, DI rinse, bake dry. __________
    g. Comments:

28. Packaging and Al-Si wire bonding
    a. Apply glue on the back of the back-plate die and attach it onto the package
    b. Hardbake @ 110 °C for 1 hour or more. __________
    c. Wire bond on the bonding pads and test the accelerometer.

APPENDIX B

ANSYS INPUT FILE FOR MELO-SI ACCELEROMETER SIMULATION

```
* Filename = in1
* Written by James Pak - 8/ 27/92

* Enable screen plotting using x-window on Sun Sparc work station
/show,x11,,1

/PREP7
/TITLE,MELO-Si accelerometer as a simple bridge
KAN,0
MAT,1
ET,1,45,,,,,,2

*       Material Properties for silicon

MP,EX,1,1.7e12
MP,NUXY,1,.063
MP,ALPX,1,2.33e-6
MP,DENS,1,2.33

*       Input geometrin parameters in CGS units
*               Thickness of the beam = 10 microns (=0.001 cm)
*               Length of the beam = 420 microns (4.042 cm)
*               Width of the beam = 160 microns (4.016 cm)
*               Thickness of die = 370 microns (=0.037 cm)
*               Half of the die length (in x dir) = 0.18 cm
*               Half of the die length (in y dir) = 0.20 cm
*               Top mass edge in x-dir = 880 microns (4.088 cm)
*               Top mass edge in y-dir = 1240 microns (=0.124 cm)
*               Width of cavity opening in x dir = 420 microns (=0.042 cm)
*               Width of cavity opening in y dir = 120 microns (=0.012 cm)
*               Distance to cavity outer edge in x dir = 0.13 cm
*               Distance to cavity outer edge in y dir = 0.136 cm
*               Bottom mass edge in y-dir = 980 microns (=0.098 cm)
*               Bottom mass edge in x-dir = 620 microns (=0.062 cm)
*               Substrate thickness = 360 microns (=0.036 cm)
*               Acceleration level = 1g (=980 cm/sec*sec)

* Create keypoints in CGS units (in cm)

* Proof mass key points

k,1,0,0,0
k,2,0,0.04,0
k,3,0,0.056,0
```

```
k,4,0,0.098,0
k,5,0.062,0.098,0
k,6,0.062,0.056,0
k,7,0.062,0.04,0
k,8,0.062,0,0

k,9,0,0,0.036
k,10,0,0.04,0.036
k,11,0,0.056,0.036
k,12,0,0.124,0.036
k,13,0.088,0.124,0.036
k,14,0.088,0.056,0.036
k,15,0.088,0.04,0.036
k,16,0.088,0,0.036

k,17,0,0,0.037
k,18,0,0.04,0.037
k,19,0,0.056,0.037
k,20,0,0.124,0.037
k,21,0.088,0.124,0.037
k,22,0.088,0.056,0.037
k,23,0.088,0.04,0.037
k,24,0.088,0,0.037

* Support keypoints

k,25,0,0.162,0
k,26,0,0.2,0
k,27,0.156,0.2,0
k,28,0.18,0.2,0
k,29,0.18,0.162,0
k,30,0.18,0.056,0
k,31,0.18,0.04,0
k,32,0.18,0,0
k,33,0.156,0,0
k,34,0.156,0.04,0
k,35,0.156,0.056,0
k,36,0.156,0.162,0

k,37,0,0.136,0.036
k,38,0,0.2,0.036
k,39,0.13,0.2,0.036
k,40,0.18,0.2,0.036
k,41,0.18,0.136,0.036
k,42,0.18,0.056,0.036
k,43,0.18,0.04,0.036
k,44,0.18,0,0.036
k,45,0.13,0,0.036
k,46,0.13,0.04,0.036
k,47,0.13,0.056,0.036
k,48,0.13,0.136,0.036

k,49,0,0.136,0.037
k,50,0,0.2,0.037
```

```
k,51,0.13,0.2,0.037
k,52,0.18,0.2,0.037
k,53,0.18,0.136,0.037
k,54,0.18,0.056,0.037
k,55,0.18,0.04,0.037
k,56,0.18,0,0.037
k,57,0.13,0,0.037
k,58,0.13,0.04,0.037
k,59,0.13,0.056,0.037
k,60,0.13,0.136,0.037

* Create volumes for mass substrate

v,9,16,8,1,10,15,7,2
v,10,15,7,2,11,14,6,3
v,11,14,6,3,12,13,5,4

* Create volumes for mass epi-region

v,17,24,16,9,18,23,15,10
v,18,23,15,10,19,22,14,11
v,19,22,14,11,20,21,13,12

* Create volume for support substrate

v,37,48,36,25,38,39,27,26
v,48,41,29,36,39,40,28,27
v,47,42,30,35,48,41,29,36
v,46,43,31,34,47,42,30,35
v,45,44,32,33,46,43,31,34

* Create volume for support epi-region

v,49,60,48,37,50,51,39,38
v,60,53,41,48,51,52,40,39
v,59,54,42,47,60,53,41,48
v,58,55,43,46,59,54,42,47
v,57,56,44,45,58,55,43,46

* Create volume for beam

v,23,58,46,15,22,59,47,14

* Proof mass substrate line div x direction

LDVS,1,,5,.2
LDVS,3,,5,5
LDVS,6,,5,5
LDVS,10,,5,5
LDVS,14,,5,5
LDVS,18,,5,5
LDVS,22,,5,5
LDVS,26,,5,5
```

```
* Proof mass epi region line div x direction

LDVS,29,,5,.2
LDVS,33,,5,5
LDVS,38,,5,5
LDVS,43,,5,5

* Proof mass substrate line div y direction

LDVS,5,,5,.2
LDVS,7,,5,5
LDVS,9,,5,5
LDVS,11,,5,5

LDVS,13,,8
LDVS,15,,8
LDVS,17,,8
LDVS,19,,8

LDVS,21,,5,5
LDVS,23,,5,.2
LDVS,25,,5,.2
LDVS,27,,5,.2

* Proof mass epi region line div y direction

LDVS,32,,5,.2
LDVS,34,,5,5

LDVS,37,,8
LDVS,39,,8

LDVS,42,,5,5
LDVS,44,,5,.2

* Proof mass substrate line div z direction

LDVS,2,,3
LDVS,4,,3
LDVS,8,,3
LDVS,12,,3
LDVS,16,,3
LDVS,20,,3
LDVS,24,,3
LDVS,28,,3

* Proof mass epi region line div z direction

LDVS,30,,1
LDVS,31,,1
LDVS,35,,1
LDVS,36,,1
LDVS,40,,1
LDVS,41,,1
```

```
LDVS,45,,1
LDVS,46,,1

* Support substrate line div x direction

LDVS,47,,5
LDVS,49,,5
LDVS,52,,5
LDVS,56,,5

LDVS,59,,5,5
LDVS,61,,5,.2
LDVS,63,,5,.2
LDVS,66,,5,.2
LDVS,67,,5,5
LDVS,69,,5,.2
LDVS,75,,5,5
LDVS,77,,5,.2
LDVS,83,,5,5
LDVS,85,,5,.2

* Support epi region line div x direction

LDVS,91,,5
LDVS,95,,5

LDVS,99,,5,5
LDVS,102,,5,.2
LDVS,104,,5,5
LDVS,109,,5,5
LDVS,114,,5,5

* Support substrate line div y direction

LDVS,51,,5
LDVS,53,,5
LDVS,55,,5
LDVS,57,,5
LDVS,62,,5
LDVS,65,,5

LDVS,71,,7,5
LDVS,72,,7,.2
LDVS,73,,7,.2
LDVS,74,,7,.2

LDVS,79,,8
LDVS,80,,8
LDVS,81,,8
LDVS,82,,8

LDVS,87,,5,.2
LDVS,88,,5,5
LDVS,89,,5,5
```

```
LDVS,90,,5,5

 * Support epi region line div y direction

LDVS,94,,5
LDVS,96,,5
LDVS,101,,5

LDVS,107,,7,5
LDVS,108,,7,.2

LDVS,112,,8
LDVS,113,,8

LDVS,117,,5,.2
LDVS,118,,5,5

 * Support substrate line div z direction

LDVS,48,,3
LDVS,50,,3
LDVS,54,,3
LDVS,58,,3
LDVS,60,,3
LDVS,64,,3
LDVS,68,,3
LDVS,70,,3
LDVS,76,,3
LDVS,78,,3
LDVS,84,,3
LDVS,86,,3

 * Support epi region line div z direction

LDVS,92,,1
LDVS,93,,1
LDVS,97,,1
LDVS,98,,1
LDVS,100,,1
LDVS,103,,1
LDVS,105,,1
LDVS,106,,1
LDVS,110,,1
LDVS,111,,1
LDVS,115,,1
LDVS,116,,1

 * Line division for beam length

LDVS,119,,8
LDVS,120,,8
LDVS,121,,8
LDVS,122,,8
```

```
* Create all the nodes

VMESH,ALL

* Clamped boundary conditions at support

NRSEL,Z,0,0
NRSEL,X,156,180
D,ALL,ALL,0
NALL

NRSEL,Z,0,0
NRSEL,Y,162,200
D,ALL,ALL,0
NALL

* Symmetry conditions

SYMBC,0,1,0
SYMBC,0,2,0

* Apply aceleration 10g in z direction

ACEL,0,0,9800

LWRITE

AFWRITE
```

APPENDIX C

FEM ANALYSIS FOR MELO-SI ACCELEROMETER DYNAMIC RESPONSE

```
* *******************************************************************
*   Finite Element Analysis of a bridge-type MELO-Si accelerometer
*   Using elastic beam simulation by Linear Interporlation
*
*
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*  -                                  Last Mod. Date : Mar. 22, 1992   -
* *******************************************************************

      PROGRAM PIEZOBEAMFEM

      IMPLICIT DOUBLE PRECISION(A-H,O-Z)
      DIMENSION AM(50,50),AK(50,50),AMEL(4,4),AKEL(4,4)
     &     ,NELCON(50,4),EVAL(50),EVEC(50,50)
     &     ,LEBC(50),UEBC(50),ELENGTH(50),DL(50)
      DOUBLE PRECISION ML(50)

      CMMON/WORKSP/RWKSP
      Real RWKSP(7158)
      CALL IWKIN(7158)

      OPEN(unit=1,file='femdatapak',status='unknown')
      OPEN(unit=11,file='mode1',status='unknown')
      OPEN(unit=12,file='mode2',status='unknown')
      OPEN(unit=13,file='x',status='unknown')


**************************
*   Constants
**************************
      pi = 4.D0*DATAN(1.D0)


**************************
*   Initialization
**************************
      DO 1 m=1,50
      DO 1 n=1,50
      AM(m,n) = 0.D0
    1 AK(m,n) = 0.D0
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***************************
*    Read in Data
***************************
      READ(1,*)
      READ(1,*) Y,rho

      READ(1,*)
      READ(1,*)  Nelem

      READ(1,*)
      DO 10 N=1,Nelem
   10 READ(1,*) NELCON(N,1),NELCON(N,2),NELCON(N,3),NELCON(N,4)

      READ(1,*)
      DO 20 N=1,Nelem
      READ(1,*)  xl,xr,thickness,width
      ML(N) = thickness*rho*width
      DL(N) = Y/12.D0*thickness**3*width
   20 ELENGTH(N) = xr-xl

      READ(1,*)
      READ(1,*) Nebc
      READ(1,*)
      DO 30 N=1,Nebc
   30 READ(1,*) Lebc(N),Uebc(N)

      Nnode = Nelem*2 + 2


******************************************
*    Assemble Global Matrix
******************************************
      DO 100 N=1,Nelem
         CALL ELEM(ML(N),DL(N),elength(N),AMEL,AKEL)
         DO 50 i=1,4
          II = NELCON(N,i)
          DO 40 j=1,4
           JJ = NELCON(N,j)
           AK(II,JJ) = AK(II,JJ) + AKEL(i,j)
           AM(II,JJ) = AM(II,JJ) + AMEL(i,j)
   40    CONTINUE
   50  CONTINUE
  100 CONTINUE


******************************************
*    Essential Boundary Condition
******************************************

      CALL EBC(Nnode,NEBC,Lebc,AK,AM)
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****************************************
*    Find Natural Frequencies
****************************************


      CALL DGVCSP(Nnode,AK,50,AM,50,EVAL,EVEC,50)

      PRINT*,'    Natural Frequency'
      PRINT*,'N      Short     Open    Real'
      DO 300 i=1,Nnode
         Freq = Sngl(Dsqrt(Eval(i))/2./pi)
         PRINT*,i,Freq
  300 CONTINUE

      DO 350 k=1,Nnode/2
      PRINT*,k,EVEC(2*(k-1)+1,5)
  350 WRITE(11,*) EVEC(2*(k-1)+1,5)
      DO 360 k=1,Nnode/2
      PRINT*,k,EVEC(2*(k-1)+1,6)
  360 WRITE(12,*) EVEC(2*(k-1)+1,6)
      x=0.
      WRITE(13,*) x
      DO 370 k=1,Nelem
      x = x + elength(k)
  370 WRITE(13,*) x*1.D6


      STOP
      END


*******************************************
      SUBROUTINE ELEM(mL,DL,L,AMEL,AKEL)
*******************************************

      IMPLICIT DOUBLE PRECISION(A-H,O-Z)
      DIMENSION AMEL(4,4),AKEL(4,4)
      DOUBLE PRECISION mL,L

      AMEL(1,1) = 156.D0
      AMEL(1,2) = 22.D0*L
      AMEL(1,3) = 54.D0
      AMEL(1,4) = -13.D0*L
      AMEL(2,1) = 22.D0*L
      AMEL(2,2) = 4.D0*L**2
      AMEL(2,3) = 13.D0*L
      AMEL(2,4) = -3.D0*L**2
      AMEL(3,1) = 54.D0
      AMEL(3,2) = 13.D0*L
      AMEL(3,3) = 156.D0
      AMEL(3,4) = -22.D0*L
      AMEL(4,1) = -13.D0*L
      AMEL(4,2) = -3.D0*L**2
      AMEL(4,3) = -22.D0*L
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      AMEL(4,4) = 4.D0*L**2
      AKEL(1,1) = 12.D0*DL/L**3
      AKEL(1,2) = 6.D0*L*DL/L**3
      AKEL(1,3) = -12.D0*DL/L**3
      AKEL(1,4) = 6.D0*L*DL/L**3
      AKEL(2,1) = 6.D0*L*DL/L**3
      AKEL(2,2) = 4.D0*L**2*DL/L**3
      AKEL(2,3) = -6.D0*L*DL/L**3
      AKEL(2,4) = 2.D0*L**2*DL/L**3
      AKEL(3,1) = -12.D0*DL/L**3
      AKEL(3,2) = -6.D0*L*DL/L**3
      AKEL(3,3) = 12.D0*DL/L**3
      AKEL(3,4) = -6.D0*L*DL/L**3
      AKEL(4,1) = 6.D0*L*DL/L**3
      AKEL(4,2) = 2.D0*L**2*DL/L**3
      AKEL(4,3) = -6.D0*L*DL/L**3
      AKEL(4,4) = 4.D0*L**2*DL/L**3

      DO 10 i=1,4
      DO 10 j=1,4
   10 AMEL(i,j) = AMEL(i,j)*mL*L/420.D0

      RETURN
      END

*******************************************
      SUBROUTINE EBC(Nnode,Nebc,LEBC,AK,AM)
*******************************************

      IMPLICIT DOUBLE PRECISION(A-H,O-Z)
      DIMENSION AK(50,50),AM(50,50),LEBC(50)


      DO 200 N=1,Nebc
      DO 100 I=1,Nnode
      AK(I,LEBC(N)) = 0.0D0
      AK(LEBC(N),I) = 0.0D0
      AM(LEBC(N),I) = 0.0D0
  100 AM(I,LEBC(N)) = 0.0D0

      AK(LEBC(N),LEBC(N)) = 1.0D0
      AM(LEBC(N),LEBC(N)) = 1.0D0

  200 CONTINUE

      RETURN
      END
```