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by

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ABSTRACT

Fully-depleted single-gated and dual-gated SOI MOSFETs are fabricated using both Epitaxial Lateral Overgrowth (ELO) and Confined Lateral Selective Epitaxial Growth (CLSEG). SOI MOSFETs and diodes are fabricated in thin ($\approx$ 1500Å) CLSEG films grown in pre-defined 2500Å thick cavities for the first time. In addition to the SOI MOSFETs fabricated using selective epitaxial growth, thin-film SOI MOSFETs were also fabricated on SIMOX wafers. The one to one comparison between the two SOI technologies proves that the ELO and CLSEG material is of at least as good if not better quality than that of SIMOX. Effective hole mobilities in the excess of 300 $cm^2/V\text{-}sec$ were obtained on thin-film ELO and $\mu_{p,eff}$ values of greater than 240 $cm^2/V\text{-}sec$ were extracted from the thin-film CLSEG devices.

A new linear sweep technique to measure generation lifetimes in thin SOI films has been developed. The measurement technique uses fully-depleted or partially depleted MOSFETs as the test structure. A detailed analytical formulation that involves the solution of Poisson's equation as applied to a fully-depleted SOI structure is presented. The analytical solutions are used to simulate the behavior of the SOI devices under the proposed linear sweep conditions. Finally, the linear sweep technique is applied to fully-depleted devices fabricated on SIMOX material and an average lifetime of 2μs is extracted from devices across the wafer.

The effects of volume inversion in thin-film short-channel SOI MOSFETs and the efficacy of dual-gate operation in enhancing their device performance have been analyzed using two-dimensional device simulations and one-dimensional analytical computations. In the strong inversion regime, the analyses suggest that when compared at constant V_G-

V_T values, the dual-channel volume inverted devices do not offer significant current-enhancement advantges, other than that expected from the second channel, over the conventional single-channel devices for silicon film thicknesses in the 0.1μm range. In its support however, two-dimensional simulations suggest that dual-gated devices are more immune to short channel effects than conventional single-gated devices. In this regard, a novel process sequence to fabricate self-aligned dual-gated MOSFETs is presented.

CHAPTER 1
INTRODUCTION : BICMOS AND SOI

1.1 Introduction : The Paradigm of High Density and High Speed

CMOS circuits hold a position of prominence in the semiconductor industry. Literally thousands of semiconductor ICs utilize the CMOS technology to achieve a myriad of functions and applications. These range from simple logic gates to memory cells to complex microprocessors. At the heart of the CMOS technology are of course the independent n-channel and pchannel MOSFETs. The simplicity in the design and fabrication of the MOSFETs and their easy adaptability to aggressive scaling were instrumental in pivoting CMOS circuits to their current position as a technological giant. In addition, CMOS circuits maintain very low power dissipation levels which makes CMOS the technology of choice in most memory and VLSI applications. However, the weak link in CMOS circuits is their speed performance. MOSFETs have low transconductances and hence low current driving capabilities. The low drive currents limit the speed with which the load capacitance are charged and discharged. Hence the maximum allowable switching speeds are limited. It is this niche that the faster ECL bipolar circuits completely occupy. The ECL circuits use bipolar junction transistors (BJTs) as their core drive element. BJTs have high current handling capabilities and thus circuits incorporating them operate at higher speeds compared to CMOS circuits. However, ECL circuits require a significant amount of static power arising from the necessity to maintain the bipolar transistors in the ON state ($V_{be} \approx 0.7V$). These power dissipation levels cause excessive device heating and demand the presence of sufficient heat sinks around the individual devices. Bipolar devices, for the aforementioned reason, cannot be integrated too extensively and consequently ECL circuits do not achieve very high integration levels. In a simplistic conclusion, whereas CMOS circuits enjoy a wide repertoire of applications due to their high integration levels and low power dissipation, their poor dynamic performances hamper their use in high speed circuits. ECL circuits fit the bill perfectly in so far as speed is concerned but fall palpably short in high integration requirements.

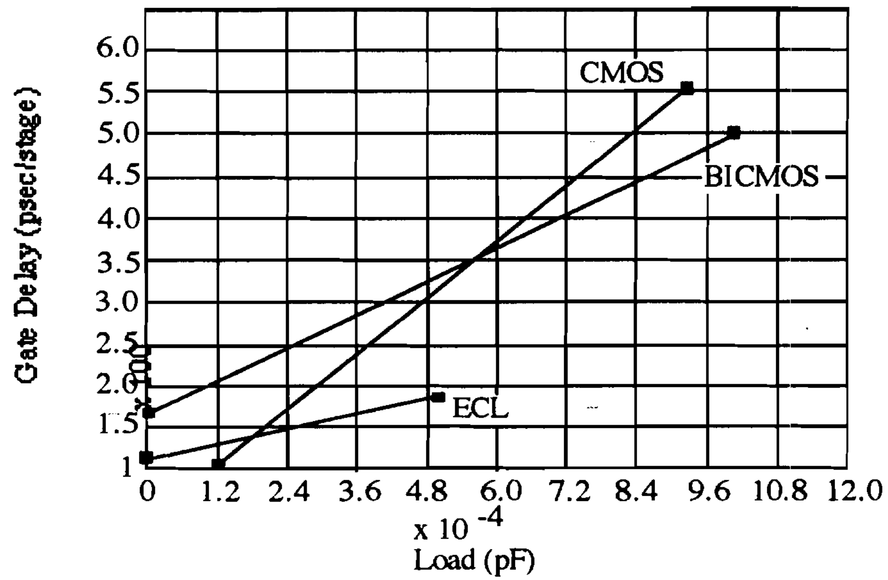
1.2 Rudiments of BiCMOS

BiCMOS (Bipolar and CMOS) has been an emerging technology in recent years [1]. As the name aptly suggests, BiCMOS is an appropriate merger of bipolar and CMOS technologies. The aim is to combine the advantages of the two, i.e.. the high integration densities and the low power consumption of CMOS and the high speed capabilities of the bipolar. The paradigm of high speed or high density thus metamorphoses into an opportunity to achieve both speed and density via a BiCMOS process. BiCMOS technologies attempt to fill the void left at the high-speed high-integration levels. By retaining the benefits of Bipolar and CMOS, BiCMOS is able to achieve VLSI circuits with speed-power-density performance previously unattainable with either technology individually.

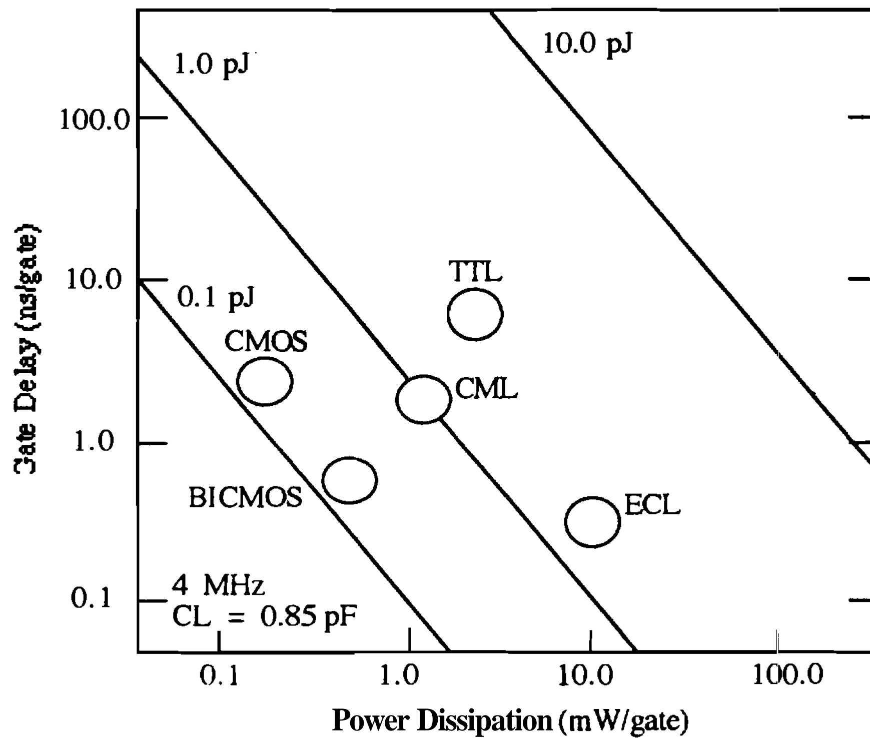
CMOS technology maintains an advantage over Bipolar in power dissipation, noise margins, packing densities and the ability to integrate large complex functions with high yields. Bipolar technology has advantages over CMOS in switching speed, current drive per unit area, noise performance, analog capability and I/O speed. It follows that BiCMOS technology offers the advantages of (1) improved speed over CMOS , (2) lower power dissipation than the Bipolar (which simplifies packaging and board requirements), (3) flexible I/O's (TTL, CMOS or ECL) - this point is significant given the growing importance of ECL I/O, historically the exclusive domain of Bipolar technology for high speed systems, (4) high performance analog integration and (5) latch-up immunity.

Figure 1.1(a) compares the gate delays for typical CMOS, BiCMOS and bipolar (ECL) technologies. It is clear that whereas BiCMOS is a definite improvement over CMOS, it is still a slower technology compared to ECL. The bipolar ECL market has historically pursued speed 'at all cost'. Thus when the power budget is unconstrained, a bipolar technology optimized for speed will almost always be faster than a BiCMOS technology. However in applications where a finite power budget exists, the ability to focus power where it is required usually allows BiCMOS speed performances to surpass that of the Bipolar [2]. This aspect of BiCMOS is made clear in fig. 1.1(b) which depicts the gate delays for the different technologies and their respective power dissipation. The compromise achieved by BiCMOS vis à vis gate delay and power dissipation is apparcnl.

CMOS technology has in recent years been aggressively scaled to sub-micron dimensions. Reduced gate lengths increase the available drive current which results in



(a)



(b)

Figure 1.1 (a) Variation of the propogation delay per gate versus the load capacitance for CMOS, BiCMOS and ECL and (b) Depicted trade-offs for the various technologies vis à vis gate delay and power dissipation

improved speed in circuits where the capacitive load is dominated by the extrinsic capacitance. However further scaling of CMOS technology is currently too expensive for the speed advantages it can offer. For the same increment in cost bipolar devices can be introduced into the process providing high capacitive load drive capability that is unmatched by state-of-the art scaled CMOS technology. As an example motivating the use of BiCMOS, figure 1.2 shows a typical memory access path in a Static Random Access Memory (SRAM) implemented using BiCMOS. The row and column decoders and the memory cells require high levels of integration in order to achieve the large memory requirements. Consequently these units in the SRAM are fabricated using the CMOS technology. However the sense circuitry and the inputloutput (I/O) periphery determine to a large extent the access time. (The propagation delay through the array is comprised of the word line delay, bit line delay and the sensing/amplification delay). Hence the I/O periphery and the sense circuitry are fabricated in ECL for greater speed. Bipolar differential pairs provide the high gain and input sensitivity required to quickly sense small differences in bit line swings. Such a merger of ECL and CMOS within a single chip is typical of BiCMOS designs, and is indicative of the compromise achieved between high integration and high speed. 64K SRAMs utilizing novel BiCMOS designs and incorporating ECL I/Os have been fabricated with access times as low as 38ns with a maximum power dissipation of just 750mW. Comparable SRAMs fabricated in ECL typically dissipate upto 6.5W of power [3].

In addition to improving circuit performance, BiCMOS lends circuit designers an additional degree of freedom in designing novel circuits by allowing the presence of both bipolar transistors and MOSFETs on the same chip. BiCMOS technology is especially well suited for I/O intensive applications. ECL, TTL and CMOS input and output levels can be easily generated with no speed or tracking consequences. The rail to rail swings and unterminated environment used in CMOS makes output switching above 33 MHz difficult. BiCMOS's inherent compatibility with ECL or TTL levels provides an ideal solution to these problems.

1.3 BiCMOS Process Technology

Although the true power of BiCMOS rests with the circuit designer, the emergence of BiCMOS has caused a proliferation of fabrication processes of varying

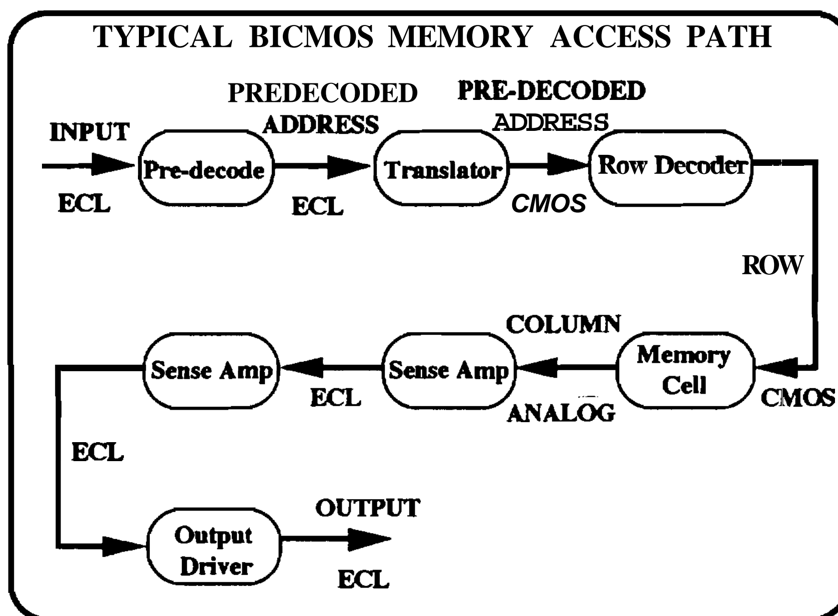


Figure 1.2 An Example of BiCMOS - a typical implementation of a BiCMOS SRAM

complexities. BiCMOS technology can be broadly classified into three groups : 1) high performance 2) low cost and 3) analog compatible. In the low cost approach, the focus is on CMOS process optimization. Bipolar devices added to the process typically don't have a buried collector and are relatively low performance devices. The idea is to compromise the NPN performance for the sake of minimizing manufacturing costs and maintaining compatibility with existing CMOS processes. The added number of process steps is kept to a minimum. One of the key aspects in a manufacturing environment is to maintain exactly the same performance for the CMOS devices so that the CMOS process files do not have to be altered. The third category of analog compatible devices differ in their requirements from the first two categories. Design rules typically do not have to be scaled as aggressively - 1.5μm-2.0μm rules suffice for most applications. High performance analog technology requirements include higher voltages (10-15V), additional components such as precision capacitors and resistors and high performance

PNPs. This implies using thicker gate oxides which reduces the digital CMOS performance. The first category is the high performance and high speed category and is by far the most complex technology. Both CMOS and bipolar device performances are typically optimized for applications in large gate arrays, memories and microprocessors. The rest of this section covers the synthesis of a high performance BiCMOS process.

There are two distinct ways to approach BiCMOS process design. One is to start with a standard CMOS process and modify it to incorporate a bipolar transistor (CMOS-based process). The other complimentary technique is to start with a set bipolar process (bipolar-based process). There is no 'correct' approach as long as the two techniques yield high-performance MOSFETs and BJTs commensurate with high performance digital circuits. However for high performance LSI and VLSI digital circuit applications, BiCMOS technology is predominantly driven from a CMOS processing base. LSI and VLSI digital BiCMOS circuits tend to be CMOS-intensive because of power dissipation limitations (for example, high density ECL I/O SRAMs). The CMOS-intensive nature of these circuits requires a process technology that results in the highest possible CMOS performance. Consequently, the BiCMOS process fabrication tends to be CMOS-based, and the process steps required to fabricate a high-performance bipolar transistor are merged with a core CMOS process flow [4-6].

A number of factors aid the integration of high-speed bipolar devices into a CMOS flow. One of the major factors is that structural requirements for realizing high-performance CMOS and bipolar transistors have tended to converge. For example, silicidation is a common requirement for CMOS and bipolar to reduce sourceldrain resistances and emitter/base resistances. Similarly, both CMOS and bipolar require heavily doped N^+ buried layers, albeit for different reasons. N^+ buried layers are common features in bipolar processes and aye introduced to minimize collector resistance. The buried layer when placed under the n-wells in CMOS circuits help reduce latch-up susceptibility. In the following paragraphs, we shall metamorphose a high-performance BiCMOS process from a base CMOS process.

The development starts with a basic n-well CMOS process as illustrated in fig. 1.3. The NMOS device is built in a thick P^- - epitaxial layer on top of a P^+ substrate. The PMOS transistor is built in an implanted N-well. The P^+ substrate is used to reduce latch-up susceptibility. A first order modification to the process involves the introduction of a simple triple-diffused emitter bipolar transistor. The process uses the N^+

sourceldrain (SID) implant to form the bipolar transistor's emitter and shallow collector contact. The P+ - S/D implant forms the extrinsic base contacts. The process requires one additional masking step to introduce the intrinsic base. This process cross-section is shown in fig. 1.4. From a bipolar standpoint, this simple approach has a number of limitations. The most significant of these is the lightly doped PMOS N-well that is used to form the bipolar collector. The low doping concentration leads to a large collector resistance, which limits the usefulness of the bipolar transistor. The next iteration involves the addition of a buried-layer and a deep n+ - sinker; both steps act to reduce the collector resistance and hence improve the performance of the bipolar transistor. In addition the epitaxial layer is grown n-type instead of p-type, so that the epitaxial layer doping now determines the collector doping. The p-channel MOSFET is formed in the n-epitaxial layer while the n-channel MOSFET requires a p-well implant. The n+ - buried layer is introduced for the p-channel MOSFET to reduce the possibility of latch-up. The resulting device structure is shown in fig. 1.5. This process requires two more masking steps, one each for the buried layer and the deep n+ - implant. The significant aspect of this iteration step is the change in the epitaxial layer doping to optimize the collector design of the bipolar transistor. The above approach, although producing a bipolar device with much improved characteristics, still has a number of drawbacks. In particular, the packing density of the bipolar devices is limited by the P- - substrate doping level that must be used to prevent punch-through from one bipolar device collector to another. Raising the doping level of the P- - substrate, while allowing the bipolar devices to be more closely spaced, causes increased collector to substrate capacitance. Also the N-type epitaxial layer has to be counter-doped to isolate the N-well regions and to form P-wells for the NMOS device. Counter doping can cause a reduction in NMOS performance through mobility degradation.

An improvement in bipolar packing density can be made by using self-aligned twin buried layers. The process cross-section is illustrated in figure 1.6. This allows the collector-collector spacing to be reduced at the cost of increased collector-substrate sidewall capacitance. The process also incorporates a twin-well CMOS process without heavily counter-doping the epitaxial layer. A near-intrinsic epi-layer is deposited for this reason. At the cost of an extra mask level, the bipolar device performance can be further improved by using a polysilicon emitter. In such a process, the NMOS and PMOS gates and the bipolar emitter share a common polysilicon deposition step. Four additional

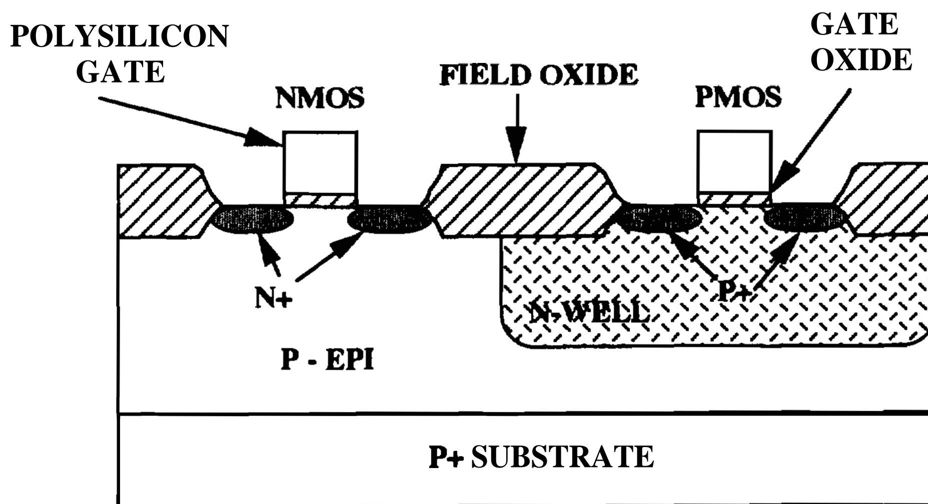


Figure 1.3 Basic N Well CMOS process cross-section

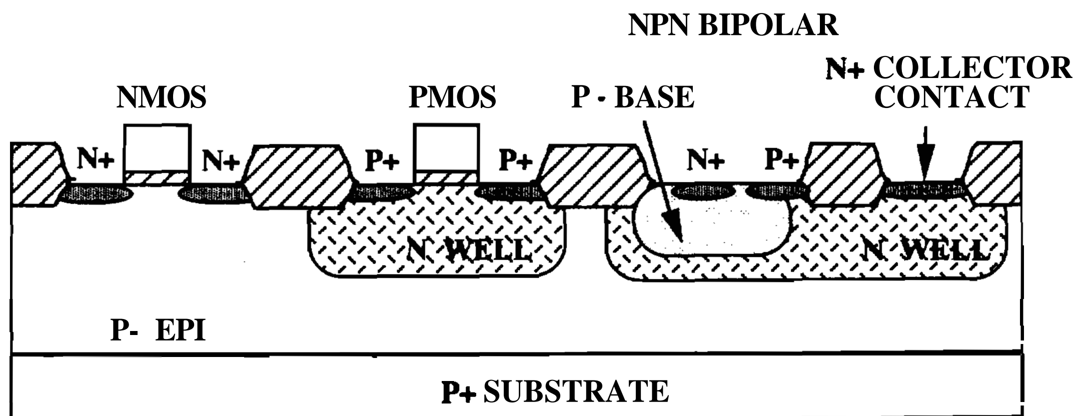


Figure 1.4 BiCMOS structure formed by the simple addition of an NPN bipolar transistor to the basic N well CMOS process

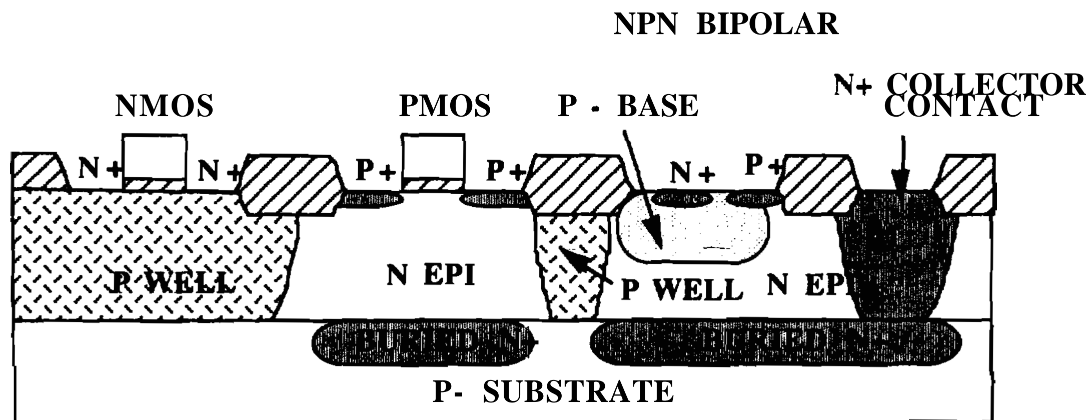


Figure 1.5 BiCMOS structure showing the addition of a buried N+ layer and deep N+ topside contact to reduce the collector resistance

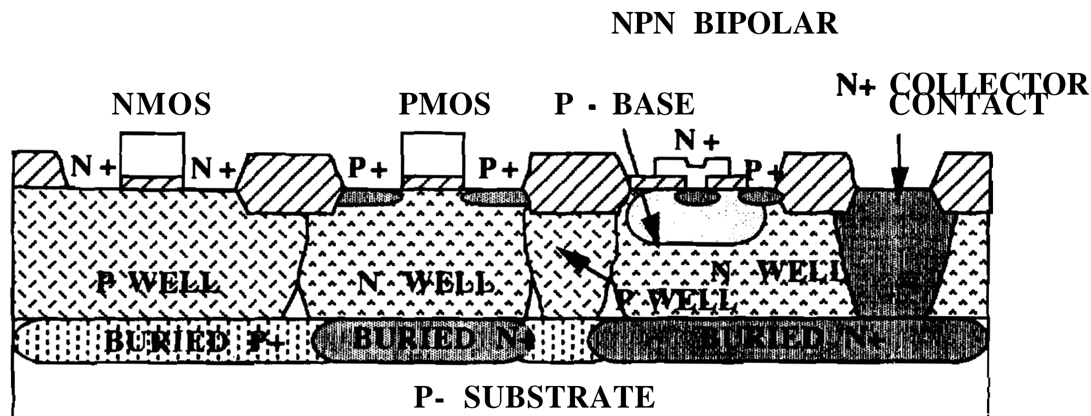


Figure 1.6 Optimized BiCMOS device structure. Key features include self-aligned P and N+ buried layers for improved packing density, separately optimized N and P wells (twin well CMOS) formed in an epitaxial layer with intrinsic background doping, and a polysilicon emitter for improved bipolar performance

masking steps are required (buried N+,deep N+, P-base, emitter) to merge this BiCMOS process with a baseline CMOS flow.

Further optimizations of the bipolar transistor and the MOSFETs are dictated by speed and reliability issues. The following modifications can be incorporated into the process shown in figure 1.6:

(i) Silicidation of all extrinsic contacts and polysilicon layers. Self-aligned silicidation (Salicide [7]) is widely used.

(ii) Sidewall oxide spacer technology is used to incorporate lightly doped drain (LDD) to prevent hot electron degradation in the NMOS transistors.

(iii) The emitter and base regions of the bipolar transistor is self-aligned to reduce device parasitics and enhance performance.

(iv) Trench isolation is used to increase the packing density and reduce the collector-substrate capacitance.

(v) Source/drain and base junction areas can be reduced through the use of local interconnects. Higher packing densities and lower capacitances can be achieved, leading to increased chip density.

A fully optimized high performance BiCMOS process is illustrated in figure 1.7. The sketch is one among an anthology of BiCMOS processes. However it typifies the fabrication processes involved and the final device structures obtained. The design considerations involved in such a process is the next topic of discussion.

1.4 Design Considerations in a BiCMOS Process

As we have stated above, BiCMOS process complexity can vary from a low-end cost-efficient process, to a high-end complex process in which all devices are optimized for maximum performance. The question often arises, "How good does an NPN have to be for a given set of MOSFET parameters and vice versa?". The answer is primarily determined by circuit requirements. Consider MOSFETs for example. For FETs speed depends on device parameters such as saturation current (I_{dsat}) and intrinsic (C_{int}) and extrinsic (C_{ext}) capacitances. These parameters in turn depend on oxide thickness, channel length and bulk doping. However in FET circuits scaling the oxide thickness does not increase speed for circuits dominated by C_{int} because both I_{dsat} and C_{int} increase at approximately the same rate. For C_{ext} dominated circuits on the other hand, scaling the

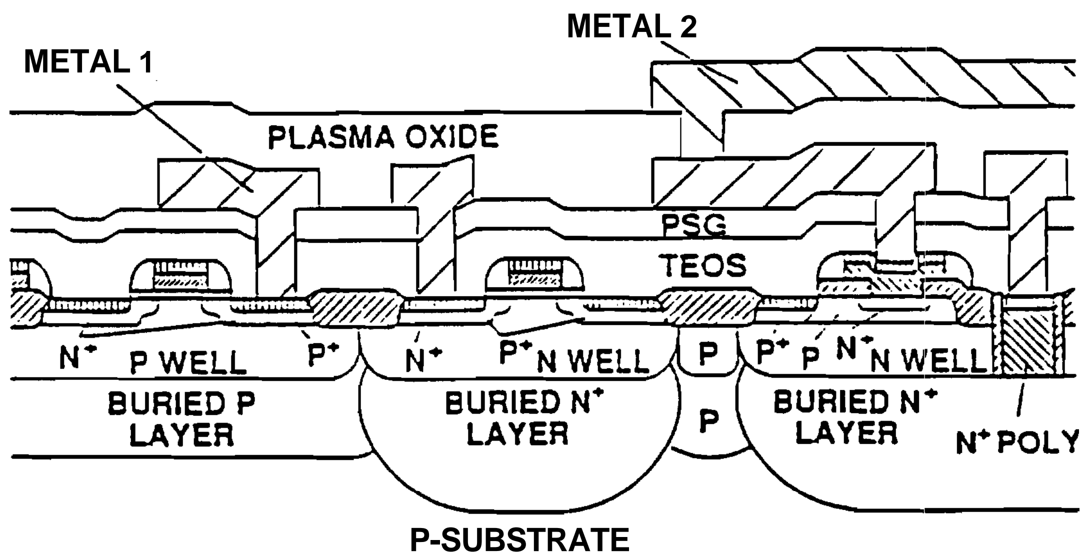


Figure 1.7 **Fully optimized, high performance BiCMOS fabricated by Texas Instruments. The process is compatible with a 0.5mm technology [IEDM '88, pp. 756]**

oxide thickness and channel length will improve the circuit speed. Thus in a BiCMOS circuit, if relatively low performance NPNs are used for primarily driving I/Os, then high-performance FETs will be required to drive the large extrinsic capacitances associated with the NPNs. This can be achieved by scaling the oxide thickness to increase I_{dsat}. Conversely, if high-performance self-aligned bipolar transistors are used, then the requirements on the MOSFETs can be relaxed [8].

To a large extent process design in BiCMOS is dictated by device design which in turn is dictated by circuit requirements. The impact of various process parameters on key device parameters for MOSFETs and BJTs are summarized in Tables 1.1 and 1.2 [1]. Tang and Soloman [9] have proposed a method for NPN device and process design which is depicted in figure 1.8. Circuit requirements determine the current density of the device. This sets the minimum collector doping and the maximum epi-thickness based on Kirk effect considerations. The current density also sets the maximum doping allowed due to the required current gain. Optimization of the base profile is driven by R_B, β and base transit time considerations. In general, a similar scheme can be followed for MOSFETs. However the criteria listed in Tables 1.1 and 1.2 highlight impacts of process parameters on device requirements for good CMOS and bipolar transistors taken individually. When the two processes are merged into a single BiCMOS process, a number of compromises are involved. Performance compromises can be minimized but at the expense of increased process complexity. Most of the compromises in performance are determined by choices made in the front-end development of the process, where the strongest coupling between device characteristics occurs.

1.4.1 Front-end Design Issues

As discussed briefly in section 1.3, there are a number of front-end design options available in designing a BiCMOS process. Front-end design involves choice of well doping concentrations, choice of N-epi or P-epi, choice of N-well or P-well processes, triple diffused process and the twin-well process with intrinsic epi. When epitaxy is chosen as a possible option, the front-end design also determines the epi-doping, buried layer considerations such as autodoping and the choice of epi-layer thickness. Table 1.3 summarizes the front-end design options and ranks the performance of the NPNs and MOS transistors as well as the ease of implementation and latch-up susceptibility [10].

Table 1.1 Primary Process Parameters and the Resulting Impact (Increase or Decrease) on the Key Electrical Characteristics of a MOSFET

		Vt Adjust				
Output	↓ tox	↑ Dose	↓ E	↓ Dt	↑ Nbc	↓ xj
Threshold Voltage	↓	↑	↑	↑	↑	↑
Body Effect	↓	↑	↓	↓	↑	↑
Transconductance	↑	↓	↓	↓	↓	↓
Subthreshold Slope	↓	↑	↓	↓	↑	↑
Short Channel Effect	↓	↓	↑	↑	↓	↓
Gate-Drain Capacitance	-	↑	-	↓	↓	↓
Series Resistance	-		-	↑	-	↑
Junction Capacitance	-	↑	↓	*	↑	↓
Hot Carrier Injection	↑	↑	↑	↑	↑	↑
Breakdown Voltage	↓	-	-	↓	↓	↓

* depends on the Nbc profile

Table 1.2 First Order Effects on NPN Parameters for Increasing Q_b, W_b and Q_c

Parameter	↑ Q_b	↑ W_b	↑ Q_c
I_C	↓	↓	-
β	↓	↓	-
R_B	↓	↓	↑
R_C	-	-	↓
I_K	↑	↓	↑
f_T	↓	↓	↑
V_A	↑	↑	-
V_{PT}	↑	↑	-
BV_{cbo}	-	-	↓
C_E	↑	-	-
C_C	-	-	↑

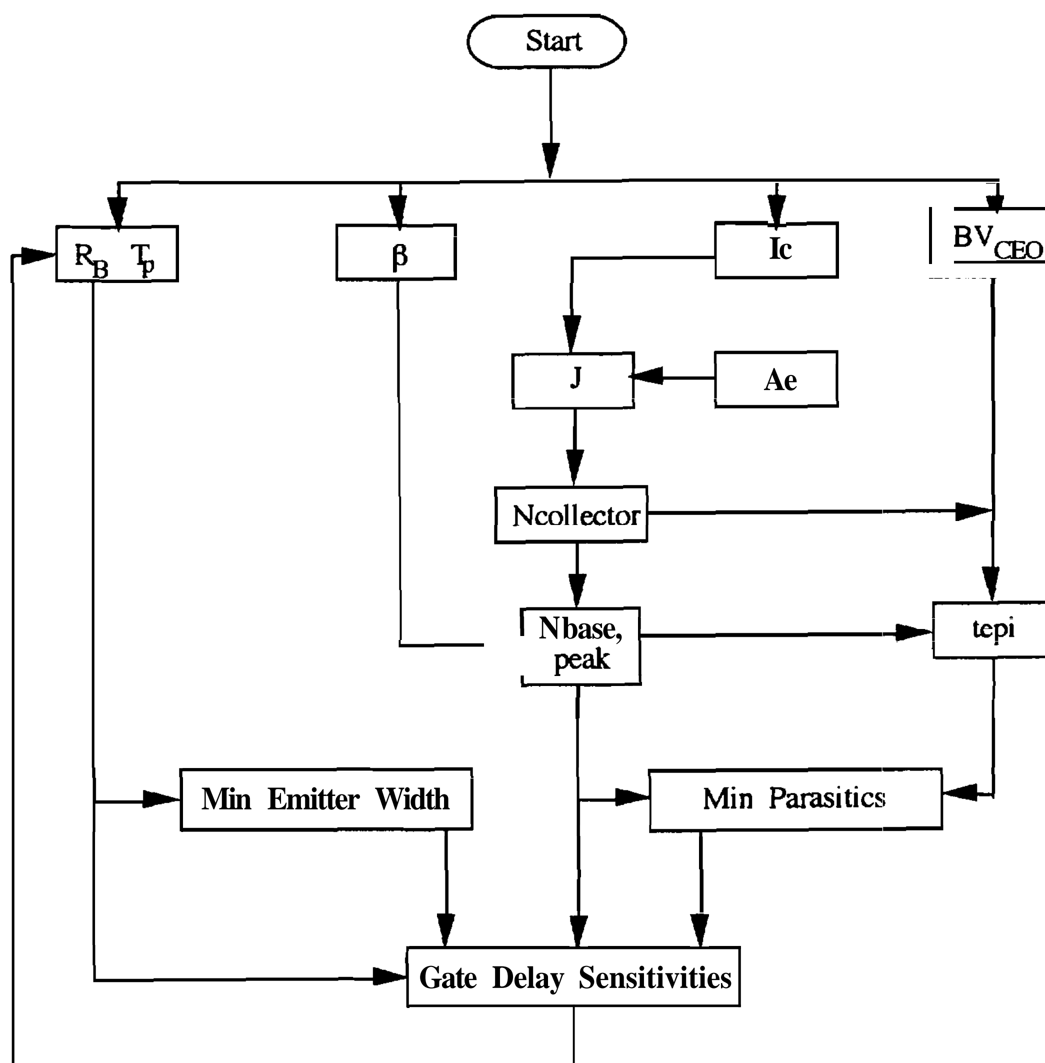


Figure 1.8 First Order NPN device design. The vertical profile is set to optimize device delay, while optimal horizontal design minimizes the parasitics [19]

Table 1.3 Ranking for Different BiCMOS Front-end Options
(1 is the best [10])

Front-End	Simplicity	CMOS	NPN	Latch-up
Triple-diffused	1	1	5	5
P-epi/N-well	3	3	2	2
N-epi/P-well	2	3	4	4
N-epi/Retro P-well	4	5	4	3
π-epi/Twin well	5	2	2	3

The triple-diffused option as seen earlier in figure 1.3 offers ease of implementation and compatibility with CMOS technology. This is obtained at the expense of NPN performance. By and large, the use of an epitaxial layer based process is essential for high-performance BiCMOS. For CMOS, the epi improves latch-up immunity, decreases the impact of substrate current and improves alpha-particle immunity in memories [10]. The bipolar transistors benefit from reduced collector resistance and suppressed Kirk effect. Thicker lightly doped epi is preferred for CMOS while optimal NPNs are obtained with a thinner more heavily doped epitaxial layer. Moreover parameters chosen for the epitaxial layer are strongly dependent on well doses, buried layer doses and well drive time for the process. Thus the optimization of epi-parameters becomes a formidable task.

Most of the front-end design constraints and compromises arise from the fact that the bipolar transistor and the MOSFETs share the same epitaxial layer.

(a) Epitaxial layer thickness : Optimal epi-thickness becomes a strong function of the particular circuit performance requirement. Depending on these requirements, the epi-thickness can be chosen to either optimize the NPN performance or the FET performance.

The bipolar transistor will set a minimum allowed thickness determined by BV_{CEO} constraints. Because of the P^+ - buried layer that is used underneath the NMOS to electrically isolate adjacent N-well tubs and reduce latch-up, the epi must be thick enough to prevent the out-diffusion of the P^+ - buried layer from excessively increasing NMOS junction capacitances and the body-effect of the NMOS transistors. On the other hand, a thick epitaxial layer degrades f_T and increases the collector resistance which would increase propagation delay. In addition, the knee current of the bipolar transistor (I_K) also decreases. This is reflected in figure 1.9 which depicts the gate delay as a function of epi-layer thickness.

(b) N-well doping profile and dose : The n-well diffused either into P-epi or π-epi forms both the collector of the bipolar transistor as well as the background doping for the p-channel MOSFET. Clearly the n-well dose and the profile constitute critical process parameters. The required n-well dose is tightly constrained by a number of conflicting needs. To control the PMOS short-channel effects, the well dose must be sufficient to prevent DIBL. A well doping of 1e16 $/cm^3$ or more underneath the base: is necessary to suppress base push-out and minimize the collector resistance of the NPN. If the N-well is used to set the PMOS field threshold then an additional constraint occurs based on the lowest doping that is acceptable at the surface. However excessive N-well dose is detrimental to PMOS body-effect considerations and to junction capacitances as well as to the collector-base capacitance of the NPN.

In figure 1.10 the general BiCMOS device design methodology is illustrated [11]. The complex procedure involved due to the conflicting needs of the CMOS and bipolar is immediately obvious.

1.4.2 Latchup in BiCMOS Processes

Latchup in CMOS circuits is a well known and well understood reliability concern. Latchup propensities in CMOS circuits fabricated in a BiCMOS process are severely reduced due to the incorporation of twin buried layers under the twin wells. In addition, the n-well resistance is significantly lowered in a BiCMOS process because of the requirements of the bipolar. Reduced beta of vertical PNP transistors because of the presence of the buried layer and the lower N-well resistance are the two major reasons for the significantly superior latch-up immunity of a BiCMOS process.

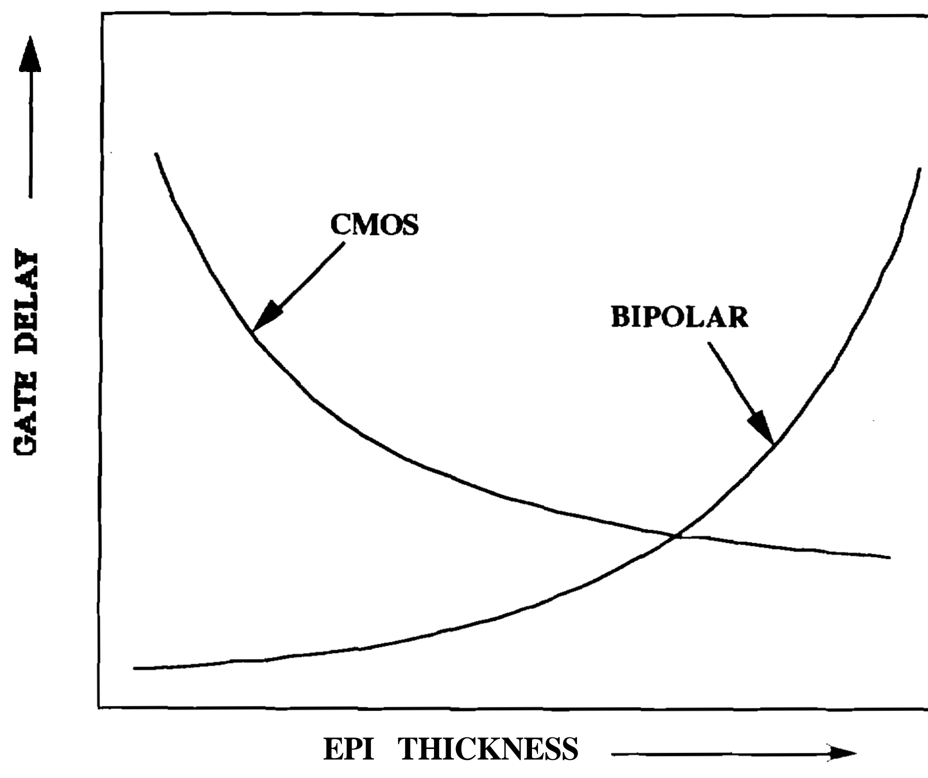


Figure 1.9 Qualitative plot of gate delay for CMOS and Bipolar ring oscillators with varying epitaxial layer thickness

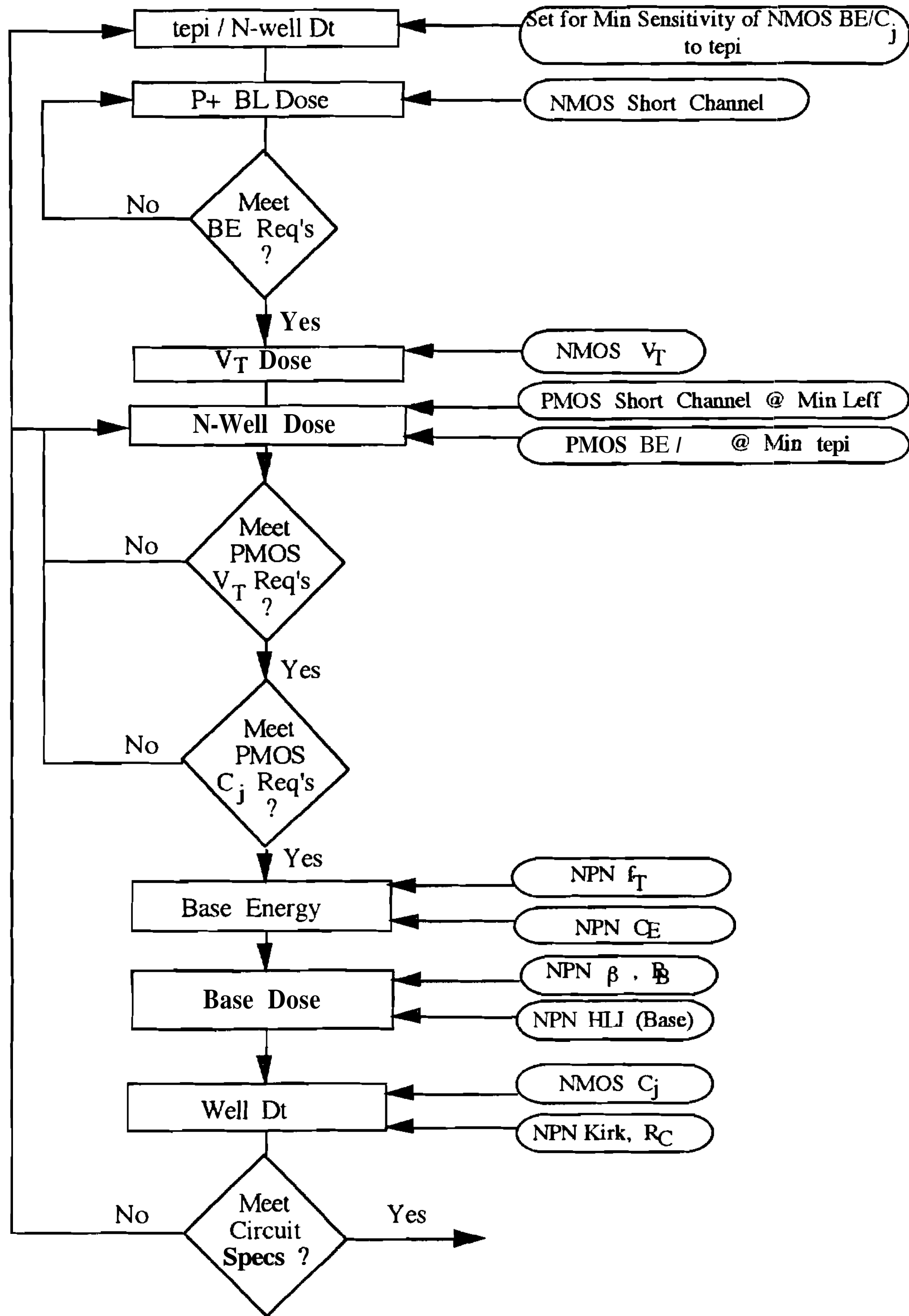


Figure 1.10 BiCMOS device design methodology derived from Response Surface Methods [11]

Certain merged CMOS/bipolar structures in a BiCMOS circuit tend to be susceptible to latchup and this reduces the design flexibility by requiring more design rules. Illustrated in figures 1.11(a) and 1.11(b) are two typical merged bipolar/CMOS structures that are susceptible to latchup. In fig. 1.11(a) at high collector currents the NPN collector could potentially enter quasi-saturation. This results in the C-B junction being forward biased which in turn injects holes in the substrate. The holes form the base current for the parasitic NPN in the SCR latch and turn on the NPNP path. In fig. 1.11(b) a very common merged device is depicted. The drain of a PMOS transistor is merged to the base of a bipolar device. Such devices have been shown to yield superior performances in BiCMOS circuits [12]. Once the PMOS transistor is turned on, the high voltage at its source appears at the base of the NPN device and establishes a current flow through it. The SCR action in this case is between the vertical NPN and lateral PNP. The collector current then continues to flow even after the PMOS is turned off.

Therefore even in conventional BiCMOS circuits reliability concerns place further restrictions on process parameters and accentuate the already existing compromises discussed in the earlier section.

1.5 Silicon-on-Insulator for BiCMOS Applications

In section 1.4 the complexities in the design and implementation of a conventional BiCMOS process were discussed in some detail. A host of compromises and process parameter restrictions were seen to be a direct consequence of the fact that the CMOS devices and the bipolar devices were fabricated in the same epitaxial layer. If it were possible to fabricate the MOSFETs and bipolar transistors in separate individual epitaxial layers, then each of the design constraints and compromises highlighted in the previous section would be substantially relaxed. The BiCMOS device design methodology of figure 1.10 would also be dramatically simplified. It would then become possible to independently control and tune the CMOS and bipolar devices in order to attain the best performances for the combined BiCMOS technology.

Silicon-on-Insulator (SOI) processes allow MOSFETs and bipolar transistors to be fabricated in separate epitaxial islands. A simplified process sequence demonstrating the integration of SOI MOSFETs into a BiCMOS process is shown in figure 1.12. A

(a)

(b)

Figure 1.11 (a) Latchup in a merged CMOS/Bipolar device and (b) Latchup of a merged PMOS and NPN bipolar transistor structure in the same N-well

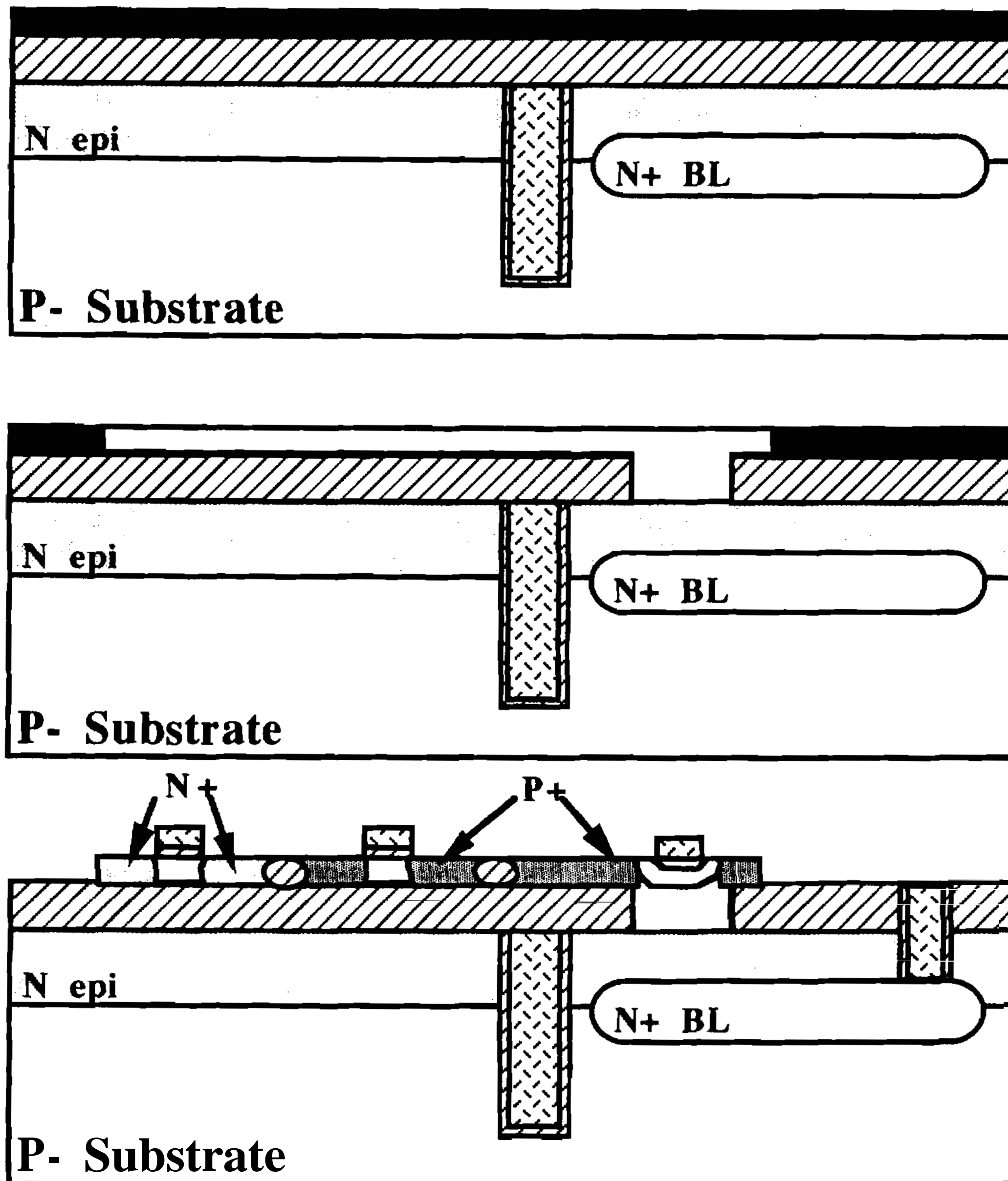


Figure 1.12 Quasi-SO1 BiCMOS process with CMOS and Bipolar fabricated in independent epitaxial regions ; a significant simplification of the process results

significant feature of the process is its 'quasi-SOI' nature. That is, the MOSFETs are fabricated on SOI material, while the bipolar transistor is fabricated in the bulk substrate.

Such a merger of bulk and SOI is indispensable because of the difficulty in fabricating high performance bipolar transistors in thin-film SOI material. The process highlights the advantages of combining SOI MOSFETs with conventional bipolar transistors.

SOI device islands for MOSFETs significantly simplifies the isolation between devices in the proposed quasi-SO1 BiCMOS process. Due to the ultra-thin nature of the SOI films, LOCOS isolation is extremely easy to implement and birds beak effects are reduced to a minimum. Epitaxial growth can be optimized for the bipolar transistor in terms of both the epi-layer doping and thickness. The SOI layer thickness can be independently achieved by chemical-mechanical planarization. The SOI CMOS process has no wells to be concerned about and therefore the compromises made in the conventional BiCMOS process flow vis à vis well dose and well drive times are avoided. The presence of the buried oxide layer and the thin nature of the SOI film provides a natural protection against latch-up. There are no buried layers required for the MOSFETs. This again simplifies the epitaxy process because boron out-diffusion does not have to be accounted for when analyzing process options. The twin buried layers inherent to a conventional BiCMOS structure complicate the epitaxy process, since vertical and lateral autodoping effects must be considered for both N and P well regions. Autodoping is a very severe concern especially for near intrinsic epi-growth, more so for thinner epitaxial layers. In addition to the conventional CMOS latchup immunity, the SOI devices also prevent the latchup susceptive SCR paths discussed in figures 1.11. Merged bipolar / CMOS circuits can be designed without any specific design rules. This would increase packing densities. One of the most common design rules for reducing latchup is providing body ties, which take up a lot of silicon area.

The SOI MOSFETs fabricated in the quasi-SO1 BiCMOS process have reduced peripheral junction capacitances. They promise faster operating speeds as compared to bulk MOSFETs. Moreover recent studies on thin-film SOI MOSFETs indicate improved immunity to short-channel effects and enhanced device performance for SOI MOSFETs as compared to conventional bulk MOSFETs. The properties of SOI MOSFETs will be considered in greater detail in the next chapter.

In thin-film SOI MOSFETs the threshold voltage is typically controlled by the gate work function. The CMOS threshold implant schemes are also simplified as the thin films result in uniform doping profiles. Since SOI MOSFETs show great short-channel immunity, retrograde doping to prevent bulk punch through can be avoided. A common processing factor between the SOI MOSFETs and conventional FETs is the LDD requirement to reduce hot-camer generation and improve device reliability. All bipolar process steps can be optimized for the bipolar without compromising the CMOS devices, following the design procedure shown in figure 1.8.

Finally, there are a large number of applications for BiCMOS technology which will result in a single chip straddling the analog-digital boundary. In such circuits the greater part of the silicon area, utilizing CMOS, will be used for the digital signal processing of signals. A much smaller portion will be devoted to the essential analog processing needed to interface with the outside world. Both analog and digital circuits fabricated on the same chip results in the most efficient use of silicon. In mixed-mode analog-digital circuits BiCMOS provides the high gain of bipolars, the low input offset voltages of differential pairs and also high input impedance FETs. A major concern in such a mixed mode process is the probability of crosstalk between the analog and digital circuitry through the substrate. Analog circuits tend to be extremely sensitive to noise. Digital circuits on the other hand are extremely noisy. When they are fabricated on the same substrate, the digital noise affects the performance of the analog circuitry. It has been shown that mixed mode circuits fabricated with SOI substrates show a lesser degree of crosstalk [13]. Thus for optimum performance the digital CMOS circuitry could be fabricated on SOI material and the lower performance but more precise analog devices can be fabricated in the substrate. Such a design again points to a quasi-SO1 BiCMOS process.

1.6 A 3-D BiCMOS Process : A Combination of SOI and Bulk Silicon Processing

With the material presented in the previous sections as the prime motivation, in this section we describe the process design of a novel 3-dimensional BiCMOS process which uses selective epitaxial growth to form the bipolar epi-layer and epitaxial lateral overgrowth to form the 'quasi-SOI' layer. Unlike the quasi-SO1 BiCMOS process illustrated in figure 1.12, the 3-D BiCMOS process includes an NMOS device fabricated

in the substrate with a PMOS load device fabricated directly over it on SOI material. This arrangement lends the process a 3-D configuration. The proposed BiCMOS process shows promise due to its 3-dimensional nature, novel improvements and compatibility with existing technology. The entire fabrication process uses 12 masks to first metallization. This is in comparison to the 20-30 masks in a conventional high performance BiCMOS process [14,15]. The vast reduction in lithography steps are due to the simplifications in the process brought about by the use of the SOI load device. Similar 3-D circuits have been proposed with the SOI load device fabricated in polysilicon deposited by LPCVD. The polysilicon active load TFT is limited in its performance by the poor mobility of the SOI material. The current drive is small and the discharging of capacitive nodes charged by unwanted radiation effects such as alpha-particles are consequently slow.

As described in the previous sections of this chapter, the integration of CMOS and bipolar technologies on the same chip allows circuit designers to take advantage of the low power dissipation of the CMOS and the high transconductance of the BJT. As a result the BiCMOS gate has a better drive capability then CMOS, while maintaining low total power consumption. Another issue in process technology design is the continuous effort to increase integration densities. In this regard three dimensional integration should provide a viable solution to improving packing densities. To address these issues, a BiCMOS process was developed which incorporates a 3-D CMOS and a high-performance bipolar transistor. The key feature of the process is the use of separate thicknesses for the epitaxial silicon layers used in making the bipolar and the CMOS. This allows independent control of the bipolar collector to emitter distance and hence the collector to emitter breakdown voltage.

The process features and the fabrication sequence are described in the next section. Results from process simulations and numerical device simulations are presented in section 1.6.2.

1.6.1 Design of the BiCMOS Process

The process uses Epitaxial Lateral Overgrowth (ELO) of silicon for 3-D integration and the inherent merging of devices. The final cross-section of the devices is shown in figure 1.13. The output of the CMOS inverter is inherently merged with the

base of the bipolar transistor. The bipolar transistor of the BiCMOS cell bears similarities to the super-self-aligned (SST) BJT. An important feature oi the bipolar transistor is the independent control of its collector-emitter breakdown voltage which allows for the design of BiCMOS circuits for speed or power applications. This is especially important for the potential use of BiCMOS in mixed-mode analog/digital applications as discussed in section 1.5. The flexible epitaxial layer thickness of the bipolar transistor stems from the fact that the active area is fabricated from a trench. The trench depth controls the epi-layer thickness and the bipolar device parameters. This also facilitates access to the buried sub-collector via an arsenic doped polysilicon layer. The novel collector contact engineering results in a significant reduction in active area and collector-substrate capacitance. The extrinsic base contact for the BJT is made of single crystal silicon and hence reduces the base resistance [16]. However this is a second order effect since after silicidation the sheet resistance of both polysilicon and monocrystalline silicon layers become comparable. The 3-D CMOS is fabricated with a dual-gated PMOS device in SOI silicon stacked over an existing NMOS device fabricated in the substrate. The use of the SOI-layer lends the process most of the advantages discussed in section 1.5. The use of local polysilicon interconnects helps reduce active area and device parasitics. The NMOS device incorporates a LDD structure which reduces hot-electron degradation by lowering the surface electric fields at the drain junction. The properties of the dual-gated SOI device will be discussed in greater detail in the forthcoming chapters. In figure 1.13, the bipolar and CMOS devices are merged into a 'cell'. While the process is described for the merged structure, the CMOS and bipolar devices could be isolated if placed farther apart or by the addition of a masking step to etch the silicon interconnect off.

One of the major drawbacks of such a process where the PMOS device is stacked directly over the NMOS transistor, is that the junctions of the NMOS device cannot be silicided. As BiCMOS is scaled to 1μm gate lengths and below, it becomes increasingly important to minimize the series source, drain, emitter, base and collector resistance in order to realize the full performance advantages of scaled devices [17]. For MOS transistors, the channel conductance increases as the gate length decreases, and unless the sourceldrain series resistance is reduced, the saturation transconductance will be degraded. For an NMOS transistor with an effective channel length of about 0.5μm, the total source/drain series resistance must be reduced to approximately 1.2KΩ-μm, or the

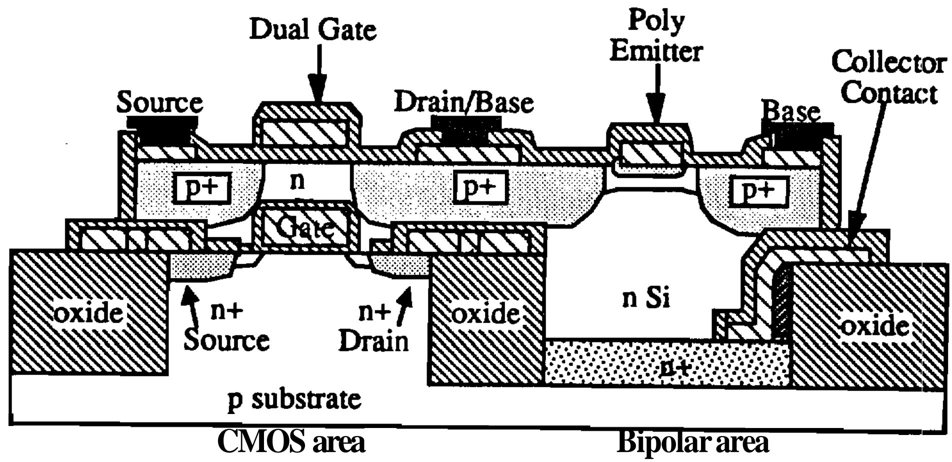


Figure 1.13 **Final device cross-section of the 3D BiCMOS process incorporating a merged PMOS/bipolar device**

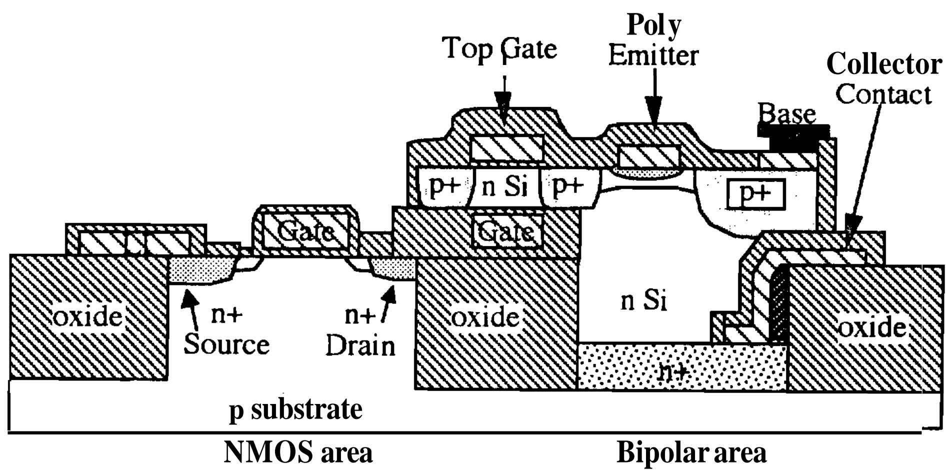


Figure 1.14 **A modified process for the 3D BiCMOS process, that places the load transistor to the side making the NMOS transistor more accessible**

saturated transconductance will be degraded by more than 10% [17]. Fortunately the impact of the **source/drain** series resistance on the device gain as the gate length is scaled is less critical for NMOS devices than for PMOS devices because arsenic can be used to make shallow highly doped layers. For high performance applications where all the device performances must be maximized, an alternate process structure based on the same basic concepts can be used. Such a structure cross-section is shown in figure 1.14. All the essential concepts and the fabrication steps are thc same. Thc only diffcrencc is that the PMOS device is moved to the side instead of being directly on top of the NMOS device. This makes the NMOS device in the substrate more accessible.

The cross sections of the process steps are shown in figure 1.15.

(a) The process begins by using a mask to define the recessed LOCOS isolation on a p-type <100> wafer. This is the first masking step of the process. After recessed LOCOS isolation, the cross section is shown in figure 1.15(a). Trench isolation could also be used instead of recessed LOCOS.

(b) The NMOS threshold implant could now be performed without a mask. Mask # 2 is then used to cover the CMOS active area and the silicon is etched in the bipolar region using RIE or a controlled wet-etch. This forms the bipolar trench and determines the collector/base junction to buried layer distance. The cross section at this stage is shown in figure 1.15(b).

(c) The photoresist is then removed and the NMOS gate oxide is grown over the CMOS region and the buried layer. This step drives in the buried layer and heals any RIE damage.

(d) In the next step a layer of polysilicon is deposited and implanted with arsenic to form the gate of the NMOS device. The polysilicon is patterned to form the gate. After a light LDD implant, LTO sidewall spacers are then formed following the processing steps for conventional LDD process. The heavily doped arsenic source/drain regions can then be implanted. This implant step is also used to form the buried layer in the bipolar process. The structure is shown in figure 1.15(c).

(d) A second layer of polysilicon is deposited to form the local interconnects and the access to the buried sub-collector in the bipolar transistor. The polysilicon layer is doped with arsenic using implantation or insitu-doping. This poly layer will form the contact to the buried layer. The poly layer is then oxidized which drives in the sourceldrain regions.

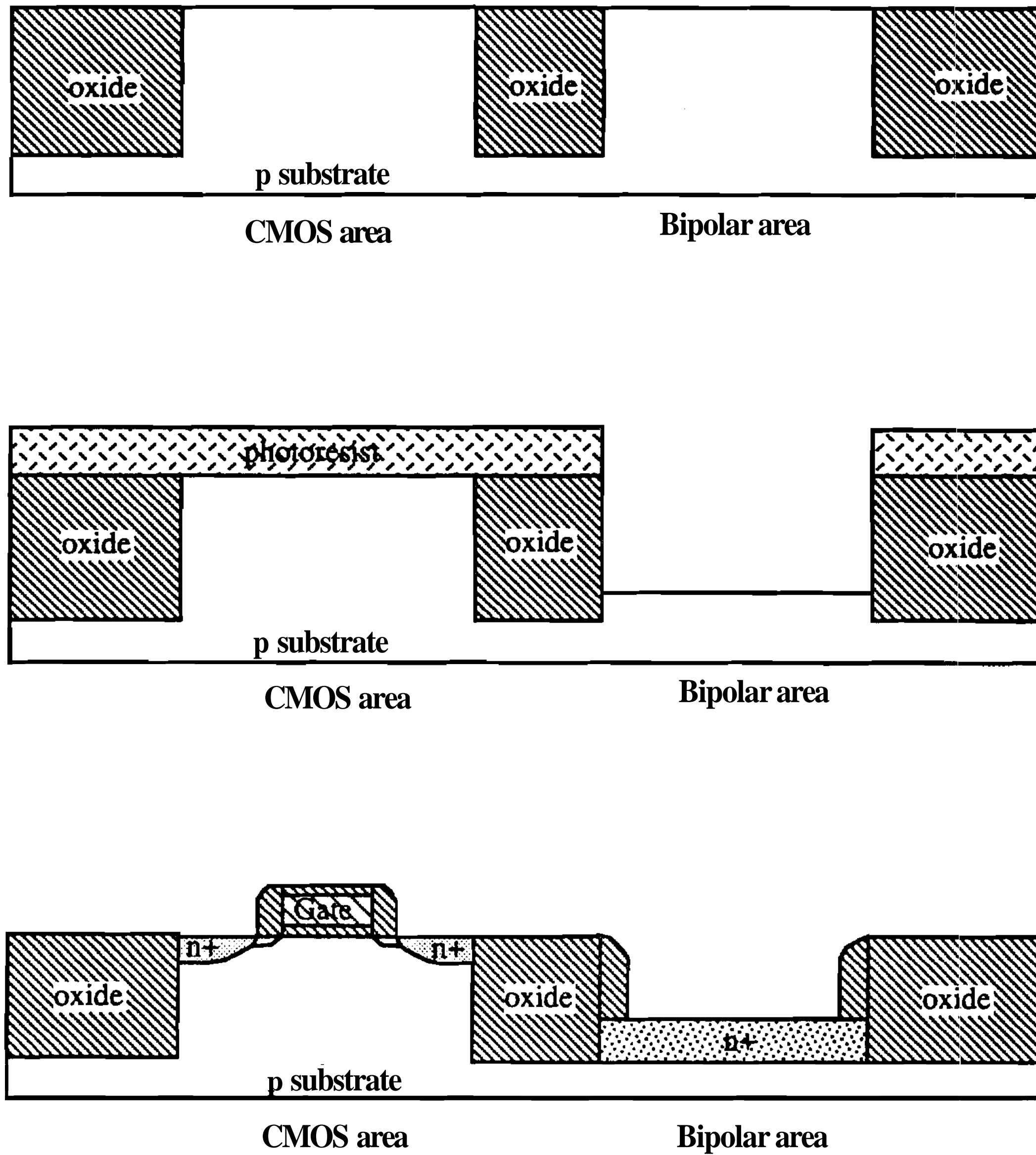
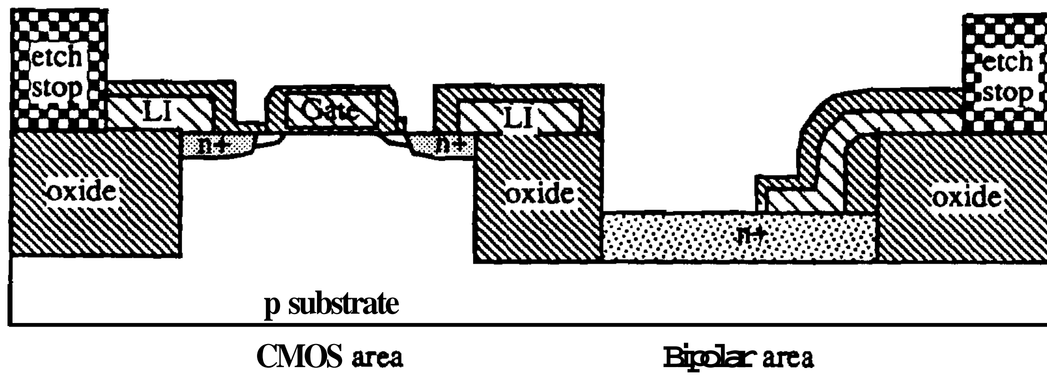
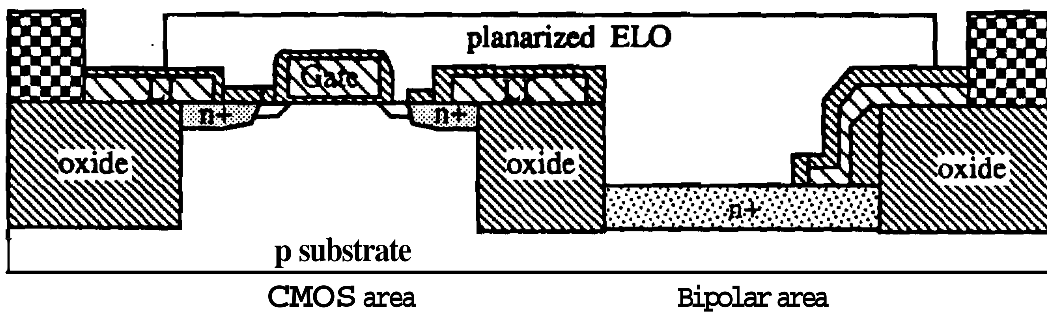


Figure 1.15 3D BiCMOS process sequence





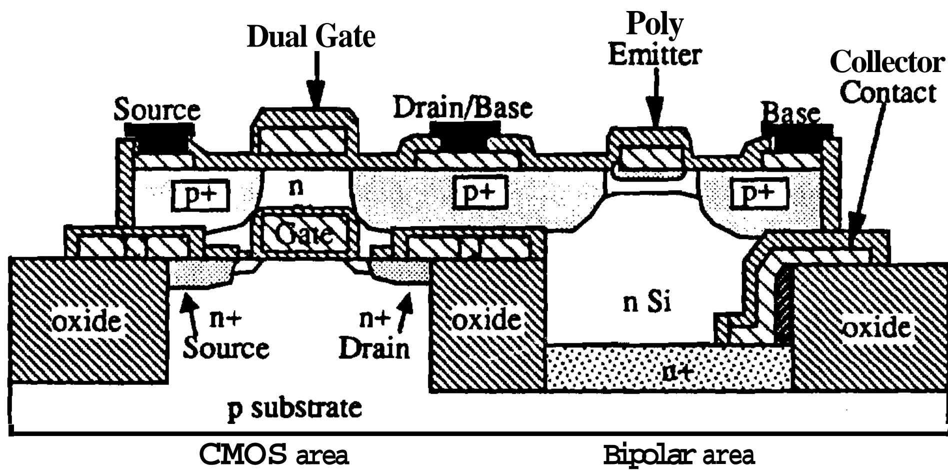


Figure 1.15, continued

(e)The poly is then defined using RIE. The sidewalls of the exposed poly layers are then oxidized.

(f) Now the top gate oxide is grown over the polysilicon gate. Then a single masking step is used to open the seed-holes in both the bipolar and the MOS regions. The wafer is now ready for selective growth of silicon as illustrated in figure 1.15(d).

(g) SEG and ELO is grown in an RF heated pancake type epitaxial reactor, using DCS as the source gas, HCl to prevent nucleation of polysilicon on exposed oxide regions and hydrogen as the carrier gas. Silicon grows from the two seed-holes and merges in the central region of the structure. The silicon is grown laterally till it completely grows over the gate. ELO silicon is then planarized using CMP and a pre-deposited etch-stop is used to stop the etch at the desired thickness. The device structure at this stage of the process is shown in figure 1.15(e).

(h) The active area is defined by mesa isolation. Gate oxidation for the PMOS top gate is performed. A non-critical mask can be used to etch the gate oxide from the bipolar regions and implanting the intrinsic base.

(l) A polysilicon layer is again deposited for the top gate and it is oxidized. Another lithography then defines the gate stack over the CMOS region and the emitter over the bipolar region. LTO spacers are formed on the gate and emitter stacks. These spacers define the link-up region in the bipolar base.

(m) An optional polysilicon layer can then be deposited and implanted with boron. This layer can be used to diffuse the heavily doped extrinsic p^+ regions. Alternately the extrinsic regions of the bipolar and the source/drain regions of the: PMOS can be implanted directly at this step.

(n) The poly layer is then defined to form the contacts which could also 'be used as local interconnect runners. Plasma oxide is then deposited and contacts are opened for subsequent metallization. The final device cross section is again shown in fig. 1.15(f).

The 3-D BiCMOS process has the following features in its structure :

(i) It has an inherently merged BJT and CMOS for reduced active area.

(ii) The CMOS is stacked in a 3-D configuration and the SOI load device is controlled by two gates.

(iii) The bipolar transistor has a self-aligned non-overlapping base/emitter.

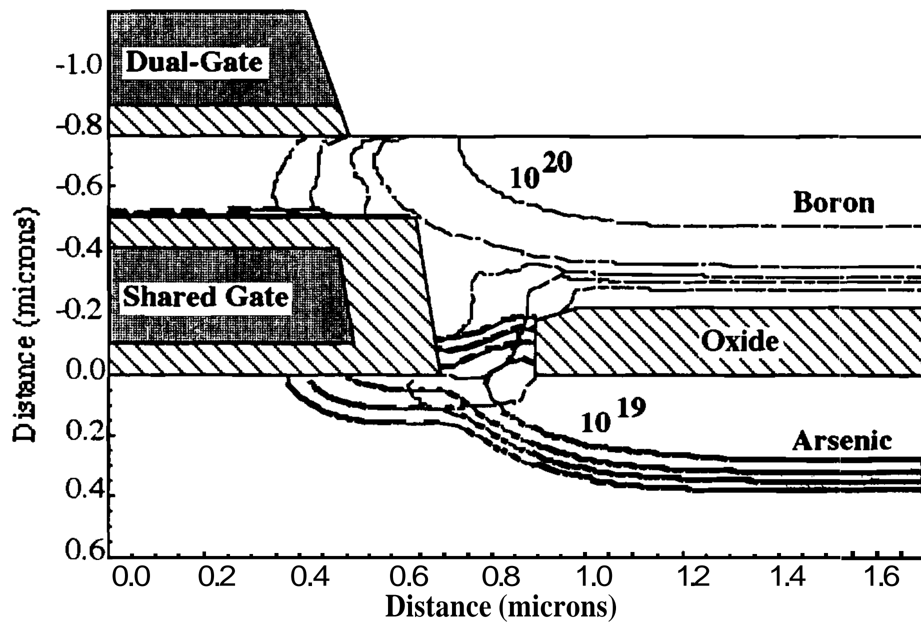
(iv) The bipolar device has a novel poly-silicon collector contact to the buried layer.

(v) There is independent control of the key parameters of the process such as the bipolar epi-thickness.

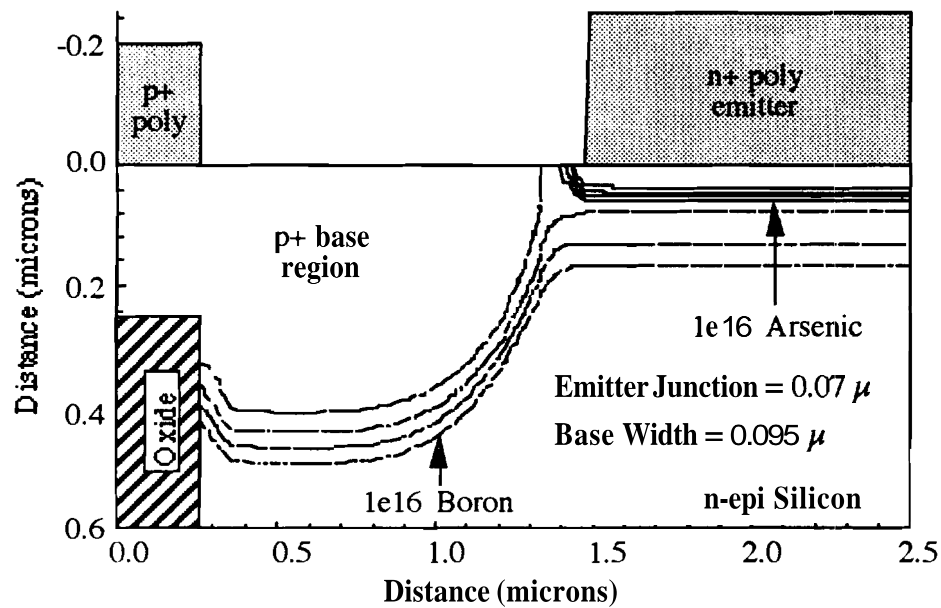
(vi) The bipolar has mono-crystalline extrinsic base contacts.

1.6.2 Process and Device Simulations

The T-SUPREM4 process simulator [20] was extensively used to investigate the fabrication process of the proposed 3-D BiCMOS structure. Most of the process steps involved in the fabrication were directly simulated through available commands in the software. However due to the three-dimensional nature of the structure, often a number of deposition steps and etch steps were used to attain the required structure, although in practice a single step would suffice. This was especially true when simulating the selective epitaxial growth process. TSUPREM-4 does not simulate selective epitaxial growth. In order to accurately model the growth and to include such effects as out-diffusion of impurities, a number of deposition, etch and diffusion steps were substituted for a single deposition step. The final output showing the CMOS and bipolar device structures are shown in figures 1.16(a) and (b). Shallow junction depths are obtained for the NMOS source/drain regions. Lateral out-diffusion of arsenic and boron is also minimized. In the bipolar transistor shallow emitter and base junction depths were obtained. The TSUPREM-4 simulator did not account for boron channeling effects and therefore the base profile obtained was somewhat aggressive and to some extent underestimated. Another critical process parameter to be optimized was the thickness of the top gate LTO oxide spacer which also determines the base link-up region. In the figure the p^+ boron extrinsic base provides a satisfactory link-up to the intrinsic base. Increasing the oxide spacer too much would result in degraded device performance through increased PMOS Source/Drain resistance and increased base resistance. Once the process steps had been fine tuned to optimize booth the bipolar and CMOS doping profiles, the process file was transferred to the PISCES-IIB device simulator to model the behavior of the dual-gated SOI PMOSFET. The transfer characteristics of the MOSFET and its output characteristics are shown in figure 1.17. The lateral shift in the transfer characteristics indicates that the dual-gated device operates at a slightly lower threshold voltage than the single gated MOSFET controlled by either the top gate and the bottom gate. The steeper slope to the dual-gated device curve is also indicative of a higher

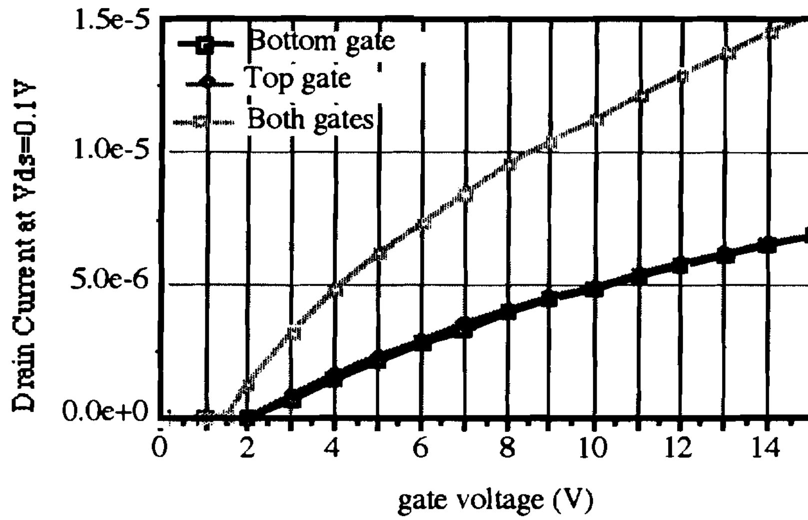


(a)

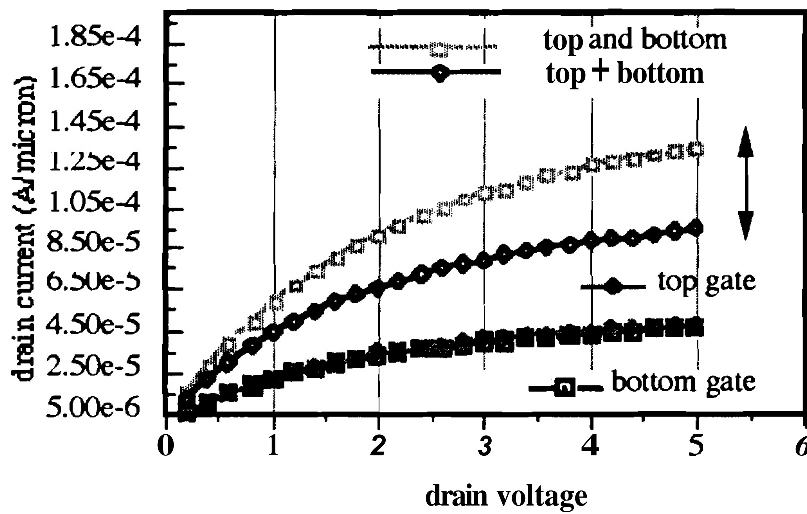


(b)

Figure 1.16 (a) Simulated structure in SUPREM IV showing the Boron and Arsenic contours for the stacked PMOS device and (b) 2D doping profiles of the BJT obtained from SUPREM IV



(a)



(b)

Figure 1.17 PISCES-IIB simulations lor the dual-gated PMOS shown in fig. 1.16(a). (a) the transfer characteristicsand (b) the output characteristics

transconductance under dual-gate operation. Figure 1.17(b) compares the output characteristics of the dual-gated device to the single gated device controlled by either the top or bottom gates. A large increase in available current is observed for the dual-gated device. This increment is over twice the current of the single-gated device due to the lowered threshold voltage in the device under dual-gate operation. Thus, the dual-gate SOI MOSFET provides at least twice the current for the same utilization of area as the device operated with only one gate. The area advantage it offers is enhanced when one considers that it is stacked above the NMOS and hence doesn't take up any silicon real estate.

1.7 Chapter Summary and Thesis Organization

BiCMOS technology significantly enhances speed performances while incurring a negligible power or area penalty. Thus BiCMOS can provide applications with CMOS power and densities at speeds which were the exclusive domain of bipolar technology. The main considerations in designing a BiCMOS process flow was considered in detail. The main disadvantages of BiCMOS evidenced in sections 1.3 and 1.4 is the greater process complexity. The complex process is a result of design constraints placed by conflicting needs of the bipolar and the CMOS devices. Most of the conflicts and subsequently most of the compromises and trade-offs occur at the front end of the process, which deals mainly with the choice of epitaxial parameters.

A majority of the design constraints due to the varying needs of the bipolar and CMOS devices disappear if the two devices are fabricated on separate epitaxial layers which can be optimized independently. Silicon-on-insulator technology provides us the means to be able to integrate MOSFETs and BJTs into a common process flow while keeping them in separate epitaxial tubs. Thus the epitaxial layer parameters can be chosen to primarily optimize the bipolar device, and the epi-layer thickness for the MOSFETs is determined separately by chemical mechanical planarization. The SOI MOSFETs thus fabricated show significant short channel immunity and have a natural isolation due to the buried oxide layer. This removes a number of process requirements such as retrograde well doping, choice of well doses, and back end well drive times. In addition the use of quasi-SOI techniques provides increased latchup immunity in merged

bipolar/CMOS structures and minimizes noise related cross-talk in mixed mode analog/digital circuits.

A novel 3-dimensional BiCMOS technology was presented which uses epitaxial lateral overgrowth of silicon to form the quasi-SO1 device regions. The technology uses only 12 masking steps and provides an inherently merged BJT and CMOS for reduced active area. The BJT has a polysilicon accessed sub-collector. The process allows independent control over the bipolar and CMOS epi-layer thicknesses. The CMOS device is vertically integrated with the PMOS stacked directly on top of the NMOS device. The process can be altered to form the PMOS on field oxide away from the NMOS increasing the accessibility of the NMOS device with a minor area penalty. The concept of a 3-dimensional structure and quasi-SO1 processing is still maintained in the altered process. The process steps were designed using the SUPREM4 process simulator. The structure files from SUPREM simulations were transferred to PISCES to simulate the device characteristics of the SOI PMOS transistor. The simulations prove the feasibility of the proposed BiCMOS technology. It shows promise as a potential solution to the problems of increasing integration density and circuit speed.

Due to the size of the BiCMOS project, the process development was separated into (a) the bipolar process development and (b) the SOI MOSFET development. Details of the development and the experimental results obtained from the bipolar process have been presented elsewhere [19]. Here we concentrate mainly on the CMOS inverter with all the emphasis placed on the development of the dual-gated SOI MOSFET. In particular selective epitaxy techniques to form thin-film fully-depleted SOI MOSFETs are investigated. The material properties of the SOI film are investigated by comparing them with simultaneously processed substrate devices. Devices fabricated in selective epitaxy material (CLSEG & ELO) were also compared with the state-of-the-art SIMOX material. Finally, a new measurement technique was developed to measure generation lifetimes in thin-film (fully depleted and partially depleted) SOI MOSFETs.

This chapter provides a motivation to investigate quasi-SO1 techniques for BiCMOS applications. The quasi-SO1 process proposed above requires that the SOI technology utilized satisfy the following requirements (i) the SOI technology must be amenable to quasi-SO1 and (ii) the SOI technology must be capable of yielding high performance SOI MOSFETs. Selective Epitaxial Growth of silicon (SEG) is one of the few prevalent SOI technologies to satisfy the above two conditions. SEG has been a

topic of considerable research in recent years. However a thorough investigation of the properties of SEG with specific applications to thin-film SOI MOSFETs is still lacking. In the remainder of this document we provide an investigation of thin-film SOI MOSFETs fabricated using selective epitaxy techniques from both a fabrication and electrical standpoint. We also provide a detailed theoretical understanding of the operation and properties of dual-gated SOI MOSFETs based on numerical simulations and analytical modeling.

In Chapter 2, we briefly review the properties of thin-film SOI MOSFETs, laying emphasis on the behavioral excursions from conventional bulk MOSFETs. The chapter also reviews current SOI technologies and motivates the use of SEG to fabricate SOI MOSFETs. A novel mode of operation of thin-film SOI MOSFETs, namely dual-gate operation, is critically analyzed in Chapter 3. The use of an alternate gate material is motivated and the advantages of dual-gated devices in this regard are presented. The chapter also includes a quantum-mechanical analysis of carrier distributions in thin-film fully depleted SOI MOSFETs. In Chapter 4, we detail the process development involved in fabricating thin-film SOI MOSFETs using both epitaxial lateral overgrowth and confined lateral selective epitaxial growth. Experimental results based on the measurement and analysis of fabricated MOSFETs are presented in Chapter 5. This chapter also provides the comparison of MOSFETs fabricated in selective epitaxy material with those fabricated in state-of-the-art SIMOX material. The theoretical development, computer simulations and experimental results from a newly developed linear sweep technique to measure generation lifetimes in thin-film SOI MOSFETs is introduced in Chapter 6. Finally Chapter 7 provides a summary of the thesis and makes recommendations for future work in the area.

1.8 References

1. "BiCMOS Technology and its applications", edited by A.R. Alvarez, Kluwer Academic Publishers, 1990.

2. T. Yuzuriha, T. Yamaguchi and J. Lee , " Sub-micron Bipolar-CMOS Technology using 16GHz F_t Double-Polysilicon Bipolar devices", ***IEDM Tech. Dig.*** , pp. 748, 1988.

Proceedings from SRC's Topical Research Conference on BiCMOS , 1990.

T. Ikeda, A. Wantanabe, Y. Nishio, I. Masuda, N. Tamba, M. Okada and K. Ogiue, "High speed BiCMOS technology with a buried twin-well structure", ***IEEE Trans. on Electron Devices,*** vol ED-34, pp. 1304, 1987.

B. Bastami, C. Lage, L. Wnag, J. Small, L. Bouknight and T. Bowman, "Advanced 1μm BiCMOS technology for high speed 256K SRAMs",***Dig. of Tech. Papers, Symp. on VLSI Tech.,*** pp. 41, 1987.

R. Haveman, R. Eklund, R. Haken, D. Scott, H. Tran, P. Fung, T. Han, D. Favreau and R. Virkus, "A 0.8μm 256K BiCMOS SRAM Technology, ***Tech. Digest, IEDM,*** pp. 841, 1987.

A. Alpermin, T. Holloway, R. Haken, C. Gosmeyer, R. Karnaugh and W. Parmantic, "Development of the self-aligned titanium silicide process for VLSl applications", ***IEEE Trans. on Electron devices,*** vol. ED-32, 0pp. 141, 1985.

A.R. Alvarez and D.W. Schucker, "BiCMOS Technology for Semi-custom Integrated Circuits", ***IEEE Custom Integrated Circuits Conference,*** pp. 22.1.1, 1988.

9. P.M. Soloman and D.D. Tang, "Bipolar Circuit Scaling", ***IEEE Intl. Solid State Circuits Conference,*** pp. ***86,*** 1979.

10. A.R. Alvarez, J. Teplik, H.B. Liang, T. Hulseweh, D.W. Schucker, K.L. McLaughlin, K.A. Hansen and B. Smith, "VLSI BiCMOS Technology and Applications", ***Intl. Symp. on VLSI Technology, Systems and Applications,*** pp. 314, 1987.

11. A.R. Alvarez, J. Teplik, D.W. Schucker, T. Hulseeh, H.B. Liang, M. Dydyk and 1. Rahim, "Second generation BiCMOS Gate Array Technology", ***IEEE Bipolar Circuits and Technology Meeting,*** pp. 113, 1987.

12. N.Rovedo, S.Ogura, J.Acocella, K.Barnes, A.Dally, T.Yanagisawa, C.Ng, J.Burkhardt, E.Valsamakis, J.Hamers, T.Buti and C.Richwine, "Process design for merged complimentary BiCMOS", ***IEDM Tech. Dig.,*** pp. ***485,*** 1990.

13. I.Rahim, B.Y.Hwang and J.Foerstner, "Comparison of SOI versus bulk silicon substrate crosstalk properties for mixed-mode ICs", ***Proceedings*** 1992 ***Intl. SOI Conference,*** pp. 170, 1992.

14. S.Sun, P.Tsui, B.Somero, J.Klein, F.Pintchovski, J.Yeargain and B.Pappert, "A 0.4μm fully complementary BiCMOS Technology for advanced logic and microprocessor applications", IEDM Tech. Dig., pp. 85, 1991.

15. J.Kirchgessner, J.Teplik, V.Ilderem, D.Morgan, R.Parmar, S.Wilson, J.Freeman, C.Tracy and S.Cosentino, "An advanced 0.4μm BiCMOS Technology for high performance ASIC applications", IEDM Tech. Dig., pp. 97, 1991.

16. J.Siekinnen and G.W.Neudeck, "Self-aligned Single Crystal Contacted High-Speed Silicon Bipolar Transistor uitlizing Selective Epitaxial Growth", *PhD.* Dissertation, Purdue University, 1992.

17. D. Scott, W. Hunter and H. Shichijo, "A new transmission line model for silicided source/drain diffusions : Impact on VLSI circuits", IEEE Trans. on Electron Devices, vol. ed-29, pp. 651, 1982.

18. A.R. Alvarez, B.L. Abdi, D.L. Young, H.D. Weed, J. Teplik and E.R. Herald, "Application of Statistical Design and Response Surface Methods to Computer-aided VLSI design", IEEE Trans on Computer-aided design, vol. CAD-7, No. 2, pp. 272, 1988.

19. R.Bashir, S.Venkatesan, G.W.Neudeck and J.P.Denton, "A polysilicon contacted sub-collector BJT for a three dimensional BiCMOS process", IEEE Electron Device Letters, EDL-13, pp. 392, 1992.

20. TMA SUPREM IV "Two Dimensional Process Analysis Program", Version 8926, 1989.

CHAPTER 2
SILICON-ON-INSULATOR MOSFETS

2.1 Introduction

Increasing circuit complexity has consistently been achieved by aggressive scaling of semiconductor device dimensions, In fact the most important trend for VLSI is the relentless decrease in the minimum feature size, which defines the gate lengths in MOSFETs. Minimum feature sizes have decreased from 50 pm in 1960 to 0.8 pm in 1990. Considerable research is underway to scale devices to the deep-sub micron region (< 0.5 pm). Device scaling, in addition to increasing integration densities, yields faster devices and minimizes parasitic elements. However, of late, device scaling has approached physical limitations so that any additional scaling requires prohibitively increased process complexity.

Bulk CMOS circuits cannot be scaled too aggressively because of the fear of latch-up [1]. Latch-up becomes a severe problem in devices with small dimensions where the gain of the parasitic bipolar transistors involved in the parasitic thyristor path becomes large. For sub-micron geometry, sophisticated schemes like the use of epitaxial substrates and/or deep trench isolation have to be used to counter latch-up. This impacts both the cost and the yield of manufacturing. Miniaturization of bulk MOSFETs proved to be the mythical Pandora's box. It brought into focus the numerous difficulties such as short-channel effects, narrow-channel effects and hot-electron effects. The reduction in gate length of bulk MOSFETs results in charge sharing between the sourcetdrain regions and the gate-controlled region. The effective charge controlled by the gate is reduced as a consequence of the charge sharing, which in turns reduces the threshold voltage of MOS transistors [2-5]. Since the percentage charge associated with the sourcetdrain regions is a function of the gate length, the effective charge controlled by the gate also depends on L. This causes the threshold voltage to depend on the channel length. As the channel length

decreases the threshold voltage begins to roll-off. The variation in threshold voltage with channel length is a measure of the short channel immunity of the device.

In long-channel devices, there exists a potential barrier between the source and the channel. As the gate length becomes smaller, the source and drain diffusions are brought closer together. The distance between the source and the drain may be insufficient to entirely accommodate the depletion regions of each diffusion. This causes the potential barrier between the source and the channel to decrease. In other words, the barrier is now lower than in the long channel case. The situation is exacerbated when a reverse bias is applied to the drain diffusion. There is now an increased possibility of field lines penetrating from drain to source, thereby lowering the barrier still more. This effect is called Drain-induced-bamer-lowering (DIBL) [6-10]. DIBL results in an unwanted current path. Devices operating with DIBL are said to operate in the punch-through mode [11,12]. As stated in [11], the primary method to counter punch through is to increase the channel-doping concentration. This results in a severely degraded mobility and hence lower output conductance. Typical short channel bulk MOSFETs require channel doping concentrations around $2\times10^{17}/cm^3$. The majority carrier (electron) mobility at this doping level at room temperature is approximately 520 cm^2/V-sec as compared to 1076 cm^2/V-sec at a doping concentration of $1\times10^{16}/cm^3$ [13]. The higher channel doping also increases the transverse electric fields which contribute to reduce the mobility even further [14]. Furthermore, the high channel impurity concentration degrades the sub-threshold slopes and may in some cases result in unwanted OFF-state leakage currents [15]. Many current applications of MOS circuits such as high density dynamic RAMs, switched capacitor circuits etc. depend critically on current flowing in the device in the sub-threshold region of operation.

Finally, the decreased gate-length and the increased channel doping cause large electric fields at the drain junction. The fields are large enough to induce hot-electron injection into the gate. Hot-electron-induced device degradation has become a major reliability concern in sub-micron MOSFETs [16-18]. The hot-electrons injected into the gate, generate interface traps which causes threshold voltage shifts during device operation. Moreover, the large longitudinal fields result in mobility degradation due to velocity saturation effects [19,20]. One of the most common ways to reduce the electric field has been to use a Lightly-Doped-Drain (LDD) structure [21-25]. However, careful optimization of the LDD implants are required to prevent severe device performance degradation due to increased Source/Drain resistance [26].

Several difficulties related to device processing and fabrication confront aggressively scaled devices. Device isolation, to date, has mainly been achieved by advanced LOCOS schemes [27]. However, with reduced dimensions, there is a increased possibility of cross-talk between adjacent circuits. Advanced birds beak free LOCOS schemes such as Poly-buffered LOCOS (PBL) or Recessed Poly-buffered LOCOS (RPBL) have to be embraced which again increases process complexities. Trench-isolation is another strong contender but is viable only if the sidewall leakage along the trench walls can be minimized. Trench isolation is under active research for isolation in 0.4 µm and 0.25 µm technologies, primarily to avoid an epitaxial step to provide latch-up immunity. Epitaxy is by far the most expensive and most defect prone step in semiconductor manufacturing.

As device dimensions shrink the capacitance associated with the gates of the MOSFET also decrease. In SRAM applications in particular, the load capacitance is determined by this gate capacitance and the value of the capacitance in turn determines the amount of charge stored on the storage node. If the amount of charge stored is very small then the SRAM cell becomes more susceptible to single-event-upset (SEU) errors due to alpha particles. In other words, it does not take a large amount of charge collection resulting from an alpha-particle strike to change the charge state of a storage node. This is also true in DRAMs, and has resulted in accelerated research into novel 3-dimensional ways to increase the capacity of the storage nodes. Soft-errors in high density memories have plagued scaled bulk MOSFETs [28].

Soft errors are caused by alpha-particles (emanated by nuclear radiation in the environment) which change the charge state of logic gates in a memory cell. The severity of soft-errors on the performance of logic circuits was responsible for directed research into radiation hard technologies. Silicon-on-Sapphire(SOS) was the first technology suggested and has been a topic of considerable research [29,30]. The high cost and low yield of SOS devices prompted research into other silicon-on-insulator (SOI) technologies, specifically, silicon-on-oxide. Silicon-on-Insulator (SOI) devices circumvent most of the major concerns in scaled bulk MOSFET technology. Hence, it is considered a very promising substitute to bulk MOSFETs. Besides, single layer SOI devices are the first step towards multi-layer three-dimensional integration [31].

In the following sections, we discuss the prevalent SOI technologies and detail the unique properties afforded by SOI devices which make them attractive for sub-micron

VLSI. The techniques involved in SOI fabrication are briefly reviewed in Section 2.2. Finally, in section 2.3 we elaborate on the properties of SOI MOSFETs, laying emphasis on the behavioral excursions from bulk MOSFETs. The section also enumerates existing analytical models which explain the behavior of thin-film SOI MOSFETs.

2.2 Silicon-on-Insulator Technologies

SOI materials provide a viable technology for high-density, large-integration and high-performance VLSI circuits. The majority of the advantages of SOI are derived from the capability of total electrical isolation of silicon active areas. Figure 2.1 depicts a typical SOI MOSFET, with a fully electrically isolated active area. The electrical isolation is provided by the buried oxide (which has since come to be referred to as the back gate insulator). The silicon substrate typically forms the "back gate". The difficulties with SOI mainly arise from defects at the two back interfaces in fig. 2.1. Back-interface 1, which is present in the channel region of the device, is the more important of the two. This defect-rife region provides easy leakage paths that can degrade device performance. Another primary concern is the material quality of the silicon film. Fabrication of quality SOI films is essential to achieving the potentials of SOI in IC fabrication.

Advanced SOI technologies have been under development for the last 25 years. There are several techniques that have been proposed and used to form SOI layers. Some hold more promise than others. The SOI technologies in vogue include Silicon-on-Sapphire [29,30,32-35], Zone Melt Recrystallization (ZMR) [36-40], Separation by implantation of oxygen (SIMOX) [41-44], Full isolation by oxidation of porous silicon (FIPOS), [45-47], wafer bonding and thinning (BESOI) [48] and lateral solid phase epitaxy (LPSEG) [49,50]. A complete summary of all of the above technologies is shown in Table 2.1. Of the above methods, ZMR and SIMOX have emerged as leading contenders, compatible with full-scale IC fabrication. Almost all available data on thin-film SOI MOSFETs have been measured on devices fabricated either in SIMOX or ZMR films. Of late BESOI (bonded etch-back) wafers are becoming extremely competitive and while the wafers are still not commercially available, the technology has matured at a very rapid rate and should sec proliferated growth in the coming years. Silicon-on-Sapphire was the starting point of all SOI technologies. In the following, a more detailed description is provided for SOS, SIMOX and BESOI.

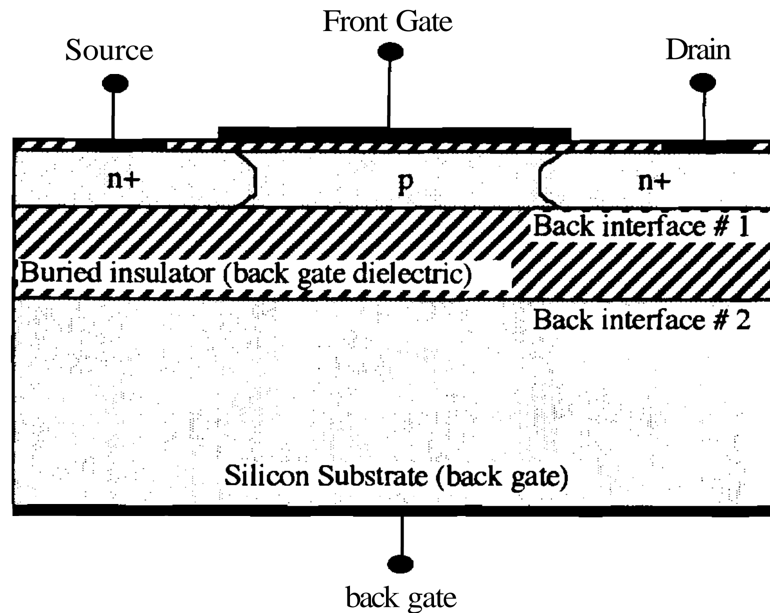


Figure 2.1 A typical SOI thin-film MOSFET with a back gate contact

2.2.1 Silicon-on-Sapphire (SOS)

Since the work by Manasevit in the late 1960's, SOS technology has experienced considerable evolution. 64K SRAMs with access times in the 12-40 ns range are now routinely manufactured by Hughes and Harris semiconductors for space applications. Silicon-on-Sapphire (SOS) involves the hetero-epitaxial growth of silicon on single crystal sapphire (Al_2O_3). Sapphire acts as the substrate as well as the insulator. Epitaxial growth is carried out by conventional CVD using the pyrolytic decomposition of silane. Hetero-epitaxial growth of a silicon film can never produce a defect free material if the lattice parameter of the insulator do not perfectly match those of silicon. If the epitaxial layer is very thin then the lattice remains strained and does not relax. The epitaxial layer then would be essentially defect free. The major crystallographic defects in the SOS material are microtwins, stacking faults and dislocations. Compressive stress is measured in SOS devices due to the lattice mismatch and the thermal expansion coefficient mismatch. The compressive stress causes the kx and ky ellipsoids to become more populated with electrons than the kz ellipsoid. As a result, the effective mass of the electrons in the

Table 2.1 SOI Technologies [33]

SOI Technology	Usable SOI Area	3D Candidate	SOI perfectness	Particularities
Laser Recrystallization	small	Yes	entrainment defects	Technology to be applied during IC processing; careful engineering required to prevent device degrading; submicron MOS ; low throughput
Electron-beam Recrystaliization	small	Yes	entrainment defects	Technology to be applied during IC processing; vacuum environment; careful engineering required to prevent device degrading; submicron MOS; low throughput; pseudo line scan
Graphite-strip heater Recrystallization	larger up to full scale	No	carbon contamination can be made defect free	Technology to be applied in the early stage of IC processing; higher throughput; lower defect density; submicron MOS; wafer warpage
Tungsten lamps Recrystallization	larger up to full scale	No	can be made defect free	Technology to be applied in the early stage of IC processing; well suited for thicker (> 10 microns); higher throughput; wafer warpage
SIMOX	full wafer	No	dislocations to be prevented; oxide precipitates to be annealed	A technology for wafer suppliers before IC processing; most adapted to existing silicon technology; submicron MOS
FIPOS	small islands fully isolated	No	not dislocation free	A technology with a limited applicability due to the smallness of the islands; a technology before IC processing; submicron and thicker layers
Lateral solid phase growth	small stripes	Yes	microtwins	A technology with a limited applicability due to the smallness of the stripes; processing IC compatible; submicorn MOS
Wafer Bonding	full wafer	Yes	comparable to bulk silicon	Advanced technology of wafer production; thicker SOI layers; technology for wafer suppliers
Hetero-Epitaxy	substrate scale	Probably Yes	so far not defect free due to lattice mismatch and dilatation	Technology to be evaluated; IC compatibility dependent on substrate material

inversion layer becomes larger than bulk silicon. Consequently, a relatively low channel mobility is observed in SOS MOSFETs. In addition microtwin defects in the epitaxial silicon lower the carrier mobility and cause large values of back channel leakage currents [32]. As a result SOS films typically show a large reduction of carrier mobility with decreasing epitaxial thickness as the proximity to the back interface increases. However sub-micron device design and processing require films thicknesses of 0.2 microns or less. Recent advances in SOS technology such as Solid Phase Epitaxy and Regrowth (SPEAR) [34] and Double Solid-Phase Epitaxy (DSPE) [35] have improved the physical and electronic properties of SOS films. The DSPE technique involves the amorphization of the entire silicon film with a silicon implant. Only the top layer is left un-amorphized, where the original defect density is lowest. Then a thermal annealing step is used to induce solid-phase regrowth of the amorphized silicon using the top layer as seed. A second silicon implant is then used to amorphize the top of the silicon layer, which is subsequently recrystallized in a solid-phase regrowth step using the bottom of the film as a seed. Due to the defects near the interfacial regions, circuit designers have been limited to using films of about 0.5 µm thickness. With the solid-phase regrowth techniques, the crystal quality of the interfacial regions have been improved significantly and has allowed the effective use of 0.1 µm films. The higher mobility in these improved films have also allowed the circuit designers to address high speed device markets on SOS. Although SOS devices are still the only commercially available products in SOI technology [33], the high cost associated with the use of sapphire has prompted further research into alternate SOI technologies.

2.2.2 Zone Melt Recrystallization SOI (ZMR)

The grain sizes of polycrystalline silicon films on insulating substrates, are greatly increased by the passage of a narrow molten zone. This is the basic principle upon which ZMR SOI films are based. Fig. 2.2 (a) illustrates the commonly used technique to form ZMR films. A thin layer of polysilicon is deposited over oxide and is capped by another oxide layer. Intense heat in the form of a laser, electron-beam, graphite strip heater or a high power halogen lamp is used to melt the polysilicon in narrow strips. As the molten silicon cools, it recrystallizes back into single-crystal silicon. The molten front is typically scanned across the entire wafer. In order to get a ordered crystal with a fixed crystal orientation, seeded recrystallization could also be used [36].

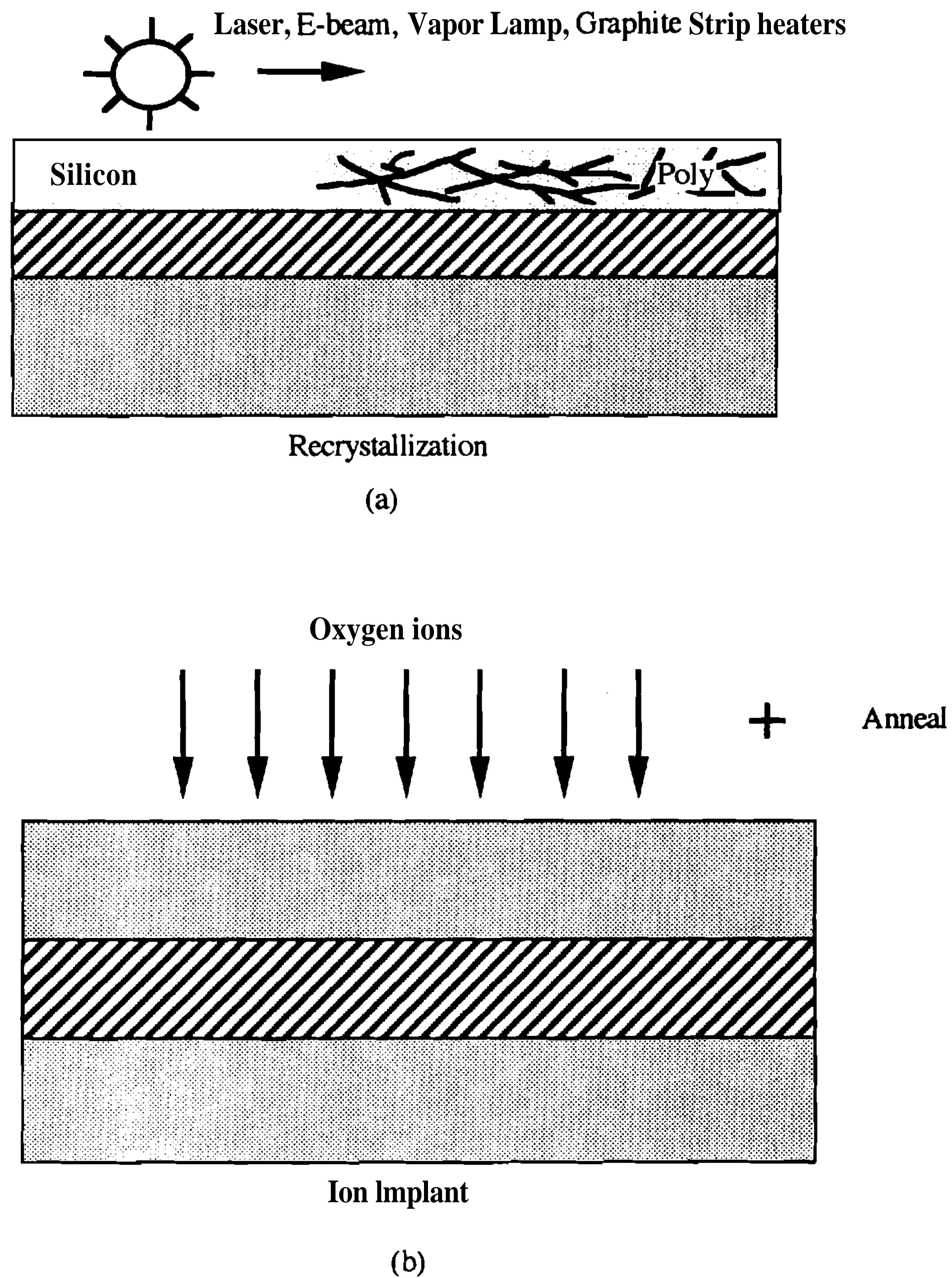


Figure 2.2 Sketch illustrating the two principal SOI technologies (a) zone-melt-recrystallization (ZMR) and (b) ion-implanted oxygen (SIMOX)

The main defects in ZMR films are grain boundaries (GB) and sub-grain boundaries (SGB). The GBs and the SGBs usually occur parallel to the scanning front. GBs can severely affect MOSFET performance by degrading the mobility. Besides, the grain boundaries give rise to enhanced diffusion of impurities, which necessitate low temperature processing. SGBs drastically reduce the minority carrier lifetimes in ZMR films. This makes the ZMR films relatively inaccessible to BiCMOS. Often, voids result from imperfections in the growth front [37]. Moreover, mass transport occurs during the zone melting process leading to non-uniformity in the thickness of the SOI film throughout the wafer. Another problem is that of possible wafer warpage due to the high temperatures required for recrystallization.

A number of devices have been reported fabricated in ZMR films [38,39], including three-dimensional multiple-layer structures [40].

2.2.3 Separation by Implanted Oxygen (SIMOX)

The acronym SIMOX stands for 'separation by implanted oxygen'. The principle of SIMOX material formation is very simple and involves the formation of a buried layer of SiO_2 by implantation of oxygen ions beneath the surface of a silicon wafer. Since the implanted oxygen atoms are used to actually synthesize a SiO_2 layer, the oxygen dose must be very heavy ; typically about 2 x 10^{18} /cm^2. SIMOX has been under active research since 1977. A SIMOX wafer is prepared (Fig. 2.2 (b)) by implanting a silicon wafer with oxygen ions at 150-200Kev and to an ion dose of typically 1 - 2 x10^{18} /cm ^{2}. The wafer is typically heated to about 400°C or higher during the ion-implantation process. This prevents the wafer from turning amorphous during implantation. After the oxygen is implanted, the wafer is typically annealed above 1150°C in an inert ambient. Thc high temperature anneal repairs the damage introduced during implantation and allows the excess oxygen in the surface silicon to out-diffuse. The high temperature step also increases the dielectric strength of the buried oxide [41-44].

The oxygen dose must be higher than the critical dose of 1.4 x 10^{18} /cm^2. Below this dose silicon particulates or islands are often present in the buried oxide. This reduces the di-electric strength of the oxide and results in larger back oxide leakage currents. The optimum wafer temperature during the implant is 600-650°C. An as-implanted SIMOX wafer consists of a top layer of predominantly single crystal silicon but which is highly

disordered and contains a lot of oxygen precipitates. The anneal temperature must be chosen such that all the oxygen precipitates are dissolved. The complete dissolution of all precipitates occurs at an annealing temperature of around 1300°C. The annealing ambient is typically nitrogen with 2% oxygen. The oxygen allows for the growth of some oxide on the superficial silicon layer which protects the silicon from pitting which occurs when the silicon is annealed at high temperatures in pure nitrogen. The annealing steps usually last about 6 hours. The material quality of the wafers has been improved dramatically by using multiple implant/anneal cycles with annealing temperatures in the excess of 1300°C. The principal defects in the material are threading dislocations of the order of $10^5/cm^2$. Very few, if any bipolar devices have been fabricated in SIMOX material and it is hard to assess its applicability to BiCMOS. Due to the high annealing temperatures, the utility of SIMOX to multi-layer three-dimensional integration is cramped. Besides, the thickness of the back oxide is difficult to precisely control. The straggle of the implant profile and the dissolution of the oxygen precipitates and their subsequent motion towards the silicon-oxygen interface causes the buried oxide thickness to be larger than expected. As will be discussed later, the thickness of the buried oxide can be exploited to alleviate short channel effects in moderately thin-film devices and in deep-sub micron devices. Another severe drawback is wafer throughput. Due to the large energies and implant doses involved, even high current implanters typically take hours to implant a single wafer. This directly leads to higher wafer costs.

Despite the above drawbacks, SIMOX is currently the most widespread of the SOI technologies. The conventional IC manufacturing process used (implantation and annealing) as well as the full-wafer isolation attained are the primary reasons for its popularity.

2.2.4 Bonded Wafer and Etch-back SOI (BESOI)

The principal of the bonding and etch-back technique is extremely trivial. It is so simple that it is a wonder the technology has taken so long to blossom. Two oxidized wafers are 'glued' or 'bonded' together with the oxidized faces in contact.. One of the wafers is subsequently polished or etched down to a thickness suitable for SOI applications. This is illustrated in fig. 2.3 (a). The other wafer serves as the mechanical substrate and is called the 'handle wafer'. When two hydrophilic surfaces such as oxidized

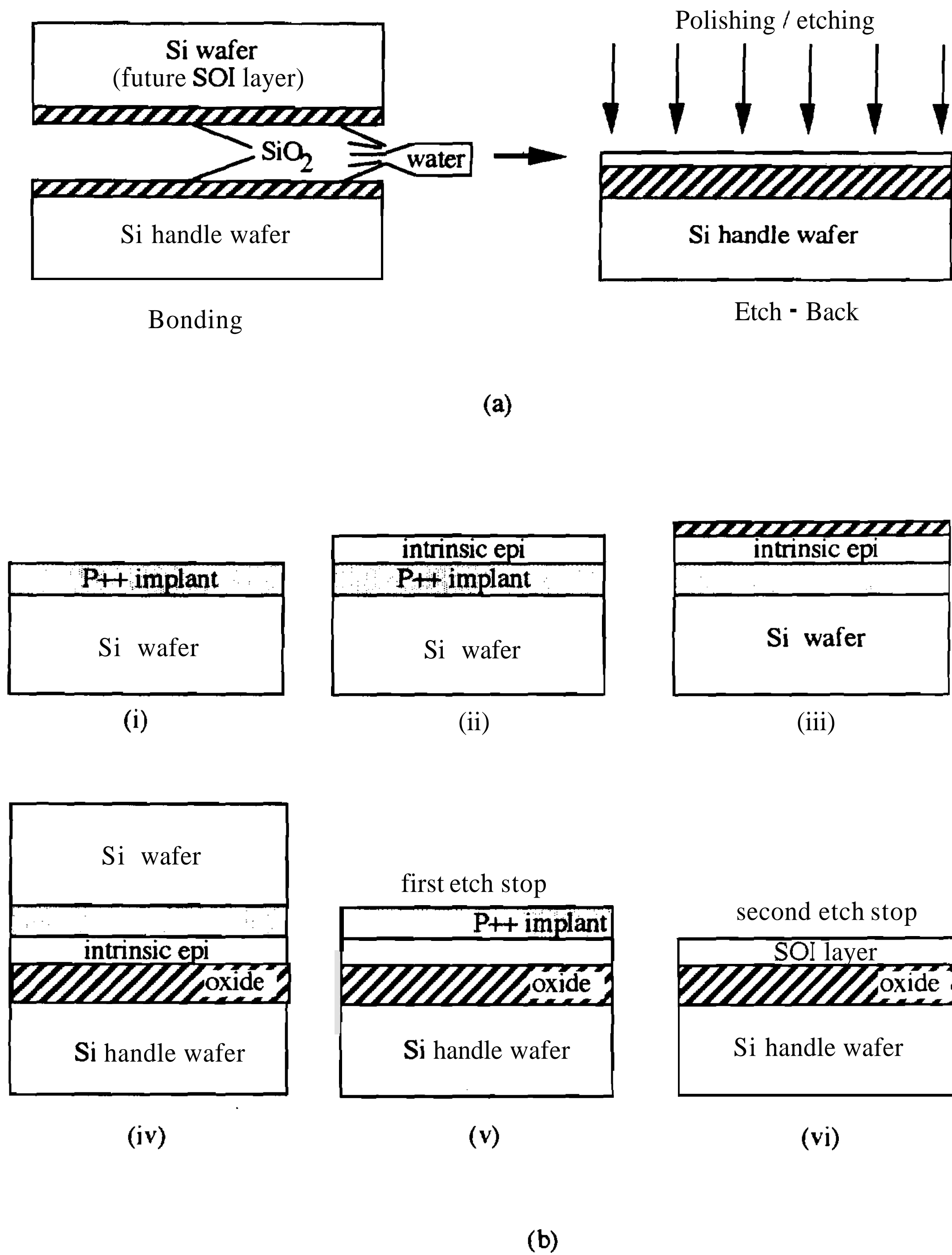


Figure 2.3 (a) Bonding of two oxidized silicon wafers (left), and polishing/etching of one of the wafers and (b) the double-etchstop technique to achieve SOI wafers by the bonded etch-back method

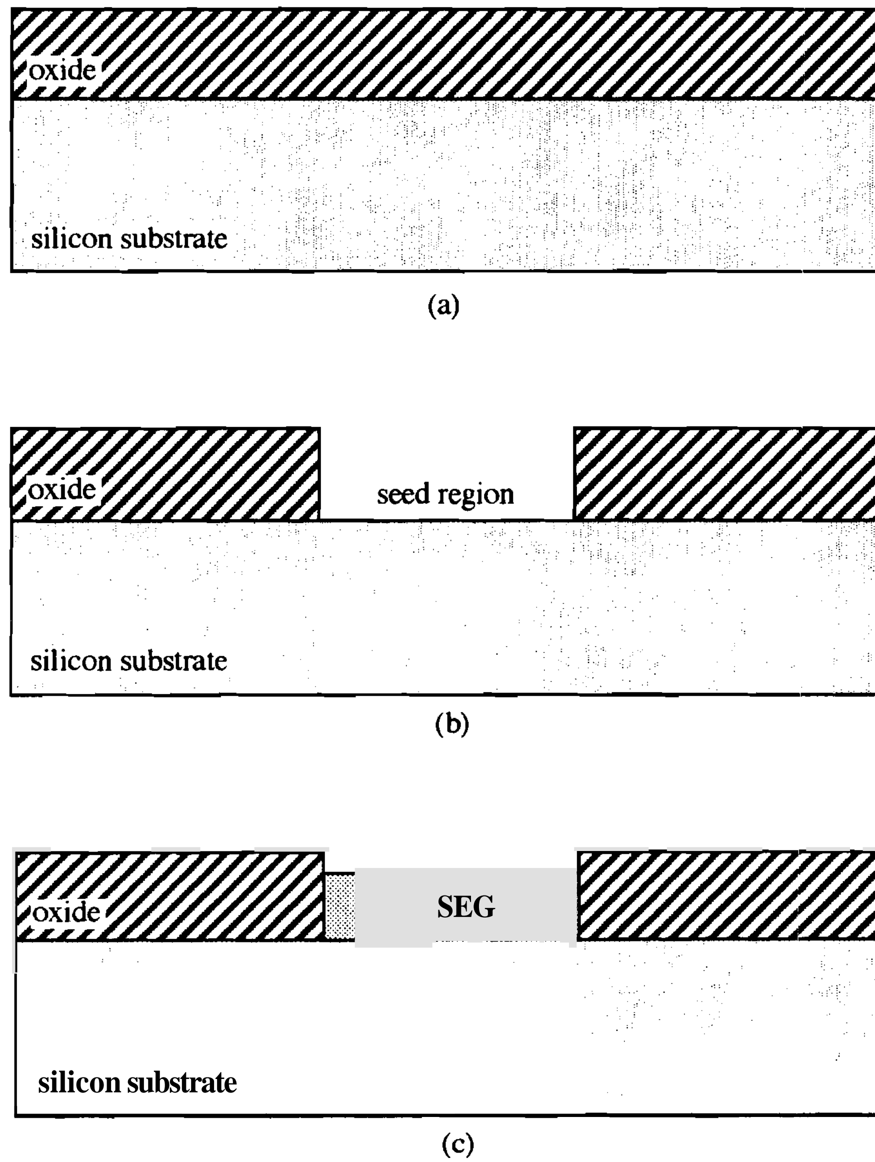
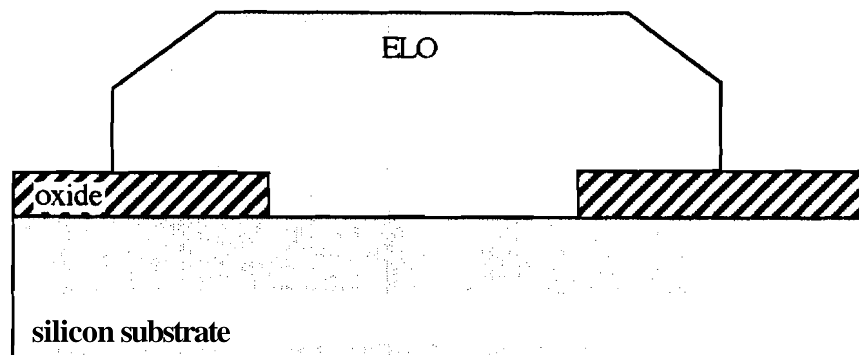
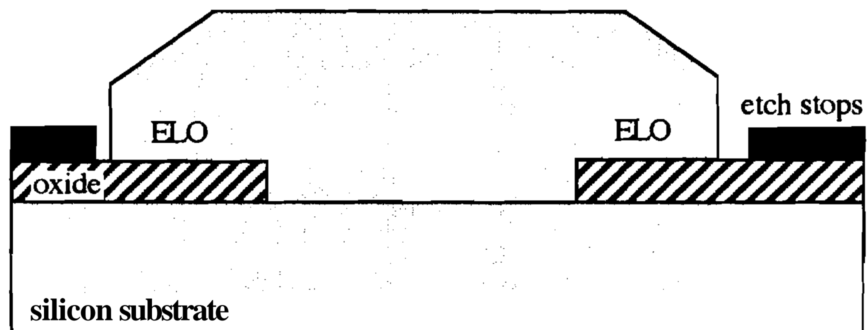


Figure 2.4 Process flow for Selective Epitaxy of silicon (a) Oxidize silicon substrate (b) Etch seed windows in the oxide (c) Grow epitaxial silicon selectively in the exposed silicon areas.



(a)



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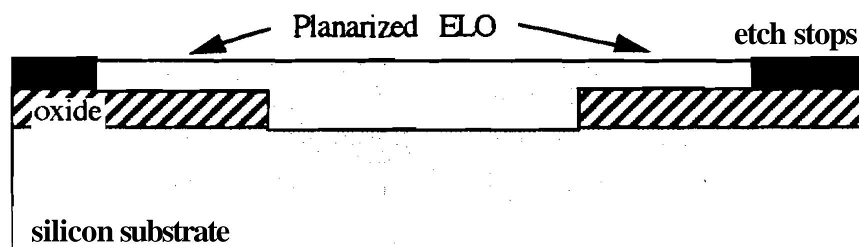


(c)

Figure 2.5 (a) Typical Cross-section of Epitaxial Lateral Overgrowth (b) Chemical Mechanical Polishing (CMP) Process:nitride/oxide etch-stops. (c) Finished structure through CMP

When epitaxial silicon is allowed to grow beyond the restricting rnasking oxides, epitaxial lateral overgrowth (ELO) results. This process is illustrated in Fig 2.5 (a). Since ELO forms epitaxial silicon layers over oxide, it is considered to be another SOI technology. One of the problems associated with ELO is that the growth in the lateral dimension is equal to the vertical growth giving an aspect ratio of unity. Therefore, formation of thin SOI films requires that the epitaxial film be planarized. Chemical Mechanical Polishing[51] provides an excellent scheme to planarize the epitaxial silicon over large areas with excellent uniformity across the wafer. Figs. 2.5 (b) and (c) illustrate the chemical-mechanical planarization process. Etch stops of either silicon nitride or silicon dioxide are deposited and patterned prior to epitaxial growth. CMP then planarizes the silicon with extremely high selectivity over the etch-stop material. The etch effectively stops when the nitride or oxide is encountered. Thin SOI films can be formed using a combination of ELO and CMP. In order to be a viable SOI technology, the epitaxial siliwn must be of high quality. Material quality of ELO has been extensively studied [52] and high performance bipolar transistors have been successfully fabricated in ELO silicon. Thus ELO proves to be a very promising SOI technology for integrating SOI MOSFETs with either bulk or SOI minority carrier devices such as bipolar transistors.

A major problem associated with Selective Epitaxial growth is the: degradation of the mask oxide during growth [53]. It has been shown that the masking oxide must be at least 800Å thick to obtain complete isolation for a typical deposition temperature of 900°C and pressures of 150mTorr. Lower pressures help reduce the growth temperature and could possibly reduce the minimum requisite oxide thickness. Three-dimensional stacked capacitors [54] and three-dimensional CMOS devices [55] have been fabricated with excellent characteristics using ELO. In both cases, polysilicon was used as the gate material and poly-oxides were used as the gate dielectric. C-V characterization [56] demonstrated excellent characteristics for the back interface with low interface state densities, indicating the applicability of poly-oxides for device fabrication. Recently very thin-film CMOS devices have been fabricated in epitaxial silicon over oxide using a combination of ELO and CMP [57], demonstrating its viability for thin film applications.

A complete characterization of the thin-films fabricated by ELO is still lacking. It is partially the purpose of this study to understand the characteristics of thin-films of silicon fabricated by ELO/CMP. It is also necessary to provide a direct comparison of the interface states of the poly-oxide/silicon interface to that of a good crystalline silicon dioxidelsilicon

interface to further confirm the continued viability of polysilicon as the back gate material in thin-film SOI applications.

Another form of selective epitaxial growth, called Confined Lateral Selective Epitaxial Growth (CLSEG), has been developed [58,59]. CLSEG obviates the need for planarization after epitaxial growth by confining the growth within a pre-defined cavity. The aspect ratio of the cavity then determines the aspect ratio of the final SOI film. The basic growth and fabrication process is illustrated in Fig. 2.6. Fabrication starts with an oxidized silicon wafer, in which seed holes are patterned. A brief oxidation (100Å) is used to cover the seed-hole and a layer of amorphous silicon (a-Si) is conformally deposited over the entire wafer. The thickness of the a-Si determines the thickness of the cavity and hence the final thickness of the SOI film. The a-Si film is patterned and defined with a photomask and then oxidized. This step converts the a-Si into smooth large grained polysilicon and forms a thin oxide on the surface. A layer of silicon nitride or oxide is then deposited over the entire wafer for mechanical support. Via holes are etched in the support layer down to the poly. The polysilicon is then etched out of the cavity using an ethylene diamine solution with high selectivity to oxide. Once the cavity is cleared, the seed hole is reopened with a brief buffered HF dip. Epitaxial silicon is then grown in the cavity using procedures similar to SEG and ELO. Feasibility of the CLSEG process has been demonstrated for thick (0.27 to 1 micron) films. The material quality has been shown to be excellent by fabricating diodes, MOSFETs and BJTs [60]. However, detailed characterization of CLSEG, especially for thin films, as required to assess the viability of the technology for thin-film SOI is far from complete. It is proposed herein to characterize the thin CLSEG films and compare its quality to ELO/CMP films of the same thickness.

In summary, the prevalent SOI technologies have been reviewed with emphasis on ZMR and SIMOX. The two are currently the most popular technologies to achieve SOI. Finally, selective epitaxial growth techniques in the form of epitaxial lateral overgrowth and confined lateral selective epitaxial growth were introduced as novel ways to fabricate "device island" type SOI structures. Device island SOI, as opposed to full wafer SOI, allows active devices on SOI only in required areas. The rest of the wafer could if necessary be 'bulk-based'. The fabrication processes for ELO and CLSEG were reviewed. This material forms the background for the remainder of the proposal.

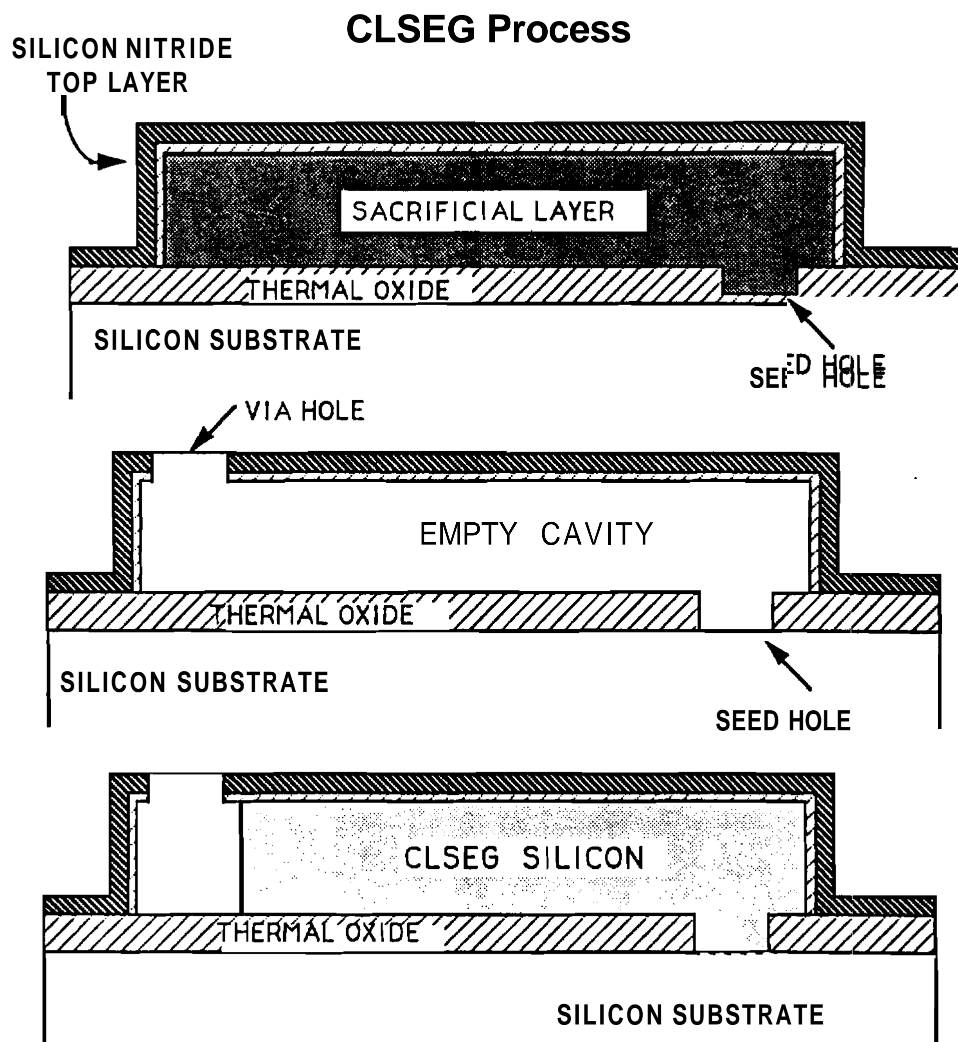


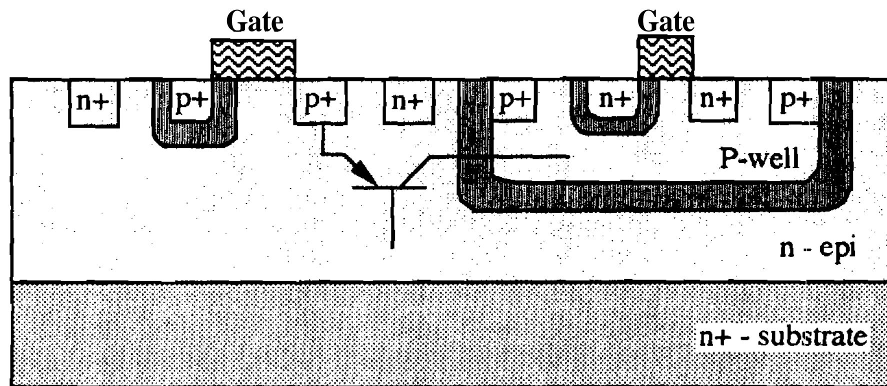
Figure 2.6 Process sequence for Confined Lateral Selective Epitaxial Growth (CLSEG)

2.3 Comparison of Bulk and SOI Processing Technologies

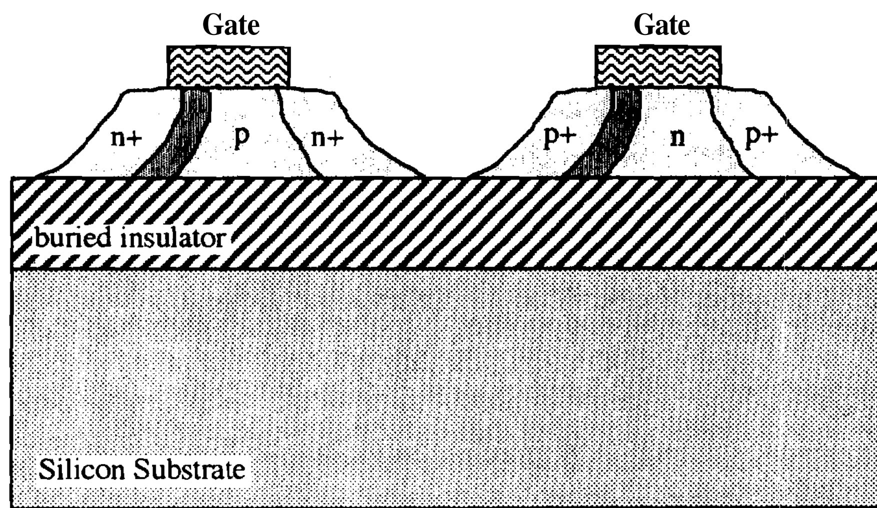
Complimentary MOS (CMOS) is by and large the technology of choice for the realization of integrated circuits on SOI substrates. In this section, CMOS processing on bulk silicon and on SOI wafers are compared. Processing techniques for the fabrication of CMOS circuits in bulk silicon and in SOI are very similar. Figure 2.7 presents cross-sections of CMOS inverters made in bulk (p-well technology) and in thin-film SOI substrates. From the cross-sections it is obvious that SOI processing, and more specifically thin-film SOI processing, is simpler that bulk processing. For instance there is no need to create diffused wells in SOI. The entire impurity profile in the channel area of thin-film SOI MOSFETs is determined by a single shallow implant. Table 3.2 compares simplified CMOS process flows for bulk and thin-film fully depleted (FD) SOI.

Isolation between SOI devices is simple due to the presence of the buried insulator. Two main isolation techniques are widely used. The first is conventional LOCOS isolation. The difference between LOCOS in bulk silicon and in SOI devices is the presence of thin-films in SOI devices. Hence care must be taken not to over-oxidize during isolation lest the silicon film get lifted up along the edges. This is particularly true for really small active area dimensions. In an SOI process, the thickness of the oxide which must be grown to fully isolate the silicon islands is 2.5-3 times the thickness of the silicon film. The LOCOS isolation process is illustrated in figure 2.8. The bottom corners of the silicon islands are extremely thin as seen in the figure. An inversion layer can form in these regions which could degrade sub-threshold slopes and is also a source of leakage currents when the device is turned off. Therefore, a heavy P^+ - implant must be used for n-channel devices to turn these edge leakage off.

Mesa isolation is the other technique to isolate silicon islands from one another. This technique is attractive because of its simplicity. However, a review of the current literature does not reveal a single process that uses mesa-isolation. This may be because LOCOS isolation has become extremely standard in CMOS processing. Mesa processing is illustrated in figure 2.9. In extremely thin gate oxides grown on mesa-isolated islands, a reduction of the gate oxide breakdown has been observed [134]. This is because oxidation of silicon comers produces SiO_2 layers with non-uniform thicknesses. The thickness of the oxide grown on the comers of an island can be 30 to 50% thinner than that grown on its top surface. Oxidation is also known to sharpen silicon comers. This effect is enhanced if more than a single oxidation step is performed (i.e. if a sacrificial oxide is grown and



(a)



(b)

Figure 2.7 (a) Bulk silicon CMOS cross-section. Also illustrated is a parasitic bipolar transistor and (b) an SOI structure. The reverse biased depletion regions are indicated in both sketches

Table 2.2 Comparison of Bulk and Thin-Film Fully Depleted (FD) SOI CMOS Process Flows. N+ Polysilicon is used as the Gate Material

BULK CMOS	FD SOI CMOS
Oxidation	Oxidation
Well lithography	
Well doping and drive-in	
Nitride deposition	Nitride deposition
Active area lithography	Active area lithography
Nitride etch	Nitride etch
Field implant lithography	
Field implant	
Field oxide growth	Field Oxide growth
Nitride strip	Nitride strip
P-channel lithography	
Anti-punchthrough implant	
Gate oxide growth	Gate oxide growth
P-channel Vth implant	P-ch Vth implant
N-channel Vth lithography	N-channel Vth lithography
Anti punch-through implant	
N-channel Vth implant	N-channel Vth implant
Poly deposition and doping	Poly deposition and doping
Gate lithography and etch	Gate lithography and etch
P^+ S&D lithography	P^+ S&D lithography
P^+ S&D implant	P^+ S&D implant
N^+ S&D lithography	N^+ S&D lithography
N^+S&D implant	N^+S&D implant
S&D reoxidation	S&D reoxidation
Dielectric deposition	Dielectric deposition
Contact hole lithography	Contact hole lithography
Contact hole opening	Contact hole opening
Metallization	Metallization
Metal lithography	Metal lithography
Metal patterning	Metal patterning
Sintering	Sintering

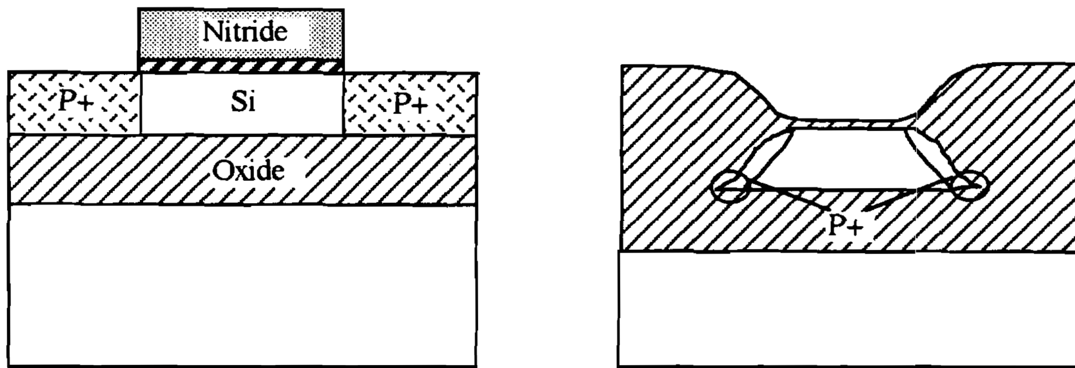


Figure 2.8 LOCOS isolation. The circles at the edges of the silicon island (left) indicate where source-to-drain edge leakage may occur

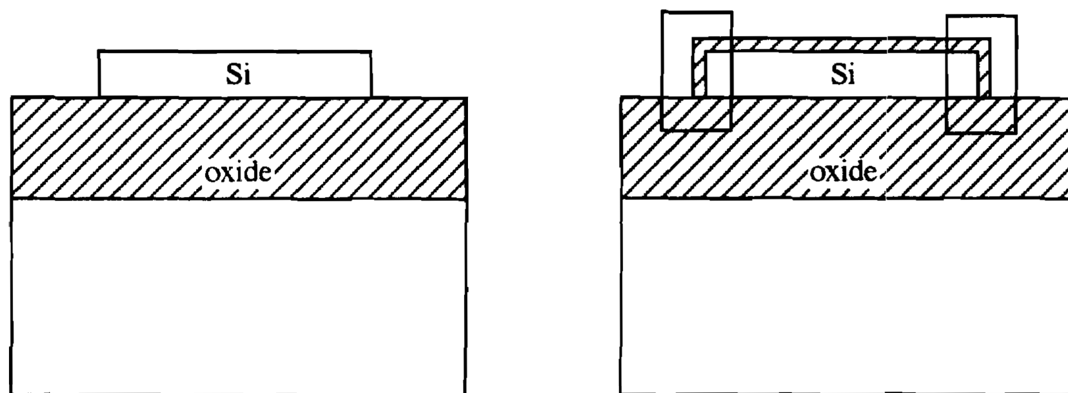


Figure 2.9 Mesa isolation. The boxed in areas highlight regons where edge leakages could occur causing degraded sub-threshold charactenstics

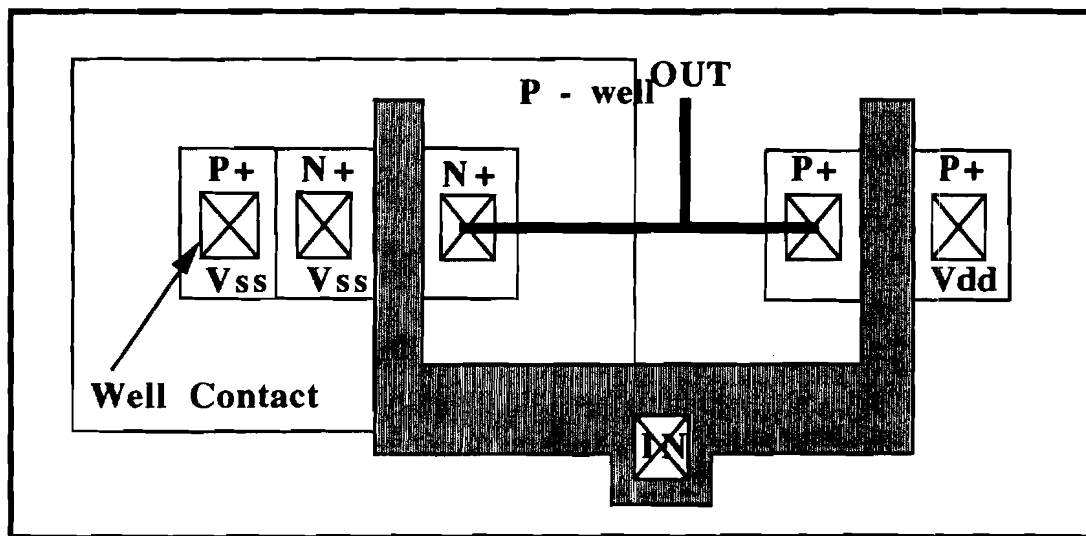
stripped prior to oxidation) [135]. In a mesa-process, the gate oxide and the gate material covers both the top and the edges of the silicon island. Therefore there exist latcral (edge) transistors in parallel to the main (top) device. Furthermore, due to charge sharing between the main and the edge devices, the threshold voltage is reduced at the comer of the island [136]. This can produce a kink in the sub-threshold characteristics as well as leakage currents. Both oxide breakdown and the leakage currents can be improved by using P^+ sidewall doping and mesa-edge rounding techniques [134].

The optimization of the doping concentration in thin-film, fully-depleted devices is a matter of balance between two effects. Firstly, the doping concentration must be low enough to ensure full depletion, and secondly, it must be high enough to provide devices with a suitably large threshold voltage [137]. Finding such a balance is usually not a problem in p-channel devices with N+-poly gates, but as shall be seen in Chapter 3, it requires some attention for n-channel transistors. Simulations show that both the doping concentration and the silicon film thickness have to be optimized in order to produce useful values of the threshold voltage. As far as doping profiles are concerned there is no room in thin-film SOI MOSFETs to create anything but an almost flat doping profile. In thin-film SOI technology, the sourceldrain series resistance can reach very high values which can jeopardize the speed performances of the circuits. It becomes imperative just as in the case of bulk MOSFETs to form a silicide on the sources and drains to reduce their sheet resistance. The specifics of the silicidation process must be altered from the typical bulk process to account for the ultra-thin nature of the SOI film [138].

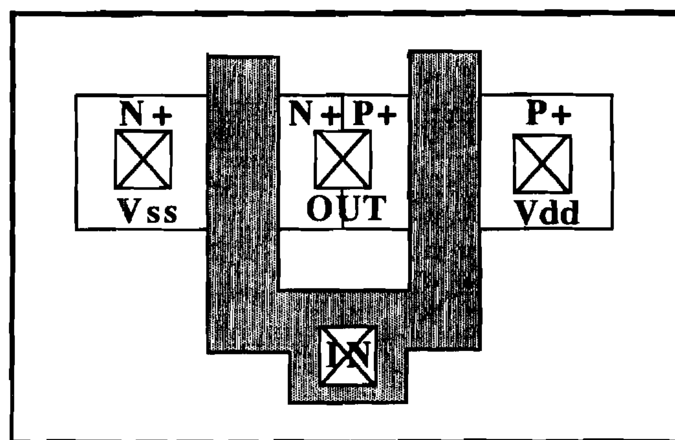
Finally, SOI CMOS technology offers a higher integration density than bulk CMOS. This is evident from the comparison between the layout of the bulk CMOS inverter and that of an SOI CMOS inverter depicted in figure 2.10. This higher density results mainly from the absence of wells in SOI. A second cause of increased density is the possibility of having a direct contact between the P^+ and N^+ junctions. The number of contact holes per gate is also lower.

2.4 Properties of Silicon-on-insulator MOSFETs

The drawbacks and limitations of bulk MOSFETs were detailed in the introduction to this Chapter. Silicon-on-insulator (SOI) MOSFETs were introduced as an alternative to bulk MOSFETs in the short-channel regime. In the following sub-sections the main



(a)



(b)

Figure 3.10 Layout of a (a) bulk CMOS inverter and (b) a SOI CMOS inverter

properties of SOI-MOSFETs which make them an attractive prospect for sub-micron VLSI, will be reviewed. SOI-MOSFETs have conventionally been thick-film MOSFETs. Thick-film MOSFETs are the devices in which the channel region is = fully depleted by the gate during normal operation, i.e. the maximum depletion width prior to inversion is less than the film thickness. The silicon film thickness is larger than twice the value of W, In such a case, there is no interaction between the depletion zones arising from the front and back interfaces, and there exists a piece of neutral silicon beneath the front depletion zone. Device operation in thick-film SOI MOSFETs is therefore similar to bulk MOSFETs and the only significant differences are the floating substrate effects encountered in thick-film MOSFETs. Floating substrate effects form a subject of later discussion. Of late, thin-film MOSFETs operating in the fully depleted mode have been shown to have tremendously improved properties over partially depleted thick-film MOSFETs. In a thin film SOI device, the silicon film thickness is smaller than W_{max}. In that case, the silicon film is fully depleted at threshold, irrespective of the bias applied to the back gate. The front and back interfaces interact with each other when the channel is fully depleted. Because both front and back interfaces can be either in accumulation, depletion or inversion there are 9 modes of operation in the fully depleted SOI MOSFET. However only the regimes of operation where the back surface is depleted are 'useful' operating regions. Unless specifically mentioned, the MOSFETs are assumed to be thin-film and fully depleted, and in the following sections, these properties are briefly reviewed.

2.4.1 Conventional Properties of SOI MOSFETs

Figure 2.7 sketches a bulk CMOS device cross-section and a typical SOI structure. The reverse-biased p-well forms the isolation between the n-MOSFETs and the p-MOSFETs in the bulk CMOS process. More importantly, various parasitic elements exist. In the figure, the parasitic bipolar formed by the p-n-p regions in the structure is shown. Though the parasitic devices are biased off under normal operation, random electrical perturbation can trigger bipolar action resulting in "latch-up". The junction areas present in the structure contribute to the capacitance and reduce circuit speed. The SOI structure inherently overcomes these CMOS deficiencies. The parasitic bipolar elements do not exist and the problem of parasitic latch-up is completely avoided. Also, the junction area is drastically reduced. The simplicity of the isolation technique allows the minimum device separation to be determined only by the lithography. This results in higher packing density

and smaller chip size. The reductions in the parasitic capacitance should lead to an increase in circuit speed. SOI devices have a much smaller charge collection volume than bulk CMOS devices and are therefore more immune to soft-errors caused by alpha-particles. The radiation hardness of SOI technology should permit greater flexibility in circuit design and layout due to simpler processing.

2.4.2 Threshold Voltage of Fully Depleted MOSFETs

The threshold voltage of an enhancement mode bulk n-channel MOSFET is given by,

$$V_{th} = V_{FB} + 2\Phi_F + qN_A W_{max}/C_{ox} \tag{1}$$

where V_{FB} is the flat band voltage equal to $(\Phi_{MS} - Q_{ox}/C_{ox})$, Φ_F is the Fermi potential equal to $kT/q\ln(N_d/n_i)$, and W_{max} is the maximum depletion width given by $\sqrt{4\varepsilon_o K_s \Phi_F/qN_A}$.

In a thick film SOI device where the film thickness $t_{si} > 2\,W_{max}$, there can be no interaction between the front and back depletion zones. The threshold voltage is the same as in a bulk transistor and is given by eqn. (1).

In a thin-film, fully depleted enhancement mode n-channel devices, the interaction between the two interfaces forces one to solve Poisson's equation in the channel in order to determine the threshold voltages. Assuming the depletion approximation, the equation is

$$\frac{d^2\Phi}{dx^2} = \frac{qN_A}{\varepsilon_{si}} \tag{2}$$

When integrated twice this yields the potential distribution as a function of position in the film.

$$\Phi(x) = \frac{qN_A}{2\varepsilon_{si}}x^2 + \left[\frac{\Phi_{sb} - \Phi_{sf}}{t_{si}} - \frac{qN_A t_{si}}{2\varepsilon_{si}}\right]x + \Phi_{sf} \tag{3}$$

where Φ_{sf} and Φ_{sb} are the potentials at the front and back silicon/oxide interfaces, respectively.

Similarly, the field distribution in the film can be expressed as,

$$E(x) = -\frac{qN_A}{\varepsilon_{si}}x - \left[\frac{\Phi_{sb} - \Phi_{sf}}{t_{si}} - \frac{qN_A t_{si}}{2\varepsilon_{si}}\right] \quad (4)$$

Gauss' Law is then applied to the front and back interfaces.

$$V_{ox_f} = \frac{\varepsilon_{si}E_{sf} - Q_{ox_f} - Q_{inv_f}}{C_{ox_f}}$$

$$V_{ox_b} = \frac{-\varepsilon_{si}E_{sf} - qN_A t_{si} + Q_{ox_b} + Q_{s_b}}{C_{ox_b}} \quad (5)$$

$$V_{G_f} = \Phi_{sf} + V_{ox_f} + \Phi_{MS_f}$$

$$V_{G_b} = \Phi_{sb} + V_{ox_b} + \Phi_{MS_b}$$

Q_{ox} is the fixed charge density, Q_{invf} is the front inversion charge density (<0) and Q_{sb} represents the charge state of the back interface ($Q_{sb} = 0$ under depletion, $Q_{sb} > 0$ under accumulation and $Q_{sb} < 0$ under inversion). Combining equations (1) - (5) we get the desired relationships between the front gate voltage and the back gate voltage.

$$V_{G_f} = \Phi_{MS_f} - \frac{Q_{ox_f}}{C_{ox_f}} + (1 + \frac{C_{si}}{C_{of}})\Phi_{sf} - \frac{C_{si}}{C_{ox_f}}\Phi_{sb} - \frac{\frac{1}{2}Q_{dep} + Q_{inv_f}}{C_{ox_f}}$$

$$V_{G_b} = \Phi_{MS_b} - \frac{Q_{ox_b}}{C_{ox_b}} - \frac{C_{si}}{C_{ox_b}}\Phi_{sf} + (1 + \frac{C_{si}}{C_{ox_b}})\Phi_{sb} - \frac{\frac{1}{2}Q_{dep} + Q_{s_b}}{C_{ox_b}} \quad (6)$$

where $C_{si} = \varepsilon_{si}/t_{si}$ and $Q_{dep} = -qN_A t_{si}$.

If the back surface is accumulated, $\Phi_{sb} \approx 0$ and at threshold $Q_{invf} \approx 0$. Then,

$$V_{th_{f,ACC}} = V_{FB_f} + \left(1 + \frac{C_{si}}{C_{ox_f}}\right)(2\Phi_F) - \frac{Q_{dep}}{2C_{ox_f}} \quad (7)$$

If the back surface is inverted, $\Phi_{sb} \approx 2\Phi_F$ and once again the threshold voltage is obtained as,

$$V_{th_{f,INV}} = V_{FB_f} + 2\Phi_F - \frac{Q_{dep}}{2C_{ox_f}} \tag{8}$$

Finally, when the back surface is depleted,

$$V_{th_{f,DEP}} = V_{th_{f,ACC}} - \frac{C_{si}C_{ox_b}}{C_{ox_f}(C_{si} + C_{ox_b})}(V_{G_b} - V_{G_{b,ACC}}) \tag{9}$$

Thus under these conditions the front gate threshold voltage varies linearly with the back gate voltage. The dependence of the front gate threshold voltage on the back gate voltage is qualitatively depicted in figure **2.11.** The dependence of the front gate threshold voltage on the back gate bias decreases with increasing $t_{ox,b}$. When $t_{ox,b}$ is very large (back gate oxide is very thick) then the front gate voltage is virtually independent of the. back gate bias.

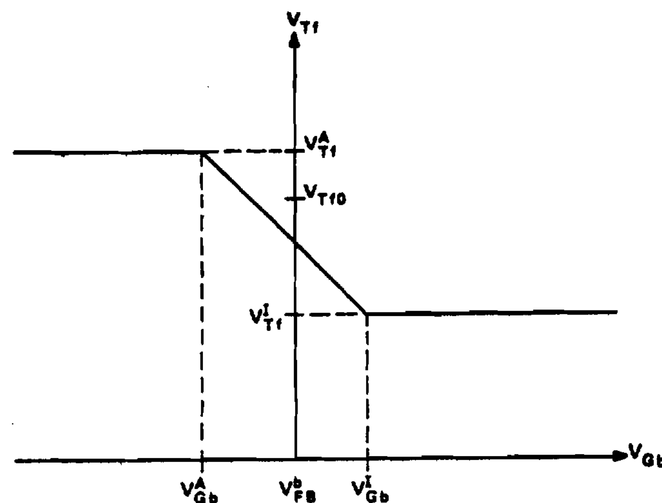


Figure 2.11 Theoretical dependence of V_{Tf} on V_{Gb} for a completely depleted SOI MOSFET. For reference, the corresponding bulk MOSFET threshold voltage V_{Tfo} is indicated [62]

of a MOSFET, g_m, is a measure of the effectiveness of the control of the drain current by the gate voltage. The saturation **transconductance** is given by [65],

$$g_m = \frac{dI_{d}}{dV_{G_f}} = \gamma \frac{W}{L} C_{ox_f} \mu (V_G - V_{th}) \quad (14)$$

where $\gamma = C_{ox_f} / (C_{ox_f} + C_{sub})$ is again the efficiency factor. The substrate capacitance is a combination of both the capacitance of the **SOI** film and the back oxide capacitance for the case when the back surface is depleted. Thus the efficiency factor γ is reduced from its maximum value of 1.0 for the case when the back oxide thickness is infinite, to 0.94 when t_{box}=3500Å (t_{box} is the buried oxide capacitance) and further to 0.77 when t_{box} = 1000Å. Thus, the transconductance enhancements in **SOI** MOSFETs over bulk MOSFETs is maximum for thick back gate oxides. For thinner back gate oxides, the drain saturation voltages are reduced by the efficiency factor γ, and the saturation current and transconductance enhancements are also reduced by y.

Another effect which is expected to increase the current in **ultra-thin-film SOI-**MOSFETs is the effect of vertical field on the surface mobility **[63]**. In MOS devices in general, increasing the vertical field confines the **carriers** to the surface region where there are more scattering sites. Thus increased vertical fields result in degraded effective mobility. The surface electric field in a thin-film **SOI** device with the back surface depleted is lower than the surface electric field in a bulk MOSFET. To first order, the surface fields in a FD **MOSFET** is $\frac{qN_A t_{si}}{2\varepsilon_{si}}$ and that in a bulk MOSFET is $\frac{qN_A W_{max}}{\varepsilon_{si}}$. Since thin-film fully-depleted **SOI-MOSFETs** have smaller vertical fields, they are expected to have a higher effective mobility than corresponding bulk MOSFETs. Moreover, since the field remains constant from source to drain, there is no mobility degradation towards the drain. This increased effective mobility translates into a higher drain current. Mobility enhancement due to decreased vertical electric fields have been observed experimentally **[66].The** maximum of mobility is obtained right above threshold, but is rapidly overshadowed by the decrease of mobility caused by the increase of Q_{inv} when the gate voltage is significantly larger than V_{th}.

For a given gate voltage, **SOI-MOSFETs** have a larger number of inversion electrons than **bulk-MOSFETs**. Therefore, **bulk-MOSFETs** have lower saturation drain voltages than **SOI-MOSFETs** for the same gate voltage. This is shown in Fig. 2.13.

However in short-channel device fabricated in the sub-micron region velocity saturation effects limit the output current [67]. Velocity saturation acts to reduce the saturation voltage; for both the SOI MOSFETs and the bulk MOSFETs. Fig. 2.13 also illustrates the dependence of the saturation voltage on gate length. In long channel MOSFETs, the saturation voltage of SOI MOSFETs were larger than that of bulk MOSFETs due to larger channel charge. As the channel lengths become shorter, the saturation voltage of both SOI and bulk MOSFETs decrease and approach the same value. The saturation current densities should in principle also approach the same value. Under high fields the saturation current density is written as [139],

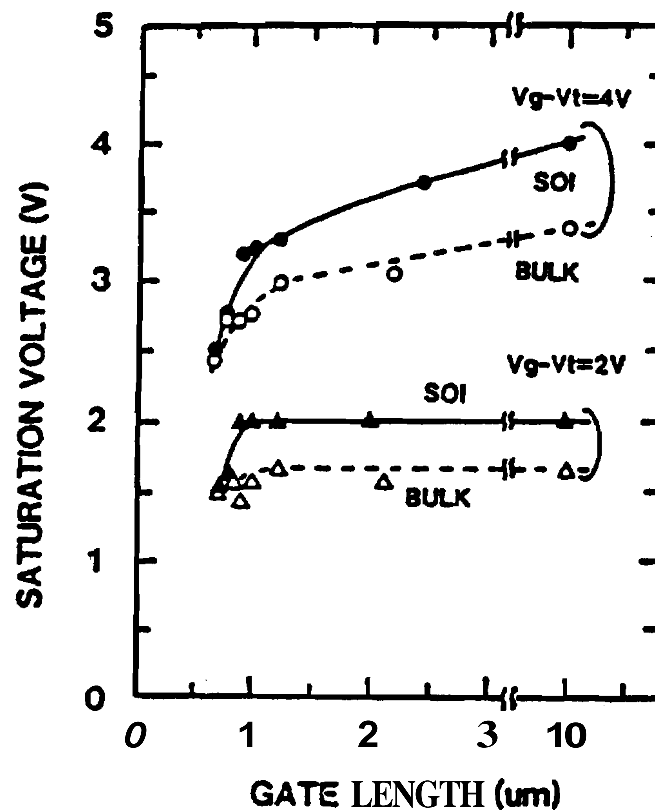
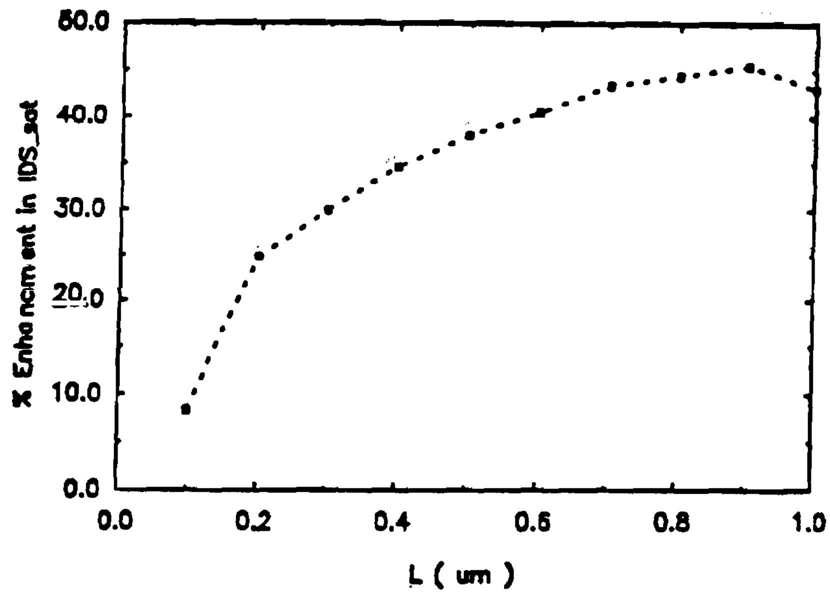
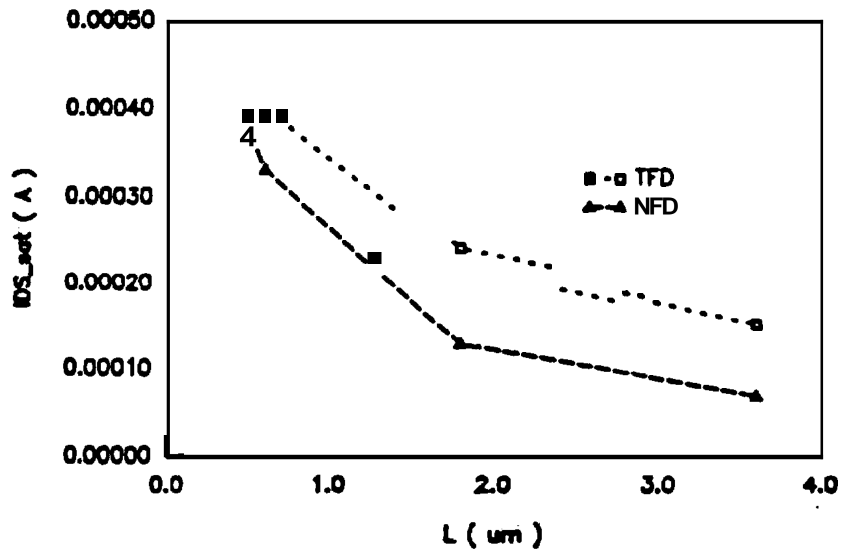


Figure 2.13 Dependence of the saturation voltage on channel length for thin-film SOI MOSFETs and bulk MOSFETs [67]



(a)



(b)

Figure 2.14 (a) Simulated relative (to bulk counterparts) enhancement of current versus channel length of fully depleted n-channel SOI MOSFETs and (b) Measured current versus channel length of fully depleted (TFD) and their bulk (NFD) counterparts [139]

$$I_{ds_{sat}} = \frac{WC_{ox_f}}{1+\alpha} \frac{m(V_{G_f} - V_{th})^2 v_{sat}}{1 + \frac{m(V_{G_f} - V_{th})}{1+\alpha}} \quad (15)$$

where m = $\mu/2Lv_{sat}$. Thus for short channel lengths,

$$I_{ds_{sat}} = WC_{ox_f} v_{sat}(V_{G_f} - V_{th}) \quad (16)$$

The enhancement due to a is thus lost at the short channel lengths. This is clearly demonstrated in figure 2.14, where the current densities of similar geometry bulk and thin-film SOI MOSFETs approach each other in the deep sub-micron regime.

SOI MOSFETs are more immune to short-channel effects as will be discussed later. The channel doping of SOI MOSFETs can therefore be low even in the sub-micron regime whereas short-channel bulk MOSFETs require higher doping concentrations than those for long channel devices. Therefore, the SOI MOSFETs provide higher mobility and higher saturation velocities for carriers. This effect is responsible for the larger current drives of the SOI MOSFETs, even in the presence of velocity saturation and is depicted in Fig. 2.15.

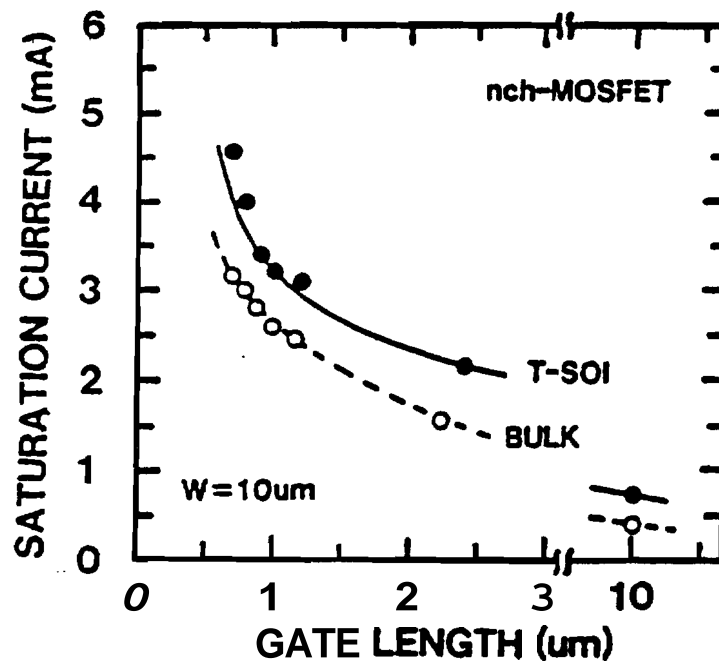


Figure 2.15 Dependence of the saturation current on channel length for thin-film SOI MOSFETs and bulk MOSFETs [67]

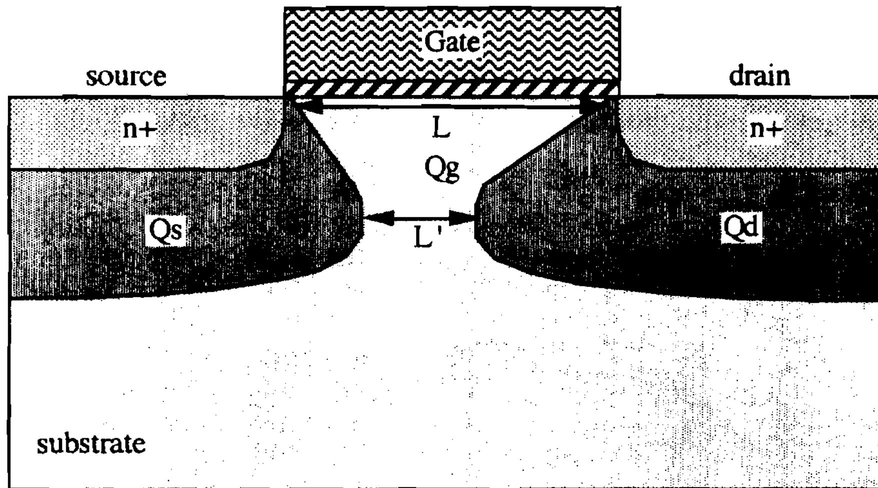
Therefore, in summary, SOI MOSFETs provide higher saturation currents than corresponding bulk MOSFETS in long channel devices due to increased drain saturation voltages. In the short channel regime, SOI MOSFETs allow lower channel doping concentrations than bulk MOSFETs. Although the drain saturation voltages are almost equal because of velocity saturation, the SOI MOSFETs provide larger currents because of the lower channel doping.

2.4.4 Short Channel Effects

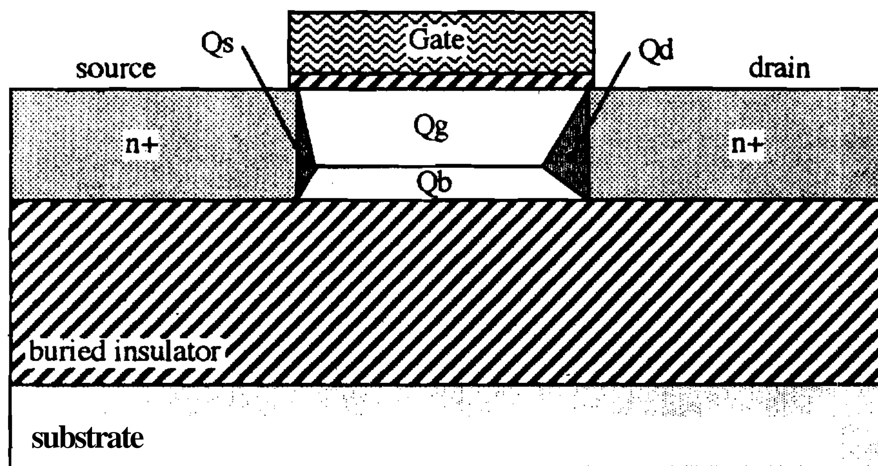
Short Channel effects cause a significant change in device behavior. A number of effects come into focus as channel lengths are shortened: (1) Channel Length modulation (2) Threshold voltage lowering (3) Drain induced barrier lowering and punchthrough (4) hot-electron effects and (5) mobility degradation due to large electric fields [68]. The threshold voltage variation with channel length and DIBL are predominantly due to charge sharing between the S/D and the gate. A major advantage of SOI MOSFETs is its greater immunity to short-channel effects [69].

A first order estimation of the dependence of threshold voltage on the channel length can be determined from geometrical considerations [70]. Fig. 2.16 illustrates the typical depletion regions existing in short-channel bulk and SOI MOSFETs. It can be seen that in thin-film SOI MOSFETs , only a small fraction of the depletion charge under the gate is controlled by the source and drain. On the other hand, in bulk MOSFETs, a larger portion of the charge under the gate can be partitioned into the Source and Drain. This portion increases relative to the total depletion charge as the channel lengths decrease. Since the gate controls less and less substrate charge, the threshold voltage decreases with channel length. Therefore, in thin-film SOI MOSFETs, the threshold voltage remains more or less constant for gate lengths down to 0.5μm. This is illustrated in figure 2.17. One can see that the threshold voltage roll-off starts to occur at significantly smaller gate lengths in thin-film SOI transistors than in bulk devices.

Alleviated short-channel effects have been studied analytically [71-73] and have been verified experimentally [74]. In [71], Young studied the short-channel effect in fully depleted SOI MOSFETs , using an analytical two-dimensional model and PISCES



(a)



(b)

Figure 2.16 Schematic cross-section of a (a) bulk and (b) thin-film SOI transistor. Qg, Qb, Qs and Qd are the depletion region charges associated with the gate, back interface, source and drain respectively

simulations. It was established that the reduction in threshold voltage due to short channel effects decreases with decreasing silicon film thickness. Comparison with the analytical models for bulk MOSFETs [75] showed the advantages of SOI MOSFETs over their bulk-silicon counterparts. In addition to threshold voltage roll-off with gate length, other short-channel effects such as drain-induced-barrier lowering, channel length modulation and velocity saturation were investigated in detail by Fossum et al [72] based on a charge-based

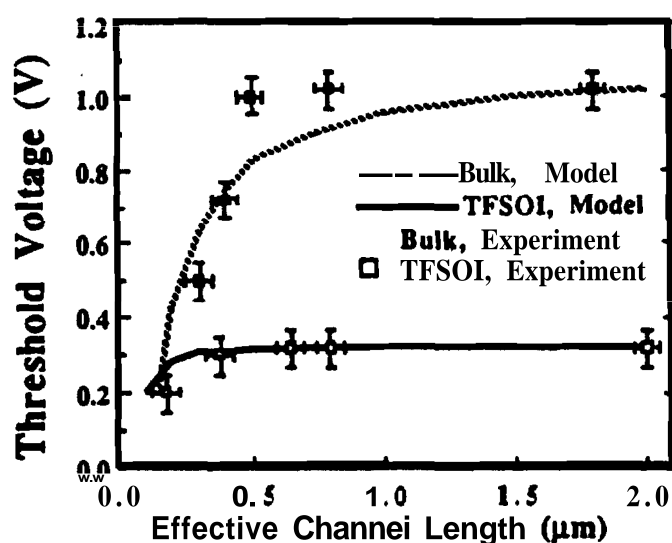


Figure 2.17 Threshold voltage roll-off comparison between bulk MOSFET and thin-film SOI MOSFETs

large signal model for a transistor in strong inversion [73]. It was shown that the presence of the back gate significantly affects the behavior short channel devices. In addition to thinning the SOI film, operating the device with the back gate held in accumulation ameliorates threshold-voltage reduction, DIBL and channel length modulation. The short channel effect is smaller in thin-film devices with accumulation at the back side than in thin-film fully depleted devices but both of them show less short-channel effects than their bulk

counterparts. However, accumulated back surfaces degrade transconductances and drive currents [65] and also result in increased drain electric fields which exacerbate hot-electron effects as well as reduce the carrier mobility. Hence, design trade-offs would be involved in controlling the short-channel effects, through the accumulation of the back interface. An optimum control of the space charge in the silicon film by the gate (which would further minimize the short channel effect) could be obtained by using double-gate devices (one gate below the active silicon film and one gate above it). Making such devices is a real technological challenge, but some practical schemes will be proposed in later chapters.

Another short channel effect, called drain-induced conductiuity enhancement (DICE) is also due to charge sharing between the gate and the junctions[73]. DICE is caused by the reduction of the depletion charge controlled by the gate due to a size increase of the drain junction-related depletion zone, which itself increases with V_{DS}. In order to model the DICE effect, an analysis involving the solution of the two-dimensional Laplace equation (in a fully depleted device) must be carried out. It can be shown that the DICE effect is lower in thin-film SOI devices than in bulk devices [72].

2.4.5 Sub-threshold Slope

Sub-threshold slope is an extremely important MOSFET parameter, as it characterizes the region between the off-state and the on-state. The inverse sub-threshold slope (S) is defined as $\delta V_G/\delta(\ln I_d)$, when the channel is in the weak inversion regime. For bulk MOSFETs, it can be shown that S can be approximated by [76],

$$S = \frac{kT}{q}\log(10)\left(1 + \frac{(C_D + C_{it})}{C_{ox}}\right) \tag{17}$$

where C_D , C_{it} and C_{ox} are the depletion capacitance, the interface trap capacitance and the gate capacitance respectively. The depletion capacitance is small in the case of SOI MOSFETs. Moreover. the depletion charge does not vary with gate bias. Therefore, in thin film SOI MOSFETs, the value of the inverse sub-threshold slope approaches a minimum value given by [77],

$$S = \frac{kT}{q}\log(10)\left(1 + \frac{C_{it}}{C_{ox}}\right) \tag{18}$$

Though this expression, derived from bulk MOSFET theory cannot be strictly applied to thin-film SOI MOSFETs, it explains to a first order the improved sub-threshold slopes for SOI MOSFETs compared to bulk MOSFETs. Physically the inverse sub-threshold slope 'S' is a measure of the gate voltage swing required to change the drain current by an order of magnitude. The value of S then determines the minimum value of the threshold voltage for acceptable leakage currents. Typically a ratio of 10^5 is required for the ratio of ON-state to OFF-state current. If the value for S were 100mV/decade then '5S' would determine the minimum threshold voltage for an ideal device in the absence of fixed charges. Sharp sub threshold slopes then allow devices to operate at low threshold voltages, which increases the saturation voltage and hence the saturation current and speed of the device. Colinge et al [78] proposed a capacitance divider model to understand the sub-threshold slopes under different substrate bias conditions. The models under different bias conditions are shown in Fig. 2.18.

$$S = \frac{dV_G}{d(\log I_d)} \tag{19}$$

The sub-threshold current of an MOS transistor is a minority carrier diffusion current

$$I_D = -qAD_n\frac{dn}{dy} = qAD_n\frac{n(0)-n(L)}{L}$$
$$n(0) = n_{po}e^{\beta\Phi_s};n(L) = n_{po}e^{\beta(\Phi_s - V_D)} \tag{20}$$

The inversion channel can be approximated by a box carrier profile with a uniform carrier concentration n(0) and a thickness 'd' defined as the distance from the Si-SiO_2 interface at which the potential is lowered by kT/q [70].

$$d = \frac{kT/q}{E_s} \quad ; \quad E_s = -\frac{d\Phi_s}{dx} \tag{21}$$

Using these expressions the current is written as,

$$I_d = \left(\mu_n\frac{W}{L}q\left(\frac{kT}{q}\right)^2\frac{n_i^2}{N_A}(1-e^{-\beta V_D})\right)\frac{e^{\beta\Phi_s}}{-d\Phi_s/dx} \tag{22}$$

From (19) we can write,

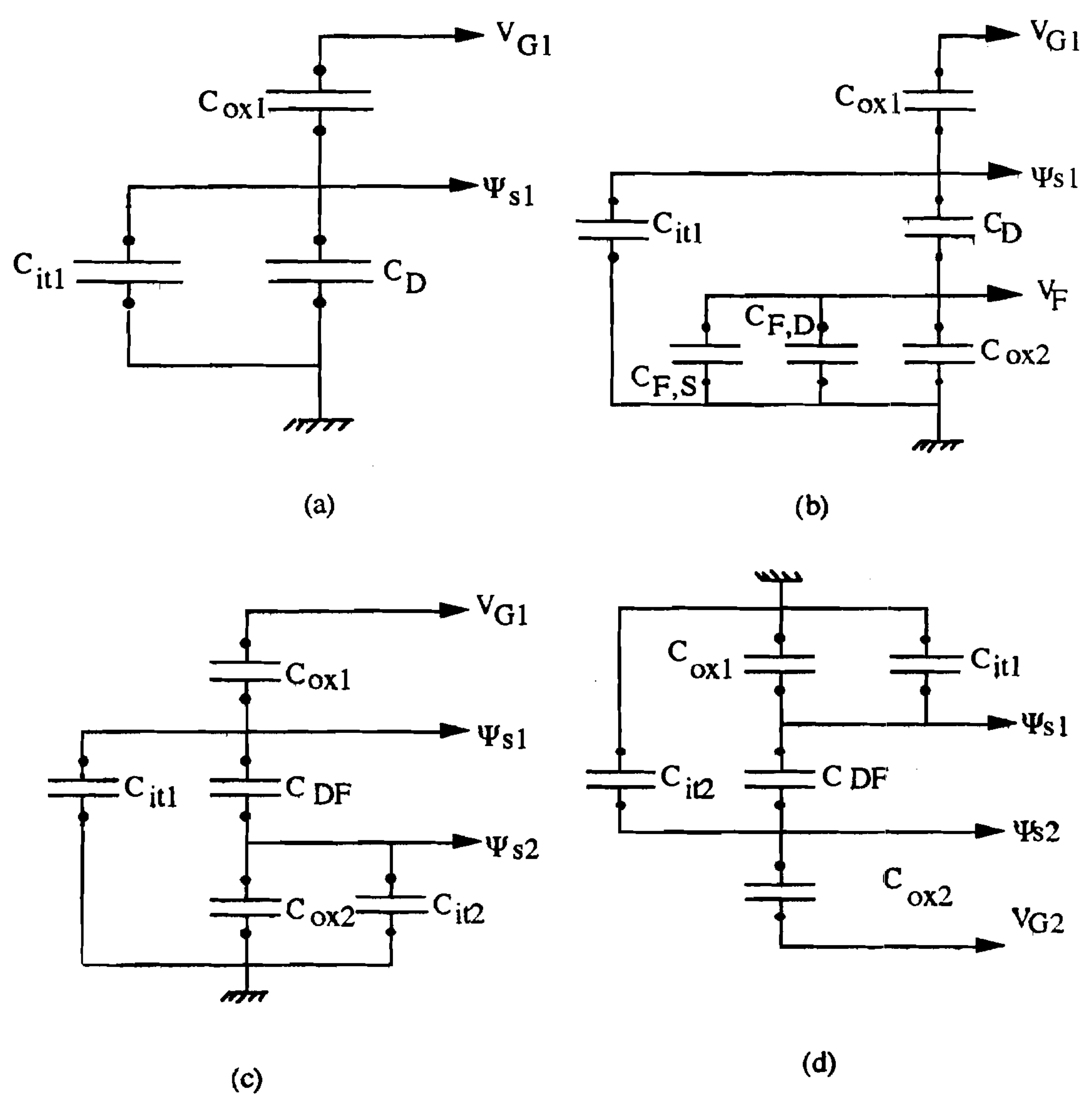


Figure 2.18 Equivalent capacitor models for (a) bulk MOSFET or thick-film MOSFET with film contact (b) Thick-film SOI MOSFET without film contact, Vf is the film potential (c)Thin-film fully depleted SOI MOSFET with front gate control (fixed back bias) and (d) Thin-film fully depleted SOI MOSFET with back gate control (fixed front bias)

$$S = \frac{\ln(10)}{\frac{d\ln(I_d)}{dV_G}} = \ln(10)\left[\frac{1}{\frac{1}{I_D}\frac{dI_D}{d\Phi_s}\frac{d\Phi_s}{dV_G}}\right] \qquad (23)$$

From the I_D expression of eqn. (22),

$$\frac{1}{I_D}\frac{dI_D}{d\Phi_s} = C = \frac{q}{kT} - \frac{\frac{d}{d\Phi_s}\left(\frac{-d\Phi_s}{dx}\right)}{\frac{-d\Phi_s}{dx}} \qquad (24)$$

The second term in C is a correction term that accounts for the reduction in current increase due to the increase of the surface electric field with increasing surface current (bias). So far the above expressions derived are general and applicable to both bulk and SOI MOSFETs. Qualitatively since the increase in surface electric field with increasing surface potential is lower for SOI MOSFETs, C in eqn. (24) is larger than in a bulk MOSFET. Generally, this correction term can be ignored and $C = q/kT$.

$$\therefore S = \frac{kT}{q}\ln(10)\frac{dV_G}{d\Phi_s} \qquad (25)$$

$\frac{dV_G}{d\Phi_s}$ *can* be determined for all cases using the capacitor divider networks.

Neglecting the presence of interface states, the expression for the sub-threshold slope S can be written for both bulk and SOI MOSFETs as [78],

$$S = \frac{kT}{q}\ln(10)(1+\alpha) \qquad (26)$$

where again $\alpha = C_{sub}/C_{ox}$, and the capacitance C_{sub} depends on the device structure as detailed in section 2.4.3. Since $\alpha_{FD,SOI} < \alpha_{bulk} < \alpha_{ACC,SOI}$, the inverse sub-threshold slope has the lowest (i.e. best) value in the fully depleted device, it is larger in the bulk device and even larger in the device with the back interface accumulated. Sub-threshold slopes are degraded when the back interface is accumulated, because this condition is similar to the thick-film case. In fact, it was determined that the slopes under accumulated back surface were worse than the bulk case. Depletion at the back surface does not change the sub-threshold slope; it affects only the threshold voltage. However, when the back

surface is inverted so that there is a channel current in the off-state, the sub-threshold slope decreases because of the poor control of the back channel current by the front gate voltage. The observed dependence of the sub-threshold slopes on the back surface potential is shown in figure 2.19. Thus, so long as the back surface is depleted, thin-film SOI MOSFETs provide superior sub-threshold slopes over corresponding bulk MOSFETs.

In short-channel devices however, an increase in sub-threshold slope results due to back surface leakage and DIBL [139]. Thin-film SOI MOSFETs then lose some of its advantages in the short-channel region. This is illustrated in figure 2.20. The degradation in sub-threshold slope is a lot lesser in thinner films. The curves in fig. 2.20 assume a back oxide thickness of 4000Å. The worsening sub-threshold slopes at short channel lengths can be reduced further by using thinner back oxides. Thinner back oxides would result in a slightly larger sub-threshold slope under long channel conditions due to the increase in the 'a' factor, but the degradation would be avoided. Once again, dual-gated devices would continue to provide extremely low sub-threshold slopes even at short channel lengths and would also provide excellent total dose radiation hardness due to the thinner back oxide. Balestra and Brini [79] recently proposed analytical expressions for the sub-threshold slopes based on the assumption that the potential distribution in the SOI film is linear. Based on their model, they investigated the parametric dependencies of the sub-threshold slope on the silicon film thickness, channel doping, and the back oxide thickness. In particular, it was shown that the subthreshold slope of the MOSFET increases as the back oxide thickness is reduced. This can also be deduced from the capacitor divider networks presented earlier. Thinner back oxides increase the back gate capacitance. This increases the back gate control over the channel and reduces the front gate control over the channel. Hence the sub threshold slope shows a slight degradation. In Chapter 3, a method to reduce the short-channel effects in a hot-carrier resistant design is presented, which involves thinning the back gate oxide. In light of the above dependence. such a design would be accompanied by higher inverse sub-threshold slopes. Thus SOI VLSI design implies trade-offs among the different parameters.

2.4.6 High Field Effects

The high electric fields near the drain of short-channel SOI MOSFETs give rise to hot-carrier effects just as they do in bulk MOSFETs. However, in addition to hot carrier

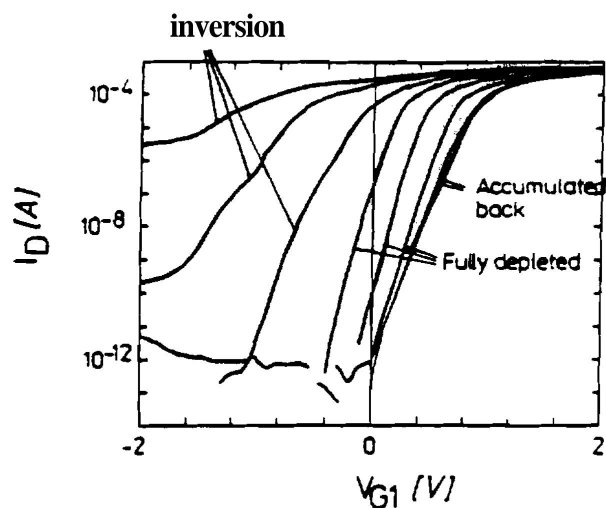


Figure 2.19 Measured subthreshold characteristics of a thin-film SOI n-channel MOSFET at different back gate voltages [78]

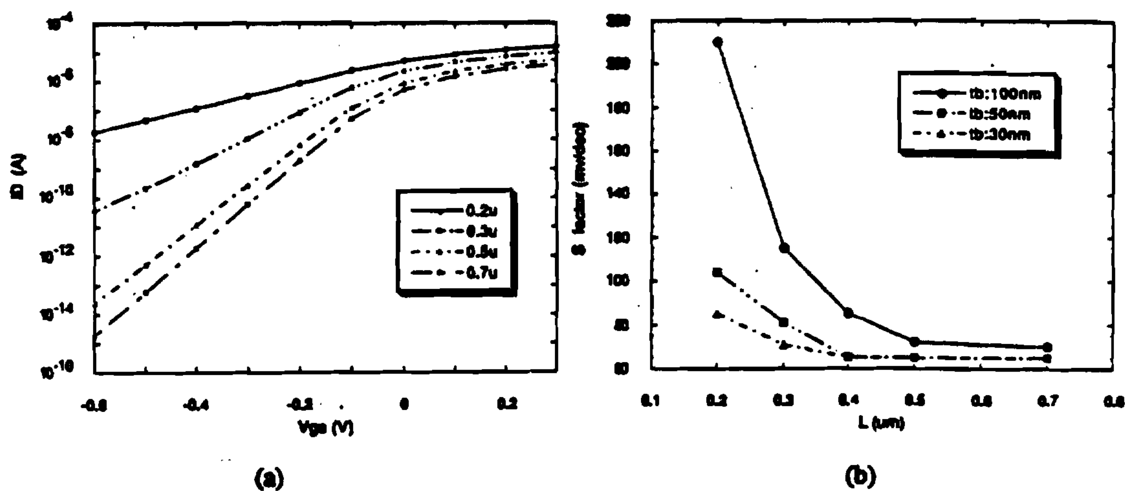


Figure 2.20 Simulated (a) subthreshold current versus gate-source bias and channel length (with t_b=100nm) and (b) gate-voltage swing versus channel length and film thickness of fully depleted SOI MOSFETs [139]

degradation, there are other deleterious effects due to the unique nature of the SOI device. These are the kink-effects and the parasitic bipolar effect. In this section each of these effects are discussed briefly, to give an overview of some of the major problems facing SOI technology today.

2.4.6.1 Hot Carrier Effects

The utility of short-channel devices is inherently dependent on the reliability of the devices. Reliability is directly related to the immunity of the devices to hot-carrier effects. The horizontal electric field in the transistor, which is roughly proportional to the ratio of the supply voltage to the gate length, increases as the device dimensions are reduced, When the transistor operates in the saturation mode, a high electric field develops between the channel pinch-off point and the drain junction. This electric field gives the electrons such a high energy that some of them can be injected into the gate oxide, thereby damaging the oxide-silicon interface [140]. At very high injection levels tunneling current through the gate can actually be measured [141]. The injected electrons cause shifts in the threshold voltage and the transconductance through the generation of interface states which begin to act as hole traps. Likewise, they also degrade the sub-threshold slopes and which results in a higher leakage current. Hot-carrier injection at the back interface (which is not as high in quality as the front interface to begin with) increases off-state leakage in SOI MOSFETs [142-143]. To first order the maximum drain electric field can be written as [87],

$$E_m = \frac{V_{DS} - V_{DS_{sat}}}{l_c} \tag{27}$$

where l_c is defined as the characteristic length given by, $l_c = t_{si}\left[\frac{C_b\beta}{2C_{ox_f}(1+a)}\right]^{1/2}$ and $a = \frac{C_{si}}{C_{ox_f}}$ for accumulated back surfaces and $a = \frac{C_{si}C_{ox_b}}{(C_{si}+C_{ox_b})C_{ox_f}}$ for depleted back surfaces. $\beta = 1$ for accumulated back surfaces and $\beta = 1+\frac{C_{si}}{C_{si}+C_{ox_b}}$ for depleted back surfaces. Therefore, the multiplication factor is lower for thin-film SOI MOSFETs because of the 'a' term in the expression for the characteristic length. This is illustrated in fig. 2.21, which presents the multiplication factor in bulk and fully depleted SOI MOSFETs of similar geometry.

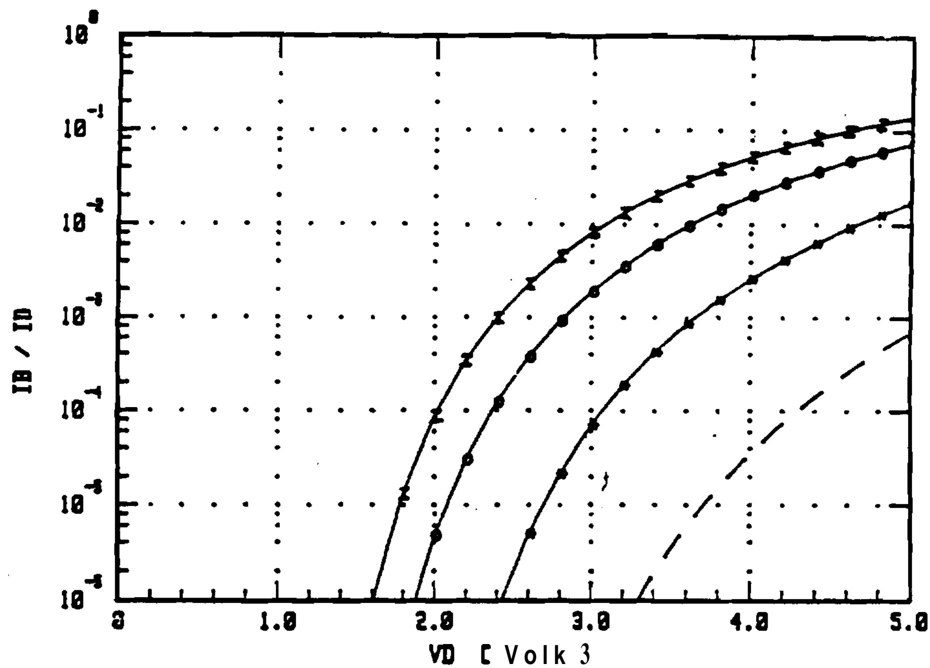


Figure 2.21 Simulated (M-1) versus V_{DS} for n-channel SOI MOSFETs [fully depleted, with film thicknesses of 100nm (*) and 300nm (-), and back surface accumulated, with film thicknesses of 100nm (I)] contrasted with a bulk MOSFET (o) [87]

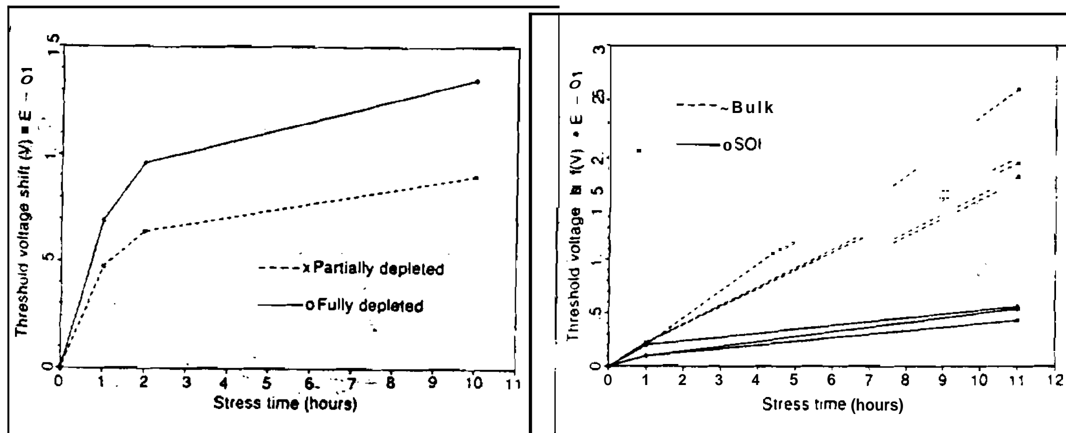


Figure 2.22 Threshold voltage shift as a function of electric field stess time in (a) bulk MOSFETs and partially depleted SOI MOSFETs and (b) partially and fully depleted SOI MOSFETs [69]

Short-channel bulk MOSFETs require complex processing and lightly doped drain structures to lower the drain electric field and reduce hot-carrier effects. SOI MOSFETs have been shown to have reduced hot-electron related degradation of threshold voltages and transconductances compared to their bulk counterparts [80]. In Fig. 2.22, the threshold voltage degradation in thin-film fully depleted SOI MOSFETs, thick-film partially depleted SOI MOSFETs and bulk MOSFETs are compared under similar stressing conditions. Thin-film fully depleted MOSFETs showed the least amount of hot-carrier degradation. The maximum drain electric field E_m is a function of the drain saturation voltage $V_{d\ sat}$. The lower the $V_{d\ sat}$, the higher the electric field. In section 2.4.3, it was stated that the drain saturation voltage of thin-film MOSFETs is greater than that in a bulk MOSFET. due to the fully depleted channel from source to drain. Therefore, the maximum drain electric field is lower in thin-film MOSFETs which results in lower hot-canrier-degradation. However, it has been observed that the drain electric field in ultra-thin SOI-MOSFETs increases considerably due to two-dimensional effects [81-85] resulting in lower breakdown voltages. Design rules for these MOSFETs require the presence of LDD regions, similar to the case of bulk MOSFETs [86]. For minimum hot-carrier-induced degradation. SOI MOSFETs with moderately thin (not ultra-thin) films must be fabricated [87]. In such cases, it has been shown through numerical simulations that the multiplication factor at the drain of the SOI device without LDD is in fact less than that in a bulk device with LDD. For lower drain electric fields, it is required that the back film interface be maintained in depletion i.e. the silicon film must be fully depleted. Accumulated back interfaces increase the electric field at the drain and result in degraded hot-carrier-induced-lifetimes. Thus. SOI-MOSFETs at worst would have the same hot-carrier-related problems as bulk MOSFETs and would require similar drain engineering. But, because of the ability to vary the silicon film thickness, it may be possible to design the SOI MOSFET with thicker films and acceptable short-channel effects [87], resulting in enhanced device performance over bulk MOSFETs.

2.4.6.2 Kink Effect

Floating substrate effects have been observed in bulk MOSFETs [88, 89] but only under specific conditions and low temperatures. In general, floating substrate effects are unique to SOI MOSFETs. First evidence of floating substrate effects (also referred to as the "Kink Effect") were found in thick-film SOS transistors and thick-film partially

depleted SOI MOSFETs [90-95]. Kink-effects have also been observed in thick-film partially depleted SOI MOSFETs. In partially depleted thick-film SOI MOSFETs (weak) impact ionization at the drain produces electron-hole pairs; the electrons are swept into the drain whereas the holes are injected into the substrate. This situation is similar to the one observed in bulk MOSFETs. If there were a bulWsubstrate contact, the generated holes would recombine at the contact and constitute the substrate current. However, in the absence of a substrate contact, the holes accumulate at the substrate and forward bias the source-body junction as depicted in figure 2.23 (a). The substrate develops a positive potential V_{BS} in order to lower the barrier at the source junction. The potential V_{BS} adjusts itself to maintain equilibrium between the generation rate of holes and the recombination at the source. The positive potential V_{BS} of the substrate results in a body-effect, similar to bulk MOSFETs, and decreases the threshold voltage of the device. This reduction in threshold causes a lank in the output characteristics as shown in Fig. 2.24.

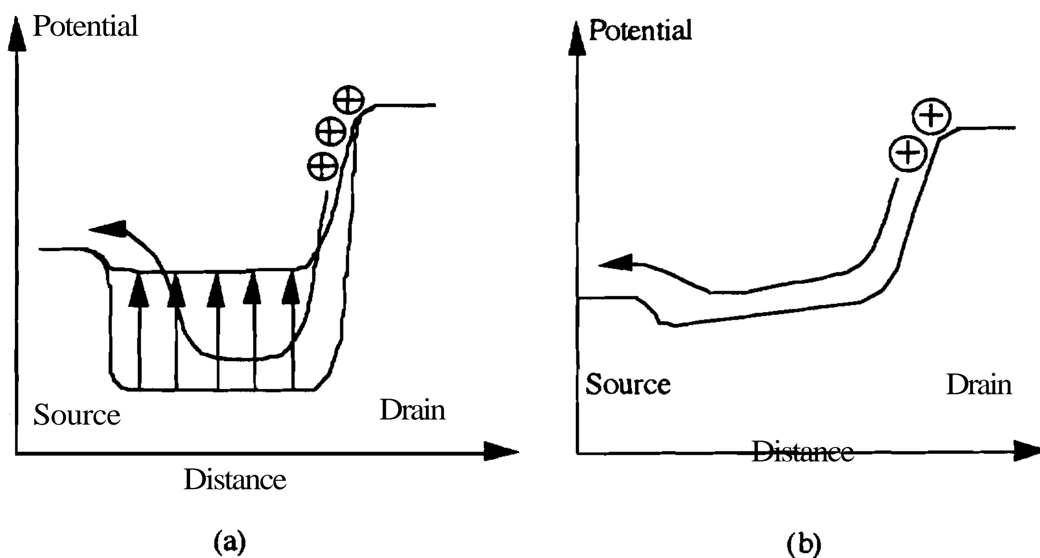


Figure 2.23 (a) Potential in the neutral region from source to drain in the Partially depleted device before and after the onset of the lank effect (lower and upper curves, respectively) (b) Potential from source to drain in the fully depleted device

Kink effects in SOI and SOS MOSFETs have been modeled both analytically [96] and using two-dimensional numerical simulations [97]. The kink effect is responsible for the observation of anomalous sub-threshold slopes for partially-depleted SOI MOSFETs [98,99]. When the body floats, the (relatively weak) impact ionization that aan occur near the drain in the sub-threshold region (in addition to the other carrier generation mechanisms) can result in holes being injected into the neutral body. The hole injection charges the body and produces a forward bias on the body-source junction, which reduces the threshold voltage while the device operates in the sub-threshold region. As a result. the sub threshold current jumps from a high-V_{th} characteristic to a low-V_{th} curve and gives rise to a very steep sub-threshold slope. The steep sub-threshold slopes disappear in fully depleted MOSFETs, which lends credence to their association to the kink effect phenomenon. Moreover, the kink effect causes significant drain current overshoots [100] in the transient characteristics of the MOSFET. Therefore, in summary, the kink effects are not wholly desirable. One way to avoid the kink effect is to incorporate a substrate contact to the device. The holes generated by impact ionization would then recombine at the substrate contact rather than accumulate in the bulk. This is akin to the behavior in bulk MOSFETs. However, incorporating a substrate contact results in a more complicated fabrication process and increases the active device area It has been demonstrated that the use of thin-film fully depleted MOSFETs effectively eliminates the kink in the output drain characteristics [101,102]. Thin-film fully depleted MOSFETs have a significantly lowered source to body potential barrier compared to partially depleted MOSFETs as shown in Fig. 2.23 (b), The majority carrier holes generated at the drain can therefore more easily recombine at the source. There is, as a result, a minimal body-effect which in turn results in the disappearance of the kink. Fig. 2.24 again shows the nullified kink-effect in the fully-depleted devices. The devices can be either extremely thin-film and fully depleted at all times, or thick-film and fully depleted by applying a back gate voltage. If a negative back bias is used to induce an accumulation layer at the back interface, the device behaves as a partially depleted device, and the kink reappears [101].

2.4.6.3 Parasitic Bipolar Effects

There exists a parasitic bipolar transistor in every MOS structure. If we consider an n-channel device, the N+-source, p-type body, and the N+-drain form the emitter, base and collector of an NPN bipolar transistor. In a bulk device, the base of the bipolar transistor is

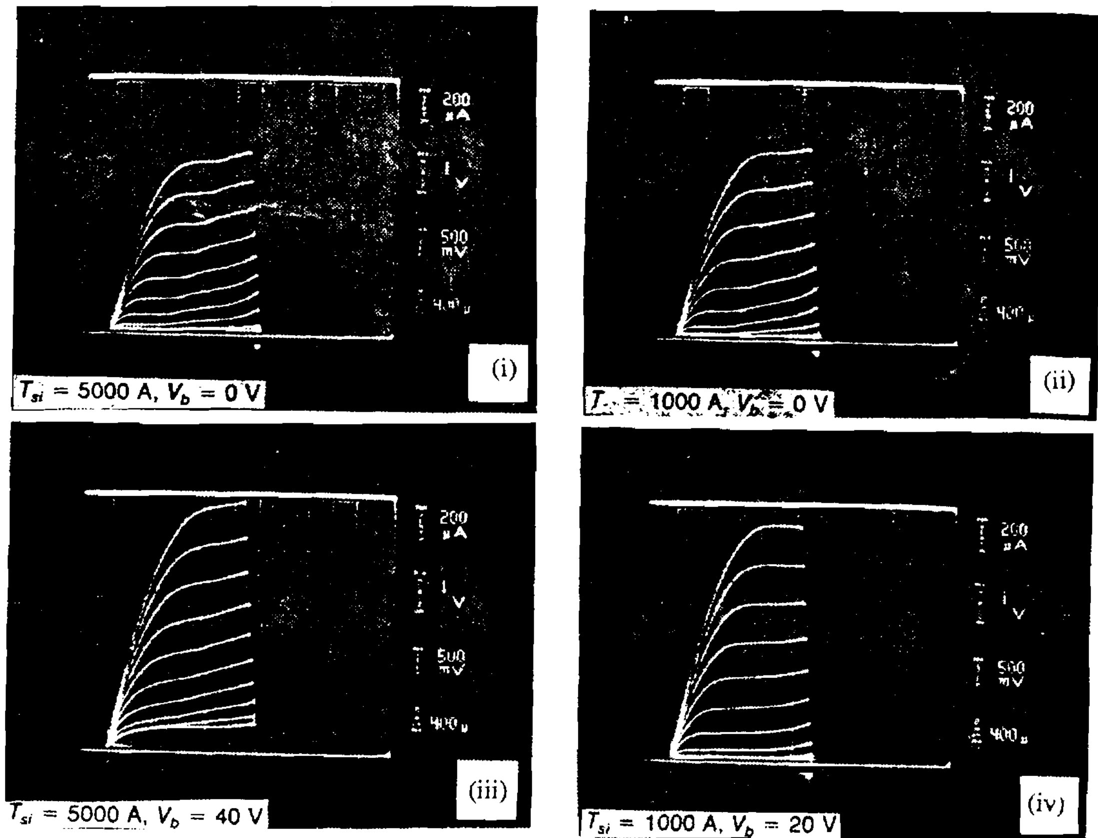


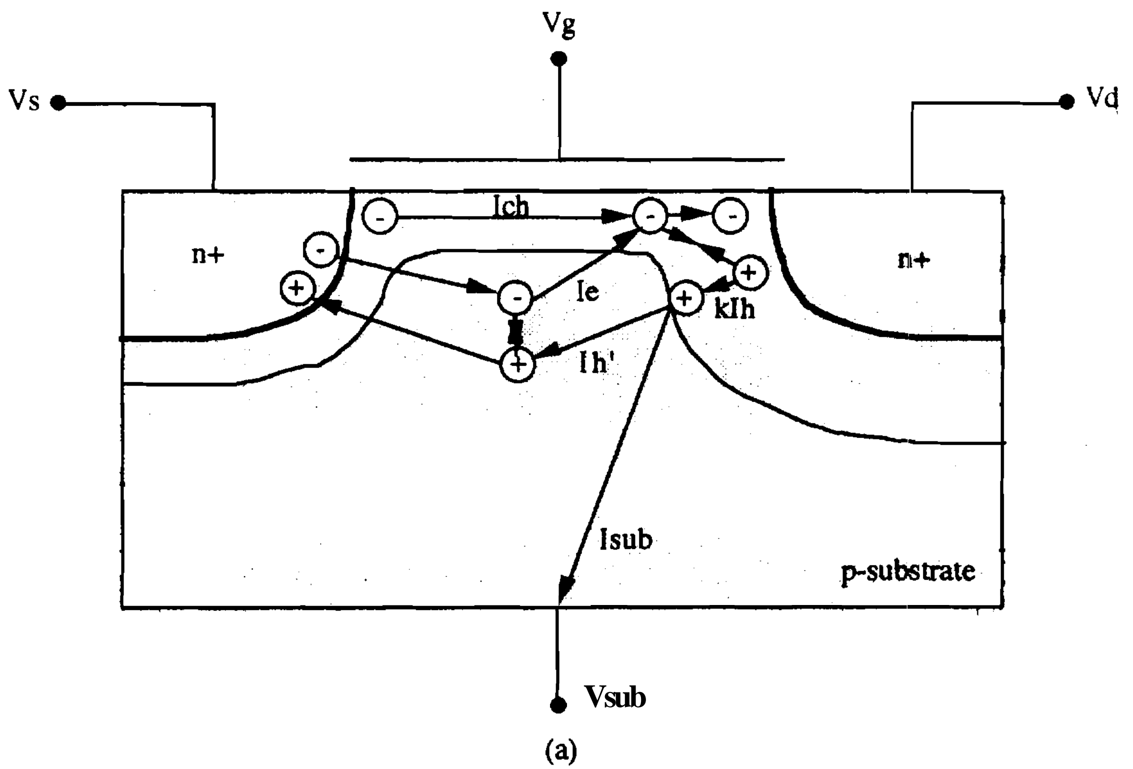
Figure 2.24 Output characteristics of two transistors, one made in a 500nm thick SOI film and the other made in a 100nm thick film. Only the device in (iv) is fully depleted and does not show the 'kink' [69]

usually grounded by means of a substrate contact. In an SOI device, however the body (base) is usually left floating. This parasitic bipolar transistor is the origin of two major undesirable effects in SOI devices: (a) the single transistor latch and (b) the reduction of the drain breakdown voltage.

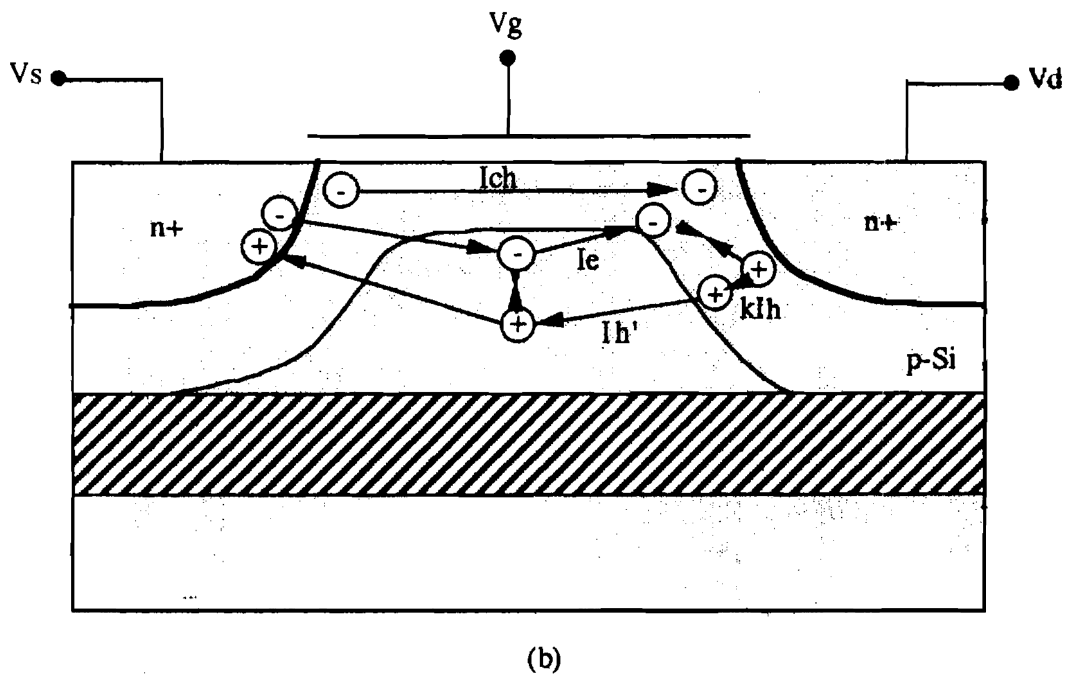
2.4.6.3.1 Reduced Drain Breakdown Voltage

The kink-effect is inherently tied in with the drain breakdown phenomena in thin-film SOI MOSFETs. Clearly, the cause for both the effects is the same, namely, impact ionization at the drain. Thin-film SOI MOSFETs while demonstrating eliminated kink-effects, also show a significantly reduced drain breakdown voltage [103-105]. The reduced breakdown voltage is due to the parasitic bipolar action in thin-film MOSFETs. The parasitic bipolar, an n-p-n transistor for a n-channel MOSFET, is formed by the n+-source, the p-body and the n+-drain. The impact ionization generated holes serve as the base current for the lateral bipolar transistor, on injection into the source. This causes a back injection of electrons from the source which add to the channel inversion electrons. These electrons in turn impact ionize at the drain enhancing the base current and thus turning the bipolar transistor on. The regenerative action eventually leads to device breakdown. The breakdown mechanism is similar to that in bulk MOSFETs but is exacerbated by the absence of the bulk-substrate contact. Fig. 2.25 gives a pictorial explanation for the breakdown mechanism in bulk and SOI MOSFETs. Bipolar snapback effects in the sub threshold region, due to the activation of the parasitic bipolar transistor have also been observed experimentally [106-107]. A complete analysis of the floating body effects in SOI MOSFETs and its effect on the breakdown and bipolar latch-up phenomena based on two-dimensional, two-carrier numerical simulations has recently been published [108].

Although thin-film devices do not show any discernible kink effects, the quasi-fermi level separation between the source and the body (which determines the forward bias potential V_{BE} for the emitter-base junction of the parasitic BJT) is greater for the thin-film devices than it is for the thick-film devices. The reason for this can be qualitatively described as follows. The forward bias developed across the source-body junction determines the injection and subsequent recombination of holes in the quasi-neutral



(a)



(b)

Figure 2.25 Schematic diagram showing current flow in (a) bulk-silicon and (b) SOI n-channel MOSFETs operated in the saturation regime.

source[1]. The thinner films have larger drain electric fields and therefore a greater generation of holes. Coupled with the fact that the thinner films provide a smaller volume for recombination, the forward bias developed in the thinner films must be greater to maintain the equilibrium between carrier generation and recombination. Therefore, to state that the substrate potential does not increase in the thin-film MOSFETs would be incorrect. The substrate potential does indeed increase as the above argument suggests. However, since the thin-film devices are fully depleted, its depletion charge is largely independent of the substrate bias and therefore the thin-film devices are less prone to the body effect which causes the kink in the partially depleted devices. Furthermore, due to the substantial forward bias developed across the body-source junction (base-emitter junction for the lateral BJT), the thin-film SOI MOSFETs show a drastic reduction in breakdown voltages due to parasitic bipolar action. The thinner the film, the more pronounced the parasitic bipolar and the lower the breakdown voltage. The smaller breakdown voltages in thin-film devices versus those with thicker films have also been observed experimentally [109].

The breakdown voltage of thin-film SOI MOSFETs thus depends on both the electric field (and multiplication) at the drain as well as on the emitter injection efficiency and current gain of the lateral bipolar transistor. Schemes to increase the breakdown voltage by decreasing the drain electric field [110] and decreasing the current gain [109] have been proposed. Decreasing the current gain implies the use of a lightly doped source to reduce the injection efficiency. This has its repercussions on the transconductance and current drive due to increased source resistance. Intentionally incorporating lifetime lulling trap centers in the MOSFET body also reduces the gain of the parasitic transistor, but would result in enhanced leakage currents in the drain and source depletion regions. The leakage current at the drain is another source for the base current and its increase is undesirable. Electric fields at the drain can be reduced by either using thicker films or by incorporating LDD regions. A novel way to reduce the drain electric field by using a drain thickened structure has been recently proposed [110]. The drain regions of the device are made in thicker material while the channel region is made in thinner material. No viable technique to fabricate such a device has been presented so far.

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[1] The recombination in the SOI MOSFETs is more dominant in the quasi-neutral source than at the junction. The transverse electric field in the channel region physically seperates the electrons and the holes at the source-body junction, greatly reducing their probability of recombination.

2.4.6.3.2 Single Transistor Latch

The single transistor latch phenomena is qualitatively described in figure 2.26 and is again a direct result of the parasitic bipolar transistor in fully depleted SOI MOSFETs.

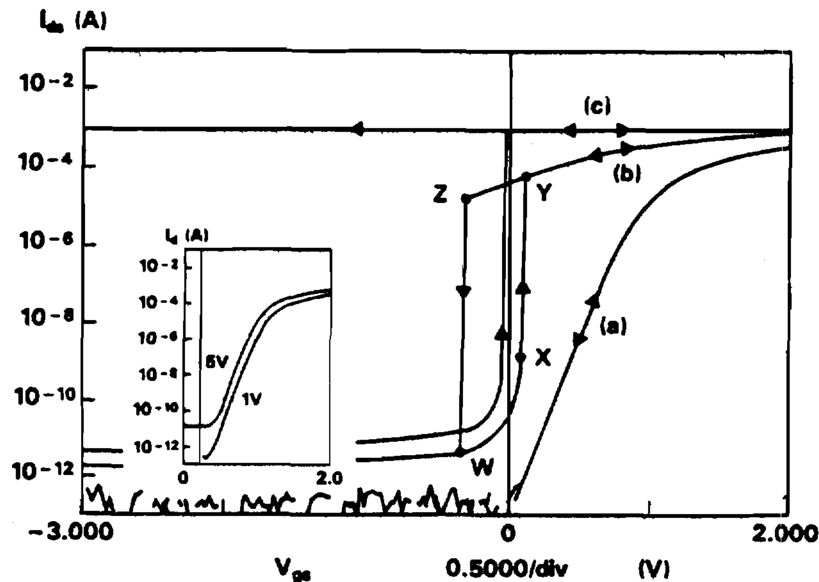

Figure 2.26 Illustration of the single transistor latch [106]. Curve (a) depicts the normal sub threshold characteristic at low drain voltage, curve (b) illustrates the anomalistically sharp sub threshold slope due to the bipolar action and finally curve (c) shows the device in the latched state

The single transistor latch results due to the triggering of the parasitic bipolar transistor in the sub-threshold region. If the drain voltage is high enough, impact ionization can occur in the sub threshold region even though the drain current is very small. In the figure, at low drain biases, a normal sub threshold characteristic is obtained under both forward and reverse voltage scan conditions (curve a). If the drain voltage is increased (curve b), the impact ionization near the drain increases and raises the body potential. This reduces the

threshold voltage under the forward gate voltage scan and leads to an anomalistically sharp increase in the drain current. As the drain current increases, so does the impact ionization and a positive feedback is maintained. During the descending voltage scan, the regenerative impact ionization mechanism under the large drain bias keeps the body voltage high and the threshold voltage low. A high drain current is observed until the gate voltage drop below the value required to maintain positive feedback. Once this point is reached the drain current suddenly drops. As a consequence, a hysteresis is observed in the sub threshold characteristics in curve b. If the drain bias is large enough the positive feedback loop cannot be turned off once it is triggered and the device cannot be turned off even if the gate voltage is reduced (curve c). The device is then said to be latched. Such parasitic latch phenomena can directly affect the switching behavior of CMOS circuits fabricated using fully-depleted SOI MOSFETs [142]. Consider for example a simple CMOS inverter. During the pull-down transient, the drain is at a high voltage and the gate is low. If the input voltage rise time is sharp then there could be a sufficient channel current in the n-channel device while its drain voltage is high, thus triggering the bipolar latch. This would increase the current flowing through the n-channel device and increase the discharging of the output node. The latch is not maintained in the steady state, because the drain voltage quickly becomes low. During the pull-up transient, the gate voltage is initially high and the drain voltage is low. If the fall time is slow or the leakage currents are significant, then the device will latch during the pull-up transient and would remain latched even when the gate voltage becomes zero. The latch is thus maintained under steady state conditions and results in tremendous standby-by power consumption. Therefore, although there may be potential advantages of the latch during the pull-down transient, the increased power consumption in steady state makes the latch undesirable and steps must be taken to nullify or minimize its occurrence.

2.4.7 General Comments

A number of devices have been fabricated in both SIMOX and ZMR films and have been shown to demonstrate any or all of the aforementioned properties [Ill-1201. Based on trade-offs involved in device design and fabrication, various design criteria for sub micron SOI devices have also been proposed [121].

Finally, a number of device models have been proposed to more accurately characterize the device behavior in thin-film SOI-MOSFETs. An equilibrium electrostatic model based on the solution of the one-dimensional Poisson's equation was formulated [122] to explain the sub threshold characteristics in thin-film polysilicon MOSFETs. An extension of this model to the strong inversion regime based on the Pao-Sah single integration approach has also been formulated [123-125]. The above models however assume a bulk-substrate contacted device. The electrostatic analyses are not accurate for typical floating-body SOI MOSFETs. A more accurate model for floating body SOI MOSFETs has been proposed by Pierret [126]. Computations based on this model are presented in the next chapter to explain volume-inversion in dual-gate controlled MOSFETs. Two-dimensional numerical models based on the solution of the two-dimensional Poisson formulation and Monte-Carlo techniques have also been used to explain the ameliorated short-channel effects in thin-film MOSFETs [127-131].

2.5 Summary

The limitations of bulk MOSFETs in the short-channel regime were detailed. The properties of thin-film SOI MOSFETs with regard to circumventing the deleterious problems associated with bulk MOSFETs were described in detail. In particular, the higher drain saturation voltage and saturation currents, improved sub-threshold slopes, significantly enhanced immunity to short-channel effects, and the reduction of the kink-effect were described. A major concern in thin-film SOI-MOSFETs is the low breakdown voltage due to the parasitic bipolar action. The breakdown mechanisms were reviewed in detail.

Technologies used to fabricate SOI devices were enumerated and the two major technologies SIMOX and ZMR were discussed. Selective epitaxial growth of silicon was introduced as a potentially advantageous means of forming high quality SOI material. This is of particular importance when minority carrier devices are to be integrated into a SOI process.

2.6 References

1. J.E. Hall, J.A. Seitchik, L.A Arledge and P. Yang , "An improved circuit model for CMOS Latchup", ***IEEE EDL-6 (7),*** July 1985.

2. S.Liu, B. Hoefflinger and D.O. Pederson, "Interactive two-dementional design of Barrier-controlled MOS transistors".***IEEE ED - 27 (8),*** pp 1497. August 1980.

3. J.R. Brews, "Physics of the MOS Transistor". ***Applied Solid State Science, Supplement 2A,*** Academic Press. 1981.

4. P.K. Chatterjee and J.E. Leiss, "An Analytic Charge-Sharing Predictor Model For Submicron MOSFETS", ***IEDM Tech. Dig.*** pp 28. 1980.

5. T. Toyabe and S. Asai, "Analytical Models of Threshold Voltage and Breakdown Voltage of Short-Channel MOSFETs Derived from Two-Dimensional Analysis", ***IEEE ED-26 (4),*** pp. 453, 1979.

6. R.R. Troutrnan. "VLSI Limitations from Drain-Induced Barrier Lowering", ***IEEE ED-26 (4),*** pp. 461, April 1979.

7. B. Hoeneisen and C.A. Mead. "Fundamental limitations in micro-electronics- I. MOS Technology". ***Solid-State Electron.,*** vol.15, pp. 819, 1972.

8. R.R. Troutman. "An investigation of punchthrough between two ungated diffusion pockets", ***IBM Tech. Rep.,*** TR 19.0224, Jan 1972.

9. I.M. Bateman, G. A. Armstrong and J. A. Magowan, "Drain voltage limitations of MOS transistors", ***Solid-State Electron.,*** vol. 17, pp. 539, 1974.

10. R.M. Swanson and J.D. Meindl, "Fundamental performance limits of MOS integrated circuits", ***IEEE Int. Solid-State Circuits Con. Dig. Tech. Papers,*** pp. 110, 1975.

11. R.A. Stuart and W. Eccleston, "Punchthrough currents in short-channel MOST devices," ***Electron Letters,*** vol.9 , pp. 586, Dec. 1973.

12. J.J. Barnes, K. Shimohigashi and R.W. Dutton, "Short-Channel MOSFETs in the Punchthrough current mode", ***IEEE ED-26 (4),*** pp ***446,*** April 1979.

13. TMA - PISCES IIb Users Manual, Technology modeling Assosiates, 1988.

14. A.G. Sabinis and J.T. Clemens, "Characterization of the Electron Mobility in the Inverted <100> Si Surface.", ***IEDM Tech. Dig.,*** pp 18, 1979.

15. S.S. Chung and C.T. Sah, "A Subthreshold Model of the Narrow-Gate Effect in MOSFETs", ***IEEE ED-34 (12),*** pp. 2521, Dec. 1987.

16. P.E. Cottrell, R. Troutman and T.H. Ning, "Hot-Electron Emission in N-Channel IGFETs.", ***IEEE ED - 26,*** pp 520, April 1979.

17. B. Eitan and D.F. Bentchkowski, "Hot-Electron Injection into the Oxide in N-Channel MOS Devices.", IEEE ED - *28,* pp **328, 1981.**

18. C. Hu, "Hot-Electron Effects in MOSFETs", IEDM Tech *Dig.,*pp **176,1983.**

19. S.C. Sun and J.D. Plummer, "Electron Mobilitv in Inversion and Accumulation Layers on Thermally Oxidized Silicon surfaces.", IEEE *ED* - 27 *(8),* pp **1497,** Aug **1980.**

20. D.M. Caughey and R.E. Thomas, "Camer Mobilities in Silicon Empirically Related to Doping and Field.", *Proc.* IEEE, pp **2192, Dec** 1967.

21. J.J. Sanchez, K.K. Hsueh and T.A. DeMassa, "Drain-Engineered Hot-Electron-Resistant Device Stuctures : A Review", IEEE ED-36 *(6),* pp. **1125,** June **1989.**

22. S. Ogura, P.J. Tsang, W.W. Walker, D.L. Critchlow and J.F. Shepard, "Design and Characteristrics of the Lightly Doped Drain-Source (LDD) Insulated Gate Field-Effect Transistor", IEEE ED-27 *(8),* pp. **1359,** Aug. 1980.

23. H. Mikoshiba, T. Horiuchi and K. Hamano, "Comparison of Drain Structures in n-channel MOSFETs", IEEE ED-33 *(1),* pp. 140, Jan. 1986.

24. Y.Toyoshima, H. Nihara, M. Wada and K. Kanzaki, "Mechanisms of hot-electron induced degradation in LDD NMOS-FET", IEDM *TEch.* Dig., pp. **786, 1984.**

25. S. Bampi and J.D. Plummer, "A modified lightly doped drain structure for VLSI MOSFETs", IEEE ED-33, pp. **1769, 1986.**

26. M.C Jeng, J.E. Chung, P.K. Ko and C.Hu, 'The Effect of Source/Drain Resistance on Deep Submicrometer Device Performance ", IEEE ED - 37 *(11),* pp 2408, Nov **1990.**

27. K.Y. Chiu et al, "The SWAMI - A defect free and near-zero Bird's beak local oxidation process and its application in VLSI Technology," *IEDM* Tech. *Dig.,***pp. 224, Dec. 1982.**

38. B.Y. Mao, M. Matloubian, C.E. Chen, et al, 'The Effect of Post-Oxygen-Implant Annealing Tempreture on the Channel Mobilities of CMOS Devices in Oxygen-Implanted Silicon-on-Insulator Structures, IEEE EDL - *8 (7),* pp 306, **1987.**

29. G.W. Cullin, M.T. Dubbey and R.K. Smeltzer, "Recent Advances in the Heteroepitaxy of Silicon on Sapphire Technology.", *Symp* on VLSI, vol 84 (7), pp 230, May **1984.**

30. G.A. Garcia, R.E. Reddy and M.I. Burgener, "High-Duality CMOS; in Thin (100nm) Silicon-on Sapphire.", IEEE EDL - 9 *(1),* pp **32,** Jan **1988.**

31. K. Sugahara et al, "SOI / SOI / Bulk-Si Triple-Level Structure for Three-Dimensional Devices.", IEEE EDL - 7 *(3),* pp 193, Mar **1986.**

32. P.K. Vasudev, "Recent Advances in Solid-Phase Epitaxial Recrystallization of SOS with Applications to CMOS and Bipolar Devices.", IEEE Circ. and *Dev.*, vol 3 (4), pp 17, July 1987.

33. J. Haisma, "SOI Technologies - Their Past, Present and Future.", *ESS* DRC *Proc.*, pp C4 - 3, Sept 1988.

34. P.K. Vasudev and D.C. Mayer, "Solid Phase Recrystallization of SOS.", *Proc. 1984,* MRS, Thin Film Transistors and Silicon on Insulators, vol 35, pp 35, 1984.

35. T.Inoue and T. Yoshii, "Double Solid-Phase Epitaxy of SOS.", *Appl.* Phys. *Lett.*, vol 36, pp 64, 1980.

36. H.E. Cline, "Silicon Thin Films Formed on Insulator by Recrystallization.", J. *Appl.* Phys., vol 55, pp 2910, April 1984.

37. B.Y. Tsaur, "Zone-Melting Recrystallization Silicon-on-Insulator Technology.", IEEE Circ. and *Dev.*,vol 3 (4), pp 12, July 1987.

38. M. Haond et al, "Electrical Performances of Devices made in SOI Films obtained by Lamp ZMR.", IEEE Circ. and Dev. , vol 3 (4), pp 27, July 1987.

39. B.Y. Tsaur et al, "SOIICMOS Circuits Fabricated in Zone-Melting-Recrystallized Si Films on Sic-Located Si Substrates.", IEEE EDL - *4,* pp 398, 1982.

40. D. Bursky, "Laser Recrystallization Stratifies Three Levels of Silicon on a Single Chip.", Electronic Design, vol 33, pp 68, May 1985.

41. H.W. Zaur, "SIMOX SOI for Integrated Circuit Fabrication.", IEEE Circ. and Dev., vol 3 (4), pp 6, July 1987.

42. K. Izumi, M. Dohen and H. Ariyoshi, "CMOS Devices Fabricated on Buried SiO_2 Layers formed by Oxygen Implantation into Silicon.", *Electronics* Letters, vol 114 (18), pp 593, Aug 1978.

43. K. Oniuada, Y. Omura and E. Sauo, " A High-Speed Buried Channel MOSFET Isolated by an Implanted Silicon Dioxide Layer.", IEEE ED - 28 *(9),* pp 1084, Sept 1981.

44. T. Ohno, K. Izumu, M. Shimaya and N. Shiono , "Total Dose Effects of Gamma-Ray Irradiation on CMOS/SIMOX Devices.", IEEE Circ. and *Dev.*, Nov 1987.

45. S. S. Tsao, "Porous Silicon Techniques for SOI Stuctures ", IEEE Circ. and *Dev.*, Nov 1987.

46. K.Barla, G. Bomchil, R. Herino and A. Honroy, "SOI Technology using Buried Layers of Oxidized Porous Si.", IEEE Circ. and Dev., Nov 1987.

47. E.J. Zorinsky, D.B. Spratt and R.L. Vinkus, "The ISLANDS Method - A Manufacturable Porous Silicon SOI Technology.", *IEDM Tech. Dig.*, pp 431, 1986.

48. J.B. Lasky, "Wafer Bonding for Silicon - on - Insulator technologies.", *Appl. Phys. Lett.* , vol 48 (1), pp 78, Jan 1986.

49. H. Ishiwara. M. Tanaka and S. Lurukawa, "Lateral Solid Phase Epitaxy in Selectively P - Doped Imorphous Si. Film.", *Appl. Phys. Lett,* vol 49 (20), pp 1363, Nov 1986.

50. Y. Kunii, M. Tabe and K. Kajiyama. "Solid-Phase Lateral Epitaxy of CVD Amorphous Silicon by Furnace Annealing.", J. *Appl. Phys.,* vol 54 (5), pp 2847. May 1983.

51. B. Davari et al, "A new planarization technique using a combination of RIE and Chemical Mechanical Polishing (CMP)", *IEDM Tech. Dig.* , pp. 61, 1989.

52. L. Jastrzebski, J.F. Lovboy and R. Pagliaro, "Growth of Electronic Quality Silicon over Oxide by Epitaxial Lateral Overgrowth.", J. *Electrochem. Soc.,* vol 129, pp 2645, 1982.

53. J.A. Friedrich and G.W. Neudeck, "Oxide Degradation during Selective Epitaxial Growth of silicon.", J. *Appl. Phys.,* vol *64* (7), pp 3538, Oct 1988.

54. J.A. Friedrich, 'Three-Dimensional MOS Process Development.". Phd Dissertation, Purdue University, 1988.

55. R.P. Zingg, "Local Epitaxial Overgrowth for Stacked Complementary MOS Transistor Pairs.". Phd Dissertation, Purdue University, 1990.

56. J.A. Friedrich and G.W. Neudeck, "Interface Characterization of Silicon Epitaxial Lateral Growth over Existing Si02 for Three - Dimensional CMOS Structures.", *IEEE EDL - 10 (4),* pp 144, April 1989.

57. G. Shahidi et al , "Fabrication of CMOS on Ultra-thin SOI obtained by Epitaxial Lateral Overgrowth and Chemical-Mechanical Polishing", *IEDM Tech. Dig.,* 1990.

58. P. J. Schubert, "Study of a new silicon epitaxy technique: Confined Lateral Selective Epitaxial Growth", *PhD Dissertation,* Purdue University, May 1990.

59. P.J. Schubert and G.W. Neudeck. "Vertical Bipolar Transistors fabricated in local silicon-on-insulator films prepared using CLSEG", *IEEE ED-37*, pp 2336, Nov. 1990.

60. P.J. Schubert and G.W. Neudeck. "Confined Lateral Selective Epitaxial Growth of Silicon for Device Fabrication", *IEEE EDL-11 (5),* pp. 181, May 1990.

61. R.F. Pierret, "Field Effect Devices.", vol 4, Modular Series on Solid State Devices. ed. R.F. Pierret and G.W. Neudeck. Addison Wesley, 1983.

62. H. Lim and J. Fossum. "Current - Voltage Characteristics of Thin - Film SOI MOSFETs in Strong Inversion.", *IEEE ED - 31 (4),* pp 401, April 1984.

63. J.C. Sturm, "Performance Advantages of Submicron Silicon- on-Insulator Devices for ULSI.", Mat Res. *Soc.* Symp. Proc., vol 107, pp 298, 1988.

64. J.C. Sturm, T. Tokunaga and J.P. Colinge, "Increased Drain Saturation Current In Ultra-Thin Silicon-on-Insulator (SOI) MOS Transistors.", IEEE EDL - 9 (*11*), Sept 1988.

65. J.C. Sturm and T. Tokunaga, "Dependence Transconductance on Substrate bias in Ultra-Thin Silicon-on-Insulator MOS Transistors.", Electronics *Letters,* vol 25 (18), pp 1233, Aug 1989.

66. M. Yoshimi et al, "Observation of Mobility Enhancement in Ultra-Thin SOI MOSFETs.", Electronics Letters, vol 24 (17), pp 1078, Aug 1988.

67. Y. Yamaguilu et al, "Improved Characteristics of MOSFETs on Ultra-Thin SIMOX." *IEDM* TECH. Dig.. pp 825, 1989.

68. C. Duvvury, "A Guide to Short Channel Effects in MOSFETs.", *IEEE* Circ *and* Dev., vol 2 (6), pp 6, 1986.

69. J.P. Colinge, "Some Properties of Thin - Film SOI MOSFETs.", IEEE Circ. *and* Dev., Nov. 1987.

70. S.M. Sze, "Physics of Semi Conductor Devices.", John Wiley & Sons, pp 474, 1981.

71. K.K. Young, "Short Channel Effect in Fully Depleted SOI MOSFETs.", IEEE ED - *36 (2),* Feb 1989.

72. S. Veeravaghavan and J.G. Fossum, "Short Channel Effects in SOI MOSFETs.", IEEE ED - *36 (3),* Mar 1989.

73. S. Veeravaghavan and J.G. Fossum, "A Physical Short Channel Model for the Thin - Film SOI MOSFETs Applicable to Device and Circuit CAD.", IEEE ED - *35 (11),* Nov 1988.

74. J.P. Colinge and T.I. Kamins, "CMOS Circuits made in Thin SIMOX Films.", Electronics Letters, vol 23, pp 1162, Oct 1987.

75. L.A. Akers and J.J Sanchez, 'Threshold Voltage Models of Short, Narrow and small Geometry MOSFETs : A Review .", Solid State Electronics, vol 25 (7), pp 621, 1982.

76. S.M. Sze, "Physics of Semiconductor Devices.", 2nd ed , John Wiley and Sons, pp 447, 1982.

77. J.P. Colinge, 'Sub threshold slope of Thin-Film SOI MOSFETs .", IEEE EDL - 7 *(4),* pp 224, 1986.

78. J.P. Wouters, J.P. Colinge and H.E. Maes, "Subthreshold Slope in Thin Film SOI MOSFETs.", IEEE ED - 37 (9). pp 2022, sept 1990.

79. J. Balestra, M. Benachir, J. Brini and G. Ghibando, "Analytic Models of Subthreshold Swing and Threshold Voltage for Thin- and Ultra-thin Film SOI MOSFETs.", IEEE ED - 37 *(11)*, pp 2303, Nov 1990.

80. J.P. Colinge, "Hot-Electron Effects in Silicon-on-Insulator n-Channel MOSFETs.", IEEE ED - 34 *(10)*, pp 2173, Oct 1987.

81. P.H. Woerlee et al, "Half-Micron CMOS on Ultra-Thin Silicon-on-Insulator," IEDM Tech. Dig, pp 821, Nov 1989.

82. P.M. Woerlee et al, "A Half-micron CMOS Technology using Ultra-Thin Silicon-on-Insulator," IEDM Tech. Dig, pp 583, 1990.

83. J.G.Fossum, Proc. of the Fourth International Symposium on *SOI* Technology and Development, pp 491, The Elec. Chem Soc. , 1990.

84. J.Y. Choi, J.G.Fossum, "SOI Design for Submicron CMOS", IEEE *SOS/SOI* Workshop Proc. pp23, 1989.

85. M. Yoshimi et al., "High Performance SOI MOSFET using Ultrathin SOI film" *IEDM* Tech Dig, pp 640, 1987.

86. G.A. Armstrong and W.D. French, "Optimized Design for a 0.5 µm Gate Length n-channel SOI MOSFET", Electronics Letters, vol 26 (15), pp 1196, July 1990.

87. J.G.Fossum, J.Y.Choi, and R. Sundaram, "SOI Design for Competitive CMOS VLSI", IEEE ED - 37, pp724, Mar 1990.

88. A. Boudou and B.S. Doyle, "Hysteresis I-V Effects in Short-Channel Silicon MOSFETs.", IEEE EDL - 7 *(10)*, pp 570, 1987.

89. H.P. Zappe, R.K.Gupta, I. Sakai and C. Hu, "Operation of CMOS Devioces with a Floating Well.", IEEE ED - 34 *(2)*, pp 335, 1987.

90. J. Tihani and H. Schlotterer, "Properties of MOS Transistors due to the Floating Substrate and the Finite Volume." IEEE ED - 22, pp 1017, 1975.

91. S.S. Eaton and B. Lehovic, "The Effect of Floating Substrate on, the Operation of Silicon-on-Sapphire Transistors.", IEEE ED - 25, pp 907, 1978.

92. S.S. Eaton and B. Lehovic, "Frequency Dependent Propagation Delay in Silicon-on-Sapphire Digital Integrated Circuits.", Solid State Electronics,,vol 21, pp 1253, 1978.

93. C. Ipri, "The Properties of Silicon-on-Sapphire Devices, and Integrated Circuits.", in Silicon Integrated Circuits, D. Kahng, ed., New York : Academic, pp 253, 1981.

94. K. Kato and K. Taniguchi, "Floating Substrate Effects on the Characteristics of SOI MOSFETs.", Extended Abstracts 2nd Int. Workshop Future Electtron Devices, pp 123, 1985.

95. M. H. Gao, J.P. Colinge, S.H. Wu and C. Claeys, "Improvement of Output Impedance in SOI MOSFETs.", *ESSDERC Proc.,* pp 445, 1990.

96. I.M. Hafez, G. Ghibaudo and F. Balestra. "Analysis of the Kink Effect in MOS Transistors.", *IEEE ED* - 37 *(3)*, pp 818, 1990.

97. K. Kato, T. Wada and K. Taniguchi, "Analysis of Kink Characteristics in Silicon-on-Insulator MOSFETs using Two-Carrier Modeling.", *IEEE J. of Solid State Circuits,* SC-20, pp 378, Feb 1985.

98. J.G. Fossum, R. Sundaresan and M. Matloubian, "Anomalous Subthreshold Current-Voltage Characteristics of n-Channel SOI MOSFETs.", *IEEE EDL - 8 (11)* , pp 544, 1987.

99. J.R. Davis, A.E. Glaccum, K. Reeson and P.L.F. Hemment, "Improved Subthreshold Characteristics of n-Channel SOI Transistors.", *IEEE EDL* -7 *(10),* pp 570, 1986.

100. K. Kato and K. Taniguchi, "Numerical Analysis of Switching Characteristics in SOI MOSFETs.", *IEEE ED* - 33, pp 133, Jan 1986.

101. J.P. Colinge, "Reduction of Kink Effect in Thin Film SOI MOSFETs.", *IEEE EDL - 9 (2),* pp 97, Feb 1988.

102. M. Hazamu et al, "Suppression of Drain Current Overshoot in SOI MOSFETs using an Ultra Thin SOI Substrate.", *Electronics Letters,* vol 24 (20), pp 1266, 1988.

103. J.B. Mchitterick, "Sourc -drain Breakdown in Thin SOI Transistors.", *IEEE SOS /SOI Workshop Proc.,* pp 17, 1989.

104. K.K. Young, "Avalanche-Induced Drain Source Breakdown in Silicon-on-Insulator n-MOSFETs.", *IEEE ED* - 35 *(4),* pp 426, April 1988.

105. M. Haond and J.P. Colinge, "Analysis of Drawn Breakdown Voltage in SOI n-Channel MOSFETs.", *Elecnonics Letters,* vol 25 (24), pp 1640, 1989.

106. C.E. Chen, M. Matloubian, R. Sundaresan et al, "Single Transistor Latch in SOI MOSFETs.", *IEEE EDL - 9 (12),* pp 636, Dec 1988.

107. G.A. Armstrong, J.R. Davis and A. Doyle, "Characterization of Bipolar Snapback and Breakdown Voltage in Thin-Film SOI Transistors by Two-Dimensional Simulation.", *IEEE ED* - 38 (12), pp 328, feb 1991.

108. J.Y. Choi and J.G. Fossum, "Analysis and Control of Floating-Body Bipolar Effects in Fully Depleted Submicrometer SOI MOSFETs.", to be published in IEEE Trans on Electron Devices, June 1991.

109. M. Yoshinu et al , "Analysis of the Drain Breakdown Mechanism in Ultra-thin-film SOI MOSFETs.", *IEEE ED* - **37,** pp 2015, Sept **1990.**

110. Y. Yanaguchi et al , Structure Design for submicron MOSFET on Ultra-thin SOI.', *IEDM Tech. dig.,* pp 591, **1990.**

111. H. Lifka and P.H. Woerlee, "Thin Simox SOI Material for Half-Micron CMOS.", *ESSDERC Proc.,* pp 453, **1990.**

112. A. Kamgar et al ,"Ultra-High Speed CMOS Circuits in Thin SIMOX Films.", *ZEDM Tech. dig.,* pp 829, 1989.

113. K. Terrill, J. Woo and D.K. Vasudev, "Design and Performance of Submicron MOSFETs on Ultra-thin SOI for Room Temperature and Cryogenic Operation.", *IEDM Tech. dig.,* pp 294, 1988.

114. T.W. MacElvee et al , "High Performance Fully Depleted Silicon-on-Insulator transistors.", *IEEE ED* - **37,** pp 1444, **june 1990.**

115. D.C. Mayer, "Modes of Operation and Radiation Sensitivity of Ultra-Thin SOI Transistors.", *IEEE ED - 37,* pp **1280,** May **1990.**

116. T. Elewa et al , "Performance and Physical Mechanisms in SIMOX MOS Transistors Operated at Very Low Temperature.", *IEEE WD* - **37,** pp **1007,** April **1990.**

117. L. Hobbs, A. Matheison and W.A. Lane, "Improved Breakdown for SOI MOSFETs fabricated in electron-beam Recrystallized Polysilicon, *IEEE EDL - 9 (8),* pp 385, Aug 1988.

118. K. Izumi, M. Dohen and H. Ariyoshi, "CMOS Devices fabricatecl on Buried SiO_2 Layers Formed by Oxygen Implantation into Silicon.", *Electronics Lett.,* vol 14, pp 593, 1978.

119. S. Seki, O. Kogure and B. Tsujiyama, "Laser-Recrystallized Polycrystalline-Silicon Thin-Film Transistors with Low Leakage and High Switching Ratio.", *IEEE EDL - 8 (9),* pp 425, **1987.**

120, K. Barla et al , "Characteristics of SOI CMOS Circuits made in $N/N^+/n$ oxidized Porous Silicon Structures.", *Electronics Lett.,* **vol 22,** pp 1291, 1986.

121. G.A. Armstrong, W.D. French and J.R. Davis, "Design Considerations for 0.5 micron Ultra-thin-film Submicron SOI Transistors by Two-dimensional Simulation.", *ESSDERC Proc.,* pp 425, **1990.**

122. A. Ortiz-Conde and J.G. Fossum, "Subthreshold Behaviour of Thin-Film LPCVD Polysilicon MOSFETs.", *IEEE ED - 33,* pp 1563, Oct 1986.

123. A. Ortiz-Conde et al , "The Foundation of a Charge-Sheet Model for the Thin-film MOSFET.", *Solid State Electron,* vol **31,** pp 1497, 1988.

124. A. Ortiz-Conde et al . "The Non-Equilibrium Inversion layer Charge of the Thin-Film SOI MOSFET." *IEEE ED* - **36,** pp 1651, Sept 1989.

135. C. Mallikarjun and K.N. Bhat, "Numerical and Charge Sheet Models for Thin-Film SOI MOSFETs.", *IEEE ED* - **37,** pp **2039,** Sept 1990.

126. Pierret . R.F. - unpublished.

127. J.C.S. Woo, K.W. Terrill and P.K. Vasudev, "Two-Dimensional Analytic Modeling of Very Thin SOI MOSFETs.", *IEEE* ED - **37,** Sept **1990.**

128. E. Sano, R. Kasai et al , "A Two-Dimensional Analysis for MOSFETs Fabricated on Buried SiO_2 Layer.", *IEEE ED - 27,*.**pp 2043,** Nov **1980.**

129. D. Handre and F. Van de Wiele, "Second-Order Analytical Modeling of Thin-Film SOI MOSFETs.", *IEEE SOS / SOl Workshop Proc.,* pp **27, 1989.**

130. M. Yoshimi et al , "Two-Dimensional Simulation and Measurement of High Performance MOSFETs made on a Very Thin SOI Film.", *IEEE ED* **- 36,** pp **493, 1989.**

131. K. Throngnumchai, K. Asada and T. Sugano, "Modeling of **0.1 µm** MOSFETs on SOI Structure Using Monte Carlo Simulation Technique.", *IEEE ED* **-33,** pp **1005,** July **1986.**

132. W.P. Maszara, "Strain Compensated Epitaxial Etchstop for BESOI", *IEEE SOI Conference* , pp. **6,** 1992.

133. H. Goutou, A. Sekiyama, T. Seki, S. Nagai, N. Suzuki, M. Hayasaka, Y. Matsukawa, M. Miyazima, Y. Kobayashi, S. Enomoto and K. Imaoka, *Tech. Dig. IEDM,* pp. **912, 1989.**

134. M. Haond and O. L. Niel. *Proceedings IEEE SOSISOI Tech. Conference,* pp. 132, **1990.**

135. R.B. Marcus and T.T. Sheng, **J.** *ElectroChem Soc.*, vol. **129,** pp. **1278, 1982.**

136. M. Matloubian, **R.** Sundaresan and H. Lu, *Proceedings IEEE SOS/SOI Tech. Conference,* pp. **80, 1988.**

137. J.P. Colinge, *Proceedings IEEE SOS/SOl TEch. Conference,* pp. **13, 1989.**

138. T. Nishimura, Y. Yamaguchi, A. Miyatake and Y. Akasaka, *Proceedings IEEE SOS/SOI TEch. Conference,* pp. **132, 1989.**

139. J.G. Fossum, S. Krishnan and P.C. Yeh. "Performance limitations of deep-submicron fully depelted SOI MOSFETs", *IEEE Intl. SOS/SOI Conference,* pp. **132, 1992.**

140. K.M. Chain, S.Y. Oh, D. Chin and J. L. Moll , "Computer-aided design and VLSI device development", *Hingman, MA,* Kluwer Academic Publishers, pp. 240, 1986.

141. P.K. Ko, S. Tam, C. Hu, S.S. Wong and C. G. Sodini, *IEDM Tech. Dig.,* pp. 88, **1984.**

142. J. Fossum, P.C. Yeh and J. Choi, "Floating-body problems and benefits in fully-depleted SOI CMOS VLSI circuits", *IEDM Tech. Dig.*, pp. 325, 1991.

CHAPTER 3

THIN-FILM DUAL-GATED SOI MOSFETS

3.1 Introduction

A number of advantages of thin-film SOI MOSFETs have been discussed in Chapter 2. Historically, research into SOI devices was carried out with a single application in mind, namely, radiation-hard devices for space applications. Of late, the potential applications of SOI devices have extended to the field of power devices due to the blocking voltage capabilities of the back oxide which results in reduced surface electric fields (RESURF) [1-4]. Perhaps of greater importance is the extension of SOI devices into the realm of high-speed digital circuits - until now the sole property of bulk CMOS VLSI [5-10]. As generations of computer technology evolve there is a concomitant increase in speed. Clock speeds in particular (though they do not solely dictate the speed of microprocessors) have jumped from 20-MHz in 1988 to 50-MHz today and designs involving higher clock speeds are already in progress. Every increase in speed also involves a decrease in the minimum feature size of devices. In CMOS technology this means shrinking gate lengths. The deleterious effects of aggressive scaling were discussed in detail in Chapter 2. Silicon-on-insulator devices allow the extension of current technology to a future generation. This is largely due to the minimized parasitic capacitance in a SOI structure. Thus, largely due to the reduction of load capacitance in a CMOS circuit, SOI devices allow the technology to operate at the same gate length while providing speeds compatible with a future generation. Again, research into SOI devices with reach-through junctions was prompted by this potential increase in speed due to minimized parasitics. All other advantages of SOI MOSFETs described in Chapter 2 must be considered to be serendipitous windfalls.

A significant advantage of SOI MOSFETs stems from the fact that the device performances can be altered by the action of a 'back gate'. Conventionally, the silicon

substrate acts as the back gate as illustrated in Fig. 2.1. The bias applied to the substrate modifies the surface potential in the channel at the back interface (back interface 1 in Fig. 2.1). In a fully-depleted device the front interface and the back interface are electrostatically coupled together. When the back surface is accumulated then the device: can no longer be considered fully-depleted as the accumulation layer at the back cannot be depleted by the front gate. In chapter 2 it was noted that the back surface potential can affect the device performance of the MOSFET operated using the top surface gate. This back gate control lends designers the option of maintaining the back interface in either accumulation or depletion and can be used to optimize device design by controlling either short-channel effects or hot-electron effects [11]. Long-channel fully-depleted SOI MOSFETs show significantly enhanced saturation drain currents and transconductances over bulk MOSFETs. They also exhibit superior sub-threshold slopes. However it was noted in the previous chapter that at short channel lengths the advantages of SOI MOSFETs in terms of current, transconductance and sub-threshold slopes were lost. The degradation in current is limited by fundamental device physics and velocity saturation. But the degradation in sub-threshold slopes, short channel effects and DIBL can be controlled by the back-gate. This leads to the concept of the Dual-Gated MOSFET.

In this chapter, we shall discuss some of the advantages of dual-gated MOSFETs. In a dual-gated MOSFET, the top and bottom gates are biased simultaneously. The device is then essentially a dual-channel device with surface inversion channels induced at the front and back interfaces. The various reported configurations of dual-gated devices are illustrated in figure 3.1. In section 3.2, the concept of volume inversion in dual-gated devices is discussed and common misconceptions are clarified. Some of the advantages of dual-gated MOSFETs are then analyzed in section 3.3. All the results shown in this chapter are based on either numerical simulations or analytical computations. The goal is to identify definite trends by making fair comparisons between the different devices. It is not the aim of this chapter to predict the exact device parameters such a current density etc. for different processes, or to optimize process parameters to achieve a desired performance level. Finally in section 3.4, we outline a novel process to fabricate a fully self-aligned dual-gated SOI MOSFET using the vertically seeded epitaxial lateral overgrowth technique. The device has significant advantages over existing dual-gated SOI MOSFET technologies. The self-alignement between the top and bottom gates minimizes parasitics and reduces active area.

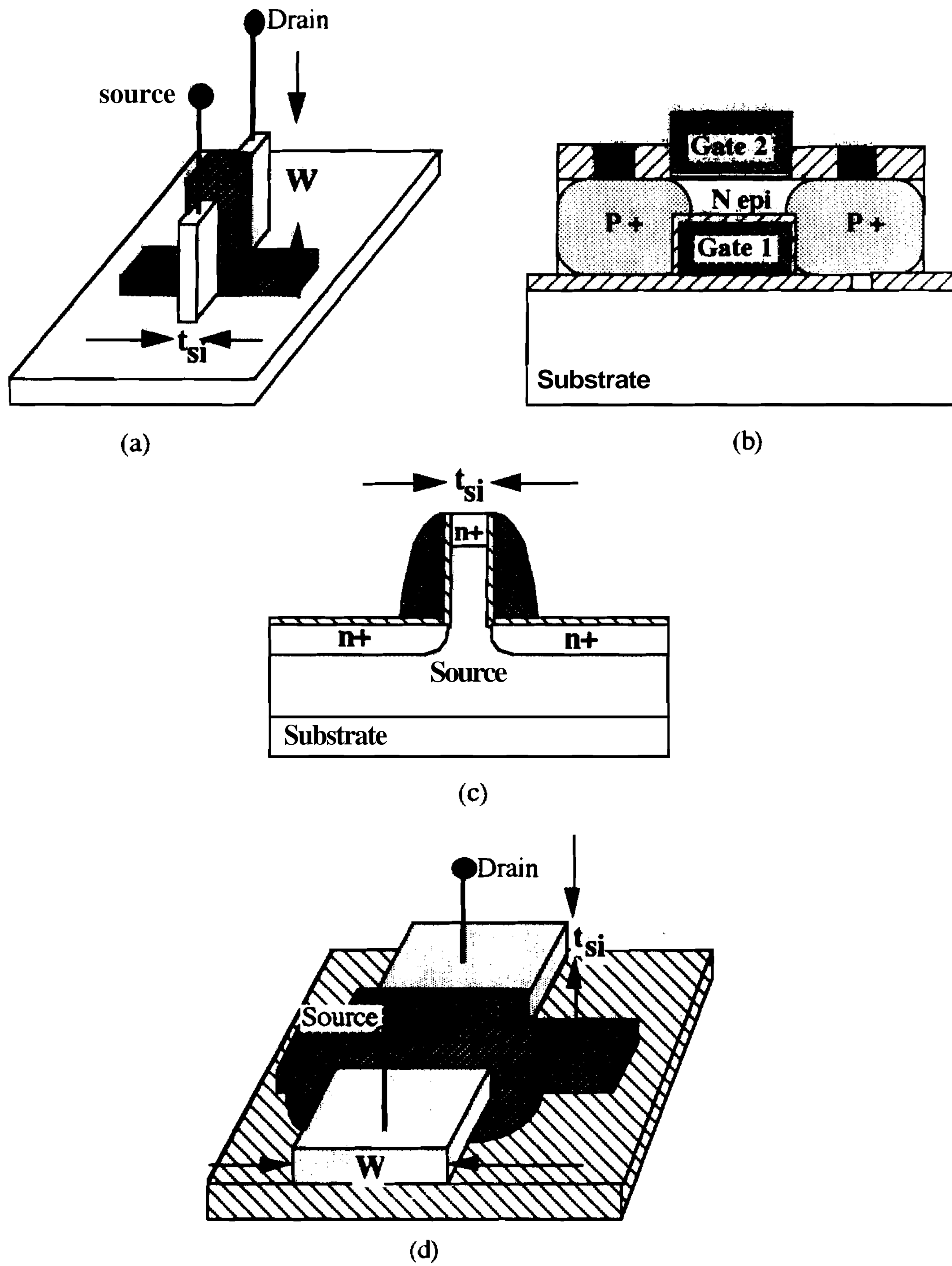

Figure 3.1 Various configurations of dual gated devices reported in the literature

3.2 Volume Inversion

A novel mode of operation of dual-gated SOI MOSFETs was proposed by Balestra et al [12], in which the top and bottom gates were biased simultaneously. A significant enhancement in device performance was predicted for this mode of operation, due to volume inversion in the channel caused by the action of the two gates. A device in volume inversion contains an electron density that is greater than the channel doping throughout the thickness of the semiconducting film. The performance enhancement of such a device was theorized to arise from the reduced influence of surface scattering on the "bulk" carriers in the film. Recently Zingg et al [13] and Colinge et al [14] demonstrated improved characteristics in dual-channel SOI MOSFETs. The performance enhancements in the above cases were shown by comparing the output characteristics of a dual-channel MOSFET to the more conventional single-channel MOSFET of Fig 2.1. However, the measured drain current was the cumulative sum of that due to volume inversion and the inherent additional current resulting from the lowered threshold voltage of the dud-channel MOSFET. Any enhancements due to just volume inversion effects were not clearly identified. Drain current enhancements resulting from solely bulk inversion must be determined by comparing dual-channel and single-channel MOSFETs at constant V_G-V_T values. In the fallowing section, we investigate the effects of volume inversion in thin-film SOI MOSFETs and the efficacy of dual-gate operation in enhancing their device performance.

3.2.1 Numerical Simulations

In order to determine the performance enhancements in dual-channel SOI devices. over 100 different two dimensional device simulations were performed using the PISCES-IIB device simulator [15]. The device structures used in the simulations are illustrated as insets in Fig 3.3 (a). In addition to field and doping dependent carrier mobilities, the effect of the perpendicular electric field on carrier mobility was incorporated to account for surface mobility degradation associated with increased carrier scattering. The inclusion of the perpendicular electric field model is crucial to simulating thin-film SOI devices where there could be substantial sub-surface currents. For the sample simulations described herein, interfacial traps were neglected at the two gate oxide-semiconductor interfaces white fixed interface charges of $10^{10}/cm^2$ and $10^{11}/cm^2$ were specified at the front and

back interfaces respectively.[1] The gate material was chosen to be degenerately doped n^+-polysilicon. All devices had a gate length of $1\mu m$ and a gate oxide thickness of 200Å commensurate with typical $1\mu m$ design rules [16]. The single-gated device had a buried oxide thickness of 300nm and for both devices the channel doping was uniform at $7x10^{16}/cm^3$ with a silicon film thickness of $0.1\mu m$. For the assumed film thickness, this was the largest value of the film doping concentration that yielded a fully-depleted device at threshold.

The output drain characteristics of the SG and DG MOSFETs were simulated for a constant (V_G-V_T) to exclude extraneous enhancements related to the lower threshold voltage of the DG MOSFET. The threshold voltage was determined by linearly extrapolating the linear region of the I_D-V_G curve to zero drain current. The threshold voltage of the SG MOSFET is 0.4V and that of the DG MOSFET is 0.13V. The output characteristics of the SG and DG MOSFETs are shown in figure 3.2. The drain current characteristics of the DG MOSFET were seen to be consistently greater than that of the SG MOSFET. Figure 3.3 (a) illustrates the output characteristics of the two devices under strong inversion conditions at V_G-V_T=2.6V and figure 3.3 (b) depicts the transconductance of the DG and SG MOSFET. As illustrated in Fig. 3.3 (a), the saturation drain current of the DG MOSFET was observed to be about twice that of the SG MOSFET. This factor of two increase is expected due to the existence of two surface channels inside. the DG MOSFET. A non-trivial performance enhancement must be measured by the increment over this base 'factor of 2' increase. Unfortunately, only a 5-10% incremental increase was observed in the drain current. Similarly, the transconductance of the DG MOSFET shows about a 10% increase over twice the value of the SG MOSFET only in the weak inversion region around the threshold voltage. Once the device reaches strong inversion , the enhancement in the transconductance decreases.

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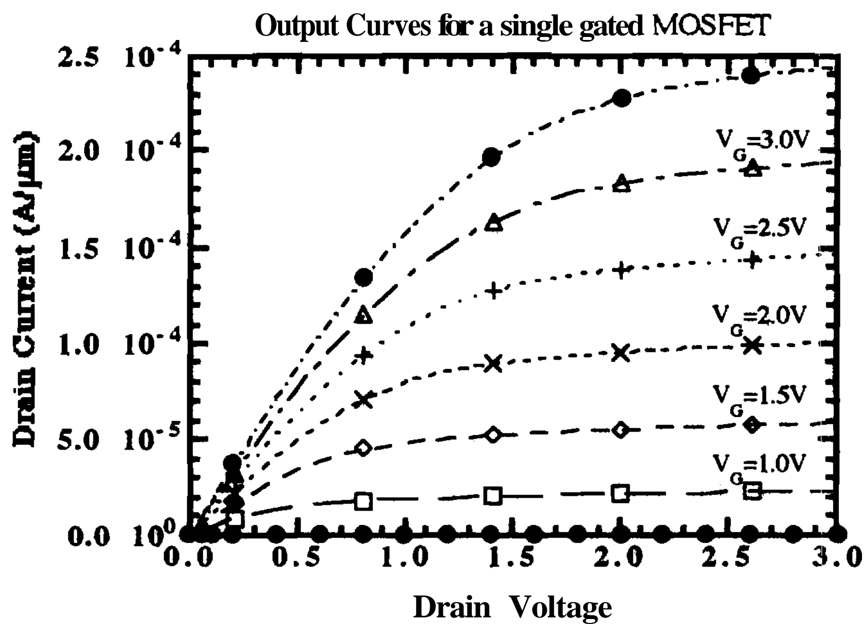
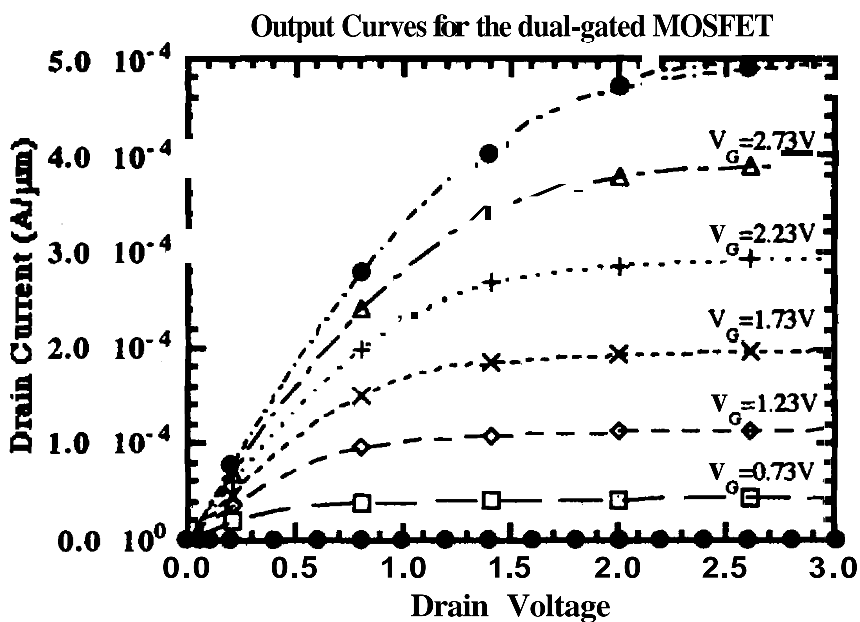
[1]Although a symmetric device structure was used in the simulations, the different values of the fixed charge assumed at the front and the back interfaces resulted in a small asymmetry in the computed carrier distributions. Similar results were obtained when the fixed charge density at the two interfaces were neglected in the simulations.

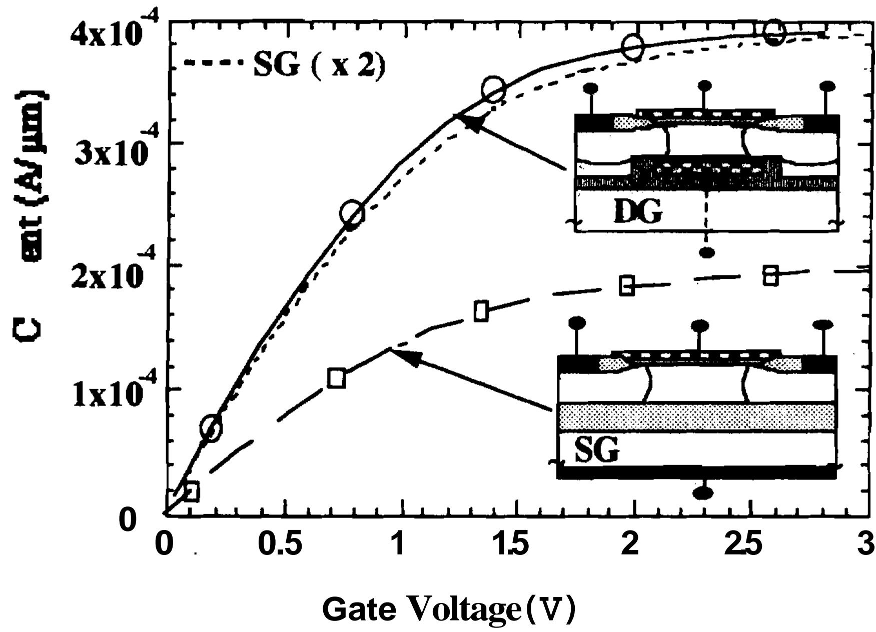


(a)

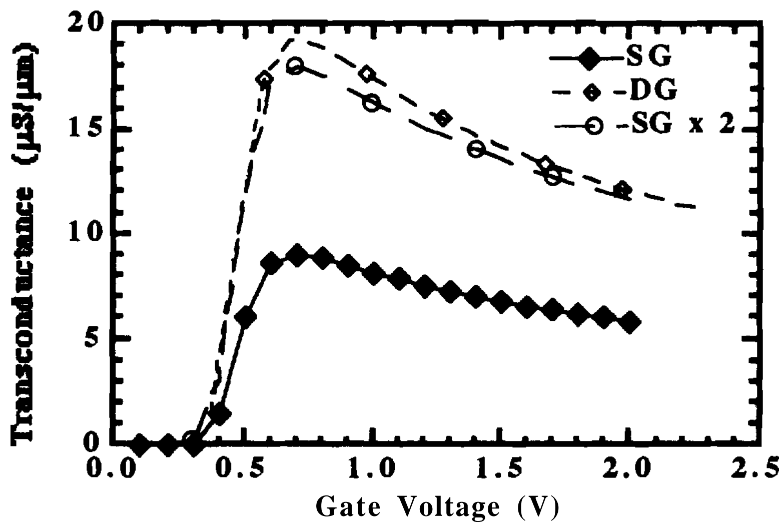


(b)

Figure 3.2 Output characteristics for (a) a single gated (SG) MOSFET and (b) a dual-gate (DG) MOSFET



(a)



(b)

Figure 3.3 (a) Output drain characteristics of the SG and DG **MOSFETs** at V_G-V_T=2.6V. The simulated **MOSFET** structures are shown as insets in the figure (b) **transconductance** variation for DG and SG **MOSFETs** at V_D=0.1V

As noted in reference [14], the inversion layer is more or less evenly distributed across the silicon film at threshold. For surface potential increments beyond threshold, the inversion electrons are added to the surface while the bulk inversion density does nut increase significantly. The surface inversion layer effectively shields the bulk inversion charges under large gate biases, causing them to be more or less pinned to their values at the onset of inversion. Consequently, only a very small increase in current was observed due to the larger mobilities of the bulk electrons. The integrated carrier concentration-mobility (μ-n integral) at the source of the DG MOSFET is plotted in Fig. 3.4. The region of slowly varying μ-n across the bulk of the SOI film is indicative of the relatively negligible contribution of the bulk inversion electrons to the μ-n integral and hence to the drain current. A sharp slope in this region would be indicative of a significant current contribution in the bulk. At a constant V_G-V_T the total-film μ-n integral in the DG MOSFET is almost exactly twice that in the SG-MOSFET, consistent with the two-times current difference. Thus, unless the surface mobility is significantly lower than the mobility in the bulk or the bulk carrier concentration is comparable to the concentration at the surface, volume inversion is not expected to cause a significant enhancement in the output drain current

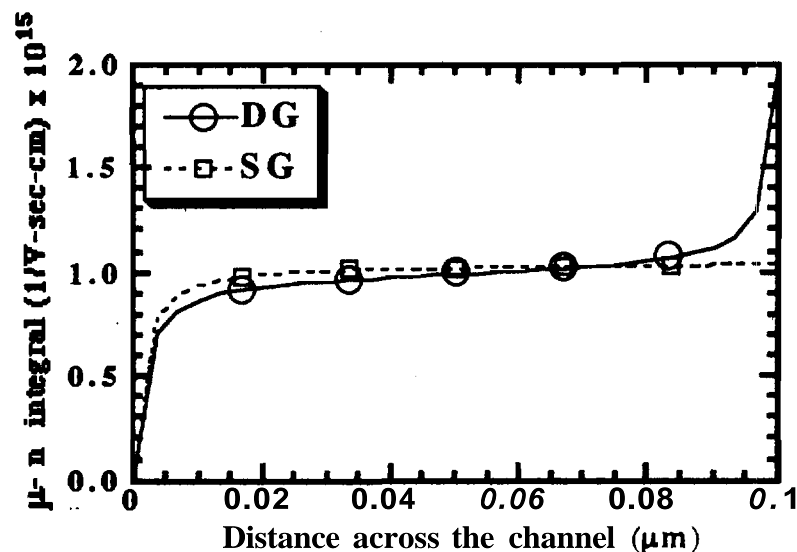


Figure 3.4 Integrated mobility-electron density product (∫μn dx) as a function of position in the SOI film

3.2.2 Analytical Formulation

In addition to the PISCES simulations, one dimensional equilibrium electrostatic computations were carried out by solving Poisson's equation as applied to a fully depleted SOI film. Poisson's equation is written as,

$$\frac{dE}{dx} = \frac{\rho}{K_s\varepsilon_o} = q(p - n + N_D - N_A) \qquad (1)$$

In a bulk MOSFET, the field and the charge density are zero, deep in the silicon film. It is therefore convenient to use this as the reference point. However in a dual-gated MOSFET there is no region of the semiconductor with zero charge density. The qualitative potential distribution under dual-gate operation in a n-channel MOSFET is shown in figure 3.5.

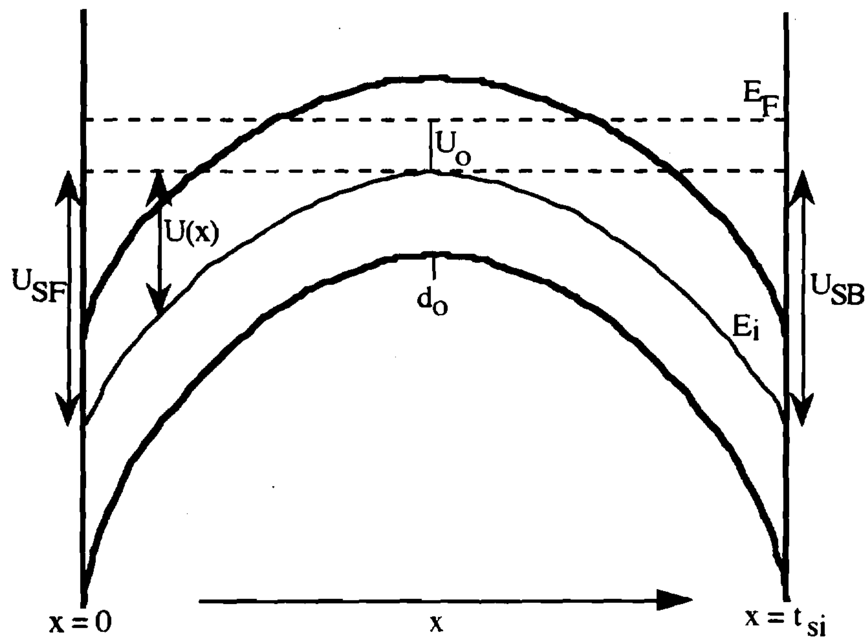


Figure 3.5 Energy band diagram for a symmetric dual-gated MOSFET with both surfaces under inversion

In this mode of operation the surface potentials at the front and back interfaces, ϕ_{SF} and ϕ_{SB} respectively, are both greater than zero. Moreover, there always exists a point (d_o in the figure) at which the electric field is zero. This point is chosen as the reference for the potential.

Introducing the normalized potentials,

$$U(x) = \frac{\phi(x)}{kT/q} = \frac{E_i(d_o) - E_i(x)}{kT}$$

$$U_{SF} = \frac{\phi_{SF}}{kT/q} = \frac{E_i(d_o) - E_i(0)}{kT} \quad (2)$$

$$U_{SB} = \frac{\phi_{SB}}{kT/q} = \frac{E_i(d_o) - E_i(t_{si})}{kT}$$

and by definition, $$N_D - N_A = n_i[e^{-U_F} - e^{U_F}] \quad (3)$$

where U_F is the fermi potential. To **account** for the full-depletion of the film, we also define U_o such that,

$$U_o = \frac{E_i(d_o) - E_F}{kT} \quad (4)$$

where E_F **denotes** the position of the fermi level. $U_o = U_F$ only in the $t_{si} \rightarrow \infty$ limit. Then by virtue of the choice of the reference point, $U(d_o) = 0$.

$$p = n_i\, e^{[E_i(x) - E_F]/kT} = n_i\, e^{[E_i(x) - E_i(d_o) + E_i(d_o) - E_F]/kT}$$

$$\therefore \qquad p = n_i\, e^{[U_o - U(x)]} \quad (5)$$

In similar fashion $$n = n_i\, e^{[U(x) - U_o]} \quad (6)$$

Poisson's equation can then be written as,

$$\frac{dE}{dx} = \frac{qn_i}{K_s\varepsilon_o}\left[e^{U_o - U(x)} - e^{U(x) - U_o} + e^{-U_F} - e^{U_F}\right] \quad (7)$$

Therefore,

$$\frac{d^2U}{dx^2}=\left(\frac{q^2n_i}{K_s\varepsilon_o kT}\right)\left(e^{U-U_o}-e^{U_o-U}+e^{U_F}-e^{-U_F}\right) \quad (8)$$

$$\frac{d^2U}{dx^2}=\frac{1}{2L_D^2}\left(e^{U-U_o}-e^{U_o-U}+e^{U_F}-e^{-U_F}\right)$$

$$\text{where } L_D=\sqrt{\frac{q^2n_i}{K_s\varepsilon_o kT}}=\text{the intrinsic Debye length} \quad (9)$$

Integrating eqn. (9) in the standard manner,

$$\int_0^{dU/dx}\frac{dU}{dx}d\left(\frac{dU}{dx}\right)=\frac{1}{2L_D^2}\int_0^U\left(e^{U-U_o}-e^{U_o-U}+e^{U_F}-e^{-U_F}\right)dU \quad (10)$$

Since at $x = d_o$, $E = -dU/dx = 0$ and $U(x) = 0$,

$$\frac{dU}{dx}=\frac{1}{L_D}\left[e^{U_o}(e^{-U}-1)+e^{U_F}U+e^{-U_o}(e^{U}-1)-e^{-U_F}U\right]^{1/2} \quad (11)$$

$$E(x)=-\frac{kT}{q}\frac{dU}{dx}=\hat{U}_{SF}\frac{kT}{q}\frac{F(U,U_o,U_F)}{L_D} \quad \text{for } 0<x<d_o$$

$$=-\frac{kT}{q}\frac{dU}{dx}=-\hat{U}_{SB}\frac{kT}{4}\frac{F(U,U_o,U_F)}{L_D} \quad \text{for } d_o<x<t_{si} \quad (12)$$

$$\text{where } F(U,U_o,U_F)=\left[e^{U_o}(e^{-U}-1)+e^{U_F}U+e^{-U_o}(e^{U}-1)-e^{-U_F}U\right]^{1/2}$$

Now,

$$\frac{dU}{dx}=-\hat{U}_{SF}\frac{F(U,U_o,U_F)}{L_D} \quad 0<x<d_o$$

$$=\hat{U}_{SB}\frac{F(U,U_o,U_F)}{L_D} \quad d_o<x<t_{si} \quad (13)$$

Separating variables in the above equation and integrating from $x=0$ to $x=d_o$ and $x=d_o$ to $x=t_{si}$ respectively,

$$\int_{U_{SF}}^{0} \frac{dU}{F(U,U_o,U_F)} = -\hat{U}_{SF} \int_{0}^{d_o} \frac{dx}{L_D} \qquad 0<x<d_o$$

$$\int_{0}^{U_{SB}} \frac{dU}{F(U,U_o,U_F)} = \hat{U}_{SB} \int_{d_o}^{t_{si}} \frac{dx}{L_D} \qquad d_o<x<tsi \tag{14}$$

Therefore, by combining the equations (14) we get,

$$\left[\int_{0}^{U_{SF}} \frac{dU}{F(U,U_o,U_F)} + \int_{0}^{U_{SB}} \frac{dU}{F(U,U_o,U_F)}\right] = \hat{U}_S \frac{t_{si}}{L_D} \tag{15}$$

since $\hat{U}_{SF} = \hat{U}_{SB} = \hat{U}_S$ under dual-gate operation. Given the surface potentials U_{SF} and U_{SB}, equation (15) determines the parameter U_o. Once U_o is determined, the potential profile and the electron and hole distributions can be easily obtained using,

$$\int_{U}^{U_{SF}} \frac{dU'}{F(U',U_o,U_F)} = \hat{U}_S \frac{x}{L_D} \qquad 0\le x\le d_o$$

$$\text{and} \quad \int_{U}^{U_{SB}} \frac{dU'}{F(U',U_o,U_F)} = \hat{U}_S \frac{t_{si}-x}{L_D} \qquad d_o\le x\le t_{si} \tag{16}$$

From Gauss' Law, the terminal relationships can then be written as,

$$V_{GF} = \frac{kT}{q}(U_{SF}+U_F-U_o) + \frac{K_s\varepsilon_o}{K_{ox}}E_{SF} + \Phi_{MS}$$

$$V_{GB} = \frac{kT}{q}(U_{SB}+U_F-U_o) - \frac{K_s\varepsilon_o}{K_{ox}}E_{SB} + \Phi_{MS} \tag{17}$$

Under symmetric conditions, $d_0 = t_{si}/2$ and the above equations simplify immensely.

Using the above analytical formulation it was found that, for .a given SOI film thickness, the inversion charge density inside the film became independent of doping when the doping concentration was reduced below a certain critical value. Moreover, the cited limiting case corresponded to the maximum volume inversion. Based on the foregoing observations, the maximum bulk inversion charge density for a given silicon film thickness was obtained by simply dropping the bulk terms in the Poisson formulation. Fig. 3.6 shows the limiting-case electron distribution in the SOI film of a symmetrical dual-channel

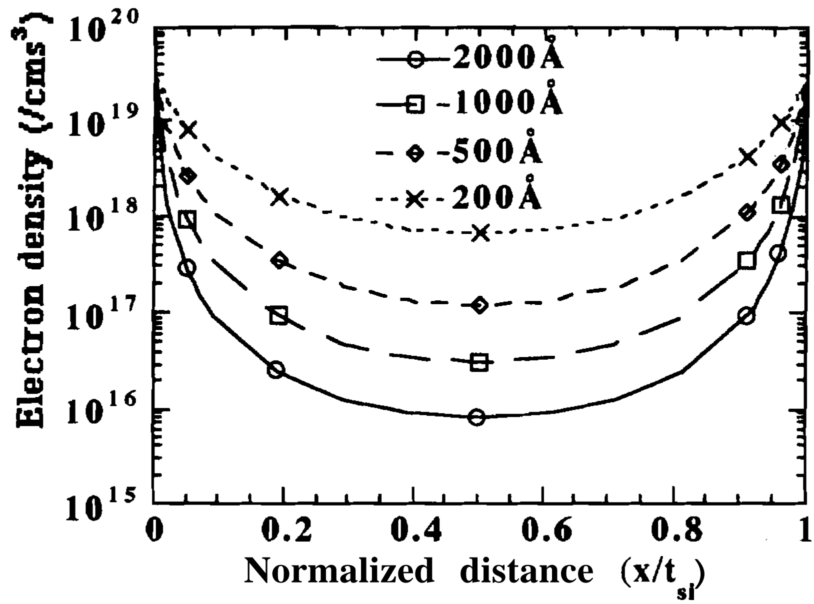


Figure 3.6 Limited-case plot of the electron density distribution in the channel for different SOI film thicknesses

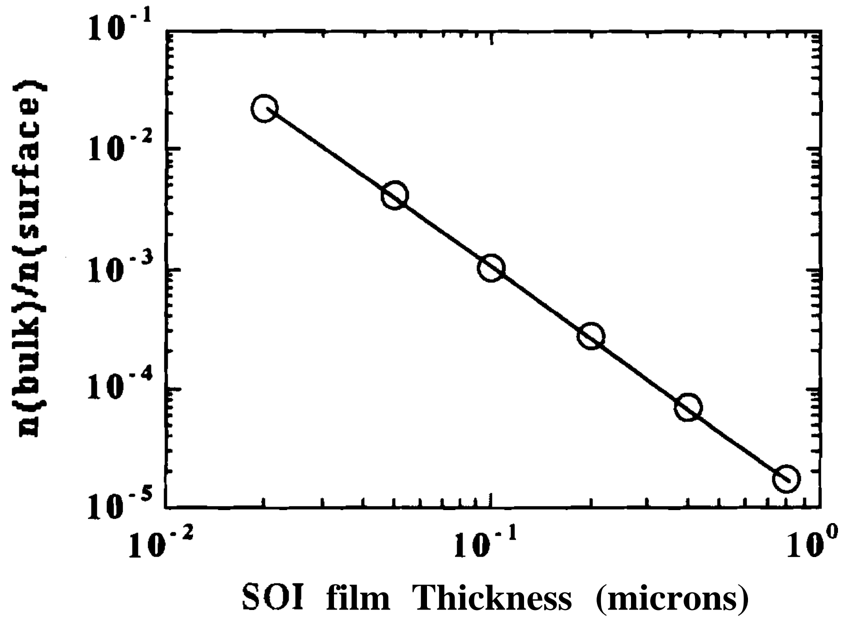


Figure 3.7 Maximum ratio of the electron density in the middle of the channel (bulk) to that at surface. The surface potential in all cases is the same

MOSFET for a select number of film thicknesses. The surface electron concentration is fixed at the band-edge value in all cases; i.e E_C is assumed equal to E_F at the semiconductor surface. The ratio of the electron concentration in the bulk to the electron concentration at the surface is plotted as a function of film thickness in figure 3.7.

Examining Figs. 3.6 and 3.7 note that, for a film thickness of 1000Å, the bulk electron concentration is roughly three orders of magnitude lower than the surface electron concentration. Since the surface mobility is the same order of magnitude as the bulk mobility, the bulk electrons are expected to make a negligible contribution to the μ-n integral. Effectively, the drain current flows almost exclusively in the: surface channels which extend about 100Å into the film on either side. For the effects of volume inversion to be significant, the carrier concentration profile in the semiconducting film must be more or less uniform. With reference to Fig. 3.7, this would require very thin films ($\leq$ 200Å) which are extremely difficult to fabricate.[17].

Contrary to previous assertions, it was concluded that the dual-channel SOI MOSFET would provide only a small incremental (> 2X) current enhancement over the single-channel SOI MOSFET when compared at equal V_G-V_T values. This conclusion in itself does not detract from the potential use of dual-gated SOI MOSFETs in CMOS VLSI circuits. The presence of an independently controllable second gate gives circuit designers a good measure of flexibility in circuit design. Whereas, the use of a single gated MOSFET constrains all devices to operate at the same threshold voltage, the use of a dual-gated transistor allows the devices to operate at different threshold voltages.

3.2.3 Quantum Mechanical Analysis

The analytical results in the previous section were applied to films that were 200 Å thick. At these dimensions there might be concern as to whether quantuim-effects become important or not. To make sure quantum-effects did not change carrier distributions significantly, 1-D Quantum-mechanical computations were performed for both the 1000Å and the 200Å films. The conduction band profile was provided from the analytical solution and hardwall boundary conditions were applied at the two ends to account for the confinement by the oxide interfaces. The computations did not incorporate a self-consistent Poisson solver, but provided fairly accurate first order results [18,19]. The forthcoming

sketch of the quantum-mechanical computations do not fall into the author's expertise and he acknowledges the help and support of R. Lake who ran these simulations.

The bare and essential outlines of the computations are sketched below. The details are provided in references [18,19]. Since the problem essentially involves an equilibrium solution, the computations start with the finite difference solution of the equilibrium Green's function definition of Schrodinger's equation,

$$\left(E + \frac{\hbar^2}{2m^*}\nabla^2 - V(\bar{r}) + i\frac{\hbar}{2\tau}\right) G(\bar{r},\bar{r}') = \delta(\bar{r}-\bar{r}') \qquad (18)$$

$V(\bar{r})$ includes the electrostatic potential and any conduction band discontinuities.
τ for this problem was chosen to be 0.5 ps.
$\hbar/2\tau$ represents the random potential due to the impurities and phonons.
m^* was chosen to be the density of states effective mass given by 1.182 m_o. However, for calculating energy levels and wave-functions, the conductivity effective mass should be used since this is the dynamic part of the solution. Then once the energy levels and wave-functions are computed, the electron density should be calculated using the density of states effective mass. Unfortunately, the program was only set up to use a single effective mass m^*.

To determine the electron density, the following basic equations were used,

$$D(\bar{r},E) = \sum_m |\Psi_m(\bar{r})|^2 \delta(E-E_m) \qquad (19)$$

This defines the local position dependent density of states. The usual definition of the density of states is then given by the integral,

$$D(E) = \int d\bar{r}\, D(\bar{r},E) = \sum_m \delta(E-E_m) = \int dE'\, D(E')\,\delta(E-E') \qquad (20)$$

Let $H_o = \frac{\bar{p}^2}{2m^*} + V(\bar{r})$. Expanding $G(\bar{r},\bar{r}')$ in eigenstates of H_o,

$$G(\bar{r},\bar{r}',E) = \sum_m \frac{\phi_m^*(\bar{r})\phi_m(\bar{r}')}{E-\varepsilon_m+i\frac{\hbar}{2\tau}} \qquad (21)$$

The density of states is then defined as.

$$D(\bar{r},E) = -\frac{1}{\pi}\,\mathrm{Im}[G(\bar{r},\bar{r}',E)]$$

$$= \frac{1}{\pi}\sum_{m}\frac{|\phi_m(\bar{r})|^2\,\hbar/2\tau}{(E-\varepsilon_m)^2+(\hbar/2\tau)^2} \qquad (22)$$

The quantity $\frac{1}{\pi}\frac{\hbar/2\tau}{(E-\varepsilon_m)^2+(\hbar/2\tau)^2}$ is a Lorentzian of full width at half maximum equal to . In the limit $\hbar/\tau \rightarrow 0$, the Lorentzian $\rightarrow \delta(E-\varepsilon_m)$. In this limit eqn. (22) reduces to eqn. (19). The finite value of $\hbar/\tau$ gives a finite width to the energy states of the system. The program calculates $G(\bar{r},\bar{r}',E)$ from eqn. (18), $D(\bar{r},E)$ from eqn. (22), then weights $D(\bar{r},E)$ by $f(E)$ and integrates over E to get $n(\bar{r})$.

The results of the computation are shown in figure 3.8. The quantum-mechanical simulations were carried out for both the 1000Å and the 20081 films. In the 1000Å film the 1-D density of states $N_0(z;E)$ follows the conduction band profile. All the available states are determined by the triangle potential wells at either surface and no bound states due to the 'particle in a box' type confining potential is found. This is made more clear in figure 3.9 where the shadow plots of the calculated strictly 1D density of slates ($N_0(z;E)$ are plotted, with the conduction band profile superposed. The dark regions are regions of high density of states. The contribution to the density of states from the transverse energies have been ignored in the plot due to clarity. In the 20081 case, a significant contribution is seen to arise from the 'particle in a box' confinement as evidenced by the non-zero DOS distributions along the middle of the channel. However, the significant energy levels are still determined by the states fixed at the two surfaces by the triangular potential. Once again the shadow plot of figure 3.9 (b) confirm that the dominant energy states occur at the two surfaces. This proves that while there is a quantum effect in the thin 20081 films, the electron density distribution is not affected by them. Finally, figure 3.10 that compares the electron density distributions between the quantum mechanical picture and the analytical picture prove the accuracy of the analytic computations.

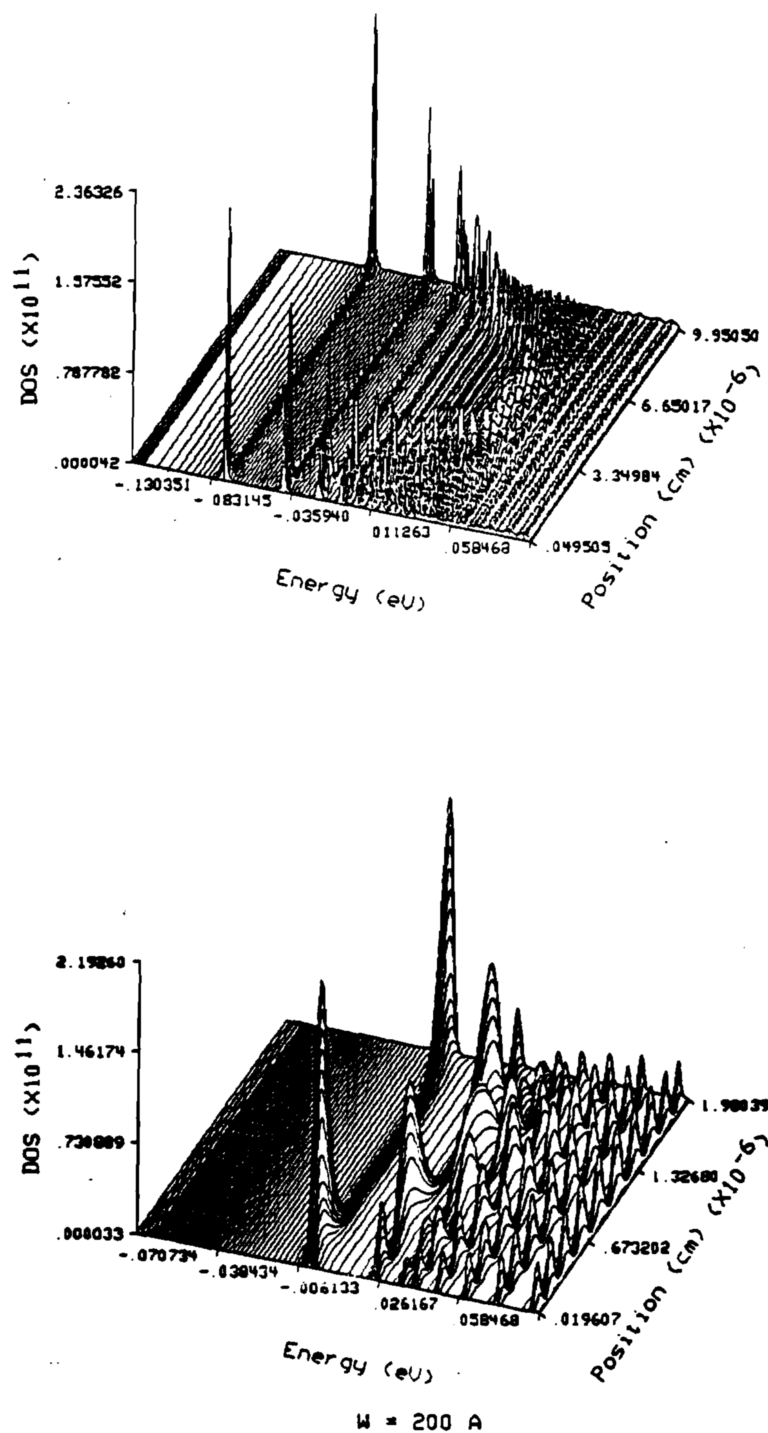
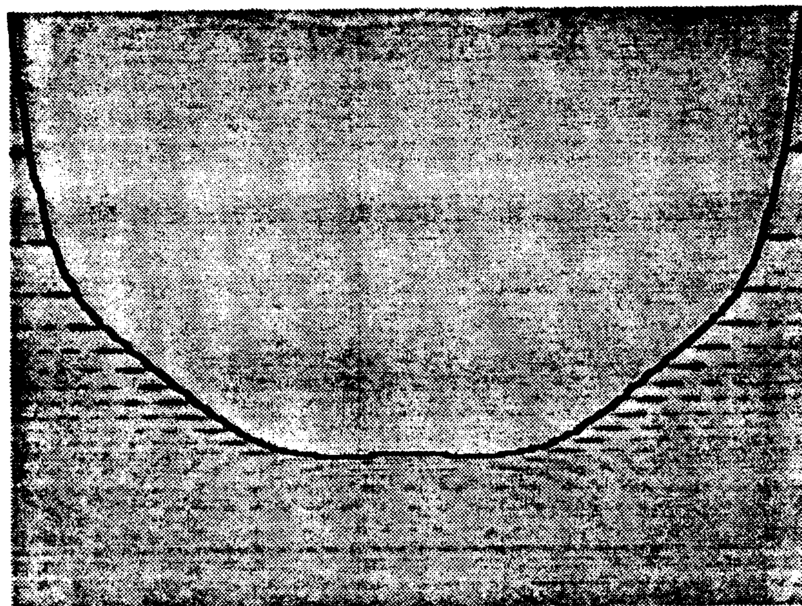


Figure 3.8 Three-dimensional plots of the strictly 1-D $N_0(z;E)$ computed using the quantum-mechanical approach for (a) a 1000Å film and (b) a 200Å film



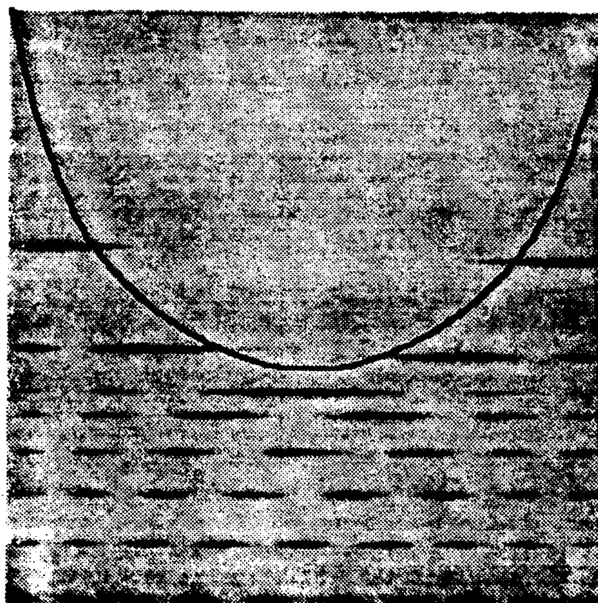


Figure 3.9 Shadow plots of the calculated, strictly 1D density of states $N_o(z;E)$ with the conduction band superposed for (a) a 1000Å film and (b) a 2008, film. Dark regions are regions of high density of states

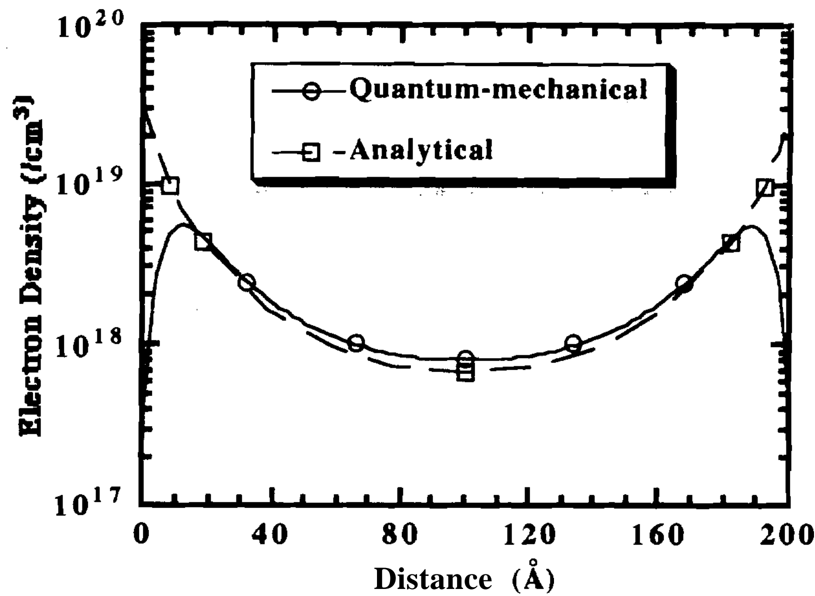
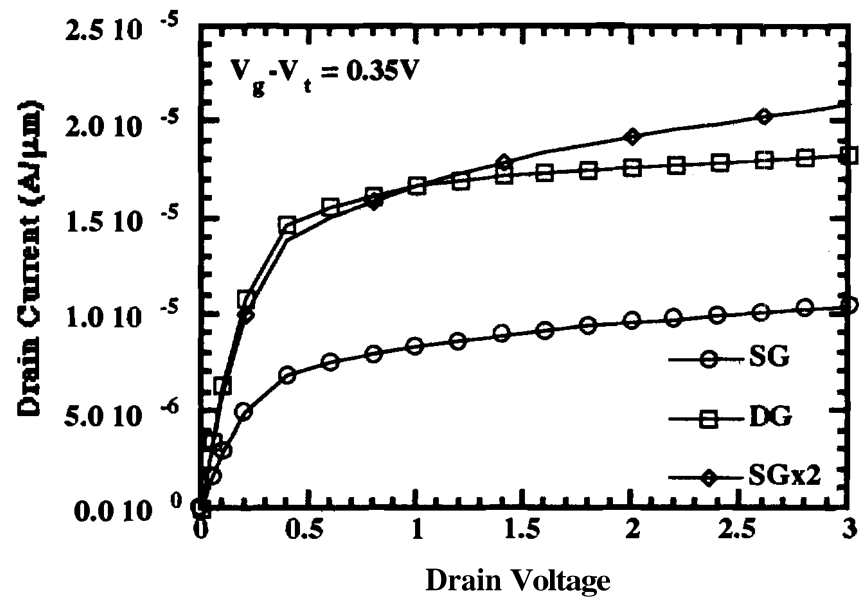


Figure 3.10 Comparison of the electron density distnbutions obtained from the analytical formulation and from the quantum formulation for a 200Å thick film

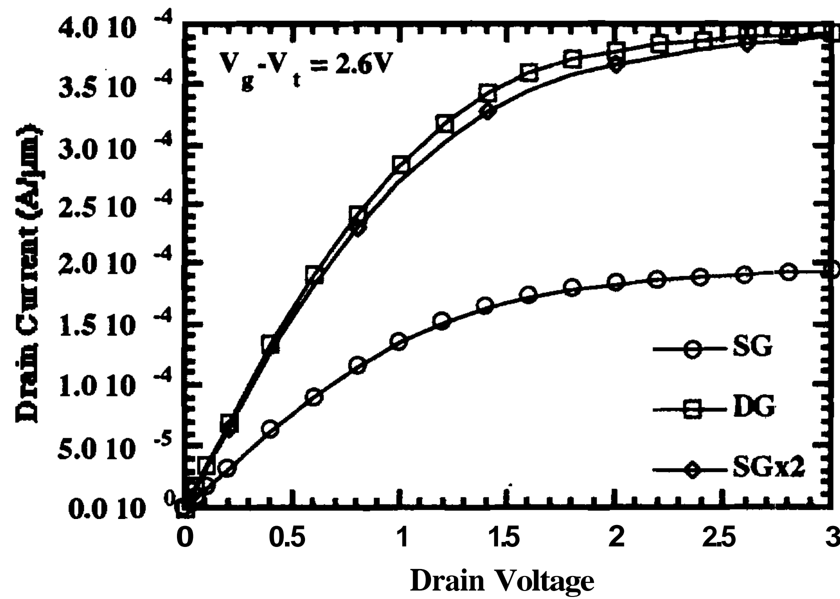
3.2.4 A Final Note on Current Enhancements

In dealing with drain current enhancements, it is very important to clearly define the term 'enhancement'. In the above sections, the enhancement has been defined as the ratio of the current in the dual-channel device to twice the current in the single channel device where the drain current is calculated under strong inversion (V_G-V_T=2.6V) and in saturation (V_D=3.0V). This definition of enhancement is used because this is the 'useful' enhancement in output current. Extreme care must be taken in comparing the output currents for single and dual-gate devices especially for short channel lengths. If the device design is such that the single-gated devices show significant short-channel effects such as channel length modulation, then the compared enhancements depend on the drain and gate voltages at which the currents are measured.

At the lower gate biases, the single channel devices suffer from severe channel length modulation. This is shown by the slope in the output characteristics for the single channel devices shown in tig.3.11 (a). The dual-channel devices are immune to **channel**



(a)



(b)

Figure 3.11 Output characteristics for a single-gated device and a dual-gated device for (a) V_G-V_T=0.3V and (b) V_G-V_T=2.6V. In fig. (a) the single-gated device shows evidence of channel length modulation

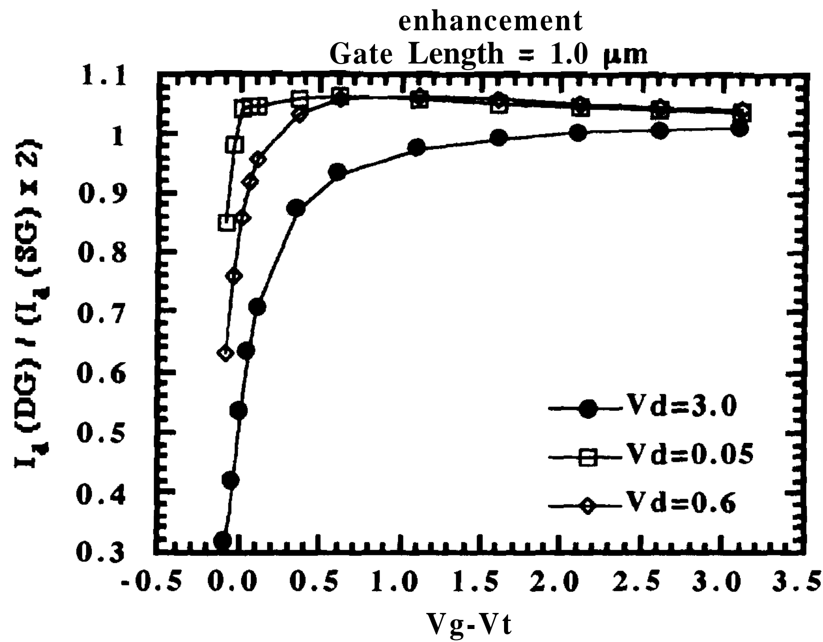
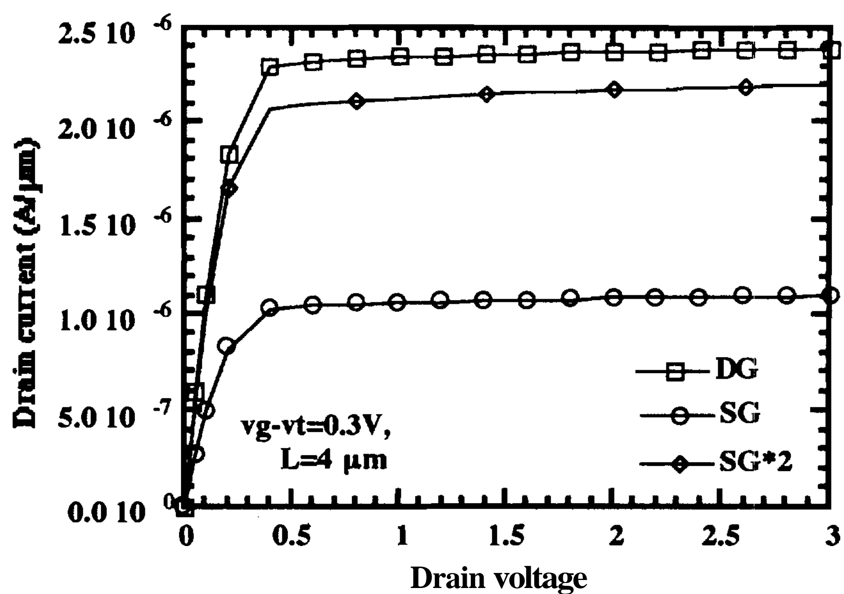


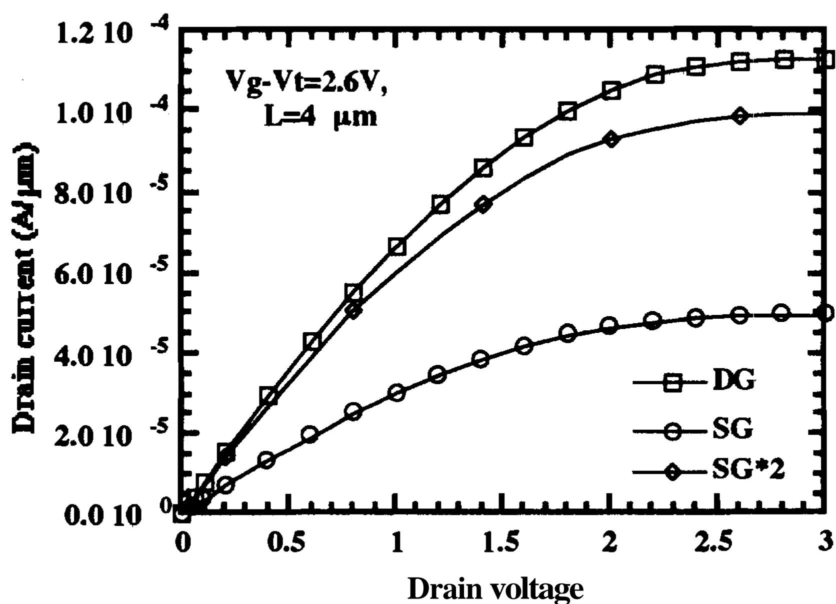
Figure 3.12 Enhancement in the drain current of dual-gated devices over single-gated devices as a function of gate voltage for different drain voltages

length modulation due to the stronger coupling between the gate and the channel. Thus at the low gate biases the device (whose gate length is 1.0μm) shows no enhancement. In fact the DG device exhibits a lower current than SGx2 in the figure. At the larger gate biases, the channel length modulation is reduced due to the stronger coupling between the gate and the channel (figure 3.11 (b)) and the enhancement consequently increases. This dependence of the enhancement on the gate bias is shown in figure 3.12. If the enhancement were calculated at a lower drain voltage (V_d=0.05V), then the channel length modulation effect is not seen. The enhancement defined at this lower drain voltage is also shown in figure 3.12. Again the maximum enhancement is about 10%.

In order to confirm the channel length modulation effect, the same device structure but with a gate length of 4.0μm was used in the simulations. The channel length modulation effects disappeared as expected and the enhancement was more or less independent of the drain voltage at which they were calculated. The output characteristics of the SG and DG MOSFETs with L=4.0μm under both weak and strong inversion is



(a)



(b)

Figure 3.13 Output characteristics for a long channel (4 μm) single-gated device and dual-gated device for (a) V_G-V_T=0.3V and (b) V_G-V_T=2.6V. No channel length modulation is observed even for small gate voltages

shown in figure 3.13. The flat saturation regions for both the DG and the SG devices in both the curves confirms the absence of short-channel effects. The enhancement in current is also very similar.

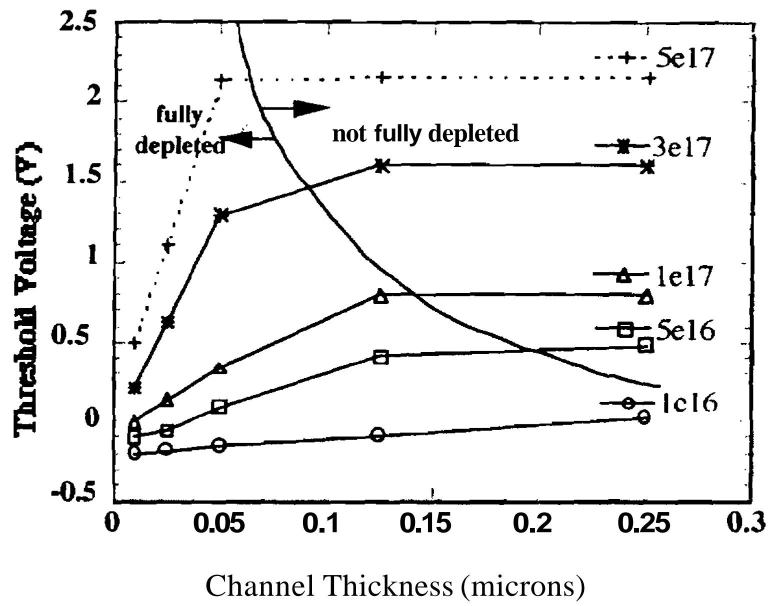
Thus in conclusion due to severe short channel effects encountered in the SG MOSFET, the enhancement in the drain current of the DG MOSFET is dampened at the lower gate voltages and the enhancement approaches a maximum value at V_G-V_T=2.6V. The analyses and the conclusions in the previous sections have therefore been restricted to the strong inversion region of operation.

3.3 Short Channel Immunity in Dual-Gated SOI MOSFETs

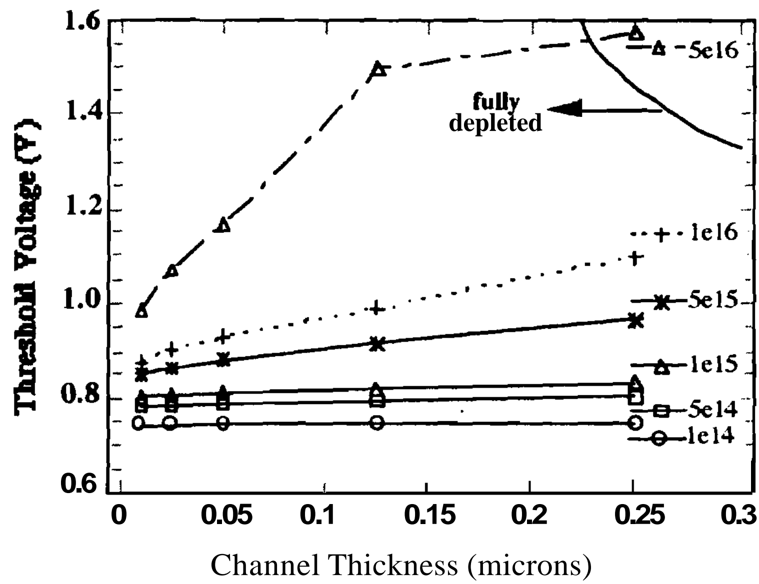
In this section, the advantages of dual-gated thin-film SOI MOSFETs, are described with particular emphasis placed on its short-channel immunity. Short channel effects in n-channel silicon-on-insulator (SOI) MOSFETs with P^+ polysilicon gates are analyzed using two-dimensional device simulations. The analyses suggest that dual-gated MOSFETs with P^+ polysilicon gates are more immune to short channel effects than conventional single-gated devices. Digressing for a moment, the use of P^+-polysilicon gates allows the threshold voltage of conventional single-gated Silicon-on-Insulator(SOI) MOS Field Effect Transistors to be fixed by 'work function engineering' rather than by intrinsic device parameters such as channel doping and SOI film thickness. Consequently, the channel doping in these devices can be extremely low which results in superior gains and higher channel mobilities. However, simultaneously the devices demonstrate severe short channel effects such as drain-induced-banier-lowering(DIBL) and premature punchthrough. Dual-gated MOSFETs with P^+-polysilicon gates control the short-channel effects while simultaneously reaping the benefits of low channel doping concentrations. In addition, the dual-gated MOSFET could significantly increase the design window options (in so far as the choice of film thickness is concerned) available so that the device could be designed to counter both the large drain fields (which lead to hot-electron effects and parasitic bipolar action) as well as short channel effects such as punch-through and DIBL. Mahli et al [20] and Davis et al [21] have extensively studied the applications of P^+-polysilicon gates in thin-film SOI technology. Aoki et al [22] have also investigated the design considerations for thin-film fully-depleted devices and provided useful guidelines for the theoretically allowable film thickness, channel doping, and gate work function. It was concluded that

P+-polysilicon gates provide a larger design window than do N+-poly gates for thin-film SOI device applications. In addition, Pt-gated devices provide higher gain and improved breakdown capabilities over similar devices with N+-gates[21].

The choice of gate material affects the device performance of thin-film SOI MOSFETs. N+-polysilicon gates are the most commonly used gate material in CMOS designs for both n-channel and p-channel SOI MOSFETs. However, in N^+-poly gated thin-film fully-depleted n-channel SOI MOSFETs, the threshold voltage is a strong function of both the channel doping and the SOI film thickness. As the film thickness is reduced the threshold voltage decreases till it finally achieves a negative value commensurate with normally-on operation which is obviously undesirable from the point of view of static power dissipation. The use of P^+-gated buried n-channel devices overcomes this drawback. P^+-polysilicon gates allow the threshold voltage to be fixed by 'work function engineering' rather than by the intrinsic device parameters such as channel thickness or doping. Thus, the threshold voltage of devices with P^+-poly gates remain approximately independent of the channel doping or thickness for a range of values of the two parameters. The threshold voltage of n-channel SOI MOSFETs with both n^+-polysilicon and p^+-polysilicon gates are plotted in figure 3.14 as a function of doping concentration and silicon film thickness. These values were obtained for long-channel devices from the analytical formulation detailed in Section 3.2.2. The threshold voltage of the n+-gated device shows a strong dependence on the channel doping and the SOI film thickness. For normally-off operation the practical device threshold voltage must be in the range from 0.5-0.7 V. With reference to the figure, n-channel thin-film SOI MOSFETs with n+-gates would require extremely high channel doping concentrations in the order of $10^{17}/cm^3$ to achieve threshold voltages in the vicinity 0.5V. The heavy doping concentration affects several device characteristics. Specifically, the vertical electric field increases and degrades mobility due to increased surface scattering. Besides, the low field mobility is also drastically reduced by impurity scattering. The low field mobility affects both the transconductance and the output drive current capability of the dlevice. In addition the gain of the device is also reduced. Moreover, the process variation tolerance is extremely poor and small variations in the channel doping profile or SOI film thickness could cause a large variation in the threshold voltage. For a p^+-gated n-channel MOSFET, the threshold voltage shows little or no variation with channel thickness or channel doping for doping concentrations in the range from 10^{14}-$10^{15}/cms^3$. The threshold voltage is pinned at around 0.8-0.9V for channel thicknesses around 100nm and channel doping



(a)



(b)

Figure 3.14 Threshold voltages in (a) N+-polysilicongated and (b) p^+-polysilicon gated n-channel SOI MOSFETs, as a function of channel thickness and channel doping

concentrations from 1×10^{14}-$5\times10^{15}/cms^3$. Thus, normally-off operation is easily achieved for very low doping concentrations which results in increased effective channel mobilities and consequently improved device gain and transconductance. Also, the process variation tolerance is considerably better.

The threshold voltage of p^+-gated n-channel MOSFETs, which is fixed at around 0.8V as seen above, is higher than the optimum 0.5V and has been considered a major 'drawback' of the above device [23]. The higher the threshold voltage the lower the saturation current capability of the device. Therefore, it is advantageous to operate the device at as low a threshold voltage as possible without suffering from excessive off-state leakage. In fig. 3.15 we plot the simulated output drain characteristics of the single-gated thin-film n-channel MOSFET with n^+ and p^+ polysilicon gates. Two dimensional simulations were carried out over a range of bias conditions and structural dimensions using the PISCES-IIB device simulator. In addition to field and doping:dependent carrier mobilities, the effect of the perpendicular electric field on carrier mobility was incorporated to account for surface mobility degradation associated with increased carrier scattering. Variations in structural dimensions included varying the SOI film thicknesses and the front and back oxide thicknesses. The SOI film doping concentration was also varied in all simulations. The results were similar in all cases investigated so long as fair comparisons were maintained between n+-gated and p^+-gated devices. Only the results from sample devices are presented herein. The simulated devices, unless otherwise specified, had a drawn gate length of 1 µm and oxide thicknesses (both front and back for the dual-gated MOSFET) of 250Å. Interfacial traps were neglected at the two interfaces. Fixed interface charges were specified as $10^{10}/cms^3$ and $10^{11}/cms^3$ for the front and back interfaces respectively. The single gated devices had a buried oxide thickness of 3000Å. The SOI film thickness was 0.1µm. Abrupt source/drain junctions were assumed for all device structures simulated. The device with the n+-poly gate has a channel doping of $7\times10^{16}/cms^3$ and a threshold voltage of 0.4V (which is slightly lower than the optimally desired value) while the p^+-poly gated device has a channel doping of $1\times10^{15}/cms^3$ and a threshold voltage of 0.9V. The drain currents are plotted for the same value of V_{GS} (=5.0V). It is clear that although the p^+-gated device has twice the threshold voltage of the n+-gated device, the output current capabilities of the two devices are more or less identical. In fact, the p^+-gated device exhibits a higher saturation drain current, due mainly to its larger gain evident in fig. 3.15 by its larger slope in the linear region. The larger gain arises from the low channel doping in the p^+-gated devices which in turn yields higher channel mobilities.

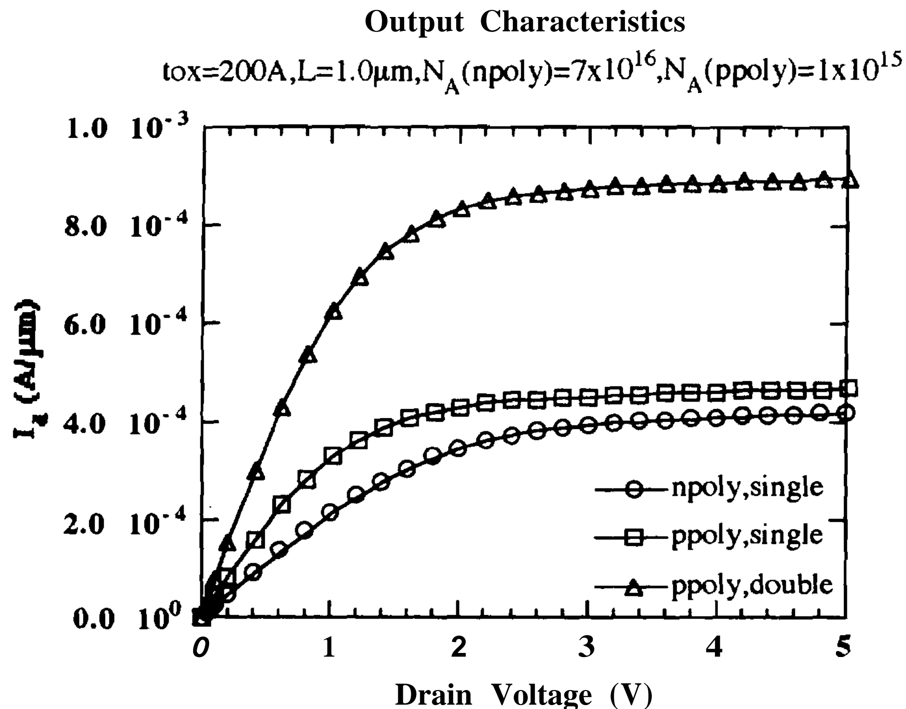


Figure 3.15 Comparative output characteristics of n+-poly single, p^+-poly single and p^+-poly dual gated n-channel SOI MOSFETs

Thus the Large threshold voltages of the p^+-gated devices cannot entirely be considered a disadvantage. In addition, the higher V_T should yield better noise margins for the device and lower off-state leakage currents.

A second major disadvantage with the use of p^+-polysilicon gates noted in references [21,23] is the poor off-state characteristics of the device. The poor off-state characteristics result from the weak gate control of the channel region by p^+-gates. The off-state characteristics are controlled by the fringing fields at the back interface. The fringing field [24] depends on the channel doping at the back interface, the thickness of the SOI film, the charge state of the back interface and the thickness of the buried oxide layer. Increasing the channel doping, accumulating the back interface and reducing the buried oxide thickness all contribute to increasing the value of the fringing field. In [21,23] the first two methods of increasing the fringing fields were provided as possible soiutions to

improving the off-state characteristics of the SOI devices with p^+-poly gates. Specifically, the two solutions offered were (i) to introduce a heavily doped channel region at the back gate and (ii) to accumulate the back interface with an appropriate substrate bias. Both of these proposed techniques act to inhibit the penetration of the drain field in the channel region at the back interface and increase the front gate control of the channel region. However, neither of these solutions are practically realizable. Due to the ultra-thin nature of the SOI film (typically 100nm or less) it is extremely difficult to control the channel implant so as to obtain an extremely sharp profile at the back interface, while maintaining a very low uniform doping concentration in the rest of the channel region. Again, accumulating the back interface using a substrate bias would require large biases for the thick back oxides encountered (voltage values greater than 5 volts are typically unavailable on CMOS chips). Moreover, the substrate bias would serve to deplete the back interfaces in complimentary p-channel devices unless additional process steps were undertaken to isolate the substrates for the individual devices.

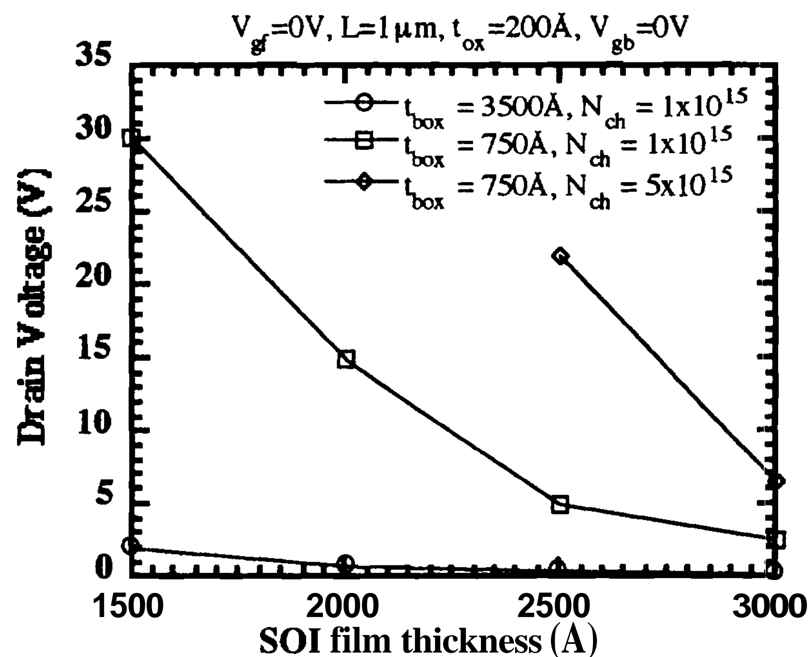
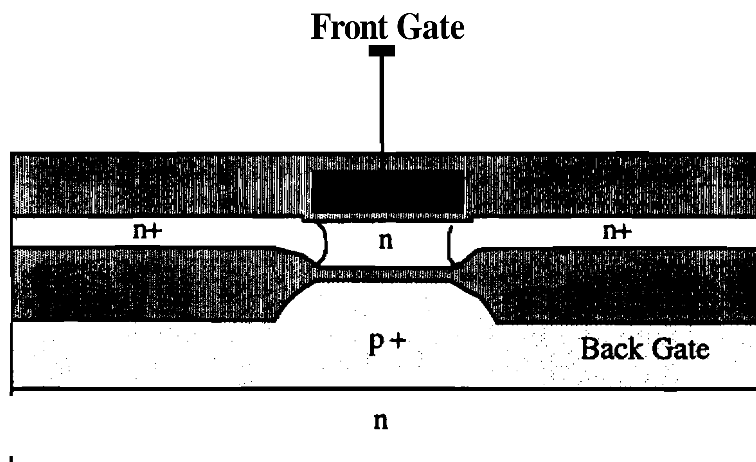


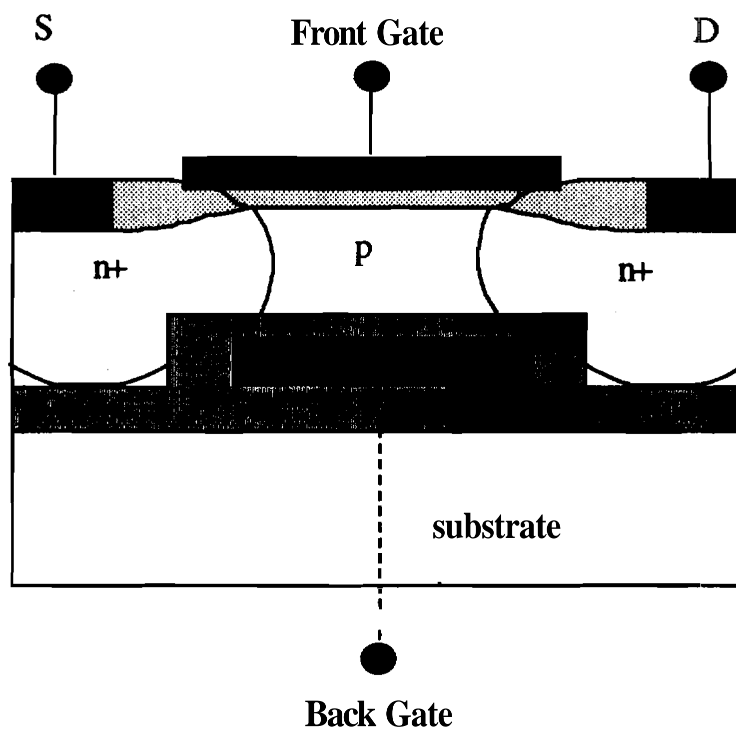
Figure 3.16 Variation of the punchthrough voltage for thick and thin back oxide thicknesses as a function of the SOI film thickness for n-channel SOI MOSFETs with neutral gates

Another scheme to increase the fringing fields at the back interface and never before exploited explicitly for this reason is to reduce the back/buried oxide thickness. In fig. 3.16 we plot the variation of the punch-through voltage of p^+-poly gated n-channel SOI devices as a function of channel thickness for two different back oxide thicknesses. It can be seen that a reduction in the buried oxide thickness from 3500Å to 750Å causes a large increase in the punch-through voltage. In the above calculations the punch-through voltage has been defined as the drain voltage (with V_{GS}=0.0V) at which the drain current reaches 1nA/µm.

However, decreasing the back oxide thickness uniformly across the wafer (as was proposed in reference [25]) would significantly increase the sourceldrain to substrate capacitance of the devices and result in poor speed performances. Moreover, it was seen in Chapter 2 that the inverse sub-threshold slope of the SOI MOSFET increased as the buried oxide was made thinner. Thus thinning the buried oxide and using it as a parameter to control short-channel effects in conventional single-gated MOSFETs would definitely be detrimental to the main advantages offered by the SOI devices, namely, lower parasitic junction capacitance and improved sub-threshold slopes. Taking this argument a step further, if the back oxide thickness could indeed be used as a parameter to control short-channel effects in p^+-gated thin-film SOI MOSFETs, the buried oxide must be selectively thinned down in the channel region alone as shown in fig. 3.17(a). This would take care of the problem of increased parasitic source/drain capacitance. Operating the device under dual-gate control would provide excellent gate control over the channel region and thereby maintain extremely sharp sub-threshold slopes. A device structure that achieves the above constraints is the dual-gated device. The device structure is schematically illustrated in fig. 3.17(b). The dual-gated device lends the designer the option of either keeping the back gate grounded or using the device under dual-gate control. Dual-gate operation would be the preferred mode of operation. The device structure of figure 3.17(a) was in fact proposed in reference [26] as the ultimate scalable MOSFET. The thinner oxide in the channel region and the p^+-substrate are proposed to alleviate problems related to punch through in the near intrinsic channel. The p^+-polysilicon gate replaces the p^+-substrate in the dual-gated device structure. The need to self-align the top and bottom gates is apparent in figures 3.17(a) and (b). Any overlap of the S/D regions and the bottom gate only adds to parasitic capacitance which would ultimately slow down the device performance. In the following section a process to form a fully self-aligned dual-gated structure will be introduced for the first time. Like any self-aligned scheme, the proposed process aims at reducing device parasitics while maintaining a high device performance.



(a)



(b)

Figure 3.17 (a) SOI MOSFET structure with thin back-oxide in the channel region and thick back-oxide in the extrinsic region (b) Dual-Gated SOI MOSFET with polysilicon gates. This is structurally similar to (a) above

In fig. 3.15 we have also plotted the output characteristics of the dual-gated device under dual-gate operation. The dual-gated device again has a channel doping of $1x10^{15}/cms^3$ and a threshold voltage of 0.9V [2]. The current vector plots illustrating current flow in the dual-gated device and the single gated device are depicted in figure 3.18. The figure indicates the presence of a large sub-surface current due to volume inversion in the dual-gated device. The single gated device however shows mainly surface conduction. In spite of the additional bulk current flowing in the dual-channel device, a two times increment in current is observed over the single gated device corresponding to the two surface channels present under dual-gate operation, commensurate with the results presented in section 3.2. The two-times current increase is however not the prime motivating factor dictating the use of dual-gated devices. The impact of the dual-gate device is felt in terms of its short-channel immunity. Figure 3.19 shows the potential contours for p^+-poly single-gated and dual-gated devices when V_{DS}=5.0V and V_{GS}=0.0V. The figure indicates a significantly smaller excursion of the drain field in the channel region of the dual-gated MOSFET. The lesser penetration by the drain field results in better punch-through capabilities and lower off-state leakage. The DIBL immunity offered by the dual-gated MOSFET is clearly illustrated in fig. 3.20, which shows the conduction band profile for p^+-gated single-gated (SG) and dual-gated (DG) MOSFETs for both low and high drain biases. The barrier reduction at the source by the drain field is seen to be lower in the DG device than in the SG device. Also shown as insets in the figure are the degradation in the sub-threshold slopes under high drain biases for the SG and DG devices. These curves further confirm the DIBL immunity offered by the DG MOSFET. Fig. 3.21 shows the threshold voltage roll-off for the SG and DG devices as a function of gate length. The threshold voltage roll-off (which is a measure of the short-channel effect) is lower for the DG MOSFET than for the SG device. Only at a gate length of 0.4 μm does the DG MOSFET begin to suffer from any short-channel effects. Thinner (front and back) gate oxides must be used at these channel lengths to ensure good device characteristics.

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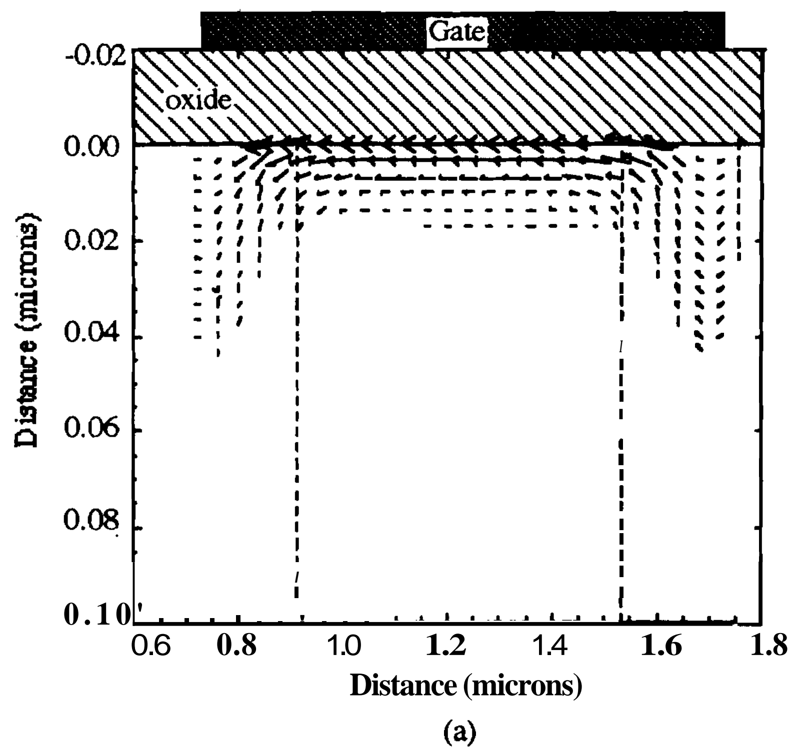
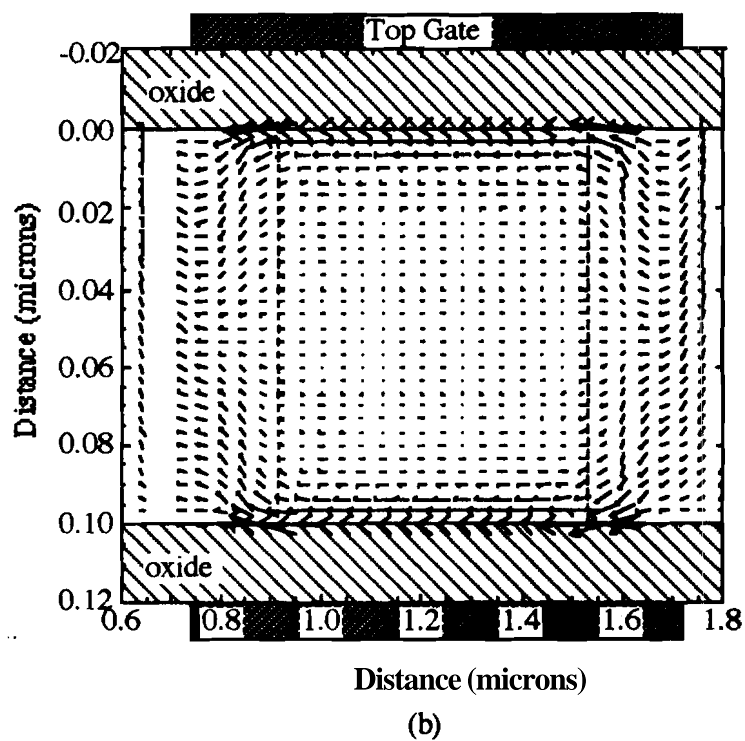
[2]Since the threshold voltage of p^+-poly devices is fixed by the gate work function rather than the intrinsic device parameters, the threshold voltage of the p^+-poly dual-gate devices is the same as that of the single gate devices. When n^+-poly gates are used, V_T of the dual-gated devices are typically a lot smaller than the V_T of corresponding single-gated devices and they consequently demand a higher channel doping concentration to maintain normally-off operation and minimize off-slate leakage currents.

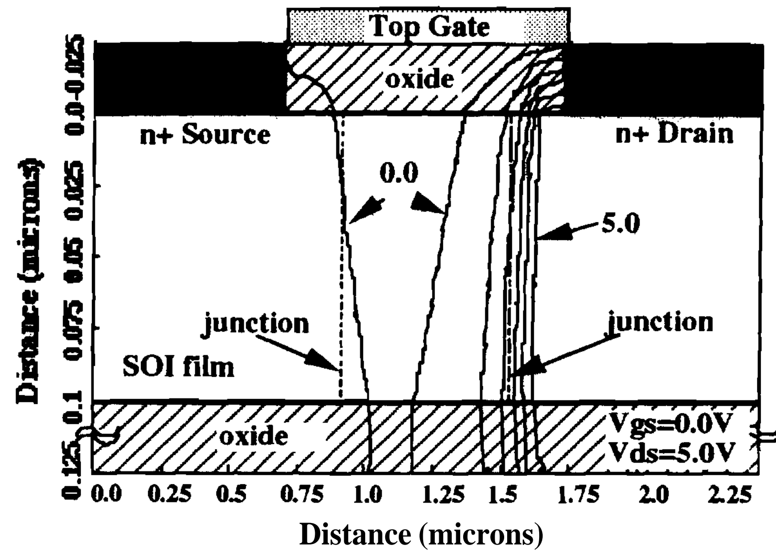


(a)

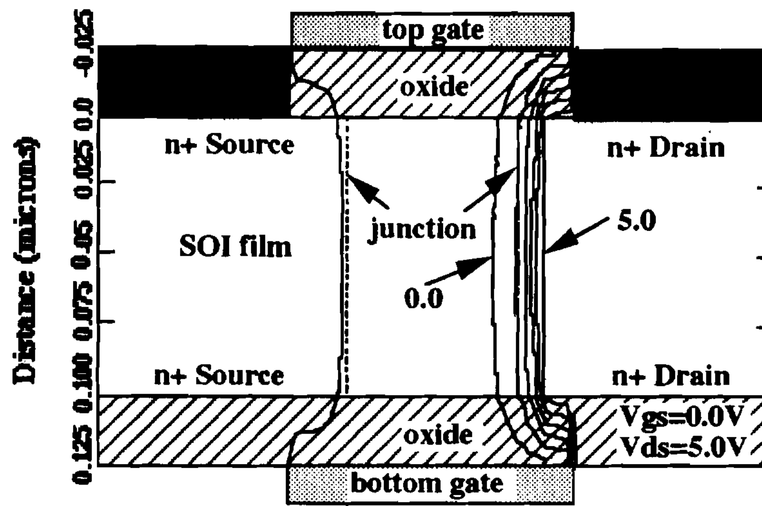


(b)

Figure 3.18 Current vector contours for (a) single-gated and (b) dual-gated n-channel SOI MOSFETs with p^+-polysilicon gates

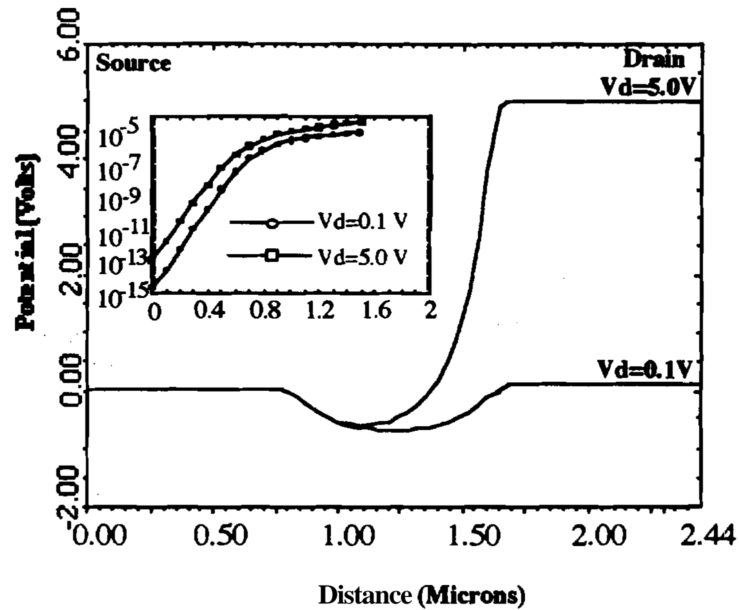


(a)

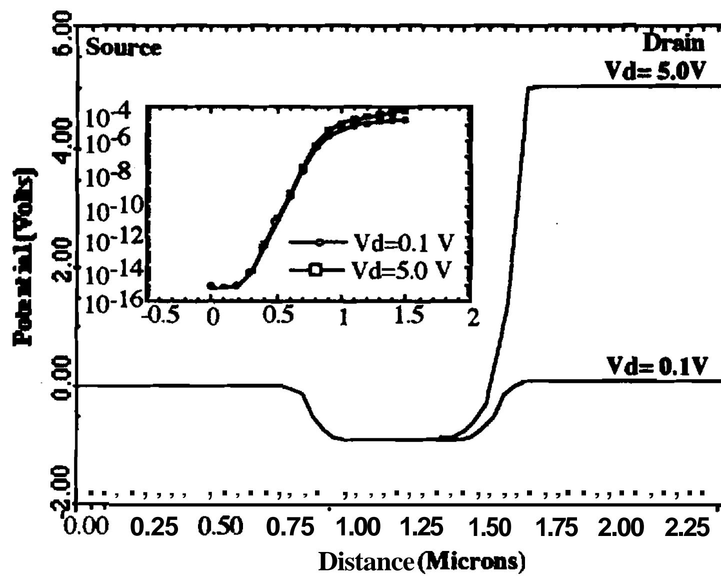


(b)

Figure 3.19 PISCES simulated equipotential contours in increments of 0.1V at V_{DS}=5V and V_{GS}=0V for (a) a single gated NMOSFET and (b) a dual-gated NMOSFET. The gate material in both cases is P^+-polysilicon and the channel doping is $1x10^{15}/cm^3$



(a)



(b)

Figure 3.20 PISCES simulated conduction band profile from Source to Drain for (a) a single-gated NMOSFET and (b) a dual-gated NMOSFET. The band bending is plotted along the back interface for the single gated MOSFET and along the center of the SOI film for the dual-gated MOSFET. The sub-threshold characteristics under low (V_D=0.1V) and high (V_D=5.0V) are shown as insets

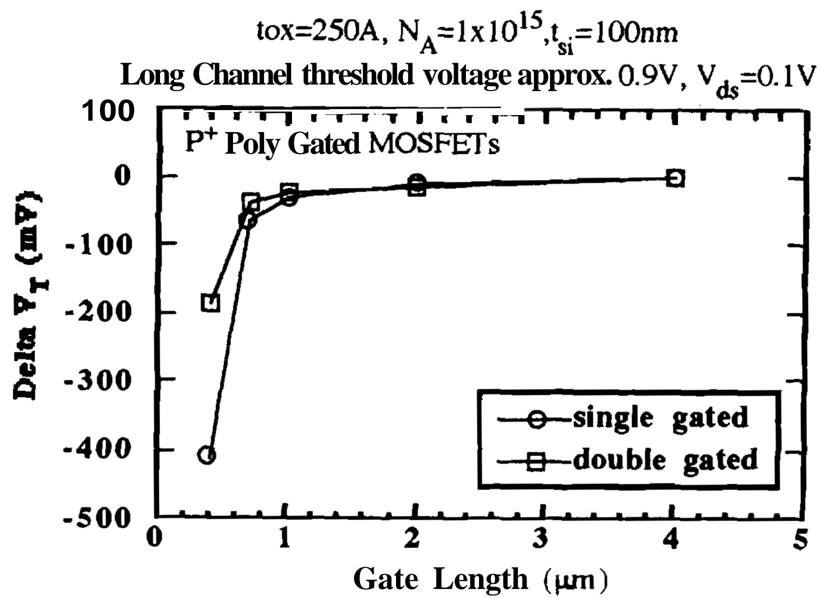


Figure 3.21 Simulated threshold voltage roll-off versus channel length for a single-gated and dual-gated MOSFET

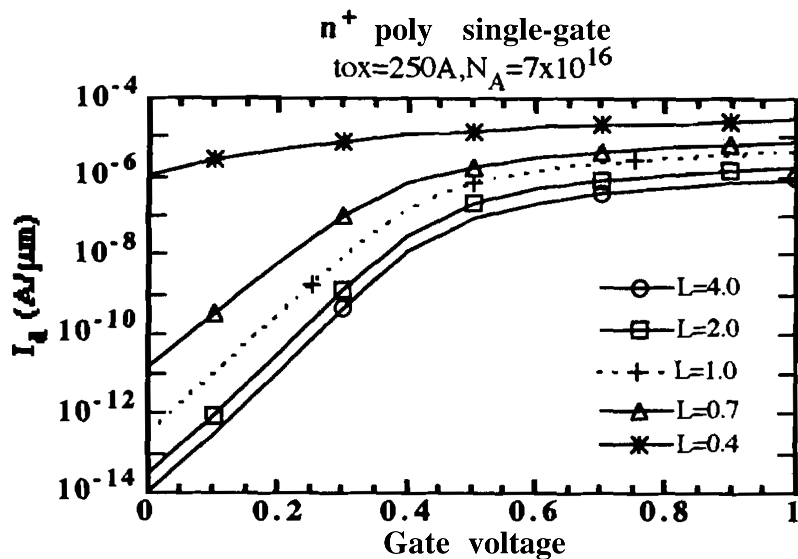


Figure 3.22 Subthreshold characteristics for a single-gated NMOS device as a function of the channel length. The gate material is n+-polysilicon

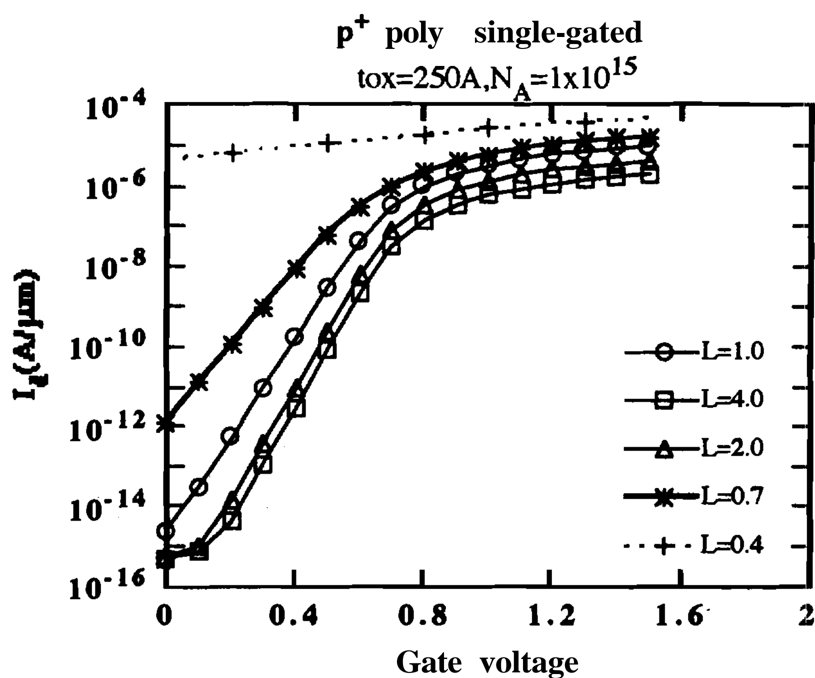


Figure 3.23 Subthreshold characteristics for a single-gated NMOS device as a function of the channel length. The gate material is p^+-polysilicon

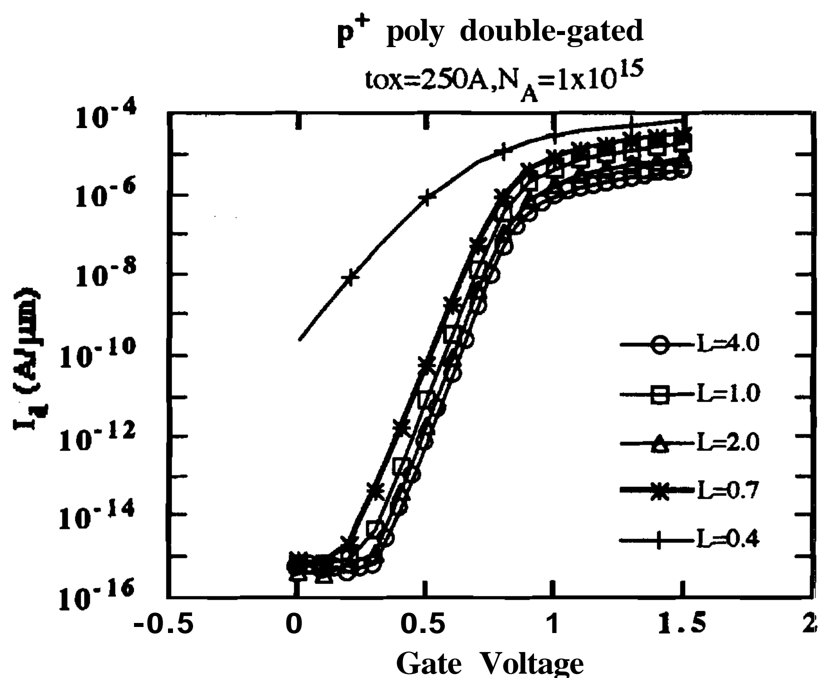


Figure 3.24 Subthreshold characteristics for a dual-gated NMOS device as a function of the channel length. The gate material is p^+-polysilicon

In Chapter 2, the effect of decreasing channel lengths on the sub-threshold characteristics was discussed. As the channel length decreases, the sub-threshold slope gradually degrades due to back channel leakage. At short channel lengths, thin-film single-gated SOI MOSFETs lose their advantage (superior sub-threshold slopes) over bulk MOSFETs. This is made clear in figure 3.22 and 3.23, which illustrates the degrading sub-threshold characteristics for both n+-polysilicon and p^+-polysilicon gated n-channel SOI MOSFETs. Finally, in figure 3.24 the improved sub-threshold behavior in dual-gated devices is depicted.

In summary, dual-gated devices with p^+-poly gates show improved short-channel immunity over corresponding SG devices while simultaneously maintaining the advantages of low channel doping, high gain and large process tolerances. In addition, the dual-gated device offers the option of operating either under single or dual gate control.

The increased fringing fields (obvious from fig. 3.19(b)) which lends the dual-gated MOSFET its short-channel immunity does not augur well with the device's hot-electron immunity. In fact, as shown in reference [26], the multiplication factor increases with increasing fringing fields. Therefore, it is imperative that lightly-doped-drain (LDD) regions be introduced to the reduce the propensity for hot-electron effects. Lightly doped source (LDS) regions should also be incorporated to minimize the likelihood of parasitic bipolar effects. Another effective scheme to reduce the field strength and its related hot-electron effects is to incorporate elevated sourceldrain structures. (A process flow demonstrating the fabrication of a elevated source/drain structure in a dual-gated SOI MOSFET is shown in the next section). The electric field in the channel of SOI MOSFETs decreases as the channel thickness increases. Thus in addition to drain engineering, the channel thickness could also be increased to reduce the channel fields. The maximum allowable channel thickness would again be determined by DIBL and punchthrough requirements. The short-channel immunity offered by the two gates allows the channel thickness of DG MOSFETs to be doubled without compromising device performance. Thus, the dual gated device provides a larger design window in terms of allowing both a range of channel doping concentrations and a range of channel thicknesses.

Lastly, in fig. 3.25 we plot the avalanche generation rate for the dual-gated device. The maximum avalanche generation rate occurs in the middle of the channel away from either the front or back interfaces. Hot-electron generation and its consequent injection into the front or back oxide interfaces causes both threshold voltage shifts and increased sub-

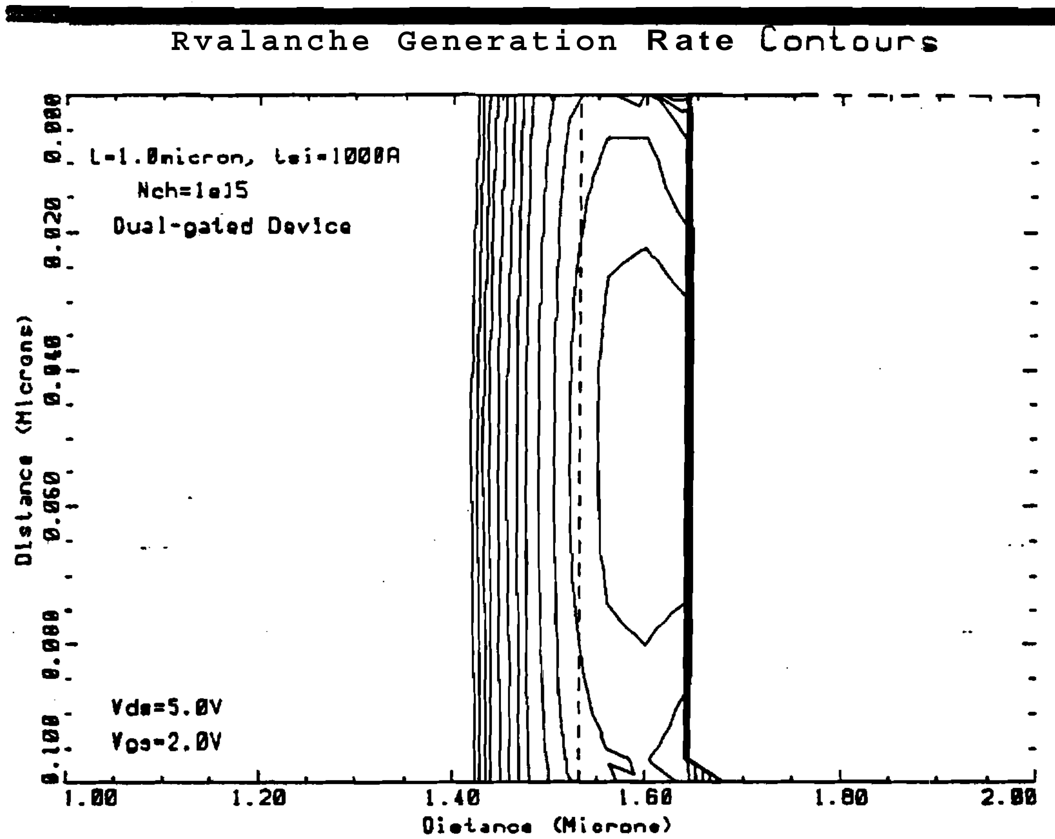


Figure 3.25 **PISCES simulated avalanche generation rate contours for a dual-gated n-channel MOS field effect transistor**

threshold leakage. By confining the hot-electron generation away from the interfaces these effects would be minimized.

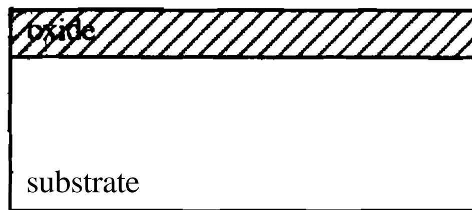
Before concluding this section it is important to reiterate that these simulations were made on a number of device structures and the trends established above were observed in all cases. Further optimizations to the device structures would change individual device parameters such as saturation current density, the onset of threshold voltage roll-off or the amount of sub-threshold degradation. But the superior short-channel immunity in the dual-gated device will be maintained under all cases simulated.

3.4 Process Design for Fully Self-Aligned Dual-Gated SOI MOSFETs

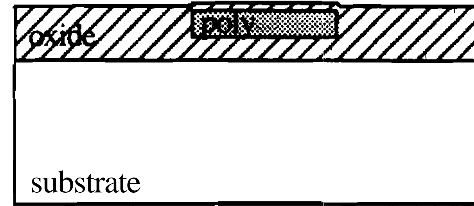
In this section we propose a novel process to fabricate a fully self-aligned dual-gated SOI MOSFET incorporating elevated source/drain regions. The top and bottom gates are self-aligned to attain minimum parasitic capacitances. The process flow is detailed in figs. 3.26 -3.28. In the first step , a first SOI region is epitaxially grown over a bottom gate either using epitaxial lateral overgrowth (ELO) [27] or confined lateral selective epitaxial growth (CLSEG) [28]. The length of the bottom gate is immaterial as long as it is larger than the actual gate dimension. The detailed process cross-sections are presented in figure 3.26 and 3.27. The individual process steps are clearly labeled in the figure. The top gate material is then deposited, defined and dry-etched down to the top gate oxide. After oxide spacers are formed, etching is continued vertically through the SOI layer and down to the bottom gate oxide to form the stack shown in fig. 3.28(5). Once again the individual process steps are described in detail in the figure. Nitride spacers are then formed to inhibit oxidation at the exposed SOI film sidewalls and the bottom gate is defined through continued dry-etching (fig. 3.28(7)). The bottom gate is oxidized so that it is completely isolated. The nitride spacers are then removed from the stack to expose the sidewalls of the SOI film. These sidewalls are now used as seed holes for selective epitaxial silicon deposition to form the source and drain regions. In-situ doping could be used to form the lightly doped source and drain regions. The n+- region is then implanted from the top to form the elevated S/D regions. The advantage of such a structure is the minimized source/drain resistance even for ultra-thin channel regions. Both the top and bottom gates are defined with a single lithography and are thus self-aligned. This reduces all parasitic overlap capacitance between either gate and the source/drain regions. The completed

Process Flow for the Fully-self-aligned Dual-gated SOI MOSFET

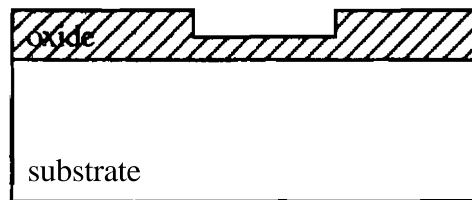
1. Front end processing (ELO)



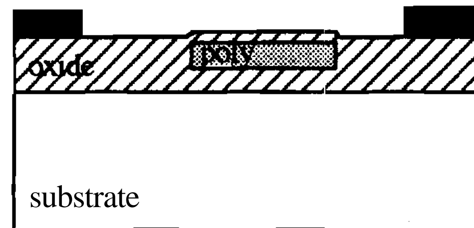
1, Field Oxidation



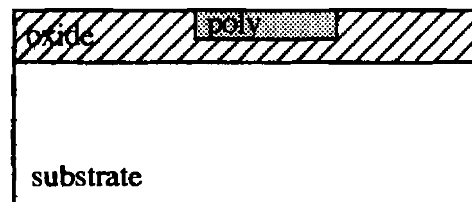
4. Oxidize bottom gate - either oxide or oxy-nitride



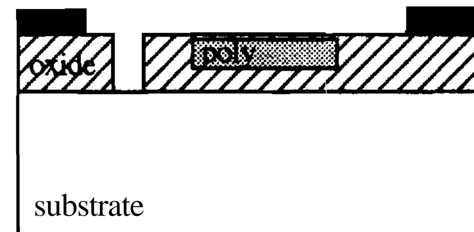
2, Pattern Gate1 mask, etch oxide trench



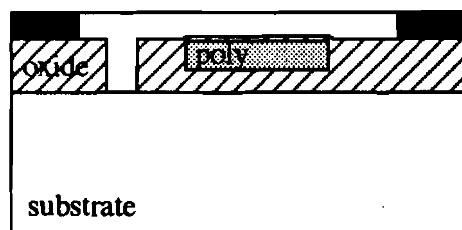
5. Deposit and pattern planarization etch stops



3. Deposit Gate1 and planarize to fill trench



6. Open seed holes



7. Grow epitaxial silicon and planarize to the etch stop

Figure 3.26 Self-aligned dual-gated SOI MOSFET process depicting front-end processing for ELO

2. Front end processing (CLSEG)

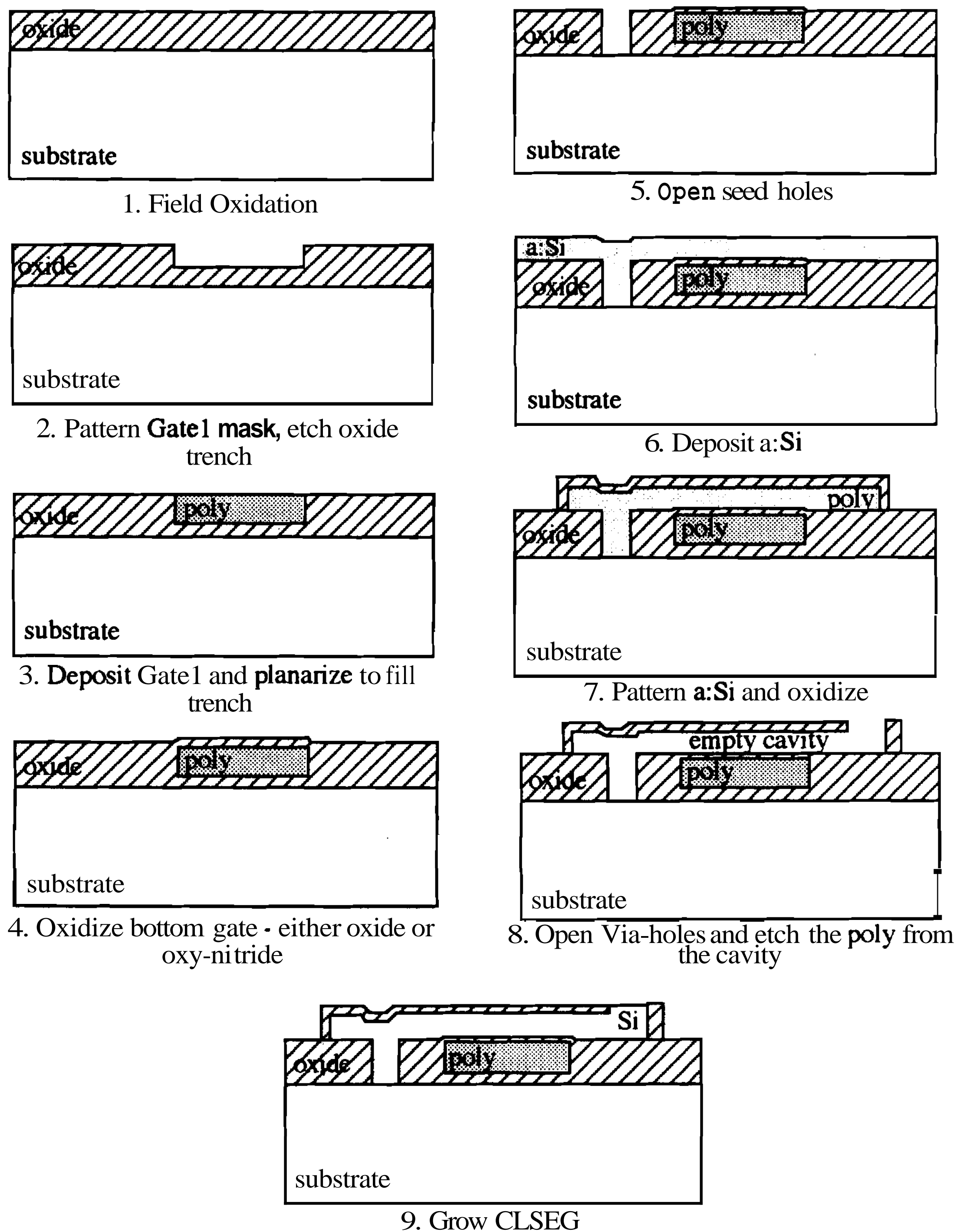


Figure 3.27 Self-aligned dual-gated SOI MOSFET process depicting front-end processing for CLSEG

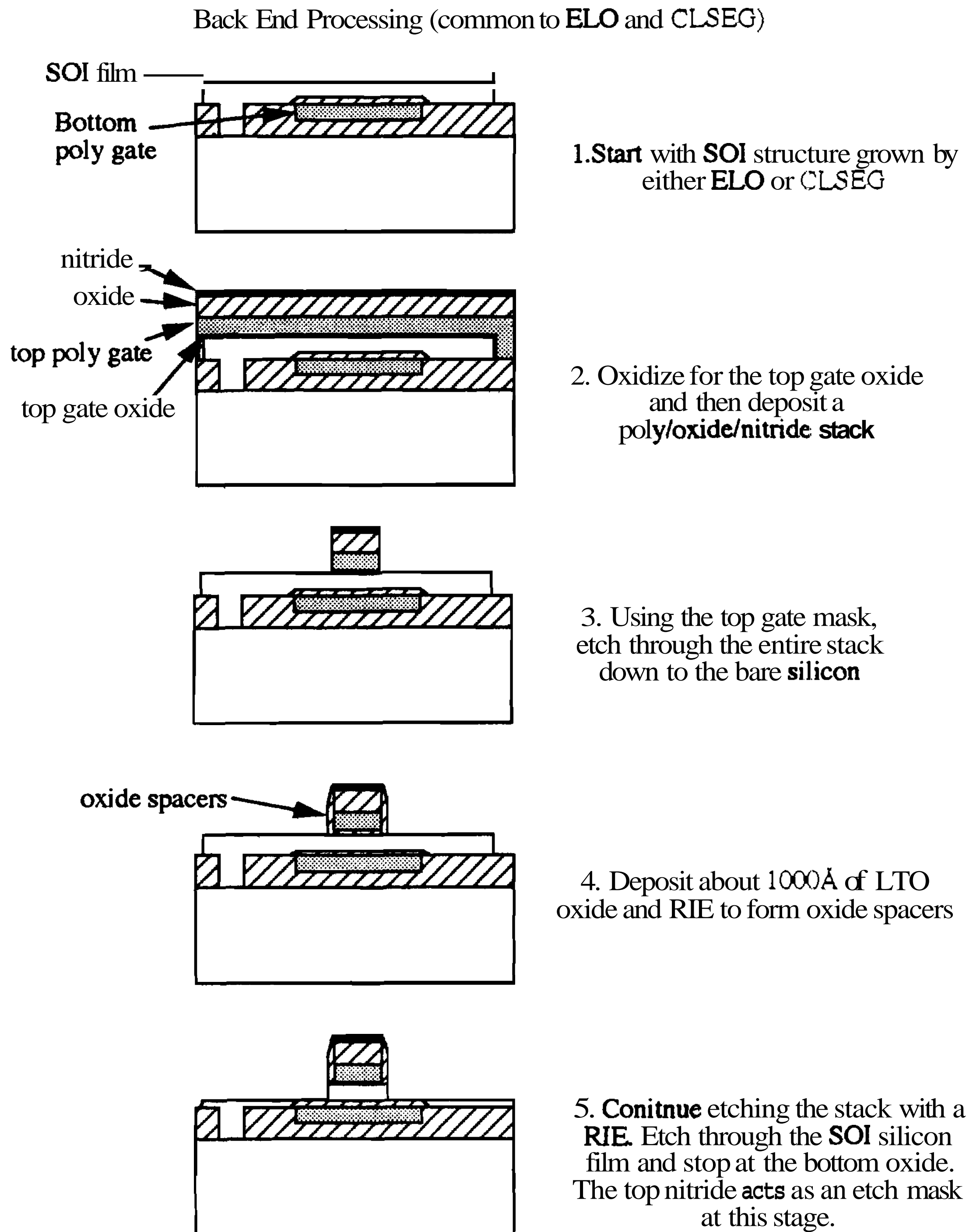
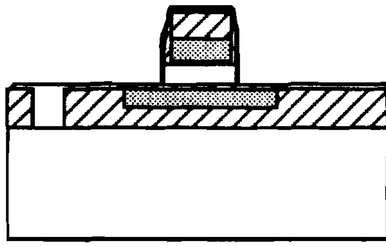
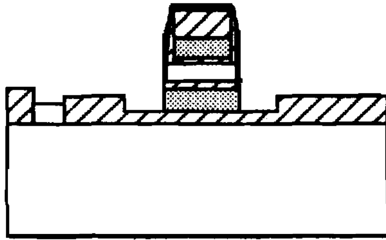


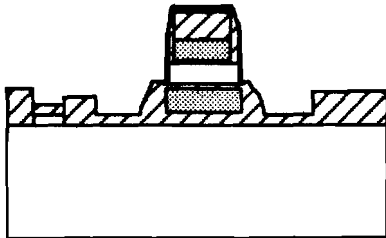
Figure 3.28 Self-aligned dual-gated SOI MOSFET process depicting back-end processing for ELO & CLSEG



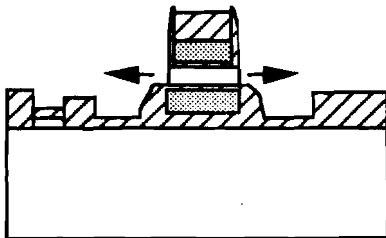
6. Deposit about 200-300Å of nitride and RIE to form the nitride spacer on the walls of the silicon film.



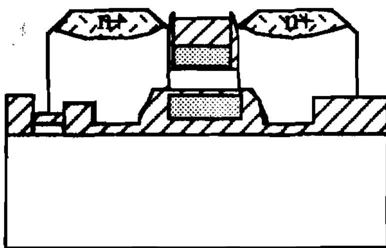
7. Continue etching through the bottom oxide andthe bottom poly gate



8. Now oxidize the bottom gate. The nitride spacers prevent oxidation on the silicon sidewalls.



9. Remove the nitride and prepare the wafer for selective epitaxy.



10. During epitaxy the n- region can be tailored depending on the device design. The n+ region can then be implanted from the top. The structure is an elevated Source/Drain structure and is the only instance of an elecvated S/D structure in SOI material.

Figure 3.28, continued

device structure is shown in fig. 3.28(10).

3.5 Conclusions

The effects of volume inversion in enhancing the properties of dual-channel MOSFETs were investigated using two-dimensional device simulations and one-dimensional analytical computations. It was shown that the output characteristics of dual-channel devices were not significantly enhanced over those of single-channel devices when the two devices were compared at constant V_G-V_T.

The design considerations involved in the fabrication of thin-film SOI MOSFETs were discussed. A new way to control short-channel effects in SOI MOSFETs by thinning the back gate oxide was recognized. Optimum device performance with reduced hot-electron-effects and reduced short-channel effects, require the fabrication of moderately thin film transistors, with thin back gate oxides. Moreover, the channel doping must be low (1-5×10^{16}) for enhanced mobility and large transconductances. This precludes the use of n+-polysilicon gates which would require very high channel doping concentrations for normally off operation. P^+ polysilicon could be used as the gate material for n-channel MOSFETs. P^+ polysilicon exhibits significant advantages as far as threshold control, breakdown and transconductances are concerned. However, in the off state. p-poly gates tend to maintain the interfaces in accumulation and therefore do not exercise sufficient control over the gate charge. As a result, p^+-poly gated devices are prone to premature punchthrough or DIBL effects, especially at the back interface. Thinning the back gate oxide again helps in controlling the DIBL and punch-through. But this scheme is detrimental to the current drive, sub-threshold slope and the parasitic drain/source to substrate capacitance. Simulations indicate that P^+-poly gates show improved short channel immunity over corresponding single-gated devices while simultaneously maintaining the advantages of low channel doping, high gain and large process tolerances. In addition, the dual gate device offers the option of operating under either single or dual-gate control.

A novel process sequence for self-aligning the top and bottom gates in a dual-gated SOI MOSFET was presented. The device has significant advantages over existing dual-gated SOI MOSFET technologies. The two gates can be independently biased which is essential for flexible design of SOI VLSI circuits. Furthermore, the top and bottom gates

are self-aligned. This self-alignment minimizes parasitics and reduces active area. The device is fully scalable and in fact conforms in device structure to the proposed ultimate scalable MOSFET.

3.6 References

1. T. Ungami and 0. Kogure, " High voltage TFTs fabricated in recrystallized polysilicon", *IEEE Trans. on Electron Devices,* ED-35(3), pp. 314, 1988.

2. A. Nakagawa, K. Furukawa, Y. Yamaguvhi, K. Tanzawa and H. Ohashi, "Application of dielectric isolation techniques based on silicon wafer bonding to power ICs", *Proc.* 1989 Symp. *High Voltage and Smart Power ICs,* pp. 271, 1989.

3. G.M. Dolny, A.C. Ipri, G.E. Nostrand, C.F. Wheatley and P.J. Wodarczyk, "Silicon-on-insulator approach for Power ICs integrating vertical DMOS and polycrystalline silicon CMOS thin-film-transistors", *IEEE Electron Device Letters* , EDL-13(10), pp. 516, 1992.

4. U. Apel, "100-V lateral DMOS transistor with 0.3μm channel in 1μm silicon-on-insulator-on-silicon, *IEEE Trans. on Electron Devices,* pp. 1655, July 1991.

5. T.W. Macelwee, I.D. Calder, R.A. Bruce and F.R. Shepherd, "High performance fully depleted silicon-on-insulator transistors", *IEEE Trans. on Electron Devices,* ED-37(6), pp. 1444, 1990.

6. T. Elewa, F. Balestra, S. Cristoloveanu, I.M. Hafez, J.P. Colinge, A.J. Auberton-Herve and J.R. Davis, "Performance and physical mechanisms in SIMOX MOS transistors operated at very low temperatures". *IEEE Trans. on Electron Devices,* ED-37(4), pp. 1007, 1990.

7. Y. Omura and K. Izumu, "Temperature Dependence of dynamic operation in ultra-thin CMOSISIMOX", *IEEE Trans. on Electron Devices,* ED-38(1), pp. 101, 1991.

8. L. Hobbs *et al.* , "SOI MOSFETs fabricated in electron-beam recrystallized polysilicon with improved breakdown", *IEEE Electron Device Letters,* pp. 385, Aug. 1989.

9. K.K. Young *et al.,* "SOI CMOS device operation at liquid nitrogen temperature", *IEEE Electron Device Letters,* pp. 126, March 1990.

10. A. Kamgar *et al..* "Ultra-high speed CMOS circuits in thin SIMOX films", *IEDM Tech. Dig.,* pp. 829, 1989.

11. J.G. Fossum, J.Y. Choi and R. Sundaram, "SOI Design for Competitive CMOS VLSI", *IEEE Trans. on Electron Devices,* ED-37, pp. 724, March 1990.

12. F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini and T. Elewa, "Double-Gate Silicon-on-InsulatorTransistor with Volume Inversion: A New Device with Greatly

Enhanced Performance," IEEE Electron Device Lett., vol. EDL-8, No. 9, pp. 410-412,1987.

13. R. P. Zingg, B. Höfflinger and G. W. Neudeck, "Dual-Gate SOI CMOS Technology by Local Overgrowth (LOG)," IEEE SOSISOI Workshop *Proc.*, pp. 134-135. 1989.

14. J. P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes and C. Claeys, "Silicon-on-Insulator 'Gate-All-Around Device'", IEDM Tech. Dig., pp. 595-598, 1990.

15. TMA, "PISCES IIB Two-Dimensional Device Analysis Program", Technology Modelling Associates Inc., Version 8908, 1989.

16. M. Yoshimi, H. Hazama, M. Takahashi, S. Kambayashi, T. Wada, K. Kato and H. Tango, "Two-Dimensional Simulation and Measurement of High-Performance MOSFETs made on a very Thin SOI Film," IEEE Trans. on *Electron* Devices, Vol. 36, No. 3, pp. 493-503, 1989.

17. G. A. Armstrong and W. D. French, "Optimized Design For a 0.5mm Gate Length n-Channel SOI MOSFET," Electronics *Lett.*, Vol. 26, No. 15, pp. 1196-1198, 1990.

18. R. Lake and S. Datta, "Non-equilibrium Green's function method applied to double-barrier resonant tunneling diodes", Phys. Rev. B, vol. 45, no. 12, pp. 6670, 1992.

19. R. Lake and S. Datta, "Energy balance and heat exchange in mesoscopic systems", Phys. Rev B, vol. 46, no. 8, pp. 4757, 1992.

20. S.D.S. Malhi, H.W. Lam, R.F. Pinizzotto, "Novel SOI CMOS Design using ultra thin near-intrinsic substrate", IEDM Tech. Papers, pp. 107, 1982.

21. J.R. Davis, G.A. Armstrong, N.J. Thomas and A. Doyle, "Thin-film SOI CMOS Transistors with p^+-polysilicon gates", IEEE ED-38, pp. 32, 1991.

22 T. Aoki, M. Tomizawa and A. Yoshii, "Design considerations for thin-film SOI/CMOS device structures", IEEE ED-36, pp.1725, Sep. 1989.

23. C.T. Lee and K.K. Young, "Sub-micrometer near-intrinsic thin-film SOI complementary MOSFETs", IEEE ED-36, pp. 2537, Nov. 1989.

24. S. Veeravaghavan and J.G. Fossum, "Short Channel Effects in SOI MOSFETs.", IEEE ED - 36 *(3)*, Mar 1989.

25. Y. Omura, S. Nakashima, K. Izumi and T. Ishii, "0.1mm gate, ultra-thin CMOS devices using SIMOX substrate with 80nm thick buried oxide layer", IEDM Tech. *Dig.*, pp. 675, 1991.

26. M. Fukuma, "Limitations on MOS ULSI's", *Symp. VLSI Technology Dig. Tech. Papers*, pp7, May 1988.

27. L. Jastrezebski *et al.*, " Growth of electronic quality silicon over oxide by epitaxial lateral overgrowth",J. *Electrochem. Soc.*, vol. *129,* pp. 2645, 1982.

28. P.J. Schubert and G.W. Neudeck, "Confined Lateral Selective Epitaxial Growth of silicon for device fabrication", *IEEE Electron Device Letters, EDL-11*(5), pp. 181, 1990.

CHAPTER 4
PROCESS DEVELOPMENT FOR ELO AND CLSEG SOI MOSFETS

Dual-gated devices extend device design options over conventional single-gated devices. The virtues of dual-gated devices were voiced in Chapter 3. The immunity to short channel effects in dual-gated devices comes about because of a more or less one dimensional potential distribution across the film. The same one-dimensional potential contours can be achieved by using a single-gated SOI MOSFET fabricated on a extremely thin (< 1000Å) silicon film. However, in terms of process development and technological feasibility, ultra-thin films are extremely difficult to fabricate. In state-of-the-art SIMOX technology for example, high-dose multiple-implants and multiple anneals have become standard process steps for achieving high quality buried oxides. Thinning the silicon film and/or the buried oxide thickness would require lower doses and lower energies, which would degrade the quality of the buried oxide and the overlying silicon film. Moreover, as the SOI films are made thinner, the film thickness uniformity conditions become a lot more stringent. From the point of view of device performance, the current drive of the individual MOS transistors fabricated on SOI material are reduced as the film thickness is decreased, due to severely increased source/drain series resistance. It also becomes extremely difficult to adapt the salicide technology (which lowers series resistances in bulk MOSFETs) to such thin films. It is therefore clearly advantageous to use a dual-gated device fabricated in thicker SOI films to control short-channel effects, while simultaneously avoiding the deleterious effects of ultra-thin films.

The role played by the buried oxide thickness in dictating the properties of SOI MOSFETs were detailed in the previous chapter. In this regard, selective epitaxy techniques play a crucial part. Selective epitaxy techniques such as Epitaxial Lateral Overgrowth (ELO) and Confined Lateral Selective Epitaxial Growth (CLSEG) can be

used to form extremely high quality thin-film SOI regions. The buried oxide design is independent of the thickness and material quality of the overlying SOI region. Therefore, if the thickness of the buried oxide were to be changed (to prevent short channel effects, for example), it could be easily accomplished using selective epitaxy. SIMOX on the other hand would require an extensive development of new implant profiles in terms of both the implant energy and implant dose, to achieve the desired buried oxide thickness. This change in the SIMOX implant parameters would affect not only the buried insulator thickness and quality, but would also affect the quality of the overlying silicon-on-insulator film. The flexibility afforded by the selective epitaxy techniques in this regard can be harnessed into the design of novel devices such as the dual-gated SOI MOS Field Effect Transistor.

A novel process to fabricate a fully self-aligned dual-gated SOI MOSFET utilizing selective epitaxy was presented in Chapter 3. This process can be easily modified to yield a variety of related SOI-MOS structures, two of which are shown in fig. 4.1. The device in fig. 4.1(a) is exactly similar to a dual-gated structure, with the exception of the individually accessible back gate. The thin-oxide uncler the channel region is self-aligned to the top gate to minimize the drain/source-substrate overlap capacitance. The purpose of the thin oxide under the channel is of course to provide adequate short-channel immunity. The device sketched in fig. 4.1(b) is a quasi-SO1 MOSFET. In this device, the source/drain regions are fabricated on SOI material whereas the channel exists in the bulk substrate material. The source/drain regions must be self-aligned to the channel region to minimize parasitic capacitances. Since the channel region is formed in the bulk substrate silicon, unwanted effects i:n thin-film SOl transistors such as premature device breakdown and floating body effects are avoided. Such a quasi-SO1 design would not only yield high performance MOSFETs that can be formed in like manner as a conventional MOSFET, but would also yield devices with minimum parasitic elements for optimum speed performance. Finally, the process could also be used to fabricate quasi-SOI, dual-gated and regular SOI MOSFETs in the same process flow, as a majority of the process steps required by the three device structures are the same. In this work, the feasibility of using selective epitaxy techniques such as ELO and CLSEG to form thin-film fully-depleted dual-gated and single-gated SOI MOSFETs has been investigated. The feasibility study includes fabricating a variety of devices on

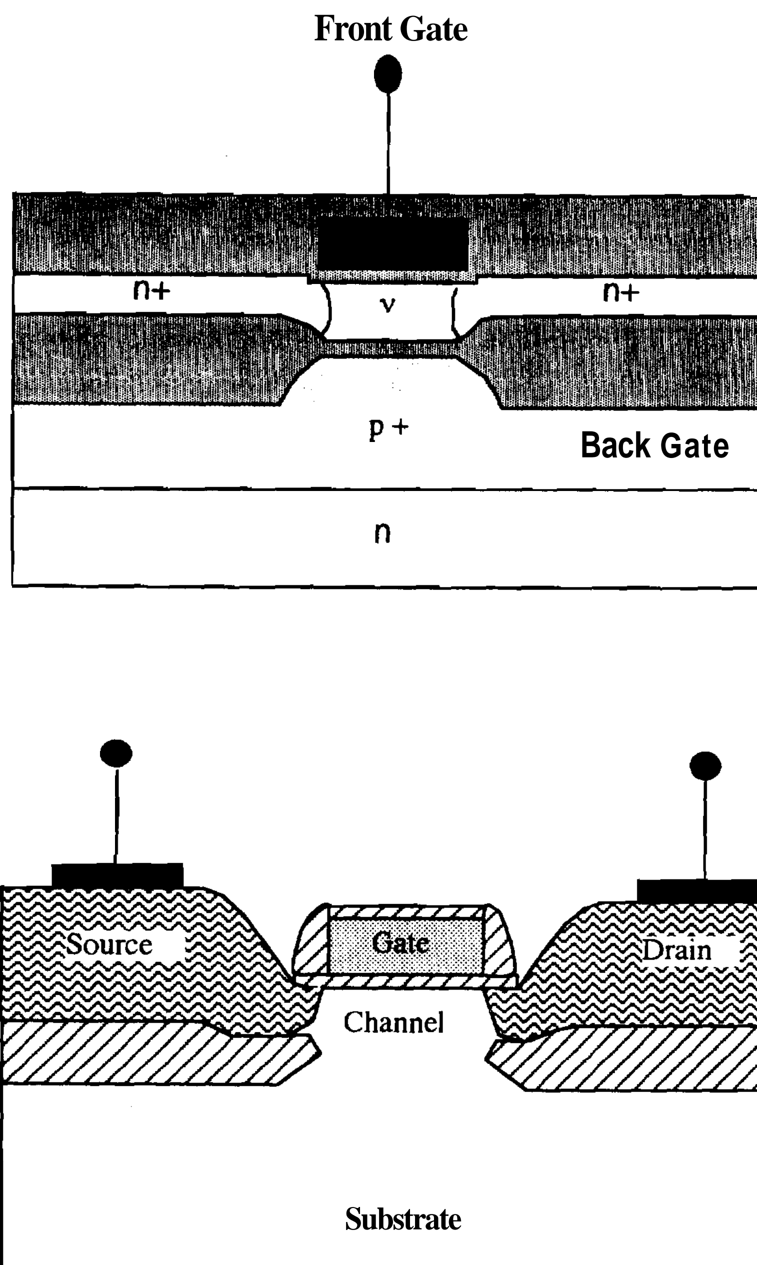


Figure 4.1 Different SOI-MOS structures that can be fabricated with slight modifications to the fully self-aligned dual-gated process

different starting material[1] and comparing their dc device parameters. To this end, a simplified process flow to fabricate the dual-gated device was pursued. The simplified process , while not self-aligned, would yield material similar in quality to that achieved by the fully self-aligned process. The only difference between the two processes is the additional epitaxy step (that involves growth from a vertical seed hole) in the self-aligned process.

Vertical seeded selective epitaxial growth has been successfully fabricated in parallel projects by Siekkinen [1] and Subramanian [2]. Some of these results are presented in section 4.1 as satisfactory feasibility indicators. In section 4.2, the simplified process flow is described and the development of some of the key steps in this process are detailed. Section 4.3 finally summarizes the important aspects of the chapter.

4.1 A Structural Study of the Fully Self-Aligned Dual-Gated MOSFET

The motivation for fabricating dual-gated MOSFETs and the process flow for fabricating the self-aligned dual-gated device was presented in Chapter 3. The first step in the process involves growth over a recessed polysilicon gate. Growth over the recessed gate is similar to growth over a planar oxide surface. This growth is fairly routine and consistently yields very good material. SEM cross-sectional micrographs of ELO and CLSEG grown over a planar oxide surface are illustrated later in this chapter. Once the ELO and/or CLSEG growth is planarized, the top gate definition over the bottom gate is easily accomplished. The most crucial step in the process is the formation of silicon nitride sidewall spacers for selective oxidation. Silicon nitride is typically deposited by Low Pressure Chemical Vapor Deposition (LPCVD). The capability for the LPCVD deposition of silicon nitride was not available at Purdue University and had to be developed during the course of this work. Initial depositions were carried out using silane (SiH_4) and ammonia (NH_3). Silane was used primarily to avoid the degradation of the vacuum pump oil caused by Di-chloro-silane (SiH_2Cl_2). However due to inappropriate mass transfer effects, all nitride depositions using silane yielded extremely

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[1] In chapter 5, results from device measurements on substrate bulk silicon, SIMOX, ELO and CLSEG will be presented.

non-uniform nitride layers. The wafers routinely exhibited a 'bulls-eye' effect due to varying layer thicknesses in the radial direction. Significantly better results were obtained using DCS and the growth uniformity across the 3inch wafer improved to within 5%. Typical deposition parameters used in this work were - T=800°C, Pressure=442mTorr, DCS flow rate=40sccm, NH3 flow rate=160sccm. It is important to note that best uniformities for the deposited nitride layers were obtained for depositions below 500mTorr.

The next step was to detennine a good dry etch profile so as to be able to form a sidewall spacer. Fr115 was typically used to etch both oxide and silicon in the DRIE 100 Drytech RIE system. A first attempt at etching Si_3N_4 was therefore attempted using Fr115. The etch rate was extremely low (50Å/min) and the profile was far from vertical. SF_6, however, yielded an extremely vertical profile and moreover, had an etch rate close to 500Å/min. SF_6 was therefore chosen as the etch gas for all subsequent nitride etches. Table 4.1 lists the typical etch rates for the various material in SF_6 and Fr115. It is

Table 4.1 Etch Rates of Silicon, Oxide and Nitride in Fr115 and SF_6

Material to be etched	Etch Gas	Etch Rate
Silicon	Fr 115	350 Å/min
	SF_6	1- 1.5 μm/min
Oxide	Fr 115	90 Å/min
	SF_6	85 Å/min
Silicon Nitride	Fr 115	50 Å/min
	SF_6	500 Å/min

readily seen that oxide has the slowest etch rate in both gases and is therefore a good etch-stop when etching polysilicon or silicon with Fr115 or when etching nitride with SF_6. In the above process, oxide and polysilicon layers alternate and it consequently becomes easy to the control the etch and discriminate between the different layer being etched. The nitride spacer formed using SF_6 is shown in fig. 4.2(a).

Finally, in order to mimic the dual-gated structure, a silicon substrate was oxidized and alternate layers of poly and oxide were deposited to represent the bottom gate, the bottom gate oxide, the SOI film, the top gate oxide and the top gate, respectively. The top gate polysilicon layer was oxidized and finally a 3000Å thick nitride layer was deposited. The top gate mask pattern was lithographically defined and the nitride, oxide and top gate polysilicon layers were sequentially etched using SF_6 and Fr115, respectively. Etching was terminated at the top gate oxide. After stripping the resist, the poly gate sidewall was oxidized and subsequently etching in Fr115 was continued till the bottom gate oxide was reached. Nitride was then deposited and SF_6 was used to form the nitride spacer. The SEM cross-section at this stage is shown in fig. 4.2(b). Further processing to attain the dual-gated structure would consist of merely etching the stack down to the bottom oxide using Fr115, oxidizing the exposed sidewall of the bottom gate poly and removing the nitride sidewall spacer. Once the nitride is removed the exposed SOI film sidewall would form a vertical seed for epitaxial growth. Both CLSEG and ELO growth from vertical seeds have been successfully accomplished and typical cross-sections of vertical seeded growth are shown in fig. 4.3. Thus, all the critical steps in the self-aligned process have been shown to be practicable:.

4.2 Simplified Process for the Dual-Gated SOI MOSFET

A major goal of this work was to fabricate thin-film fully-depleted dual-gated MOSFETs using epitaxial lateral overgrowth and confined lateral selective epitaxial growth. The structural feasibility study reported in the earlier section and other projects undertaken at Purdue using similar self-alignment principles proved that the proposed process would indeed yield the dual-gated device in a self-aligned manner. The main

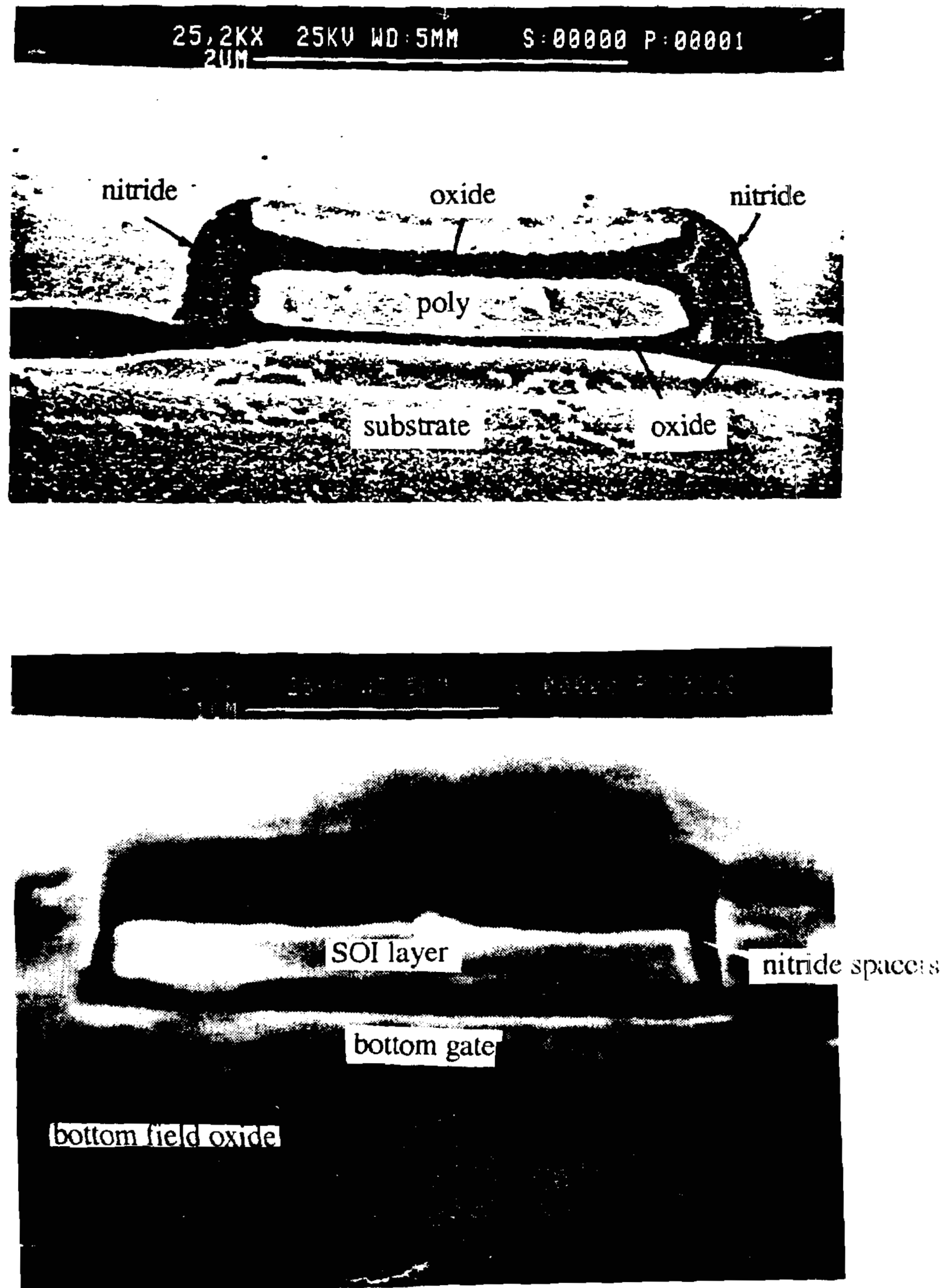
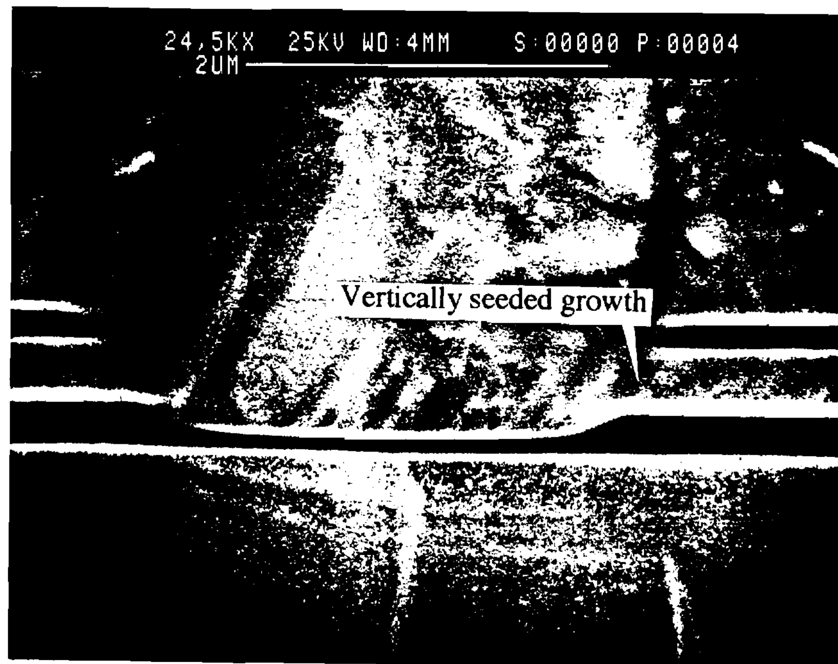
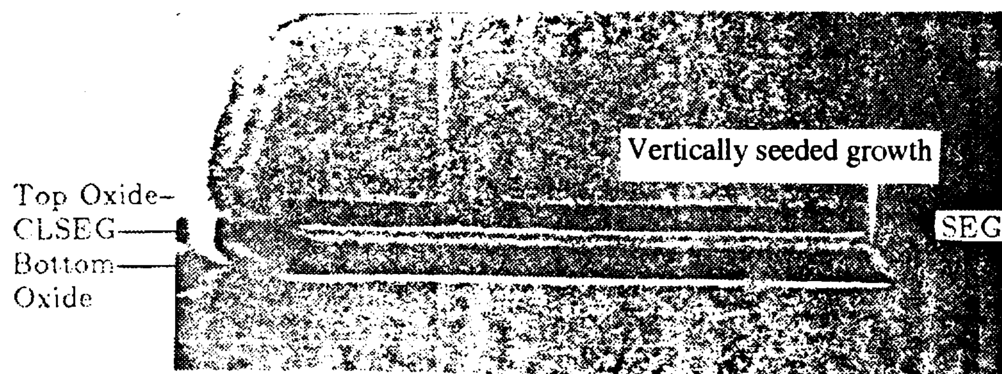


Figure 4.2 (a) SEM cross-section of nitride spacers on polysilicon gate sidewalls formed with SF_6 and (b) SEM cross-section showing feasibility of the self-aligned process. The figure shows nitride spacers formed on the gate stack, which is the essential part of the self-aligned process



(a)



(b)

Figure 4.3 Typical cross-sections of vertically seeded epitaxial growth using (a) ELO and (b) CLSEG

issue then was to study the quality of the SOI film formed during the first epitaxy step [2]. To this end, a simplified non-self-aligned process was developed. The front end processing that involves the formation of the SOI layer using either epitaxial lateral overgrowth(ELO) or confined lateral selective epitaxial growth (CLSEG) was schematically illustrated in figs. 3.27(a) and 3.27(b) in the previous chapter. The front end process used in the non-self-aligned process is essentially the same as outlined in fig. 3.27 with the exception that the bottom gate is not recessed. A detailed process description of the non-self-aligned process is given below. Process cross-sections for the front-end and back end process are provided in figs. 4.4(a)-4.4(c).

After the growth of a 0.2p.m bottom (field) oxide, the bottom gate polysilicon was deposited using the LPCVD system. Upon doping the polysilicon layer, the bottom gate was defined using MASK#1. Etching the bottom gate was carried out either with a wet ($HF:HNO_3:DI$) etch or a dry (Fr115) etch since the length of this gate did not determine the gate length of the dual-gated device. The bottom gate oxide was then grown. The seed hole was opened using MASK#2 and a wet BHF etch. The wafer is now ready for Epitaxial Lateral Overgrowth (ELO). When using Confined Lateral Selective Epitaxial Growth (CLSEG), the process continues with a brief oxidation to form a thin (150Å) oxide over the seed region followed by the cavity amorphous silicon deposition. The thickness of the amorphous silicon layer determines the final thickness of the SOI layer. The a-Si layer is then defined using MASK#3 and a thin 1200Å thermal oxide is grown over the sacrificial layer. The oxidation step converts the amorphous silicon layer into smooth grained polysilicon. A blanket LPCVD nitride is deposited at 800°C to a thickness of 0.3μm. Via holes are defined using MASK#4 and the nitride is etched in these regions using SF_6. The underlying oxide is also removed and the sacrificial layer is etched using a ethylenediamine-pyrocatechol-water mixture (EDP) at 90°C. The etch-rate is typically 1.5-2.0 μm/min. Once the polysilicon layer is completely etched away, the EDP is thoroughly washed out from inside the cavity. The thin oxide over the seed

[2] The first epitaxy step forms the channel region of the transistor. The second epitaxy step only forms the source/drain regions and could even be made of polysilicon without significantly affecting the device properties.

I. FRONT END PROCESSING (ELO)

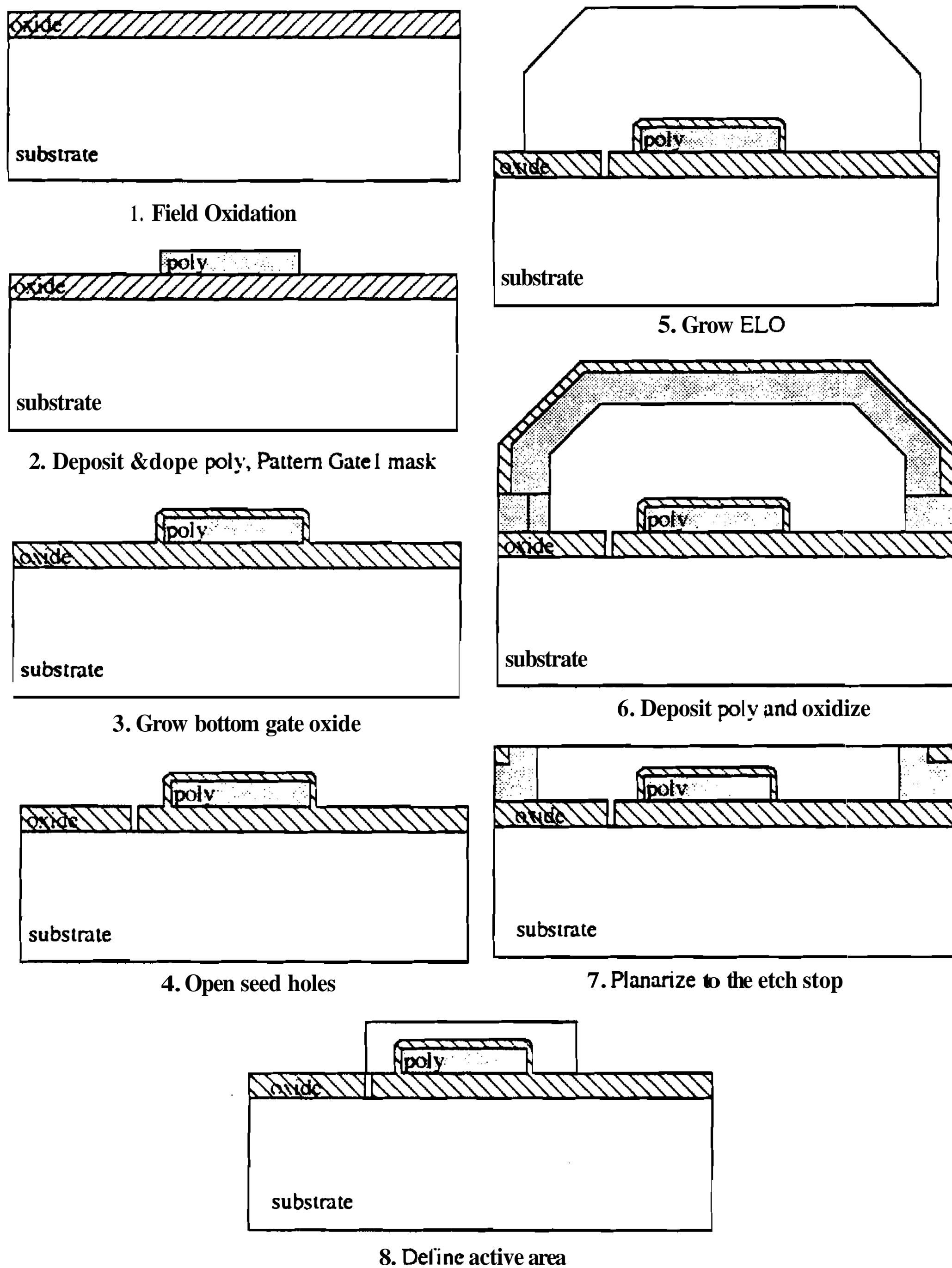


Figure 4.4 Cross-sections for the simplified non-self-aligned dual-gated MOSFET fabrication process (I) front end processing with ELO (II) front end processing with CLSEG and (III) common back end processing. Parts II III of the figure is continued on the following pages

II. Front End Processing (CLSEG)

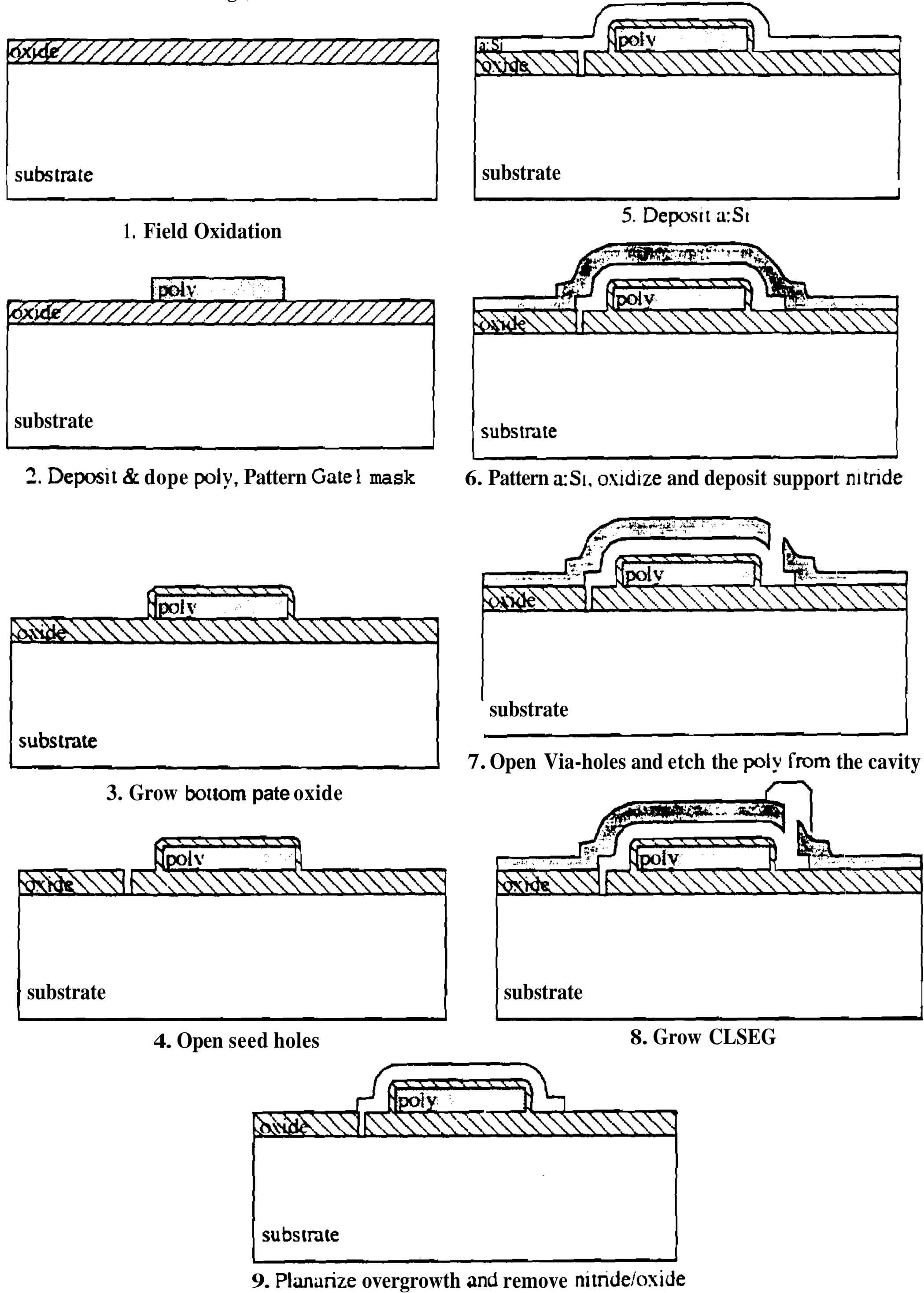
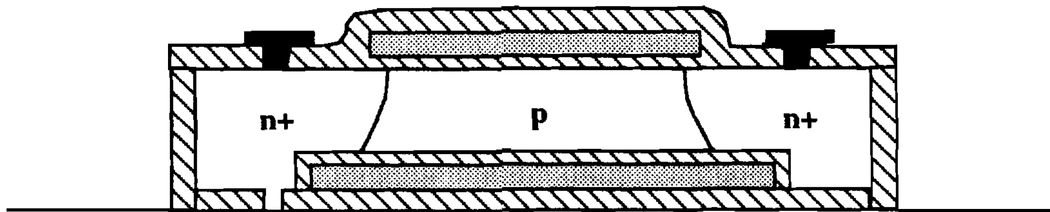


Figure 4.4, continued

USING ELO



Top gate oxidation
Top gate polysilicon deposition and definition
Source/Drain Implant
Drive-in, contact lithography and metallization

USING CLSEG

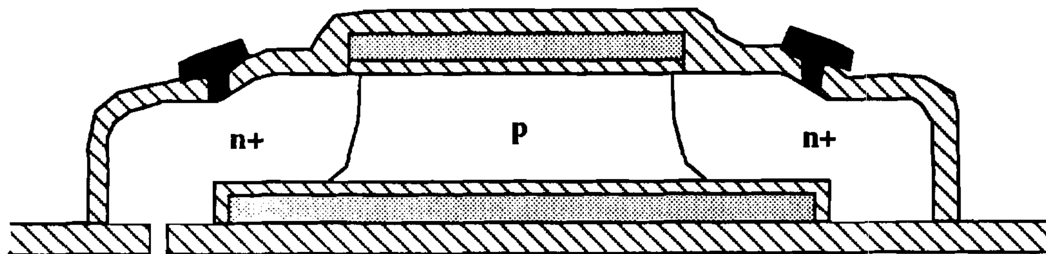


Figure 4.4, continued

region is etched in BHF. An ultra-sonic dip is used to get the BHF into the cavity[3]. After the conventional Piranha clean, both the ELO and CLSEG wafers are placed in the epitaxial reactor for selective epitaxial growth. Thc top view of as grown ELO and CLSEG after epi-growth is shown in fig. 4.5. The excess CLSEG growth emerging from the via in the CLSEG wafer is removed with chemical mechanical planarization and subsequently a hot phosphoric etch selectively removes the top cavity nitride layer. The ELO wafer is processed differently. A thin polysilicon layer is deposited and is oxidized to form an etch stop across the wafer. The thickness of the deposited polysilicon and the ply-oxide determines the thickness of the etch stop and therefore the thickness of the SOI film. The epitaxially grown silicon is planarized down to the etch stop. The poly oxide is then removed with a BHF dip and an active area mask (this is the same mask that defines the cavity layer on the CLSEG wafer) is defined. SF_6 is used to etch the excess polysilicon from the field and to mesa-isolate the ELO islands. At this stage, the ELO and CLSEG wafers are identical. The top gate oxide is then grown and polysilicon is deposited to form the top gate. The polysilicon is patterned using MASK#5 and the sourceldrain regions are implanted in a self-aligned manner. After the source/drain anneal, MASK#6 is defined to etch the contacts and MASK#7 is used to define the metal. The SEM cross-section of a finished dual-gated ELO MOSFET structure is shown in fig. 4.6. The details of the individual process steps are discussed below.

4.2.1 Bottom Gate Deposition and Doping

There are several key parameters associated with the bottom gate. The first of these is associated with the temperature of deposition. When polysilicon is deposited at the routinely used temperature (580°C-600°C), the grain size of the deposited material is large and the surface is consequently extremely rough. There are two reasons to try and obtain a smooth surface. Gate oxides grown on the rough poly surface typically have very low breakdown fields [3]. Regions with large topographical variations have extremely non-uniform local field distributions and field crowding occurs at isolated

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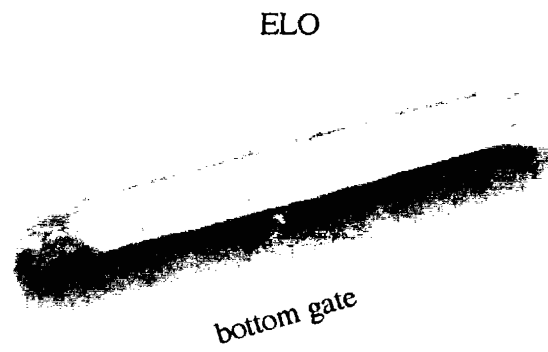
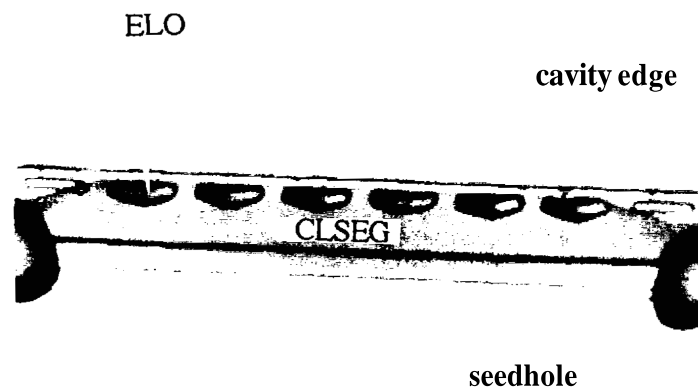
[3]The ultra-sonic dip at this stage is extremely important. If the ultra-sonic dip is omitted, the seed regions are incompletely etched and this results in poor CLSEG growth.

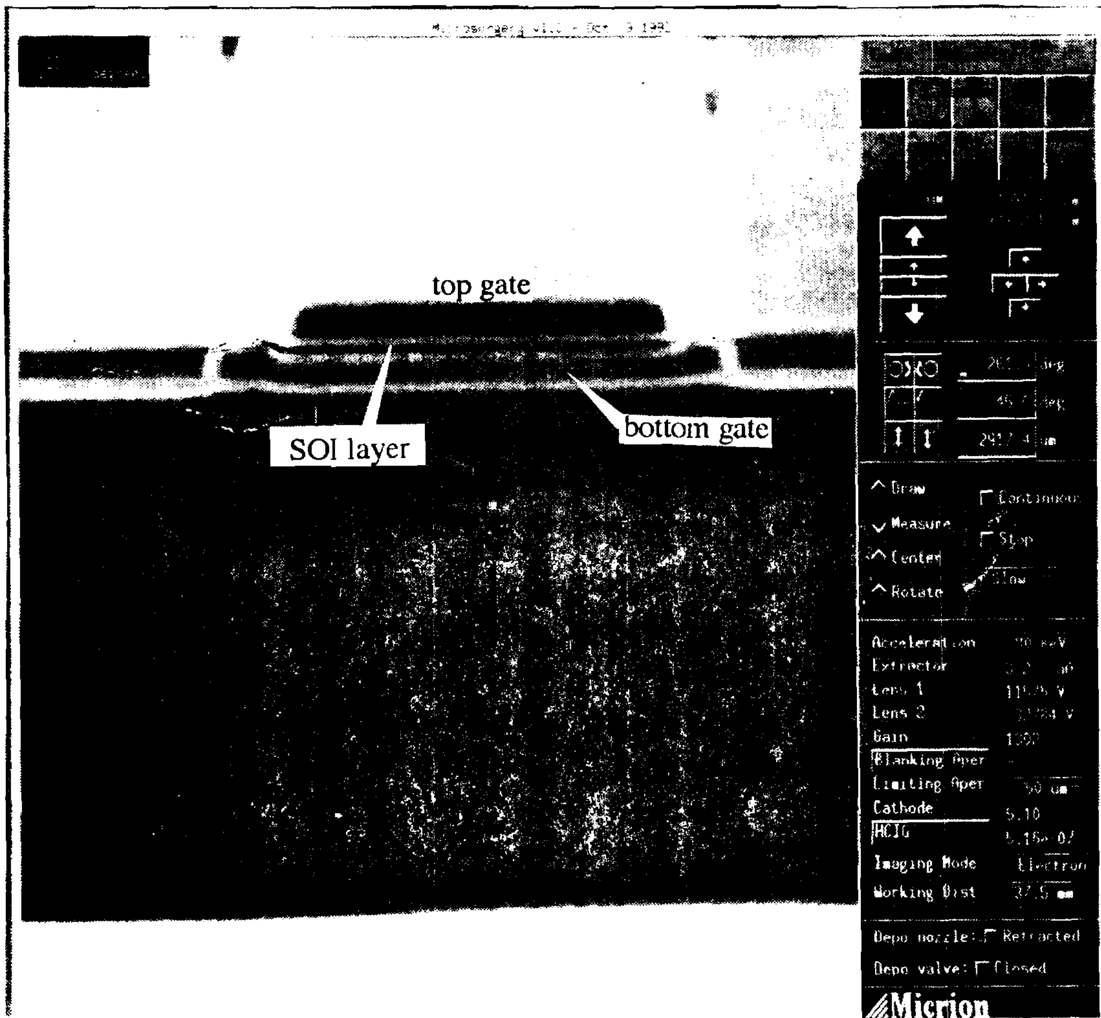


(a)



(b)

Figure 4.5 Top view photographs of as grown (a) ELO and (b) CLSEG



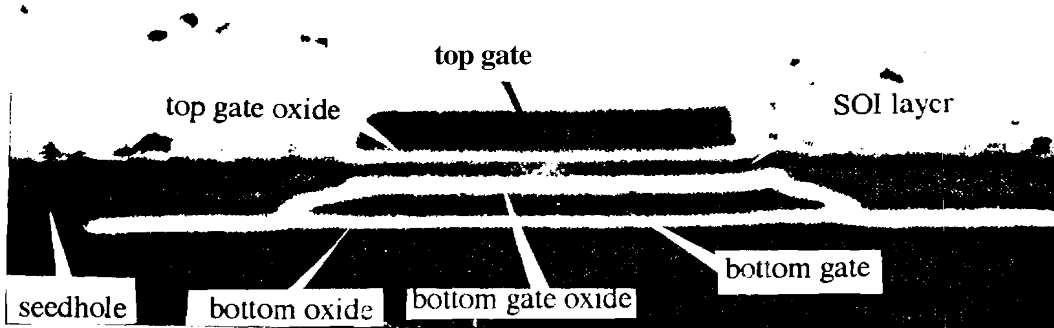
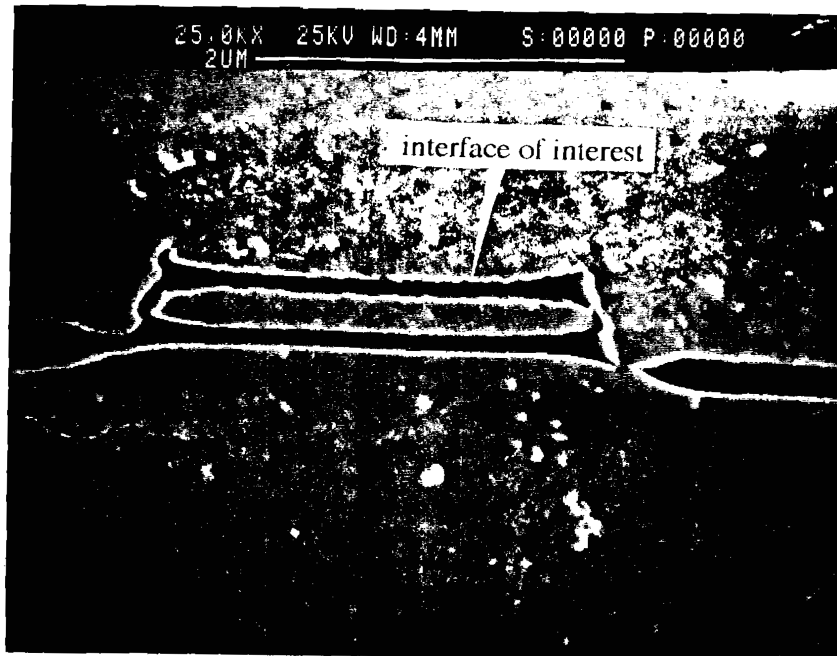


Figure 4.6 SEM cross-section of a finished duai-gated MOSFET structure fabricated using Epitaxial Lateral Overgrowth

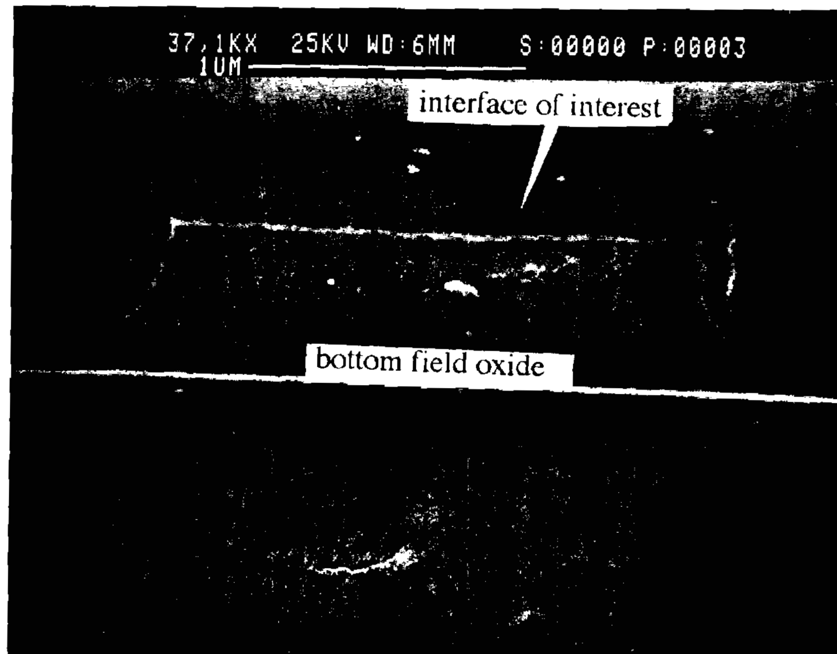
regions causing premature breakdown. Moreover, the ELO silicon must grow over this surface and the region above the bottom gate forms the all important channel region of the device. The rougher the surface of the bottom oxide, the greater the propensity for defect generation in the overlying epitaxial material. In order to obtain a smoother 'as deposited' surface, the deposition temperature was dropped to 550°C, so that the deposited material consisted of small grain amorphous silicon. At the low temperatures, the deposition was extremely specular with no visible structure even under Nomarski contrast microscopy. SEM cross-sectional micrographs of the polysilicon gate material are shown in fig. 4.7 for each of the two deposition temperatures. The difference in surface roughness is clearly discernible.

The choice between wet oxidation and dry oxidation to form the bottom gate oxide was a second factor related to the bottom polysilicon surface roughness. A dry oxidation would require a 1100°C, 50 min. thermal treatment for approximately a 1200Å thick oxide, whereas wet oxidation would involve a significantly smaller thermal budget (1000°C, 10mins.) for about 1500Å of oxide growth. Dry oxidation made the polysilicon surfaces a lot rougher than the wet oxidation, due to the higher temperature and longer times involved. Consequently, wet oxidation was chosen as the preferred mode of oxidation (especially since the oxide was thick) although the dry oxide would more than likely be a better quality oxide.

The second parameter related to bottom ply-gate deposition is the gate thickness. Initially, the polysilicon gate was deposited to a thickness of 4500Å, so that upon bottom gate oxidation, the ELO silicon encountered a step height of about 5000Å. It was found that a lot of defects were generated in the material when growing over this height. This is illustrated in fig. 4.8(a). The triangular shapes observed on the ELO edges are the edge dislocations. The majority of the dislocations are observed on the far edge of the gate. Growth from the seed region on the side that does not have the gate step shows a perfectly straight growth front with no visible defects even under Nomarski contrast microscopy. The edge defects do not propagate to the surface of the grown epitaxial film and become visible only after the ELO has been planarized down to less than a micron above the bottom gate surface as shown in the figure. When the polysilicon gate was made thinner (as deposited 2500Å), such that the total polysilicon thickness is 3000Å, the overgrowth typically showed no edge defects. A finished device picture in which the gate poly was thin is shown in fig. 4.8(b). No edge defects were observed in this case. In contrast, a similar device fabricated in dislocated material grown over a thicker

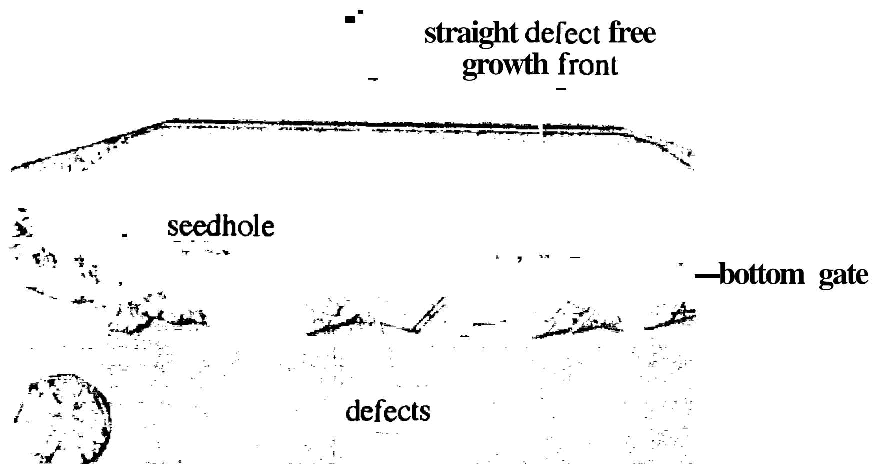


(a)

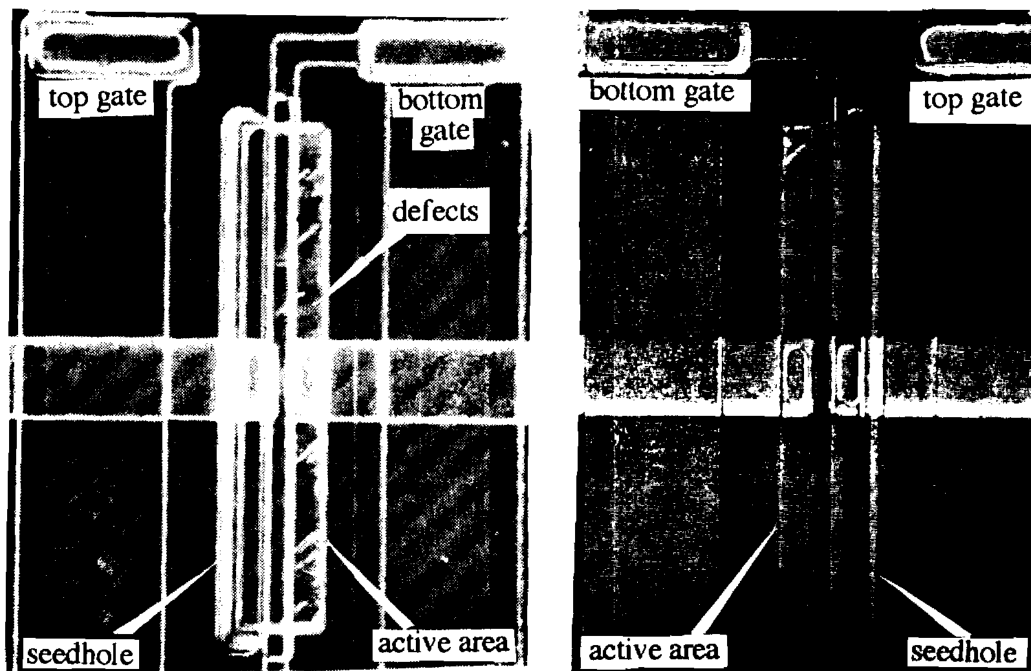


(b)

Figure 4.7 SEM cross-section of polysilicon surfaces deposited at (a) 580 °C and (b) 550 °C



(a)



(b)

Figure 4.8 Epitaxial Lateral Overgrowth over a polysilicon gate step. (a) step height is 5000Å and (b) finished devices with step heights of (i) 3000Å and (ii) 5000Å

polysilicon step is also shown alongside in fig. 4.8(b). In order to prevent or at least minimize these dislocations, it is imperative that the gate thickness be small. However, there is a certain minimum thickness that must be deposited in order to be able to make contact to it. This thickness is determined by the number of oxidation steps the bottom polysilicon gate contact runner sees (bottom gate oxidation, sacrificial top gate oxidation, top gate oxidation and finally sourceldrain oxidation). Heuristically, one arrives at 2500Å as the minimum allowable bottom poly thickness, so that one can reliable contact the poly and modulate the back interface. In light of the above discussion,,it is clear that if the bottom polysilicon gate were recessed, then this problem and the ensuing constraint on the bottom polysilicon gate thickness would not arisc. However wc did not forescc this problem at the time the masks were made and the bottom polysilicon gate mask (MASK#1) was 'light field' in nature. If this mask were used to form a recessed structure[4] one would have to use negative resist to form the trench. But the negative resist available at Purdue during this work, could not be used to define such narrow trenches (4.5μm) reliably and consistently, regardless of the combination of spin speed, exposure time, intensity or develop time used in the lithography process. The problem with not being able to recess the bottom gate is revisited when discussing chemical-mechanical-planarization (CMP) associated with CLSEG.

In order to contact the polysilicon it is necessary to dope it. Either n-type or p-type doping could be used. The dopant choices are phosphorus, arsenic and boron. The diffusion coefficients of phosphorus and boron are very high and these species are therefore not used to dope the bottom gate in this work. The bottom polysilicon gate was initially doped using an arsenic implant. The polysilicon was first deposited over the bottom oxide and a blanket implant was utilized to dope the entire layer. Subsequently, the polysilicon was lithographically defined to form the bottom gate. The CLSEG process requires the deposition of an a-Si layer after gate patterning and seedhole definition. It was found that each time the gate was doped using an arsenic implant, the subsequent a-Si layer appeared extremely spotty and rough. The amorphous layer appeared rough only in regions where the bottom poly was etched away (i.e.. over the

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[4]In order to form a recessed structure, a 4000Å deep trench is cut into a thick field oxide region. The trench is then filled with approxiamately 5000Å of polysilicon and the excess polysilicon on the field region is planarized using chemical mechanical planarization.

field oxide regions). Regions of deposited a-Si appearing over either the bottom gale or over the seedhole were however extremely smooth and showed no rough spots. This eliminates the deposition temperature as the probable cause. The same phenomena was true even with the subsequently deposited nitride layer which is deposited for cavity support. This is shown in fig. 4.9 which depicts a CLSEG wafer with an extremely spotted surface. The spotted or rough regions often acted as nucleation sites during selective epitaxy growth. It is important to reiterate that this unexplained phenomena occurred only in wafer that were implanted with arsenic. Unimplanted wafers which were otherwise identical were introduced into the LPCVD furnace at the same time as the implanted wafers, and they had extremely smooth and specular a-Si layers. The bottom gate was therefore doped using an arsenic-spin-on-dopant, to avoid any potential implantation damage caused by an arsenic implant. We do not understand this behavior at all, because Zingg et *al*. [4] in their work also used an arsenic implant and did not report any significant problems. But, we encountered this problem only on depositing an a-Si layer after the implant, a situation not encountered in reference [4]. The details of the arsenic spin-on-dopant process are presented in the process run-sheet in Appendix A.

4.2.2 Chemical Mechanical Planarization

Chemical mechanical planarization (CMP) is an essential part of the ELO process as it determines the final thickness of the SOI film. CMP was addecl to the CLSEG process to remove the excess growth coming out of the via holes as seen in fig. 4.6. Typically, CMP was performed on a Buehler grinder with a Rodel type Suba H-1 12" pad, with a polish pad speed of 150rpm. The head force was adjusted to 15 Ibs. force and the head rotation speed was fixed at 30rpm. The slurry used was a 15:1 mixture of DI water and colloidal silicon compound (NALCO 2350). The mechanism of chemical-mechanical-planarization (CMP) is as follows. Initially, only the epitaxially grown silicon is in contact with the pad and is rapidly etched through a combination of mechanical grinding and chemical etching. Once the silicon is etched down to the etch-slop (either oxide or nitride), the etching essentially stops because the area of silicon exposed is very small compared to the area of the etch-stop exposed.

In the ELO process, the chemical mechanical planarization step is carried out as shown in fig. 4.10. A thin layer of polysilicon is deposited and is subsequently oxidized

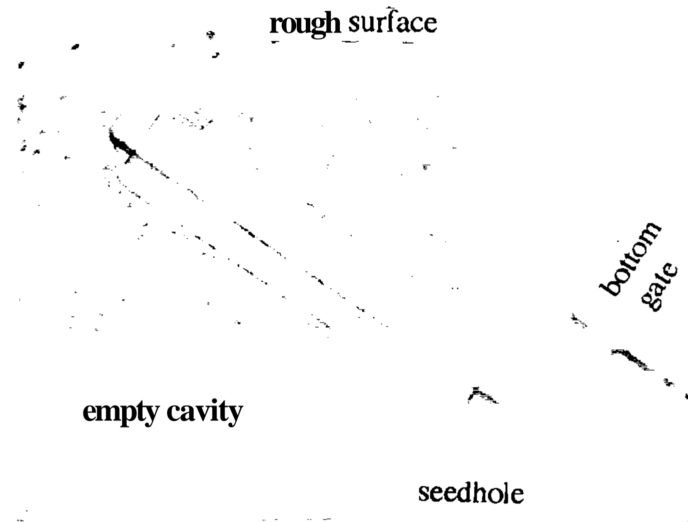

Figure 4.9 CLSEG wafer with an extremely spotted surface due to the bottom gate arsenic implant

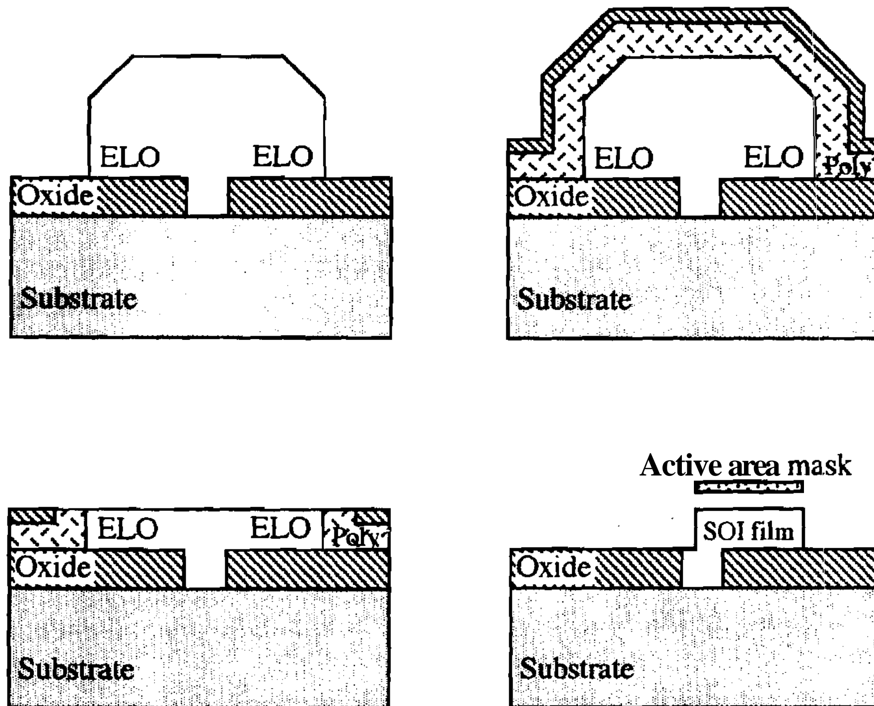

Figure 4.10 Chemical Mechanical Planarization process following epitaxial lateral overgrowth

to form approximately 2000Å of ply-oxide. The thickness of the etch stop above the field oxide was 5000Å. The thickness of the ELO above the bottom gate is then approximately 2000Å, which is sufficient for the fabrication of fully-depleted SOI MOSFET. A final 15 mins polish with NALCO 2355 was added to the planarization process in order to improve the surface smoothness of the ELO. As will be seen in Chapter 5, the subthreshold slopes on MOSFETs plananzed in NALCO 2350 alone were never as good as the device planarized with a finishing etch by NALCO 2355. Clearly, a single-gated device made at the same time as the dual-gated device would be a lot thicker (5000Å) and these device would be partially depleted. This is another reason for making recessed bottom gates - the single-gated devices and the dual-gated devices would have the same SOI film thickness.

The uniformity achieved by the chemical mechanical planarization process here at Purdue, was found to depend heavily on the density of the exposed silicon. Epitaxy runs which were completely devoid of any nucleation did not planarize very uniformly, due to an extremely small volume of silicon exposed across the wafer. On the other hand, extremely nucleated runs did not planarize at all. There was found to be an optimum degree of nucleation for which the planarization would be extremely uniform and yield highly uniform SOI films across the entire 3inch wafer (except possibly at the center). Thus the planarization process seems to depend on the mask design, which is in itself a major drawback to the CMP technique. Further work needs to be carried out to optimize the planarization process and a detailed investigation of other slumes needs to be carried out to improve the uniformity of the CMP process.

In the CLSEG process, chemical mechanical planarization is used to remove excess growth emerging from the vias as shown in the SEM cross-section of fig. 4.11. Contrary to what we expected prior to fabrication, this turned out to be the most difficult step of the CLSEG process. The chemical-mechanical -planarization step relies on the presence of a good etch-stop to iron out the non-uniformities across the wafer. In the dual-gated CLSEG devices (fig. 4.11) the excess growth from the vias often covered the bottom gate and had to be completely removed. If the silicon were not completely removed, then that region of the device would not receive any source/drain implant and in effect one could not use the structure to form the MOSFET. But the via holes were lower than the roof of the CLSEG cavity, which was raised up due to the presence of the bottom gate. Therefore, in the process of removing the excess silicon, the silicon over the bottom gate, which forms the channel of the device, was completely etched away. If the bottom

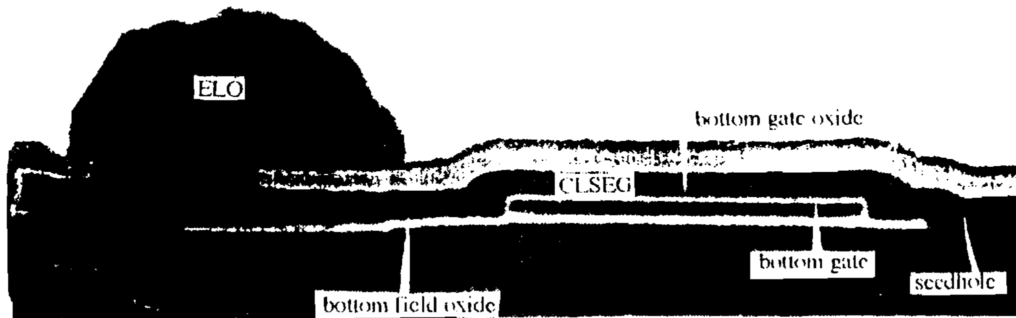

Figure 4.11 SEM cross-section of a dual-gated device after confined growth. The figure shows the epitaxial silicon emerging from the vias

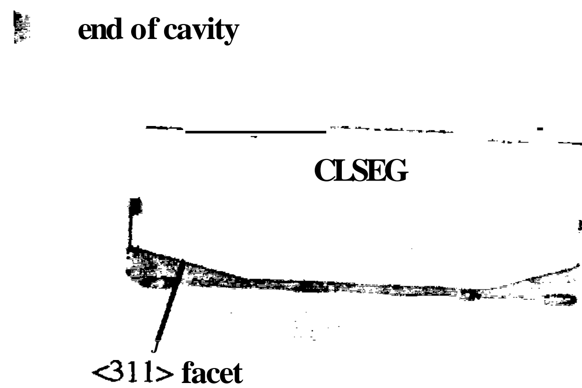

Figure 4.12 Top view photograph of a CLSEG island (single-gated devics) after the excess growth from the via is planarized and the supprot nitride is removed

gate were recessed the entire cavity would be at the same level and the cavities of the single gated and dual-gated devices would also have the same height. It would then be far easier to remove the excess growth. But since it was not possible to recess the gate, trial and error was the only available recourse to be able to obtain a viable dual-gated structure. As a result, very few working dual-gated CLSEG devices were found across the wafer. The devices, moreover, had varying silicon film thicknesses even across a single device, depending on the extent by which the overgrowth was planarized. These processing difficulties associated with the fabrication of the dual-gated CLSEG devices explain the results presented in Chapter 5. Nevertheless, the feasibility of utilizing CLSEG to form high quality thin film single-gated fully-depleted SOI MOSFETs was proven. The CLSEG islands of a single gated device after the excess planarization and the cavity nitride is removed is shown in fig. 4.12. Since dual-gatecl devices with recessed poly-gates would essentially have a planar surface for epi-growth, the results obtained on these single-gated devices can be extrapolated to prove the feasibility of thin-film dual-gated SOI MOSFETs with recessed bottom gates.

4.2.3 CLSEG Cavity Construction

In the first studies of CLSEG by Schubert et al. [5], silicon nitride/oxide was used as the top layer of the cavity for mechanical support and a-Si was used as the sacrificial layer material. The thermal oxide was 1000Å thick and the nitride was 1500Å thick. However, with this combination, the maximum cavity length that could be reliably fabricated was restricted to 8µm. MOSFET designs based on a very stringent alignment tolerance of 1.0µm and using a minimum feature size of 2.5µm, required that the minimum cavity size for the dual-gated SOI MOSFET be approximately 17µm. Thus, the CLSEG cavity width had to be extended to fabricate the dual-gated and single-gated SOI MOSFETs. This was done by increasing the top layer nitride thickness to 3000Å. The maximum thickness of the nitride is determined by the stress cracking of the nitride film which occurs around 4000Å. As shown in fig. 4.13, a 3000Å thick nitride layer allowed the formation of cavity widths up to 24µm. No evidence of sagging is visible in

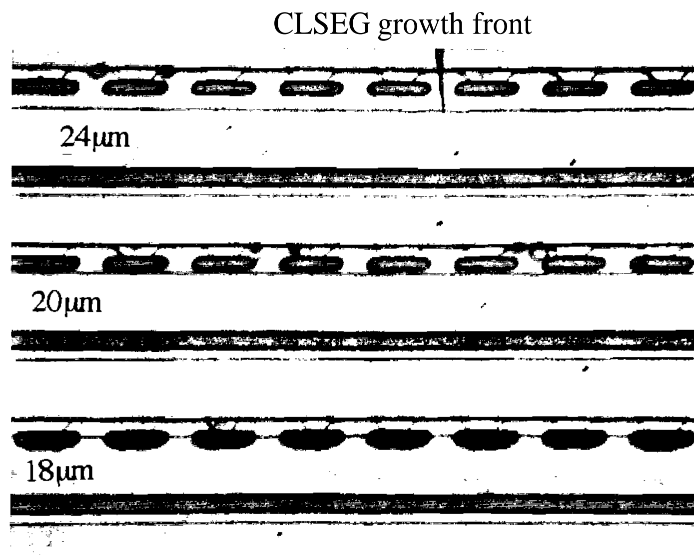

Figure 4.13 Top view photograph of CLSEG growth in a 24 μm cavity

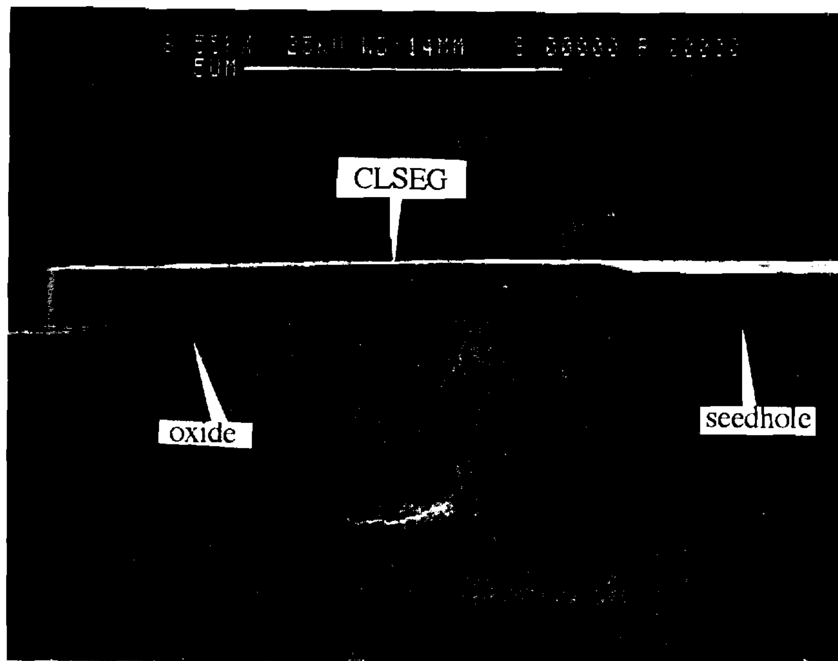

Figure 4.14 SEM cross-section of CLSEG grown in a 22 mm cavity. The figure shows no evidence of sagging

the figurc [5]. Based on the foregoing, the Lcp nitride layer thickness was chosen to be 300081. An SEM cross-section of CLSEG grown in a 22μm long cavity is shown if fig. 4.14. As can be seen in the figure, there is no evidence of sagging and the film is uniformly thick. This is especially important for thin-film SOI applications. Finally, the choice of the thicker nitride understandably raises concerns of stress dislocations being formed in the epitaxial material. TEM analysis of the as-grown CLSEG did not detect the presence of any defects in the material. A sample TEM picture is shown in fig. 4.15. The CLSEG film in this case was approximately 5000Å thick and the nitride layer was 320081. The figure shows no visible dislocations in the material, even along the top surface where we expect maximum thermal stress. It is important to reiterate that the sample examined by the TEM was a as-grown film and had its top nitride and oxide layers intact. This sample was not annealed after growth which could potentially heal the stress related defects.

4.2.4 Facets in ELO and CLSEG

A final note on the facets in Epitaxial Lateral Overgrowth and Confined Lateral Selective Epitaxial Growth is in order. In the earlier work on CLSEG, low angled end-facets were observed in the CLSEG material. The origin and cause of these facets was undetermined. A modified seed hole pattern was developed to investigate the end facets in CLSEG. The seed hole was extended out of the cavity as seen in fig. 4.16(a). Two distinct regions along the end of the cavity are clearly discernible. The first facet makes a 45° angle with the seed hole and this is the conventional <110> facet encountered during selective epitaxial growth of silicon. The second low angle facet is merely growth from the <110> facet and forms the <311> facet. The material quality of the growth from this facet is very bad as is visible in the Nomarski picture. However, this is not unique to the CLSEG process. A similar picture of ELO is shown in fig. 4.16(b). The ELO sample again shows the presence of the same two facets as the CLSEG material. They form exactly the same angles with the seed holes. Thus, contrary to what was believed earlier, CLSEG is no worse off than ELO in terms of end facets. The end facets in selective

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[5]Sagging in the CLSEG cavity is made obvious by the occurrence of diffraction rings of various colors.

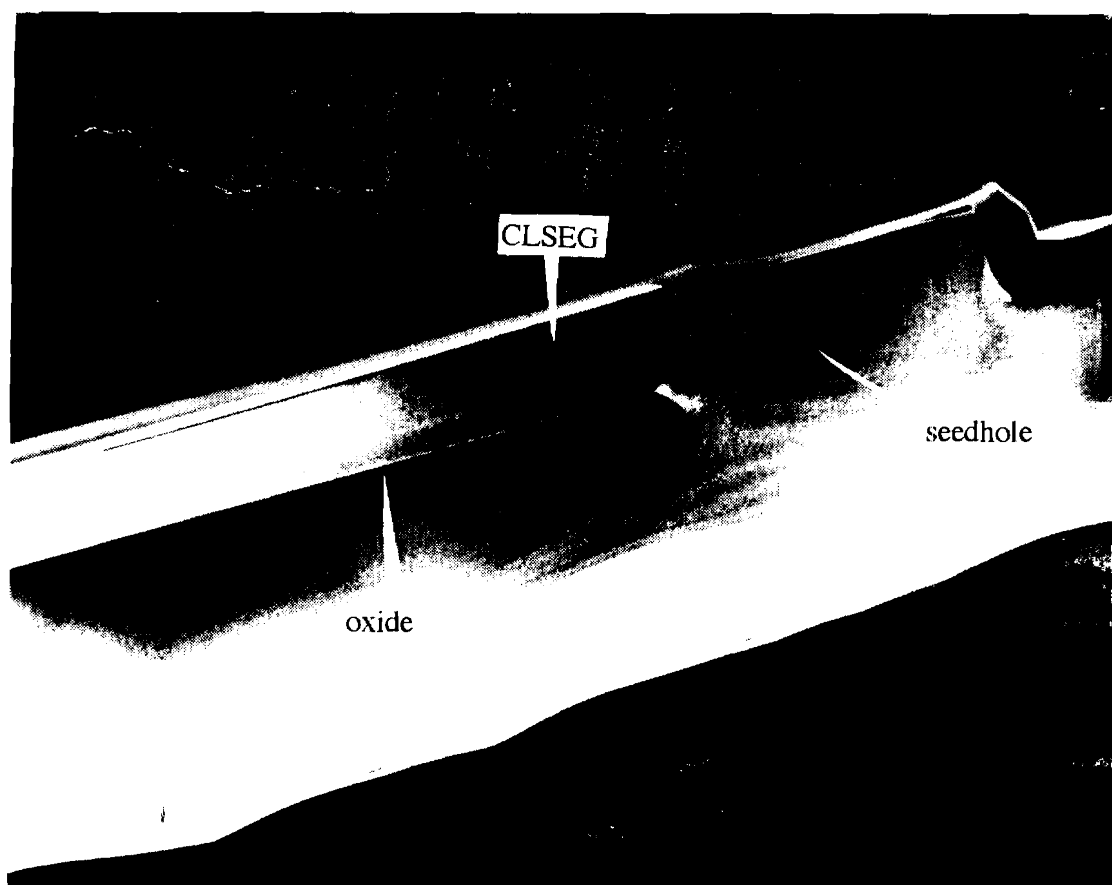
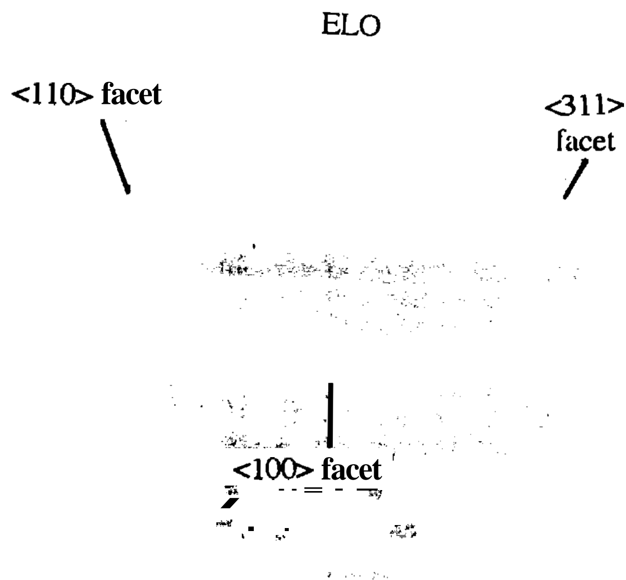
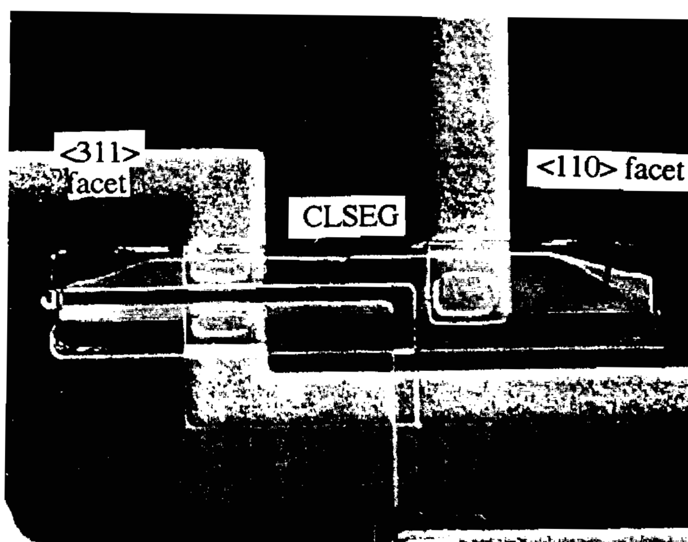


Figure 4.15 XTEM micrograph of CLSEG. The film thickness is 5000Å. No visible defects are observed anywhere in the CLSEG film



(a)



(b)

Figure 4.16 Top view photograph indicating the <311> and <110> facets in (a) ELO and (b) CLSEG

epitaxial growth is a major concern to the applications of the technology to SOI VLSI. In its defense however, the facets are an extremely predictable phenomena and therefore one can accurately position devices such that they do not intersect the poor quality material in the faceted regions. Alternately, the edges of the SOI regions grown by either ELO or CLSEG that show the <110> and the <311> facets (and the poor material between them), can be etched away using the active area mask as shown in fig. 5.41 in Chapter 5. The active area mask is used to isolate devices in any process, and therefore this step would not add any lithographic steps to the process.

In all the devices fabricated in this work, the channel region intersected the faceted regions along the ends of the device. No detrimental performance limitations were observed. Since the material along the edges is of extremely poor quality, its mobility is expected to be extremely low. Hence, these regions of the device were not considered when computing the mobility in the SOI devices fabricated using ELO and CLSEG.

4.3 Summary

Deposition parameters and etch profiles for LPCVD nitride deposition and etching were investigated fro use as nitride spacers in the fully self-aligned dual-gated SOI MOSFET process. Structural feasibility of the device and process viability were proved upon successful fabrication of the nitride spacer for selective oxidation. A non-self-aligned process to fabricate the dual-gated MOSFET by ELO and. CLSEG was developed. The process requires only one epitaxy step compared to two in the self-aligned process. Since the material characteristics of the SOI film fabricated in the non-self-aligned manner is essentially the same as that produced by the fully self-aligned process, the simplified process was used for material characterization.

Experimental fabrication required several problems to be solved in order to attain dislocation free material. CLSEG cavity widths were extended to facilitate the fabrication of minimum geometry (2.5μm) transistors. This was done by increasing the top layer support nitride thickness to 3000Å. The problem associated with the chemical mechanical planarization of the overgrowth from the vias in the dual-gated CLSEG process could not be solved reliably. The quick and reliable way around the problem is to

fabricate recessed polysilicon bottom gates so that CLSEG growth is initiated over a planar oxide surface.

Crass-sectional Transmission Electron Microscopy (XTEM) was used to confirm the excellent quality of the as-grown CLSEG material. A new cavity seed hole design confirmed that the end facets in CLSEG were essentially the same as that in ELO and is not something intrinsic to the confined growth technique.

4.4 References

1. J.W. Siekkinen, "Self-Aligned Single Crystal Contacted High-Speed Silicon Bipolar Transistor utilizing Selective (SEG) and Confined Selective Epitaxial Growth (CLSEG)", *PhD. Dissertation,* Purdue University, 1991.

2. C. K. Subramanian and G.W. Neudeck, "Large area siliconon insulator by double-merged epitaxial lateral overgrowth", *J. Vac. Sci. Technol. B,* vol. 10 (2), pp. 643, 1992.

3. L. Faraone , R.D.Vibronek and J.T. McGinn, "Characterization of thermally oxidized n^+ polycrystalline silicon", *IEEE Trans. on Electron Devices,* ED-32 (3), pp. 577, 1985.

4. R.P.Zingg, B. Hofflinger and G.W. Neudeck, "Dual-Gate SOI CMOS 'Technology by Local Overgrowth (LOG),", *IEEE SOS/SOI Workshop Proc.,* pp. 134, 1989.

5. P.J. Schubert, "Study of a new silicon epitaxy technique : Confined Lateral Selective Epitaxial Growth", *PhD. Dissertation,* Purdue University, 1990.

CHAPTER 5
ELECTRICAL MEASUREMENTS

5.1 Introduction

In the previous chapter, the process development for the dual-gated SOI MOSFET was presented. The similarities and differences associated with Epitaxial Lateral Overgrowth (ELO) and Confined Lateral Selective Epitaxial Growth (CLSEG) processing were also highlighted. Some of the difficulties in fabricating dual-gated devices with a non-recessed bottom polysilicon gate were discussed, and it was established that a far simpler, reliable and planar process results if the bottom gate were recessed to be planar with the field oxide. In this chapter, the electrical characteristics of the dual-gated SOI MOSFET fabricated using both of the above selective epitaxy techniques are presented. This establishes the feasibility of fabricating thin-film fully-depleted dual-gated SOI MOSFETs. In addition to the dual-gated devices, single-gated devices (partially depleted and fully depleted) were also fabricated. The characteristics of these devices are compared to devices fabricated in the substrate material and to the devices fabricated in commercially available SIMOX wafers.

The main purpose of this chapter is to establish the feasibility of fabricating thin-film fully-depleted dual-gated SOI MOSFETs using Epitaxial Lateral Overgrowth and Confined Lateral Selective Epitaxial Growth. A secondary and probably more important purpose was to determine the properties of the epitaxial material through DC measurements on the fabricated devices. To this aim, devices were processed simultaneously (in the same process run) on SIMOX and ELO material and their effective mobilities were compared. Such a one is to one comparison is more: valid than a comparison of the properties of ELO and CLSEG devices with the effective mobility values of SIMOX reported in literature, because both sets of devices are subjected to the same non-optimal processing environment here at Purdue. As a prologue to the chapter, we enumerate some of the new and important results presented in the text. Thin-film fully

depleted SOI MOSFETs were fabricated on ELO material for the first time at Purdue University. Values of electron and hole mobilities obtained agree rather well with typical values in bulk silicon. The direct and systematic comparison between the properties of SIMOX and ELO was initiated for the first time. The study indicates that the ELO material is at least as good if not better than the commercial SIMOX material. The advantages of ELO and CLSEG over SIMOX is more pronounced due to the superior quality of the buried (bottom) oxide in the devices fabricated using selective epitaxy. Indeed. the leakage currents across the buried oxide in SIMOX were found to be at least two orders of magnitude greater than that in ELO and CLSEG, where the buried oxide is in fact a good quality thermal oxide. Finally, thin-film fully-depleted NMOS and PMOS field effect transistors were fabricated in ultra-thin film (2500Å) CLSEG layers for the first time. Again. the properties of the CLSEG films agree very well with those of both the ELO and substrate material. The remainder of the chapter is organized as follows. Section 5.2 details the fabrication processes utilized for fabricating the different devices. The comparison between the properties of ELO and SIMOX is presented in section 5.3. CLSEG results are described in section 5.4 and the conclusions are summarized in section 5.5.

5.2 Device Fabrication

NMOS and PMOS devices were fabricated on ELO, SIMOX, CLSEG and substrate material. All MOSFETs fabricated were self-aligned poly-silicon gate devices. Initial work began with the fabrication of NMOSFETs. SIMOX, ELO and CLSEG material were grown doped to about 1-5 x 10^{15} /cm^3 (n-type). Therefore, in order to convert the material to p-type, they all needed to be implanted with a low dose of boron. A typical dose of 1x10^{12} / cm^2 and an energy of 50 KeV was used to convert the doping type. In some cases the devices required a multiple implant comprised of a 5x10^{11}/cm^2, 25 kev and a 1x10^{12}/cm^2 , 100 kev implant. The deep heavier implant was necessary to compensate the n-type dopant out-diffusion from the back gate. Once the polysilicon gate material was deposited and defined, the source, drain and gate regions were implanted with As upto a dose of 5x10^{15}/ cm^2. The source/drain implants were then annealed at 1000 °C for 9 mins. in a wet ambient to grow approximately 1200Å of oxide.

The mask used in the work was designed to produce both substrate and SOI devices on the same die. The process employed a photoresist N^+ implant mask to ensure that the arsenic was introduced only in the n^+ regions. However, it was found during the course of this work (and independently by two other researchers working in the same area) that the use of a photo-resist mask during the implant caused an inexplicable increase in the leakage current of MOSFETs fabricated in the SOI material. The substrate devices fabricated on the same die also showed large amounts of' leakage currents. Very few devices were found across the wafer with low leakage currents and these devices had poor sub-threshold slopes. The strong inversion characteristics were normal however, and therefore values for the effective mobility could be still be obtained on all the devices.. Monitor substrate devices fabricated on a different wafer but at exactly the same time as the SOI devices showed excellent device characteristics. It is our conjecture that the type-conversion threshold adjust implant (especially the high energy 100KeV implant) not only affects the mobility but also degrades the surface properties of the material which in turn affects the sub-threshold characteristics. Before any further optimization of the NMOS process could be carried out, the arsenic gas source had run dry and consequently all subsequent devices fabricated vvere p-channel MOSFETs. It is still unclear as to why the sub threshold characteristics of the fabricated NMOS devices (whether it be off-state leakage currents or degraded inverse sub-threshold slopes) were so poor. But since the same behavior was observed on the ELO, SIMOX and CLSEG devices, the poor sub threshold charactenstics cannot. be considered a reflection of the material property.

The p-channel MOS field effect transistors were also fabricated in a self-aligned manner. In order to minimize process complexity and lithographic steps and in order to avoid the photoresist implant mask process, monitor substrate devices were fabricated on a separate wafer but at exactly the same time as the SOI devices. Boron sourceldrain regions were implanted at a dose of $5x10^{15}$ /cm^2 and an energy of 25KeV. The S/D regions unless otherwise mentioned were annealed in a wet ambient at 900 °C for 40 mins. This again grows about 1200Å of oxide.

Prior to gate oxidation, the oxidation furnaces were cleaned with TCA for half an hour at 1100 °C. The temperature was subsequently dropped to 1000 °C and the gate oxidation was carried out for 45 mins in dry O_2 without TCA. This yielded an average gate oxide thickness of 550Å on most wafers. The oxide thickness was measured using profilometric measurements on different regions of each wafer. Likewise, the SOI film

thickness was measured after planarization for the ELO devices and the CLSEG devices and an average thickness of 1400Å was determined for most of the fully depleted ELO devices discussed in this chapter. The CLSEG devices were fabricated in slightly thinner 1200Å SOI layers. The SIMOX wafers were 1700-1800Å thick prior to processing. However, after the sacrificial layer oxidation and gate oxidation, its thickness reduced to 1400Å.

The drawn gate length on the mask was 2.5μm, but the gate length actually defined on the wafer was almost always closer to 3.0μm. This is a result of the pre-bake temperature and time and the exposure and develop time in the lithographic sequence, which was not optimized for the smaller geometries. Although the polysilicon gates were defined with a reactive ion etch, the wafers were always postbaked after exposure and develop at 120 °C for 20 mins prior to etching. Postbaking could cause the resist to flow, thereby increasing the defined gate length. No procedural changes were made on this account however, because this was not considered a serious problem.

Finally, all device measurements were made using a HP 4145B semiconductor parameter analyzer and the individual devices were interrogated using a micro-manipulator probe station. The devices were placed in the dark and with a steady stream of nitrogen flowing across it, to prevent anomalous leakage currents due to humidity concerns.

5.3 Epitaxial Lateral Overgrowth, SIMOX and Substrate Devices

In this section, the electrical data obtained on NMOS and PMOS devices fabricated in substrate silicon and those fabricated in SOI material (ELO and SIMOX) are presented. The NMOS device data are presented primarily to provide the effective mobility ($\mu_{n,eff}$) values for the ELO material and compare them to the values in the substrate and SIMOX material. The subthreshold characteristics of these devices were by and large very poor, due to excessive leakage currents in the devices. The PMOS device data are more ideal and a detailed look at the dual-gated device operation is provided only for the p-channel MOS field effect transistors.

5.3.1 N-channel MOS Transistors

Figures 5.1 to 5.3 show the output characteristics, the sub-threshold characteristics and the transconductance curves of a typical substrate NMOS device. Very low values of leakage currents were obtained for the source and drain junctions as evidenced by the extremely low subthreshold leakage currents. Very good inverse subthreshold slopes of around 93mV/dec were obtained on most devices. This indicates good gate oxide interface properties and emphasizes the low leakage observed in-the devices. Table 5.1 summarizes the parametric values of the baseline substrate NMOS device where all values have been averaged over at least 25 devices across the wafer. The effective

Table 5.1 Summary of Measured Data from Substrate NMOS Devices. Averages are taken over 25 devices. $L=2.6\mu m$, $t_{ox,f}=450Å$

Parameter	Average Value
$I_{D,sat}$: $V_D=V_G=4.0V$	$7.6x10^{-5}$ A/µm
S	93.2 mV/dec
Leakage	14 pA
V_T	0.28V
G_m @ $V_D=0.1V$	2.0 µS/µm
$\mu_{n,eff}$	574 cm^2/V-sec

mobility in the substrate silicon wafer was determined from the measured drain conductance (with the device biased in the linear region) to be on an average 574 cm^2/V-sec. Typical values in bulk silicon range from 600-650 cm^2/V-sec for doping concentrations in the $1x10^{16}$ /cm^3 range. This is a reasonable value for the electron mobility in bulk silicon, considering that series resistance effects have not been taken into account. A single gate length of 2.5 µm (which is also the minimum feature size) was

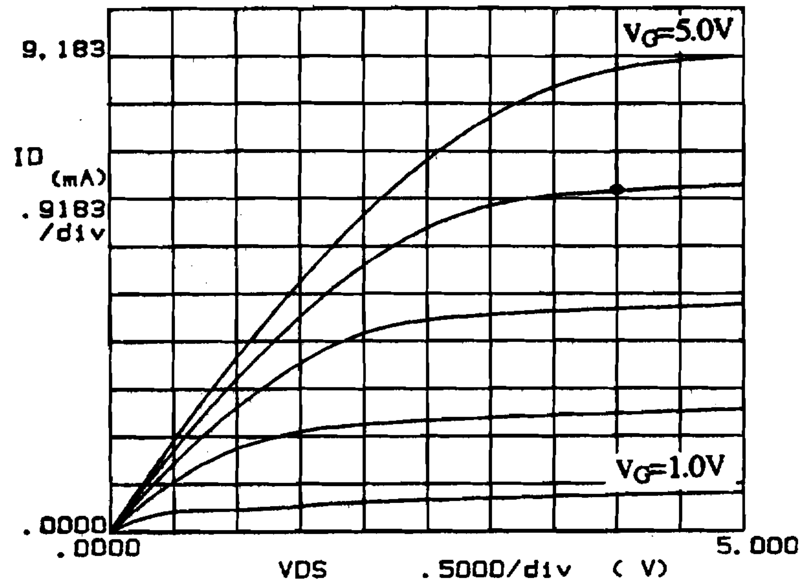


Figure 5.1 Output characteristics for a typical Substrate NMOS device

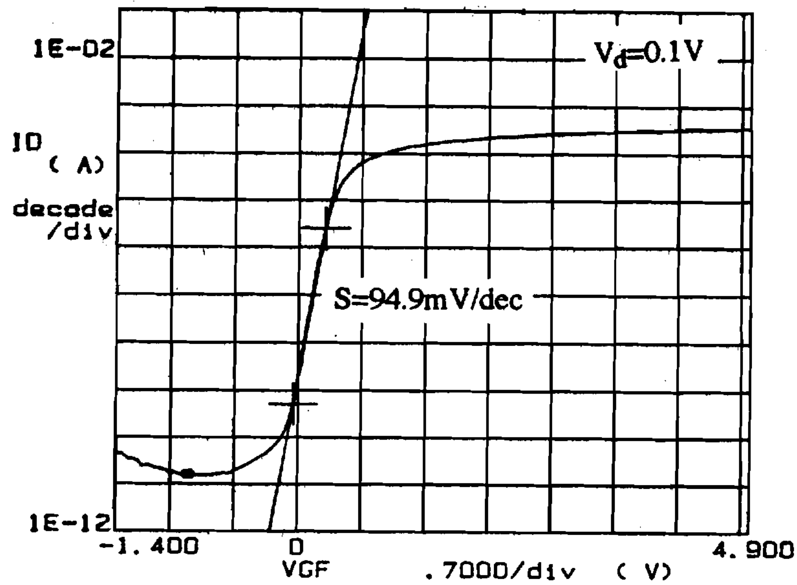


Figure 5.2 Subthreshold characteristics for the Substrate NMOS device

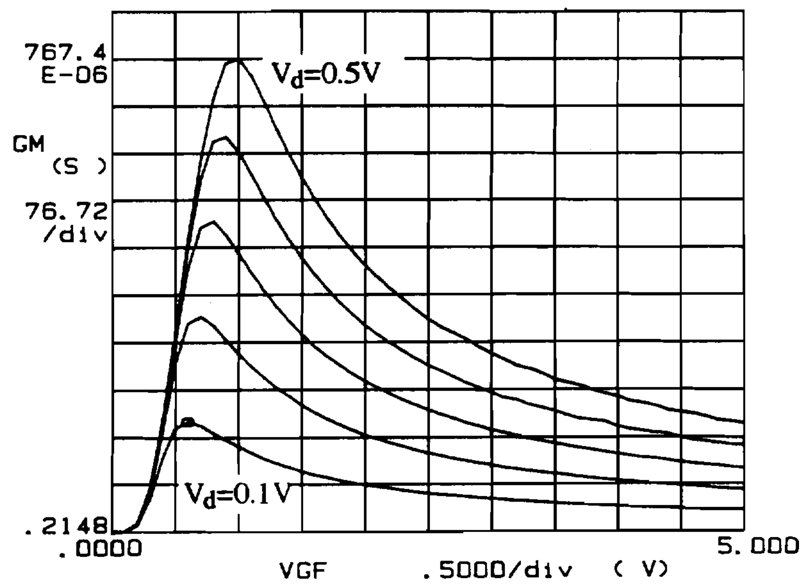


Figure 5.3 **Transconductance curves for the Substrate NMOS device for different drain voltages**

designed for all devices fabricated, in order to minimize the lateral extent of epitaxial silicon growth and hence the growth time. Typical series resistance estimation techniques require devices with a single width but with varying gate lengths - a luxury not afforded in the working mask set. As a result, estimation of the series resistance became impossible and it was consequently difficult to correct for it when computing the effective mobility. Problems associated with the series resistance will be discussed in greater detail, later in the chapter.

Figures 5.4 through 5.6 are illustrations of DC measurements for the output characteristics, sub-threshold slope and transconductance of a NMOS device fabricated on a SIMOX wafer. The summary of measured data from the SIMOX devices are presented in Table 5.2. The average subthreshold slope is rather large (351mV/dec)

Table 5.2 Summary of Measured Data from SIMOX NMOS Devices. Averages are taken over 25 devices. $L=2.6\mu m$, $t_{ox,f}=550Å$

Parameter	Average Value	Best Value
$I_{D,sat}$: $V_D=V_G=5.0V$	4.7×10^{-5} A/µm	5.3×10^{-5} A/µm
S	351 mV/dec	326 mV/dec
Leakage	100nA-10µA	100nA
V_T	1.27	-
G_m @ $V_D=0.1V$	1.0 µS/µm	1.15 µS/µm
$\mu_{n,eff}$	413	476
BV_{DS} @ $V_G=0V$	8.8V	8.9V

compared to the value obtained in the substrate device. Although the device in fig. 5.5 shows very low subthreshold leakage currents, this was more the exception than the rule.

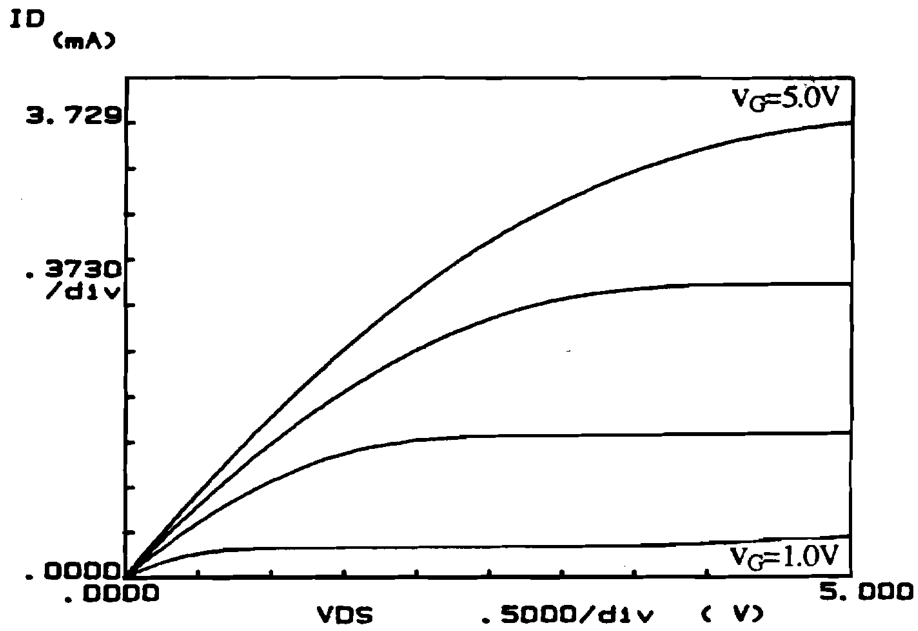


Figure 5.4 Output characteristics for the SIMOX NMOS transistor

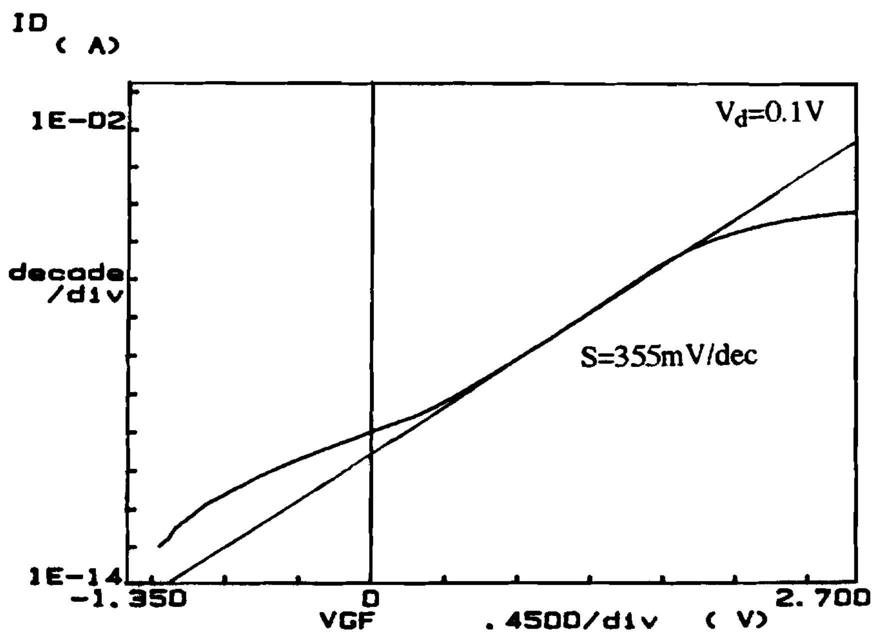


Figure 5.5 Subthreshold characteristics for the SIMOX NMOS transistor demonstrating low leakage currents

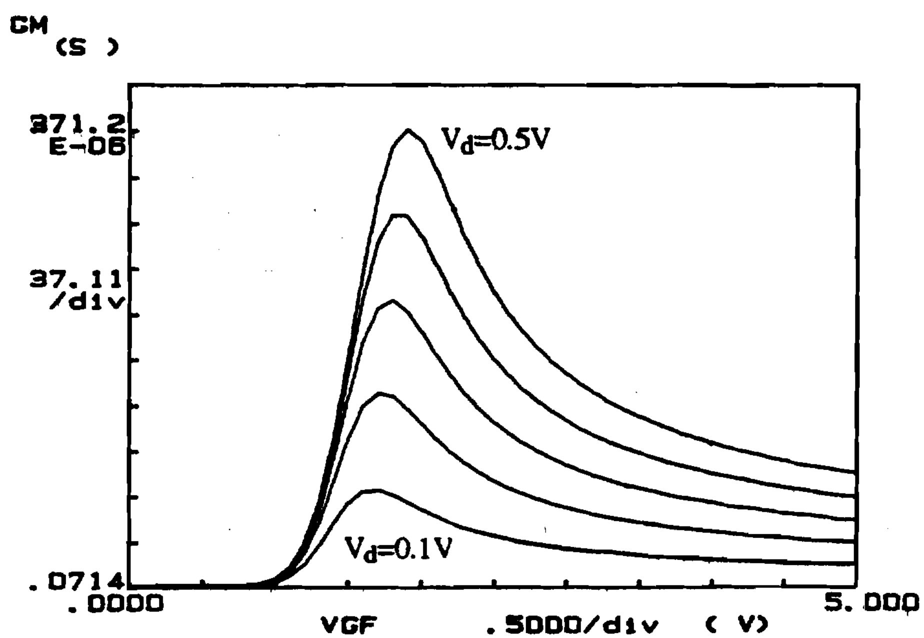


Figure 5.6 Transconductance curves for the SIMOX NMOS transistor for different drain voltages

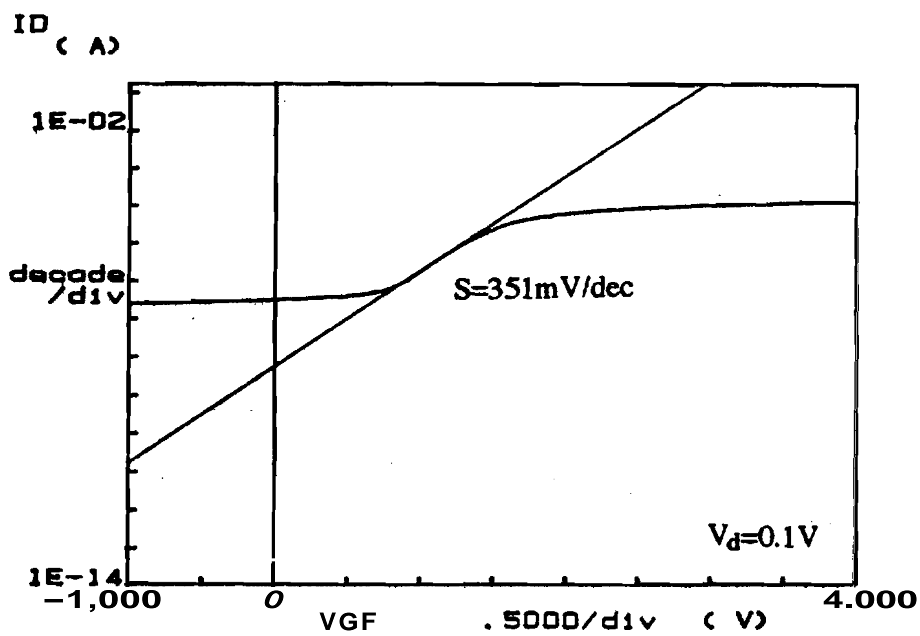


Figure 5.7 Subthreshold characteristics for the SIMOX NMOS transistor with excessive subthreshold leakage currents

Most fabricated devices showed excessive sub-threshold leakage currents as that shown in fig. 5.7. As explained in the previous section, the source of this lealkage is still unexplained. A more detailed explanation of the apparently poor subthreshold characteristic will be provided after the data for the ELO devices have been presented. The average mobility obtained on the SIMOX wafer was 413 $cm^2/V\text{-}sec$, which is significantly lower than the value obtained in the substrate devices. However, one must realize that the SOI NMOS devices (both ELO and SIMOX) were fabricated on compensated material which saw an additional threshold adjust boron implant. Suprem IV simulations of the NMOS channel region are shown in fig. 5.8 for the dual-gated ELO NMOSFET [1]. The average channel doping concentration is in the excess of $2x10^{16}$ /cm^3, whereas the substrate doping concentration is 8x1014 /cm^3 corresponding to a resistivity of 15-20 Ω-cm. Thus, one would expect the surface mobility of the substrate devices to be larger than that of the SIMOX devices. The second reason for the lower observed mobility values, which is again equally applicable to the ELO devices, is the larger series resistance associated with the thinner SOI layers. The larger series resistance could affect the computed mobility values as will be seen later. The output curves of fig. 5.4 show well defined saturation characteristics with no kinks in the measured drain current. This proves tlhat the SIMOX devices fabricated in a 1500Å thick SOI film were fully depleted. One may recall that partially depleted NMOS devices suffer from floating body effects that would result in a kink in their output characteristics.

Dual-gated MOSFETs fabricated with Epitaxial Lateral Overgrowth were fabricated at the same time as the conventional single-gated devices. The only difference between the two devices is the absence of the bottom polysilicon gate in the single-gated transistor. Since the dual-gated devices were not fabricated with a recessed polysilicon gate, the single-gated devices were always thicker than the dual-gated devices. Since CMP was used to define the thin SOI layer, the single-gated devices were typically 4500Å-5000Å thick as compared to the dual-gated devices which had an average SOI film thickness of 150081. Consequently, the ELO single-gated devices wcrc predominantly partially depleted and exhibited a kink in their output characteristics

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[1] In order lo maintain a valid comparison bctween thc ELO and SIMOX wafcr, thc SIMOX devices were implanted with exactly the same boron energy and dose as the ELO wafer. Therefore fig. 5.8 provides a reasonable estimate of the boron profile in the SIMOX wafer as well.

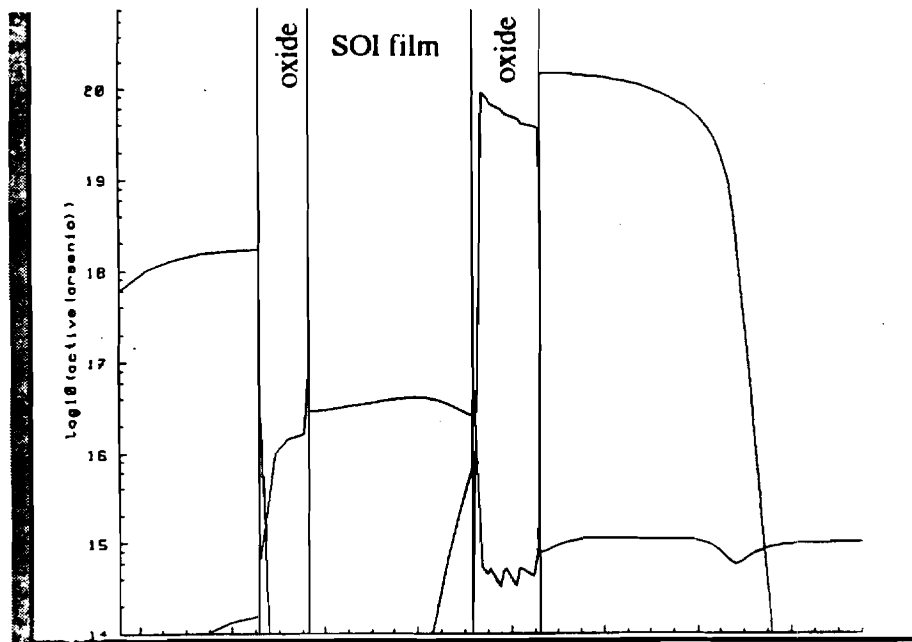


Figure 5.8 Channel doping profile for a dual-gated NMOS transistor fabricated using Epitaxial Lateral Overgrowth. The doping profile was obtained from SUPREMIV simulations

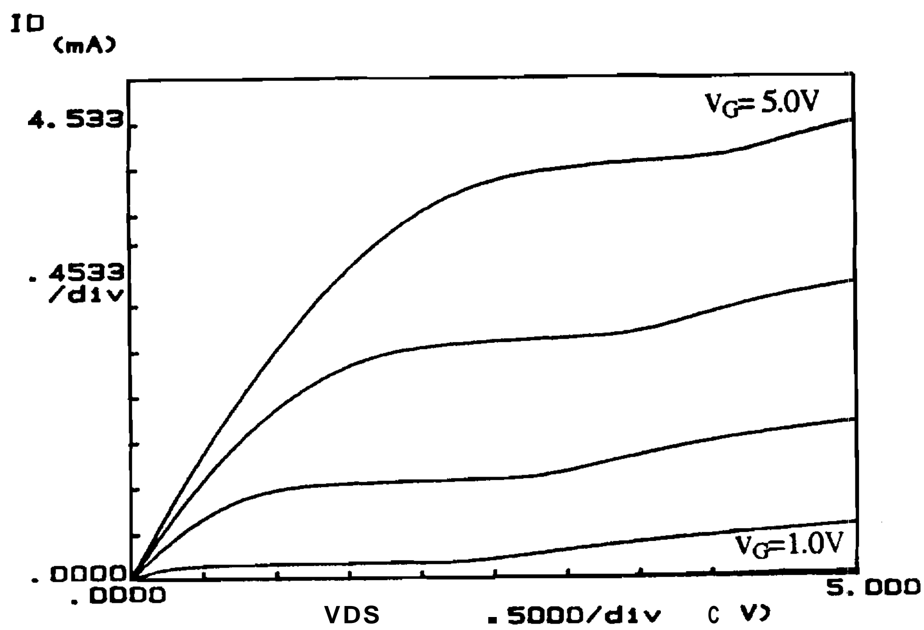


Figure 5.9 Output characteristics for a partially-depleted single-gated ELO NMOS device. The curves distinctly demonstrate the kink phenomena

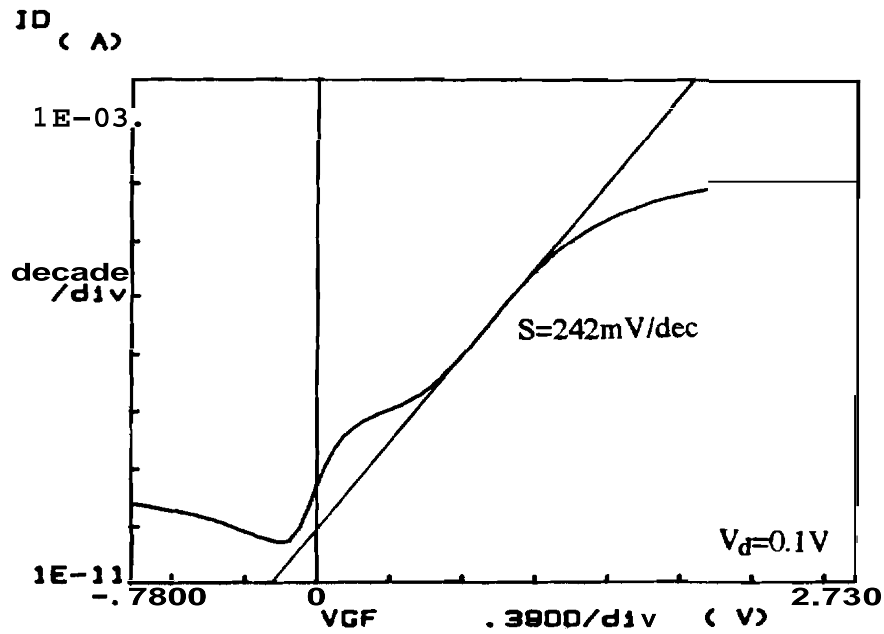


Figure 5.10 Subthreshold characteristics for the single-gated partially-depleted ELO NMOS device

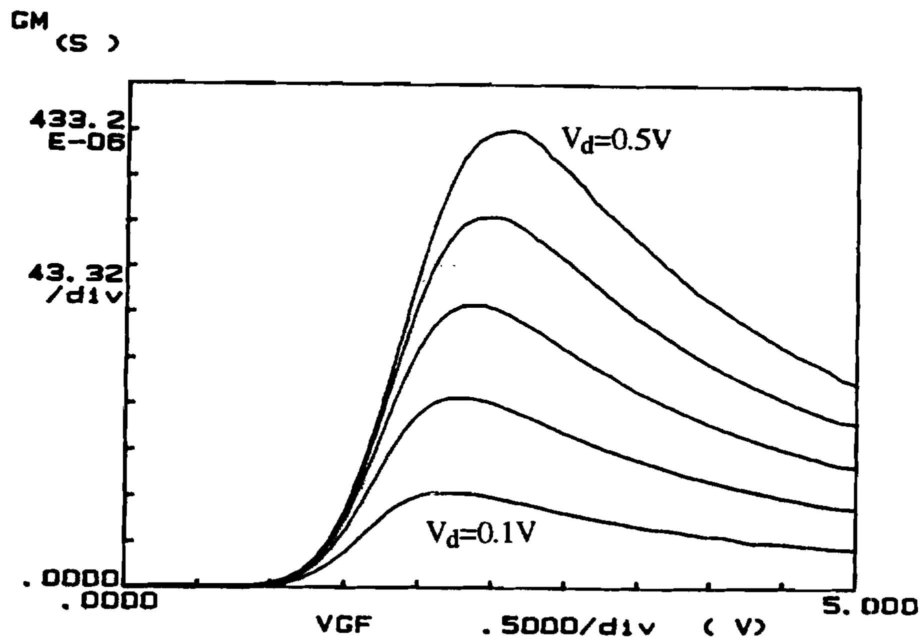


Figure 5.11 Transconductance curves for the single-gated, partially-depleted ELO NMOS transistor

clearly discernible in fig. 5.9. The output characteristics, sub-threshold curves and the transconductance g_m of the ELO partially depleted device are shawn in fig. 5.9 through 5.11. Once again, the poor sub-threshold characteristics are immediately obvious. Just as in the case of the SIMOX wafer, the low leakage currents of fig. 5.10 was a rarity and most devices exhibited the large leakage currents of fig. 5.7. The summary of measured data on the single-gated partially depleted NMOS devices fabricated on ELO material are listed in Table 5.3. The poor subthreshold characteristics observed in the NMOS SOI devices are in sharp contrast to the excellent characteristics of the substrate devices.

Table 5.3 Summary of Measured Data on Single-Gated Partially-Depleted ELO NMOS Devices. Averages are taken over 25 devices. L=2.6μm, $t_{ox,f}$=550Å, t_{si}=4500Å

Parameter	Average Value	Best Value
$I_{D,sat}$: V_D=V_G=5.0V	5.1x10^{-5} A/μm	5.8x10^{-5} A/μm
S	346 mV/dec	242 mV/dec
Leakage	100nA-10μA	100nA
V_T	1.5V	--
G_m @ V_D=0.1V	1.1 μS/μm	1.3 μS/μm
$\mu_{n,eff}$	473 cm^2/V-sec	528 cm^2/V-sec
BV_{DS} @ V_G = 0V	12.6V	13.0V

Since the only difference in the processing of the SOI (ELO and SIMOX) devices and the NMOS substrate devices is the additional boron implant required by the SOI transistors, one is apt to blame this extra processing step for the differences in the measured subthreshold charactertstics. It would be incorrect to assume that the degraded subthreshold slopes are a result of bad material since later in this chapter p-channel

MOSFETs demonstrating almost ideal behavior are presented, whose fabrication did not require a threshold adjust implant.

Our conjecture is that the non-ideal subthreshold slope is the result of a non-uniform boron doping profile in the mesa-isolated SOI islands. It is well-known that in mesa-isolated devices, if the edges of the mesa have either a thinner gate oxide or a slightly lower doping concentration, then these regions along the edges of the device would have a lower threshold voltage due to charge sharing effects. The edges could therefore turn-on prior to the main transistor such as depicted schematically in fig. 5.12. This extraneous leakage could significantly degrade the measured sub-threshold slope. It is also possible for the single kink of fig. 5.12 to become smeared out over a range of gate voltages depending in the boron doping profile. The ELO device of fig. 5.10 depicts a single kink just as qualitatively portrayed in fig. 5.12. The SIMOX device, likewise, demonstrates the slightest hint of a kink in its subthreshold curve. Further optimization of the implanted boron profile and the mesa-isolation technique may produce more ideal devices with sharper turn-on characteristics. The high values of the subthreshold leakage could only be attributed to some sort of impurity transfer between the photoresist mask and the silicon wafer. The substrate devices which were processed using an oxide mask indicate that extremely low leakage currents are possible in a photoresist free process.

The thickness of the SOI layer fabricated by Epitaxial Lateral Overgrowth is determined by chemical mechanical planarization. Non-uniformities in the planarization often resulted in regions of the wafer where the dual-gated devices were over-planarized. The single-gated devices were consequently thinner in these regions and yielded fully depleted devices. Fig. 5.13 depicts the output characteristics of a fully depleted single-gated device fabricated in ELO. Table 5.4 summarizes the measured data on these devices. The fully depleted devices again show no kinks in the saturated output characteristics. The electron mobility values obtained on the single-gated ELO devices were on an average greater than that obtained in SIMOX but less than the substrate devices. It must be reiterated however that all the mobility values are uncorrected numbers and while they indicate that the ELO quality is definitely as good as SIMOX, in terms of absolute numbers, the ELO, SIMOX and substrate devices may in fact demonstrate greater mobilities than the values computed above.

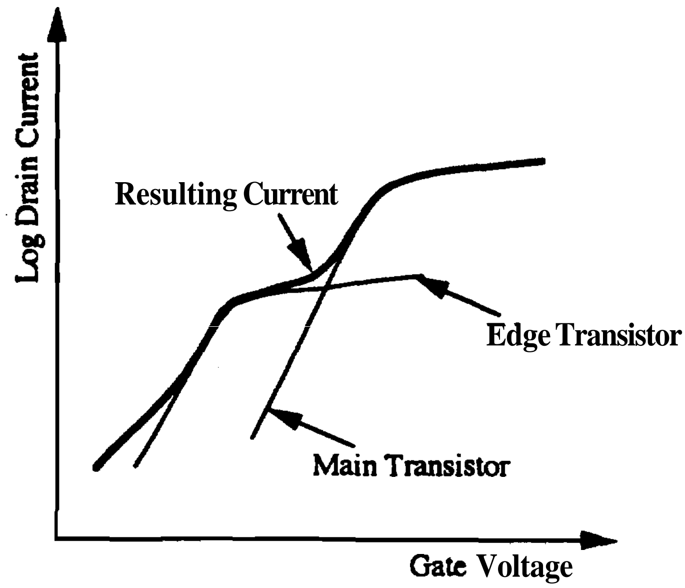


Figure 5.12 Subthreshold characteristics of a transistor with edge leakage. Depending on the amount of leakage, the subthreshold characteristics of the main transistor could be tembly degraded

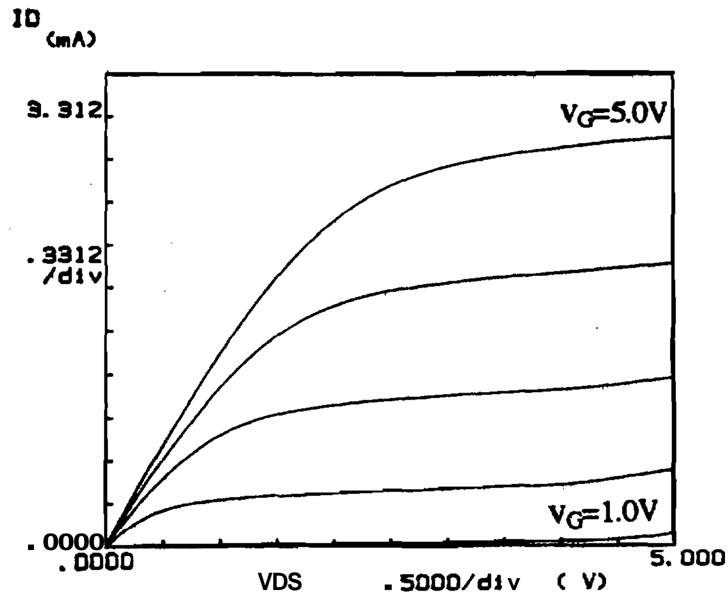
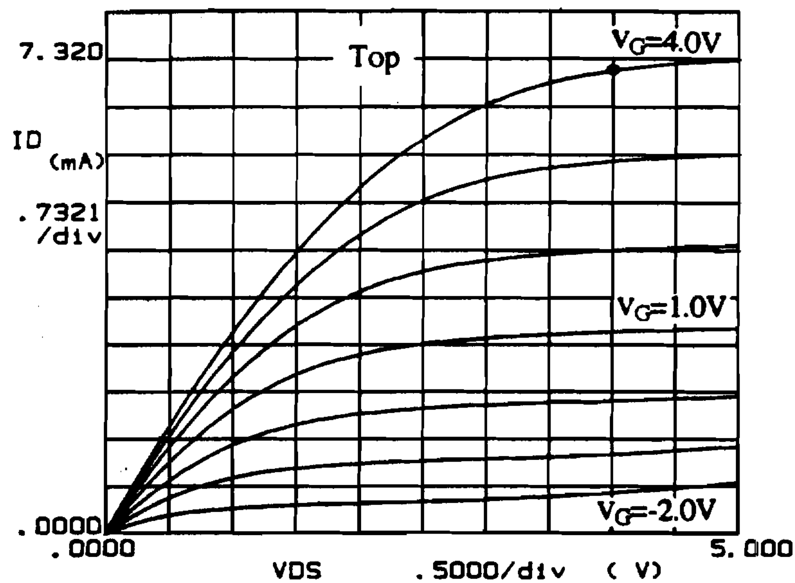


Figure 5.13 Output characteristics for a single-gated fully-depleted ELO NMOS field effect transistor. The fully depleted device shows no kink in its saturated drain current curves

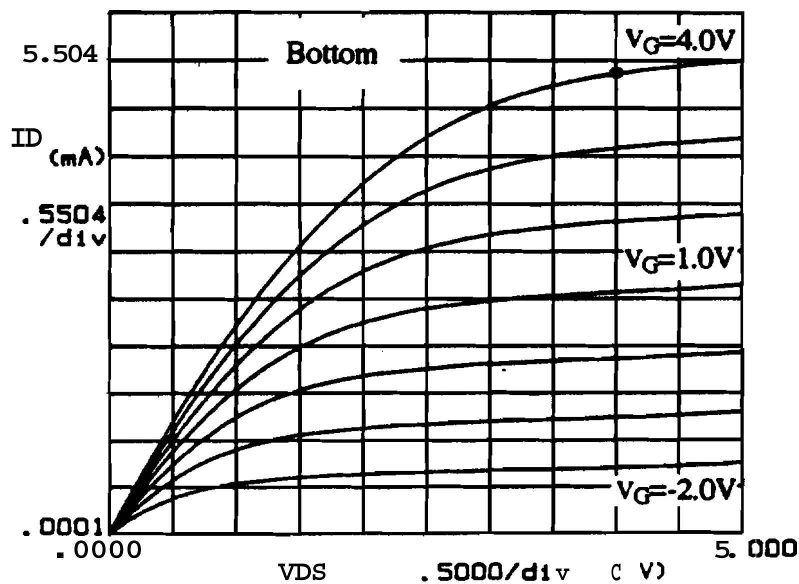
Table 5.4 Summary of Measured Data on Single-Gated Fully-Depleted ELO NMOS Devices. Averages are taken over 5 devices. L=2.6μm, $t_{ox,f}$=550Å, t_{si}=2500Å

Parameter	Average Value	Best Value
$I_{D,sat}$: V_D=V_G=5.0V	5.25x10^{-5} A/μm	5.4x10^{-5} A/μm
S	-	-
Leakage	100nA-10μA	100nA
V_T	1.35V	-
G_m @ V_D=0.1V	1.21 μS/μm	1.3 μS/μm
$\mu_{n,eff}$	477 cm^2/V-sec	490 cm^2/V-sec

Finally, to conclude this section, figs. 5.14 and 5.15 depict the output characteristics and subthreshold characteristics of a perfectly operating dual-gate transistor with the top and bottom gates biased independently. Table 5.5 presents the relevant data for the dual-gate devices. Even though the subthreshold slopes were consistently bad, very good values of electron mobilities were obtained in ELO material. The best ELO dual-gated devices showed mobilities as high as 512 cm^2/V-sec even though the SOI film in the dual-gated devices is doped a lot higher that the single-gate device doping concentration due to arsenic out-diffusion from the bottom gate. The higher n-type doping in the dual-gated transistors is not fully compensated for by the boron threshold implant. Therefore, the threshold voltages in these devices are typically a lot lower (more negative) than those in the single-gated ELO devices and the fully depleted SIMOX devices. The difference in threshold voltage also partially proves the existence of a larger n-type doping in the SOI film of the dual-gated transistor. In the next section, a more detailed look at the dual-gated device is presented through p-channel transistors fabricated in ELO. Again, the excess out-diffusion of arsenic from the bottom gate becomes obvious which in this case causes the bottom gate to have a much larger threshold voltage(a more negative value) than the top gate. Such a non-uniform doping



(a)



(b)

Figure 5.14 Output characteristics for a fully-depleted dual-gated ELO NMOS device under (a) top gate control and (b) bottom gate control

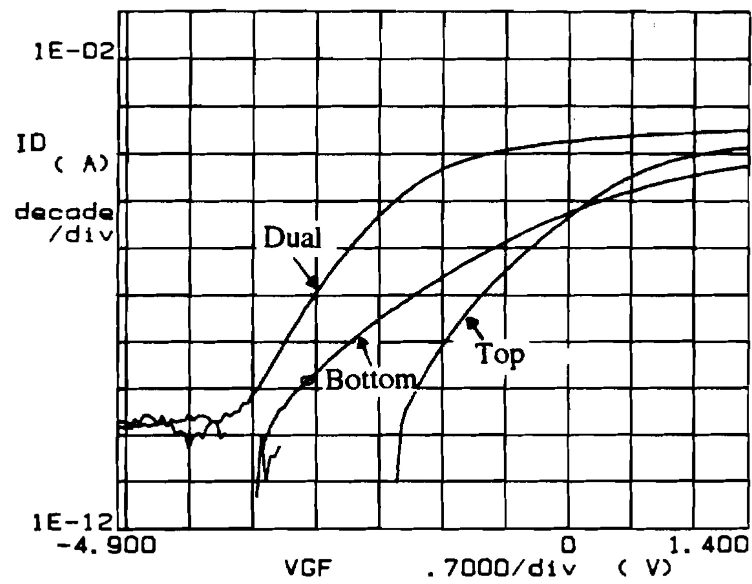


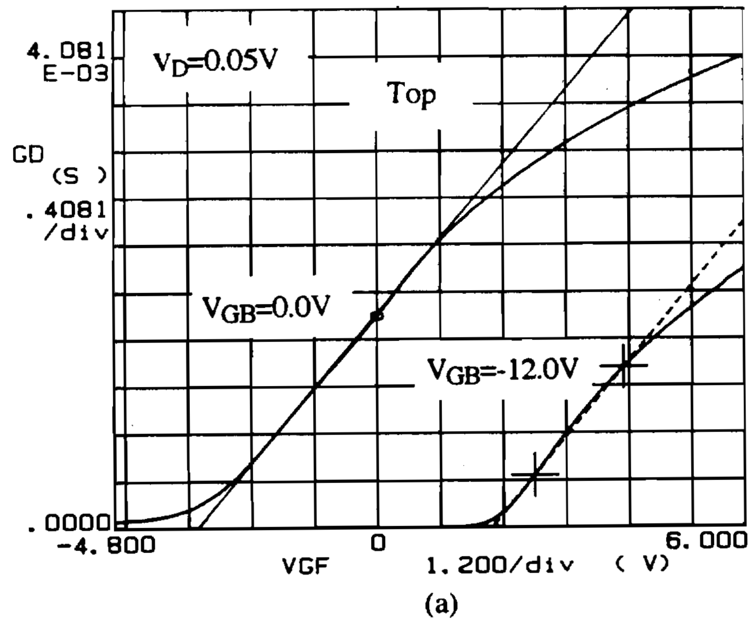
Figure 5.15 **Subthreshold curves for a fully-depleted dual-gated NMOS transistor. The subthreshold slope under dual gate operation is sharper than that under either top or bottom gate control**

profile due to dopant diffusion from the bottom gate is clearly undesirable. Alternate gate dielectrics such as oxy-nitrides and nitrided oxides must then be used to minimize the outdiffusion of the dopant impurities.

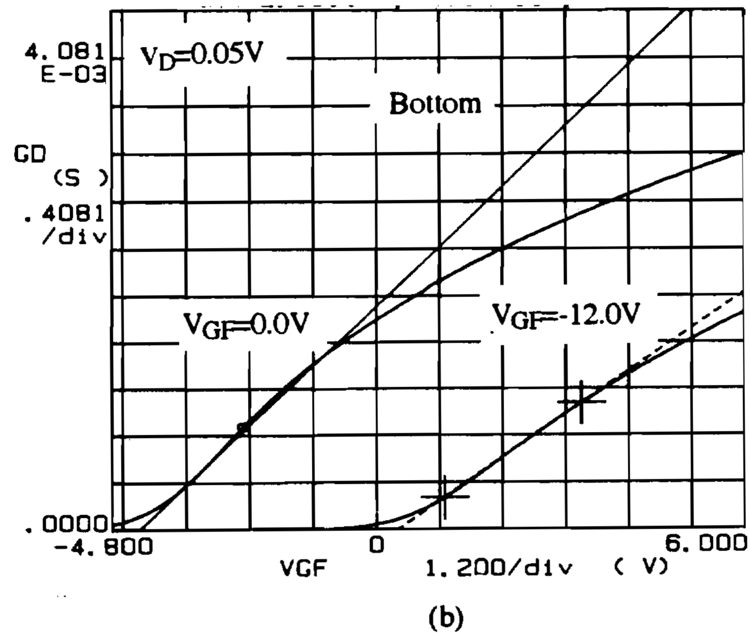
Table 5.5 Summary of Measured Data on Dual-Gated Fully-Depleted ELO NMOS Devices. Averages taken over 20 devices. $L=2.6\mu m$, $t_{ox,f}=1200Å$, $t_{ox,b}=1500Å$, $t_{si}=1250Å$

Parameter	Average Value		Best Value	
	Top	Bottom	Top	Bottom
$I_{D,sat}$	$5.1x10^{-5}$ A/μm	$3.8x10^{-5}$ A/μm	$6.3x10^{-5}$ A/μm	$4.9x10^{-5}$ A/μm
S	342 mV/dec	615 mV/dec	235 mV/dec	455 mV/dec
Leakage	1μA	1μA	1μA	1μA
V_T	-2.61V	-3.08V	-	-
G_m @ V_D=0.1	0.45 mS/mm	0.4 mS/mm	0.6 mS/mm	0.48 mS/mm
$\mu_{n,eff}$	423 cm^2/V-sec	414 cm^2/V-sec	512 cm^2/V-sec	511 cm^2/V-sec

The above results prove the feasibility of the dual-gated devices fabricated using epitaxial lateral overgrowth. The material quality is excellent not withstanding growth over a step caused by the bottom polysilicon gate. The output characteristics of the top gate and bottom gate devices show no discernible kinks which indicates a fully depleted film, The drain conductance of the top and bottom gates with the 'other' gate grounded or accumulated is portrayed in fig. 5.16. The threshold voltage of the top gate (bottom gate) increases significantly when the bottom gate (top gate) is accumulated as compared to its value when the bottom gate (top gate) is grounded. This is typical of a fully depleted film in which the two gates interact with each other through the fully depleted SOI layer ; the



(a)



(b)

Figure 5.16 **Drain Conductance in a dual gated ELO NMOS transistor (a) under top gate control and (b) under bottom gate control. In each case, the 'other' gate is either grounded or strongly accumulated**

result of electro-statically coupled interfaces. In order to improve the subthreshold characteristics of the various devices, we fabricated p-channel MOS field effect transistors. These results are presented in the next section.

5.3.2 P-Channel MOS Transistors

The discussion again begins with substrate devices. The output characteristics, the subthreshold slope and the transconductance of a typical device are shown in figs. 5.17, 5.18 and 5.19. The mobility $\mu_{p,eff}$ obtained on the substrate PMOS device is approximately 240 cm^2/V-sec which is a good number for bulk silicon. The inverse

Table 5.6 Summary of Measured Data on Substrate PMOS Devices. Average taken over 25 devices. $L=2.2\mu m$, $t_{ox,f}=550Å$

Parameter	Average value
$I_{D,sat}$: $V_D=V_G=-5.0V$	$6.1x10^{-5}$ A/μm
S	100.5 mV/dec
Leakage	< 1pA
V_T	0.25V
G_m @ $V_D=-0.1V$	0.69 $\mu S/\mu m$
$\mu_{p,eff}$	240 cm^2/V-sec

subthreshold slopes and subthreshold leakages both show extremely low values, indicative of a good device operation. The measured device parameters are summarized in Table 5.6. Figs. 5.20-5.22 are representative curves depicting the output, subthreshold

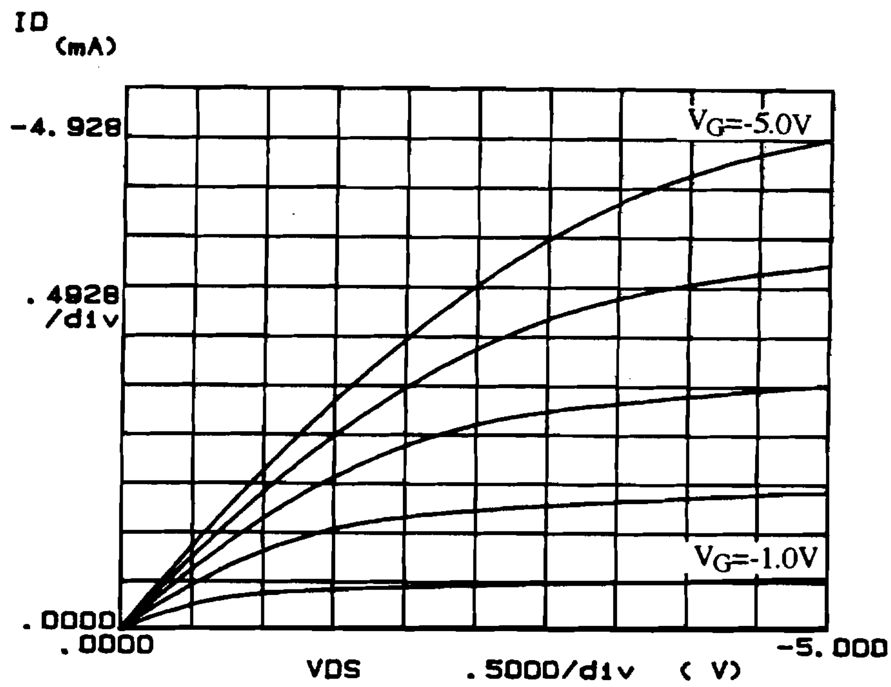


Figure 5.17 Output characteristics for a typical Substrate PMOS device

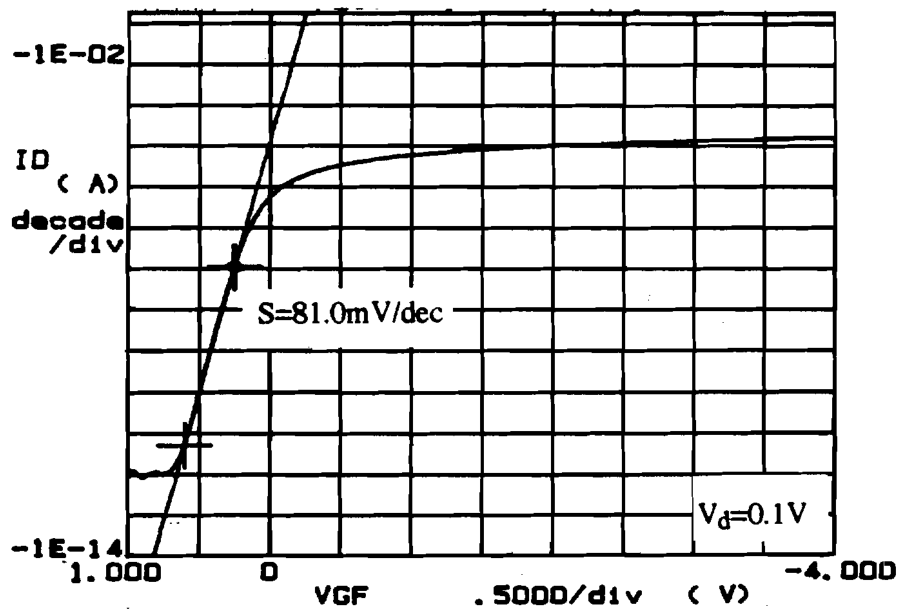


Figure 5.18 Subthreshold characteristics for the substrate PMOS device

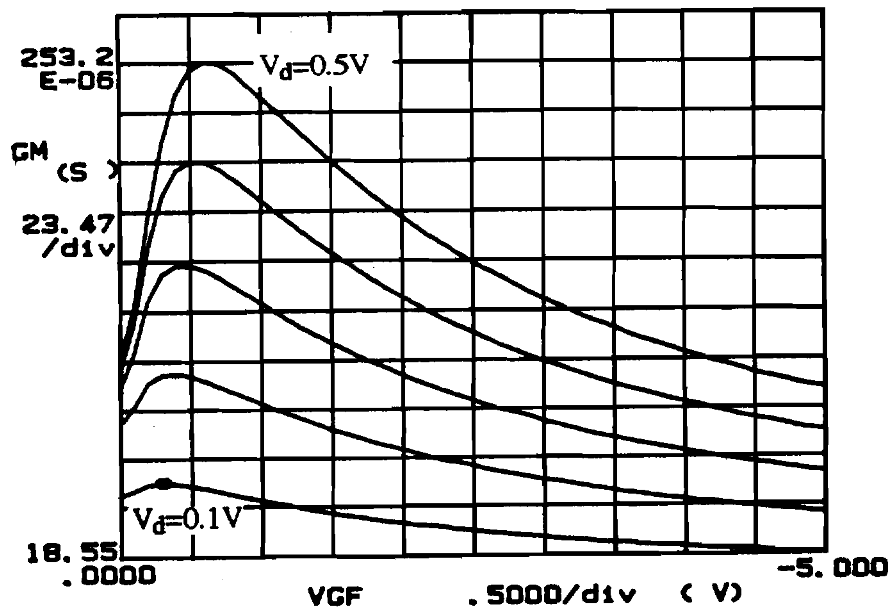


Figure 5.19 Transconductance curves for the substrate PMOS device for different drain voltages

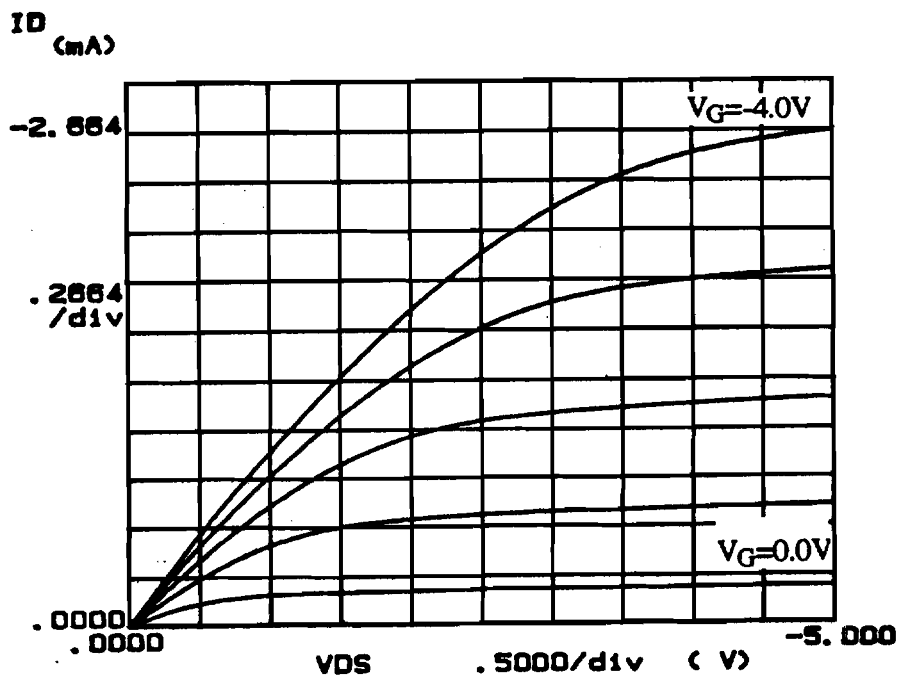


Figure 5.20 Output characteristics for the SIMOX PMOS transistor

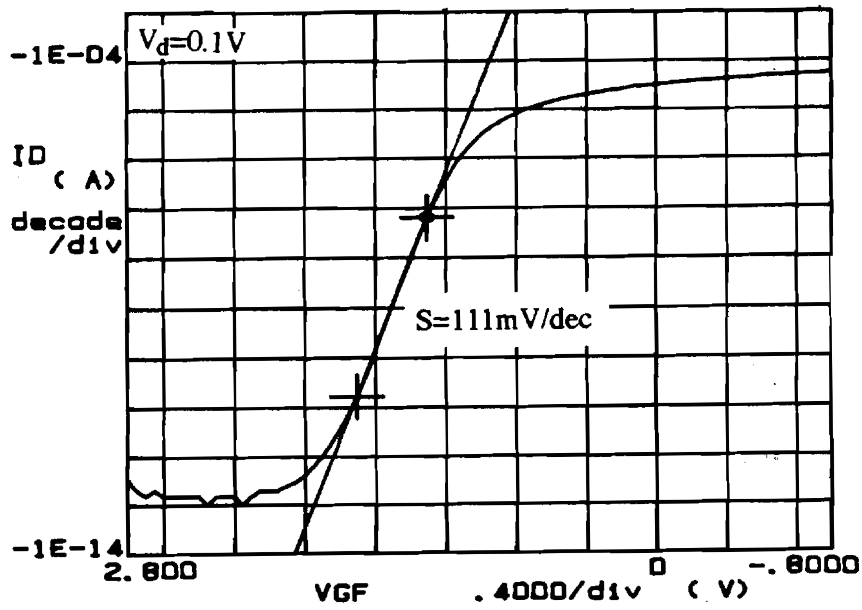


Figure 5.21 Subthreshold characteristics for the SIMOX PMOS transistor demonstrating low leakage currents

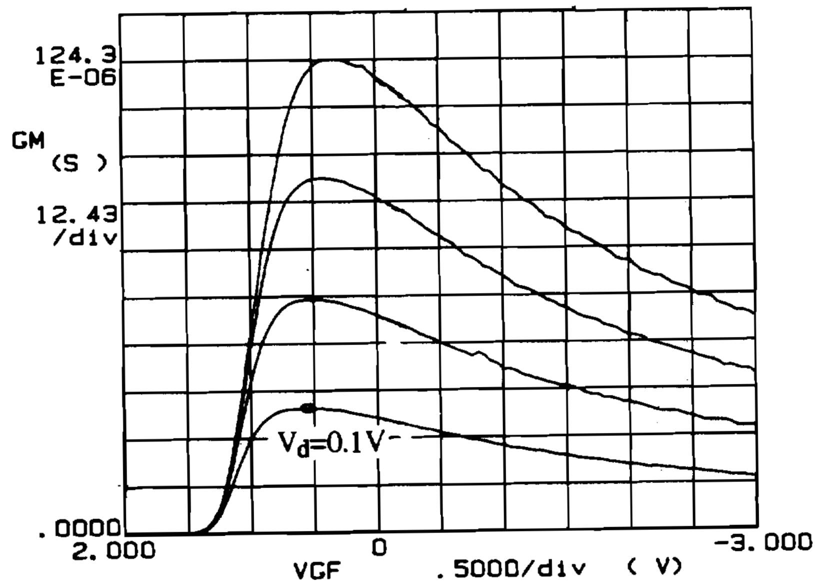
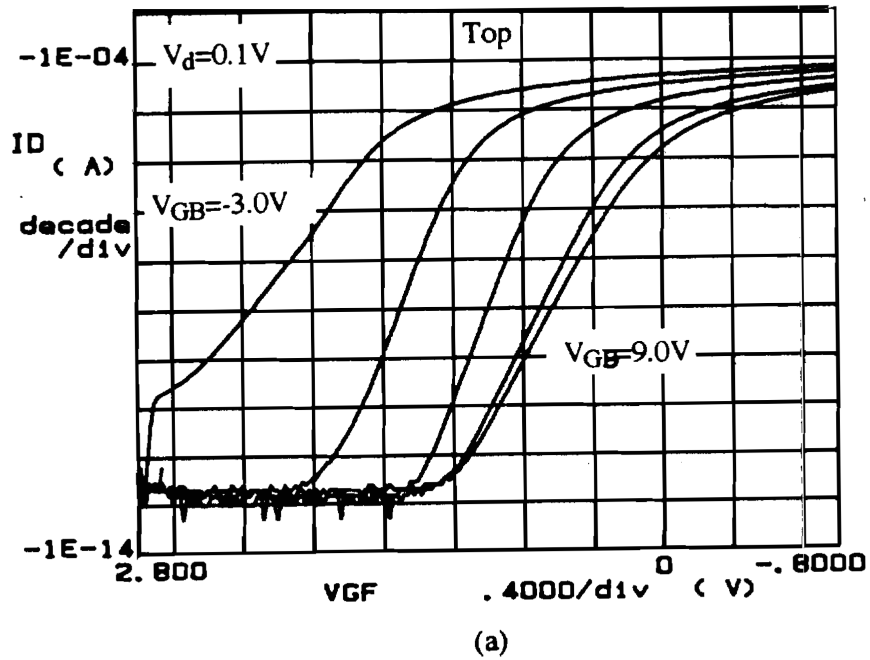


Figure 5.22 Transconductance curves for the SIMOX PMOS transistor for different drain voltages

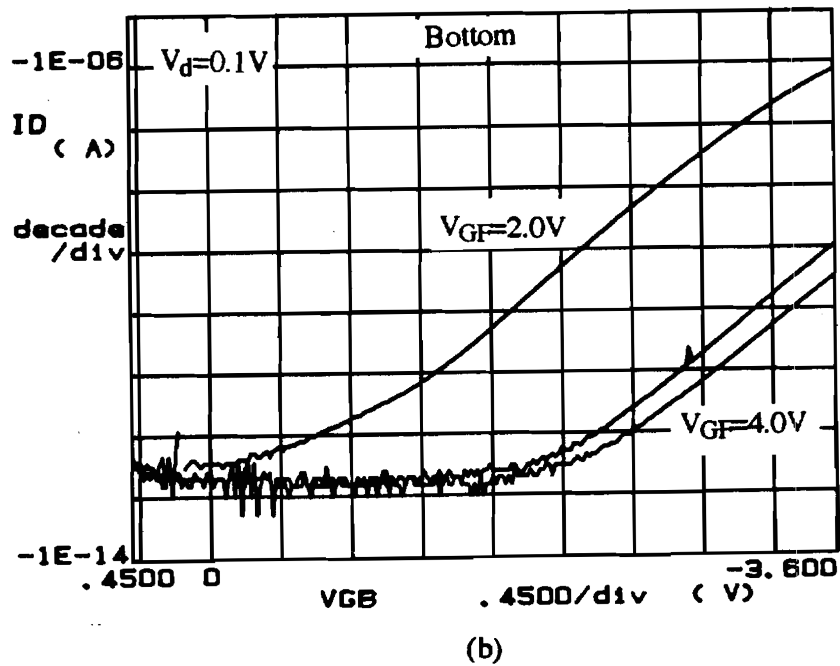
and transconductance characteristics of the SIMOX PMOS field effect transistor. The PMOS devices do not typically suffer from the kink effect since the ionization rate of holes is much less than that of electrons. The absence of the kink is not indicative of a fully depleted PMOS FET. However, if the SIMOX substrate is used as a 'back gate' and biased respective to the source, the front gate characteristics are modified as depicted in fig. 2.23 (a). This proves that the film is fully depleted through the mutual coupling of the front and back interfaces. There are a few points of interest to note in fig. 2.23 (a). The subthreshold slope and the threshold voltage change with the applied back gate bias. When the back gate is strongly accumulated, the curves do not shift to the right any more as the transistor begins to behave more like a partially depleted device. The subthreshold slope remains the same so long as the back gate is depleted, but degrades once the back gate begins to get accumulated. Fig. 2.23 (b) is a plot of the back gate subthreshold characteristics as the front gate voltage is varied. The back gate subthreshold slope of a SIMOX wafer is exceedingly bad - typically in the excess of 500mV/dec. The buried oxide, moreover, is very thick and not readily amenable to changes in thickness. These points highlight the usefulness of dual-gated devices fabricated using selective epitaxy. A summary of the measured data on the SIMOX PMOS FET is presented in Table 5.7.

Table 5.7 Summary of Measured Data on SIMOX PMOS Devices. Averages taken over 25 devices. $L=0.24\mu m$, $t_{ox,f}=550Å$

Parameter	Average Value	Best Value
$I_{D,sat}$: $V_D=V_G=-5.0$	$4.5x10^{-5}$ A/µm.	$4.9x10^{-5}$ A/µm
S	109 mV/dec	108 mV/dec
Leakage	< 1pA	< 1pA
V_T	1.08 V	-
G_m @ $V_D=-0.1V$	0.4 µS/µm	0.41µS/µm
$\mu_{p,\,eff}$	151 cm²/V-sec	164 cm²/V-sec



(a)



(b)

Figure 5.23 (a) Varying front gate subthreshold characteristics as a function of back gate bias and (b) varying back gate subthreshold curves for different front gate biases, for a SIMOX PMOS transistor

Fig. 5.24 is an example of the back gate output characteristics of the SIMOX PMOS transistor. The extremely low saturation drain currents obtained are due mainly to the thick gate oxide (3200Å), which is also the primary cause of the premature short channel effects visible in the characteristics. The mobility along the back interface of the SIMOX device is on an average about 142 cm^2/V-sec, and is comparable to the value along the cop interface quoted in Table 5.7.

Both fully depleted single-gated and fully-depleted dual-gated PMOS transistors were fabricated on ELO silicon. Tables 5.8 and 5.9 summarize the relevant data on these devices. Fig. 5.25-5.27 present the output, subthreshold and transconductance curves for the single-gated fully-depleted ELO-SOI PMOS transistor. The low value of the subthreshold leakage current and the small inverse subthreshold slope are indicative of a superior material and interface.

Table 5.8 Summary of Measured Data on Single-Gated Fully-Depleted ELO PMOS Devices. Avenges are taken over 25 devices. L=0.24µm, $t_{ox,f}$=550Å, t_{si}=1500Å

Parameter	Average Value	Best Value
$I_{D,sat}$: V_D=V_G=-5.0V	3.6x10^{-5} A/µm	5.3x10^{-5} A/µm
S	103 mV/dec	86 mV/dec
Leakage	< 1pA	< 1pA
V_T	-0.564 V	-
G_m @ V_D=-0.1V	0.48 µS/µm	0.6 µS/µm
$\mu_{p,eff}$	177 cm^2/V-sec	215 cm^2/V-sec

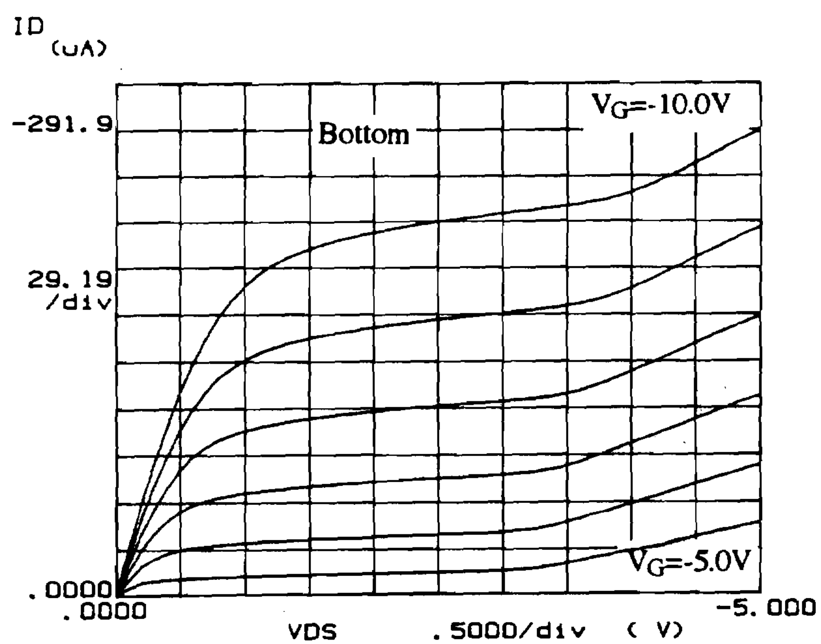


Figure 5.24 Back gate output characteristics for the SIMOX SOI PMOS; device

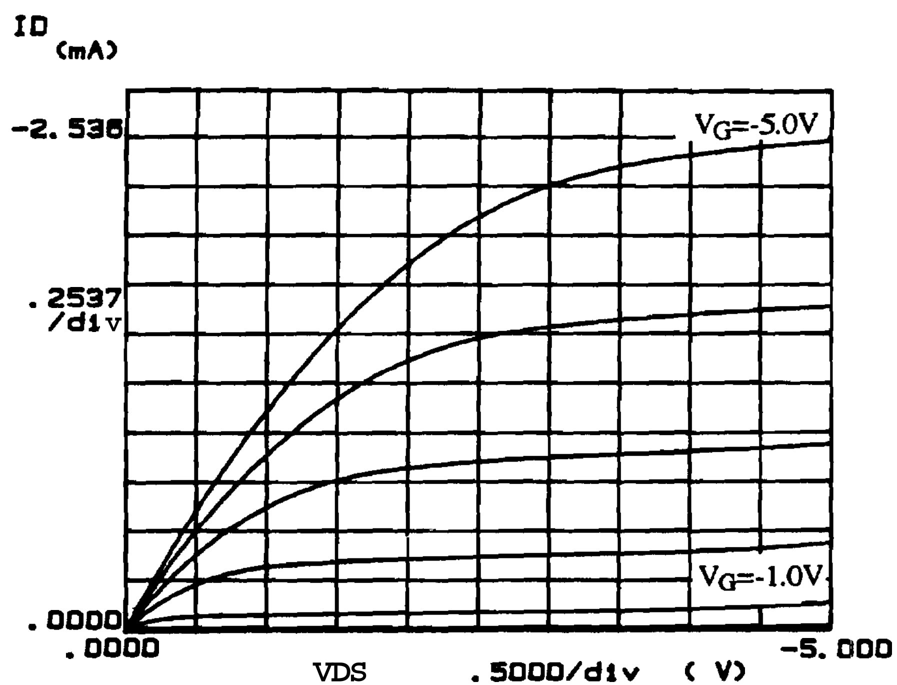
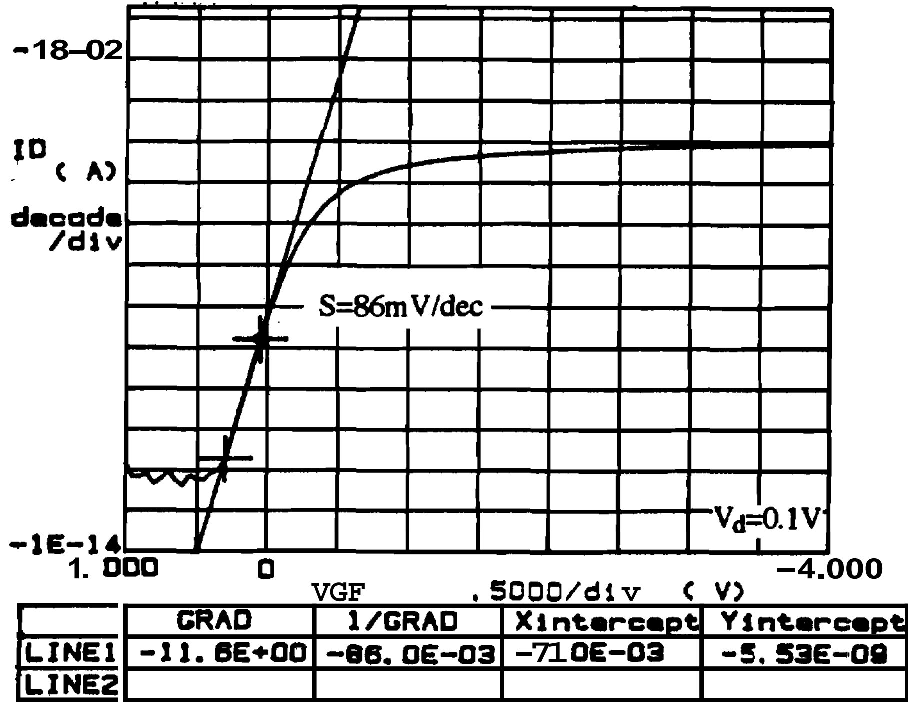


Figure 5.25 Output characteristics of a fully-depleted single-gated ELO-SOI PMOS device



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-11.6E+00	-86.0E-03	-710E-03	-5.53E-09
LINE2				

Figure 5.26 Subthreshold characteristics for the single-gated fully-depleted ELO-SOI PMOS transistor

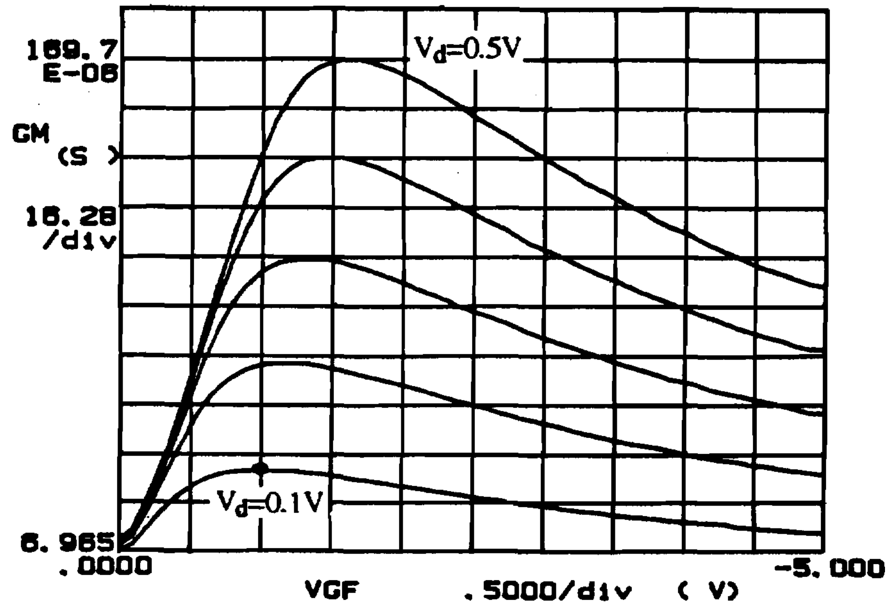


Figure 5.27 Transconductance curves for the single-gated, fullydepleted ELO P-channel SOI MOSFET

The top interface of the ELO silicon is determined by the chemical mechanical planarization process. Any surface roughness or impurities left behind by the planarization process would affect the mobility and the subthreshold slope of the fabricated device. There are two primary slumes available for chemical mechanical polishing at Purdue University - NALCO 2350 and NALCO 2355. A 1:15 mixture of NALCO 2350:DI water is typically used to planarize the ELO, and yields optimum results when planarizing large overgrowths. Characteristic etch rates arc: about a micron per minute. The NALCO 2355 slurry, to be used in a 1:10 ratio by volume of slurry:DI water under the same pad pressure and pad rotation conditions, provides an etch rate of only about 1000Å/min. Consequently NALCO 2350 was the preferred etch slurry for ELO planarization. Microscope observations indicated that a smoother and more specular finish was obtained with the NALCO 2355 etch slurry. Therefore we employed NALCO 2350 to planarize the down to the etch-stop and then incorporated a 10-15 mins. finishing etch with NALCO 2355 to yield the best possible results. A single gate fully-depleted ELO process was carried out at the same time as the process whose measured data was presented above, with the exception of the finishing NALCO 2355 planarization. The measured subthreshold slopes were consistently greater on this wafer and yielded average values of about 155mV/dec.

Figures 5.28 through 5.35 adequately describe the behavior of the dual-gate transistor. Figs. 5.28 and 5.29 present the output characteristics of the thin film fully-depleted PMOSFET under top gate control and bottom gate control respectively. The output characteristics of the device under dual-gate operation is shown in fig. 5.30, which indicates a significantly larger current flowing across the device. As seen through numerical simulations in Chapter 3, when compared at a constant V_G-V_T however,' the observed enhancement in current of the dual-gated transistor is effectively eliminated and the current under dual-gate operation exceeds the sum of the currents of the top gate and the bottom gate by approximately 15%. This is shown in figure 5.31 for two different dual-gate devices. In chapter 3, comprehensive numerical simulations using PISCES were carried out and it was concluded that the current under dual-gate operation would exceed the sum total of the currents of the top and bottom gates by a maximum of 5%, so long as all values were compared at constant gate voltage excursions above threshold. This conclusion refuted the claims made by other researches of a greater than 50% enhancement in the current under dual-gate operation. While the results presented above definitely do not indicate the preposterous 70-75% enhancements often quoted, it is still

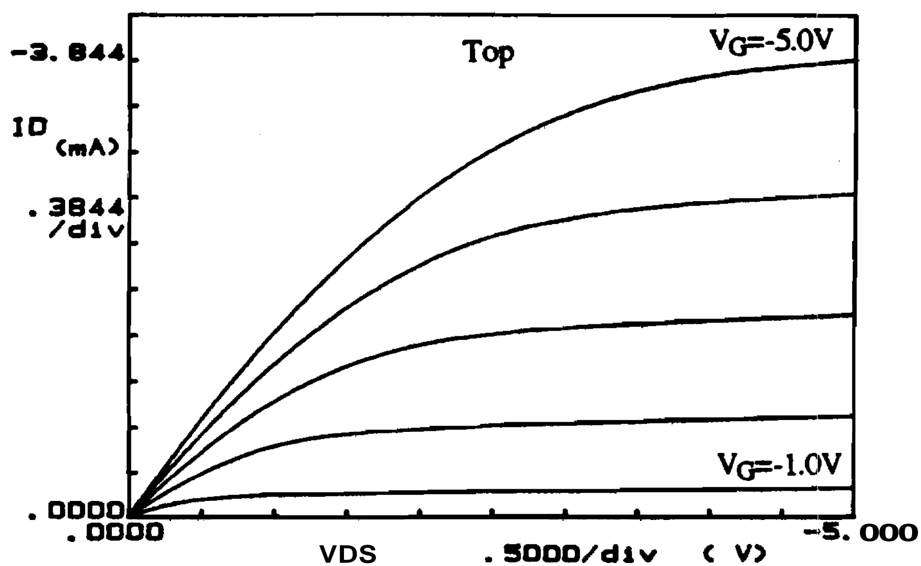


Figure 5.28 Output characteristics of the thin-film fullydepleted dual-gated ELO-PMOS transistor under top gate control

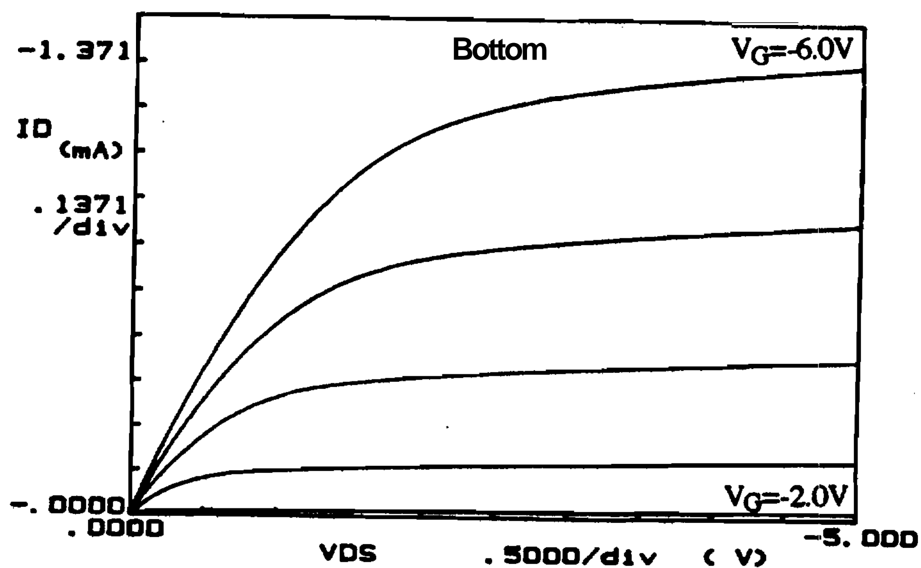


Figure 5.29 Output characteristics of the thin film fully-depleted dual-gated ELO-PMOS transistor under bottom gate control

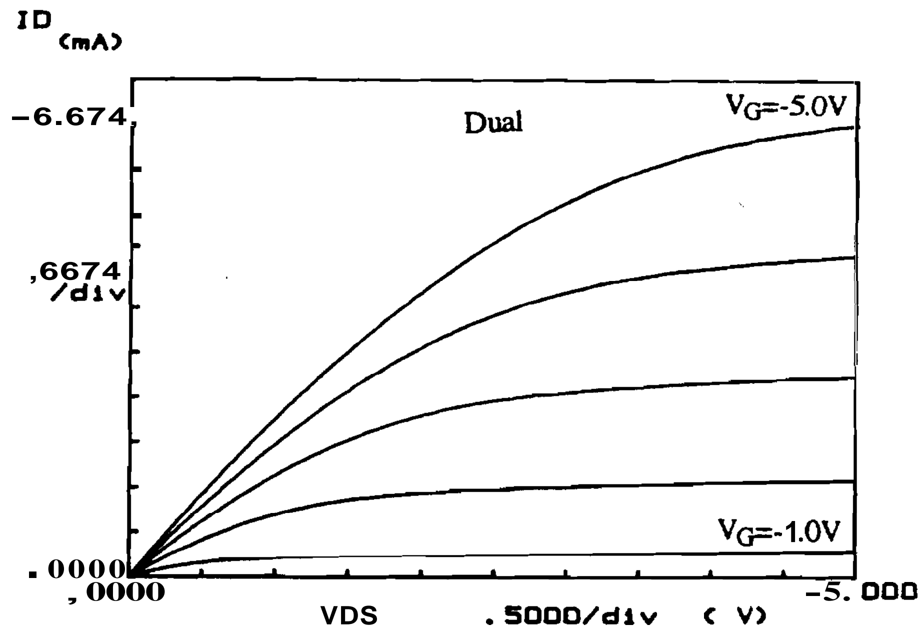
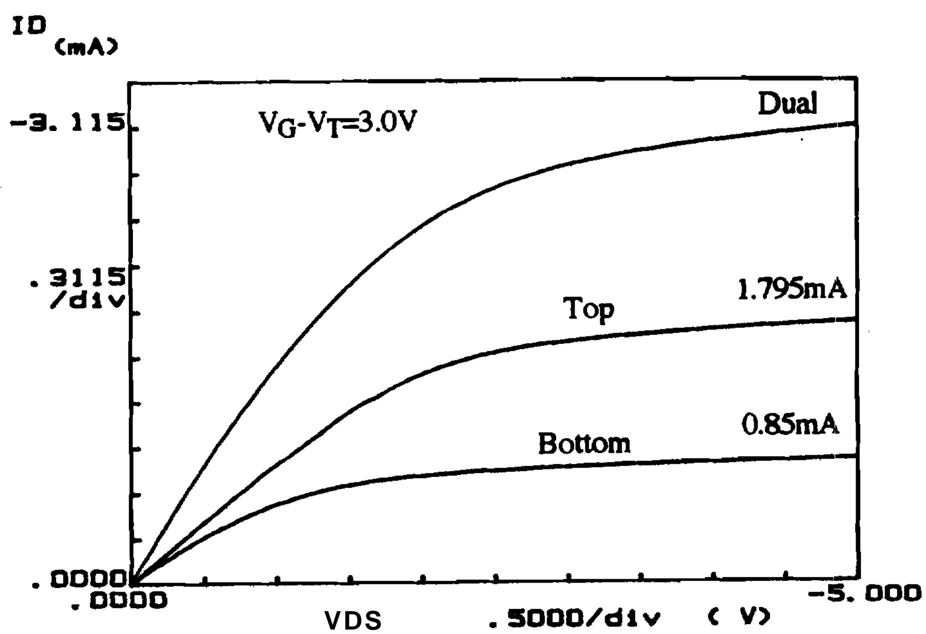


Figure 5.30 Output characteristics of the fully-depleted dual-gated ELO-SOI p-channel transistor under dual-gate control



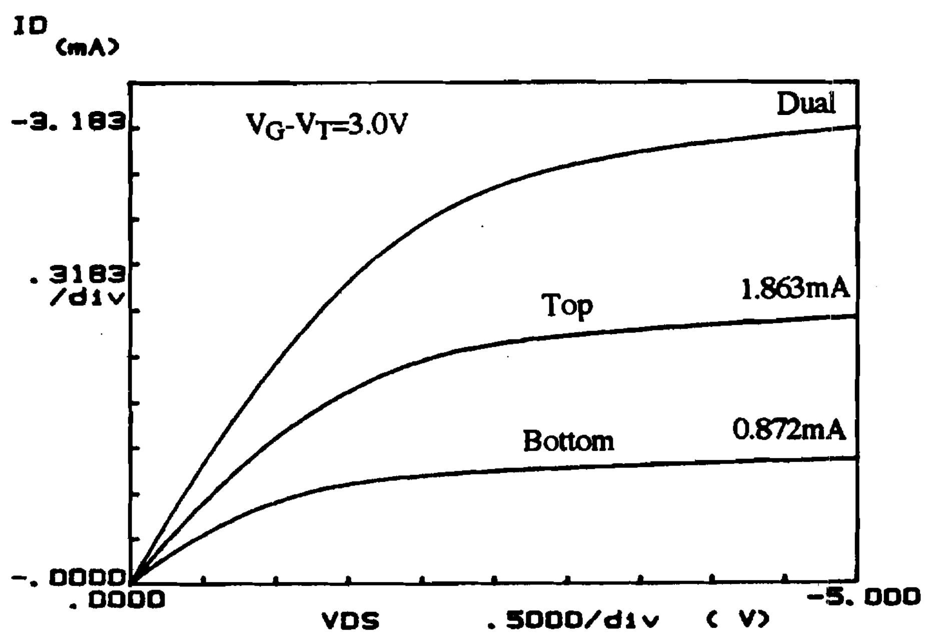


Figure 5.31 Comparison of drain currents under top gate operation, bottom gate operation and dual gate operation. The comparisons are made at a constant V_G-V_T=3.0V

Table 5.9 Summary of Measured Data on Dual-Gated Fully-Depleted ELO PMOS Devices. Average taken over 10 devices. $L=0.24\mu m$, $t_{ox,f}=550Å$, $t_{ox,b}=1500Å$, $t_{si}=1500Å$

Parameter	Top	Bottom	Dual
$I_{D,sat}$: $V_D=V_G=-5.0$	2.9×10^{-5} A/μm	1.1×10^{-5} A/μm	5.2×10^{-5} A/μm
S	117 mV/dec	146 mV/dec	95 mV/dec
Leakage	< 1pA	< 1pA	< 1pA
G_m @ $V_D=-0.1V$	0.4 μS/μm	0.31 μS/μm	0.65 μS/μm
V_T	-0.65V	-1.58V	-0.08V
$\mu_{p,eff}$	149 cm^2/V-sec	145 cm^2/V-sec	

larger than the 5% predicted by the numerical simulations. The discrepancies could potentially be due to experimental errors in computing the threshold voltage. As was seen in chapter 2 and earlier in this chapter, the threshold voltage of the top gate depends in the back gate voltage and vice versa. The threshold voltage decreases as the back gate moves into depletion and it increases when the back gate is accumulated. In the PMOS transistor, this can be translated into surface potentials by stating that the more negative the back surface potential, the lower (more positive) the threshold voltage of the top gate. As the back gate is accumulated ad the surface potential becomes zero or slightly positive, the larger (more negative) the threshold voltage of the top gate becomes. Then, the comparison of the curves at a constant V_G-V_T becomes dependent on what value of the back gate (top gate) voltage the threshold voltage of the top gate (back gate) is measured.

In the numerical simulations the back interface of the single-gated device was defined by a neutral contact (in contrast to a n^+-poly, p^+-poly or Al contacts) and thus grounding the back gate ensured that the back interface was under flat-band conditions (zero back surface potential)[2]. This is the optimum condition to make a good comparison between the dual-gated device and the single-gated device. However, in the experimental measurements of fig. 5.31, we had no way of fixing the band bending at the back interface, so that it became difficult to measure the threshold voltage of the top (or bottom) gate while maintaining the other gate under flat-band conditions. Therefore, we measured the threshold voltage of the two gates by merely grounding the other gate, knowing full well that the back interface under these conditions is not in flat-band. If the threshold voltage were measured under more accumulated conditions by applying a small positive voltage to the back gate, the measured threshold voltages of the top and bottom gates would be higher and this would reduce the measured enhancement in current under dual-gate operation. This discussion merely highlights the importance of exercising caution when comparing the characteristics of single-gated and dual-gated devices.

The subthreshold characteristics of the dual-gated device are shown in fig. 5.32. The sub-threshold slope is significantly improved under dual-gate operation as compared to the values obtained under either top gate control or bottom gate control. The dual-gate transistor in this case is non-optimal due to the large differential in the threshold voltage between the top gate and the bottom gate. This is due to the large amount of arsenic out-diffusion from the bottom gate polysilicon at the back interface. In situations where the threshold voltage of the top gate and bottom gates are equal and the device is symmetric, a significantly more improved subthreshold slope under dual-gate operation results. Figs. 5.33 and 5.34 present the subthreshold curves of the top gate and bottom gate transistors with a varying bias applied to the other gate. The changing subthresholld characteristics of the top gate with varying back gate bias and vice versa is indicative of a fully depleted film. The degraded subthreshold slopes of the top gate when the bottom gate is strongly accumulated is also clear in fig. 5.33. Finally, the transconductance of the device under top gate operation, bottom gate operation and dual gate operation are presented in figs. 5.35 through 5.37. The transconductance under dual-gate operation is slightly less than

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[2]In reality there is a non-zero back surface potential due to the small band bending forced by the fixed charge density specified at the back interface.

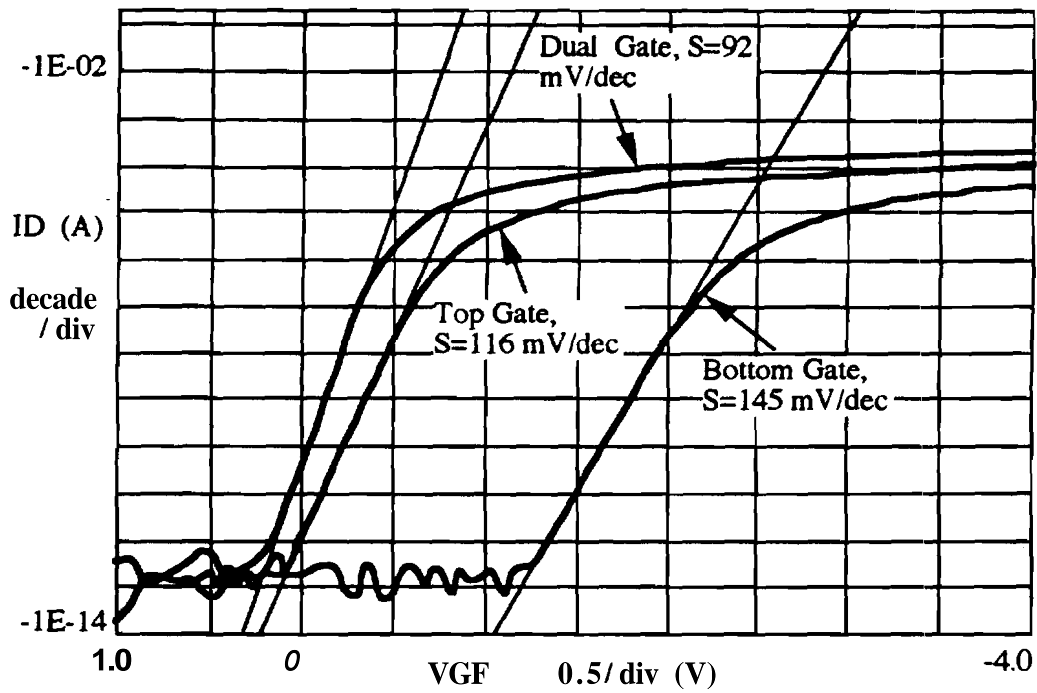


Figure 5.32 Subthreshold characteristics for the dual-gated ELO PMOS device under top gate control, bottom gate control and dual gate control

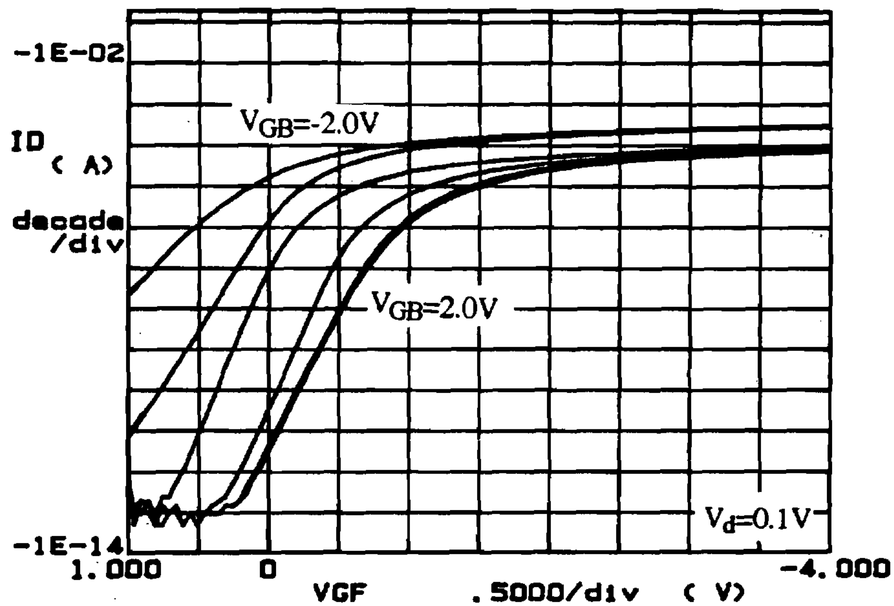


Figure 5.33 Varying front gate subthreshold characteristics as a function of the front gate bias for a dual-gated ELO-SOI MOSFET

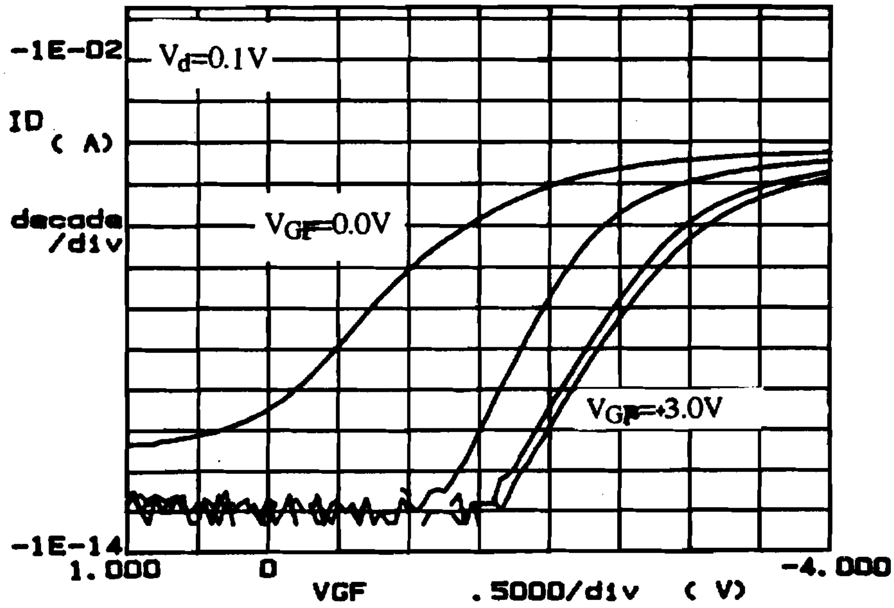


Figure 5.34 Varying back gate subthreshold characteristics as a function of the back gate bias for a dual-gated ELO-SOI MOSFET

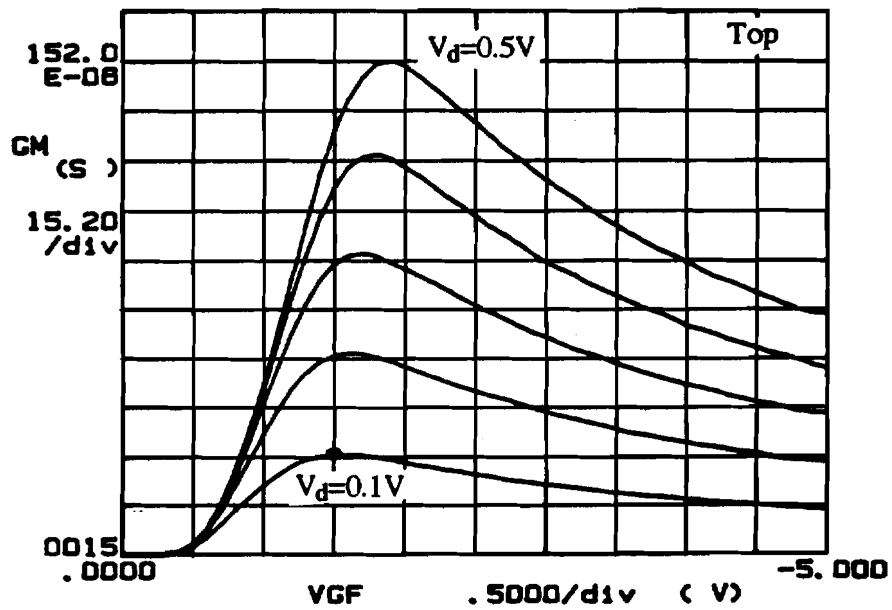


Figure 5.35 Transconductance curves for a dual-gated ELO-SOI PMOSFET under top gate control

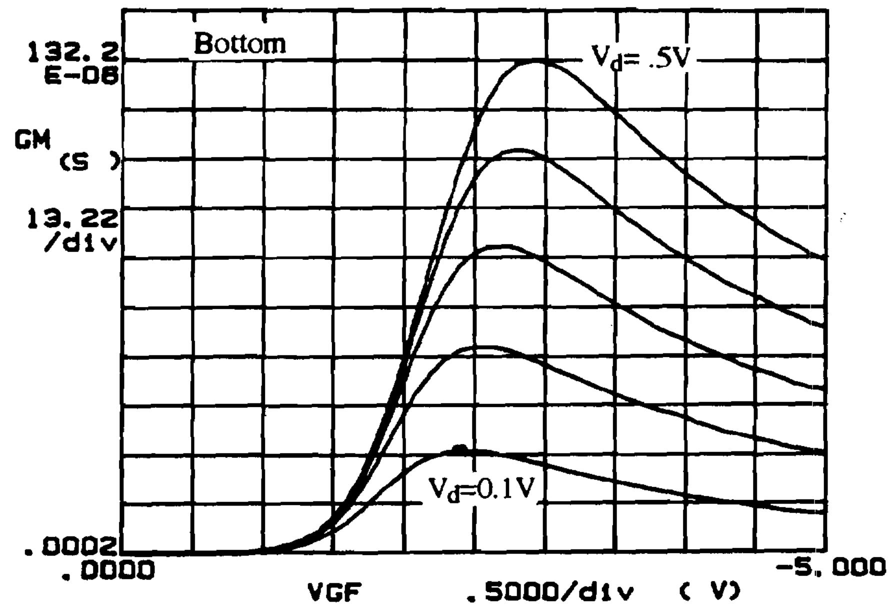


Figure 5.36 Transconductance curves for a dual-gated ELO-SOI PMOSFET under bottom gate control

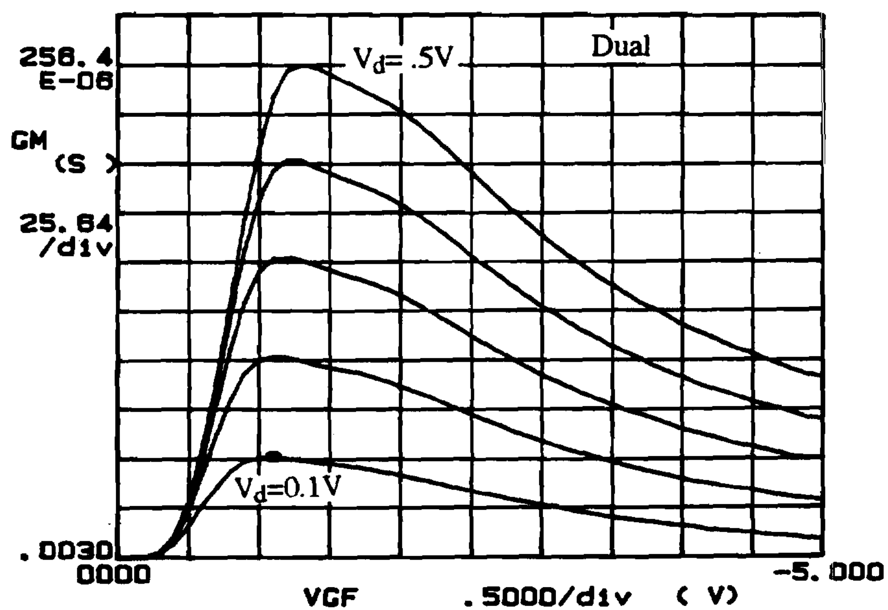


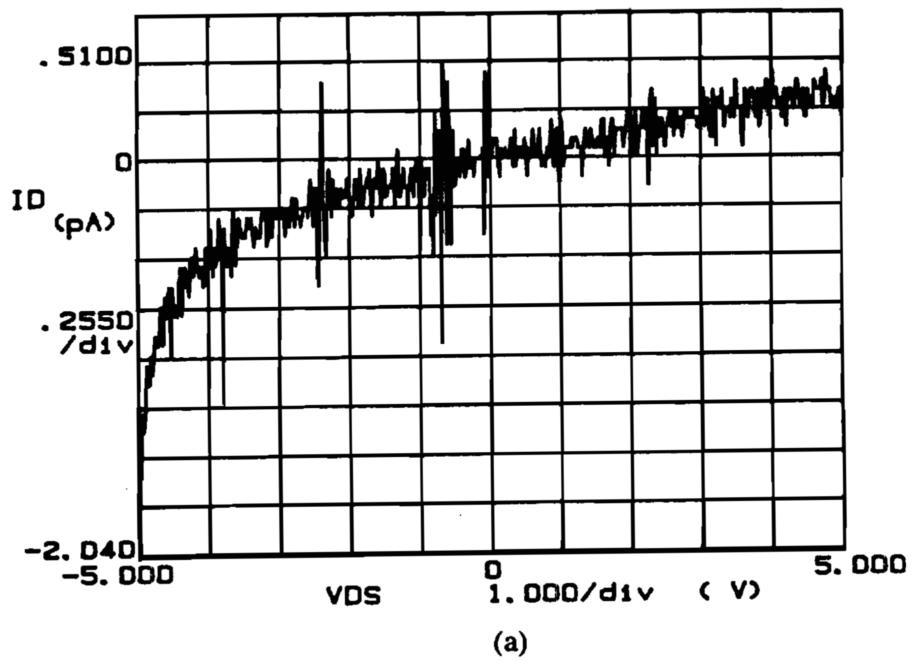
Figure 5.37 Transconductance curves for a dual-gated ELO-SOI PMOSFET under dual gate control

the sum of the transconductances in figs. 5.35 and 5.36. This is again due to the asymmetric device under test, which results in a spread out transconductance curve rather than a single sharp peak as observed in the other devices. In a symmetric device one would expect the transconductance of the dual-gated device to be about 10% larger than the transconductances of the top and bottom gate transistors.

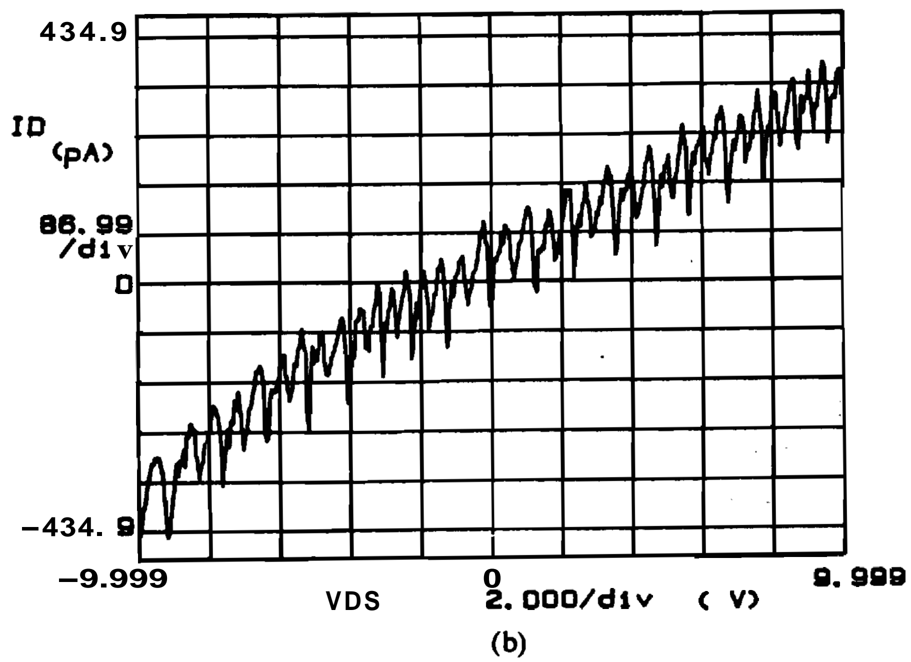
The advantages of the dual-gated device fabricated with ELO are immediately obvious upon noting the extremely low value for the back gate subthreshold slope attainable in the process. The value of approximately 150mV/dec is normal for the device structure whose gate oxide is 1500Å thick and whose channel doping is about 2-4×10^{16} /cm^3. The advantages of ELO are even more enhanced if one observes the back gate to source leakage of the SIMOX device as compared to the oxide leakage of the ELO device. The back oxide leakage currents for the SIMOX device and the ELO device are shown in fig. 5.38. It is obvious that although the SIMOX back gate is twice as thick as the ELO back gate, the leakage current through the SIMOX buried oxide is about 2-3 orders of magnitude greater than that through the ELO's buried ply-oxide. This suggests a stronger integrity for the buried oxide when using epitaxial lateral overgrowth. Another advantage of ELO towards making dual-gated devices involves the choice of the buried insulator. Since ELO involves epitaxial growth over an insulator, advanced dielectrics such as nitrided oxides can be easily used in the selective epitaxy process. This should further improve the dielectric integrity of the buried insulator in ELO. SIMOX technology falls palpably short in this regard.

5.3.3 Series Resistance Concerns

The mobility values $\mu_{p,eff}$ reported in Tables 5.7-5.9 are smaller than the values obtained in the substrate devices, except in special cases as revealed by the best values listed in the tables. The same is true of the NMOS devices presented in section 5.3.1. It is our conjecture that the lower mobility values computed throughout this chapter are a result of high source-drain series resistances, more so in the thin-film SOI devices. In Table 5.10. we list the measured resistance values of P^+ resistors on the substrate, ELO and SIMOX wafers. As can be seen, the resistance values are rather large given that the distance between the two contacts in only 20μm. The resistance is largest for the SIMOX wafers and is smallest in the substrate. This is also consistent with the fact that the



(a)



(b)

Figure 5.38 Gate to source leakages for the buried oxides in the (a) ELO-SOI and (b) SIMOX-SOI p-channel transistors

Table 5.10 Summary of Measured P^+-region Resistances on Substrate, ELO and SIMOX Wafers. L=20μm, W=14p.m

Wafer	S/D anneal temp.	Thickness	Resistance
Substrate	1000 °C	4000Å	808
SIMOX	900 °C	1400Å	450 Ω
ELO	900 °C	4000Å	175 8

SIMOX wafer has the thinnest film (1500Å) whereas the ELO films ranged in thickness from 4000Å to 5000Å. We couldn't measure the series resistance in the dual-gated structures but we expect their resistance to be larger since the films are thinner than the ELO resistance structures. The larger resistance in itself would not cause: large reductions in the mobility because the distance between the contact edge and the top channel is only 2.5 μm. The problems associated with the series resistance are inherently tied to the layout of the mask used in this work.

The mask layout of the SOI MOSFET is shown in fig. 5.39. The defined active area width on the mask in this case is 75μm, but there are only two contacts across the middle of the SOI mesa that are 10μm long and 2.5μm wide. With the resistances across the P^+ source/drain regions being as large as those listed in table 5.10, there is a substantial spreading resistance associated with the current flow along the width of the device. If the contacts were defined across the entire width of the device, then the current flow across the transistor would be uni-directional from source to drain, not withstanding the series resistance. The actual width of the current flow would then be truly represented by drawn mask width. But in the fabricated devices, the spreading resistance forces a more two-dimensional current flow as schematically illustrated in fig. 5.40. The effective width of the device would then be less than the actual drawn width of the: device, and it is this effective width that must be used in the mobility computations. It therefore stands to reason that under these conditions, applying the drawn mask width to the mobility

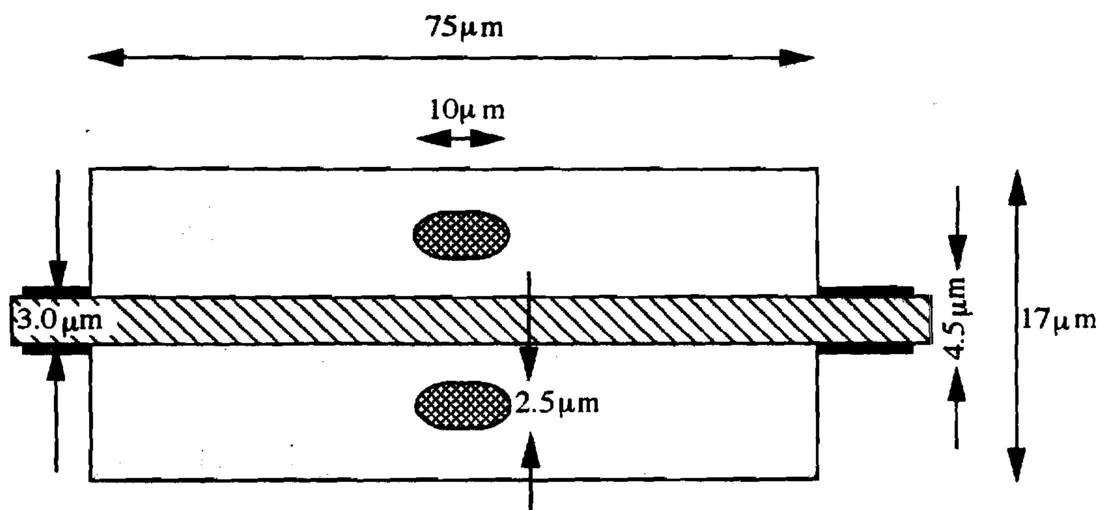


Figure 5.39 The mask layout for the dual-gated (or single-gated) SOI MOSFET

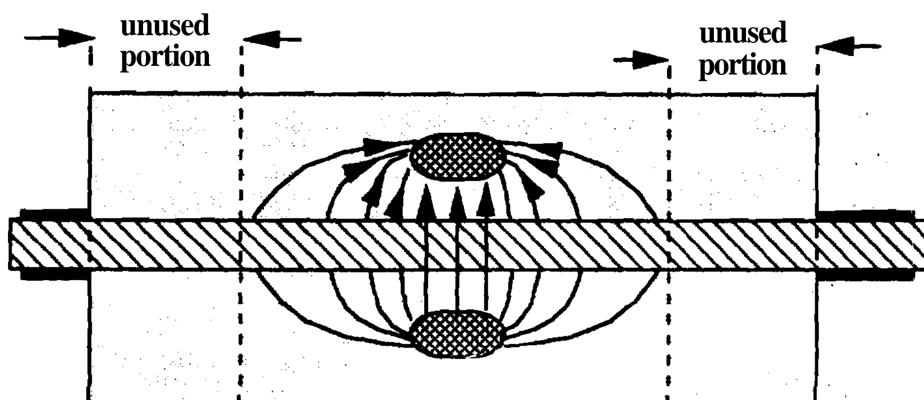


Figure 5.40 Qualitative sketch of the source to drain current contours. The current flow paths are two-dimensional due to the large spreading-resistance encountered in the devices

computations would result in an underestimated mobility value as observed in the previous two sections.

Extremely simplistic PISCES simulations of the two structures, one with the contacts as designed on the mask and the other with contacts across the entire width of the structure were carried out. The simulations suggest that the structure with the contacts defined across the width of the device, have an average resistance that is at least a factor of 3 lower than that of the structure with the smaller contacts. Alternately, the effective width of current flow in the structure with the smaller contacts is three times smaller than in the structure with the larger contacts. Therefore, in order to determine the true effective mobility, a conservative estimate for the ELO and SIMOX devices can be obtained by multiplying the mobilities listed in the tables above by a factor of 2. The mobility values of the substrate devices should also be corrected for, but the degree to which the different mobility values are corrected would depend on the resistance values measured in table 5.10. Likewise, the mobility values $\mu_{n,eff}$ of electrons determined in section 5.3.1 would also be larger than the measured values due to the two-dimensional nature of current flow in the ill-designed devices.

In order to confirm or at least lend credence to the above argument, we fabricated a simple single-gated fully-depleted ELO SOI MOSFET but reduced the active area width to 21μm. A top view of the device is shown in fig. 5.41. The contacts on this device cover a significantly larger portion of the width of the device. The output characteristics and subthreshold characteristics of the device are shown in figs. 5.42 and 5.43. The measured data are summarized in table 5.11. As can be seen in the table, the computed values of the effective mobility $\mu_{p,eff}$ devices exceed 250 cm^2/V-sec on an average and the best value obtained is almost 310 cm^2/V-sec. This confirms the excellent quality of the epitaxial lateral overgrowth SOI film.

5.4 Confined Lateral Selective Epitaxial Growth

Confined Lateral Selective Epitaxial Growth (CLSEG) is an another form of selective epitaxy in which crystal growth is confined in a pre-determined cavity defined on the wafer. In this section, the material quality of CLSEG is investigated for applications to thin-film, fully-depleted SOI MOSFETs. So far the CLSEG material has been grown to heights of 1.0μm and its material quality has been shown to be very good.

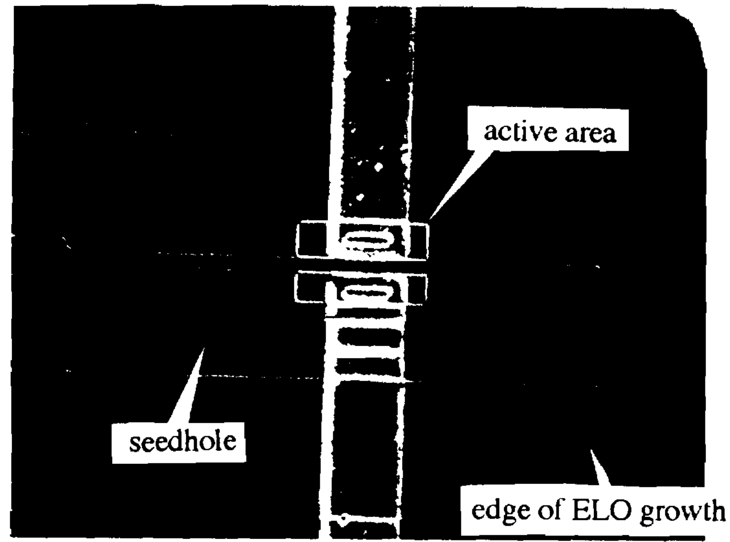


Figure 5.41 Top view of the narrow width ELO-SOI single-gated MOSFET. The narrow width structure facilitates computation of the effective mobility

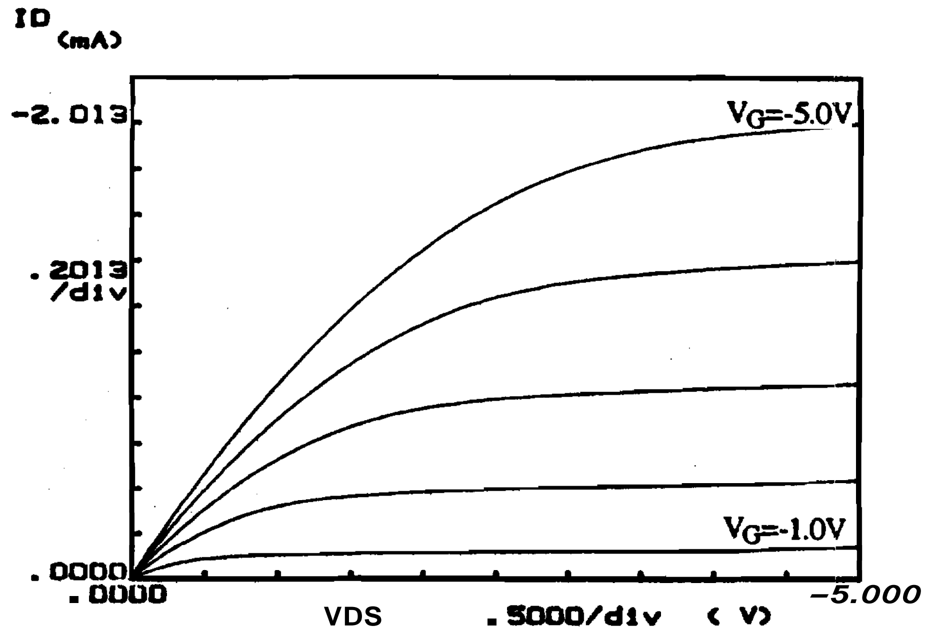


Figure 5.42 Output characteristics of a narrow width fully-depleted single-gated ELO-SOI pchannel transistor

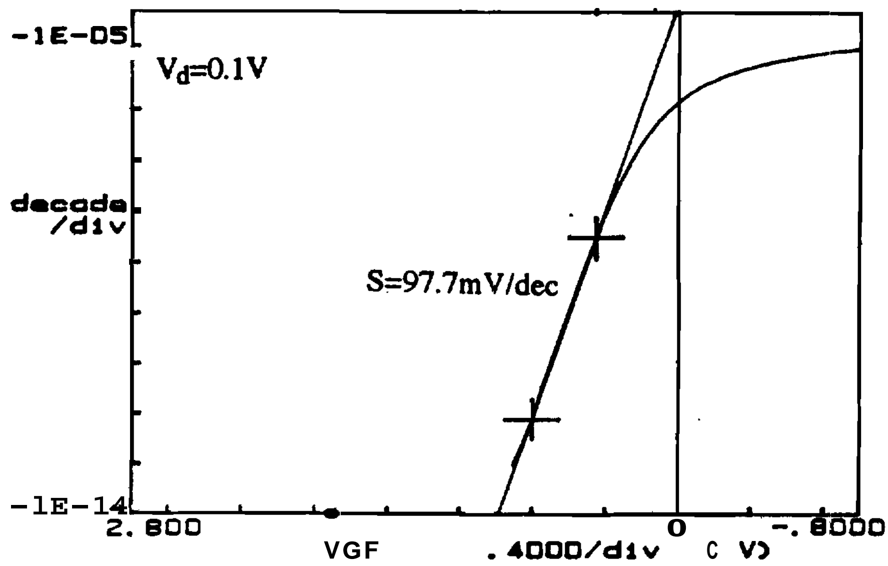


Figure 5.43 Subthreshold characteristics of the narrow-width fully-depleted single-gated ELO-SOI p-channel transistor

Table 5.11 Summary of Measured Data on Small Width Single-Gated Fully-Depleted ELO PMOS Devices. Average taken over 25 devices. L=2.4mm, $t_{ox,f}$=550Å, t_{si}=1300Å

Parameter	Average	Best
$I_{D,sat}$: V_D=V_G=-5.0V	5.3x1-$^{-5}$ A/μm	5.7x10^{-5} A/μm
V_T	0.128 V	-
S	99.9 mV/dec	97.7 mV/dec
Leakage	< 1pA	< 1pA
G_m @ V_D=-0.1V	0.63 μS/μm	0.67 μS/μm
$\mu_{p,eff}$	264 cm^2/V-sec	310 cm^2/V-sec

In this section, results from CLSEG grown in 2500Å cavities are presented for the first time. Devices fabricated in the CLSEG material include diodes, N-channel FETs and p-channel FETs. All the three devices were fabricated on three separate wafers to maintain low process complexity and to maintain a photo-resist free implant step. Once again, the NMOS process demonstrated extremely low subthreshold leakage currents but poor subthreshold slopes. However, because the subthreshold leakage is minimal, the characteristics are indicative of a good quality material. Novel dual-gated devices were also fabricated using CLSEG. As in the case of the ELO devices, CLSEG dual-gate devices also involve growth over a polysilicon gate. The CLSEG growth over a step defined inside a cavity was attempted for the first time. While the growth was successful, logistics of processing and a non-optimal mask design kept us from obtaining high-performance devices. Nevertheless, the feasibility of the concept was demonstrated.

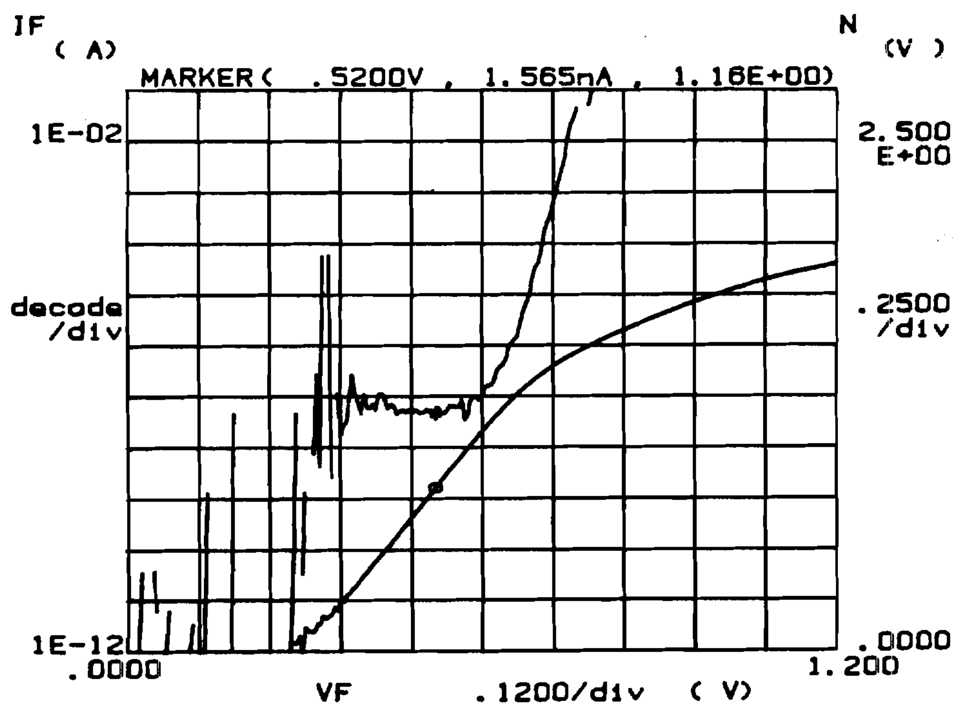
In the following sub-sections, results from CLSEG diodes, single-gated NMOS and PMOS devices and dual-gated NMOS devices are presented. The CLSEG silicon in which these devices were fabricated was only about 1500Å thick because they were thinned down after growth by a short 1-2 min CMP step using NALCO 2355 (to ensure a smooth top surface) and a post growth oxidation and strip. The CMP step did not produce any non-uniformities in the as-grown CLSEG layers, because of the short duration of the planarization process. The excellent uniformity of CLSEG was maintained across the wafer. This is a major advantage of CLSEG, as it avoids the non-uniformity concerns of chemical mechanical planarization through the definition of a pre-determined cavity with excellent uniformity (5%) across the wafer.

5.4.1 Diodes

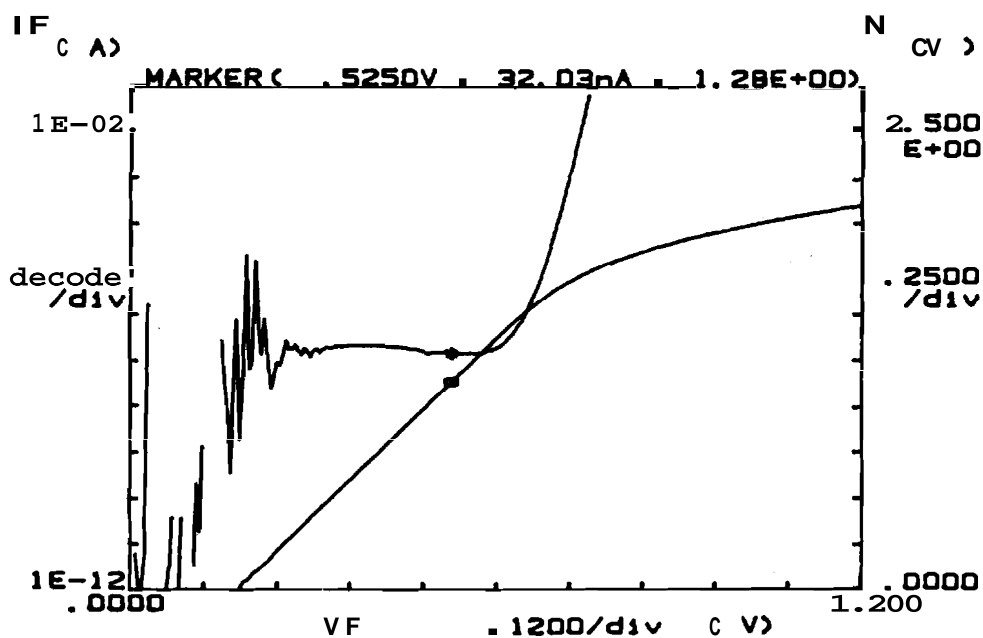
The diodes were fabricated using a photoresist free implant process in which thermal oxide was used as a mask during the arsenic implant. Typical diode characteristics are shown in fig. 5.44. The diodes demonstrated extremely low leakage currents which were below the measurement sensitivity (< 1pA) of the HP 4145B. The best ideality factor obtained was 1.16 and an average value of 1.28 was measured across 25 diodes. The high ideality factors are possibly the artifact of the large series resistance that exists in the device, which is inherent to the nature of the thin-film SOI structure. The large series resistance is also evident by the low voltage (0.5V) at which the curve begins to bend over and saturate. The low junction leakage currents, however, prove the excellent quality of the CLSEG material. Table 5.12 summarizes the measured device parameten.

Table 5.12 Summary of Measured Data on Thin-Film CLSEG Diodes

Parameter	Average	Best
Ideality Factor η	1.28	1.16
Leakage @ -2.5V	< 1pA	< 1pA



(a)



(b)

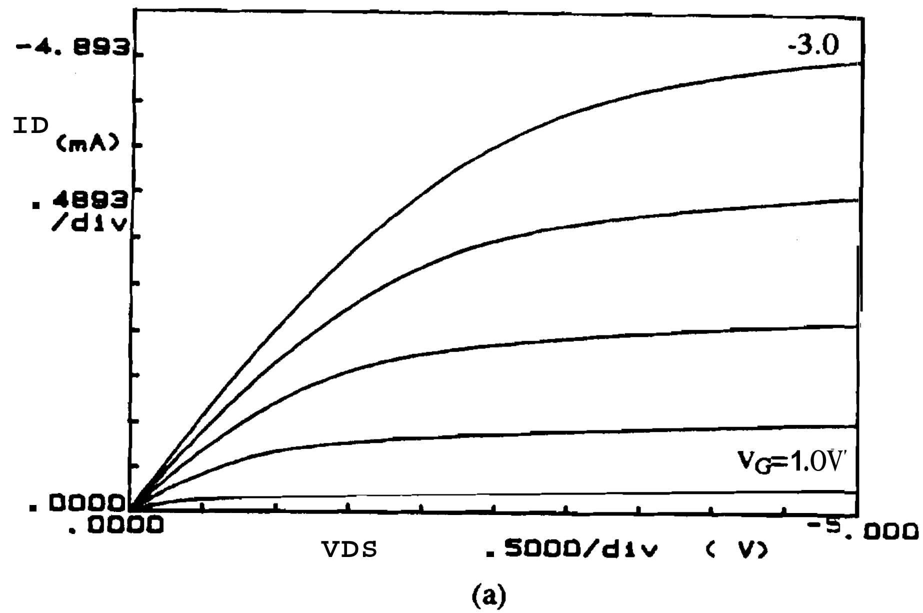
Figure 5.44 Forward characteristics of a thin-film CLSEG diode (a) the best device and (b) the average device

5.4.2 Single-Gated NMOS and PMOS Devices

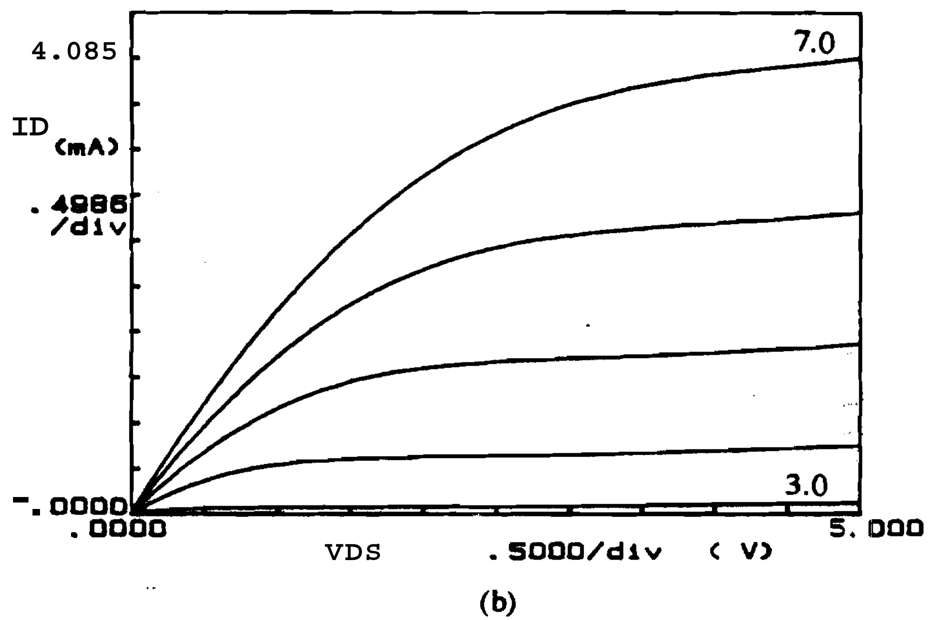
The output characteristics and the subthreshold curves for the representative NMOS and PMOS devices are depicted in figs. 5.45 and 5.46 respectively. The transconductance of the NMOS and PMOS device are shown in fig. 5.47. Tables 5.13 and 5.14 summarize the measured data on the CLSEG MOSFETs. As is evident from the tables and the figures, excellent device characteristics were obtained for the CLSEG MOSFETs. The NMOS device again demonstrates poor subthreshold slopes although the subthreshold leakages were consistently very low. The subthreshold characteristics of the NMOS device show a discernible kink just like the single gated ELO NMOSFETs of section 5.3.1. This could again be indicative of some sort of an edge leakage problem, either due to the nature of the mesa-isolated structures or simply an inadequate boron threshold adjust profile. Isolated devices were however found across the wafer with significantly better subthreshold slopes such as shown in fig. 5.48. This proves that the bad subthreshold characteristics are not due to poor material or surface properties, but due to a non-optimum process design for the NMOS devices. Moreover the PMOS devices showed very good subthreshold slopes that are comparable to those obtained in the ELO

Table 5.13 Summary of Measured Data on Thin-Film Fully-Depleted CLSEG PMOS Devices. Average taken over 20 devices. $L=2.2\mu m$, $t_{ox,f}=550Å$

Parameter	Average	Best
$I_{D,sat}$: V_D=-5.0, V_G=-2.0V	$4.42x10^{-5}$ A/µm	$6.0x10^{-5}$ A/µm
S	110 mV/dec	99 mV/dec
Leakage	15 pA	1 pA
V_T	2.08 V	-
G_m @ V_D=-0.1V	0.65 µS/µm	0.69 µS/µm
$\mu_{p,eff}$	238 cm^2/V-sec	250 cm^2/V-sec

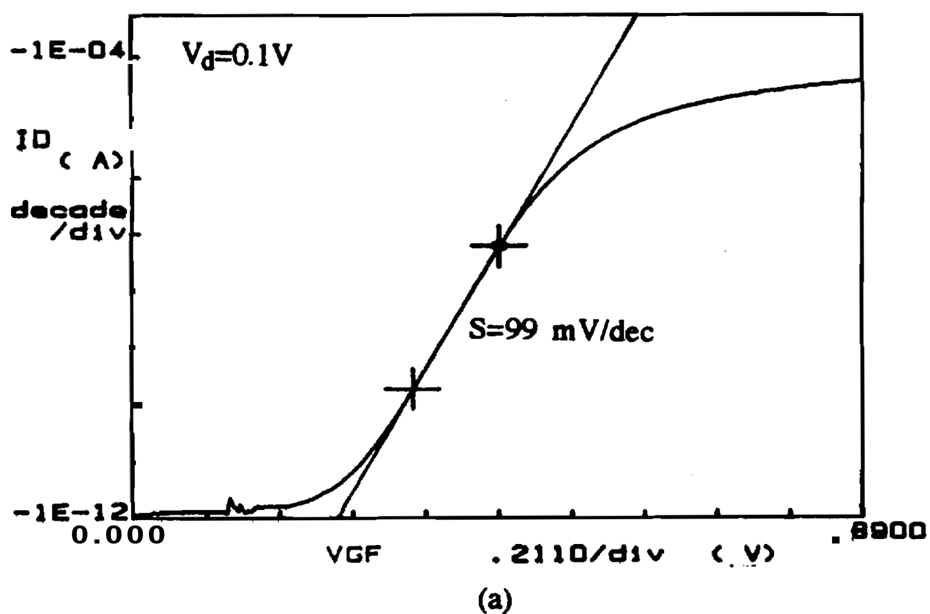


(a)

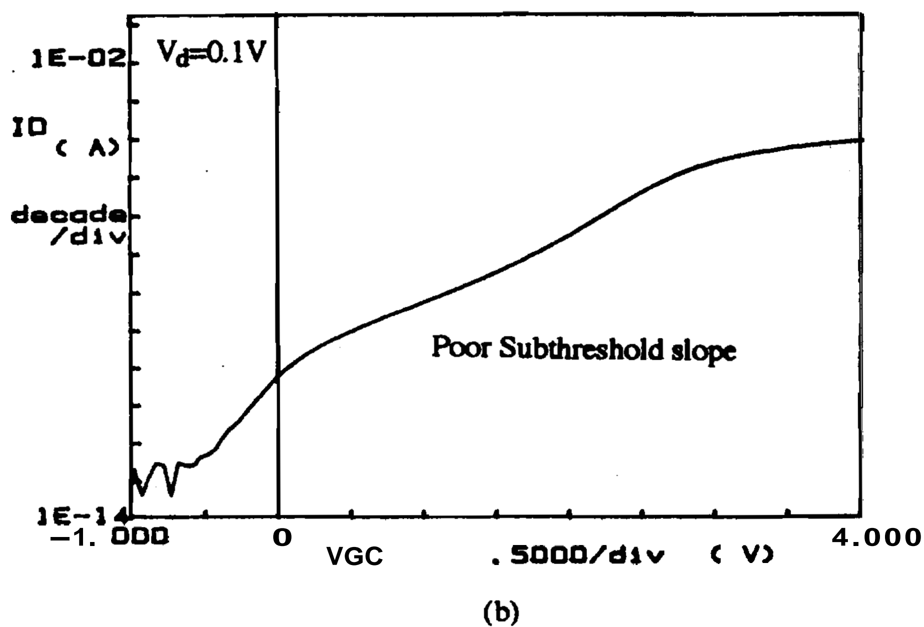


(b)

Figure 5.45 Output characteristics of a thin-film fully depleted (a) p-channel MOSFET and (b) n-channel MOSFET fabricated in CLSEG

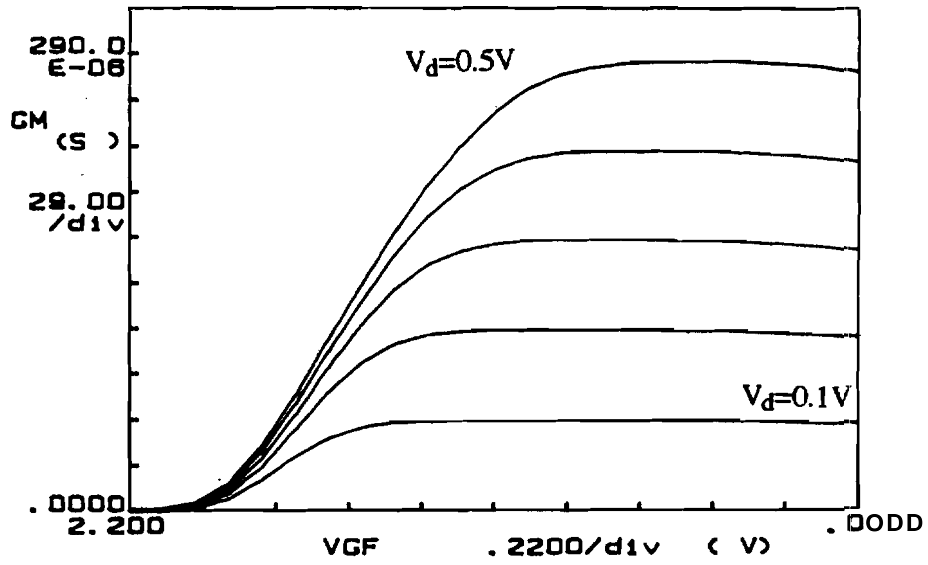


(a)

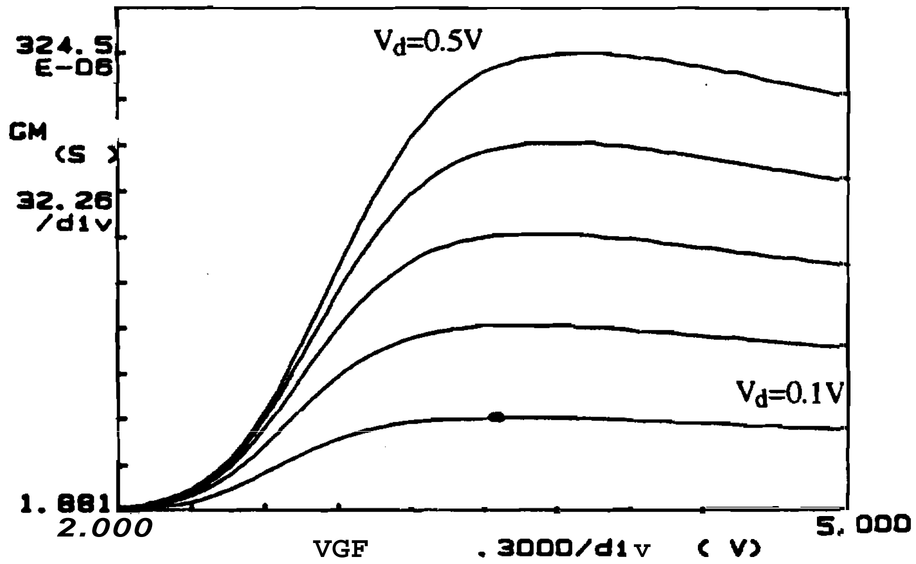


(b)

Figure 5.46 Subthreshold characteristics of a thin-film fully depleted (a) p-channel MOSFET and (b) n-channel MOSFET fabricated in CLSEG

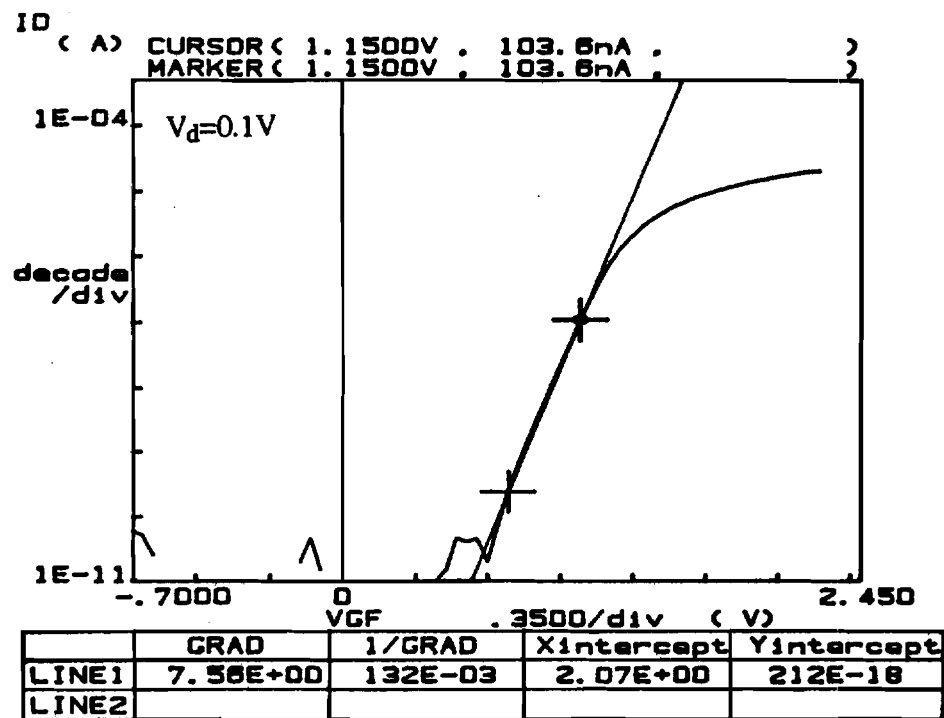


(a)



(b)

Figure 5.47 Transconductance curves for a thin-film fully depleted (a) p-channel MOSFET and (b) n-channel MOSFET fabricated in CLSEG



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	7.56E+00	132E-03	2.07E+00	212E-18
LINE2				

Figure 5.48 Subthreshold characteristics of a thin-film fully depleted SOI n-channel MOSFET fabricated in CLSEG and exhibiting a significantly better subthreshold slope

Table 5.14 Summary of Measured Data on Thin-Film Fully-Depleted CLSEG NMOS Devices. Average taken over 20 devices. $L=2.6\mu m$, $t_{ox,f}=600Å$

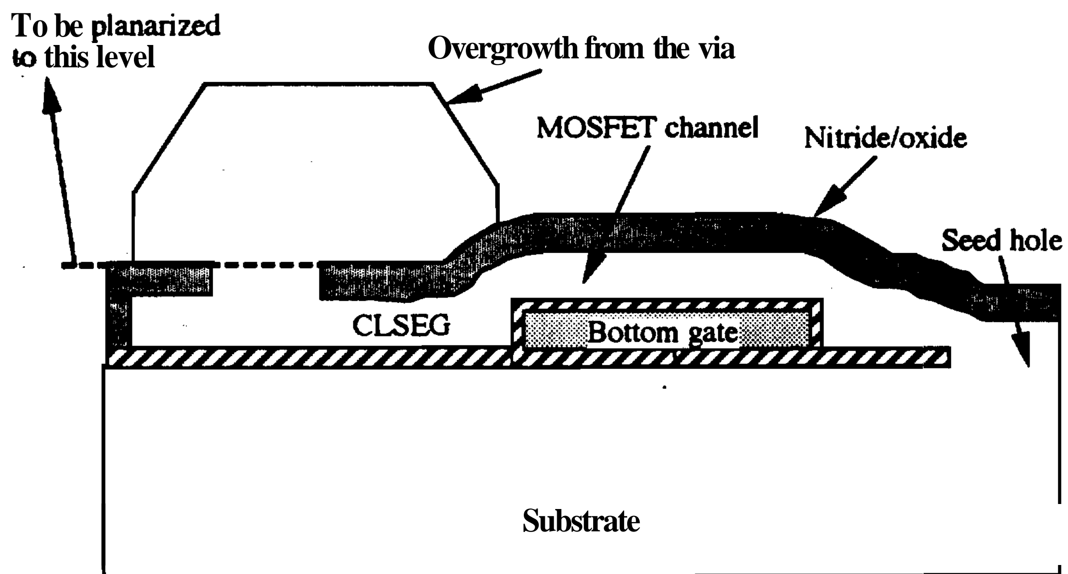
Parameter	Average	Best
: $V_D=4.0V$, $V_G=7.0V$	$6.8x10^{-5}$ A/μm	$7.7x10^{-5}$ A/μm
S	-	132 mV/dec
Leakage	5pA	1pA
V_T	2.5 V	
G_m @ $V_D=0.1V$	0.89 μS/μm	1.2 μS/μm
$\mu_{n,\,eff}$	429 cm^2/V-sec	465 cm^2/V-sec

and SIMOX devices of the previous section. Large mobility values were obtained in the thin-film CLSEG material. It should be reiterated that this is the first time electron and hole mobility values have been reported for ultra-thin film CLSEG material.

5.4.3 Dual-Gated CLSEG NMOS Devices

The successful fabrication of the dual-gated CLSEG device was constrained by inherent processing difficulties due primarily to a lack of foresight when designing the masks. The problems associated with fabricating the dual-gated devices did not result from difficulties in the selective epitaxy process, but rather from difficulties encountered in the post-epi growth processing. Epitaxial growth was typically of excellent quality as evidenced by the observation of extremely straight growth fronts and the emergence of well-faceted ELO from cavity vias. In order to explain the difficulties involved with the post-growth processing of the CLSEG wafers, a typical cross-section of a CLSEG dual-gated device is shown in fig. 5.49. Also depicted in the figure is a schematic sketch of

(a)



(b)

Figure 5.49 A dual-gated CLSEG structure immediately following confined epitaxial growth. (a) a focused-ion-beam cross-section of the dual-gated structure and (b) a schematic crosssection indicating the required level of planarization

the structure. In most cases, the nucleation emerging from the via holes grew well over the bottom gate [3].

In order to fabricate the dual-gated structure, the overgrowth from the via holes must be planarized down to the level indicated in fig. 5.49 (b). It is not enough simply to remove the silicon from over the bottom gale region, because then there would exist regions of unetched nitride under the overgrown silicon to the left of the bottom gate in the figure. The source/drain regions cannot be implanted in this case. Since the level of the cavity over the bottom gate is higher than the level to which the silicon must be planarized, the nitride layer that defines the cavity over the bottom gate: (this is also the channel region if the MOSFET) is removed and the underlying epitaxial silicon is exposed to the planarization. Once this stage is reached it becomes extremely hard to control the planarization process [4]. and the epitaxially grown silicon often gets over-etched. Alternate schemes to remove the overgrowth using dry SF_6 etching or a wet KOH etch did not provide any positive results either.

The above structural difficulties associated with dual-gated device processing using CLSEG, highlights the importance of using a recessed bottom gate. Once the bottom gate is planar with the field oxide, CLSEG growth is simple and the devices can be fabricated in like manner as the single gated devices. Despite the processing problems, a few dual-gated CLSEG devices did work and their characteristics are presented in figs. 5.50-5.52. The subthreshold characteristics and the computed mobility values were extremely poor, probably due to the extremely non-uniform epitaxial silicon SOI overlayer. As an example depicting the non-uniformity of the overlayer, fig. 5.53 depicts the transconductance of the top gate with the bottom gate groundled. Two peaks are evident in the transconductance curve indicating the presence of two devices in parallel with different threshold voltages!

[3]A majority of the epitaxial growth on the dual-gated CLSEG wafers were carried out during a period of time when the epitaxial reactor was extremely erratic in its growth rate. Consequently, the overgrowth emerging from the vias were often of gargantuan proportions.

[4]One must note that there is no etch-stop in this planarization process, and the planarization must be controlled manually. This is extremely hard to do given the non-uniform and erratic etch rates of the CMP system.

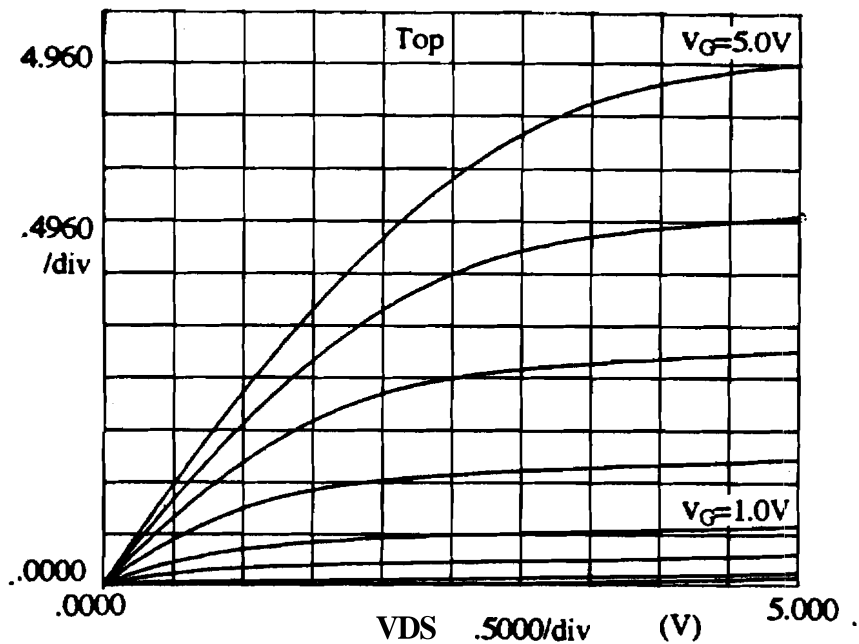


Figure 5.50 Output characteristics of the thin-film fullydepleted CLSEG-NMOS transistor under top gate control

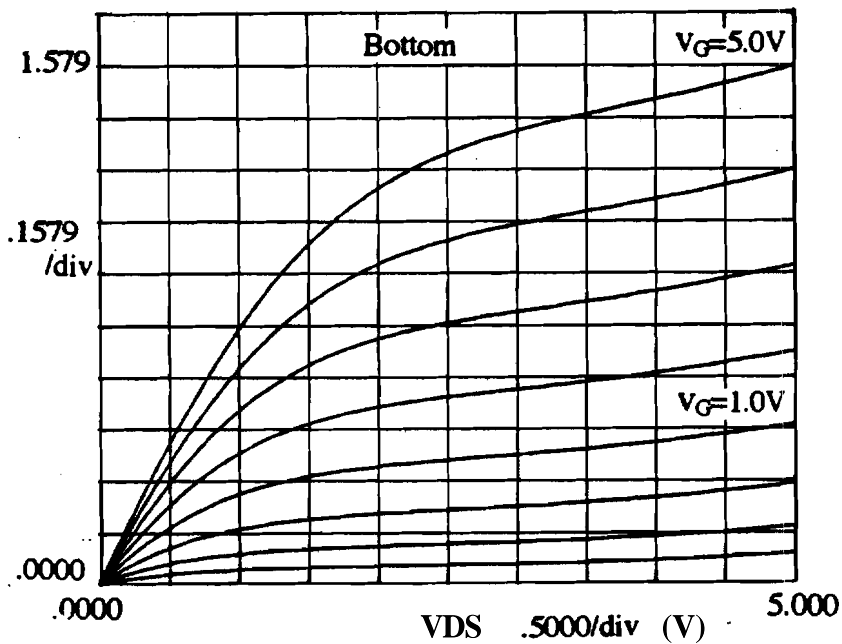


Figure 5.51 Output characteristics of the thin film fully-depleted CLSEG-NMOS transistor under bottom gate control

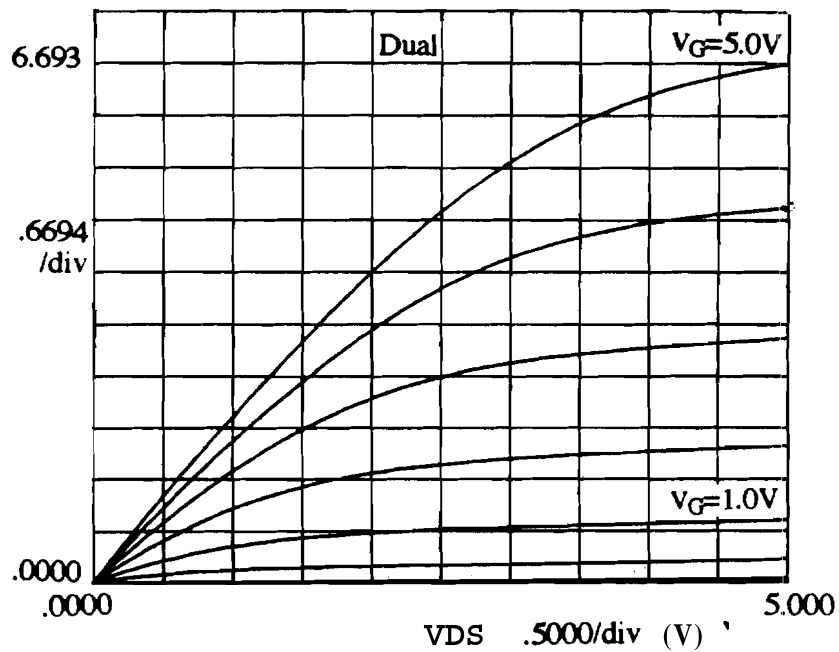


Figure 5.52 Output characteristics of the fully-depleted dual-gated CLSEG-SOI n-channel transistor under dual-gate control

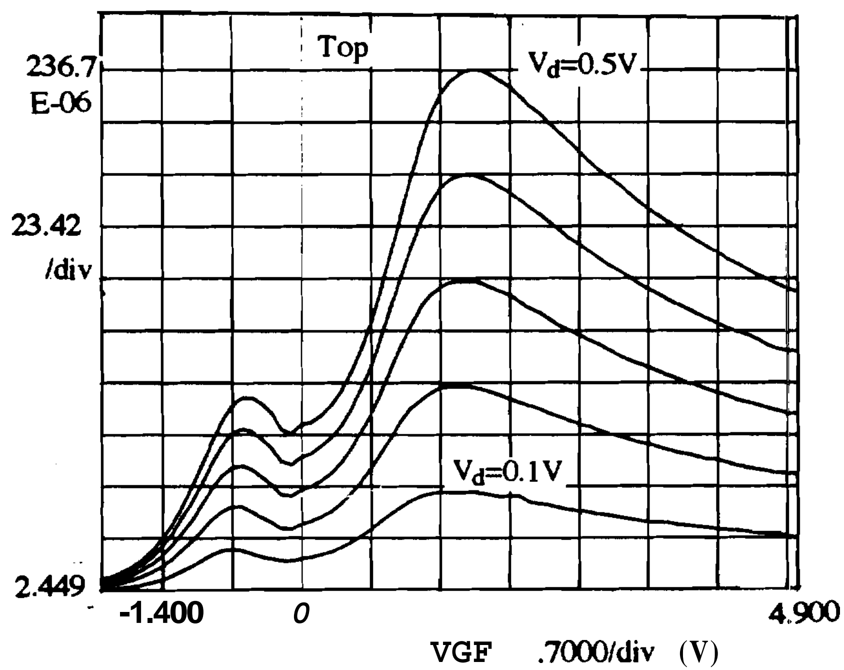


Figure 5.53 Transconductance curves of the top gate in a dual-gated n-channel device fabricated in CLSEG. The bottom gate is grounded

5.5 Conclusions

N-channel and P-channel devices were fabricated in ELO and CLSEG material. Simultaneously, device were fabricated in substrate silicon and commercially available SIMOX material. The results indicated that the SOI layers formed by selective epitaxy are at least as good if not better than the SIMOX material.

Thin-film fully-depleted SOI MOSFETs were fabricated by CLSEG for the first lime. Although the dual-gated devices did not work very well, the results from the single gated devices pointed to material of excellent quality. These results were vindicated by measurements on diodes fabricated in CLSEG material. The diodes showed very low leakage currents. However the measured ideality factors were larger than expected due to the inherently large series resistances present in the CLSEG diode structure.

Experimental evidence validating the theories regarding volume inversion presented in Chapter 3 were provided by measurements on asymmetric dual-gated devices fabricated by epitaxial lateral overgrowth.' The results denied the existence of a 50-75% enhancement in the current of fully-depleted dual-gated devices. The measured enhancements, when compared at constant gate voltages above threshold, were barely 15%. This enhancement would be further reduced if the threshold voltages of the individual gates were measured with the other gate maintained close to flat-band conditions.

CHAPTER 6
GENERATION LIFETIME MEASUREMENTS IN THIN-FILM SILICON-ON-INSULATOR (SOI) MOSFETS

The generation lifetime is a very important device parameter. The switching time of bipolar devices, the leakage currents of p-n junction diodes and charge-coupled devices (CCDs), and the refresh time of dynamic RAMs all depend on it. The generation lifetime of the semiconductor material depends directly on such parameters as the concentration of deep-levels which may result from foreign impurities or crystal defects. Therefore, the generation lifetime can and is often used as a process control monitor. It is also a very good figure of merit to compare the properties and the quality of semiconductor materials. It is therefore important to get an accurate value of the generation lifetime, τ_g.

In this chapter, we describe a new technique to determine generation lifetimes in thin-film, partially depleted or fully depleted SOI MOSFETs. In section 6.1, the basic concepts of generation lifetimes are established and the widely used techniques for determining generation lifetimes in bulk silicon MOSFETs are described. The differences in thin-film SOI MOSFETs and the review of measurements made on SOI devices are presented in section 6.2. Finally in section 6.3 we describe the new linear sweep technique applicable to thin-film SOI MOSFETs and present the experimental results obtained on thin-film fully-depleted devices fabricated on SIMOX material.

6.1 The Generation Lifetime τ_g

The generation lifetime (τ_g) is the average time required to generate an electron-hole pair (e-h pair) in a depleted region of the semiconductor device. The generation

lifetime is applicable in regions of the device where there is a paucity ot'caniers, such as in the space charge region of a reverse-biased junction.

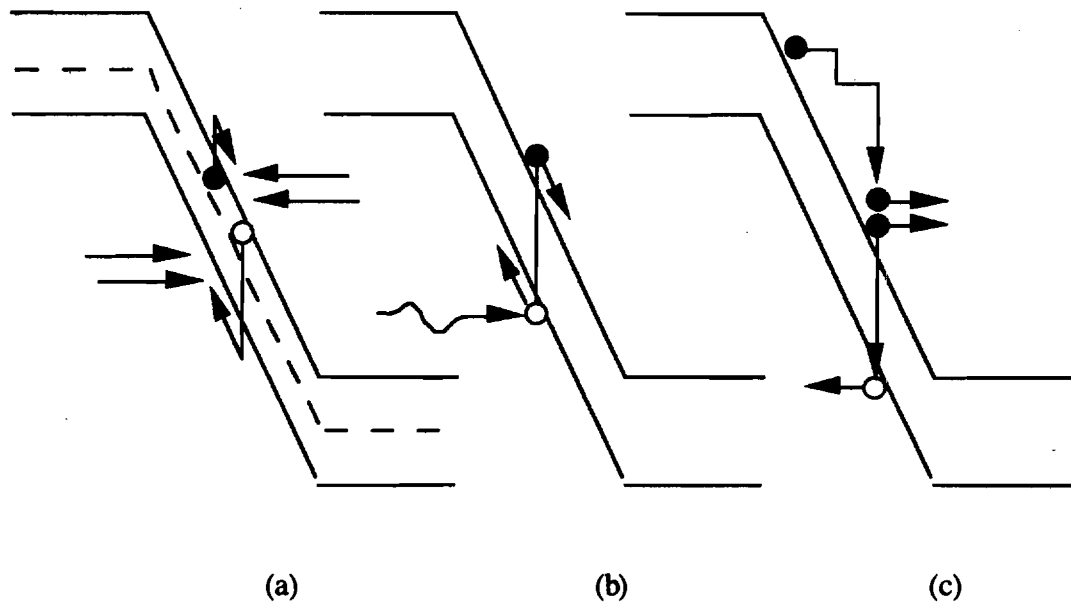


Figure 6.1 (a) Schockley-Read-Hall generation (b) optical and (c) impact ionization electron-hole pair generation

The generation mechanisms in a semiconductor are schematically illustrated in figure 6.1 [1]. The Schockley-Read-Hall (SRH) process of figure 6.1(a) is the most important generation process in silicon under dark, low electric field conditions. The thermal generation of e-h pairs proceeds via intermediate energy levels for most semiconductors. The radiative generation mechanism (Fig. 6.1(b)) involves the optical generation of e-h pairs using a photon with energy greater than the bandgap energy of the semiconductor. The optical or radiative process is absent in the dark, since the black body radiation from the surroundings is negligible under these conditions. Finally, the inverse-Auger generation mechanism (better known as avalanche multiplication) involves

three carriers. A high energy electron loses its energy by creating an e-h pair. Avalanche multiplication is dominant only under high electric field conditions and can be neglected at low fields. The generation lifetime in silicon is essentially determined by thermal generation processes given by the SRH theory and the remainder of this chapter deals with thermal generation alone.

The generation rate is defined as the rate at which carriers are generated in a given volume of the semiconductor. From the Schockley-Read-Hall (SIRH) theory, the generation rate can be expressed as,

$$G = \frac{(n_i^2 - np)}{[\tau_{po}(n + n_1) + \tau_{no}(p + p_1)]} \tag{1}$$

where n_i is the intrinsic carrier concentration, n is the electron concentration, p is the hole concentration, n_1 and p_1 are trap related parameters given by,

$$n_1 = n_i \exp[\frac{E_T - E_i}{kT}] \; ; \; p_1 = n_i \exp[\frac{-(E_T - E_i)}{kT}] \tag{2}$$

where τ_{no} and τ_{po} are the respective electron and hole lifetimes. Under reverse bias conditions, in a depleted region of the device, the mobile carrier concentration is neglected and,

$$G = \frac{n_i}{\tau_g} \tag{3}$$

where

$$\tau_g = \tau_{po}\exp[\frac{E_T - E_i}{kT}] + \tau_{no}\exp[\frac{-(E_T - E_i)}{kT}] \tag{4}$$

This is the most general expression for the generation lifetime and will be used later in the chapter during the development of the new generation lifetime measurement technique.

Any generation lifetime measurement scheme requires that (i) the device be placed in non-equilibrium (deep depletion). This involves splitting the minority and majority quasi-fermi levels (ii) an excess generation width be created which attempts to bring the device back to steady-state or equilibrium through excess carrier generation and

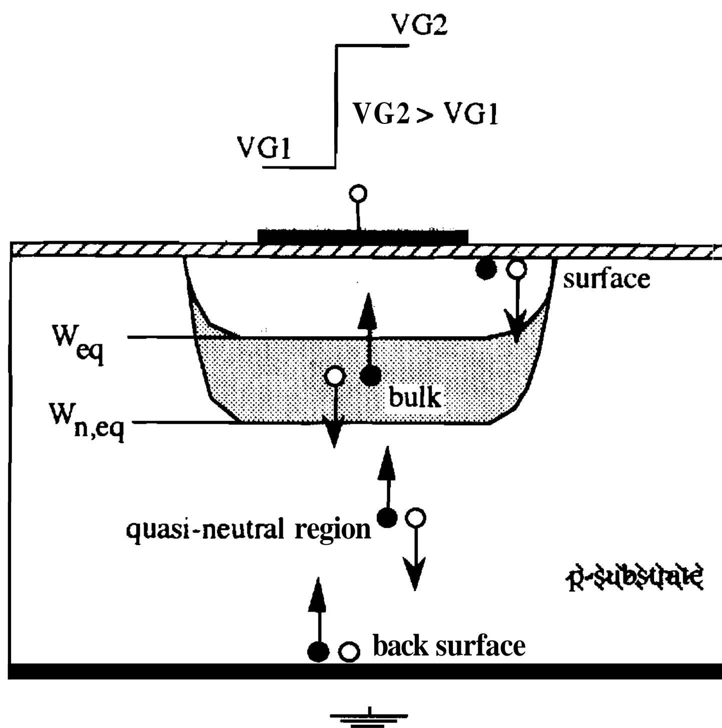
(iii) the generated charge be monitored through the choice of appropriate test structures and instruments.

In bulk silicon, the MOS capacitor is the most widely used device structure [3] and the measured capacitance is used to monitor the generated charge. The pulsed MOS-C lifetime measuring technique is the most popular technique to measure τ_g [4-8]. The method was first proposed by Jund and Poirier [4] and it involved a capacitance-time (C-t) transient measurement following an accumulation to inversion pulse. This technique was subsequently analyzed in great detail by Zerbst [5] and Heiman [6]. Various interpretational and experimental variations to this basic technique have been proposed and a review of the various methods can be found in [7] and [8]. Figure 6.2(a) illustrates the experimental conditions and figure 6.2(b) depicts the experimental C-t response and its related Zerbst plot which determines the value of τ_g. The MOS capacitor is pulsed into deep depletion and the capacitance of the device is monitored as a function of time as shown in figure 6.2(b). The inversion carriers cannot be generated immediately in response to the applied pulse. Consequently, the device is forced into non-equilibrium (deep depletion). Eventually, thermal generation within the depleted volume of the semiconductor begins to generate the requisite inversion charges to balance the charge added to the gate and the device relaxes back to equilibrium. In the non-equilibrium condition the depletion region is larger that its equilibrium value and consequently the measured capacitance is lower than the value at equilibrium. The larger depletion width provides the excess generation width which results in the excess generation that drives the device back to equilibrium. As the device approaches equilibrium, the depletion region shrinks as is evidenced by an increasing capacitance.

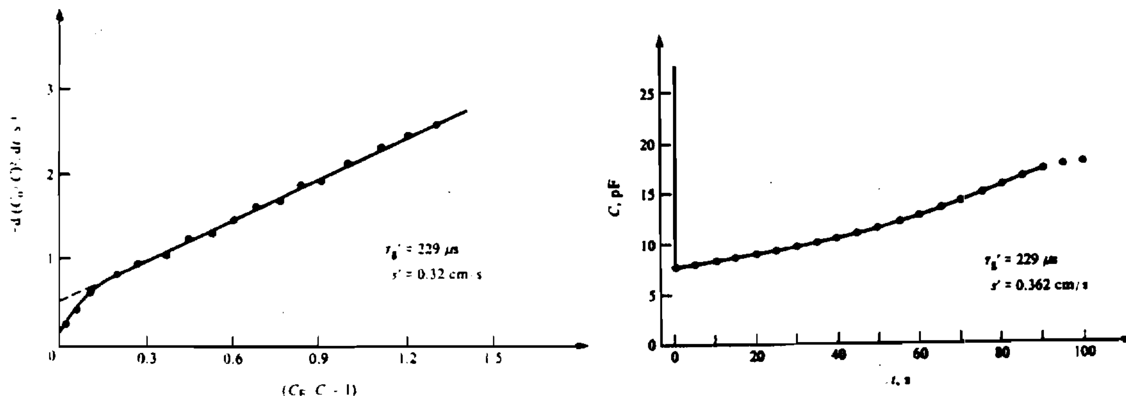
The capacitance relaxation in figure 6.2(b) is determined solely by thermal electron-hole pair generation. The e-h pair generation rate consists of both space-charge generation and quasi-neutral generation components [7] and is given by,

$$\frac{dQ_n}{dt} = \frac{-q n_i (W - W_f)}{\tau_g} - \frac{q n_i s_g A_s}{A_G} - q n_i s_{eff} = \frac{-q n_i (W - W_f)}{\tau_g'} - q n_i s_{eff} \qquad (5)$$

s_{eff} is the effective surface generation velocity and contains both the front and back interface generation terms in addition to the width-independent quasi-neutral generation parameters. Similarly τ_g' is the effective generation lifetime and contains both bulk generation (space charge region generation under the gate) term and the width-dependent



(a)



(b)

Figure 6.2 (a) Experimental conditions for the pulsed MOS C-t transient measurement and (b) Experimental C-t response of an MOS-C and its Zerbst plot [7,8]

edge generation component characterized by a surface generation velocity. W is the time-dependent depletion region width and W_f is the final equilibrium depletion region width. The term $(W-W_f)$ determines the 'effective generation width', which is the region of the semiconductor that actually generates camers. It is well known that using W for the effective generation width overestimates the generating volume because there is a significant region near the surface of the semiconductor that does not generate any carriers. Similarly, $(W-W_f)$ underestimates the effective generation width. This is made clear in figure 6.3 which qualitatively depicts the energy bands in a p-type semiconductor under deep-depletion conditions [9,10]. Rabani and Lamb [9] made a first order correction to the effective generation width as shown in the figure, The effective generation width can also be expressed as [1I]

$$W_{eff} = (W - \xi W_f) \quad \text{where } 0<\xi<1 \tag{6}$$

The major uncertainty in estimating the true generation width arises; from a lack of knowledge of the quasi-fermi Levels during the transient. Other expressions have been derived for a more accurate determination of the effective generation width [10], but typically $(W - W_f)$ has been accepted as a reasonable approximation in bulk devices.

Relating the depletion width W to the measured capacitance C, one can derive the following final expression,

$$-\frac{d}{dt}\left(\frac{C_{ox}}{C}\right)^2 = \frac{2n_i}{\tau_g' N_A}\frac{C_{ox}}{C_f}\left(\frac{C_f}{C}-1\right) + \frac{K_{ox}}{K_s}\frac{2n_i s_{eff}}{t_{ox} N_A} \tag{7}$$

This equation is the basis of the Zerbst plot. $-\frac{d}{dt}\left(\frac{C_{ox}}{C}\right)^2$ is plotted versus $\left(\frac{C_f}{C}-1\right)$ and τ_g' is determined from the slope as shown in figure 6.2(b).

A non-pulse linear sweep technique for bulk MOS capacitors [12] has also been developed. This technique promises interpretational simplicity, ease of implementation, and does not require differentiation of the experimental data. In the linear sweep technique, a linear ramp instead of a pulse, is used to drive the device into non-equilibrium. If the linear ramp applied to the gate of the MOS capacitor is very slow,

$$W_{eff} = \sqrt{W^2 - W_f^2/2} - \frac{W_f}{\sqrt{2}}$$

Figure 6.3 Energy band structure of a p-type MOS capacitor at (a) equilibrium inversion and at (b) non-equilibrium deepdepletion

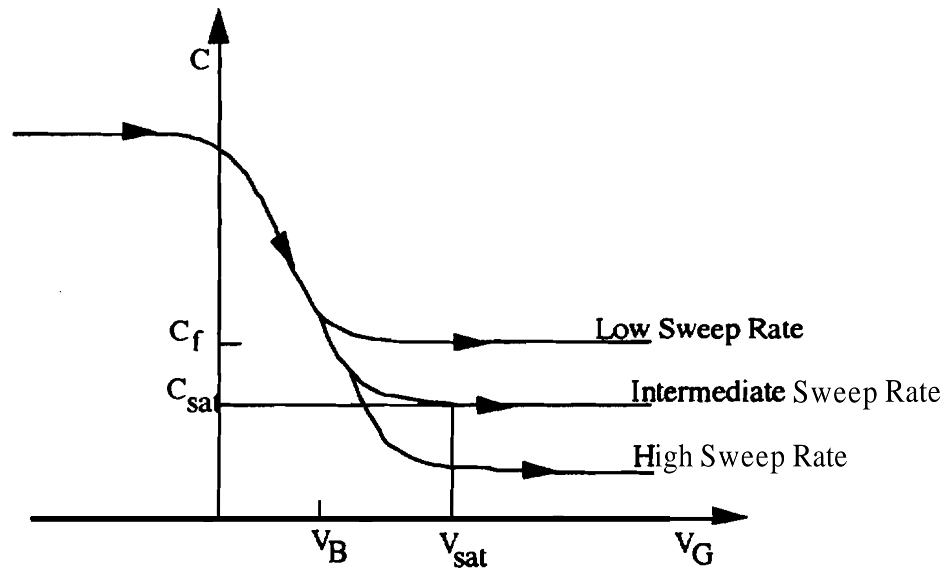


Figure 6.4 Equilibrium inversion curve at extremely slow ramp rates and deep depletion saturation curves for higher sweep rate

then the generation of carriers in the MOS-C can at all times balance the rate at which charge is added to the gate. The inversion layer can then be formed in response to the ramp and the measured C-V curve traces the equilibrium value. As the ramp rate is increased, the generation rate cannot form the inversion layer fast enough and the device enters non-equilibrium. In this condition the measured capacitance is smaller than the equilibrium value. If the ramp is continuously maintained, eventually a stage is reached when the excess generation rate equals the rate of change of charge on the gate (determined by the ramp rate) and the device reaches a quasi-steady-state situation. The depletion region width saturates and the measured capacitance also saturates, albeit at a lower value. This is depicted in figure 6.4. The measurement can be repeated for different ramp rates and the different saturated capacitance values can be obtained. Under the saturated condition, the rate of change of charge on the gate ($C_{ox}R$) exactly balances the rate at which charge is generated in the depleted semiconductor region $\frac{q n_i}{\tau'_s}(W_{sat} - W_{eq})$. W_{sat} is the depletion width at the saturated condition, and W_{eq} is the depletion width at equilibrium. Again the excess depletion width is chosen as the

effective generation width. Equating these two terms, and expressing the depletion width in terms of the measured capacitance one can readily arrive at,

$$R = \frac{q K_s \varepsilon_o n_i}{C_{eq} C_{ox} \tau_g'} \left(\frac{C_{eq}}{C_{sat}} - 1 \right) \quad (8)$$

Then the linear slope of the R v/s $\left(\frac{C_{--}}{} - 1 \right)$ plot determines the effective generation lifetime τ_g'.

The gate-controlled diode (GCD) is the second most commonly used device structure to measure the generation lifetime [13]. A cross-section of the device is shown in figure 6.5(a). A reverse bias applied to the diode is used to place the device in non-equilibrium. The diode current (instead of a capacitance) is used to monitor the charge generation in the device. For a given diode bias, the current is monitored as a function of the gate bias. The measurement procedure is depicted in figure 6.5(b). When the gate is in accumulation, the measured reverse-bias current is solely the reverse-biased junction leakage current. There is no surface or bulk generation under the gate. When the gate is biased in depletion then there is a surface and bulk contribution to the measured drain current as shown in figure 6.5(b). As the gate bias increases with the diode still biased in depletion, the diode current also increases due to the increased bulk generation associated with the increased depletion width. Finally, when the surface is inverted, the surface generation term drops and the measured diode current becomes a constant and is the sum of the bulk generation under the gate and the diode leakage current. As the diode bias is increased, the bulk generation component also increases because the maximum inversion depletion width increases with increasing diode bias.

$$I_{d_{bulk}} = \frac{q A_d n_i}{\tau_g'} (W_{n,eq} - W_{eq}) \quad (9)$$

where $W_{n,eq}$ is the non-equilibrium depletion layer width dependent on the diode bias and W_{eq} is the equilibrium depletion width when the diode voltage is zero. The effective generation lifetime τ_g' can be determined from the above expression.

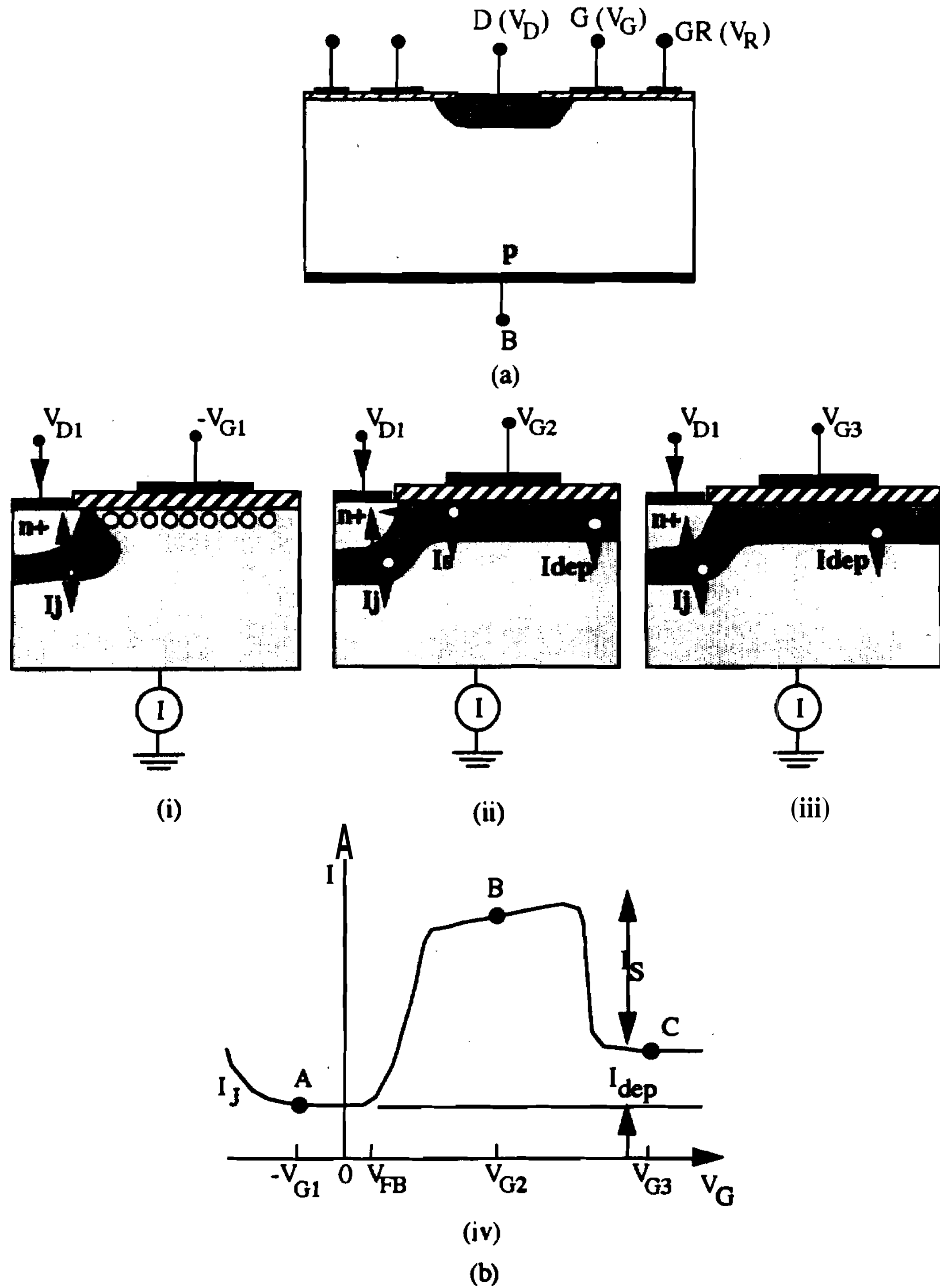


Figure 6.5 (a) Schematic cross-section of a gate controlled diode (GCD) and (b) a GCD in (i) accumulation, (ii) depletion and (iii) inversion ; (iv) shows the current voltage characteristic with points A, B and C corresponding to (i), (ii) and (iii)

6.2 τ_g Measurement in Thin-Film SOI MOSFETs

The two major electrical lifetime measurement schemes in bulk devices were discussed in the above section. In addition there are optical lifetime measurement

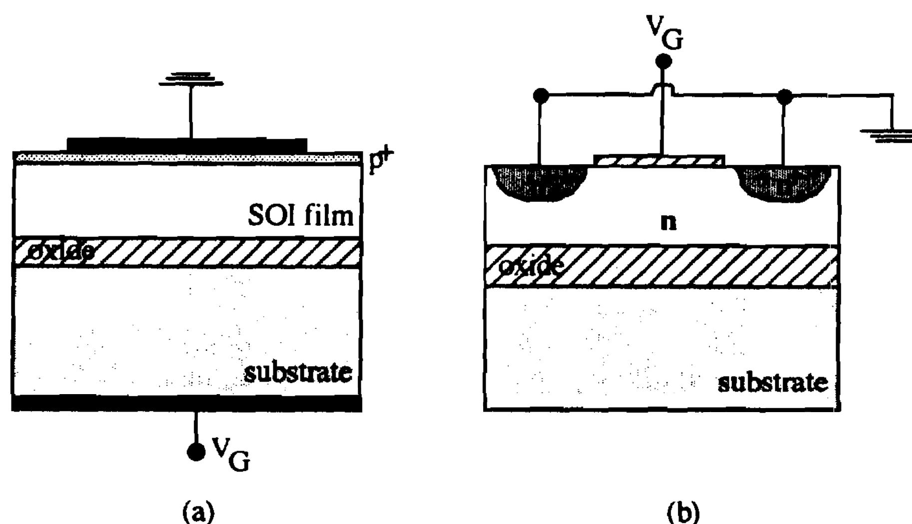


Figure 6.6 (a) The vertical inverted MOS capacitor on SOI material and (b) lateral MOS capacitor on SOI substrates. The n+ junctions could reach through to the bottom oxide interface

techniques such as the photoconductive decay technique [14] and the photoluminescence (PL) decay technique [15]. The optical measurement techniques are extremely useful because they are in general non-contacting in nature. However all optical schemes essentially create excess electron-hole pairs and therefore they measure the excess carrier lifetime or the minority carrier lifetime (recombination lifetime). The optical excitation source is abruptly terminated and the excess carrier decay rate is measured to determine the recombination properties or the recombination lifetime. Since we are: dealing with generation lifetimes in this chapter, we shall concentrate only on the electrical schemes to measure the generation lifetime.

The major difference between bulk semiconductor devices and SOI devices, apart from the presence of the buried oxide, is the ultra-thin nature of the overlying silicon film. However initial characterization schemes on SOI substrates were directly adapted from the techniques used in bulk MOSFETs. The SOI films studied were: thick (1.0 - 2.0 μm) so that conventional 'bulk' devices could be fabricated in them. For all practical purposes the devices behave like their bulk counterparts. Pulsed MOS-C measurements such as described in the previous section were made on inverted MOS capacitors as schematically illustrated in figure 6.6(a) [16-19]. Lateral MOS capacitors (fig. 6.6(b))with reach-through diffusions were also used in pulsed C-t transient measurements [20]. Capacitance measurements typically require extremely large area devices so that the measured capacitance is large enough for accurate measurements. Moreover inaccuracies in the capacitance measurements result when the series resistances are large. Thin-film SOI devices usually have large series resistances associated with them and this makes the interpretation of capacitance-based results more difficult. Thin-film transistors offer distinct advantages for defect characterization in SOI films. These advantages (when compared to capacitance measurements) include (1) no loss of sensitivity with reduced device dimensions, (2) natural utilization of the laterally distributed substrate contacts, (3) no detrimental effects due to the large series resistance and (4) test devices that are similar or identical to actual circuit components.

Depletion mode devices (deep-depletion devices or accumulation mode devices) operate on the same principle as JFETs in bulk silicon. Figure 6.7 shows the device cross-section of the depletion mode transistor (DMT). DMTs were the first transistors used to characterize generation lifetimes in thin-film SOI material [21-25]. The essential principle behind the use of DMTs to measure τ_g is the same as the pulsed MOS-C technique. A pulse is applied to the gate which places the device in deep-depletion (non-equilibrium). The device then relaxes back to equilibrium through the thermal generation of inversion charges. The relaxation transient is monitored by measuring the drain current in a DMT as opposed to a capacitance in a pulsed MOS-C measurement. The principles of the measurement and the experimental configuration are also shown in figure 6.7. The theoretical treatment follows directly the one described for pulsed MOS-Cs in the previous section. If the transient depletion width is W, then the thickness of the conducting channel between the source and drain is,

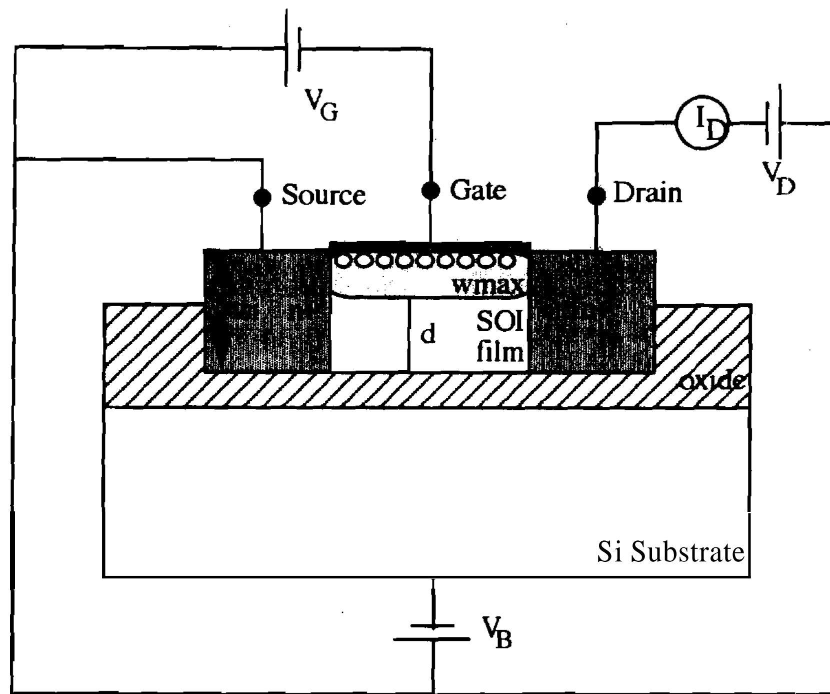


Figure 6.7 Schematic cross-section of the depletion mode transistor (DMT) and the experimental configuration for generation lifetime measurements

$$d = t_{si} - W = \left(\frac{\rho L}{V_D Z}\right) I_D = kI_D \qquad (10)$$

where ρ = sheet resistivity of the material, L = channel length and Z = channel width. V_D and I_D are the drain voltage and drain current, respectively. From the equation of charge conservation in an MOS system, the sum of the inversion charge Q_{inv} and the interface charge Q_{it} is,

$$Q_G = C_{ox}(V_G - V_{FB}) - qN_D W - \frac{qN_D}{2}\frac{C_{ox}}{\varepsilon_s} W^2 \qquad (11)$$

$$\text{and } W = t_{si} - kI_D \qquad (12)$$

Assuming (as in the bulk MOS-C case) that the total generation rate is the sum of the bulk generation component and the surface generation component, the generation rate is given by,

$$\frac{dQ}{dt} = \frac{q n_i}{\tau_g'}(W - W_f) + q n_i s_{eff} \tag{13}$$

where W_f is the final equilibrium value of the depletion width given by $W_f = t_{si} - kI_{Df}$., and I_{Df} is the final saturated value of the drain current at the end oi the transient, Differentiating eqn. (11) with respect to time and then equating it to eqn (1.3) results in,

$$-\frac{N_A}{2n_i}\frac{C_{ox}}{\varepsilon_s}\frac{d}{dt}\left[(W_f + \frac{\varepsilon_s}{C_{ox}}) - kI_D(t)\right]^2 = \frac{k[I_{Df} - I_D(t)]}{\tau_g'} + s_{eff} \tag{14}$$

By plotting the left hand side of eqn (14) versus $[I_{Df} - I_D]$, one obtains a straight line from which τ_g' can be extracted using the slope. This measurement is essentially an extension of the Zerbst technique used in pulsed MOS-C measurements, except that a current is used to monitor the generated charge instead of a capacitance. One of the requirements of this method is that the film thickness must be greater than the maximum depletion width under the gate. In other words, the film must be partially depleted. Therefore this method cannot be used to measure generation lifetimes in thin-film fully depleted SOI devices. Clearly, a pulsed MOS-C measurement technique cannot be used in that case either. because the film would be fully depleted at all times with no change in depletion layer width and hence no change in the measured capacitance.

A recent measurement scheme for measuring generation lifetimes in thin-film enhancement mode devices was proposed by Barth and Angels [26] and subsequently re-analyzed by Mukherjee et. al. [27]. Again, the measurement is made by adapting the Zerbst technique to current transients. This avoids the effect of large series resistances and parasitic capacitances, which make capacitance measurements in thin SOI films very difficult. The measurements are made on enhancement mode MOSFETs which is again advantageous because most integrated circuits use enhancement mode MOSFETs. The cross-section of a partially depleted enhancement mode MOSFET is shown in figure 6.8. In the experiment, the back gate is biased from depletion or accumulation to stronger accumulation. It must be noted that the only source of accumulation charges in the

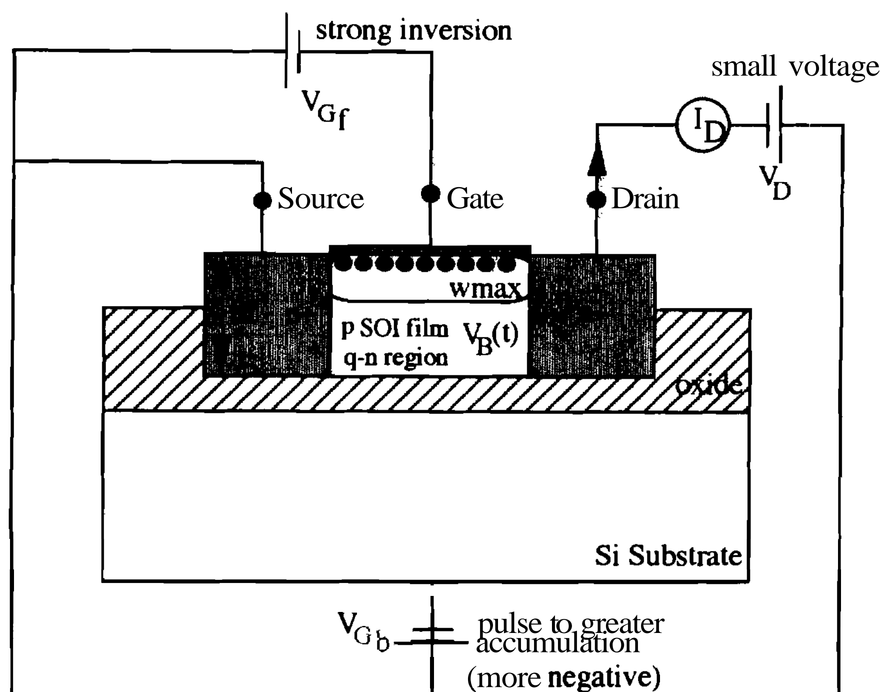


Figure 6.8 Schematic cross-section of the enhancement mode transistor and the experimental setup for generation lifetime measurements

device is from thermal generation (this is in contrast to the conventionall MOS-C case where the only source of *inversion* charges is due to thermal generation). The source/drain regions supply and remove the inversion layer charges immediately. The front gate is maintained in strong inversion at all times and the drain is biased to 100mV. This places the top-gate device in the linear region. Immediately after application of the pulse [+ve to -ve in this case], the accumulation charges cannot be generated immediately. The quasi-neutral body region present in the partially-depleted device develops a negative potential $V_B(t)$ in order to maintain charge neutrality across the back interface. The change in body potential affects the threshold voltage of the front gate transistor which in turn affects the measured drain current. The negative $V_B(t)$ increases the threshold voltage (its effect on the threshold voltage is similar to the body effect in bulk MOS transistors) and hence the measured drain current drops. As the accumulation layer is formed by thermal generation, the body potential slowly relaxes to zero and the

drain current increases to its equilibrium value tracing a relaxation transient. The theoretical analysis for the partially depleted case is presented in reference [27]. In the above pulsed technique the generated carriers not only supply the accumulation layer at the back interface but also the shrinking depletion charge at the front interface as the body potential relaxes to equilibrium. The basic equation is given by

$$G = \frac{dQ_D}{dt} + \frac{dQ_A}{dt} = q n_i \frac{(W - W_f)}{\tau_g'} + q n_i s_{eff} \quad (15)$$

where G is the generation rate, Q_D is the front surface depletion charge, Q_A is the back surface accumulation charge, τ_g' is the effective generation lifetime (accounting for bulk and sidewall generation) and s_{eff} is the effective surface generation velocity (accounting mainly for front interface generation and also for back interface generation and quasi-neutral diffusion processes). The effective generation width is obtained in a similar manner as in the bulk theory as $(W - W_f)$. The depletion charge is given simply by ,

$$Q_D = qN_A W = qN_A \sqrt{\frac{2K_s\varepsilon_o(2\phi_F - V_B(t))}{qN_A}} \quad (16)$$

The depletion region is expressed as a function of the body potential V_B. The accumulation charge at the back interface can likewise be expressed as,

$$Q_A = -C_{ox_b}(V_{G_b} - V_{FB_b} - V_B(t)) \quad (17)$$

Finally applying Gauss' law to the front gate, the total gate charge is related to the depletion charge and the inversion charge by,

$$-Q_D(t) - Q_{inv}(t) = C_{ox_f}(V_{G_f} - V_{FB_f} - 2\phi_F) \quad (18)$$

Equations (15)- (18) can be solved simultaneously and using the additional fact that the device is operated in the linear region so that the drain current is easily related to the inversion charge density by $I_D = (W/L)\mu Q_{inv} V_D$ one obtains,

$$-\frac{N_A C_{ox_f}}{2 n_i \varepsilon_s}\frac{d}{dt}\left\{K(I_{Df} - I_D(t)) + \frac{\varepsilon_s}{C_{ox_b}} + \sqrt{\frac{4\varepsilon_s\phi_F}{qN_A}}\right\}^2 = \frac{K(I_{Df} - I_D(t))}{\tau_g'} + s_{eff} \quad (19)$$

where $K^{-1} = qN_A(W/L)\mu V_D$. This equation is very similar in form to eqn. (14). Again following the Zerbst technique, the left hand side of eqn. (19) is plotted versus $K(I_{Df} - I_D)$

and τ_g' is obtained from the slope of the resulting straight line. The above analysis was carried out for a partially depleted MOSFET.

In a fully depleted MOSFET the SOI film is depleted at all times. Unlike, in the case of a partially depleted structure, the generation rate due to bulk generation cannot be written as $\frac{q n_i (W - W_f)}{}$, because $W = W_f = t_{si}$ at all times. A blind application of the formula would yield a zero generation rate at all times. On the other hand, it is incorrect to assume that the effective generation width is t_{si}, the film thickness, because then the formulation would provide a non-zero bulk generation term even under equilibrium conditions. Thus, the analysis for a fully depleted MOSFET is made extremely arduous because of the difficulty in determining the effective generation width. Experimentally, the measurement is carried out in the same way for the fully depleted device [28,29] as it was for the partially depleted device (figure 3.8). A more detailed qualitative description of the experiment is provided in the next section. Due to the fully depleted nature of the silicon film, there is no quasi-neutral region in the fully depleted MOSFET. The front and back surfaces are coupled together through the depleted film. When the pulse is applied to push the back interface into accumulation, the lack of accumulation charges immediately after the pulse forces the back surface electric field to increase so as to maintain the continuity of dielectric displacement across the back interface. Since the back and front surfaces are coupled, the front surface electric field also increases. This causes the front surface inversion charge density to decrease causing a decrease in the measured drain current. As the thermal generation in the semiconductor bulk provides the accumulation layer at the back interface, the drain current relaxes back to its equilibrium value.

Theoretical analyses of the dual-gate deep-depletion method to measure the generation lifetime in fully depleted MOSFETs have been provided in references [28,29], for the case when a pulse is applied to the back interface. However in both the references incorrect assumptions were made in computing the effective generation width. In [28], the generation rate was assumed to be constant throughout the transient. Clearly this is incorrect because the effective generation width in the semiconductor region changes with time. In [29] the trap related parameters n_1 and p_1 were chosen equal to n_i. In addition, the capture cross-sections of electrons and holes were also assumed to be equal. Neither of these assumptions are valid and could potentially result in, errors in the computed generation lifetime τ_g'. Moreover, in [29], the depletion approximation was

used to determine the relationship between the accumulation layer charge and the inversion layer charge, a formulation that may not be valid for thin films. In addition, the electric field in the depleted semiconductor film was assumed to be equal to a constant value given by the front surface electric field. This is again an unjustified approximation in the formulation that could result in an incorrect value for the effective generation width and hence the computed generation lifetime.

6.3 The Linear Sweep Technique

The widely used measurement techniques to determine generation lifetimes in bulk and thin-film SOI MOSFETs were detailed in the above sections. In the previous section the dual-gate deep-depletion measurement scheme to measure τ_g in partially depleted and fully depleted SOI MOSFETs was introduced. In this section the linear sweep technique which was first applied to bulk MOS-Cs in section 6.1, is adapted for the first time to the dual-gate deep depletion technique. Instead of applying an accumulating pulse to the back gate, a linear ramp is initiated and maintained under accumulation biases. The linear sweep technique simplifies the theoretical interpretations and provides ease of implementation.

The remainder of this section is organized as follows. In section 6.3.1, a complete solution of a 1-D Poisson's formulation is provided for thin-film SOI MOSFETs under equilibrium and non-equilibrium conditions, to explain the behavior of partially depleted and fully depleted SOI MOSFETs under linear sweep conditions. A qualitative description of the measurement is provided in section 6.3.2. Section 6.3.3 contains the quantitative solution of the problem as applied to partially depleted MOSFETs. A comparison at this point to the pulsed technique described in the previous section for partially depleted MOSFETs proves the interpretational ease offered by the linear sweep technique. The quantitative formulations for the fully depleted MOSFET are detailed in section 6.3.4. Finally, the experimental results obtained on fully depleted SOI MOSFETs fabricated on SIMOX substrates are presented in section 6.3.5.

6.3.1 Analytical Formulations

The energy band diagram of a fully-depleted thin-film SOI MOSFET with its front surface in strong inversion and its back surface in accumulation is shown in figure 6.9. Whenever the surface potential changes sign from the front surface to the back surface, there is an inflection point in the energy band diagram (denoted in the figure as d_o). At the inflection point $\frac{d^2E_c}{dx^2} = 0$, which implies that the charge density ρ is zero at that point. When both the front and back surfaces are in inversion, as seen in Chapter 3, the energy band displays a point of zero electric field, but there is no inflection point because the surfaces potentials at the front and back interfaces have the sarne sign. At the inflection point d_o, the electric field E in the film attains its minimum value given by E_o.

Expressions for the charge density, electric field and potential as a function of position inside the semiconductor are obtained by solving Poisson's' equation. In onc dimensions, Poisson's equation simplifies to,

$$\frac{dE}{dx} = \frac{\rho}{K_s\varepsilon_o} = \frac{q}{K_s\varepsilon_o}[p-n-N_D-N_A] \tag{20}$$

In the present case, we choose the inflection point d_o as the reference: point for the potential. Also, expressing the potential in terms of its normalized units,

$$U(x) = \frac{\phi(x)}{kT/q} = \frac{E_i(d_o)-E_i(x)}{kT} \tag{21}$$

$$U_{s_f} = \frac{\phi_{s_f}}{kT/q} = \frac{E_i(d_o)-E_i(\text{front surface})}{kT} \tag{22}$$

$$U_{s_b} = \frac{\phi_{s_b}}{kT/q} = \frac{E_i(d_o)-E_i(\text{back surface})}{kT} \tag{23}$$

$$U_o = \frac{\phi_F}{kT/q} = \frac{E_i(d_o)-E_F}{kT} \tag{24}$$

Also by definition, $N_D-N_A = n_i(e^{-U_F}-e^{U_f})$

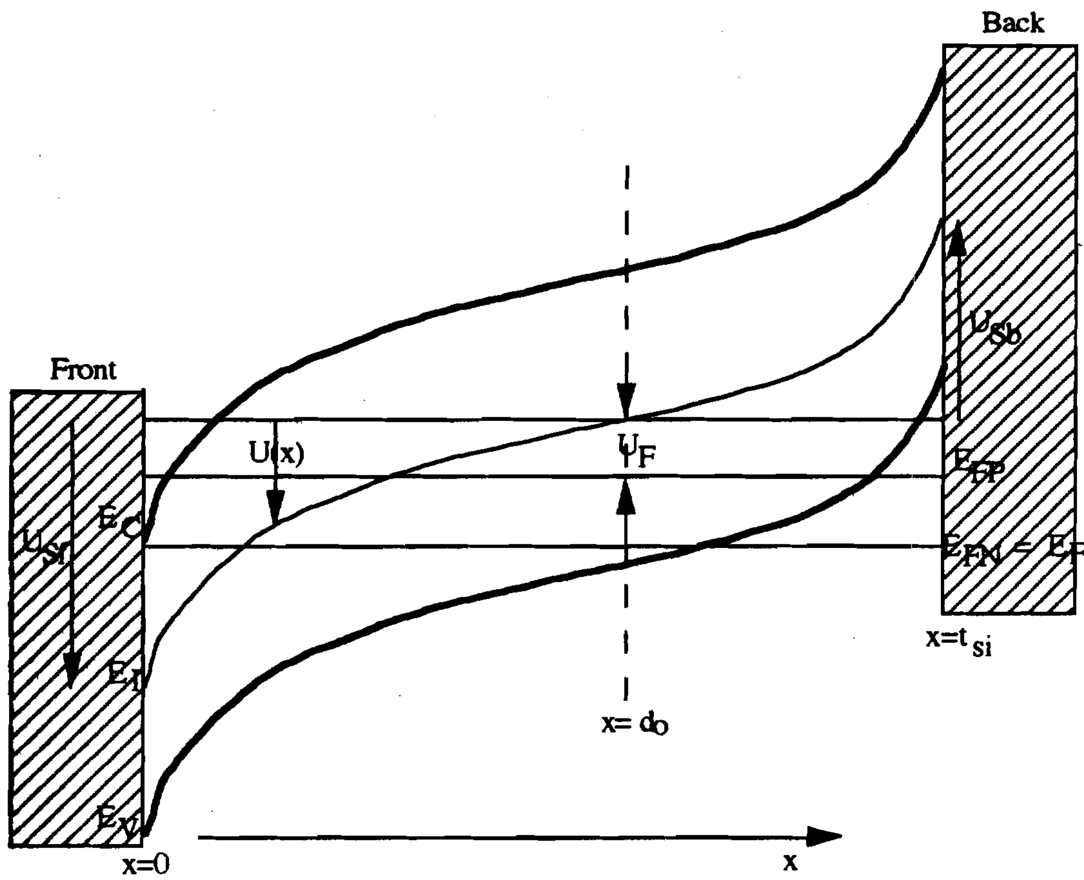


Figure 6.9 Energy band diagram for a fully depleted thin-film SOI MOSFET with a p-type channel and inversion at the front interface and accumulation at the back interface

(i) Equilibrium Formulation

The electron and hole distributions can be expressed in terms of the normalized potentials as,

$$p = n_i \exp\left[\frac{E_i(x)-E_F}{kT}\right] = n_i \exp[U_o - U(x)]$$

$$n = n_i \exp\left[\frac{E_F - E_i(x)}{kT}\right] = n_i \exp[U(x) - U_o] \quad (25)$$

Moreover, since ρ=0 and U=0 at the inflection point d_o,

$$\rho = q n_i (e^{U_o - U(x)} - e^{U(x)-U_o} + e^{-U_F} - e^{U_F}) = 0 = q n_i (e^{U_o} - e^{-U_o} + e^{-U_F} - e^{U_F}) \quad (26)$$

or

$$e^{U_o} - e^{-U_o} = e^{U_F} - e^{-U_F} \quad (27)$$

Therefore, U_o=U_F and the charge density ρ can be expressed in this case as,

$$\rho = q n_i (e^{U_F - U(x)} - e^{U(x)-U_F} + e^{-U_F} - e^{U_F}) \quad (28)$$

(ii) Non-equilibrium Formulation

The electron and hole distributions must be expressed in terms of the majority and minority carrier fermi levels.

$$p = n_i \exp\left[\frac{E_i(x)-F_P}{kT}\right]$$

$$n = n_i \exp\left[\frac{F_N - E_i(x)}{kT}\right] \quad (29)$$

For a top gate front n-channel device, i.e. a p-type SOI film, $F_N = E_F$, because the electrons are in equilibrium with the source and drain regions. The source/drain regions can instantaneously supply electrons to the inversion layer or remove electrons from the inversion layer. Again we define the normalized potentials as,

$$U = \frac{[E_i(d_o) - E_i(x)]}{kT} \quad (30a)$$

$$U_o = \frac{[E_i(d_o) - E_F]}{kT}$$

$$\xi = \frac{[F_P - F_N]}{kT} = \frac{[F_P - E_F]}{kT} \tag{30b}$$

Using these expressions, the electron and hole concentrations become,

$$p = n_i \exp\left[\frac{E_i(x) - F_P}{kT}\right] = n_i \exp\left[\frac{E_i(x) - E_i(d_o) + E_i(d_o) - E_F + E_F - F_P}{kT}\right]$$

$$= n_i \exp[-U + U_o - \xi]$$

$$n = n_i \exp\left[\frac{F_N - E_i(x)}{kT}\right] = n_i \exp\left[\frac{E_F - E_i(d_o) + E_i(d_o) - E_i(x)}{kT}\right] \tag{31}$$

$$= n_i \exp[-U_o + U]$$

Thus, the charge density is given by,

$$\rho = q n_i (e^{U_o - U - \xi} - e^{U - U_o} + e^{-U_F} - e^{U_F}) \tag{32}$$

Again, at the inflection point d_o, $\rho=0$ and U=0. Therefore,

$$\rho|_{inflection\ point} = q n_i (e^{U_o - \xi} - e^{-U_o} + e^{-U_F} - e^{U_F}) = 0 \tag{33}$$

If we can now neglect the terms e^{-U_o} and e^{-U_F}, especially since during the measurement $U_F>0$ and $\xi>0$,

$$e^{U_o - \xi} - e^{U_F} = 0 \text{ or } U_o \approx U_F + \xi \tag{34}$$

The above **formulation** says that $E_i(d_o)-F_P$ is always the same regardless of the system state or where d_o lies on the x-axis. We may therefore write,

$$\rho = q n_i (e^{U_o - U - \xi} - e^{U - U_o} + e^{-U_o} - e^{U_o - \xi}) \tag{35}$$

$$\therefore \quad \rho = q n_i (e^{U_F - U} - e^{U - U_F - \xi} + e^{-U_F - \xi} - e^{U_F}) \tag{36}$$

Thus U_o is again totally eliminated from the formulation and U is always measured relative to the d_o point. This is important because the reference point must remain the same at all times. If in eqn. (36) we substitute $\xi=0$, the equation simplifies to eqn. (28),

the expression for charge density under equilibrium conditions. We can therefore continue the derivation of the analytical expressions starting with eqn (36), knowing full well that the equilibrium solution can be obtained merely by substituting $\xi=0$ in the final result. 'ξ' is referred to as the **quasi-fermi-level** splitting parameter and can be considered a measure of the state of non-equilibrium of the device, i.e. a measure of how far from equilibrium the device is operating. In the application of the analytical expressions to the linear sweep technique, the quasi-fermi-level splitting parameter, detenrnines the ramp rate and the effective generation widths under the different saturation conditions as will be seen in the next section. The larger the value of ξ, the larger the ramp rate and the generation rate.

Maneuvering to recast Poisson's equation into a form more amenable to solution, we note,

$$E = \frac{1}{q}\frac{dE_i(x)}{dx} = -\frac{kT}{q}\frac{dU}{dx} \tag{37}$$

Poisson's Equation is then expressed as,

$$\frac{d^2U}{dx^2} = \left(\frac{q^2 n_i}{K_s \varepsilon_o kT}\right)\left(e^{U-U_F-\xi} - e^{U_F-U} + e^{U_F} - e^{-U_F-\xi}\right) \tag{38}$$

The next step is to solve the above equation subject to the boundary conditions ,

$$U = U_{S_f} \quad ; \quad x=0 \qquad\qquad U = 0 \quad ; \quad x=d_o$$

$$\frac{dU}{dx} = \left.\frac{dU}{dx}\right|_{d_o} = -\frac{q}{kT}E_o \qquad ; \qquad x=d_o$$

Multiplying both sides of eqn. (38) by (dU/dx) and integrating from $x=d_o$ to a arbitrary point x,

$$\int_{\left.dU/dx\right|_{d_o}}^{dU/dx} \frac{dU}{dx}\, d\left(\frac{dU}{dx}\right) = \frac{1}{2L_D^2}\int_0^{U(x)}\left(e^{U-U_F-\xi} - e^{U_F-U} + e^{U_F} - e^{-U_F-\xi}\right)dU \tag{39}$$

$$\left[\frac{1}{2}\left(\frac{dU}{dx}\right)^2 - \frac{1}{2}\left(\left.\frac{dU}{dx}\right|_{d_o}\right)^2\right] = \frac{1}{2L_D^2}\left[e^{U-U_F-\xi} + e^{U_F-U} + e^{U_F}U - e^{-U_F-\xi}U - e^{-U_F-\xi} - e^{U_F}\right] \tag{40a}$$

$$= \frac{1}{2L_D^2}\left[e^{U_F}(e^{-U}+U-1) + e^{-U_F-\xi}(e^{U}-U-1)\right] \tag{40b}$$

$$\frac{dU}{dx} = \left[\left(\frac{dU}{dx}\bigg|_{d_o}\right)^2 + \frac{1}{L_D^2}\left[e^{U_F}(e^{-U}+U-1) + e^{-(U_F+\xi)}(e^{U}-U-1)\right]\right]^{1/2} \tag{41}$$

We can choose either a positive or a negative sign for the square root. A look at the figure shows that the field is positive everywhere. Moreover, the front surface potential is positive. If the front surface potential were negative and the back surface potential positive, then the field would be negative everywhere. Based on this observation,

$$\frac{dU}{dx} = -\hat{U}_{S_f}\left[\left(\frac{dU}{dx}\bigg|_{d_o}\right)^2 + \frac{1}{L_D^2}\left[e^{U_F}(e^{-U}+U-1) + e^{-(U_F+\xi)}(e^{U}-U-1)\right]\right]^{1/2} \tag{42}$$

where $\hat{U}_{Sf} = 1$ if $U_{Sf} > 0$ and $\hat{U}_{Sf} = -1$ if $U_{Sf} < 0$. The electric field in the film is then given by,

$$E = -\frac{kT}{q}\frac{dU}{dx} \tag{43}$$

Let us now denote the F-function as,

$$F(U, U_F, \xi) = \left[e^{U_F}(e^{-U}+U-1) + e^{-(U_F+\xi)}(e^{U}-U-1)\right]^{1/2} \tag{44}$$

Then,

$$\frac{dU}{dx} = -\hat{U}_{S_f}\left[\left(\frac{dU}{dx}\bigg|_{d_o}\right)^2 + \frac{F^2(U, U_F, \xi)}{L_D^2}\right]^{1/2} \tag{45}$$

Separating variable and integrating,

$$\int_{U_{S_f}}^{0} \frac{dU}{\left[\left(\frac{dU}{dx}\bigg|_{d_o}\right)^2 + \frac{F^2(U, U_F, \xi)}{L_D^2}\right]^{1/2}} = -\hat{U}_{S_f}\int_0^{d_o} dx \tag{46}$$

$$\int_{0}^{U_{S_b}} \frac{dU}{\left[\left(\left.\frac{dU}{dx}\right|_{d_o}\right)^2 + \frac{F^2(U,U_F,\xi)}{L_D^2}\right]^{1/2}} = -\hat{U}_{S_f}\int_{d_o}^{t_{si}} dx \tag{47}$$

Adding equations (46) and (47),

$$\int_{U_{S_b}}^{U_{S_f}} \frac{dU}{\left[\left(\left.\frac{dU}{dx}\right|_{d_o}\right)^2 + \frac{F^2(U,U_F,\xi)}{L_D^2}\right]^{1/2}} = t_{si} \tag{48}$$

The inflection point d_o is determined from equation (46). Finally, the potential distribution across the film can be computed from

$$\int_{U}^{U_{S_f}} \frac{dU}{\left[\left(\left.\frac{dU}{dx}\right|_{d_o}\right)^2 + \frac{F^2(U,U_F,\xi)}{L_D^2}\right]^{1/2}} = x \qquad 0 \le x \le d_o$$

$$\int_{U_{S_b}}^{U} \frac{dU}{\left[\left(\left.\frac{dU}{dx}\right|_{d_o}\right)^2 + \frac{F^2(U,U_F,\xi)}{L_D^2}\right]^{1/2}} = t_{si} - x \qquad d_o \le x \le t_{si} \tag{49}$$

Once the potential distribution is determined, the electron and hole concentrations are determined from eqn. (31). The terminal voltage relationships are given by,

$$V_{G_f} = V_{FB_f} + \frac{kT}{q}(U_{S_f} - \xi) + \frac{K_s t_{ox}}{K_o} E_{S_f}$$

$$E_{S_f} = \frac{kT}{q}\left[\left(\left.\frac{dU}{dx}\right|_{d_o}\right)^2 + \frac{F^2(U_{Sf},U_F,\xi)}{L_D^2}\right]^{1/2} \tag{50}$$

The methodology for the solution of the above equations is as follows. The front gate voltage V_{Gf} and the back surface potential ϕ_{Sb} are chosen such that the front surface is in strong inversion and the back surface is in strong accumulation. The back surface potential ϕ_{Sb} is chosen such that the front surface inversion charge density is saturated for

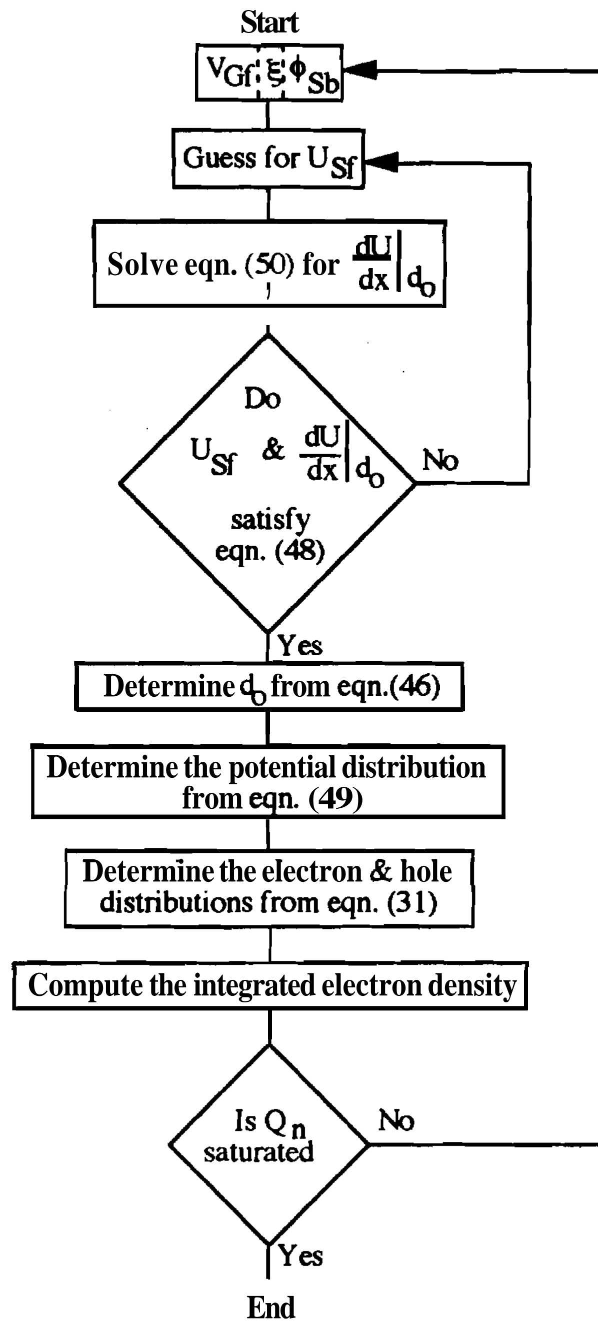


Figure 6.10 Algorithm used to determine the integrated electron density for the front n-channel device using the analytical formulation

the given choice of the quasi-fermi-level splitting 'ξ'. Given V_{Gf}, ϕ_{Sb} and ξ and knowing the device parameters such as the front and back oxide thicknesses, the channel doping concentration and the silicon film thickness t_{si}, eqns (48) and (50) are solved by the two-dimensional bisection method to determine ϕ_{Sf} and — Once $\left.\frac{dU}{dx}\right|_{x_o}$ is determined, the value of E_o is determined using eqn. (46). The value of the front surface electric field is also determined using eqn. (50). The potential distribution across the film is obtained using eqn. (49) and the electron and hole concentrations are obtained using eqn (31). The solution algorithm is shown in fig. 6.10.

6.3.2 Qualitative Description of the Linear Sweep Technique

The schematic cross-sections of a partially depleted and fully depleted N-channel MOSFET are illustrated in figure 6.11. The front surface of the SOI MOSFET is placed in strong inversion. The inversion charge density across the front interface is monitored by placing a small bias (V_D=100mV) on the drain and measuring the drain current (I_D). The bias on the drain is maintained at a small value for two reasons: (a) it allows continued use of the gradual channel approximation and the device behavior can be modeled by the 1-D formulations presented in the previous section and (b) higher drain voltages could potentially cause impact-ionization to occur near the drain which then acts as a source for additional carriers. In order that thermal generation be the only source of carrier generation, the drain field must be minimized which is achieved by keeping the drain voltage as small as possible. A linear voltage ramp of variable ramp rate is applied at the back interface. The ramp is initiated and maintained under accumulation biases, so that the back interface is constantly being pushed towards greater accumulation. It is important to note that in both the partially depleted and fully depleted MOSFETs, there is no source of accumulation charges (such as a body contact) so that all accumulation charges must be thermally generated. Moreover, the inversion charges are in equilibrium with the source and drain regions. That is to say that the source/drain regions can instantaneously supply the inversion carriers to the inversion layer or remove electrons from the inversion layer.

The measurement involves monitoring the drain current (I_d) at the fixed front gate voltage. During the initial stages of the sweep, the accumulation charges at the back

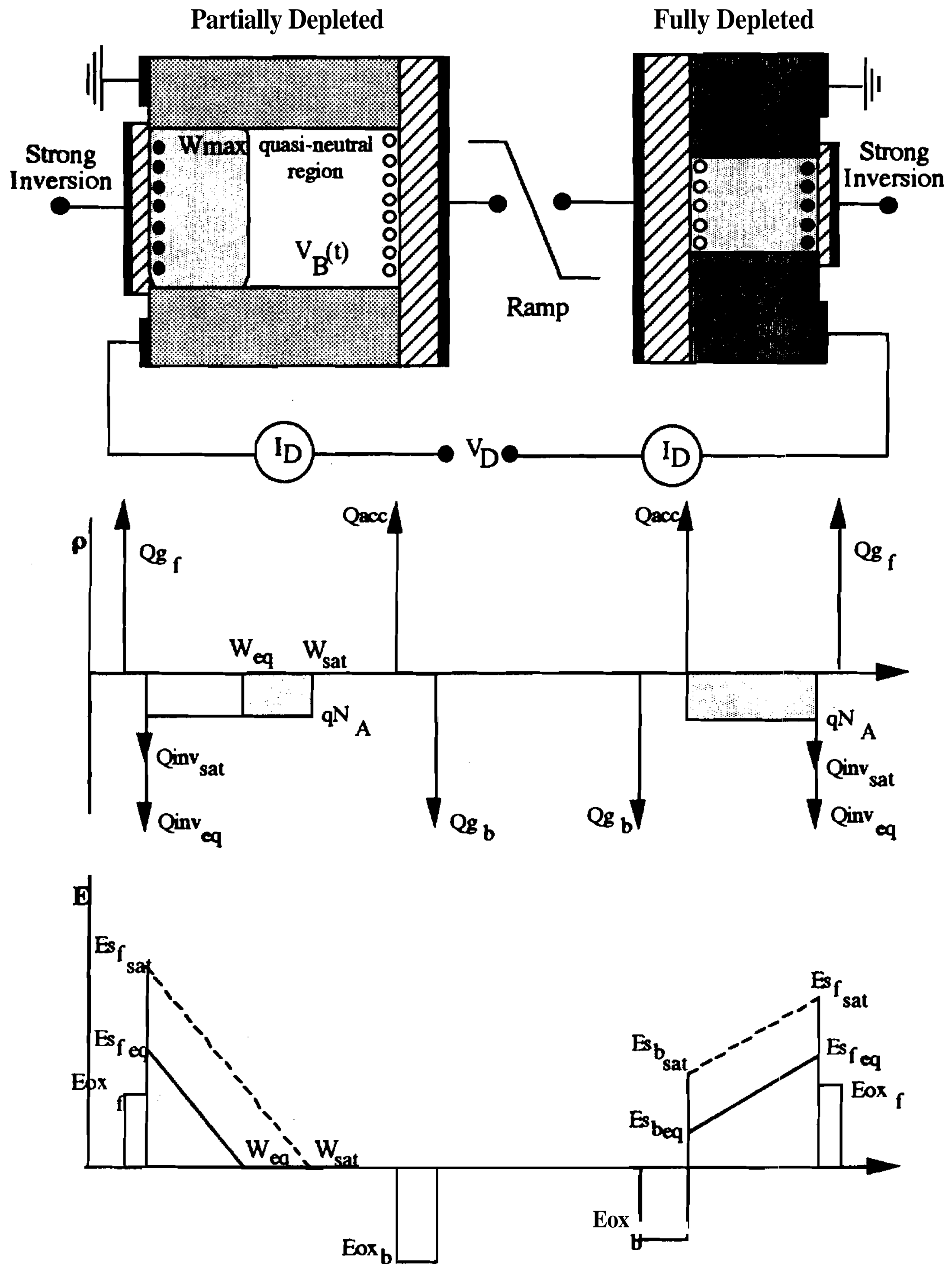


Figure 6.11 Schematic cross-section of the partially and fully depleted SOI MOSFET under the linear sweep technique. Also shown in the figure are the charge density and electric field distributions under the equilibrium and non-equilibrium saturation conditions

interface cannot be generated fast enough to offset the charge being placed on the back gate. In the partially depleted device, the quasi-neutral region develops a positive potential (for a n-channel device) in order to maintain charge neutrality across the back interface. For example, assume for the moment the delta depletion approximation shown in fig. 6.11 The field in the semiconductor at the back interface is zero. The field in the oxide then determines the amount of accumulation charge as dictated by Gauss' Law. If the back gate voltage continuously decreases (goes more negative), but there is no corresponding accumulation charge formation, then the field across the back oxide cannot increase which forces the quasi-neutral region to develop a positive potential as seen in the figure. The quasi-neutral body potential has the same effect on the front-channel transistor, that the body voltage in a bulk MOSFET has on its device performance. The threshold voltage of the front channel transistor decreases due to the widening of the depletion layer under the front interface. The measured drain currenl consequently decreases due to a decrease in the front channel inversion charge density. In a fully-depleted MOSFET the front and back interfaces are electro-statically coupled together. When the back gate voltage decreases but there is no attendant increase in the back surface accumulation charge density, the back surface electric field increases in order to maintain the dielectric displacement continuity across the back interface. Due to the coupling between the two interface, the front surface electric field also increases as seen in fig. 6.11. The field across the front oxide is however constant. Therefore the field at the front interface in the silicon film must be balanced by a decrease in the inversion charge density at the front interface in order to maintain the displacement continuity there. Consequently the measured drain current again decreases just as in the case of the partially depleted MOSFET.

The inversion charge density in the semiconductor volume decreases in both the partially depleted and the fully depleted MOSFETs until such time that the generation rate within the semiconductor exactly balances the rate at which charge is being added to the back gate by the linear voltage ramp. Once the dynamic steady state is attained, where for every charge added to the back gate there is a compensating accumulation charge generated in the semiconductor, the inversion charge in the semiconductor (Q_n) saturates. The measured current (Id) would also saturate. If the linear ramp were extremely slow, then there is sufficient time for the accumulation layer to form at all times. In this case the measured drain current wouldn't change very much. (The drain current would show a slight decrease with increasing back gate bias even under

equilibrium conditions because of the small dependence of the front channel current on the back surface potential, which though ideally pinned at zero, does increase a small amount with increasing back gate voltage). For increasing values of the: ramp rate the drain current saturates at decreasing values as it takes longer for the semiconductor generation to match the rate of change of charge at the back gate. This **conduct** is shown in figure 6.12 which depicts the simulated dependence of the inversion charge density (which is proportional to the drain **current** Id) on the **back** gate voltage for increasing rates of linear sweep (R). The most important feature of the linear sweep **characteristics** shown in fig. 6.12 is the existence of a readily observable saturation inversion charge density **(Qn_{sat})**. The simulations were **carried** out using the analytical expressions derived in section 6.3.1.

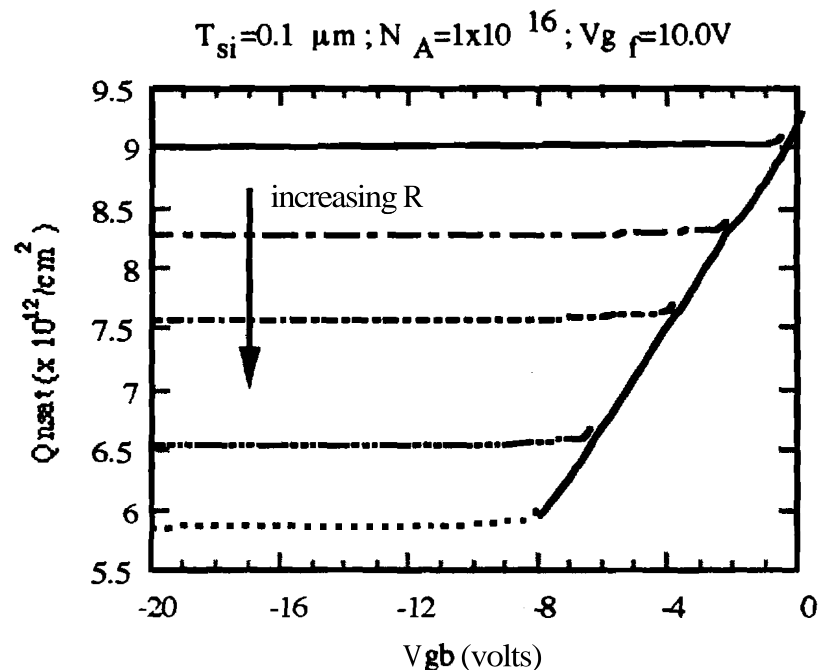


Figure 6.12 Simulated linear sweep characteristics for a fully depleted **SOI** MOSFET

Since the back gate is always in strong accumulation and the front gate is always maintained in inversion, the two interfaces do not contribute to carrier generation and the only viable generation mechanism is bulk generation. In this regard it is important to note that there is a distinct possibility that the front surface could come out of strong inversion if the ramp rate applied were too large. In this case the front interface will contribute to the total generation and the generation lifetime measured would be incorrect. If there is any additional generation in the semiconductor such as field-enhanced generation or oxide leakage, then the curves would not saturate but would instead show a tendency to gradually increase. Hence using the linear sweep technique it is possible to detect these non-ideal situations, which would not have been detected were the pulsed technique used.

Finally, we must develop the relevant equations which would aid the application of the analytical formulation above to the linear sweep technique. The generation rate according to the Schockley-Read-Hall theory is given by eqn. (1) and is repeated here as eqn. (51).

$$G = \frac{(n_i^2 - np)}{[\tau_{po}(n + n_1) + \tau_{no}(p + p_1)]} \tag{51}$$

Since ξ is the quasi-fermi-level splitting parameter, the np product can be written as $n_i^2 e^{-\xi}$. G is the generation rate per unit volume per sec , and can now be recast as,

$$G = \frac{n_i^2(1-e^{-\xi})}{\tau_{po}(n+n_1)+\tau_{no}(p+p_1)} = \frac{n_i(1-e^{-\xi})}{(\tau_{po}\frac{n_1}{n_i}+\tau_{no}\frac{p_1}{n_i})+(\tau_{po}\frac{n}{n_i}+\tau_{no}\frac{p}{n_i})}$$

$$= \frac{n_i(1-e^{-\xi})}{\tau_g\left(1 + \frac{\tau_{no}}{\tau_g}\frac{p}{n_i} + \frac{\tau_{po}}{\tau_g}\frac{n}{n_i}\right)} \tag{52}$$

τ_g is given by eqn. (4). The generation rate per unit area per sec is then obtained by integrating eqn. (52) across the entire film . The rate of generation of accumulation charges is then given by,

$$\frac{dQ_{acc}}{dt} = \frac{q n_i}{\tau_g} W_{eff} \tag{53}$$

where the effective generation width W_{eff} is defined from first principles by,

$$W_{eff} = \int_0^{t_{si}} \frac{(1-e^{-\xi})\,dx}{1 + \frac{\tau_{no}}{\tau_g}\frac{p}{n_i} + \frac{\tau_{po}}{\tau_g}\frac{n}{n_i}} \tag{54}$$

Therefore, for a given choice of the quasi-fermi-level splitting ξ (which defines the ramp rate R), the electron and hole distributions across the SOI film can be determined following the algorithm outlined in figure 6.10. The effective generation width can then be obtained using eqn. (54).

6.3.3 Partially Depleted MOSFET

A qualitative description of the linear sweep measurement for a partially depleted MOSFET was presented in the previous section. In the following, we develop the relevant equations to be able to extract the generation lifetime.

For a partially depleted SOI MOSFET, the steady-state charge generation rate within the semiconductor can be written as,

$$G = \frac{q n_i}{\tau_g} W_{eff} = \frac{q n_i}{\tau_g}(W_{sat} - W_{eq}) \tag{55}$$

The effective generation width is expressed as in the bulk case as $(W_{sat}-W_{eq})$. Only bulk generation is considered because surface generation is avoided by the nature of the measurement. Quasi-neutral region generation in the volume of the: semiconductor within one diffusion length of the depletion region is also neglected in the analysis. In eqn. (55), W_{sat} is the saturated depletion width beneath the front gate under dynamic steady-state and W_{eq} is the equilibrium depletion width. When the quasi-steady state condition is reached, the generation rate of accumulation carriers in the volume of the semiconductor exactly equals the rate at which charge is added to the back gate by the linear ramp. Charge is added to the back gate at a rate given by $C_{ox_b} \frac{dV_{G_b}}{dt} = C_{ox_b} R$. Therefore, under steady-state the charge balance equation is,

$$C_{ox_b} R = \frac{q n_i}{\tau_g}(W_{sat} - W_{eq}) \tag{56}$$

Since the device is biased in the linear region of operation, the drain current is given by,

$$I_D = \frac{W}{L}\mu Q_n V_D = \frac{W}{L}\mu C_{ox_f}(V_{G_f} - V_{T_f})V_D \tag{57}$$

The threshold voltage of the front gate is given by the bulk MOSFET theory as.

$$V_{T_f} = 2\phi_F + \frac{qN_A}{C_{ox_f}}W = 2\phi_F + \frac{qN_A}{C_{ox_f}}\sqrt{\frac{2K_s\varepsilon_o(2\phi_F - V_{BS})}{qN_A}} \tag{58}$$

If the current under the non-equilibrium saturation condition is $I_{D,sat}$ and the equilibrium current is $I_{D,eq}$, then from eqn. (57),

$$I_{D,sat} - I_{D,eq} = \frac{W}{L}\mu C_{ox_f} V_D(V_{T_{f,sat}} - V_{T_{f,eq}}) \tag{59}$$

The threshold voltage under equilibrium and non-equilibrium conditions are,

$$V_{T_{f,eq}} = 2\phi_F + \frac{qN_A}{C_{ox_f}}W_{eq} \tag{60}$$

$$V_{T_{f,sat}} = 2\phi_F + \frac{qN_A}{C_{ox_f}}W_{sat} \tag{61}$$

Therefore, the difference $I_{D,sat}$-$I_{D,eq}$ is given by,

$$I_{D,sat} - I_{D,eq} = \frac{W}{L}\mu C_{ox_f} V_D \frac{qN_A}{C_{ox_f}}(W_{sat} - W_{eq}) \tag{62}$$

From equations (56) and (61),

$$I_{D,sat} - I_{D,eq} = \frac{W}{L}\mu V_D qN_A \frac{C_{ox_b}R\tau_g}{qn_i} = \frac{W}{L}\mu V_D \frac{N_A C_{ox_b}\tau_g}{n_i}R \tag{63}$$

Thus, τ_g can be determined from the linear slope of a $I_{D,sat}$ versus R plot. Results based on the exact 1-dimensional analytic model are shown in fig. 6.13 for a partially depleted MOSFET.

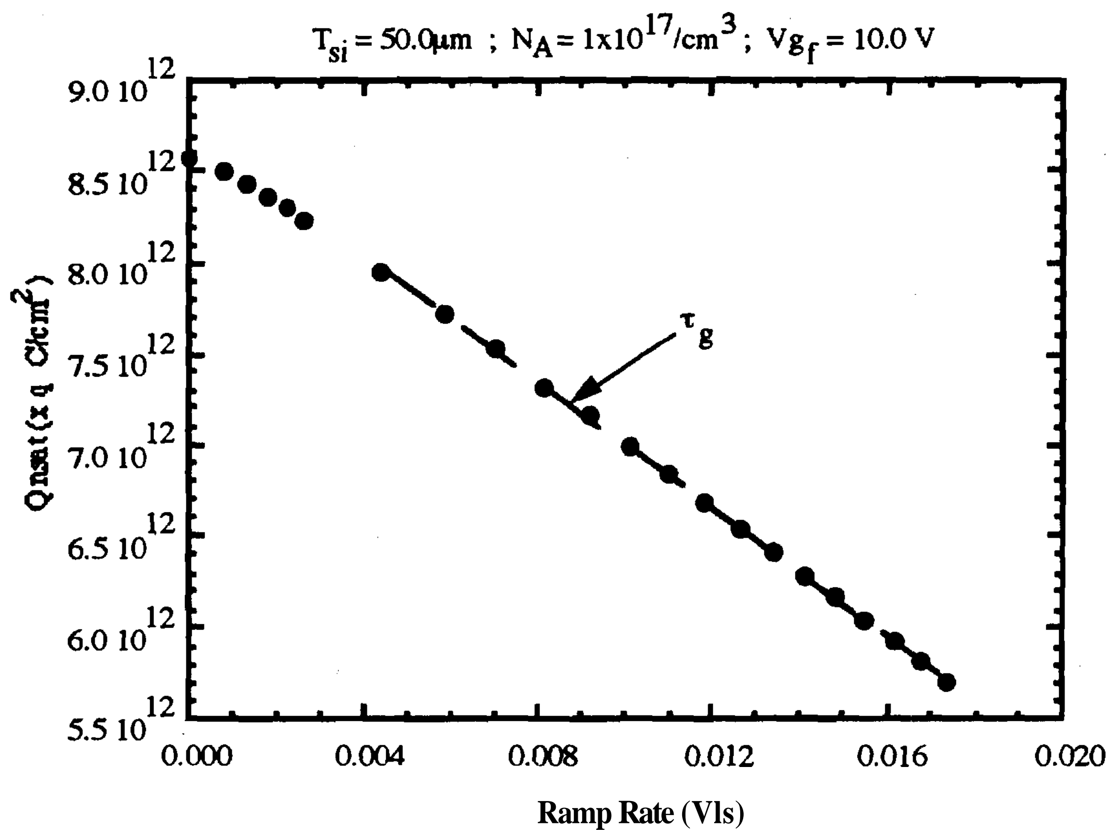


Figure 6.13 Qn_{sat} versus Ramp Rate plot for a partially depleted SOI MOSFET. The linear slopeof the plot yields τ_g. Qn_{sat} is proportional to the measured drain current Id_{sat}

6.3.4 Fully Depleted SOI MOSFETs

The measured drain current in the linear region for the fully depleted SOI MOSFET is given by,

$$I_D = \left(\frac{W}{L}\mu V_D\right)Q_n = \left[\frac{G_D}{C_{ox_f}(V_{G_f} - V_{T_f})}\right] V_D Q_n \tag{64}$$

The generation rate of accumulation charges per unit area per sec. is,

$$G = \frac{q n_i}{\tau_g} W_{eff} \tag{65}$$

where W_{eff} is again the effective generation width. Again, all surface generation components are suppressed in the measurement. As seen in section 6.3.2, there is a potential difficulty in determining the effective generation width. Clearly, the bulk approximation cannot be used in this case. The generation lifetime must be determined from the basic equation(s) derived from the SRH theory as given by eqn. (54) and repeated here for clarity.

$$W_{eff} = \int_0^{t_{si}} \frac{(1-e^{-\xi})\,dx}{1 + \frac{\tau_{no}}{\tau_g}\frac{p}{n_i} + \frac{\tau_{po}}{\tau_g}\frac{n}{n_i}} \approx \int_0^{t_{si}} \frac{dx}{1 + \frac{\tau_{no}}{\tau_g}\frac{p}{n_i} + \frac{\tau_{po}}{\tau_g}\frac{n}{n_i}} \tag{66}$$

where

$$\frac{\tau_g}{\tau_{no}} = \frac{\tau_{po}}{\tau_{no}}\frac{n_1}{n_i} + \frac{p_1}{n_i} \; ; \; \frac{\tau_g}{\tau_{po}} = \frac{n_1}{n_i} + \frac{\tau_{no}}{\tau_{po}}\frac{p_1}{n_i} \tag{67}$$

Thus, W_{eff} depends on $n(x)$, $p(x)$, τ_{no}/τ_{po} and (E_T-E_i). τ_{no}/τ_{po} is the ration of the capture cross-sections of electrons to holes, and (E_T-E_i) determines the trap related parameters n_1 and p_1. The electron and hole distributions can be determined using the analytic expressions of section 6.3.1. We can therefore compute the exact W_{eff} using eqns. (66) and (67) provided the values of τ_{no}/τ_{po} and (E_T-E_i) are known. Let us assume for the moment that we do know τ_{no}/τ_{po} and E_T-E_i and that W_{eff} could be exactly computed. Then under the dynamic steady-state condition, the rate of accumulation charge generation given by eqn. (64) must exactly equal the rate of change of charge on the back gate.

$$\frac{q n_i}{\tau_g} W_{eff} = C_{ox_b} R \quad \Rightarrow \quad W_{eff} = \frac{C_{ox_b} \tau_g}{q n_i} R \tag{68}$$

τ_g can then be **determined** from the linear slope of the W_{eff} vls R plot.

In the experiment the two measurable parameters are R, the ramp rate and I_{Dsat}, the saturated drain current. In the case of the partially depleted device it was easy to draw an explicit relationship between I_{Dsat} and R. However, in the fully depleted device, the relationship is implicit through the effective generation width. Different values of I_{Dsat} correspond to different values of W_{eff} which in turn is related to the ramp rate.

6.3.4.1 **Determining** the Effective Generation Width

In order to get an insight into the behavior of W_{eff} on the trapping parameters

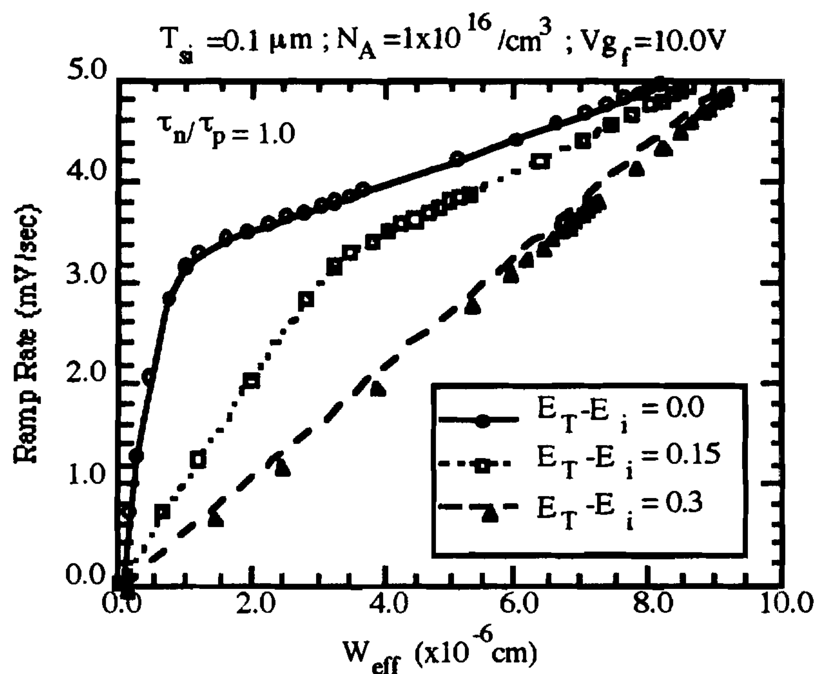


Figure 6.14 R versus W_{eff} plot for different assumed values of E_T-E_i. The computed t_g from the linear slope of this plot varies with the choice of E_T-E_i

τ_{no}/τ_{po} and E_T-E_i, we use the analytic simulation detailed in fig. 6.10 and work backwards. We begin by assuming a known device which fixes the values of τ_{no}/τ_{po}, E_T-E_i and τ_g. The structural device parameters such as the front and back gate oxide, the channel thickness and the channel doping concentration are also assumed to be known. One can then compute the effective generation width W_{eff} using eqns. (66)and (67)and the ramp rate using eqn. (68). Clearly a plot of W_{eff} v/s R for this ideal case would result in straight line going through the origin. This is illustrated in fig 6.14. The assumed device parameters are indicated in the figure (τ_g=20.0 μs, τ_{no}/τ_{po} = 1.0. E_T-E_i = 0.3eV).

It is worthwhile to note that the computation of W_{eff} does not involve the generation lifetime τ_g. The values of the ramp rate determined in the above calculations could now be considered the 'measured' ramp rates corresponding to the saturated

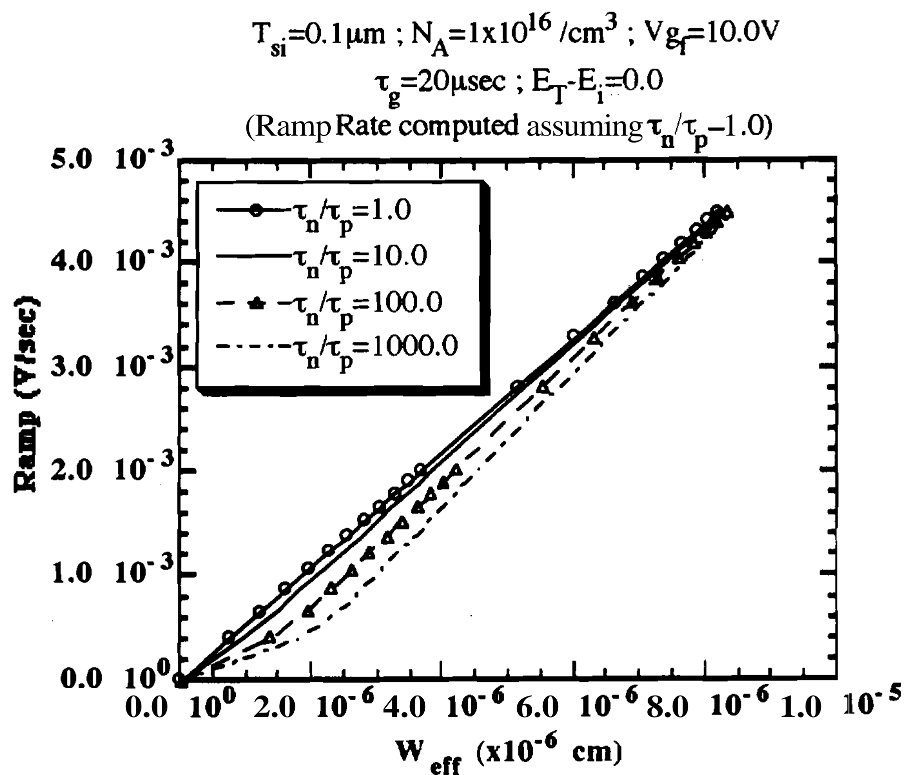


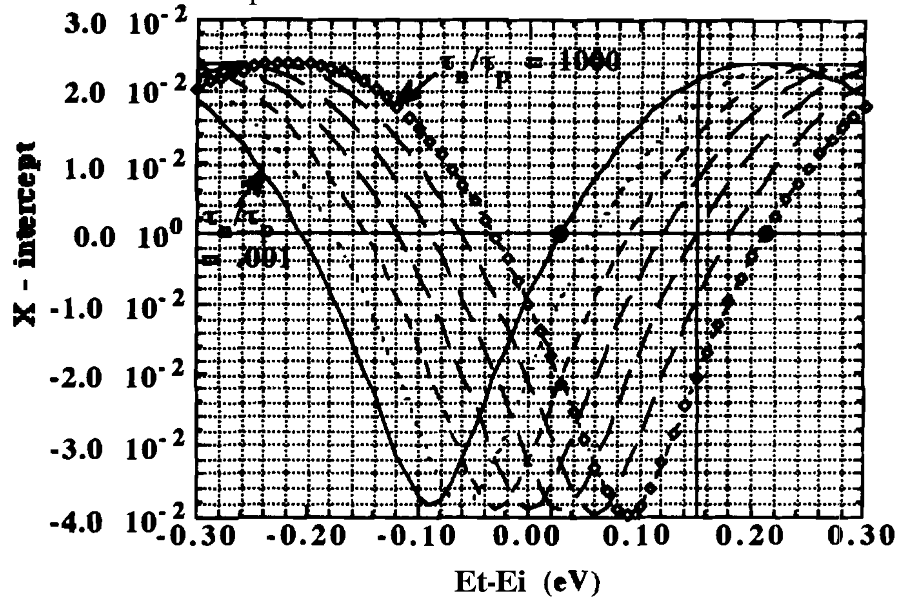
Figure 6.15 R versus W_{eff} plot for different values of τ_{no}/τ_{po}

inversion charge densities (drain currents). If one now chooses an 'incorrect' value of E_T-E_i and then re-computes the effective generation width, the plot is no longer a perfect line. This is also shown in figure 6.14 for E_T-E_i = 0.1eV and E_T-E_i = 0.2eV(these are 'incorrect' assumptions for E_T-E_i, the 'correct' value being 0.3eV). Similarly, if we fix E_T-E_i and choose 'incorrect' values of τ_{no}/τ_{po}, the W_{eff} v/s R plot again deviates from the straight line dictated by eqn. (68) as illustrated in fig. 6.15. It is clear after studying figs. 6.14 and 6.15 that an incorrect assumption in the value of E_T-E_i and/or τ_{no}/τ_{po} could potentially yield erroneous values for the computed generation lifetimes.

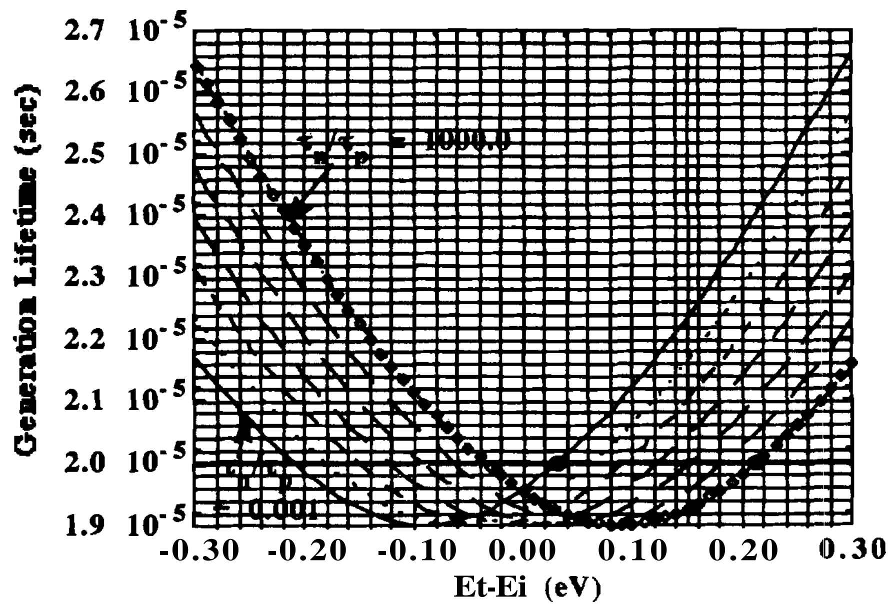
If one assumes the correct values of E_T-E_i and τ_{no}/τ_{po}, then the W_{eff} v/s R plot is a straight line through the origin. For all other choices, the plot develops a non-zero x-intercept. This observation gives us a methodology to get at the correct value of the generation lifetime. For a fixed value of τ_{no}/τ_{po}, we can vary E_T-E_i until the x-intercept of the W_{eff} v/s R plot becomes zero. The slope of the line with the zero x-intercept then determines the generation lifetime τ_g. This methodology is demonstrated in fig. 6.16. E_T-E_i is varied for different choices of τ_{no}/τ_{po}. In each case the x-intercept obtained is plotted in fig. 6.16(a). The corresponding generation lifetimes obtained from the slope of the line are plotted in fig. 6.16(b). It is observed that when the x-intercept is zero, the corresponding generation lifetime value is 20.0 μs, which was the value initially assumed in the simulations (fig. 6.13).

Another interesting point emerges from fig. 6.16. It can be seen that there exists pairs of values of τ_{no}/τ_{po} and E_T-E_i that provide the same correct value of the generation lifetime. With reference to the figure, for example, the 2-tuples (1000,0.21) and (0.001,0.03) both yield curves with a unique τ_g=20μs. Therefore, in conclusion, although we cannot uniquely determine all the parameters τ_{no}/τ_{po}, E_T-E_i and τ_g, we can unambiguously determine the generation lifetime τ_g.

In order to throw further light on this matter, we first look at the electron and hole density distributions across the film as plotted in fig. 6.17. The electron density distribution plotted on a semi-log scale is non-linear near the two surfaces but is more or less linear near the center of the film, more so under the non-equilibrium deep depletion conditions. This implies that the electron and hole distributions become:exponential near the center of the film. Since the contribution to the effective generation width essentially comes from the center of the film, little error is made in assuming that the carrier distributions are exponential across the entire film. An exponential carrier distribution in



(a)



(b)

Figure **6.16** Variation of (a) the X-intercept and (b) the slope of the W_{eff} v/s R plot as a function of E_T-E_i for different values of τ_n/τ_p

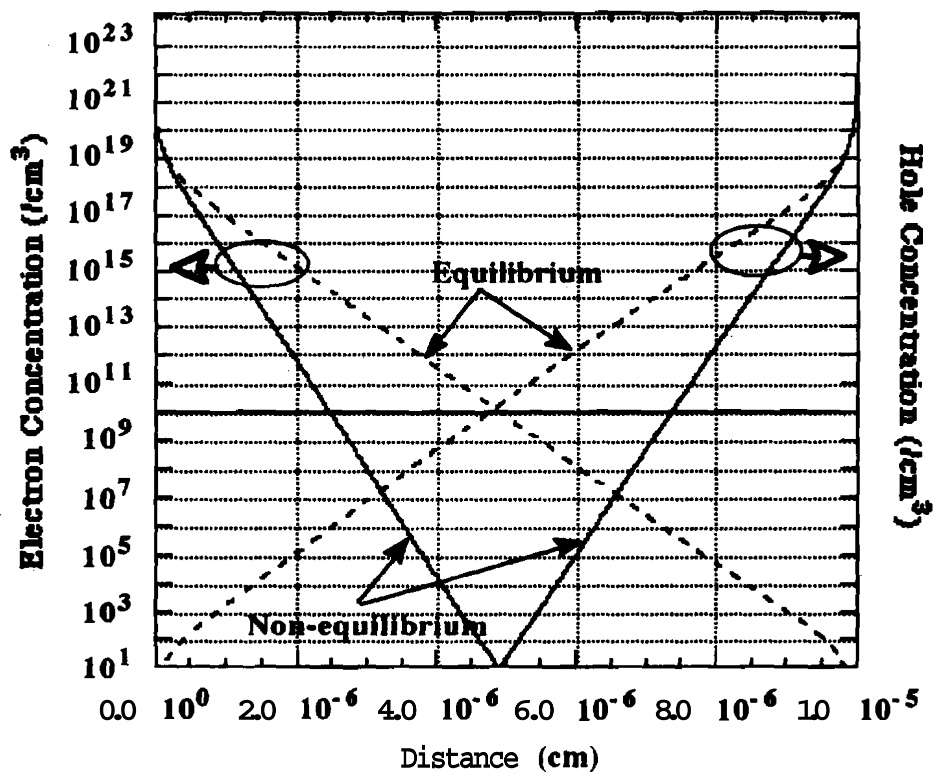


Figure 6.17 Electron and hole distributions in a fully depleted SOI MOSFET under equilibrium and non-equilibrium conditions

turn implies a linear potential distribution or a constant field distribution across the film. Under these assumptions the effective generation width W_{eff} given by eqn. *(66)* can be simplified as follows. Let $\alpha = \tau_{no}/\tau_g$ and $\gamma = \tau_{po}/\tau_g$. Then,

$$W_{eff} = \int_0^{t_s} \frac{dx}{1+\alpha \frac{p}{n_i} + \gamma \frac{n}{n_i}} = \int_0^{t_s} \frac{dx}{1+\alpha e^{U_F - U} + \gamma e^{U - U_F - \xi}} \quad (69)$$

Without making any error in the computation, the limits of integration can be extended from $-\infty$ to $+\infty$.

$$\therefore \quad W_{eff} = \int_{-\infty}^{\infty} \frac{dx}{1+\alpha e^{U_F - U} + \gamma e^{U - U_F - \xi}} = \frac{1}{\left.\frac{dU}{dx}\right|_{d_o}} \int_{\infty}^{-\infty} \frac{dU}{1+\alpha e^{U_F - U} + \gamma e^{U - U_F - \xi}} \quad (70)$$

$\left.\frac{dU}{dx}\right|_{d_o} = -\frac{q}{kT}E = -\frac{E_o}{\beta}$ $\left(\beta = \frac{kT}{q}\right)$ is the value of dU/dx at the inflection point and this value is assumed to be constant across the entire film. This assumption is valid since the surfaces do not contribute to the effective generation width.

$$\therefore W_{eff} = \frac{-\beta}{E_o} \int_{\infty}^{-\infty} \frac{dU}{\gamma e^{-(U_F+\xi)} e^{U} + \alpha e^{U_F} e^{-U} + 1} = \frac{\beta e^{U_F+\xi}}{\gamma E_o} \int_{-\infty}^{\infty} \frac{e^U \, dU}{e^{2U} + \frac{e^{U_F+\xi}}{\gamma} e^U + \frac{\alpha e^{(2U_F+\xi)}}{\gamma}}$$

$$= \frac{\beta e^{U_F+\xi}}{\gamma E_o} \int_0^{\infty} \frac{dy}{y^2 + \frac{e^{U_F+\xi}}{\gamma} y + \frac{\alpha e^{(2U_F+\xi)}}{\gamma}} \quad (71)$$

The discriminant of the quadratic expression in the denominator is,

$$\Delta = b^2 - 4ac = \frac{e^{2U_F+2\xi}}{\gamma^2} - 4\frac{\alpha}{\gamma} e^{2U_F+\xi} = \frac{e^{2U_F+\xi}}{\gamma}\left[\frac{e^{\xi}}{\gamma} - 4\alpha\right] = \frac{e^{2U_F+\xi}}{\gamma^2}\left[e^{\xi} - 4\alpha\gamma\right] \quad (72)$$

$$\therefore \quad W_{eff} = \frac{\beta e^{U_F+\xi}}{\gamma E_o} \frac{\gamma}{e^{U_F+\xi/2}(e^{\xi} - 4\alpha\gamma)^{1/2}} \ln\left[\frac{2y + \frac{e^{U_F+\xi}}{\gamma} - \frac{e^{U_F+\xi/2}}{\gamma}(e^{\xi} - 4\alpha\gamma)^{1/2}}{2y + \frac{e^{U_F+\xi}}{\gamma} + \frac{e^{U_F+\xi/2}}{\gamma}(e^{\xi} - 4\alpha\gamma)^{1/2}}\right]_0^{\infty}$$

$$= -\frac{\beta}{E_o}\frac{e^{\xi/2}}{(e^{\xi}-4\alpha\gamma)^{1/2}}\ln\left[\frac{\frac{e^{U_F+\xi}}{\gamma}-\frac{e^{U_F+\xi/2}}{\gamma}(e^{\xi}-4\alpha\gamma)^{1/2}}{\frac{e^{U_F+\xi}}{\gamma}+\frac{e^{U_F+\xi/2}}{\gamma}(e^{\xi}-4\alpha\gamma)^{1/2}}\right] = -\frac{\beta}{E_o}\ln\left[\frac{e^{\xi}-e^{\xi/2}(e^{\xi}-4\alpha\gamma)^{1/2}}{2e^{\xi}}\right]$$

$$= -\frac{\beta}{E_o}\ln\left[\frac{1-e^{-\xi/2}(e^{\xi}-4\alpha\gamma)^{1/2}}{2}\right] = -\frac{\beta}{E_o}\ln\left[\frac{1-(1-4\alpha\gamma e^{-\xi})^{1/2}}{2}\right] = -\frac{\beta}{E_o}\ln\left[\frac{1-(1-2\alpha\gamma e^{-\xi})}{2}\right]$$

$$= -\frac{\beta}{E_o}\ln\left[\frac{\alpha\gamma e^{-\xi}}{2}\right] = -\frac{\beta}{E_o}[\ln(\alpha\gamma)-\xi]$$

$$\bullet \quad W_{eff} = \frac{\beta}{E_o}[\xi - \ln(ay)] \tag{73}$$

Let (α,γ) be the 'true' values for the device fixed by the true values of $(\tau_{no}/\tau_{po}, E_T\text{-}E_i)$. Then, the measured ramp rate could be written as $R = \frac{qn_i}{C_{ox}\tau_g}\frac{\beta}{E_o}[\xi - \ln(\alpha\gamma)]$. Let us choose two arbitrary values of $(\tau_{no}/\tau_{po}, E_T\text{-}E_i)$ such that the chosen pair yields the 2-tuple (a,, γ_o). The effective generation width for this choice of trap parameters is $W_{eff} = \frac{\beta}{E_o}[\xi - \ln(\alpha\beta)]$. The slope of the R v/s W_{eff} line is

$$\frac{dR}{dW_{eff}} = \frac{dR/d\xi}{dW_{eff}/d\xi} = \frac{qn_i}{C_{ox}\tau_g}\left[\frac{E_o-(\xi-\ln(\alpha\gamma))^{dE}/_{d\xi}}{E_o-(\xi-\ln(\alpha_o\gamma_o))^{dE}/_{d\xi}}\right] \tag{74}$$

In order for the slope to be unique, a y = $\alpha_o\gamma_o$. Thus any choice of $(\tau_{no}/\tau_{po}, E_T\text{-}E_i)$ that satisfies the above condition will yield a unique value of τ_g, the generation lifetime.

6.3.4.2 Determining the Generation Lifetime

This section sketches the necessary steps to obtain the generation lifetime.

Step 1. Carry out the linear sweep experiment as detailed in section 6.3.2. Measure the saturated drain currents and the corresponding values of the ramp rate R.

Step 2. Measure the threshold voltage of the device under strong **accumulation**. Also measure the drain conductance of the MOSFET while operating the device in the linear region and at the same drain voltage at which the linear sweep measurement was made.

Step **3.** Calculate the saturated inversion charge density Qn_{sat} using eqn. (64).

Step **4.** Simulate the device for different values of 'ξ' and determine the simulated saturated inversion charge density $Qn_{sat,sim}$. The channel doping concentration and the oxide thickness could be varied to fit the simulated inversion charge density to the experimentally obtained value under equilibrium conditions.

Step 5. Use interpolation on the simulated ξ v/s $Qn_{sat,sim}$ curve to determine the values of ξ that correspond to the experimentally determined values of Qn_{sat}.

Step **6.** Compute the electric field (E_o) at the inflection point (d_o) for each value of ξ obtained in step 5, by running the analytical simulations again.

Step **7.** For an arbitrarily chosen value of τ_{no}/τ_{po}, W_{eff} is calculated using equation **(73)** for a range of values of E_T-E_i. The value of E_T-E_i at which the x-intercept of the W_{eff} v/s R plot becomes zero is determined.

Step 8. The slope of the W_{eff} v/s R plot is used to calculate the generation lifetime according to eqn. (68).

6.3.4.3 A Final Note

The linear sweep technique has its advantages over the pulsed technique because it is easy to analyze and it becomes possible to determine τ_g without making any assumptions on the values of trap parameters. Typically, the pulsed measurement techniques require differentiation of experimental data which can produce extremely noisy results. The linear sweep technique avoids any such differentiation. Finally, in the above analysis, surface generation is not taken into account. If there were a small surface component to the generation, or there is a small constant generation term either due to oxide leakage or drain field effects, then the W_{eff} v/s R plot would not have a zero x-intercept. In this case, the algorithm is modified to pick out the E_T-E_i for which the W_{eff}

v/s R plot shows the smallest deviation from the straight line. (i.e. for which the relative error of the least squares fit is minimum).

The methodology used to determine W_{eff} can be easily adapted to generation lifetime measurements made on gate contolled diodes fabricated in fully depleted SOI MOSFETs. Indeed in a gate controlled diode, the quasi-fermi level is directly determined by the applied idode bias, and the effective generation width can be obtained in a manner similar to that discussed above. In this case, however, the generation lifetime is determined from the linear slope of a W_{eff} v/s I_D plot where I_D is the measured reverse bias diode current, which is predominantly determined by bulk generation, provided the gate is biased suitably.

Finally, in the above analyis the channel mobility is assumed to be constant under the different non-equilibrium conditions. This is not a bad assumption provided the gate oxides are thick and the effect of the perpendicular electric field on the mobility is minimal. However for thinner gate oxides the channel mobility could show a significant dependence on the transverse surface electric field which could result in an overestimation of the generation lifetime. The linear sweep technique., by virtue of its quasi-steady state computations, lends itself to the potential for correcting for the decreased channel mobility at each saturated point.

6.4 Experimental Results

Fully depleted p-channel SOI MOSFETs were fabricated on SIMOX substrates. The process flow was presented in Chapter 4. The schematic diagram of the fabricated MOSFET is shown in figure 6.18. The device is a mesa-isolated edgeless MOSFET. Excess carrier generation at the device edges is avoided in an edgeless geometry. The gate length is approximately 2.0 μm. A total of four devices on two SIMOX substrates were measured, three from one wafer and one from the other. A summary of the device parameters for the four samples are shown in Table 6.1. In sample G, which was fabricated on a n-type substrate, the substrate was implanted n+, prior to metallization. The film thickness was determined from profilometric measurements. The back oxide thickness was provided by the vendor. The nominal value of the back oxide thickness was changed to match the simulated and experimental inversion charge density. The

front gate oxide thickness was again determined from profilometric measurements on thickness measurement bars fabricated on the same die.

Table 6.1 Device Parameters for the Four Samples used in the Linear Sweep Measurement

	Substrate	t_{oxf}	t_{oxb}	t_{si}	N_D	G_D	$V_{Tf,acc}$
Sample C	p-type	550Å	3100Å	1500Å	$1.8x10^{15}$	52.8e-6	-6.5
Sample D	p-type	550Å	3085Å	1500Å	$1.8x10^{15}$	44.2e-6	-6.44
Sample E	p-type	550Å	3100Å	1500Å	$1.8x10^{15}$	48.9e-6	-6.68
Sample G	n-type	500Å	4100Å	1400Å	$1.6x10^{15}$	43.6e-6	-9.05

All the electrical measurements were made using the HP4145B. The ramp rate in the 4145B was adjusted by varying the number of points chosen for a given sweep. The time taken for the sweep was measured using a stop watch. Each sweep was carried out five times and the measured time was averaged so that any errors in the measurement of the ramp rate would be minimized. Contrary to the measurement description presented in the earlier sections, the back gate was maintained in strong inversion while the front gate was swept to greater accumulation with varying ramp rates. Since the back gate oxide is very thick, the effect of perpendicular electric fields on the back gate characteristics is minimized. This strengthens the constant mobility assumption made in the theoretical analysis.

The front gate and back gate sub-threshold characteristics for sample E are shown in fig. 6.19. The front gate sub-threshold characteristics vary with the back gate voltage and vice-versa. This confirms that the SOI MOSFET is indeed fully-(depleted. The subthreshold slope also depends on the charge state of the other interface, which is again indicative of a fully depleted film. The back gate subthreshold curves cease to vary once the front gate voltage reaches 2V. Thus the front interface is strongly accumulated at 2V and the linear sweep was therefore initiated at 3V. The back gate drain conductance

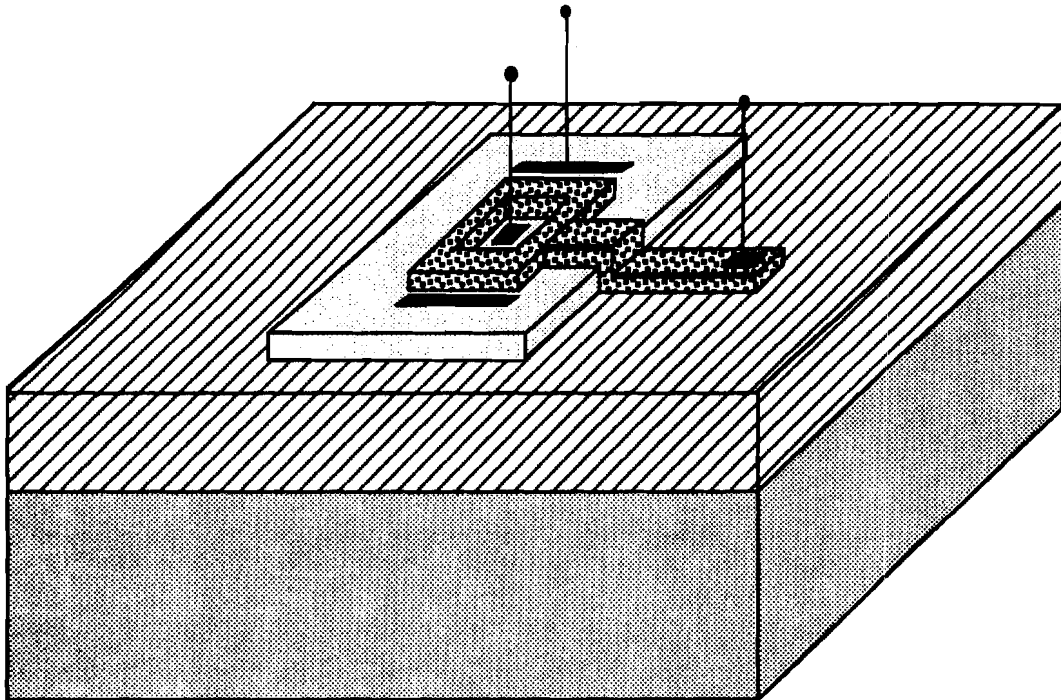
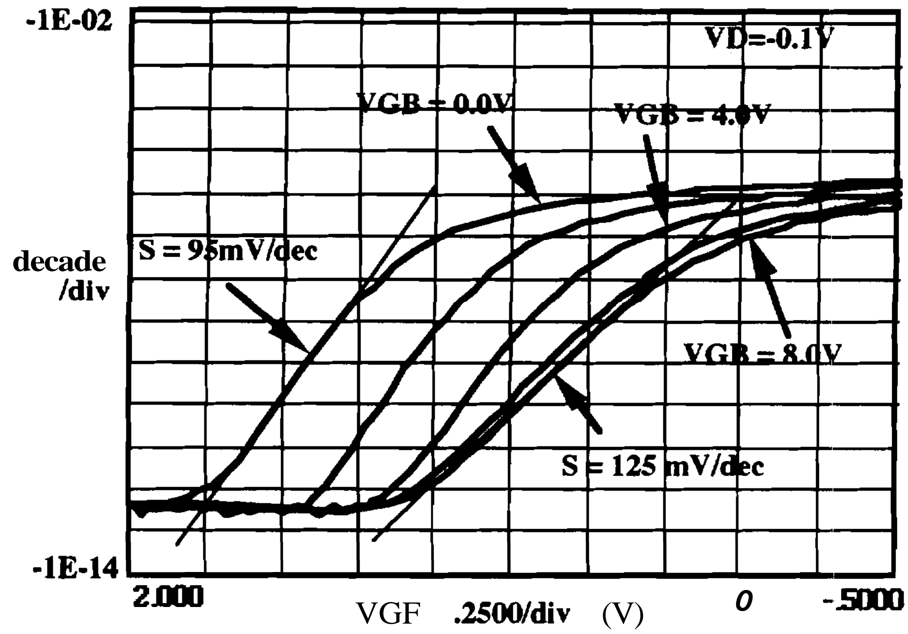
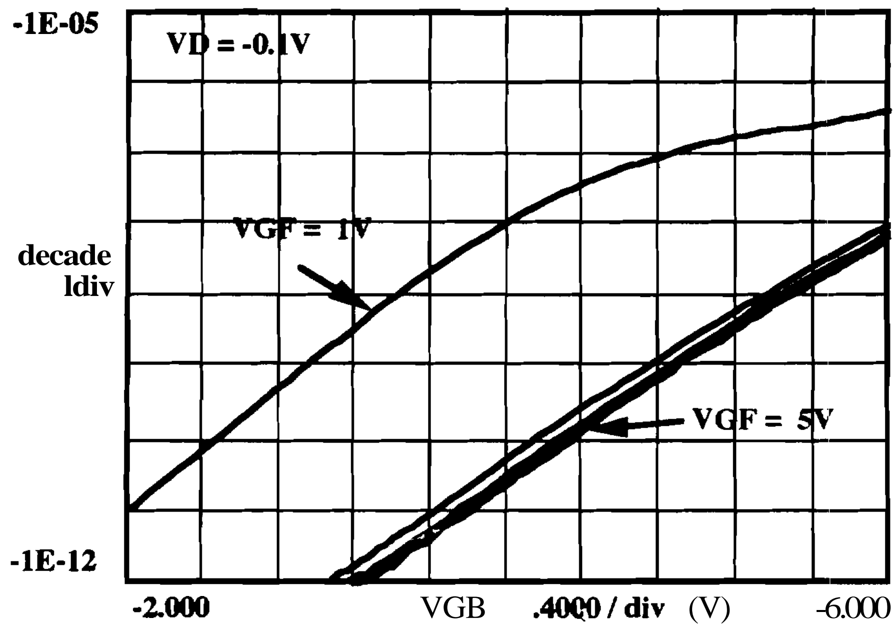


Figure 6.18 A schematic illustration of the edgeless mesa-isolated SOI MOSFET fabricated on a SIMOX substrate



(a)



(b)

Figure 6.19 Subthreshold characteristics for Sample E (a) front gate and (b) back gate. In each case the other gate is used as a second variable parameter

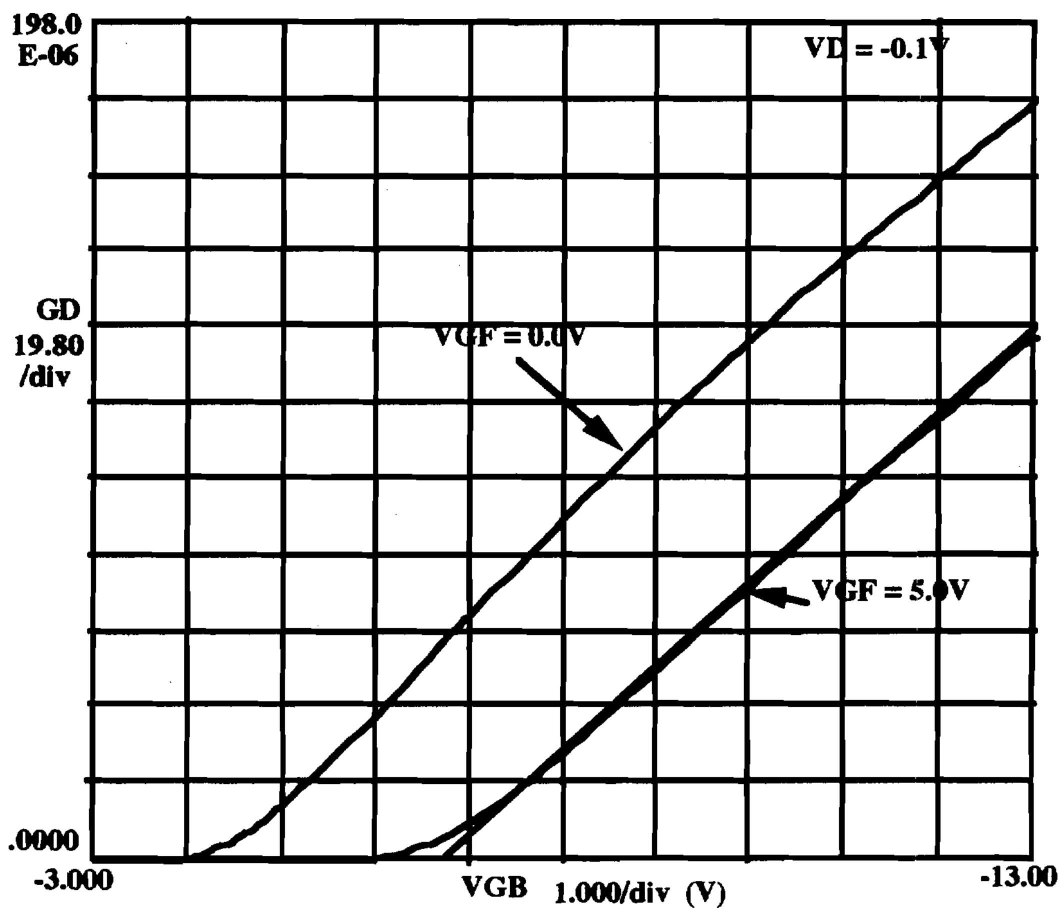


Figure 6.20 Drain conductance for Sample E under back gate operation. The front gate is strongly accumulated at 5.0V. The drain conductance and the back gate threshold voltage are measured with the front gate in strong accumulation

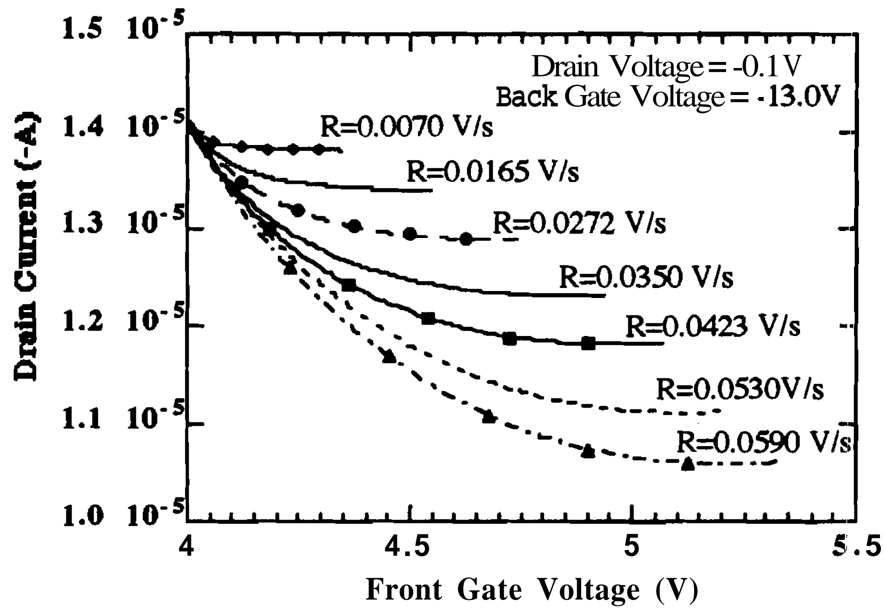
curve with the front gate biased in accumulation is shown in fig. 6.20 for the same device. The linear drain conductance region shows no deviation from linearity even for large back gate voltages. This confirms the weak dependence of the channel mobility on the perpendicular electric field.

The linear sweep characteristics for sample E are presented in fig. 6.21 (a) and the corresponding W_{eff} v/s R plot is presented in fig. 6.21 (b). The linear sweep characteristics show well saturating curves just as was expected from the theory developed earlier. In computing W_{eff}, τ_n/τ_p was assumed to be 100.0, since the ratio of the capture cross-sections of electrons to holes is typically 100.0. E_T-E_i was varied till the relative error of the least squares fit became minimum. This also gave a x-intercept very close to zero. The x-intercept could not be made exactly zero, possibly due to an extraneous generation term as discussed in the previous section. The generation lifetime is determined from the slope of the line to be 1.7 μsec. This value agrees with typical numbers quoted for SIMOX wafers.

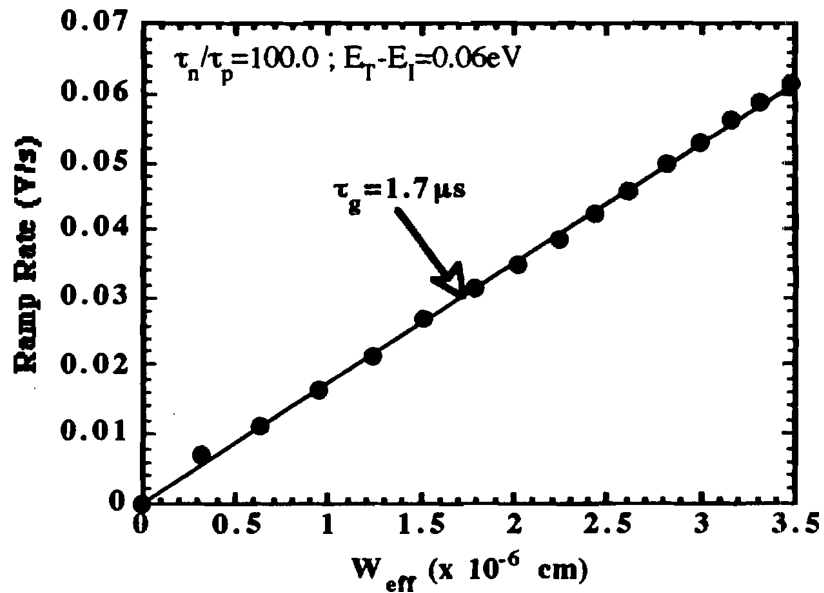
Linear sweep measurements were also made on two other devices fabricated on the same wafer. The measured linear sweep characteristics and the W_{eff}-R plot for samples C and D are shown in figs. 6.22 and 6.23. Finally, the technique was also applied to a device fabricated on the second SIMOX wafer (sample G). Its characteristics are shown in fig. 6.24. The measured generation lifetime values on all the samples arc summarized in Table 6.2.

Table 6.2 Summary of Measured Generation Lifetimes

	Generation Lifetime
Sample C	2.3 μs
Sample D	2.4 μs
Sample E	1.7 μs
Sample G	0.3 μs

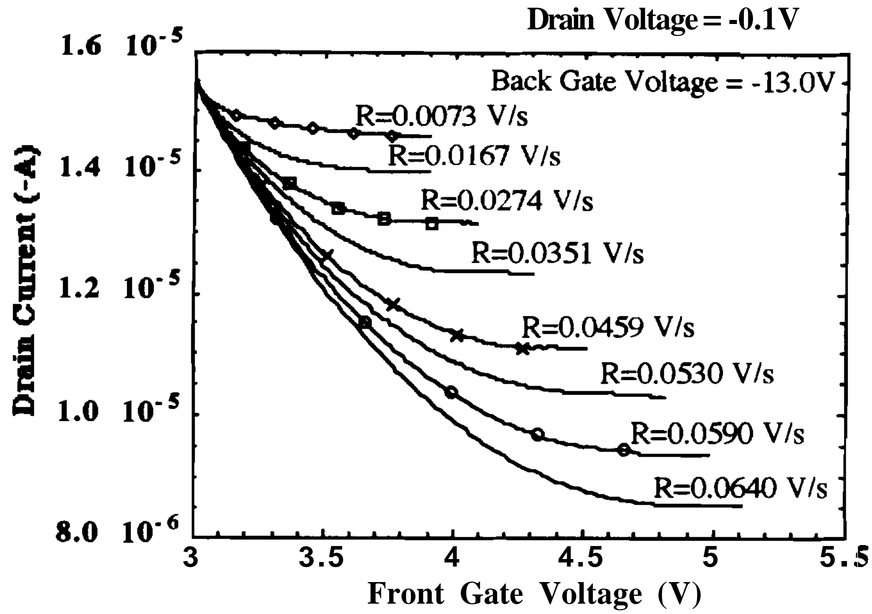


(a)

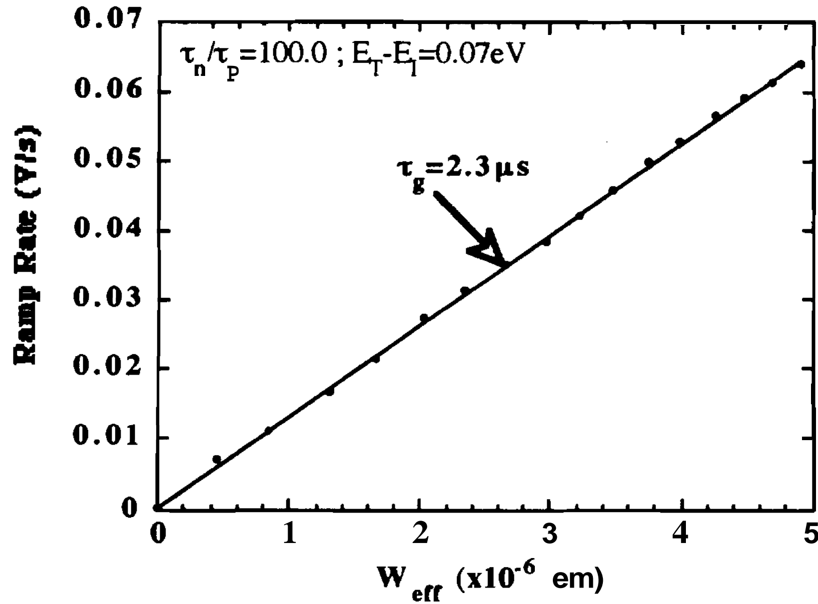


(b)

Figure 6.21 (a) The linear sweep characteristics for smaple E and (b) the corresponding W_{eff} v/s R plot



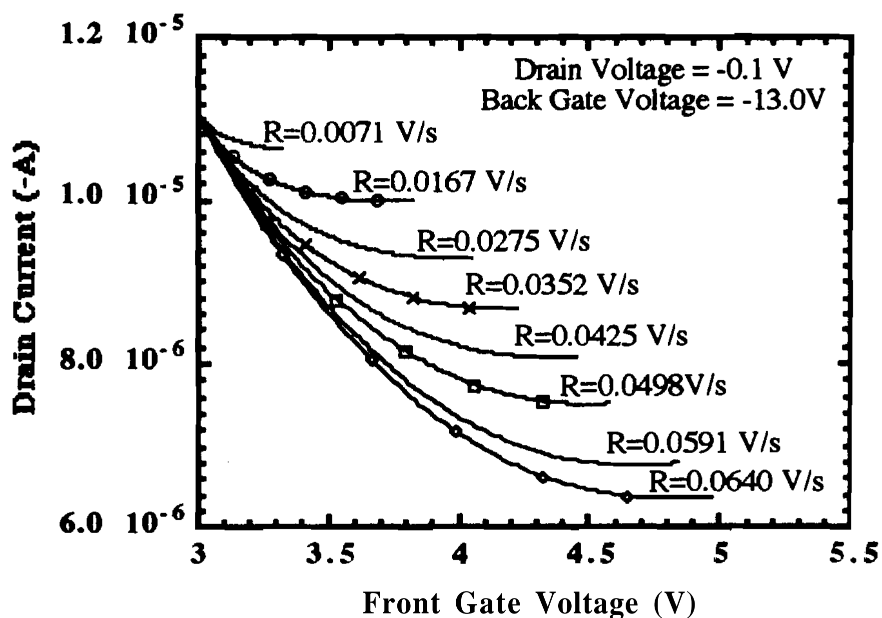
(a)



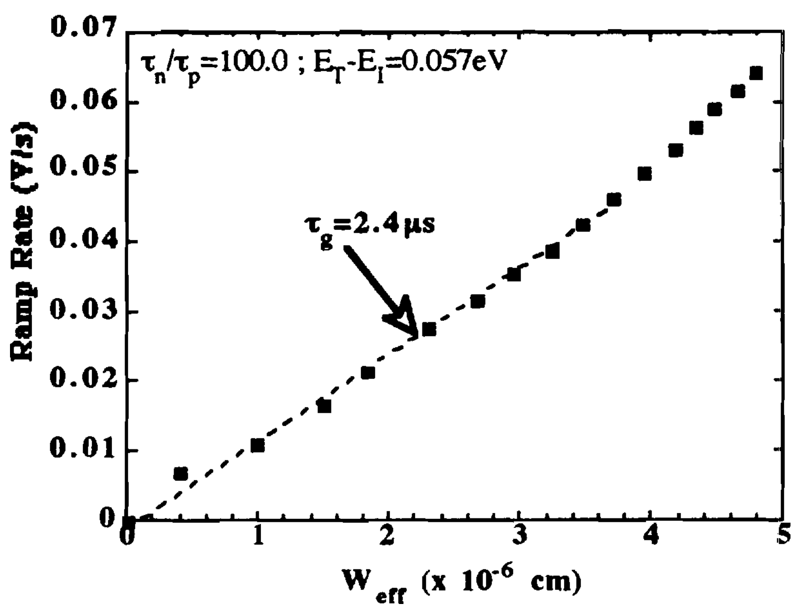
(b)

Figure 6.22 (a) The linear sweep characteristics for smaple C and (b) the corresponding W_{eff} v/s R plot

SIMOX PMOS - Sample D

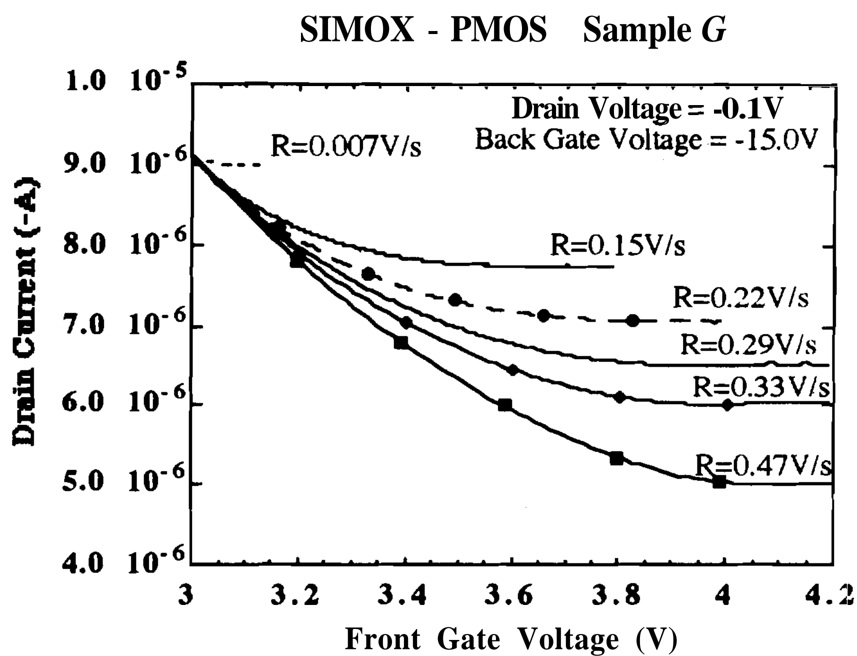


(a)

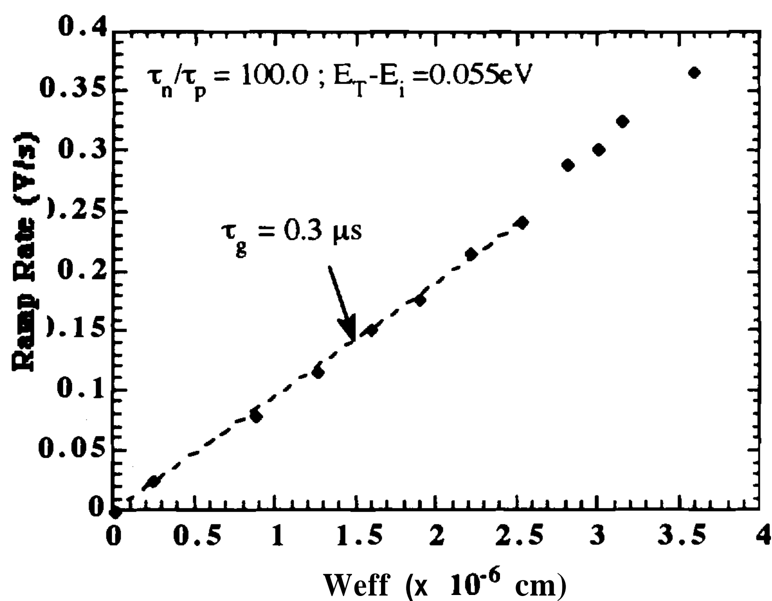


(b)

Figure 6.23 (a) The linear sweep characteristics for smaple D and (b) the corresponding W_{eff} v/s R plot



(a)



(b)

Figure 6.24 (a) The linear sweep characteristics for smaple G and (b) the: corresponding W_{eff} v/s R plot

6.5 Conclusions

A new generation lifetime measurement technique was proposed and verified. The analytical formulations that described the device behavior under linear sweep conditions were developed and the device behavior was successfully simulated. The linear sweep technique was applied to both the partially depleted and fully depleted SOI MOSFETs and the theoretical derivations of the appropriate formulas were presented. Finally a novel algorithm to accurately determine the generation lifetime without a requiring unique knowledge of the trap related parameters in the device was detailed and the measurement technique was experimentally verified by applying the procedure to fully depleted SIMOX MOSFETs. The generation lifetime values achieved on the SIMOX devices ranged from 0.3 μs to 2.4 ps, which is a fairly typical range for SIMOX material.

6.6 References

1. S.M. Sze, "Physics of Semiconductor Devices", *J. Wliley & Sons,* 2nd Edition, New York, 1981.

2. R.F. Rerret, "Advanced Semiconductor Fundamentals", vol VI *, Modular Series on Solid State Devices, Addison Wesley Publ. Co.* , Reading, *MA*, 1986.

3. D.K. Schroder, "Advanced MOS Devices", *Modular Series on Solid' State Devices, Addison Wesley Publ. Co.,* Reading, *MA,* 1987.

4. C. Jund and R. Poirier, "Carrier concentrations and minority carrier lifetime measurement in silicon epitaxial layers by the MOS capacitance method", *Solid State Electron.,* vol. 9, pp. 315, 1966.

5. M. Zerbst, "Relaxationseffekte an Halbleiter-Isolator-Grenzflächen", *Z. Angew. Phys.,* vol. 22, pp. 30, May 1966.

6. F.P. Heimen, "On the determination of minority carrier lifetime from the transient response of an MOS capacitor", *IEEE Trans. on Electron Devices,* vol. ED-14, pp. 781, Nov. 1967.

7. D.K. Schroder, "Semiconductor Material and Device Characterization", *John Wliley and Sons,* New York, 1990.

8. J.S. Kang and D.K. Schroder, "The pulsed MIS capacitor - a critical review", *Phys. Stat. Sol.,* vol. 89a, pp. 13, May 1985.

9. K.S. Rabbani and D.R. Lamb, "On the Analysis of pulsed MOS capacitance measurement", *Solid State Electron.,* vol. 21, pp. 1171, 1978.

10. X. Zhang, "An improved model of 'generation width' for pulsed MOS C-t transient analysis", *Solid State Electron.,* vol. 33 (9), pp. 1139, 1990.

11. R.F. Pierret, "Rapid interpretation of the MOS-C C-t transient", *IEEE Trans. on Electron Devices,* ED-25 (9), pp. 1157, Sept. 1978.

12. R.F. Rerret, "A Linear Sweep MOS-C technique for determining minority carrier lifetimes", *IEEE Trans. on Electron Devices,* ED-19 (7), July 1972.

13. A.S. Grove, "Physics and Technology of Semiconductor Devices", *John Wiiley and Sons,* New York, 1967.

14. N.M Johnson and A. Chiang, *IEEE Trnas. on Electron Devices,* ED-32, pp. 1559, 1985.

15. P.C. Yang and S.S. Li, "Determination of excess carrier lifetimes in silicon-on-insulator wafers by a contactless optical technique", *Intl. SOI Conference Proceedings,* pp. 14, 1992.

16. N.M. Johnson, "Electrical Characterization of crystallized-silicon thin films", *Mat. Res. Soc. Symp. Proc.,* vol. 53, pp. 337, 1986.

17. A. Chantre, D. Ronzani and D.P. Vu, "Minority carrier lifetime studies in halogen lamp recrystallized SOI films", *Mat. Res. Soc. Symp. Proc.*, vol. 53, pp. 349, 1986.

18. T.I. Kamins, "Minority carrier lifetime in dielectrically isolated single-crystal silicon films defined by electrochemical etching", *Solid State Electron.,* vol. 17, pp. 675, 1974.

19. T. Elewa, H. Haddara and S. Cristoloveanu, "Interface properties and recombination mechanisms in SIMOX structures", in ***The Physics and Technology of Amorphous*** SiO_2, R.A.B. Devine *Ed.,* New York, pp 553, 1988.

20. J.C. Sturm, J.D. Plummer and J.F. Gibbons, "Measurement and reduction of interfaces states at the recrystallized silicon-underlying insulator interface", *Appl. Phys. Lett.,* vol. *46* (12), pp. 1171, June 1985.

21. D.P. Vu and J.C. Pfister, "Characterization of beam-recrystallized Si films and their Si/SiO_2 interfaces in silicon-on-insulator structures", *Appl. Phys. Lett.,* vol. *48* (1), pp. 50, Jan. 1986.

22. P.K. McLarty, T. Elewa, B. Mazhari, M. Mukherjee, T. Ouisse, S. Cristoloveanu, D.E. Ioannou and D.P. Vu, "Minority carrier generation in very thin silicon on insulator films", *Proceedings of the Intl. SOI Conference,* pp. *54,* 1990.

23. D.P. Vu and J.C. Pfister, "Determination of minority carrier generation lifetimes in beam-recrystallized silicon-on-insulator by using a depletion mode transisotr", *Appl. Phys. Lett.*, vol. 47, pp. 950, Nov. 1985.

24. T. Elewa, H. Haddara and S. Cristoloveanu, Tamer generation and trapping properties in SIMOX structures", in *Solid State Devices,* G. Soncini and P.U. Calzolari (Eds.), pp. 599, Elsevier Science Publishers B.V (North-Holland), 1988.

25. S. Cristoloveanu, "Electrical evaluation of SIMOX material and integrated devices", *Mat. Res. Soc. Symp. Proc.,* vo. 107, pp. 335. 1988.

26. P.W. Barth and J.B. Angell, "A dual-gate deep-depletion technique for generation lifetime measurements", *IEEE Trans. on Electron Devices,* vol. ED-27 , pp. 2252, Dec. 1980.

27. M. Mukherjee, D.E. Ioannou, S. Cristoloveanu and B. Mazhari, "Characterization of carrier generation in enhancement-mode SOI MOSFETs", *IEEE Electron Device Letters,* EDL-11 (9), pp. 409, Sept. 1990.

28. L.T. McDaid, et al. , *IEEE Electron Device Letters,* vol. EDL-12, pp. 318, June 1991.

29. N. Yasuda et al., "A new lifetime measurement technique for fully deplsted SOI MOSFETs", *IEEE Trans. on Electron Devices,* vol. ED-39, pp. 1197, May 1992.

CHAPTER 7
CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

Microelectronics has in recent years seen a relentless drive towards aggressive scaling of semiconductor device dimensions. The minimum feature size of devices, which in CMOS technology is determined by the gate length, is already down to 0.4μm and active research is being carried out to advance technology to the 0.25μm regime. Further scaling of device dimensions is however yielding diminishing returns, largely due to the prohibitively increased cost of CMOS process development, increased process complexity and the need to revamp and retool the manufacturing technology for each new generation of microprocessors[1]. In order to make further advances financially profitable, what is really needed is a way to maintain the current manufacturing sophistication and the current feature sizes, while at the same time achieving a future generation in terms of speed. Silicon-on-insulator technologies satisfy this rather challenging criteria. The reduced parasitic capacitances in SOI (both individual device parasitics and global parasitics such as wiring and line capacitances) result in speed performances which are on an average about three times faster than that in a comparable CMOS technology.

SIMOX technology currently represents the state-of-the-art in SOI development. However selective epitaxial techniques such as Epitaxial Lateral Overgrowth (ELO) and Confined Lateral Selective Epitaxial Growth (CLSEG) provide a simpler and far cheaper option as compared to SIMOX, while simultaneously providing circuit designers vast freedom in designing circuits with mixed substrate and SOI device components. Consequently, the prime objective of this research was to advance the state-of-the-art of

[1]Microprocessors like DRAMs , form the technology driver for new generations of process technologies.

ELO and CLSEG for competitive SOI VLSI applications. In this regard, fully-depleted SOI devices were fabricated simultaneously in ELO, CLSEG and SIMOX in order to maintain a fair comparison between the properties of the three materials. Results from this work indicate that ELO and CLSEG are of at least as good if not better quality than SIMOX. This conclusion coupled with the flexibility offered by the selective epitaxy techniques makes ELO and CLSEG a far more competitive technology for SOI VLSI.

Thin-film ($\approx$ 1500Å) fully-depleted SOI MOSFETs fabricated in CLSEG grown in pre-defined 2500Å cavities were fabricated for the first time. Both n-channel and p-channel devices exhibited excellent device characteristics and effective hole mobilities approaching 240 $cm^2/V\text{-}sec$ were extracted from the PMOSFETs. The absence of the kink-effect in the n-channel transistors proved that the devices were indeed fully-depleted. In addition, fabrication of thin-film fully-depleted dual-gated devices were attempted in CLSEG for the first time and marginal success was achieved.

In order to take advantage of the flexibility offered by ELO, dual-gated fully-depleted SOI MOSFETs were fabricated at Purdue for the first time. The devices showed excellent properties and the effective electron and hole mobilities obtained on the devices were comparable to the devices fabricated with a single gate. The quality of the epitaxial material was found to depend on the step height of the bottom polysilicon gate. When the step height was about 5000Å, the material developed a lot of edge defects along the growth front that encountered the step. The defects were considerably reduced if the step height was maintained less than 3000Å. Thus for best material, ELO growth must be initiated and maintained along a smooth planar surface. In this regard, the bottom-gate of the dual-gated devices must be recessed in the field oxide.

A new linear sweep technique to determine generation lifetime measurements in thin-film SOI material using a fully-depleted thin-film SOI MOSFET was developed. This technique provides an accurate measure of the generation lifetime and makes no approximations in its theoretical development, unlike the other electrical techniques proposed in the literature. An accurate analytical formulation for the 1-D dual-gated SOI MOSFET was developed for both equilibrium and non-equilibrium conditions. The exact solution to Poissons equation was then used to simulate the behavior of the SOI MOSFETs under the proposed linear sweep conditions. The new technique was then applied to fully-depleted thin-film SOI MOSFETs fabricated on SIMOX material and an average lifetime of 2μs was extracted from devices across the wafer.

The effects of volume inversion in enhancing the properties of dual-channel MOSFETs were investigated using two-dimensional device simulaticns and one-dimensional analytical computations. It was shown that the output characteristics of dual-channel devices were not significantly enhanced over those of single-channel devices when the two devices were compared at constant V_G-V_T.

A novel process sequence for self-aligning the top and bottom gates in a dual-gated SOI MOSFET was presented. The device has significant advantages over existing dual-gated SOI MOSFET technologies. The two gates can be independently biased which is essential for flexible design of SOI VLSI circuits. Furthermore, the top and bottom gates are self-aligned. This self-alignment minimizes parasitics and reduces active area. The device is fully scalable and in fact conforms in device structure to the proposed ultimate scalable MOSFET.

7.2 Recommendations

A major difficulty in fabricating the dual-gated devices using CLSEG arose from the fact that the bottom gate was not recessed. Using a recessed bottom gate would ensure a planar growth surface for CLSEG and ELO and would significantly ease the process development. However, the current mask design could not be used to fabricate the recessed structure. Consequently future research on dual-gated devices should incorporate recessed bottom gate for improved material quality as well as ease of fabrication.

A second major drawback of the dual-gated devices was the fact the top and bottom devices in the dual-gated structure were not symmetrical. The bottom gate oxide was always grown thicker than the top gate oxide, and to be absolutely certain that the oxide didn't degrade under the adverse selective epitaxy conditions, the oxide was made 1500Å thick. In addition, there was a lot of arsenic out-diffusion from the bottom poly gate which pushed the threshold voltage of the bottom device higher than that of the top gate. In order to counter both these problems, further investigations must be made on the possibility of using alternate dielectrics such as nitrided oxides or oxide/nitride stacks.

Although it was the original intent to study the interface traps at the front and back interfaces of the ELO devices and compare them to the SIMOX devices, difficulties

encountered in processing precluded the fabrication of the five-terminal devices that could be used for making charge-pumping measurements. Alternate schemes to measure the front and back interface state densities must be exploited. The process flow for fabricating the SOI MOSFETs must be modified so that photo-resist need not be used as an implant mask. Moreover, the mesa-isolation process must be optimized for making better quality NMOS devices with sharp subthreshold slopes. In this regard, the optimum mask design for ELO and CLSEG would be to first grow the epitaxy material from a long seedhole and then segment this epitaxial region into requisite active areas. This is opposed to the mask design which was adopted in the current research in which each device had its own respective seedhole.

The generation lifetime measurement technique must be applied to both the ELO and CLSEG material to determine the lifetimes in the selective epitaxy material and then compare them to those in the SIMOX material. The modified linear sweep method that incorporates a feedback loop can be applied in cases where the ramp rate is very small. This would speed up the data acquisition process.

Finally, the fully self-aligned process detailed in the thesis can he attempted to achieve the ultimate scalable MOSFET structure.

APPENDICES

Appendix A - Run Sheets

RUN SHEET
DUAL-GATE SOI MOSFET USING
ELO

Process Steps | Date/Time

1. Start with p-type <100> wafers. Number of wafers ________
   Process run nomenclature ______________
   Resistivity ____________ ____________

2. **Degrease** the wafers
   (a) TCA - ultrasonic - 10 mins ____________
   (b) ACE - ultrasonic - 10 mins ____________
   (c) METH - ultrasonic - 10 mins ____________
   (d) DI Rinse - 5mins ____________

3. PIRANHA clean. 2:1 :: H_2O_2 : H_2SO_4 - 10 mins ____________
   DI Rinse - 10 mins ____________

4. FIELD OXIDATION - Tube#4 - H_2 Burn - 2000Å
   Time ________ Temp __________
   Color ________ Approx. Thickness ____________ ____________
   Comments:

5. PIRANHA clean - 2:1 :: H_2O_2:H_2SO_4 - 10 mins
   DI Rinse - 10 mins ____________
   (unless the process is continued immedialtely after field oxidation)

6. Polysilicon deposition for Gate1. (3000Å)
   Temp : 550°C Time: ________ Pressure: __________
   Gas Flow rates : SiH_4 __________ ____________
   Comments:

7. Polysilicon Doping. Use Spin-on dopant for Arsenic
   Prebake at 150 °C for 20 mins. Wait for the wafer to cool.
   Spin the dopant on at 1000rpm for 20 secs. Bake at 150 °C for
   15 mins. Introduce slowly into the furnace at 1100 °C and anneal
   for 1 hour. Wait for the wafers to cool completely before dipping
   in BHF.
   Parameters : ______________________________
   Sheet Resistivity : ______________________ ____________

8. PHOTOLITHOGRAPHY # 1
   (a) Expose wafers to HMDS - 5 mins ____________
   (b) Spin positive photoresist Speed: 4000rpm, Time: 40 secs ____________
   (c) **Prebake** Temp: 95°C Time: 30 mins ____________
   (d) Expose Time: 7.5 secs POLY GATE 1 MASK ____________
   (e) Develop in AZ351 1:5 ____________
   (f) **Post bake** Temp: 120°C Time: 20 mins ____________

9. RIE Material etched: Oxide, Gas used: Freon 115,

Time: _________ , Power: __________ , Flow: __________ ____________
Etch Rate: _________
Comments:

10. Remove the positive photoresist with acetone. ____________
TCA, ACE, METH, DI clean ____________

11. PIRANHA clean - 2:1 :: H_2O_2:H_2SO_4 - 10 mins ____________
DI Rinse - 10 mins ____________

12. Remove surface oxide with a BHF dip. ____________

13. Bottom Gate Oxidation. Tube#1, Dry/Wet Oxide. (1500 Å)
Temperature: _________, Time : ____________, O_2: ________
Color : _____________ ____________
Comments:

14. PIRANHA Clean. 2:1 :: H_2O_2:H_2SO_4 - 10 mins
DI Rinse - 10 mins ____________
(unless continuing the process directly after gate oxidation)

15. PHOTOLITHOGRAPHY # 2
(a) Expose wafers to HMDS ____________
(b) Spin AZ 1350 Positive Resist on.
Speed: 4400 rpm, Time: 40secs ____________
(c) Prebake. Temp: 95°C Time : 30 mins ____________
(d) Expose Time : 7.5 secs SEED HOLE MASK ____________
(e) AZ 351: H_2O :: 1:5 Develop for 40 secs. Agitate. ____________
(f) Postbake. Temp: 120°C. Time: 20 mins ____________

16. Wet etch Material Etched: Oxide, BHF
Etch Rate: ____________ ____________
Comments:

17. PIRANHA Clean. 2:1 :: H_2O_2:H_2SO_4 - 10 mins
DI Rinse - 10 mins ____________

18. BHF dip to clear seed hole (15-20 secs) Agitate ____________

19. PIRANHA Clean. 2:1 :: H_2O_2:H_2SO_4 - 10 mins
DI Rinse - 10 mins __________
Extremely important step. Make sure the wafers are thoroughly cleaned and blow dried.

EPITAXY STEP.
Growth Length: 13 microns. Growth Rate: ____________
Temp: ____________, Pressure: ______________________
Time: _____________ ____________
Comments: Determine the n-type doping based on threshold requirements.

21. Polysilicon deposition for the etch stop. Thickness 3000Å

Temp : 550°C Time: ________ Pressure: __________
Gas Flow rates : SiH_4 __________ ____________
Comments:

22. Oxidize the polysilicon 2000Å
Temperature: _________, Time : ___________, O_2: ________
Color : ____________ ____________
Comments:

23. Chemical Mechanical Planarization. Use a final 2355 planarization
Parameters : ________________________________ ____________

24. Determine Thickness of the SOI layer from alpha step measurements.
Thickness: ______________

At this stage, depending on whether the devices are PMOS or NMOS, there would have to be a boron counter-doping to make the channel doping p-type.

25. Define the active area mask. PHOTOLITHOGRAPHY # 3
   (a) Expose wafers to HMDS ____________
   (b) Spin AZ 1350 Positive Resist on.
   Speed: 4400 rpm, Time: 40secs ____________
   (c) Prebake. Temp: 95°C Time : 30 mins ____________
   (d) Expose Time : 7.5 secs A/A MASK ____________
   (e) AZ 351: H20 :: 1:5 Develop for 40 secs. Agitate. ____________
   (f) Postbake. Temp: 120°C, Time: 20 mins ____________

26. GATE OXIDATION. Tube # 5, Dry oxide, TCA. (550 Å)
Temp: ________, Time: ___________, O_2: ___________ ____________
Color: _______________, Thickness: ________________
Comments:

27. Polysilicon deposition for Gate2. (4000-4500Å)
Temp : 550°C Time: ________ Pressure: __________
Gas Flow rates : SiH_4 __________ ____________
Comments:

28. PHOTOLITHOGRAPHY # 4
   (a) Expose wafers to HMDS ____________
   (b) Spin AZ 4110 Positive Resist on.
   Speed: 4400 rpm, Time: 40secs ____________
   (c) Prebake. Temp: 90°C Time : 30 mins ____________
   (d) Expose Time : 6.5 secs POLY Gate 2 MASK ____________
   (e) AZ 351: H20 :: 1:5 Develop for 40 secs. Agitate. ____________
   (f) Postbake. Temp: 120°C, Time: 20 mins ____________

36. RIE. Material Etched: Poly, Gas Used: Fr115
Time: _________, Power: _________, Gas Flow: ________ ____________

37. Remove Photoresist. ACE, METH, DI Rinse ____________

38. PIRANHA Clean. 2:1 :: H_2O_2:H_2SO_4 - 10 mins

DI Rinse - 10 mins ____________

39. Source/Drain Implant for self-aligned process
Dose: Energy: ____________

40. Source/Drain Anneal
Temp: ________, Time: ____ , O_2: ____________ ____________
Color: ________________, Thickness: ________________
Comments:

41. PHOTOLITHOGRAPHY # 5
(a) Expose wafers to HMDS ____________
(b) Spin AZ 4110 Positive Resist on.
Speed: 4400 rpm, Time: 40secs ____________
(c) Prebake. Temp: 90°C Time : 30 mins ____________
(d) Expose Time : 6.5 secs CONTACT MASK ____________
(e) AZ 351: H20 :: 1:5 Develop for 40 secs. Agitate. ____________
(f) Postbake. Temp: 120°C, Time: 20 mins ____________

42. BHF dip. ____________

43. PHOTOLITHOGRAPHY # 6
(a) Expose wafers to HMDS ____________
(b) Spin AZ 4110 Positive Resist on.
Speed: 4400 rpm, Time: 40secs ____________
(c) Prebake. Temp: 90°C Time : 30 mins ____________
(d) Expose Time : 6.5 secs Metalization MASK ____________
(e) AZ 351: H20 :: 1:5 Develop for 40 secs. Agitate. ____________
(f) Postbake. Temp: 120°C, Time: 20 mins ____________

44. METALLIZATION.
Parameters: ____
Thickness: ________________ ____________

45. Lift-Off metal. Agitate in Acetone. ____________

46. Remove Photoresist. ACE, METH, DI Rinse. ____________

47. Metallization Anneal. Tube # 8.
Temp: ________, Time: ____________ ____________

48. ELECTRICAL TESTING. ____________

RUN SHEET
DUAL-GATE SOI MOSFET USING
CLSEG

Follow steps detailed in the ELO process till step # 17

18. Oxidation to protect seed region (200Å)
Temp: 1000 °C, Time: 8 mins, Dry O_2 ____________

19. Amorphous silicon deposition. (3000 Å) SiH_4: ______
Temp: 550°C, Time: ________, Pressure: ________, ____________

Comments:

20. PHOTOLITHOGRAPHY # 3
    (a) Expose wafers to HMDS ____________
    (b) Spin AZ 1350 Positive Resist on.
        Speed: 4400 rpm, Time: 40secs ____________
    (c) Prebake. Temp: 95°C Time : 30 mins ____________
    (d) Expose Time : 7.5 secs AIA MASK ____________
    (e) AZ 351: H20 :: 1:5 Develop for 40 secs. Agitate. ____________
    (f) Postbake. Temp: 120°C, Time: 20 mins ____________

21. RIE. Material Etched: Polysilicon, Gas : Freon 115
    Time __________, Power: __________, Gas Flow: _________
    Etch Rate: ______________ ____________
    Comments: Etch to the field oxide. Remember thc color of the field oxide after the last oxidation.

22. Remove Photoresist. ACE, METH, DI Rinse ____________

23. PIRANHA Clean. 2:1 :: H_2O_2:H_2SO_4 - 10 mins
    DI Rinse - 10 mins ____________

24. OXIDATION to convert the A:Si to Poly. Tube # 1, Wet Oxide (1000 Å)
    Time : ________, Temp: ____________, O_2 : ____________ ____________
    Comments:

25. NITRIDATION. Deposit Cavity support nitride. (3000 Å)
    Temp : 800°C, Time : ________, SiH_2Cl_2:__________, NH_3: ________
    Color: __________________ ____________
    Comments:

26. PHOTOLITHOGRAPHY # 4
    (a) Expose wafers to HMDS ____________
    (b) Spin AZ 1350 Positive Resist on.
        Speed: 4400 rpm, Time: 40secs ____________
    (c) Prebake. Temp: 95°C Time : 30 mins ____________
    (d) Expose Time : 7.5 secs VIA HOLE MASK ____________
    (e) AZ 351: H20 :: 1:5 Develop for 40 secs. Agitate. ____________
    (f) Postbake. Temp: 120°C, Time: 20 mins ____________

27. RIE. Material Etched: Nitride, Gas: SF_6
    Time __________, Power: __________, Gas Flow: _________
    Etch Rate: ______________ ____________

28. Remove Photoresist. ACE, METH, DI Rinse ____________

29. PIRANHA Clean. 2:1 :: H_2O_2:H_2SO_4 - 10 mins
    DI Rinse - 10 mins ____________

30. BHF Dip to clear surface oxide ____________

31. EDP Etch to clear the polysilicon and open the cavity
    EDP composition ____________________
    Temp: __________, Time: ___________, Etch Rate: ____________________________
    Comments:

32. PIRANHA Clean. 2:1 :: H_2O_2:H_2SO_4 - 10 mins
    DI Rinse - 10 mins ____________

33. BHF dip to clear seed hole (200 Å, 15-20 secs) Ultrasonic ____________

34. PIRANHA Clean. 2:1 :: H_2O_2:H_2SO_4 - 10 mins
    DI Rinse - 10 mins ____________
    Extremely important step. Make sure the wafers are thoroughly cleaned and blow dried.

35. SILICON EPITAXY STEP.
    Growth Length: 13 microns. Growth Rate: ____________
    Temp: ____________, Pressure: ____________
    Time: ____________ ____________
    Comments: Determine the n-type doping based on threshold requirements.

36. Chemical Mechanical Planarization.
    Parameters: ____________ ____________

37. Remove nitride. Boil in Hot Phosphoric Acid.
    Time: ________, Temp: ____________ ____________
    Remove Oxide. BHF Dip.
    Time: ________, Temp: ____________ ____________

38. Determine Thickness of the SOI layer from alpha step measurements.
    Thickness: ____________

At this stage, depending on whether the devices are PMOS or NMOS, there would have to be a boron–counter-dop& to make the channel doping p-type.

39. GATE OXIDATION. Tube # 5, Dry oxide, TCA. (550 Å)
    Temp: ________, Time: ____________, O_2: ____________ ____________
    Color: ____________, Thickness: ____________
    Comments:

40. POLYSILICON DEPOSITION. Gate 2.
    Temp: 550, Time: ____________, Pressure: ____________ ____________
    Comments:

41. Polysilicon Doping. IF NECESSARY
    Parameters: ____________ ____________
    Sheet Resistivity: ____________

42. PHOTOLITHOGRAPHY # 5
    (a) Expose wafers to HMDS ____________
    (b) Spin AZ 1350 Positive Resist on.
        Speed: 4400 rpm, Time: 40secs ____________
    (c) Prebake. Temp: 95°C Time : 30 mins ____________
    (d) Expose Time : 7.5 secs POLY Gate 2 MASK ____________
    (e) AZ 351: H20 :: 1:5 Develop for 40 secs. Agitate. ____________
    (f) Postbake. Temp: 120°C, Time: 20 mins ____________

43. Poly Etch. Remove the excess polysilicon using a wet etch. Could also use the RIE. ____________

44. Remove Photoresist. ACE, METH, DI Rinse ____________

45. PIRANHA Clean. 2:1 :: H_2O_2:H_2SO_4 - 10 mins
DI Rinse - 10 mins ____________

AT THIS TIME THERE IS A CHOICE OF TWO PROCESSES. ONE IS A 7-MASK PROCESS WHICH COULD YIELD PMOS DEVICES (ie dual-gated PMOSFETs). BUT IT WOULD YIELD NOTHING ELSE. THE OTHER IS A 8-MASK PROCESS WHICH WOULD YIELD NMOS DEVICES, SUBSTRATE MOSFETS, DIODES, GATE-CONTROLLED DIODES AND SUBSTRATE CONTACTED DEVICES.

46. Implantation for Source/Drain regions
Parameters: ____________________ ____________

47. OXIDATION/ANNEAL. Tube # 4. H_2- bum. (1200Å)
Time: __________, Temp: __________, Color: ______________ ____________
Comments:

48. PHOTOLITHOGRAPHY # 6
(a) Expose wafers to HMDS ____________
(b) Spin AZ 1350 Positive Resist on.
Speed: 4400 rpm, Time: 40secs ____________
(c) Prebake. Temp: 95°C Time : 30 mins ____________
(d) Expose Time : 7.5 secs CONTACT MASK ____________
(e) AZ 351: H_2O :: 1:5 Develop for 40 secs. Agitate. ____________
(f) Postbake. Temp: 120°C, Time: 20 mins ____________

49. BHF dip. ____________

50. METALLIZATION.
Parameters: ____________________
Thickness: ____________________ ____________

51. PHOTOLITHOGRAPHY # 7
(a) Expose wafers to HMDS ____________
(b) Spin AZ 1350 Positive Resist on.
Speed: 4400 rpm, Time: 40secs ____________
(c) Prebake. Temp: 95°C Time : 30 mins ____________
(d) Expose Time : 7.5 secs Mettalization MASK ____________
(e) AZ 351: H_2O :: 1:5 Develop for 40 secs. Agitate. ____________
(f) Postbake. Temp: 120°C, Time: 20 mins ____________

52. Lift-Off metal. Agitate in Acetone. ____________

53. Remove Photoresist. ACE, METH, DI Rinse. ____________

55. Metallization Anneal. Tube # 8.
Temp: __________, Time: ______________ ____________

56. ELECTRICALTESTING. ____________

Appendix B - Layout and sizes of the different SOI structures

The following figures shows the layout and the widths of the four different devices used in the test mask set.

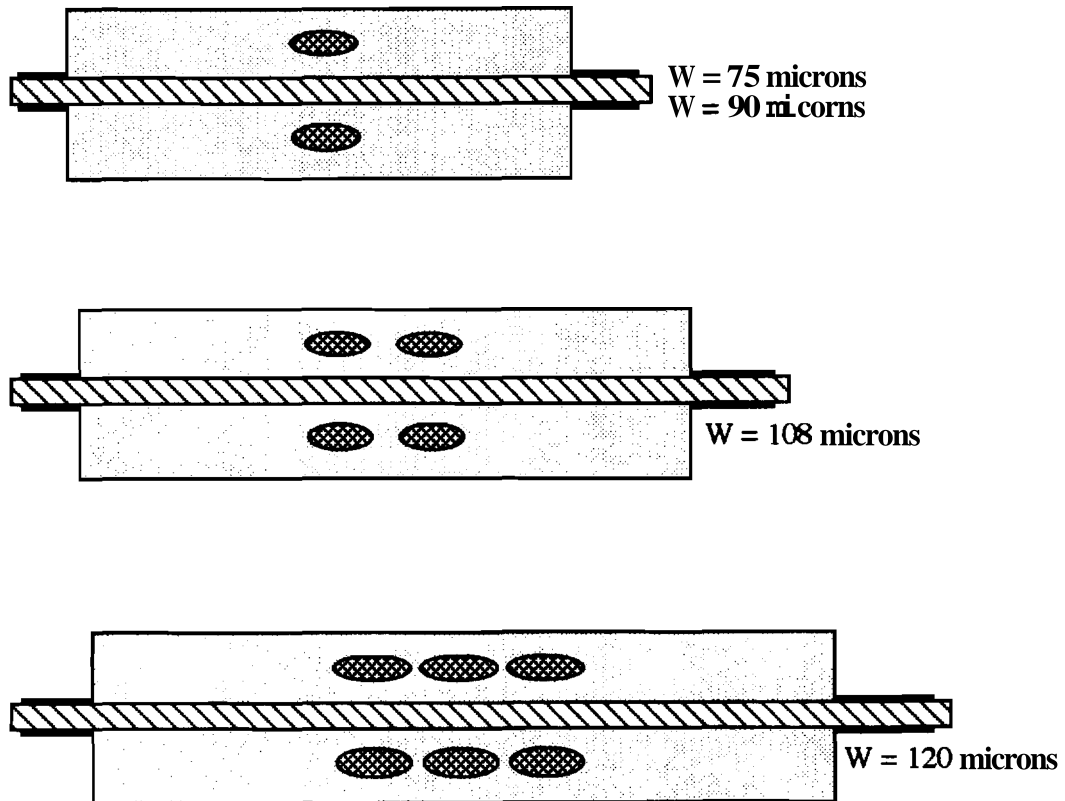


Figure B.1 Layout and sizes of the different SOI structures