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We report on nanoelectronic device applications of a nonalloyed contact structure which utilizes a surface layer of low-temperature grown GaAs as a chemically stable surface. In contrast to typical *ex situ* ohmic contacts formed on *n*-type semiconductors such as GaAs, this approach can provide uniform contact interfaces which are essentially planar injectors, making them suitable as contacts to shallow devices with overall dimensions below 50 nm. Characterization of the native layers and surfaces coated with self-assembled monolayers of organic molecules provides a picture of the chemical and electronic stability of the layer structures. We have recently developed controlled nanostructures which incorporate metallic nanoclusters, a conjugated organic interface layer, and the chemically stable semiconductor surface layers. These studies indicate that stable nanocontacts ($4\,\text{nm}\times 4\,\text{nm}$) can be realized with specific contact resistances less than $1\times 10^{-6}\,\Omega\,\text{cm}^2$ and maximum current densities ($1\times 10^6\,\text{A/cm}^2$) comparable to those observed in high quality large area contacts. The ability to form stable, low resistance interfaces between metallic nanoclusters and semiconductor device layers using *ex situ* processing allows chemical self-assembly techniques to be utilized to form interesting nanoscale semiconductor devices. This article will describe the surface and nanocontact characterization results, and will discuss device applications and novel techniques for patterning close-packed arrays of nanocontacts and for imaging the resulting structures. [S0734-211X(99)05504-3]

I. INTRODUCTION

There have recently been numerous examples of prototype electronic devices having nanometer scale dimensions.[1–4] While the dimensions of some features within these devices are in the nanometer range, frequently the overall device dimension is orders of magnitude larger, particularly in structures employing semiconductor channels and source/drain regions. This size discrepancy is due to the need for ohmic contact structures which are 1 μm or greater in lateral extent and typically 100 nm or greater in depth. For example, in compound semiconductor devices based on GaAs, contacts such as alloyed Au/Ge/Ni on *n*-type layers are spatially nonuniform and also consume a significant surface layer in order to provide suitably low specific contact resistivity.[5] Thus, even though the active area of the device is in the nanometer scale, the contacts to the device still require areas $\sim 10^2-10^4$ greater than the active device. For devices with vertical current flow, such as resonant tunneling diodes (RTDs), the use of alloyed contacts often dictates that the active area of the device is buried deep beneath the semiconductor surface. In contrast, an ohmic contact technology which can provide nanometer contact dimensions, both laterally and vertically, would allow the demonstration of the high circuit densities promised by nanometer scale device concepts. Contacts suitable for high density nanoelectronic devices must provide low contact resistance and must be spatially uniform at the nanometer length scale. This article describes a nonalloyed ohmic contact structure suitable for *n*-type GaAs and discusses developments aimed at nanoelectronic device and circuit applications.

II. OHMIC CONTACT STRUCTURE

The ohmic contact structure[6] employs a surface layer of low-temperature grown GaAs (LTG:GaAs), i.e., GaAs grown at a temperature of 250–300 °C by molecular beam epitaxy. Because of the low growth temperature, ~1–2% *excess* arsenic is incorporated during growth. This excess arsenic is responsible for several interesting electronic properties, including a short minority carrier lifetime and bulk Fermi level pinning (in as-grown material).[7] For as-grown material, which is used exclusively in the work reported in

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this article, the excess arsenic is distributed in high concentration ($\sim 1.0\times 10^{20}\,\mathrm{cm}^{-3}$) of point defects, primarily as arsenic antisite defects.[7] These defects are observed as a band of states located approximately midgap in the GaAs.[8] Previous studies indicate that these states prevent the GaAs surface from rapidly oxidizing due to the relatively low concentration of minority carrier holes in the surface layer.[9,10] As a result, the presence of the gap states can be observed using scanning tunneling microscopy (STM) even following brief air exposure of the samples.[9]

The *ex situ*, nonalloyed ohmic contacts employing a LTG:GaAs surface layer can provide specific contact resistivity (ρ_c) below $1\times 10^{-6}\,\Omega\,\mathrm{cm}^2$.[6] Applications of this contact to shallow device layers and studies of the temperature stability have been reported.[11] These contacts may be appropriate for nanometer scale device applications since they would not suffer from the deep interface and spatial nonuniformity of Au/Ge/Ni contacts. In addition, this type of contact structure and the chemically stable LTG:GaAs surface layer are compatible with chemical self-assembly techniques, which can provide ordered organic monolayer films, one and two-dimensional arrays of nanoscale features, and other interesting structures.[12]

We have previously shown that high performance nano-contacts can be formed to GaAs device layers using this nonalloyed ohmic contact approach.[13] In that study, a controlled area nano-contact was formed by a single-crystal, 4-nm-diam Au nanocluster deposited on the surface. The semiconductor layer structure employs a thin (10 nm) layer of LTG:GaAs to facilitate a high quality, nano-contact to $n+$GaAs(100) layers grown at standard temperatures. Controlled mechanical tethering and electronic coupling between the Au cluster and the LTG:GaAs surface was achieved via a self-assembled monolayer (SAM) of *p*-xylene-α, α'-dithiol ($C_8H_{10}S_2$), also denoted as xylyl dithiol (XYL), which was formed on the (LTG:GaAs) surface before Au cluster deposition. Probing of the resulting nano-contact structure using STM current–voltage spectroscopy indicates that the specific contact resistance, $1\times 10^{-6}\,\Omega\,\mathrm{cm}^2$, and maximum current density, $1\times 10^{6}\,\mathrm{A/cm}^2$, of the nano-contact are both comparable to that achieved in high quality large-area ohmic contacts to *n*-type GaAs.[13]

III. PATTERNING TECHNIQUES

The current work involves definition of device structures in the GaAs material using XYL based etch masks and the development of shallow device technologies which can be compatible with such patterning techniques. For the monolayer based etch masks, a SAM of XYL is deposited in selected regions on the GaAs surface using an elastomeric stamp pad technique, as illustrated in Fig. 1. A stamp pad of poly(dimethylsiloxane) (PDMS) elastomer was made using a mold consisting of an oxidized silicon wafer in which the desired pattern had been defined by photolithography and transferred into the silicon dioxide using wet chemical etching. The GaAs samples were exposed to air for several days before preparation for stamped deposition. Following a HCl based oxide strip, the samples were transferred into a dry nitrogen atmosphere for the stamping. The elastomer stamp pad was ''inked'' by soaking it in a 1 mM solution of XYL in ethanol for 5 min. After the excess solvent had evaporated, the stamp pad was placed on the GaAs surface for a period of 18 h. Afterwards, the GaAs sample was thoroughly rinsed in ethanol to remove excess XYL.

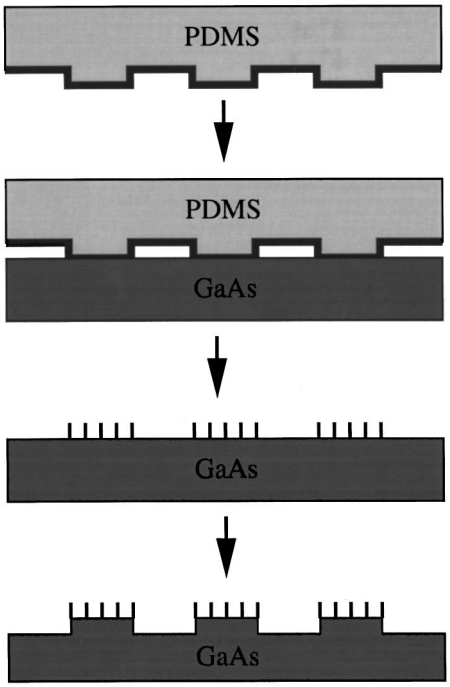

FIG. 1. Schematic diagram of the procedure used to deposit a monolayer of xylyl dithiol in specified regions on the LTG:GaAs surface. The procedure uses an elastomer stamp pad which has been lithographically patterned to provide the desired xylyl dithiol pattern. Illustrated steps are: (i) stamp pad is inked with xylyl dithiol, (ii) inked stamp pad placed on GaAs surface for 18 h, (iii) stamp pad is removed and sample is rinsed in ethanol to leave a patterned monolayer, and (iv) GaAs is etched using wet chemical etching.

Optical methods with a high surface sensitivity, such as ellipsometry, have been widely applied in surface science studies. However, it has not been until recently that ellipsomicroscopy for surface imaging (EMSI) has been developed and its submonolayer sensitivity has been exploited to obtain information about spatio-temporal pattern formation in heterogeneously catalyzed reactions.[14] EMSI is also well suited to study other ultrathin adsorbate layers and has the advantage that it can characterize the uniformity and stability of a thin (monolayer) coating as a function of position and time. With suitable optics, the EMSI technique has a spatial resolution of $\sim 3\ \mu$m. For these reasons, EMSI was used to investigate the surface of representative samples of both the LTG:GaAs-capped and the xylyl dithiol coated LTG:GaAs wafers. Figure 2 shows an EMSI image of the patterned regions of XYL on LTG:GaAs. This image was obtained after the third step illustrated in Fig. 1, i.e., before etching of the GaAs layers. The contrast is therefore due to the presence of a SAM of XYL on the surface, with a thickness of approximately 1 nm. The stable optical properties observed in this study and in experiments on unpatterned layers of XYL on

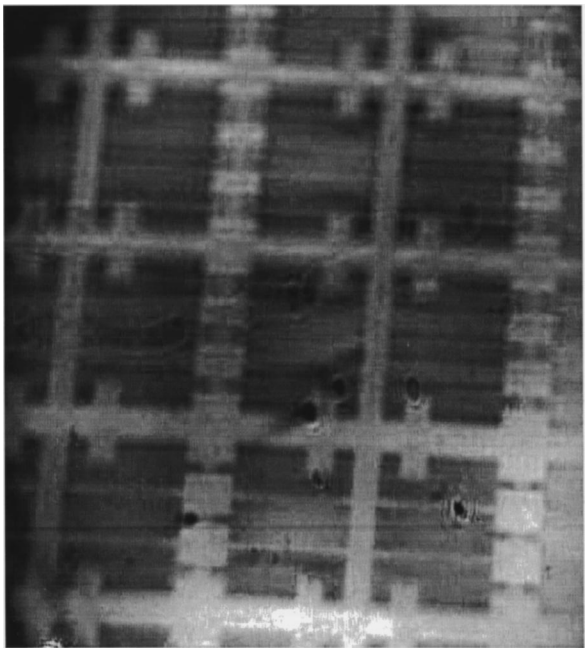

FIG. 2. Ellipsometric image of patterned regions of xylyl dithiol on LTG: GaAs, before GaAs etching. Light regions are coated with xylyl dithiol.

LTG:GaAs indicate that the XYL coated LTG:GaAs is a stable surface even under air exposure. It is believed that the sulphur to GaAs bond provides passivation comparable to that observed in studies involving elemental sulphur, with additional stability provided by both the characteristics of the LTG:GaAs and the organic tail of the XYL molecule.

The patterned monolayer of XYL was used as an etch mask for wet chemical etching of the GaAs layers. Figure 3 shows a scanning electron micrograph of a pattern etched into the LTG:GaAs capped device structure using a HCl: H_2O_2:H_2O based wet etch. In the semiconductor layer structure, a thin (5–10 nm) LTG:GaAs layer provides effective surface passivation. This layer prevents oxidation of underlying doped layers, as well as providing bulk Fermi level pinning. Because of the pinning effect, it is possible to

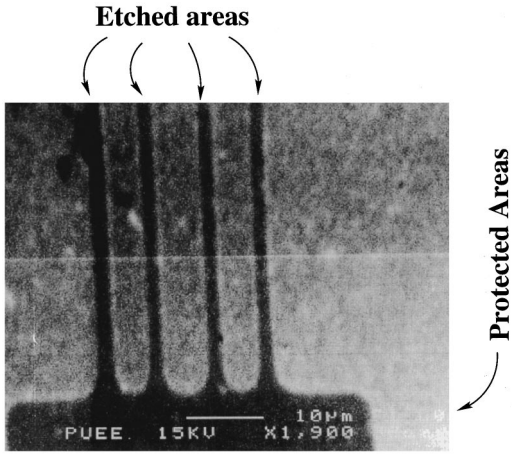

FIG. 3. Scanning electron micrograph of regions of GaAs patterned using wet chemical etching with stamped xylyl dithiol as etch mask.

achieve very high activated donor density ($\sim 1\times 10^{20}/\mathrm{cm}^3$) in the space charge regions immediately beneath the LTG: GaAs cap.[6] These characteristics enable the low-resistance nonalloyed ohmic contact, even for LTG:GaAs cap layers as thin as 2 nm. The removal of the LTG:GaAs cap is sufficient to destroy this passivation behavior and is therefore sufficient to pattern devices which use relatively thin doped (10–20 nm) layers beneath the cap. We have shown that GaAs based field-effect transistor layers can be effectively patterned by removal of approximately 3 nm of LTG:GaAs.

IV. SHALLOW DEVICES/ETCHING

To explore the possibility of making controlled heterostructures extremely close to the surface we have applied thin LTG:GaAs cap layers on thin $n++$ layers. For example, it has been possible to grow a 100-Å-thick Si-doped GaAs layer doped at $\sim 10^{20}/\mathrm{cm}^{-3}$ on an *i*-GaAs (unintentionally doped) buffer layer and capped by a 35 Å LTG: GaAs layer. To illustrate the effective surface passivation and the ability to isolate regions using a shallow etch, we have built transmission line method (TLM) structures[15] on this layer structure. The sheet resistance of this 135 Å contact structure measured from TLM patterns with *ex situ* Ti/Au contacts fabricated using conventional UV lithography was $R_{\mathrm{sh}}\approx 633\,\Omega/\mathrm{square}$ with a contact resistance $\rho_c\approx 7\times 10^{-7}\,\Omega\,\mathrm{cm}^2$. The variation across the sample was less than 15%. The measured sheet resistance and contact resistance indicate that the ohmic contacts to the layer are low resistance and that the thin LTG:GaAs cap layer had provided effective passivation of the heavily doped GaAs layer even in those regions not covered by metal. The measured sheet resistance is consistent with that predicted for a 10-nm-thick layer with activated donor density well above the bulk limit of $\approx 5\times 10^{18}\,\mathrm{cm}^{-3}$ Given that the $n++$ layer is only 3.5 nm from the semiconductor surface, an unpassivated layer of this thickness would be expected to be largely (or completely) depleted by the surface Fermi level pinning, coupled with effects of surface oxidation. In that case, the low donor activation found in bulk GaAs doped with Si (as described earlier) would be expected in the remainder (un-oxidized portion) of the layer.

The next step is to demonstrate that controlled stripping of this LTG:GaAs cap layer causes the oxidation and/or repinning of the Fermi level of the underlying $n++$ layer wherever the LTG:GaAs cap has been removed, thus causing the electrical isolation of the various $n++$ islands whose surface is protected by the contact metal. It has to be noted that while the oxidation rate of the LTG:GaAs layer is very small compared to that for conventional *n*-GaAs, a thin protective oxide layer ($t_{\mathrm{ox}}\approx 30\,\text{Å}$) will form on the surface on exposure to the ambient. This oxidation process can be accelerated either by increased minority carrier generation in the LTG:GaAs induced by incident photons or by the use of a strong oxidizing ambient. Upon stripping of this thin oxide layer, the fresh surface begins oxidizing. Repeated formation followed by stripping of the thin oxide layer allows one to etch controllably thin layers of LTG:GaAs. Once the LTG:

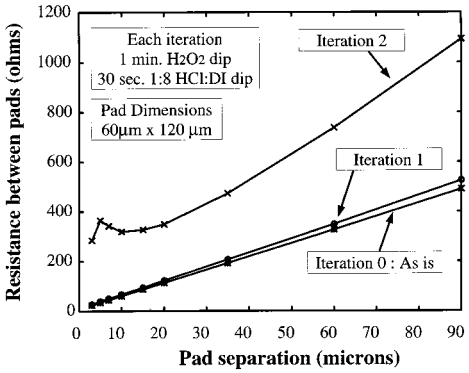

FIG. 4. Measured resistance vs pad separation for TLM structure with 60 μm$\times$120 μm pads on device layer. Curves are shown for (i) unetched sample (as deposited), after one etch iteration of approximately 2.5 nm, and after two etch iterations, with a total etch depth of approximately 5 nm. The change in resistance indicates a dramatic change in the sheet resistance between the contacts.

GaAs cap has been etched, the dynamics of the surface Fermi level pinning causes the formation of a relatively thick oxide and a large depletion region at the surface. Due to this behavior, controlled chemical etching using oxidation followed by stripping of the oxide thus formed leads to etching of only the LTG:GaAs cap and can be used to isolate $n++$ islands as shown in Fig. 4. In this case, the sample surface was oxidized by exposing it to a hydrogen peroxide solution in steps of 60 s. Each oxidation iteration was followed by a stripping of the oxide using a 30 s dip in a dilute HCL:DI solution (1:8). The resistance between the TLM contact pads was measured after each such oxidation and strip ''iteration.'' This oxidation and stripping iteration etches about 30 Å material at each instance. After three such iterations the contacts were completely isolated. The data plotted in Fig. 4 show the measured resistance between adjacent pads versus pad separation for both the ''as-deposited'' case and following one and two iterations of etching. The increase in resistance following controlled etching of the LTG:GaAs cap layer is associated with a decrease in the conductance of the $n++$ layer between two contacts. The measured resistance versus pad spacing relationship changes little after the first iteration, indicating that the passivation effect of the LTG:GaAs layer is still active. After the second iteration, the measured resistance increases dramatically, indicating that the contacts have been effectively isolated. This is as expected, since the entire LTG:GaAs layer has been removed at this point, so the passivation effect is gone. Since the y intercept, as well as the slope of the curve, changes dramatically it appears that the conductive layer between electrodes has been effectively pinched off. Although the proximity of metal electrodes likely plays a role in the exact nature of the resistance versus spacing relationship after etching, the general trend should be observed even if metal electrodes were not present. The results of this study lead us to conclude that the passivation characteristics of thin layers of LTG:GaAs make this structure well suited for shallow-etched nanoelectronic stuctures. This feature will likely be essential for the realization of high density circuits, since relatively gentle (and low-damage) etching techniques can be used to pattern and isolate devices.

The ability to isolate islands of $n++$ regions by stripping the LTG:GaAs is a novel way to fabricate both conventional devices and nanoelectronic devices. For example, we have been able to fabricate a metal semiconductor field effect transistor (MESFET) by combining the ability to make low resistance ohmic contacts using LTG:GaAs capped $n++$ layer and the modification of the conduction into the substrate upon stripping the LTG:GaAs cap. The MESFET structure has an active region comprised of a 1500 Å n-doped layer ($\approx 2\times 10^{17}\,\mathrm{cm}^{-3}$) separated from the nonalloyed ohmic contact structure ($\approx 10^{20}\,\mathrm{cm}^{-3}$ capped by a 35-Å-thick LTG:GaAs) by a 50 Å n-doped ($\approx 1\times 10^{16}\,\mathrm{cm}^{-3}$) layer. Ti/Au contacts using conventional UV lithography were used to define the source and drain contacts. Before the gate deposition the surface was treated with 3–5 iterations of the oxidation/strip iteration used in the study shown in Fig. 4. This would etch almost all of the top contact layer structure and the metal would be deposited on the lightly doped n-GaAs layer to form a Schottky contact. The resulting low-leakage MESFET indicates that we have been able to achieve good FET performance using a single structure to provide the source/drain contacts and the low-resistance channel access region. The chemical stability and surface electronic characteristics of the LTG:GaAs layer play essential roles in providing an effective capping layer. Thus we are able to exploit the passivation/surface pinning characteristics of the LTG:GaAs layer on thin $n++$ layers and modify the type of contact (i.e., either a ohmic or Schottky contact) to the underlying heterostructure to form ohmic contacts and gate regions, respectively.

For nanoelectronic device applications, these shallow etching techniques are especially interesting since they are compatible with self-assembly techniques, including the SAM based patterning described earlier in this article. SAM based resists can potentially provide nanometer scale patterns, but typically do not allow deep etching due to their limited resistance to wet chemical and dry etching techniques. However, it should be feasible to remove 10–20 nm of material using these materials as resists. In addition, self-assembly techniques can provide structures such as uniform islands and arrays of dots or lines, all at the nanoscale. The demonstration of suitable device and contact structures therefore opens up the possibility of realizing nanoelectronic circuits using relatively high throughput fabrication techniques.

V. CONCLUSIONS

In conclusion, we have described a nonalloyed contact structure which may be suitable for high density nanoelectronic device applications and discussed several experiments aimed at developing nanoscale device structures. A self-assembled monolayer of an organic tether molecule has been deposited selectively in regions defined by an elastomer stamp pad. The patterned SAM has been imaged using an ellipsometric imaging technique and has been used as an

effective mask for the wet chemical etching of the GaAs device layers. In addition, it has been shown that the thin layer of LTG:GaAs provides effective surface passivation for a FET-like device structure and that such devices can be patterned by shallow etching (~5 nm) of the layers. These demonstrations provide device approaches and fabrication techniques which can be integrated to develop a high density nanoelectronic device technology with high throughput fabrication processes.

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