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SELF-ALIGNED SINGLE CRYSTAL CONTACTED HIGH-SPEED SILICON BIPOLAR TRANSISTOR UTILIZING SELECTIVE (SEG) AND CONFINED SELECTIVE EPITAXIAL GROWTH (CLSEG)

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ABSTRACT

A new high-speed bipolar transistor structure, the ELOBJT-3, is proposed as a novel application of selective epitaxy technology. The new structure is greatly suited to high-speed ECL circuits, where C_{cb}, C_{π} and R_{bx} are of prime importance. The reduction of these parasitics to their nearly theoretical minimums is accomplished through the use of dielectric isolation and concentric contacting. For extremely high speed operation, dimensions can be scaled to sub-micron size due to the completely self-aligned emitter-base region.

Simulation was used to compare important device parameters of the ELOBJT-3 device and a comparably sized existing high speed bipolar structure. Results showed significant improvement in all three of the investigated parameters. R_{bx}, C_{cb}, and C_{π} had reductions of 77, 58, and 43 percent respectively. These simulated values were used in a circuit simulation where ELOBJT-3 devices provided a 37% reduction of propagation delay. The device simulations verified the ELOBJT-3's significantly reduced parasitics and propensity for high speed operation.

The ELOBJT-3 self-aligned pedestal structure was obtained following considerable process development. It was found that CLSEG could be grown within an oxide cavity without the use of nitride. If nitride was used, a passivation technique was developed which virtually eliminated nucleation and clogging at the via holes. **A** PNP configured ELOBJT-3 device with N+ doped CLSEG base contacts was built to establish feasibility of the self-aligned structure. Also, fully functional NPN devices were built in a simplified structure with current gains up to 90. Dislocations and defects at the SEG edge produced unacceptable emitter-collector leakage currents unless the emitter **was** moved away from the SEG edge. The

reported problems with junctions located at SEG sidewalls were avoided by moving the junction out of the sidewall area. Finally, parasitic measurements were correlated with computer simulation to validate the previous comparison simulations.

CHAPTER 1 - INTRODUCTION

After more than three decades of use, silicon bipolar devices have established themselves as a mature integrated circuit (IC) technology. Having only been invented in 1947, the basic materials and device operation were investigated in the 1950's. The 1960's found many applications of bipolar devices which eventually gave birth to the IC, where silicon bipolar transistors were successfully integrated on a single substrate. IC's got down to work in the 1970's as silicon bipolar technology became the workhorse of the semiconductor industry. But as times surely change, the 1980's saw bipolar move over to make room for the highly successful complementary metal oxide semiconductor (CMOS) devices. However, as the limits of speed and power are continually expanded, silicon bipolar technology has again stepped back into the spotlight as the only commercially viable high performance technology available today for ultimate speed. In the 1990's we'll continue to see many refinements and high performance improvements added to existing silicon bipolar devices as they attempt to maintain their position versus other advanced technologies.

One of the primary reasons for bipolar's resurgence has been the market's recent push for faster and more versatile circuits which therefore translates to the device level. As a result, silicon bipolar technology can now be found in digital, analog, mixed analog/digital, and high power circuits. The combination of CMOS and bipolar into BiCMOS should push many new circuit applications to the forefront.

1.1 The Digital Bipolar Market

Three commercially viable digital bipolar circuits are Transistor Transistor Logic (TTL), Emitter Coupled Logic (ECL), and Integrated Injection Logic (I^2L). Daring the 1970's, reasonable speed and reliable medium current operation made

TTL the industry standard for MSI and LSI designs. Today, due to the advent of CMOS and advances in other logic families, TTL's medium speed and relatively large power usage have forced it out of everything but the replacement parts and hobby markets. Though I^2L is not frequently heard of today, it still holds its own niche in the digital bipolar market. I^2L is used where digital/analog functions are required on one chip (TV applications) and power and speed are traded off for the lowest possible power-delay product. But unless new unseen developments occur, the surrounding technologies will eventually consume the I^2L market. Although ECL has possibly the highest power usage of all logic types, it is still the high-speed technology of choice because of ECL's fast switching speed, low logic levels, and high current drive capability. Not traditionally being highly integrated, there have been reports of commercially available ECL logic chips with over 100,000 transistors.[1] Although not immediately in danger, ECL is beginning to be challenged by inherently faster but less mature technologies such as GaAs MESFET's and Silicon alloyed HBT's.

1.2 The Analog Bipolar Market

As the marketplace has tried to accommodate the increased need for real world interaction, a renewed interest has developed in analog circuiits. Bipolar is clearly head and shoulders above MOS technology for use in analog circuits again because of its speed, high gain, and high current driving capabilities. Newer applications for analog bipolar are: high switching-speed power supply controllers, and single chip high-speed I/O ports for MOS microprocessors, disk drives, and micro-stepping motors. As speeds have been continually increased, bipolar operational amplifiers are now available for use as video and pulse amplifiers, DAC and ADC buffers and line drivers. An extremely interesting development was the use of complementary bipolar processes in operational amplifiers which yielded bandwidths greater than 400 MHz, but with a power consumption of less than 100 mW. The last promising area of analog bipolar is smart power technology where very high current/voltage drive devices and control logic are located on one chip to decrease total package cost. These novel applications have provided renewed growth and vigor in the analog bipolar market.

1.3 The BiCMOS Market

Despite the success of digital bipolar and renewed growth in analog bipolar, BiCMOS promises to be the boom technology of the 90's. BiCMOS technology borrows the low power consumption/high packing density advantage of CMOS and the fast switching-speed/high current drive of bipolar to form a technology which walks the middle ground between speed and power. Recently, BiCMOS has been used to fabricate extremely fast access time (less than 3 ns) SRAM's and high frequency microprocessors (70 MHz) using similar design rules as existing CMOS processes. Figure 1.1 shows BiCMOS's place between ECL and CMOS in the digital logic field.

1.4 A New Bipolar Market

As the marketplace continues to demand more capability and flexibility in integrated circuits, advances will continue to be made to silicon bipolar devices.[3] Although other materials (GaAs, silicon-germanium alloys) seem to possess better inherent characteristics than silicon, they are for the most part unproven, immature technologies. There are those that still believe that silicon has many more miles left, as well as some who believe that silicon's ease of manufacture and solid reliability will never be overcome. At the least, you can be sure that bipolar integrated circuits made in silicon material will be around for years to come.

1.5 Scope

This document details the development of a novel advanced silicon NPN bipolar transistor which will have applications to all three bipolar markets. Chapter 2 of this document will review the literature to detail the present state-of-the-art in bipolar circuits, devices, and materials technologies relevant to this new device. Chapter 3 will then present the new ELOBJT-3 device, and compare the device to existing high-speed devices using computer simulations. Chapter 4 will detail the process development of the ELOBJT-3 device, including the various experimental projects leading up to the fabrication of the ELOBJT-3 device. Measurement and analysis of parasitic device parameters and fully functioning

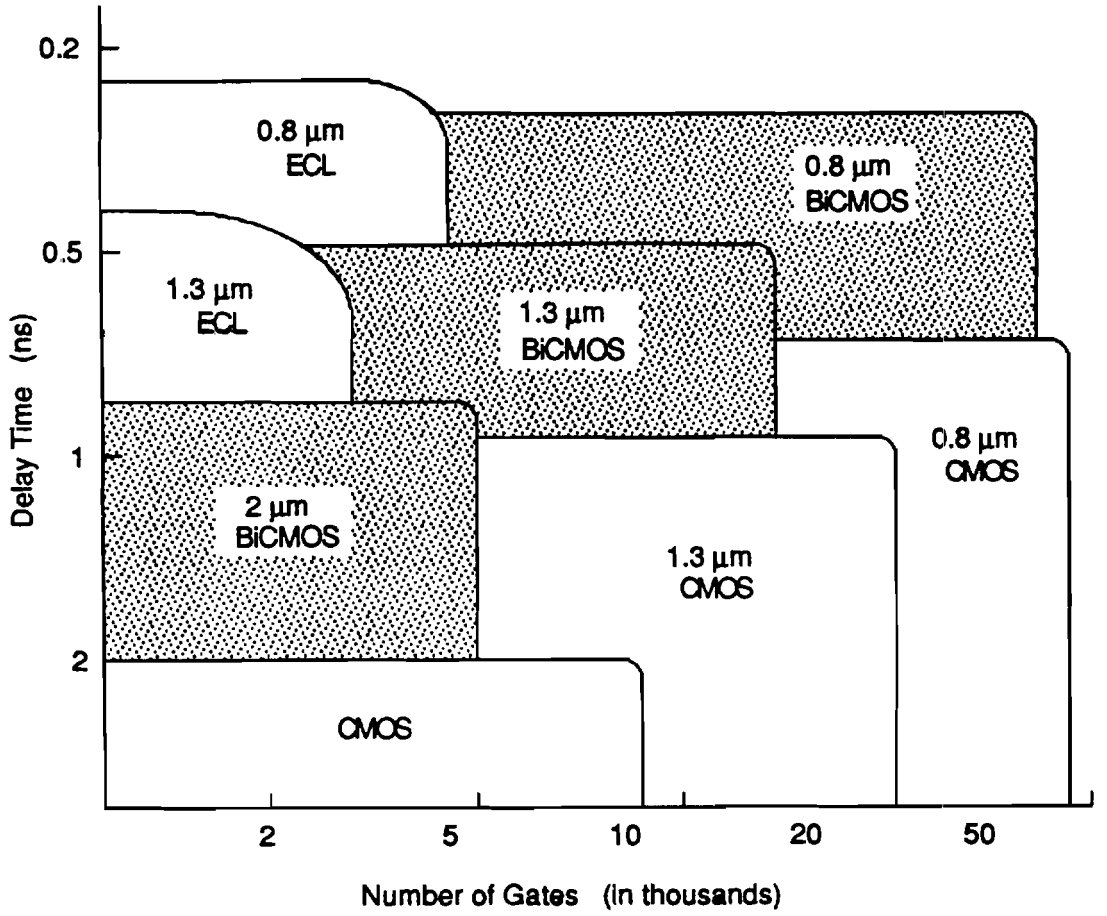

Figure 1.1. **Conceptual graph showing the placement of various digital circuit types within the delay time vs number of gates field.**[2]

ELOBJT-3 devices is presented in chapter 5. Finally chapter 6 will summarize the work performed and make recommendations for future work in the area.

1.6 References

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2. Brian Santo, "BiCMOS Circuitry: the Best of Both Worlds," IEEE Spectrum, vol. 26, pp. 50-53, IEEE, May, 1989.

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CHAPTER 2 - BACKGROUND

Although open-ended. investigation is typical of the pure science areas, engineering research by definition tends to be more defined and goal-oriented. Therefore it is important in any engineering research project undertaken to have a clear picture of where the state-of-the-art now stands and what direction advances should take. Of paramount importance to the engineer is making sure that there is a need or desirable application of the research to be performed. This chapter therefore looks at three background issues: the present state-of-the-art in bipolar devices, the device needs of the various circuit types available, and the new materials technologies which make the proposed research possible.

2.1 Device Technology

The large advancement made in bipolar devices during the last decade has greatly contributed to the resurgence of bipolar devices in the IC marketplace and enabled bipolar to maintain a definite speed advantage over CMOS circuits. Several excellent review papers have been written on the subject of high-speed bipolar devices.[1-3] Here we investigate three state-of-the-art bipolar device technologies. The Super Self-Aligned Transistor (SST) device has become widely accepted in various forms in industry, while silicon/germanium HBT's are trying to establish their significant promise despite initial skepticism. Work on a novel polysilicon pedestal type structure is presented due to its similarity to the ELOBJT-3 structure. Finally, figures of merit for high-speed bipolar transistors are discussed.

2.1.1 Super Self-Aligned Transistor (SST)

In 1980, Sakai and Konaka et al. reported a new bipolar structure and fabrication process[4,5] which drastically reduced device geometries and parasitics,

thereby significantly improving device speed. The Super Self-aligned Technology (SST) emerged from the 1980's as the clear leader of all other proposed device technologies because of its clear advantages in reducing device dimensions, overall simplicity, and use of standard process techniques. Figure 2.1 shows one of the many versions of the SST design.[6]

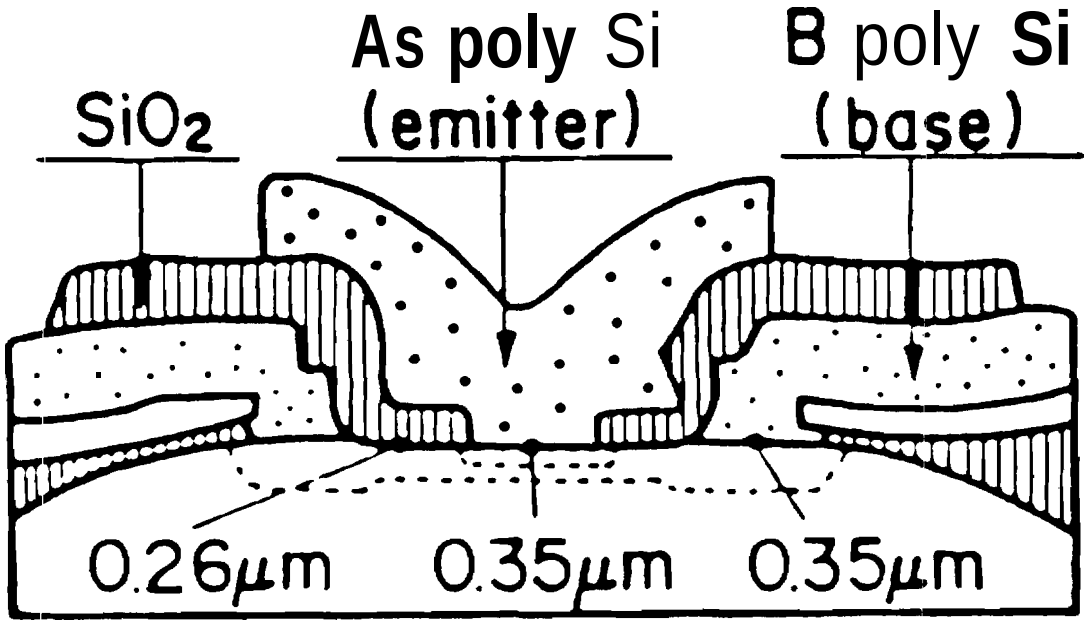


Figure 2.1. Device cross-section of the SST bipolar transistor.[6]

The bipolar device shown in Figure 2.1 has an emitter area of approximately 0.35 x 5.0 μm^2 and measured device parameters as shown in Table 2.1. Through reductions in collector-base capacitance (C_{cb}), base resistance (R_b), and cut-off frequency (f_T), non-threshold logic gate propagation delays (τ_d) of 30 ps/gate were obtained.

The SST's acceptance by industry is evidenced by the many variations made by other groups based on the original design.[7-11] Although each group provided their own name for their specific device, generally the SST-type devices can be distinguished by several features. First, only one lithography step is used to define the central active region area. All other features are self-aligned to this

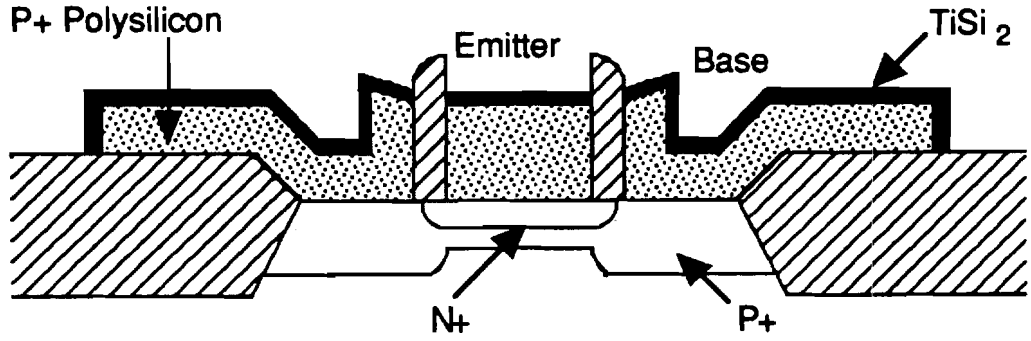
Table **2.1.** Measured Device Parameters of an SST with **0.35** x **5** μm^2 Emitter Area.

S_E	**0.35** x **5**	μm^2
τ_F	**8.4**	ps
R_b	**310**	ohm
R_e	**18.5**	ohm
R_c	**62.4**	ohm
C_{cb}	**7.4**	fF
C_{eb}	**10.4**	fF
C_{cs}	**22.9**	fF
BV_{EBO}	**5.7**	V
BV_{CEO}	**6.1**	V
h_{fe}	**180**	
f_T	**17.1**	GHz
τ_d	**30**	ps

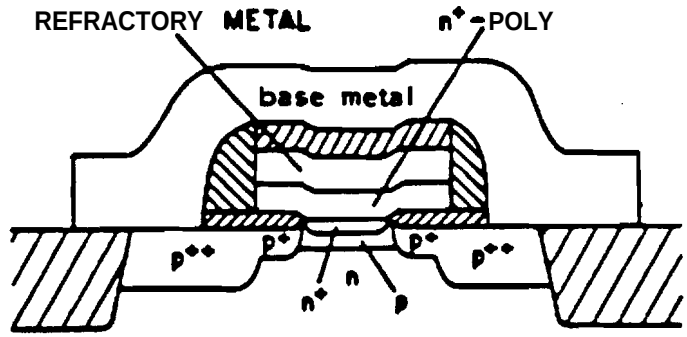
central region. The elimination of lithographic alignment by using self-alignment allows the devices to have extremely small spacings between base and emitter contacts, and thereby reduced overall device dimensions. Generally, the devices use doped polysilicon from which to diffuse the extrinsic base and intrinsic emitter regions, and to make contact to these single crystal base and emitter regions. A few representative SST-type devices are shown in cross-section in Figure **2.2.**

Despite the **SST's** success, the technology has several shortcomings. The first problem is the lower quality of the thermally grown polysilicon oxide and deposited oxide. Increased leakage current and low reverse bias breakdown voltage has been reported at the emitter-base junction interface with the spacer oxide, as well as between the base and emitter polysilicons **themselves.**[12] The second problem with the SST transistor is the difficulty of controlling the exact spacer length during processing. This causes many problems because of the spacer length's

(a)



(b)



(c)

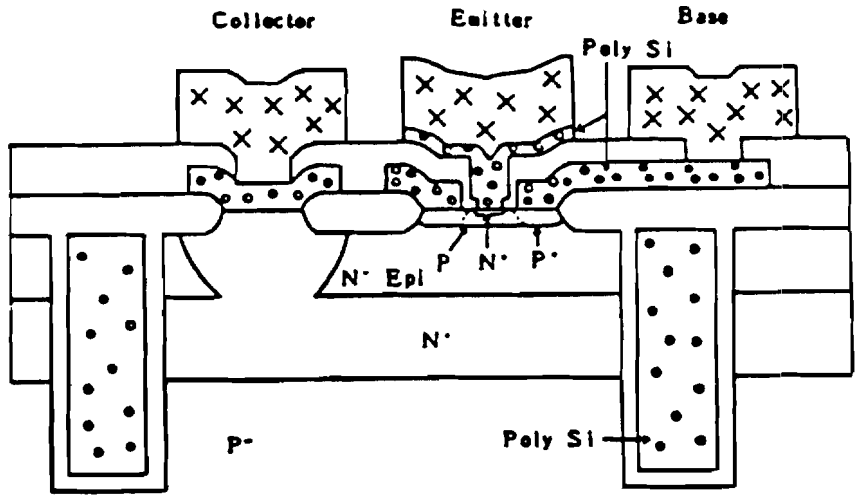


Figure 2.2. **Cross-sections of SST-based bipolar transistors: (a) AT&T's Non-Overlapping super self-Aligned structure (NOVA),[7] (b) IBM's self-aligned lateral profile transistor,[8] (c) Fujitsu's Emitter-base Self-aligned Structure with Polysilicon Electrodes and Resistors (ESPER).[11]**

effect on device performance.

The third shortcoming is related to the inherent design of the device's base region. As detailed by the SST designers, base-collector capacitance C_{cb} is the primary target for reduction in order to reach ultimate high speed operation. Regardless of the SST process achieving remarkably small geometry due to self-alignment (0.35 μm emitter lateral width), all SST-like designs fail to achieve a minimum sized base-collector junction and therefore fail to reduce the base-collector capacitance to its theoretical minimum. Therefore, although the SST is a remarkable achievement in device self-alignment and size reduction, it does not approach the theoretical limit of high-speed operation for silicon bipolar devices.

2.1.2 Heterojunction Bipolar Transistor (HBT)

As the performance of silicon bipolar devices has advanced, a conflicting requirement has been confronted. In order to further improve the device switching speed, the base-transit time needs to be reduced primarily by shortening the base thickness. This however conflicts with the need to keep the base arbitrarily thick in order to avoid unwanted base resistance and base width modulation effects. It is theorized that if the base doping is increased, base thickness can be decreased to reduce the transit time, and yet avoid increased resistance and modulation effects due to the reduced thickness. This idea's flaw is that the added base doping causes increased back-injection of holes into the emitter from the base, and thereby degrades the emitter injection efficiency, increases charge storage in the emitter, and increases emitter/base capacitance. A heterojunction can provide a bandgap discontinuity at the emitter/base junction to increase the electron injection into the base or suppress the unwanted back-injection of holes, and thereby counter the negative effects of increased base doping.

Two methods of arriving at an emitter/base heterojunction have been investigated.[13] One of the first methods to be investigated historically was the use of a wide bandgap emitter material such as Oxygen-Doped Silicon Epitaxial Films (OXSEF), β-SiC, and amorphous and microcrystalline silicon. These techniques at first appeared to be the most desirable due to their ease of incorporation into standard silicon bipolar processing routines. However, several factors such as high thermal requirements, large bulk and contact resistances, and poor stability have led to the demise of this technique.

The second technique is that of using a narrow bandgap alloyed material in the base sandwiched between homogeneous silicon material in the ennitter and collector to form a double heterojunction bipolar transistor (DHBT). In theory, the effect of the narrow-bandgap base material on an NPN device is to increase the minority carrier injection into the base from the emitter, whereas the wide-bandgap emitter acts to reduce the back-injection of holes from the base. Although both act to preserve emitter injection efficiency, they affect their changes in opposite ways.[14] Initial attempts were made at fabricating the appropriate heterojunction Si/SiGe layers using molecular beam epitaxy (MBE). Due to the inability of MBE techniques to produce low defect density, high purity, flexible doping, and high throughput processing, chemical vapor deposition (CVD) techniques have become more popular for fabrication of the lneterojunction layer:;. Kamins et al. reports transistors with common-emitter current gains of about 50, and f_T of about 28 GHz for devices with 25 nm thick, $7x10^{18}cm^{-3}$ doped base layers.[15] Unity-gain cutoff frequencies f_T can be expected in the 50-100 GHz range[16] as DHBT structures are perfected. As stated by Kamins, the primary limitation of frequency response was the large collector-base capacitance resulting from the mesa structure used in their devices.

Although HBT technology holds great promise for the future,, there remain some very important issues to be resolved. HBT's can be built in a variety of material systems, for example GaAlAs/GaAs, InAlAs/InGaAs/InP, and SiGe/Si. Of these, SiGe/Si holds the most immediate promise because of its similarity with standard silicon processing.[17] However, the SiGe/Si HBT must further improve its process integration to obtain more advanced structures which are able to showcase its advanced materials technology. Additionally, the major difficulty to be surmounted is the question of long-term material reliability of strained-layer SiGe alloys.

2.1.3 Polysilicon Pedestal Bipolar Transistors

In recognition of the need to focus on the reduction of base/collector parasitics while maintaining the active area's size for current drive, several pedestal-type bipolar designs have been demonstrated. The easiest device to fabricate is undoubtedly the Pedestal Bipolar Transistor (PBT) of Hebert and Roulston.[18] The PBT device cross-section in Figure 2.3 shows the extrinsic base region

completely oxide isolated from the collector region and concentric around the intrinsic region located beneath the emitter. The process uses standard

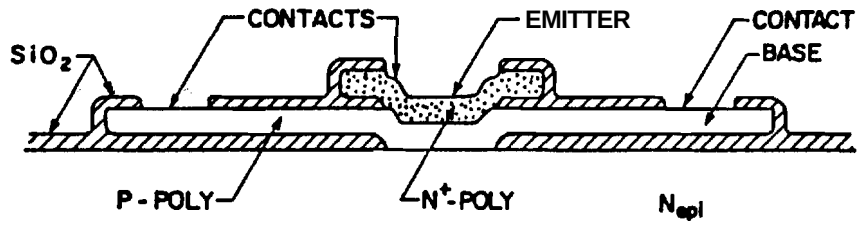


Figure 2.3. Cross-section of the Pedestal Bipolar Transistor.[18]

polysilicon processing techniques and wet etching to deposit and define the base polysilicon layer on top of the 0.5 μm field oxide. A rapid thermal anneal of 1150° C for 40 seconds in oxygen is used to recrystallize the portion of the polysilicon layer overlying the substrate. The base layer is then boron doped and oxidized, and the emitter window is lithographically defined. An in-situ doped phosphorus polysilicon emitter is then deposited for the final structure.

The PBT device has two primary drawbacks. First and foremost, it is not self-aligned and therefore cannot be scaled to sub-micron dimensions. The lack of self-alignment also means the emitter opening cannot be reliably aligned to the base/collector junction below. Secondly, locating the intrinsic device region in largely polysilicon material makes for a decidedly poor operating device as evidenced by the PBT's electrical results. DC gains in the forward direction did not exceed unity, primarily because of large base recombination currents in the polysilicon. However, reverse gains of up to 10 were measured with emitter/base (lower junction) ideality factors of 1.62. For the unique application stated in the paper, integrated injection logic circuits, the PBT devices were just barely sufficient.

Although slightly more advanced processing is required, the pedestal-type structure of Liaw and Seiter showed much more promise as a high-speed bipolar

device.[19] As seen in Figure 2.4, the central intrinsic device is composed of selective epitaxy material contacted concentrically by a heavily doped layer of polysilicon. The process starts with the deposition of a tri-layer stack of silicon dioxide,

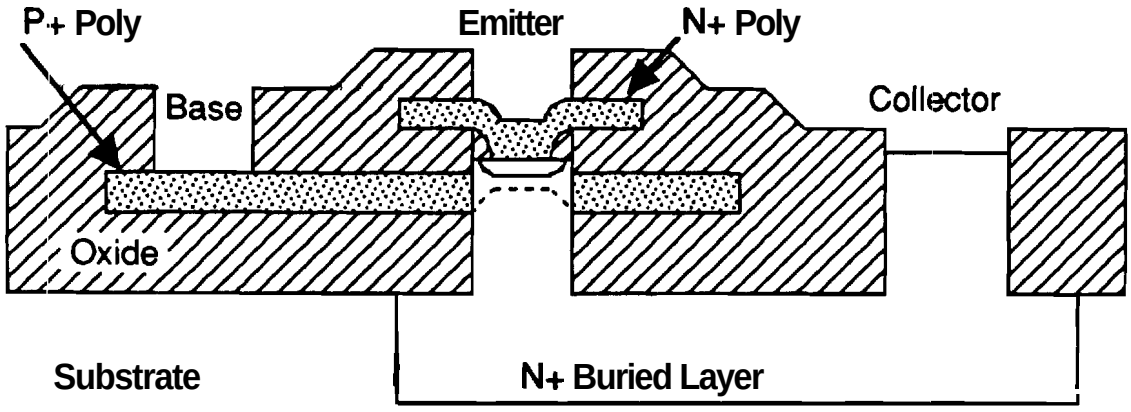


Figure 2.4. Cross-section of a pedestal-type bipolar device which utilizes selective epitaxial growth within a trench with a sidewall polysilicon base contact.[19]

heavily P+ doped polysilicon, and silicon dioxide. A special multi-layer mask is then. used to RIE etch a vertical trench through the tri-layer stack of oxide/polysilicon/oxide to the substrate. Selective epitaxial growth (SEG) is then used, to refill the trench with single-crystal silicon material contacted on its sidewalls by the P+ polysilicon layer. Standard base and emitter implants are then used to locate the intrinsic base and emitter regions in the self-aligned pedestal.

Contrary to the PBT device, this structure attempts to locate its intrinsic regions and junctions in single-crystal material, not polysilicon. However, upon growth of the SEG within the trench, it is impossible to avoid nucleation of polysilicon from the exposed P+ polysilicon at the sidewalls. As SEG growth continues, the single-crystal material advancing from the substrate merges with the polysilicon growth from the sidewall forming highly defective material at least within approximately 0.3-0.4 μm of the sidewall edge. As stated by the

researchers, these defects may be the limiting factor of the design in that they caused low emitter/base breakdowns and high emitter/base recombination currents as well as emitter/collector diffusion pipes. Although this pedestal-type structure seemed to hold great promise, the defects inherent in its fabrication process have precluded any further investigation.

2.1.4 Figure of Merit for High-Speed Transistors

A figure of merit (FOM) is a variable whose value is a numerical indicator of the quality or merit of a specific device or process. In this context, we seek an FOM which indicates a bipolar device's propensity for effecting high-speed operation within a circuit. For years, the IC industry has been advancing the state-of-the-art in bipolar devices and reporting their results in terms of two specific FOM's, the unity-gain cutoff frequency, f_T, and the maximum frequency of operation, f_{max}. Although in the past f_T and f_{max} have been decent indicators of eventual circuit speed, at today's geometries and parasitic values these figures of merit are becoming less and less accurate at indicating the high-speed potential of bipolar devices. However, because of their extensive use in the literature, they will be covered here. Newer, more accurate FOM's will be detailed in later sections because they pertain to specific circuit topologies.

The magnitude of the unity-gain cutoff frequency, f_T, is defined as the frequency at which the common emitter forward current gain, h_{fe}, is reduced to unity. The cutoff frequency can easily be related to the physical structure of the device through the equation,

$$f_T = \frac{1}{2\pi\tau_{ec}} \tag{2.1}$$

where τ_{ec} is the delay time encountered by the carriers as they flow from emitter to collector.[20] The delay time can be divided into four major delays, each representing a separate effect,

$$\tau_{ec} = \tau_e + \tau_b + \tau_c + \tau_c' = \frac{kT}{qI_E}C_e + \frac{W_B^2}{2D_B} + \frac{X_C}{2v_s} + R_cC_{cb} = \frac{1}{2\pi f_T} \tag{2.2}$$

The first term (τ_e) represents the time needed to charge the emitter depletion region and can be thought of as a simple RC time constant where $kT/qI_E = R_E$. The second term in the delay expression (τ_b) is the base layer charging time and

accounts for the minority carrier diffusion across the base with a uniform doping. The third term (τ_c) accounts for the continuation of the carrier motion as the carriers are quickly accelerated across the collector-base depletion region. It is assumed that the depletion layer electric field will be sufficient to supply saturated velocity (v,) to the carriers in this region. The last term (τ_c') expresses the final charging time, that of the collector region. The four charging time delays represent sequential events as the carriers move from emitter to collector, and together represent the total delay of carrier motion in the bipolar device.

As is evident from the many device parameters present in the delay expression, there are many ways to reduce the overall delay time and thereby increase the transistor's high frequency operation limit. However, most of the simple parameter improvements suggested by equation 2.2 have long since been made. What remains are a mixture of conflicting requirements, fundamental limits, and changes requiring significant effort or innovation. For example, the emitter current (I_E) can be increased in order to decrease emitter depletion charging time, but this drives up power consumption and eventually encounters large current density effects. Similarly, although the collector-base depletion thickness (X_C) can be reduced, a conflicting effect is to increase the collector-base capacitance (C_{cb}).

The maximum frequency of operation, f_{max}, is defined as the frequency of operation where the unilateral power gain reduces to one.[21] f_{max} can be related to the cutoff frequency through,

$$f_{max} = \sqrt{\frac{f_T}{8 \pi R_b C_{cb}}} \tag{2.3}$$

where R_b is the total base resistance. Equation 2.3, however, was derived before the advent of the integrated circuit. In the late 1950's, it was applied to discrete bipolar devices which were inserted in special optimizing networks. Normally, both the output and input to the device were neutralized with appropriate complex networks, the load was impedance matched to the output, and the circuit operated at one single optimum frequency. This is obviously not the case in either analog or digital integrated circuits today. In addition, Equation 2.3 is not generally valid, but limited to a range of R_b C_{cb} values, such that it does not hold for ;arbitrarily small R_b or C_{cb}. It therefore becomes obvious that these figures of merit, although reported extensively in the literature, are not suitable for guiding

us in the area of device design in today's technology.

2.2 Circuit Considerations

Although there exists great emphasis on making faster and faster bipolar devices, this work is derived from the market's desire for faster integrated circuit speed. Therefore, all device improvements should be judged by their ability to increase the operating speed of the circuit in which they are used. This chapter attempts to look past the specific advances made by present state-of-the-art devices (Section 2.1), in order to see what device requirements are made by today's advanced circuits. Section 2.2.1 reveals the needs of the fastest silicon-based digital circuit type, emitter coupled logic (ECL). Section 2.2.2 looks at the requirements of I^2L, the bipolar circuit type with the best speed/power combination. Finally, the area of analog bipolar circuits is considered to see what device improvements are needed.

2.2.1 Emitter Coupled Logic (ECL)

Emitter coupled logic derives its name from the way that the emitters in the central current switch are tied together or coupled to form essentially an analog differential amplifier as seen in Figure 2.5. In reality, ECL is an analog circuit used in a digital application. This differential amplifier or emitter coupled pair is a non-saturating current switch because during normal switching operation of the circuit neither transistor is allowed to enter the saturation mode of operation. The saturation mode for a bipolar transistor is defined as forward biasing both emitter-base and collector-base junctions. The undesirable feature of saturation mode is that both junctions of the transistor are heavily filled (saturated) with minority carriers. In order to turn-off, a longer period of time is needed for these carriers to leave, thus slowing down switching operation. Thus, the ECL circuit type is based on non-saturating operation.

As seen in Figure 2.5, the basic circuit is comprised of the two transistor emitter coupled pair, a generic constant current source connected to the emitter pair node, collector resistors connecting the transistors to the positive voltage supply, emitter followers for level-shifting the output, and a generic voltage reference

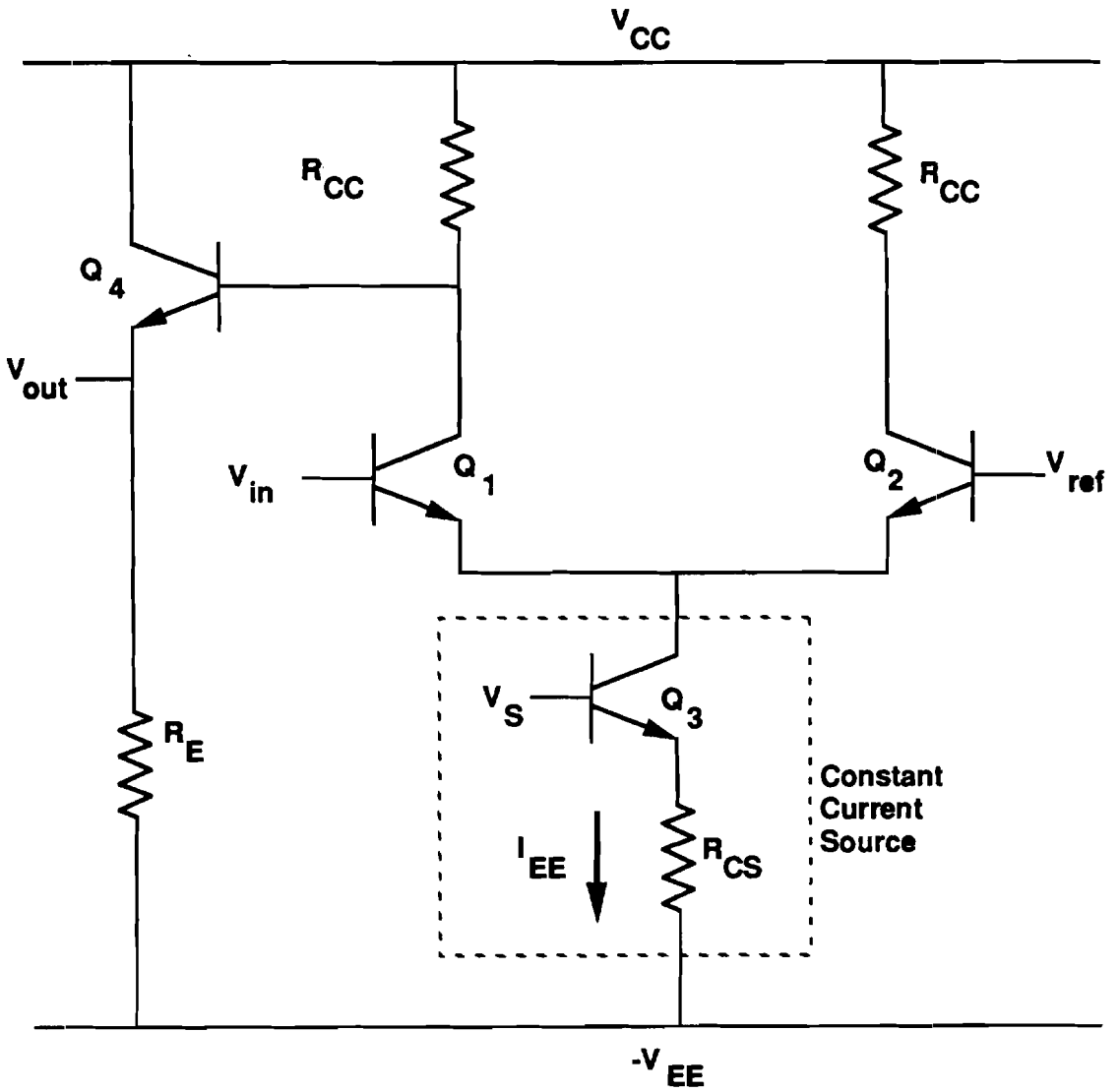


Figure 2.5. Basic ECL inverter circuit configuration. Voltage reference network is not shown.

circuit. Operation of the circuit is as follows. The current source demands a constant current from the emitter node, but does not care from which transistor (or both) it flows. A constant voltage reference V_{ref} is applied to the base lead of the reference transistor Q2. If the input signal applied to the base of transistor Q1 is more than a few tenths of a volt greater than V_{ref}, due to the differential amplification, transistor Q1 turns on and the majority of the current flows through the left side of the emitter coupled pair. Likewise, if the input voltage is less than a few tenths below V_{ref}, the majority of the current flows through the reference side and the input side turns off. As the opposite sides of the differential pair turn on/off, the collector node voltages move from V_{CC} (off) to $V_{CC} - R_{cc}I_{EE}$.

An extremely rigorous analysis by Ghannam et al. has produced general analytical expressions for the propagation delay of an ECL circuit.[22] Their model is applicable at low-level injection, unity fan-in/fan-out, and includes delays related to the transit time, load, and junction capacitances. However, these expressions are so general and complex as to be of little use in determining requirements for bipolar devices. Several less general analyses have been reported which are more easily interpreted.

Chor et al.[23] performed simulations of ECL circuits employing polysilicon emitter devices. In their analysis, Chor et al. stated the inability of an analytical expression, such as Equation (2.2), to accurately indicate a bipolar device's performance in a digital circuit. Therefore, they formulated an approximate expression for ECL delay time using a linear combination of the time constants of the circuit, where each time constant is multiplied by a unique weighting factor. For the ECL gate depicted in Figure 2.5, the delay expression is given by

$$\tau_d = \sum_i K_i R_i C_i + \sum_j K_j \tau_j \qquad (2.4)$$

where K_i and K_j are the weighting factors for the charging and delay terms, respectively. A total of 38 terms in the sum were used to approximate the delays in the ECL circuit. A sensitivity analysis was then used to determine constant values for the weighting factors over specific ranges of allowed device parameter values. After determining the form of the total expression, SPICE simulations were run as a comparison to validate Equation (2.4).

Experimentally, a set of non-optimized 6 x 6 μm^2 polysilicon emitter bipolar transistors were fabricated and tested for device parameters. These measured

parameters were then used in Equation (2.4) to investigate the size of the contribution from each of the sums as listed in Table 2.2. From Table 2.2, the relative importance of each of the terms can easily be seen with the $R_{bx}C_{cbx}$ and the $R_L C_{cbx}$ terms dominating the total time delay.

Table 2.3 shows four of the prominent device parameters and the sum of the percentage of total delay for the components in which they appear. The importance of these four device parameters in determining the overall delay time and therefore maximum operating frequency of the circuit is evident. However, the importance of a specific device parameter is not determined solely by its value, but also by its value relative to other parameters of the device, and how the device is being used in a circuit.

A further investigation of analytical ECL delay expressions was performed by Wen Fang[24] using measured device data from 0.5 μm self-aligned transistors in conjunction with SPICE simulations. Numerous sensitivity analysis simulations were run to determine the appropriate weighting factors (the K values of Equation 2.4) for his sum of time constants expression. Once determined, the weighting factors produced an analytical expression that matched the SPICE simulations to within 5% over large variances in device parameter values. The analytical expression obtained for a state-of-the-art 0.5 μm silicon device was

$$\tau_d = 1.2\tau_F + 3.2R_b\,C_{cbi} + 0.95R_b\,C_{eb} + 1.15R_b\,C_d + 1.5R_L\,C_{cb} + 0.27R_L\,C_{cs} + 0.31R_L\,C_L + 3.85R_e\,C_{cb} \quad (2.5)$$

This expression is extremely useful due to its very simple linear, yet accurate connection of measurable device parameters to actual circuit propagation speed.

Stork actually attempted to directly, analytically relate the gate delay of an ECL circuit to measurable device parameters.[25] He used a circuit topology identical to Figure 2.5, and assumed a voltage swing of V_S volts, and constant current source of I_S amps. He then proceeded to split the transistor delay characteristics into two fundamental terms, T_B the intrinsic bipolar device delay, and T_C the combination of the delay produced by the parasitics and the load. The collector and base were decoupled using the miller effect relationship,

$$C_{cbM} = (1 + |A_v|)\,C_{cb}. \quad (2.6)$$

Since the effective voltage gain $|A_v|$ of a logic gate is 1, $C_{cbM} = 2C_{cb}$. This is then added to the C_{cb} of the emitter follower and the C_{cs} of Q1, the collector

Table 2.2. Components of Propagation Delay for 6 x 6 μm^2 Polysilicon Emitter Transistor.[23]

Time Constant	Delay (ps)	% of Total Delay
τ_F	72.0	3.1
$R_{bi}C_{cbi}$	128.9	5.6
$R_{bi}C_{cbx}$	195.8	8.5
$R_{bi}C_{be}$	209.8	9.0
$R_{bi}C_{d}$	155.8	6.7
$R_{bx}C_{cbi}$	49.6	2.1
$R_{bx}C_{cbx}$	573.4	24.7
$R_{bx}C_{be}$	94.8	4.1
$R_{bx}C_{d}$	63.6	2.8
$R_{L}C_{cbi}$	30.5	1.3
$R_{L}C_{cbx}$	507.8	21.9
$R_{L}C_{be}$	52.9	2.3
$R_{L}C_{cs}$	37.6	1.6
$R_{L}C_{L}$	70.5	3.0
$R_{c}C_{cbi}$	6.36	0.3
$R_{c}C_{cbx}$	49.4	2.1
$R_{c}C_{d}$	3.27	0.1
$R_{c}C_{be}$	7.00	0.3
$R_{c}C_{cbi}$	0.39	<0.1
$R_{e}C_{cbx}$	4.28	0.2
$R_{e}C_{be}$	0.26	<0.1
$R_{e}C_{d}$	0.19	<0.1
$R_{e}C_{cs}$	0.17	<0.1
$R_{e}C_{L}$	0.33	<0.1
Total Delay	2315	100

Table 2.3. Sum of Percentage Delay Components from Table 2.3 in Which Device Parameter Appears. Derived from Chor et al.[23]

Device Parameter	% of Total Delay
C_{cbx}	57.4
R_{bx}	33.7
R_{bi}	29.7
C_{cbi}	9.3

resistance added, and the final parasitic charging term is,

$$T_C = R_c(3C_{cb} + C_{cs}) \tag{2.7}$$

The total current switch delay expression is then,

$$T_{CS} = 1.7 \times \sqrt{\tau_F(R_c + 2R_b)(3C_{cb} + C_{cs})} \tag{2.8}$$

where τ_F is the forward transit time of the device, $R_b = R_{bi} + R_{bx}$ is the total base resistance of the device, $R_c = R_{ci} + R_{cx} + R_{cc}$ is the sum of the device and circuit collector resistances, and C_{cb} and C_{cs} are the collector-base and collector-substrate capacitances respectively of the device. The relationship between f_T and τ_F is expressed as

$$\tau_F + \frac{kT}{qI_E}C_e + R_cC_{cb} = \frac{1}{2\pi f_T} \tag{2.9}$$

At the current density of maximum f_T, the second and third terms of equation 2.9 are negligible and τ_F can be approximated as

$$\tau_F = \frac{1}{2\pi f_{T(MAX)}} \tag{2.10}$$

Equation 2.8 is valid for state-of-the-art bipolar devices and ECL circuits where T_B and T_C are within a factor of 3 of each other, which is the case for most current devices. T_{cs} is an excellent figure of merit for bipolar devices to be used in ECL circuits because it shows the direct relationship of circuit speed to

measurable device parameters, namely C_{cb}, R_b, and C_{cs}.

It now seems appropriate to return to the subject of f_T as a figure of merit for high-speed bipolar devices. In the past, the use of f_T was warranted due to the intrinsic device's relatively slow speed. However, over the years as the intrinsic device doping profile has been all but perfected, the transit time τ_F of the forward carriers in the intrinsic device has become a much smaller portion of the switching time of today's state-of-the-art bipolar device. f_T will still be used in the future for reporting basic improvements in forward transit time, for example in advanced silicon/germanium heterojunction devices.

Chuang et al. [26] investigated the ability of high-f_T transistors to effect increased circuit speed in standard ECL bipolar circuits. They used SPICE circuit simulations to compare the propagation delay of ECL circuits employing two distinct bipolar models. The models were based upon identically sized devices fabricated with their silicon homo-junction process and their silicon/germanium heterojunction process. The two devices had f_T's of 48 and 70 GHz respectively.

Results of their simulations showed that the higher f_T device, 70 versus 48 GHz, produced a speed improvement of 19.4% (unloaded) and 10.1% (loaded) at a maximum power of 3.0 mW/gate. At a more reasonable power of 0.5 mW/gate, the improvement was 6.7% (unloaded) and 2.5% (loaded). As explained by the researchers, this relatively small improvement was due to the fact that "the base transit time contributes to only about 1/3 of the unloaded delay at maximum speed, and even less at low power (where device parasitics dominate)."

2.2.2 Integrated Injection Logic (I^2L)

Two teams of researchers in the early 1970's were independently responsible for inventing merged transistor logic, also known as integrated injection logic I^2L. This digital circuit type was bipolar's answer to MOS IC's in the early days of LSI. Eventually, the significant advances and levels of integration of MOS and CMOS were to overcome I^2L. However, for cettain mixed analog/digital functions, I^2L is still employed today.

Figure 2.6 shows a standard I^2L digital gate circuit and typical device cross-section using standard junction-isolated, double-diffused bipolar technology.[27] The lateral PNP transistor is called the injector and provides carriers to the base

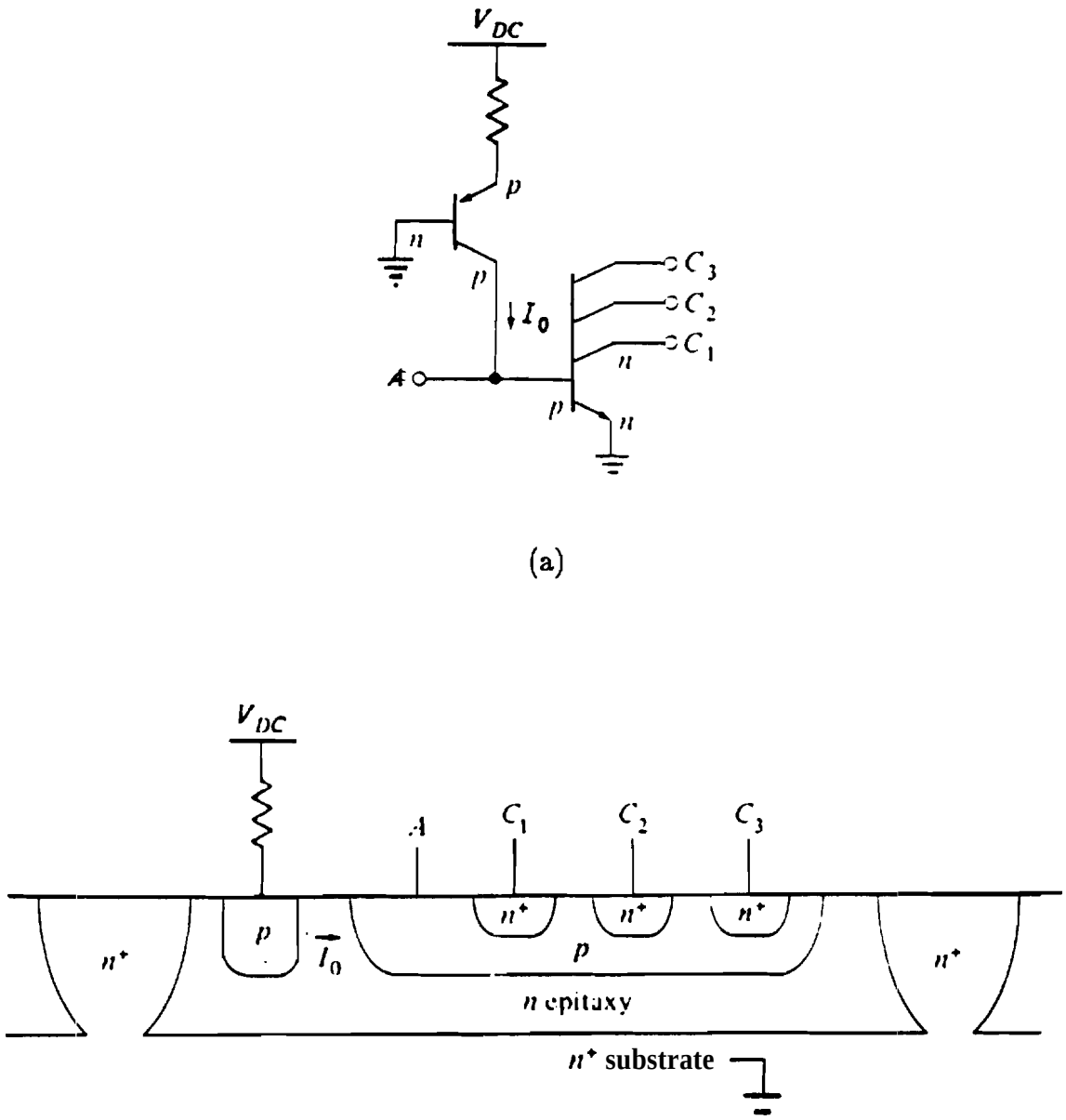


Figure 2.6. Standard I^2L digital gate: (a) circuit diagram, (b) device cross-section.[27]

region of the NPN switching transistor. When the input A is high (V_{DC}), the current I_o is into the base of the NPN, and all the NPN collectors are pulled low (near ground potential). Alternately, when the input A is low (the input is being fed by a previous gate's collector which is pulled low), the current I, goes to supply the previous gate's collector. The advantage of the I^2L circuit is that it merges n and p regions from the NPN and PNP transistors for significant space savings as seen in the device cross-section of Figure 2.6(b). Additionally, I^2L has great flexibility in logic design due to its multiple collector feature, and the ability to tie multiple buried emitters together with a single buried layer reduces the amount of chip metallization needed. It also uses virtually no gate level resistors.

The serious drawback which held I^2L back was the fabrication technology available at the time. Large alignment tolerances and lithography resolution made all areas of the devices large, especially the buried emitter regions. Because I^2L circuits use the transistor in the saturation mode when an output is pulled low, the large, lightly doped, buried emitter areas saturate with charge and take relatively long periods of time to turn off. This charge storage phenomenon acts to give I^2L circuits relatively slow switching response, e.g. in the 10 to 100 MHz range. I^2L frequency response could be significantly improved if the buried emitter region could be reduced in size to include only the intrinsic device region. Further, I^2L circuit speeds suffer because of low reverse current gains ($\beta = 5$—10) due to the non-optimized upside-down doping profiles. Circuit speeds could be improved if doping profiles were changed to provide more normal current gains for the NPN devices.

An example of an advanced bipolar structure applied to I^2L circuits is the SIdewall Contacted Structure (SICOS)[28] shown in Figure 2.7. Nakamura et al. reported fabrication of I^2L circuits employing SICOS bipolar transistors with 3 x 3 μm^2 collectors regions. The structures produced a minimum gate delay of 290 ps/gate and power delay products of 15 fJ/gate at low injector current levels for ring oscillators with fanouts of one. This power delay product is more than two orders of magnitude better than that realized by the junction-isolated structures of Figure 2.6(b). The SICOS technology did not make the transition to the commercial market because of fabrication difficulties. However, it is still an excellent example of the merit of I^2L circuits given an advanced BJT device structure.

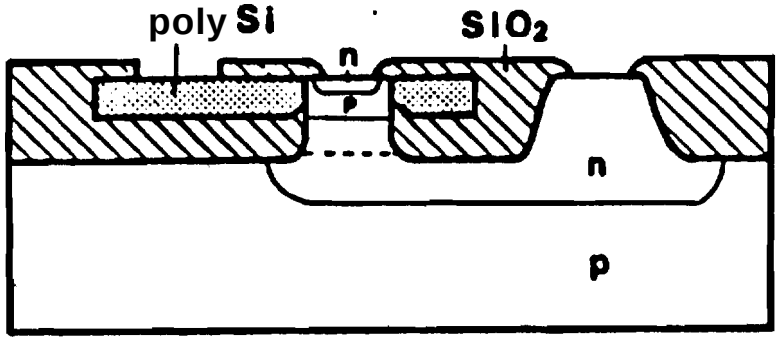


Figure 2.7. Cross-sectional device structure of SIdewall Contacted Structure (SICOS) bipolar transistor used in I^2L circuits.[28]

2.2.3 Analog-Amplifiers

The last type of circuit to be considered is analog bipolar. Although there has been a great proliferation of digital circuits due to the computer revolution, it is still a decidedly analog world. Most analog circuit types can be generalized to the multi-stage amplifier design as seen in Figure 2.8. Simmons and Taylor used the circuit of Figure 2.8 to develop a new figure of merit for bipolar devices used in general analog circuits.[21] The unity power transfer ratio frequency, ω_{PT}, is defined as the frequency where the ratio of power out of an amplifier stage divided by the power into the stage is reduced to one. This frequency is of primary importance because it is the maximum frequency where a srnall signal can be propagated through a multi-stage circuit without reduction of overall power.

Initially, the analysis was completely general and yielded some extremely large expressions for ω_{PT}. The authors then chose to use certain simplifying assumptions in order to pare down the equations to more simple expressions for interpretation. Unfortunately, the assumptions used were: C_L is much larger than all other capacitances, R_e is negligible, C_{be} is much less than C_{cb}, and C_{cs} is ignored. These assumptions are not generally valid for the current or future state-of-the-art bipolar devices and circuits.

However, their results did reveal some interesting facts regarding analog bipolar circuits. First, the number of occurrences of the parameters C_{cb}, R_{bx}, and

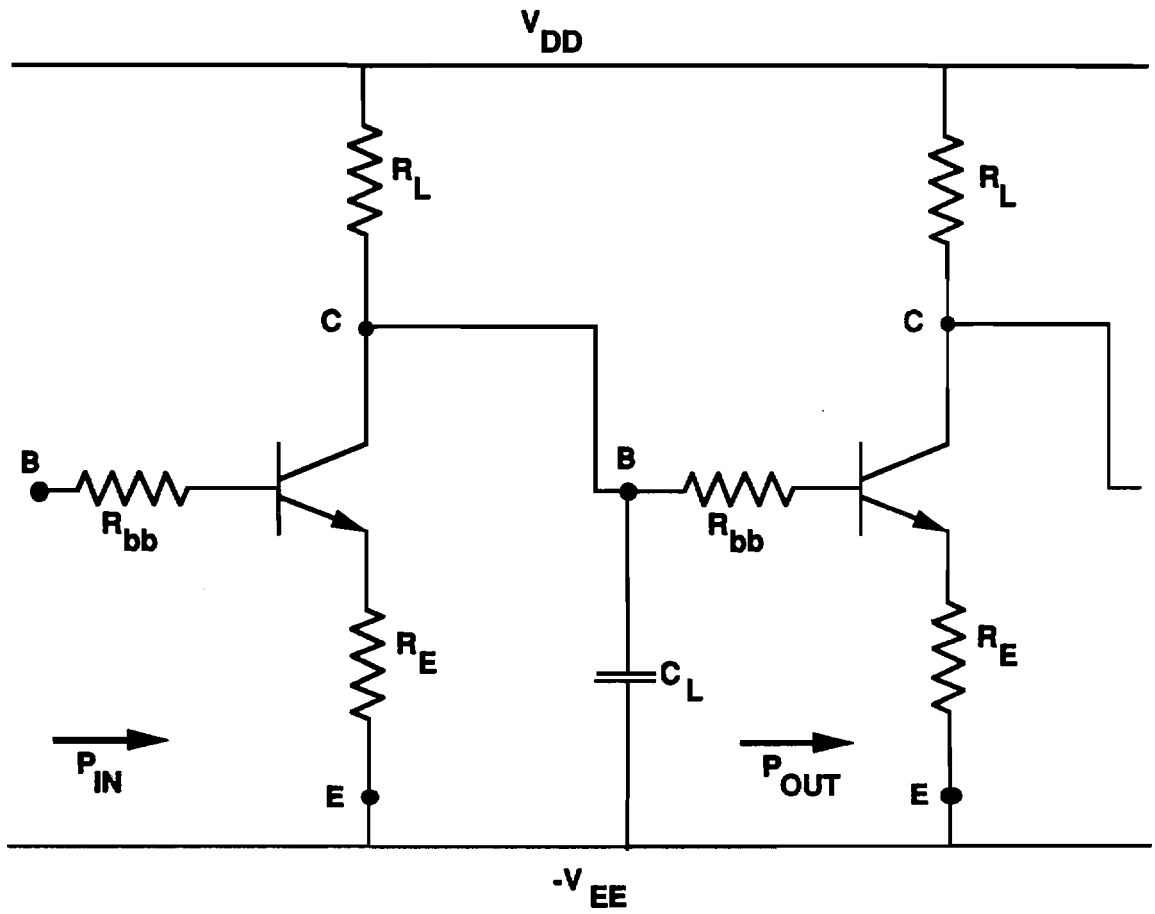


Figure 2.8. **Generalized multi-stage common-emitter amplifier model used for determining a new figure of merit for a bipolar device in an analog circuit.[21]**

C_{cs} in their general ω_{pT} expression was enough to suggest these parameters' importance in determining the bipolar device's high-frequency response. Second, at large DC operating currents, a reduction of R_{bx} to the tens of ohms range has a significant effect on the unity power transfer ratio frequency ω_{pT}. Finally, under no circumstances will the unity power transfer ratio frequency ω_{pT} exceed the unity gain cutoff frequency ω_T.

2.3 Materials Technology

Recent advances in silicon materials processing have opened. the door to many new devices and structures. This section briefly reviews work: reported primarily in the 1980's of selective, lateral, and confined lateral epitaxial growth. Although there is a relative abundance of growth characterization in the literature, reports of electrical characterization of the new materials is not abundant. Emphasis will be placed on electrical characterization because of its importance to building devices in the material.

2.3.1 Silicon Selective Epitaxial Growth (SEG)

Selective epitaxial growth (SEG) of silicon, first reported in the 1960's,[29] was a natural extension of the full wafer epitaxial technology being developed at that time.. As seen in Figure 2.9(a), the SEG process starts with the patterning of a seed hole in the masking oxide to expose the silicon substrate surface. The wafer is then subjected to an epitaxial growth sequence where it is hoped that silicon epitaxy will selectively nucleate and grow inside the seed window, but will not grow. on the masking oxide surface. Results of SEG growths using $SiCl_4$ as the silicon source, at atmospheric pressure, and without the addition of HCl to prevent nucleation were poor.[30] The prevention of silicon nucleation on the masking surface, as well as maintaining even growth across the masking window, was difficult.

However, the 1970's brought continued development in selective epitaxy. Comparison studies were made between growth methods using various reactor gas combinations such as SiH_4/H_2, SiH_4/Ar, and $SiCl_4/H_2/HCl$.[31] The $SiCl_4/H_2/HCl$ composition, with controlled amounts of added HCl to prevent silicon nucleation on the masking oxide, emerged as the best overall arrangement for producing

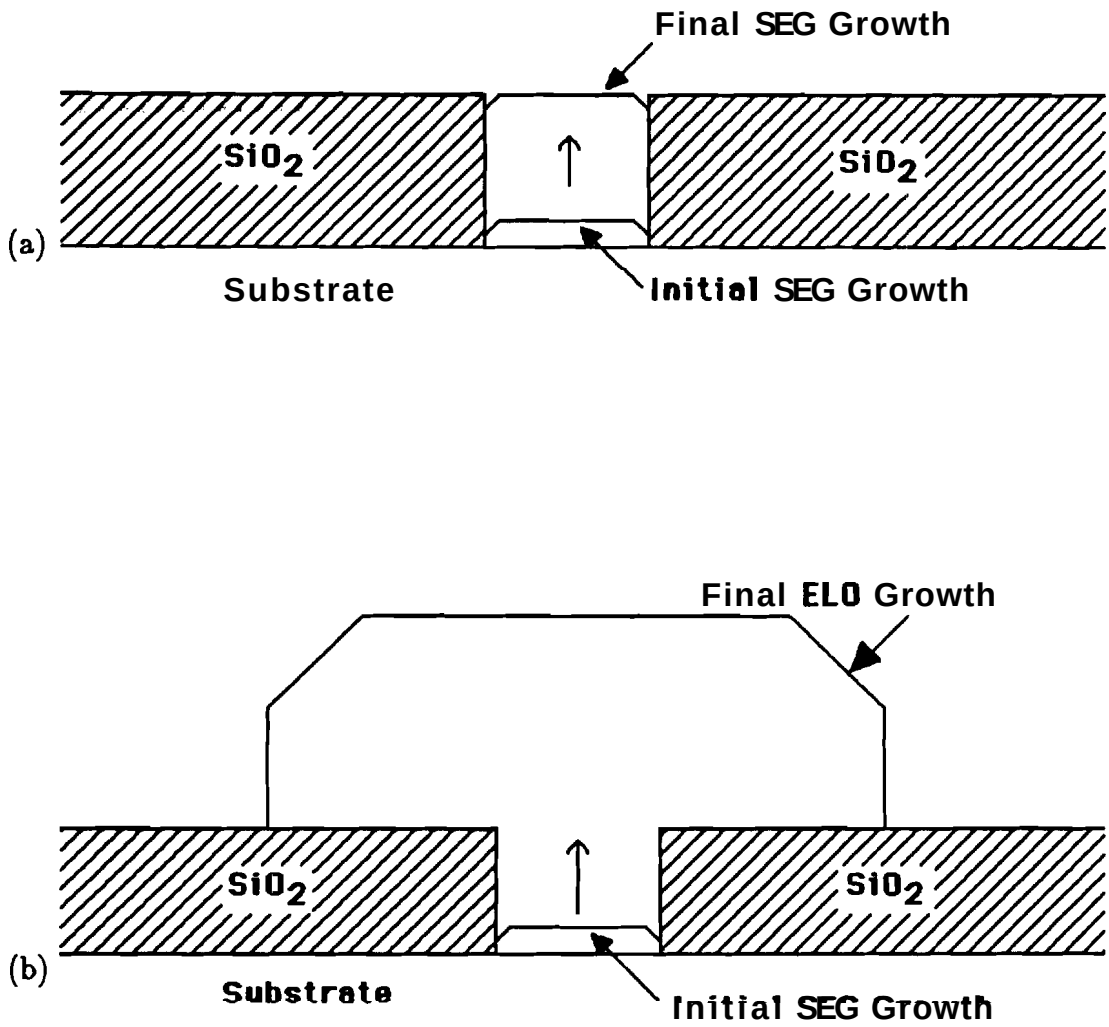


Figure 2.9. Two major selective epitaxy technologies: (a) Selective Epitaxial Growth (SEG) of silicon terminates as the SEG surface reaches the masking layer surface, (b) Epitaxial Lateral Overgrowth (ELO) allows the silicon material to grow out laterally over the masking surface.

selective, uniform growth surfaces. The $SiCl_4/H_2/HCl$ gas composition was considerably less sensitive to variations in reactant concentrations and growth temperatures across the wafer than the other two systems.

Significant breakthroughs in SEG technology finally arrived with the use of reduced pressures (<200 Torr), reduced temperatures (<1000°C), and dichlorosilane in the source gas composition ($SiH_2Cl_2/H_2/HCl$) as reported by Tanno et al. in 1982.[32] The reduced pressures and temperatures resulted in: a) improved SEG surface planarity and morphology, b) improved selectivity, c) apparent reduction in SEG/sidewall interface defects, d) decreased temperature variability, and e) decreased undercutting of the masking material.

In the area of electrical material quality, there are many varied reports of junction diodes, and both MOS and bipolar transistors fabricated; in bulk SEG material. The best controlled and most detailed analysis included results of identical bipolar devices fabricated in substrate, single layer SEG and double layer SEG materials.[33] With diode ideality factors ($\eta \cong 1.0$) and peak current gains ($\beta \cong 445$—480) identical for devices in all three materials, the results demonstrated the excellent device quality of the bulk SEG material.

However, one of the major issues that developed over the use of SEG for device fabrication is the material quality at the sidewall SEG/oxide interface. Large reverse leakage currents and low reverse breakdown voltages have been reported for cliode junctions which intersect the sidewall SEG/oxide interface inside the seed hole.[34, 35] Klaasen reported development of a special device based upon a planar gate controlled diode, the sidewall gate controlled diode (SGCD),[36] for investigation of the nature of the electrical defects near the sidewall SEG/oxide interface. Carrier lifetimes were estimated at 20 ns near the sidewall in the SEG. This value is over 3 orders of magnitude lower than the bulk SEG lifetime of 100 μs as measured using standard planar gate controlled diodes. SGCD I-V plots indicated that the defects were located in the bulk near the SEG/oxide interface, but are not bonding defects at the interface. Sufficient tests to indicate whether the number of defects could be decreased were not definitive.

Generally, it is known that growth temperatures below 1000°C and pressures below 200 Torr with the gas combination of $SiH_2Cl_2/H_2/HCl$ produce the best combination of growth rate, selectivity, surface morphology, and growth uniformity. Already SEG is finding its way into commercial use as a device isolation

scheme to replace the standard LOCOS process,[35,37-39] as an aid to building VLSI SRAM's,[40] as a technique for realizing self-aligned, thin base regions,[41] and as a way to reduce lateral autodoping of buried layers.[42]

2.3.2 ELO Development

Beyond lateral device isolation, researchers have been attempting to form fully isolated SOI (Silicon On Insulator) layers with appropriate quality in which to build VLSI devices and circuits. Conventional dielectric isolation, laser and strip heater recrystallization of polysilicon, and various other methods have all failed to provide thin, low defect density, large area, SOI layers at reasonable costs.

Epitaxial Lateral Overgrowth (ELO), developed directly from SEG technology, is an alternative technique for obtaining SOI films and inter-device isolation. ELO growth, similar to SEG growth, starts with a single crystal substrate with a patterned layer of masking material, usually SiO_2. The wafer is then placed in a CVD epitaxial reactor for growth in the same manner as SEG. However, instead of terminating growth when the SEG surface is level with the masking surface, the silicon is allowed to continue to grow laterally over the surface of the oxide as seen in Figure 2.9(b). ELO experiences the same intrinsic growth difficulties as SEG, the nucleation of polysilicon on the masking oxide, and the formation of defects and subsequent decrease in material quality. For these reasons, to obtain reasonable quality ELO material, low pressures and temperatures, as well as the addition of HCl to the gas flow is necessary. Optimization of the growth process has produced single crystal ELO material with low defect density and smooth, mirror-like surfaces.

The aspect ratio is an expression which relates the amount of lateral growth across the mask surface (from the edge of the seed window) to the amount of vertical growth (above the mask surface). High quality ELO films have only been grown with aspect ratios very near 1:1. That is, for every 10 μm of lateral overgrowth, there will also occur approximately 10 μm of vertical growth above the masking surface. Therefore, although theoretically an ELO layer could be grown across an entire wafer, it is the approximate 1:1 aspect ratio and the practical limit on vertical growth which restricts the amount of ELO which can be grown laterally. The 1:1 aspect ratio of ELO growth is therefore a serious restriction to

the use of ELO by itself in forming large area, thin SOI layers for VLSI device fabrication.

One device which would potentially use ELO growth is the proposed ELO-bipolar junction transistor (ELOBJT).[43] However, in order to be feasible, a suitable planarization technique for reducing the as grown ELO height must be developed. Two general methods of planarization have been investigated for obtaining such thin ELO layers. One method involves the use of thick photoresists and damaging reactive ion and chemical etching and has difficulties retaining the thickness uniformity and quality of the ELO surface.[44] The second method, chemical-mechanical polishing (CMI?), has traditionally for full wafer planarization been an expensive, time-consuming process which also has difficulties with surface thickness uniformity. However, due to recent advances in polishing slurries and the use of local area etch stops, CMP has shown increased feasibility for use on large area VLSI wafers.

CMP's renewed growth is due to its recognition as a key technology for the realization of scaled, high-density VLSI circuits. Specifically, CMP has been utilized For shallow trench isolation in a 16 Mbit dynamic random access memory (DRAM).[45] Beyond isolation schemes, CMP has been applied to ELO growths from small seed windows in order to fabricate ultra-thin local silicon on insulator (SOI) material.[46] Shahidi et al. [47] reports the fabrication of 0.1 μm thick planarized SOI regions in up to 10 μm widths with thickness control of 10 nm or better over several square centimeters. The fabrication process can be seen in Figure 2.10 where ELO material is grown out of two adjacent seed holes and allowed to merge over an oxide surface. CMP is then used with an appropriate etch stop material (oxide) to remove the vertical height of the as-grown ELO silicon and obtain a smooth planar surface whose thickness is controlled by the thickness of the etch stop layer. CMOS devices were then fabricated in the material and showed device characteristics identical to substrate devices.

One area of investigation which ELO shares with SEG, is the material quality at the oxide interface. As the ELO material grows laterally across the masking oxide, junctions intersecting the lateral ELO/oxide interface will probably exhibit similar increases in leakage current as junctions at the vertical SEG/oxide interface. Recent results of a capacitance-voltage analysis from the growth of an ELO layer over an oxidized polysilicon gate, indicate that the surface state

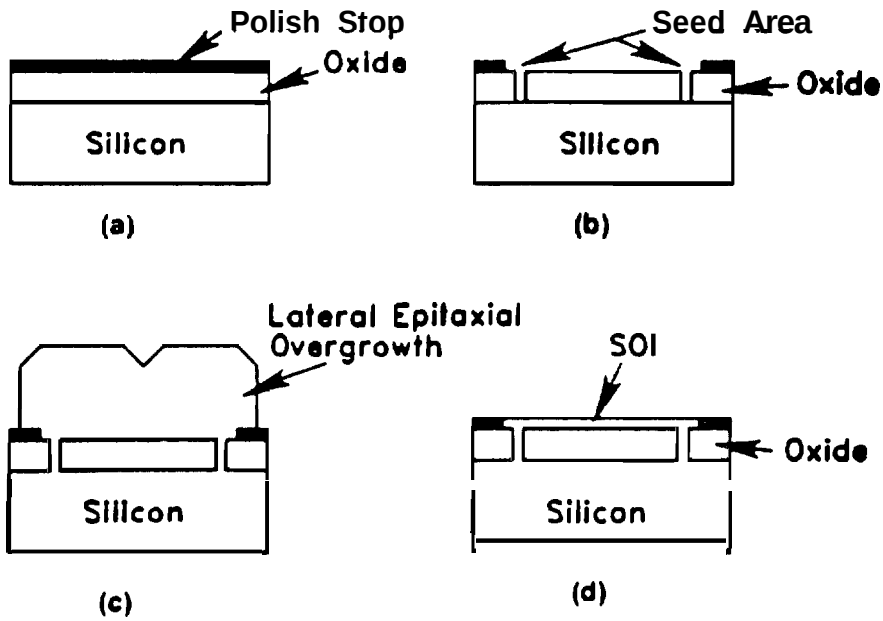


Figure 2.10. Fabrication sequence for obtaining SOI using epitaxial lateral overgrowth and chemical mechanical polishing.[47]

density at the ELO/poly-oxide interface is on the order of 10^{11} cm^{-2} eV^{-1} near midgap.[48] This value compares favorably with surface state densities of thermally oxidized silicon surfaces without post-oxidation or post-metallization annealing.

2.3.3 Confined Lateral SEG (CLSEG)

Due to the difficulty of obtaining large area, thin SOI layers with ELO technology, a novel technique called confined lateral selective epitaxial growth (CLSEG) has been developed.[49] The process starts similar to SEG with the opening of a seed window in a thick masking layer and re-oxidation of a thin oxide within the seed window. A sacrificial layer of α-silicon is then deposited and defined over the seed window, and a thin thermal oxide grown on the surface of the α-Si which recrystallizes into fine grained polysilicon. Finally, a nitride layer is deposited for mechanical support as shown in Figure 2.11(a). Next, the via holes are opened to the polysilicon layer, and a selective, isotropic etch is used to completely remove the polysilicon from the cavity. A quick BHF dip removes the

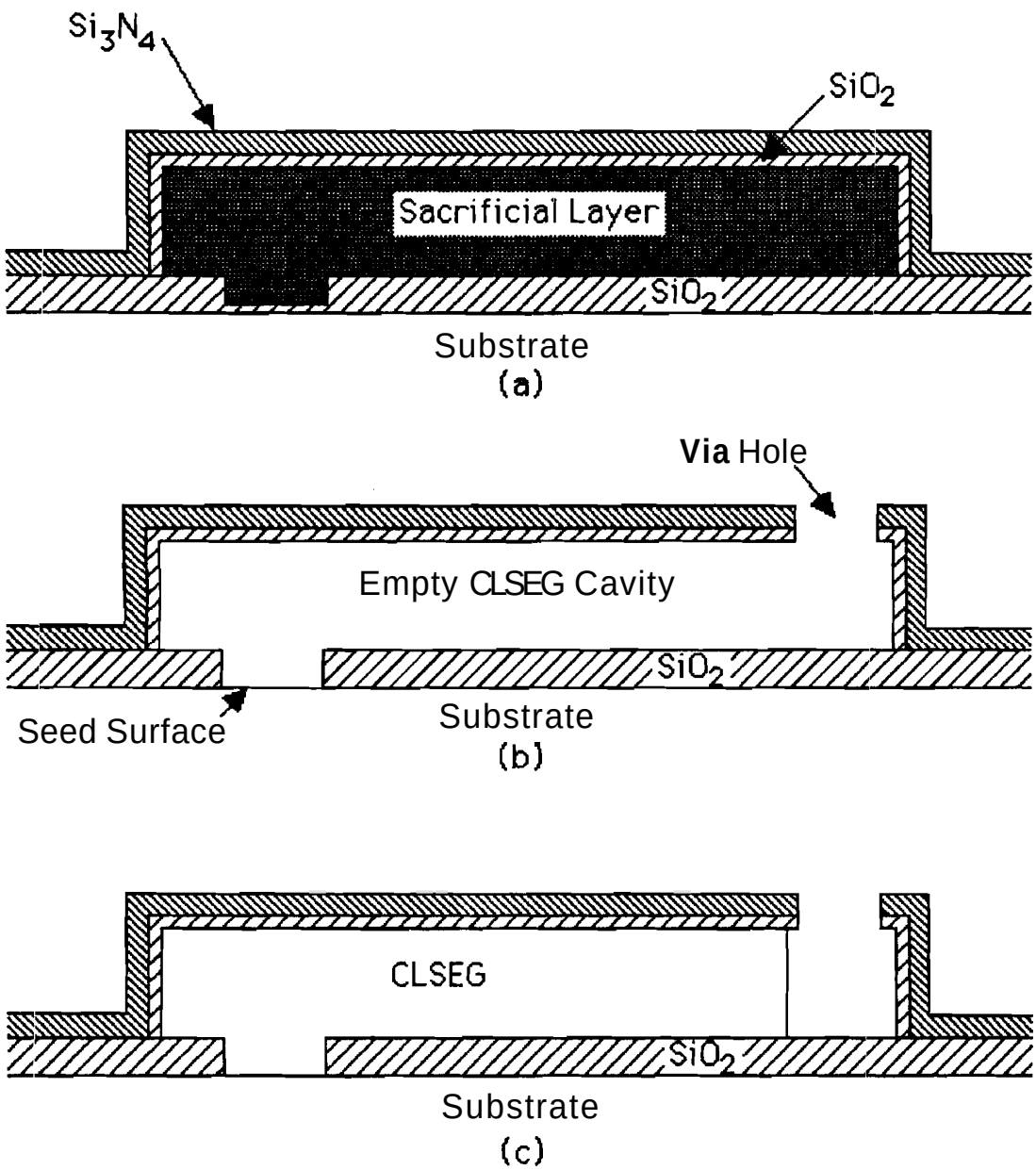


Figure 2.11. CLSEG process sequence: (a) definition of CLSEG cavity, (b) via hole and cavity etch, (c) growth of CLSEG horizontally within the cavity.

thin protective oxide from the seed surface within the cavity as seen in Figure 2.11(b). Finally, a standard selective epitaxy step produces SEG growth within the cavity nucleating on the seed surface and proceeding toward the via hole as shown in Figure 2.11(c). The bottom oxide layer was 133 nm, the top masking layer was 210 nm, and the CLSEG was approximately 900 nm thick, 8 μm wide, and 500 μm long.

Schubert fabricated junction diodes, p-channel MOSFETs, and bipolar NPN transistors in two different materials, CLSEG and large area SEG in order to determine the quality of the CLSEG material. The P/N diodes fabricated in both materials showed junction ideality factors of 1.05 or less, and virtually identical reverse leakage currents. In addition, the hole mobilities calculated from the p-channel MOSFETs were roughly equal in the range $\mu_p \cong 245-282 \frac{cm^2}{V\text{-}sec}$. Finally, vertical bipolar devices fabricated in the CLSEG [50] showed maximum current gains of 400 and junction ideality factors of less than 1.08. These results indicate that CLSEG material is of excellent device quality relative to large area SEG material whose quality was previously established.[33]

Although CLSEG material seems to show great promise for SOI integrated circuits, work is also steadily advancing on ELO/CMP techniques. Time will only tell which technique will prevail. However, it is possible that both will survive due to their respective advantages for use in varying applications.

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CHAPTER 3 - PROPOSED ELOBJT-3 DEVICE

Having explored the present level of state-of-the-art bipolar circuits, devices, and materials in chapter two, this chapter will present a new structure for a bipolar transistor, the proposed ELOBJT-3 device. The first half of the chapter details the proposed structure and fabrication sequence of the ELOBJT-3. The second half compares the device to an existing high-speed benchmark device (SST) using computer simulations of device parameters and circuit propagation delays.

3.1 Discussion of ELOBJT-3 Device

3.1.1 Structure

From the results of earlier propagation delay simulation studies,[1] the advantages and disadvantages of the originally proposed [2] ELOBJT-1 were analyzed. The primary advantage of the ELOBJT-1 device was its self-isolation and reduction of device parasitics. However, a major disadvantage was the absence of a viable technique for planarizing the two SEG/ELO growths required in the ELOBJT-1 fabrication, as well as its lack of self-alignment. Consequently, the ELOBJT-3 as illustrated in Figure 3.1 has been designed to retain and improve upon the advantages, yet overcome the disadvantages of the original design.

The ELOBJT-3 device overcomes the planarization problem of the ELOBJT-1 through use of Confined Lateral growth of SEG (CLSEG). The ELOBJT-3 as seen in Figure 3.1, is highly suited to high speed digital ECL (Emitter Coupled Logic) circuits, where reduction of collector-base capacitance C_{cb} is of prime importance. A doped CLSEG step is used for extrinsic base contacting, and a large area, SEG grown buried layer is used to simplify the process. In a circuit where a minimum collector to substrate capacitance is desired, the structure of Figure 3.1 could be modified to have dual opposing CLSEG contacts, one for extrinsic collector (to obviate the need for a buried layer) and one for

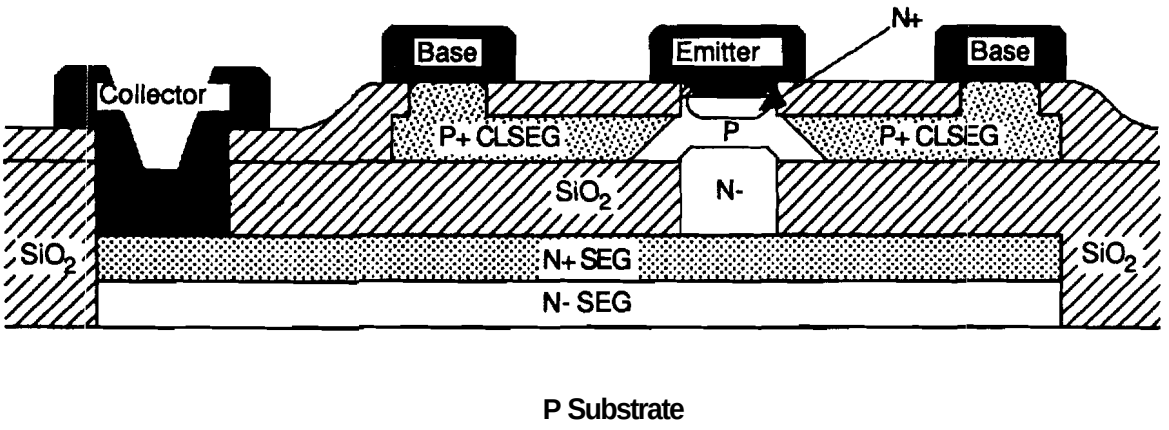

Figure 3.1. Cross-sectional device structure of the proposed ELOBJT-3 bipolar transistor.

extrinsic base.

The reduction of the C_{cb}, C_{cs}, and R_{bx} parasitics to their nearly theoretical minimums is accomplished through the use of dielectric isolation, concentric contacting, and lower resistivity single-crystalline material. The collector-base junction is confined to the intrinsic device area by dielectrically isolating the extrinsic base from the extrinsic collector with a relatively thick SiO_2 layer. As opposed to most advanced bipolar designs, the ELOBJT-3's extrinsic base contacts are made of highly doped (in situ grown) single crystal silicon material that completely surround the intrinsic device area. The lower resistivity of single crystal silicon compared to similarly doped polysilicon, [3,4] combined with concentric contacting, helps to significantly reduce the extrinsic base resistance.

The newly proposed ELOBJT-3 device contains many other advantages. Firsl; and foremost, for extremely high speed operation, the ELOBJT-3 can easily be scaled to sub-micron dimensions due to the completely self-aligned emitter-base and base/collector regions. Because the collector-base junction area is approximately the same as the emitter-base junction area, the device is expected

to have excellent forward/reverse operation characteristics, which are particularly useful for advanced I^2L circuits. Also, because the collector region of the ELOBJT-3 device is located entirely out of the substrate, device to device isolation is greatly improved without the need for complicated trench isolation techniques. As opposed to the original ELOBJT-1 structure, the new device has a relatively planar topology which is important for today's fine line lithographic processes. Finally, the device technology is extremely flexible and potentially applicable to BiCMOS structures.

3.1.2 Fabrication Process

A proposed process sequence for the ELOBJT-3 device can be seen in Figures 3.2 and 3.3. The process begins with a thick thermal field oxide into which a large SEG seed window is etched down to the P substrate. SEG is grown from the seed interface, first lightly N doped, then switching to in situ N+ doping as seen in Figure 3.2(a). It is believed that with proper growth optimization and seed hole alignment that faceting of the SEG can be minimized to an acceptable level. Growing the SEG only partially to the surface of the masking layer, the wafer is thermally oxidized as seen in Figure 3.2(b) to leave an approximately planar oxide surface.

In Figure 3.2(c), an amorphous silicon layer is deposited and patterned over one side of the underlying SEG structure, followed by a thermal oxidation to form the top cavity oxide and to recrystallize the amorphous material into fine grained polysilicon. The deposited α-Si therefore controls the exact thickness and area of the extrinsic base contact. Finally, a blanket LPCVD nitride is applied to render structural support to the top cavity oxide when the sacrificial polysilicon layer is removed. In figure 3.3(a), an anisotropic RIE etch is used to cut the central SEG seed hole through the nitride, both oxides, and the polysilicon layer. At the same time an isotropic RIE or perhaps a selective wet etch is used to clear-out most of the CLSEG cavity layer. Next, a standard N doped SEG is grown by seeding on the N+ SEG at the bottom of the seed hole. As seen in Figure 3.3(b), the SEG begins to grow laterally into the cleared CLSEG cavities, but is eventually halted as its growth seals the path of reactants into the cavity areas. A thin thermal oxidation or plasma deposited oxide caps the central SEG region to prevent further growth in later steps.

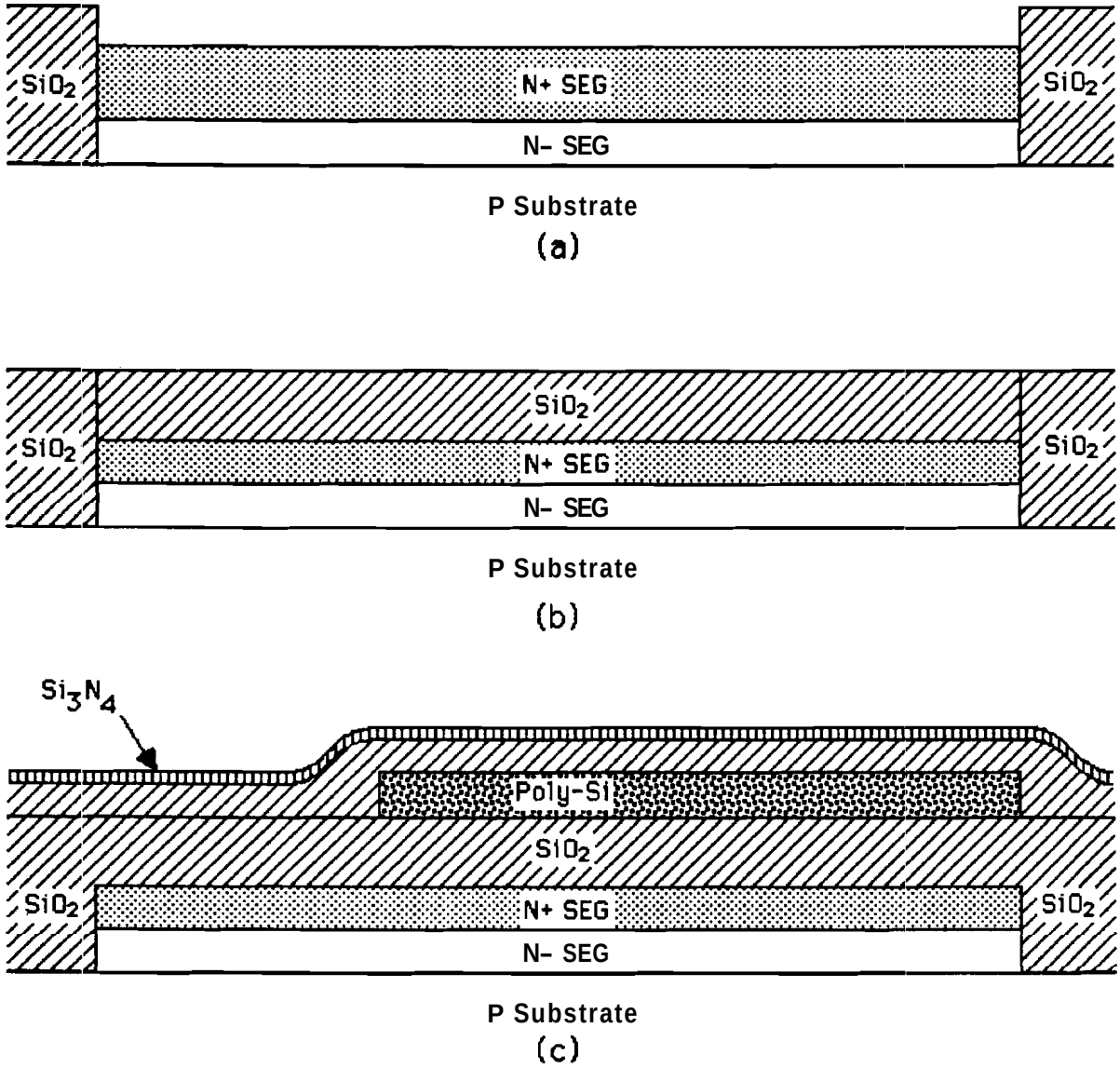

Figure 3.2. **Proposed ELOBJT-3 process sequence: (a) initial growth of N-/N+ SEG, (b) thermal oxidation to produce planar oxide surface, (c) deposit and pattern polysilicon cavity layer, oxidize to form top cavity layer, and deposit LPCVD nitride.**

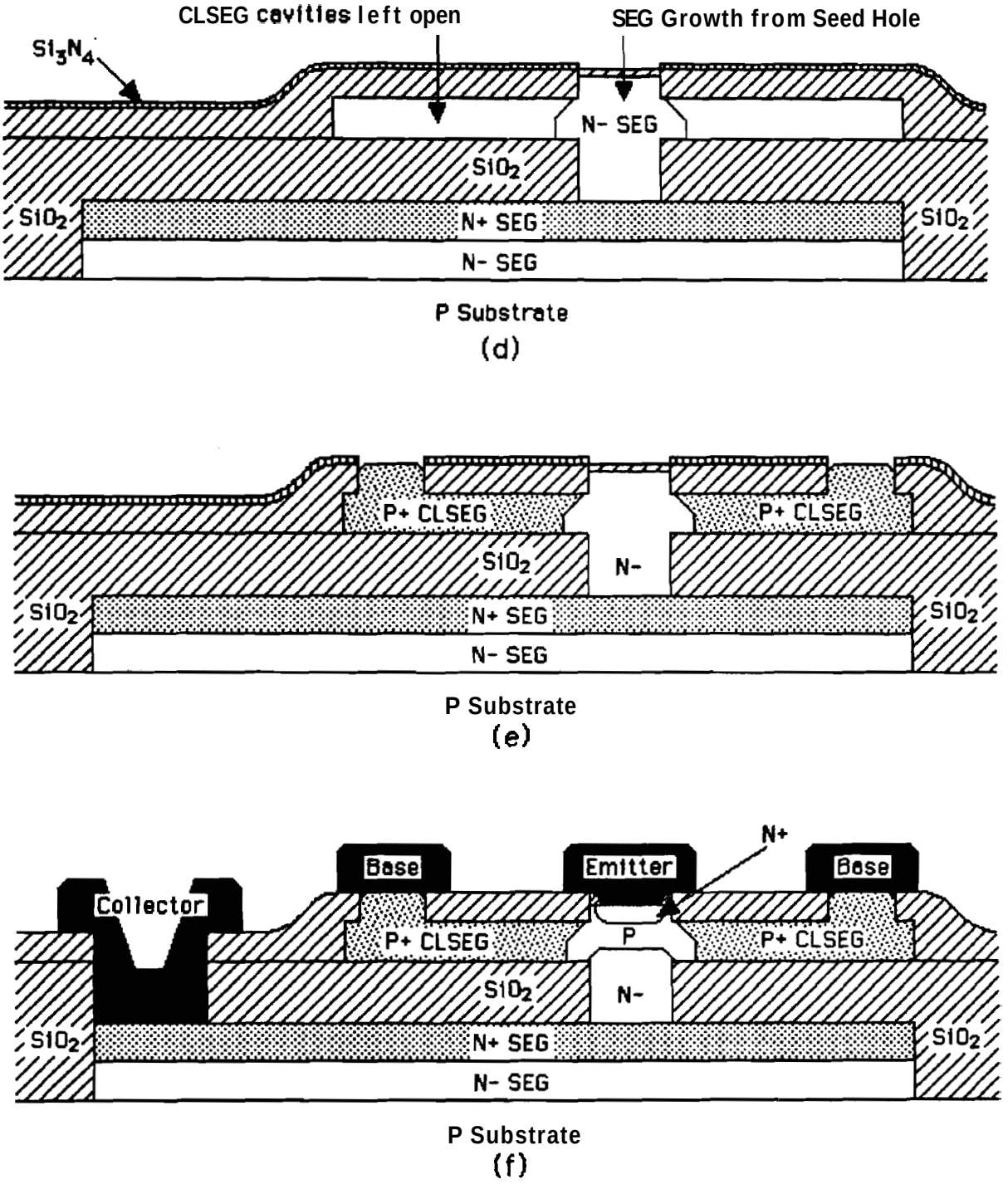

Figure 3.3. Continued proposed ELOBJT-3 process sequence: (a) etch seed window and CLSEG cavities, grow central SEG, and cap with thin thermal oxidation, (b) etch vias to cavity layer and grow P+ in situ doped CLSEG from sides of central SEG, (c) blanket implant intrinsic base, form sidewall spacer for N+ emitter implant, followed by emitter/base implant drive, etch contacts, and deposit and define metal for final structure.

Figure 3.3(c) illustrates the base via holes etched using RIE to completely clear-out whatever CLSEG cavity material is left from the previous RIE etch. After wet etching the thin oxide present on the SEG seed inside the cavity, P+ in situ doped CLSEG nucleates on the central SEG sidewall, and grows laterally, then vertically to fill the base via holes. In Figure 3.3(c), a blanket P-type Boron implant forms the intrinsic base region, followed by a thin conformal plasma oxide deposition and RIE etch to form the emitter sidewall spacer. The spacer and a non-critically aligned photoresist layer are then used to mask the SEG sidewall and the base contacts respectively from the blanket N+ emitter implant. A short thermal oxidation is used to drive and activate the base and emitter implants. Finally, the base and collector contacts are defined and etched, the thin emitter oxide is quickly removed, and metal is deposited and defined for the final structure of Figure 3.3(c).

The process includes three epitaxy steps and seven lithography steps through metallization. In terms of alignment, the structure has both self-aligned base/emitter and base/collector regions. The sub-collector is not self-aligned on the device shown in Figures 3.1 and 3.2, but would be self-aligned upon addition of an extra N+ CLSEG layer for the collector contact. All lithographic steps, excluding the trench definition, are non-minimum resolution and. most are non-critical contact alignments. Mis-alignment of the central SEG seed window to the CLSEG cavity layer will simply produce uneven CLSEG growths emerging from the base via holes. This should not be a problem since metal contact to these growths is non-critical and could even be made somewhere before the CLSEG emerges from the vias. The ELOBJT-3 structure could easily include a polysilicon emitter without any additional lithography steps by using the emitter implant mask to define a polysilicon emitter. Finally, the entire process uses largely standard IC processing equipment and technologies.

3.2 Simulation Studies

Two types of simulations were used to investigate the viability of the proposed ELOBJT-3 transistor. The device simulations attempted to calculate the relative improvement of the ELOBJT-3 device in reducing parasitic capacitances and resistances using the device simulator PISCES-IIb.[5] These parasitic device

parameters were then used to construct a full circuit model to investigate the improvement in circuit speed if the ELOBJT-3 device was used. Primarily, the device simulations were meant to establish the relative merit of the device.

3.2.1 Device Parameters

The device level simulations were used to predict, using various techniques, important device parameters expected from the ELOBJT-3 device, and to compare these parameters to those of an existing high speed bipolar structure, namely the Super Self-aligned Technology (SST). An important aspect of a comparison study is deciding upon the exact structures to be compared. Currently, the SST has the highest reported cut-off frequencies, in the 30-40 GHz range, of any standard bipolar process.[6,7] These devices have emitter widths of approximately $0.35\mu m$, even though the smallest lithography pattern size used is about $1.5\mu m$. Therefore, the $0.35\mu m$ emitter size SST device is used as the baseline device for the comparisons since there is extensive data reported for it in the literature.[8] Consequently, the ELOBJT-3 device used in the comparisons has identical minimum feature sizes and spacings of $0.35\mu m$.

This choice of equal minimum feature size for both devices might not seem fair to the SST, since the SST technology is using much larger lithography in making its $0.35\mu m$ wide emitter. However, typically the emitter width (area) of a device determines the amount of current drive of the device, and the current requirements are often fixed by the circuit design. Thus, the choice of $0.35\mu m$ minimum feature size for both the devices is justified.

Figure 3.4 shows the exact 2-dimensional structures and dimensions of the simulated SST and ELOBJT-3 devices. As much as possible, widths and thicknesses of material layers were made identical in the two devices. For these simulations, mostly regions of uniform doping density were used to approximate the real non-uniform dopings. The values relevant to the simulation of the four parasitics were: buried layer doping, $N_{BL} = 10^{19}\ cm^{-3}$, collector doping, $N_C = 10^{16}\ cm^{-3}$, intrinsic base doping, $N_{BI} = 10^{19}\ cm^{-3}$ peak gaussian, extrinsic base doping, $N_{BX} = 10^{19}\ cm^{-3}$, P+ polysilicon doping (SST), $N_{PP} = 10^{19}\ cm^{-3}$, and the usual dielectric constants for silicon and oxide.

Four base/collector parasitics of each device were simulated: C_{cb}, C_{cs}, R_{bx}, and R_{cx}. These four parameters were chosen for simulation because of their

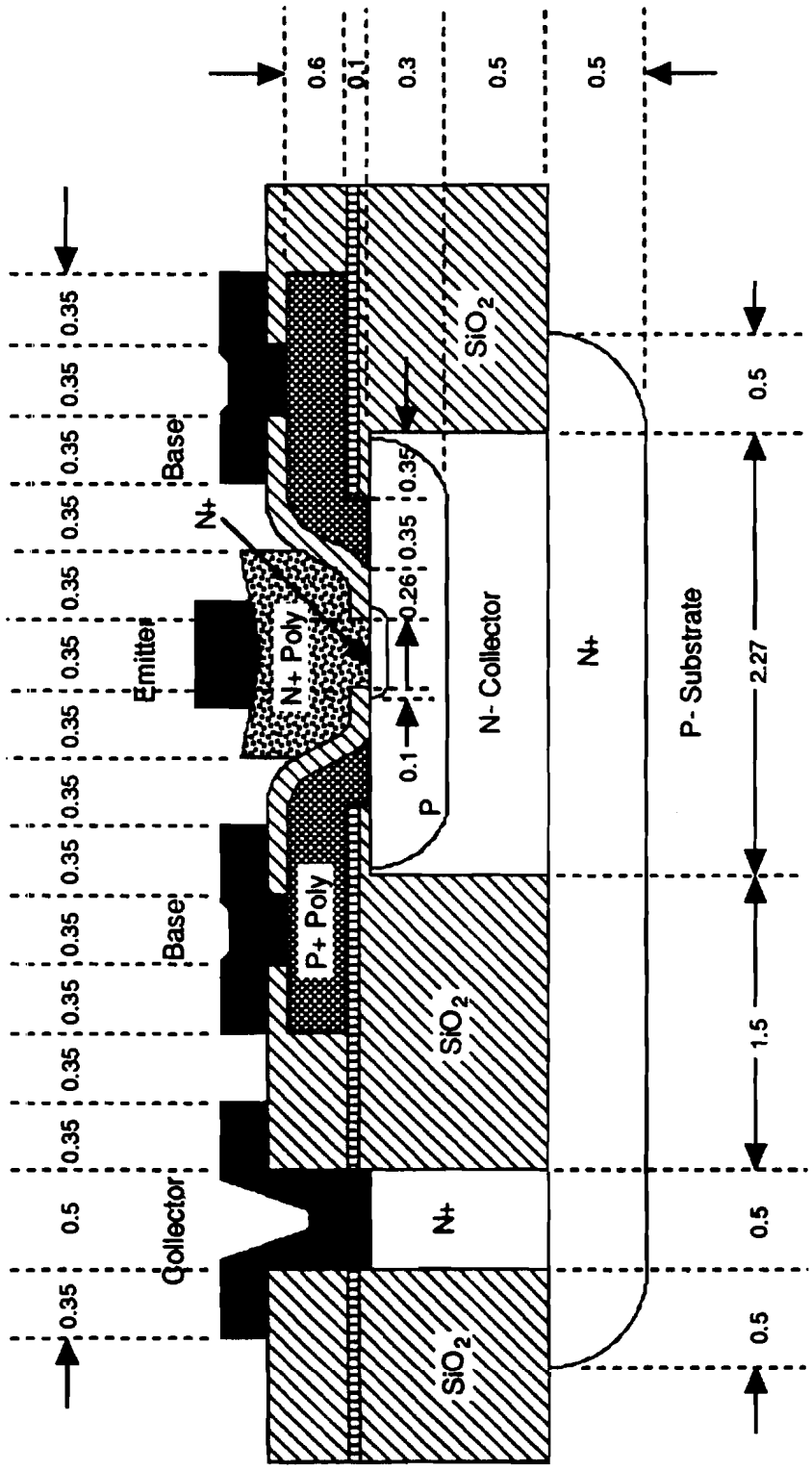

Figure 3.4 Cross-sectional device structure of the SST and ELOBJT-3 transistors showing critical dimensions used in 2-dimensional device simulations. All dimensions are in μm.

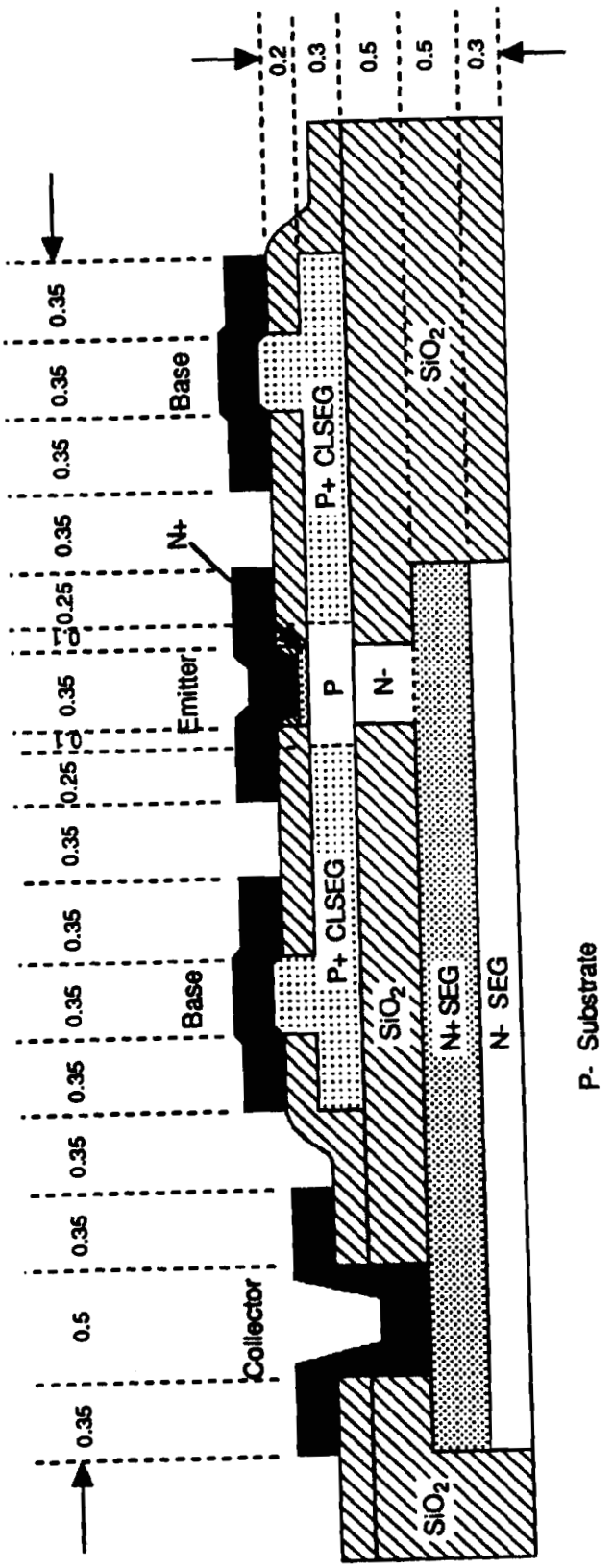

Figure 3.4. (cont.)

significant effect upon circuit propagation delay as detailed in Chapter 2, and because they would be affected by the changes in the ELOBJT-3's structure relative to the SST. An appropriate subsection of the device's total structure was used to simulate each parameter in order to reduce the number of extraneous grid points and therefore simulation processing time. For example, to simulate C_{cs} of the ELOBJT-3 device, only the collector and substrate regions were needed in the simulation grid (see Figure 3.5(a)). Alternatively, for the simulation of the ELOBJT-3 R_{bx}, only the extrinsic base material up to the edge of the intrinsic base is needed. Only one side of the two-sided structure is included, so the calculated resistance is halved for the final result (see Figure 3.5(b)). Typical active region DC bias points were first applied, and the DC solution calculated. Then, using the sinusoidal steady-state analysis option of PISCES-IIb, AC device parameters were calculated using a relatively low frequency, $f = 1KHz$, and amplitude, $V_S = 0.01V$. Finally, simplified hand calculations were performed to make sure the simulated results were within the correct order of magnitude.

The results from the device simulations are displayed in Table 3.1. As seen in the table, there are favorable improvements in three of the four ELOBJT-3 parameters. The extrinsic base resistance has been reduced by roughly 77 percent, the collector-base capacitance by 58 percent, and the collector-substrate capacitance by 43 percent. The slight increase in the collector resistance of 19 percent seems reasonable due to the narrowing of the collector's intrinsic region in the ELOBJT-3 device. However, this small increase in collector resistance is not expected to effect much change in the operating speed of a digital ECL circuit for example. As can be seen in the propagation delay terms of Table 2.2, R_c appears in terms which only account for 2.8% of the total delay. In Equation 2.5, R_c is so small it does not even appear. Overall, the preliminary device simulations verified the ELOBJT-3's reduced parasitics and propensity for high speed operation.

3.2.2 Circuit Propagation Delay

Although the results of the device simulations from section 3.2.1 indicate the ELOBJT-3 device will have remarkably improved base and collector region parasitics, a more important issue is overall circuit speed. Ultimately, improvements in device level parasitics are only important when they translate to

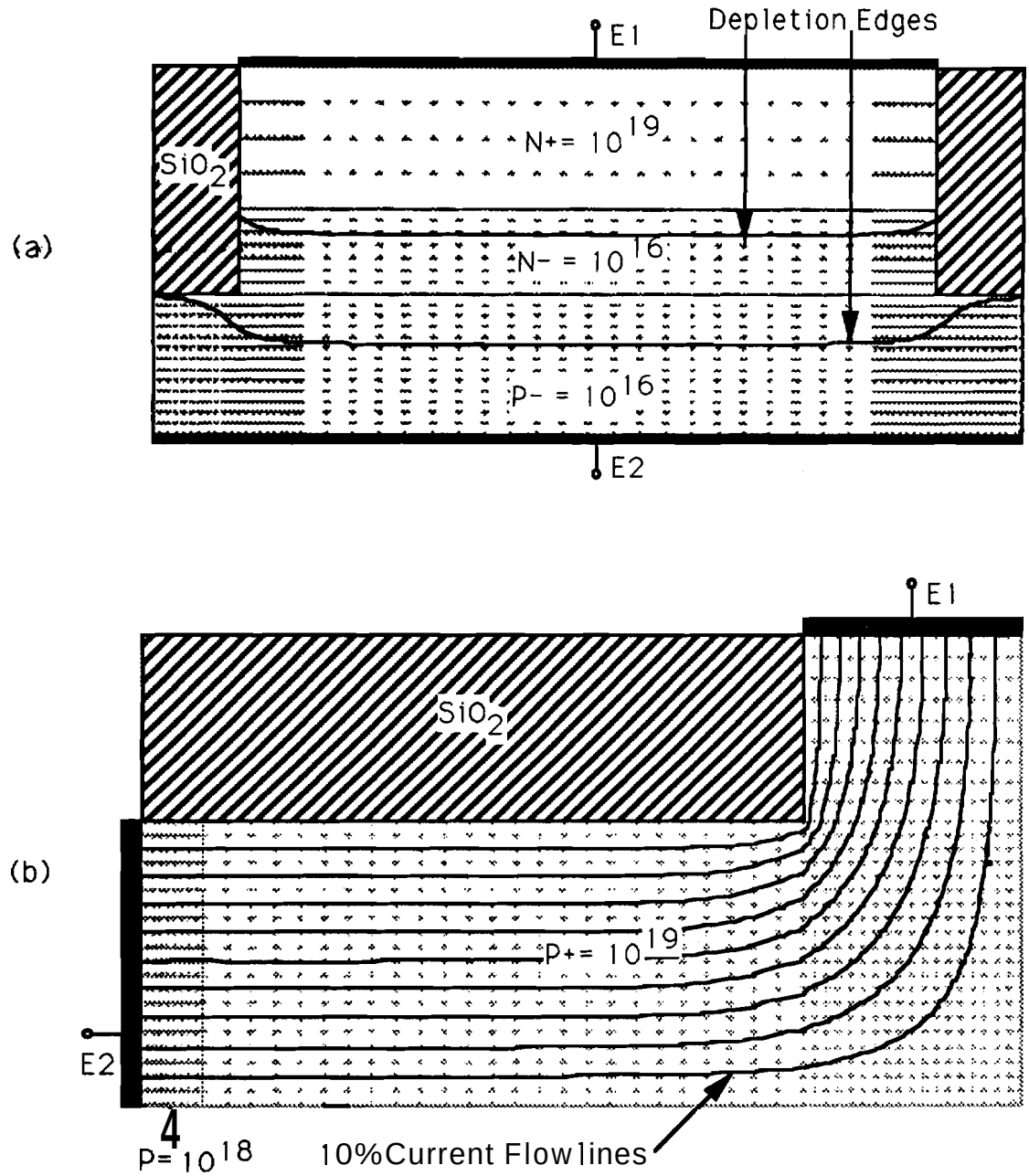

Figure 3.5. PISCES-IIb grids used in the simulation of ELOBJT-3 parameters: (a) collector-substrate capacitance C_{μ} and (b) extrinsic base resistance R_{bx}.

Table 3.1. Comparison of Parasitics for Proposed ELOBJT-3 vs SST Device (Using 0.35 μm Linewidths and Alignments).

Parameter	Method	SST	ELOBJT-3	%Change (sim. vs sim.)
$R_{bx_{(ac)}}$ $(\Omega\mu m)$	Hand Calc.	1445	260	-76.6
	Simulated	1302	304	
$R_{c_{(ac)}}$ $(\Omega\mu m)$	Hand Calc.	1214	1158	+18.8
	Simulated	766	911	
$C_{cb_{(ac)}}$ $\left(\frac{fF}{\mu m}\right)$	Hand Calc.	0.653	0.24	-58.4
	Simulated	0.697	0.29	
$C_{cs_{(ac)}}$ $\left(\frac{fF}{\mu m}\right)$	Hand Calc.	1.80	0.97	-43.1
	Simulated	1.97	1.12	

increased performance at the circuit level. Therefore, a circuit simulation comparison was performed to determine the advantages of the ELOBJT-3 device over the baseline SST device used in the device simulations.

3.2.2.1 The ECL Inverter Sub-circuit

The ECL inverter sub-circuit shown in Figure 3.6, was patterned after the standard ECL inverter circuit presented by Chor et al.[9] A constant reference voltage, $V_{ref} = 2.0v$, and current source reference voltage, $V_{cs} = 1.226v$, were chosen and are assumed supplied by an external reference voltage section not included in the simulation. The transistor current source then establishes a stable current, $I_{EE} = 0.8mA$, from the differential pair. The collector load resistors, $R_1 = R_2 = 625\,\Omega$ were then chosen to provide an approximate 0.5v output

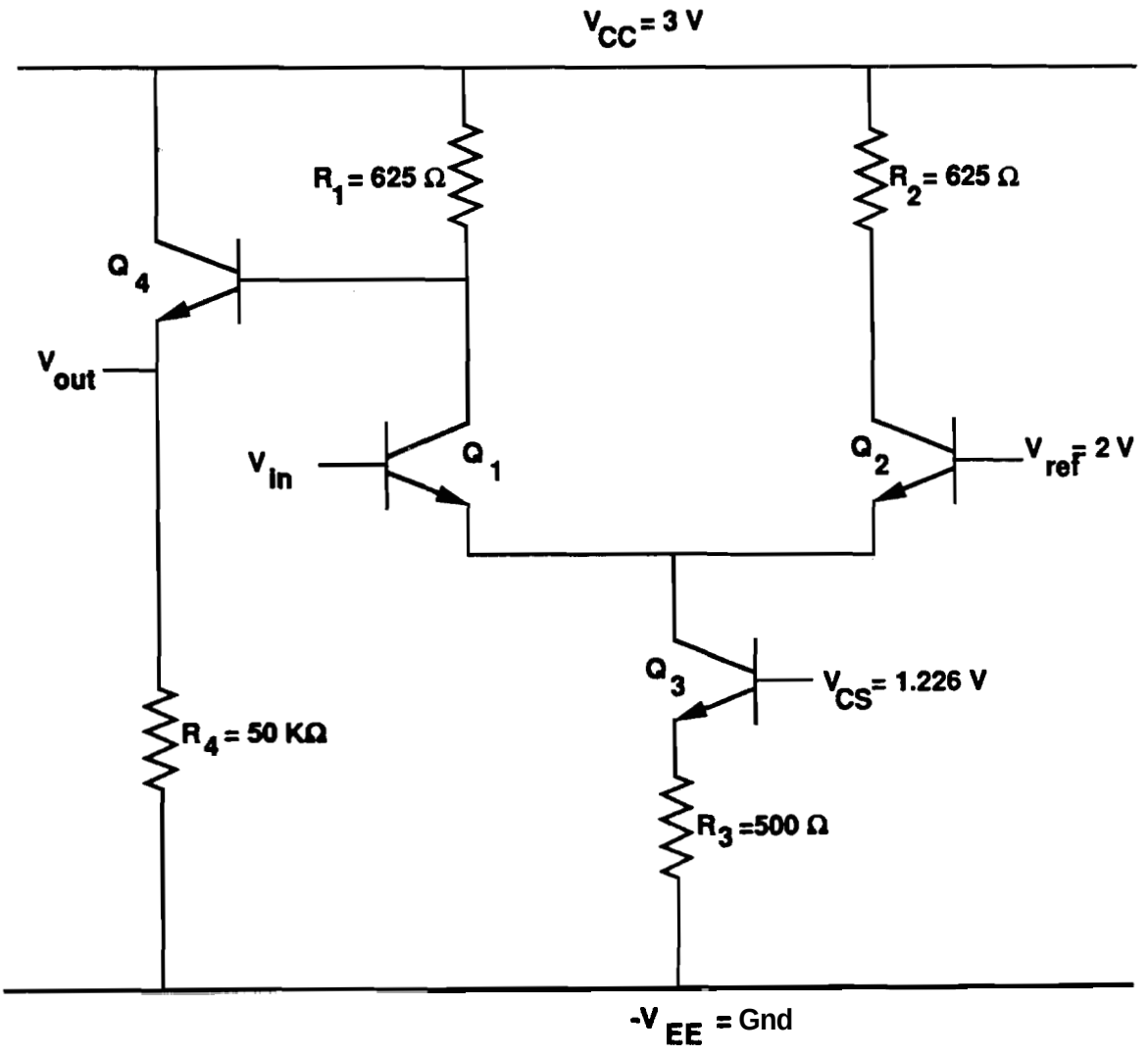

Figure 3.6. Schematic representation of the ECL inverter sub-circuit used for the propagation delay simulations.[9]

voltage swing which is very common in current ECL designs. In addition, a 3v power supply was used since this is becoming increasingly more standard in commercial ECL circuits.

An existing high-speed BJT device model from the Tspice library was used as the starting point for developing the SST and ELOBJT-3 device models. The standard Gummel-Poon 2 integral charge control model was used along with several external parasitic devices to more accurately represent real integrated bipolar devices. Basic transistor characteristics for the baseline SST device were taken from literature[10] values for an advanced self-aligned silicon bipolar device with an emitter area $A_E=0.4x4.0\mu m^2$. The SST and ELOBJT-3 models were then formed by substituting into the previous model the relevant base and collector parasitic parameter values from section 3.2.1. Since the section 3.2.1 values were calculated in a per length format, the values in Table 3.1 were appropriately multiplied or divided by 4 μm in order to form the correct values for SST and ELOBJT-3 devices with emitter areas of $A_E=0.35x4.0\mu m^2$ neglecting end effects. These values used in the circuit simulations for the SST and ELOBJT-3 device models are listed in Table 3.2. Parameters were sometimes divided into intrinsic and extrinsic components for proper insertion into the simulator's device models.

3.2.2.2 Tspice Simulations

An interactive version of the SPICE circuit simulator Tspice [11] was used to investigate the propagation delay times of two digital bipolar ECL circuits, one constructed using a model representing the standard SST baseline device, and the other using a model representing the ELOBJT-3 device. The circuit used for the simulations was a string of eight ECL inverters. In the first simulation, the propagation delay was calculated using the standard SST device model for all transistors in the circuit. The same simulation was then repeated using the ELOBJT-3 device model, and the propagation delays compared. The Tspice input file for the ELOBJT-3 inverter string is listed in Appendix A. The 8 gate ECL inverter string provides a good first order approximation of digital gate propagation delay time. [12] Propagation delays were calculated as a per gate average over four gates. The voltage waveforms from the ELOBJT-3 simulation are shown in Figure 3.7. Note that the input waveform to the fourth gate as well as the output waveform from the seventh gate follow each other through the transitions from low to high and high to low. It should also be noted that the output

Table 3.2. Summary of SST and ELOBJT-3 Device Model Values for 0.35 x 4 μm^2 Emitter Area Devices.

Parameter	SST	ELOBJT-3
r_{bx} (Ω)	325.5	76.0
r_{ci} (Ω)	301.2	375.5
r_{cx} (Ω)	82.0	80.0
C_{cbi} (fF)	0.37	0.46
C_{cbx} (fF)	2.42	0.70
C_{cs} (fF)	7.88	4.48

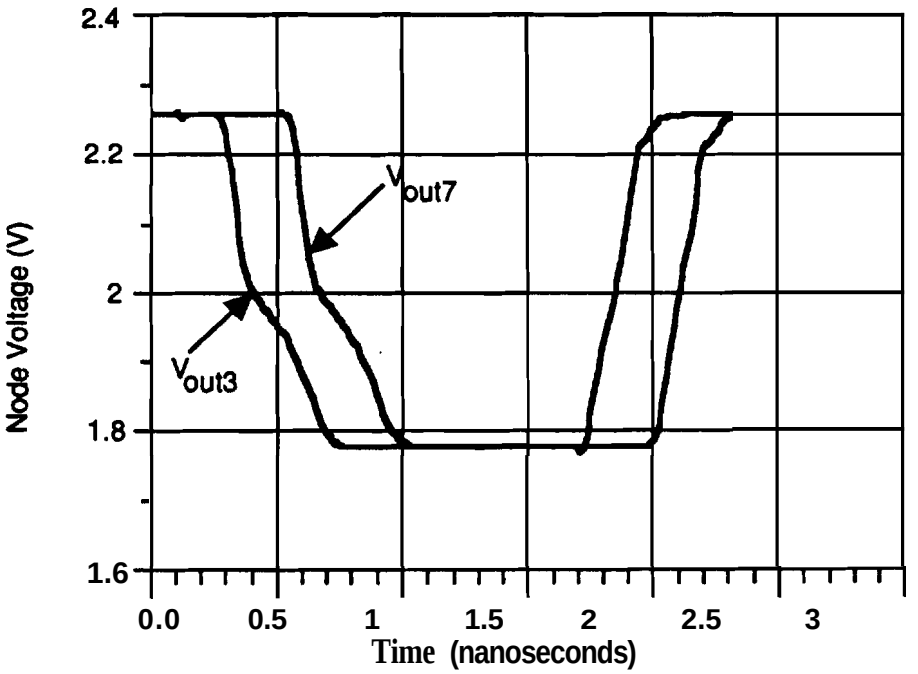

Figure 3.7. Simulated intermediate voltage waveforms output from gates #3 and #7 used in ELOBJT-3 circuit simulations. Propagation delay is taken as difference in time between the two waveforms crossing the V_{ref}=2.0v line, divided by 4 to obtain τ_d per gate.

and input do not change opposite each other because there are an even number of gates between the two signals. The propagation delay from the SST simulation measured at $V_{ref} = 2.0$ volts was determined to be approximately 104.7 ps/gate. From Figure 3.7, the ELOBJT-3 propagation delay was obtained as approximately 65.6 ps/gate. The results of the simulations are shown in Table 3.3. The

Table 3.3. Summary of Circuit Simulation Results Comparing Propagation Delays per Gate for an 8 Gate ECL Inverter String Using Two Different Bipolar Models.

Device Model	Propagation Delay τ_p (ps/gate)	% Change over SST
SST	104.7	-
ELOBJT-3	65.6	-37.3

propagation delay of the circuit employing the ELOBJT-3 device shows an improvement of approximately 37 percent over the circuit using the state-of-the-art SST baseline device.

3.2.2.3 Analytical Calculation

As one last check, the ECL inverter propagation delay was calculated using the analytical expression of Equation 2.5. However, this time the intrinsic device parameters reported by Fang[12] for a 0.5 μm emitter silicon device vvere used, with the base and collector parasitics of Table 3.2 added. The calculated delays were 13.04 ps and 21.3 ps for the ELOBJT-3 and SST devices respectively, an improvement of 38.8%. This matches almost exactly the 37.3% improvement obtained in the actual simulations. It also suggests that the discrepancy between simulated propagation delay (105 ps) and reported delay (30 ps) for the SST device comes from inaccurate intrinsic device parameters used from the existing Tspice bipolar model, or from non-optimum biasing of the Tspice circuit.

3.3 Summary

A new bipolar device structure, the ELOBJT-3, was presented which promises to provide increased speed by reducing critical device parasitics to their theoretical minimums. A fabrication process for the ELOBJT-3 device was detailed which uses largely standard commercial processing equipment and techniques. In order to determine the viability of the device, a simulation comparison of expected device parasitics for the ELOBJT-3 versus a baseline SST device was performed. Two-dimensional simulation of specific device parameters using PISCES-I1 software showed remarkably reduced values for collector-base capacitance C_{cb}, extrinsic base resistance R_{bx}, and collector-substrate capacitance C_{cs}. Finally, a Tspice circuit simulation comparing the use of the ELOBJT-3 device versus a comparably sized SST device in an 8 gate ECL inverter string clearly showed a considerable reduction (37.3%) in the average propagation delay time. The device and circuit simulations therefore qualitatively show the high-speed improvement of the proposed ELOBJT-3 device over existing state-of-the-art silicon bipolar devices.

3.4 References

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12. **Wen Fang, "Accurate Analytical Delay Expressions for ECL and CML Circuits and Their Applications to Optimizing High-Speed Bipolar Circuits," Journal of Solid-State Circuits, vol. 25, pp. 572-583, IEEE, April, 1990.**

CHAPTER 4 - ELOBJT-3 PROCESS DEVELOPMENT

The utility of the ELQBJT-3 device structure is reduced base and collector parasitics, R_{bx}, C_{cb}, and C_{cs}, as simulated in Chapter 3. However, fabrication of the ELOBJT-3 structure is needed first before measurements of these parameters can be compared to values predicted by computer simulation. Although most of the processing steps detailed in section 3.1.2 are based upon recognized industry standard techniques, one never fully understands the difficulties involved until fabrication is completed. Chapter 4 therefore details the process simulation and experimental fabrication of the proposed ELOBJT-3 device. In section 4.1, the two-dimensional simulations of the final scaled-down high-speed device are presented. The second part of the chapter, section 4.2 presents the experimental fabrication performed in obtaining a functioning ELOBJT-3 device.

4.1 Process Simulation

The TSUPREM-4 process simulator [1] has been used extensively to investigate the fabrication process of the proposed ELOBJT-3 device and to produce an output file which describes the completed device's structure and doping. Because an optimized ELOBJT-3 device is intended to be an ultra-small high-frequency device, two-dimensional simulations were essential to accurately model the peripheral and lateral aspects of the device. Although many problems were encountered in using TSUPREM-4 to simulate SEG and CLSEG growth, reasonable results were obtained.

4.1.1 Simulation of SEG/CLSEG Growth

Most of the ELOBJT-3 process steps were simulated in TSUPREM-4 with the available commands. However, the growth of selective epitaxy material is one process technology which is not supported by the software. Therefore, a number

of normal TSUPREM-4 commands were combined to approximate the growth of SEG/CLSEG for these simulations.

TSUPREM-4 does not include a rigorous epitaxy step, i.e. one which simulates dopant movement during the deposition of the epitaxy layer. However, the program does include two very versatile commands, deposition and etch. The deposition step conformally deposits a specified thickness and grid spacing of material on the exposed top surface of the structure. The etch step removes a specific material (or all material) within the boundaries of a user defined area. Finally, the core simulation capability of the program lies in its high temperature diffusion step which simulates dopant diffusion and oxide growth two-dimensionally using the specified temperature, ambient gases, and length of time.

'The simulation of SEG (CLSEG) growth began with deposition of the masking (cavity) layer(s). The seed hole (cavity) was then formed by etching away the appropriate amount of material using the etch step. Next, a deposit step was used to conformally deposit enough material to fill the seed window (cavity) with the desired amount of silicon, and at the same time depositing unwanted silicon material on the top of the masking (cavity) structure. Again, the etch step was used to remove the unwanted material and uncover the desired SEG (CLSEG) structure. Finally, the diffusion step was used to simulate the approximate thermal budget encountered during the growth of the SEG (CLSEG). In this roundabout way, growth of SEG and CLSEG were accurately simulated with the TSUPREM-4 program.

4.1.2 Discussion of Main Processing Steps

Having become familiar with the capabilities of the TSUPREM-4 simulator, the first main task was to translate the proposed process sequence of Figures 3.2 and 3.3 into a workable TSUPREM-4 input file. Table 4.1 details the major steps of the ELOBJT-3 process simulation. The actual input file is listed in Appendix B.

Every simulation run began by defining the initial grid, choosing enough points to ensure sufficient accuracy, yet not too many to overload. the host computer and require immense amounts of run-time. The substrate was defined with a uniform phosphorus doping of $10^{19} cm^{-3}$ and became the buried. collector layer of the device. The next group of steps formed the central SEG region as detailed

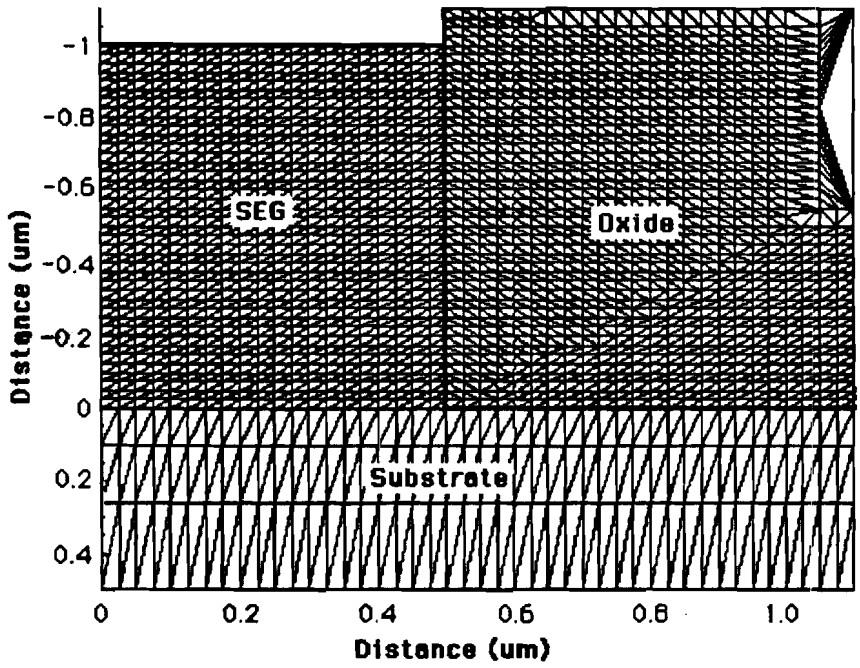
Table 4.1. Summary of Major Process Steps in TSUPREM-4 Input File Used to Simulate Fabrication of ELOBJT-3 Transistor.

Step	Description
1	Setup initial grid including buried layer
2	Etch central SEG seed hole and grow SEG
3	Wet oxidation to cap central SEG region
4	Etch CLSEG cavity and grow CLSEG
5	Etch off SEG cap oxide
6	Ion implant base
7	Form sidewall spacer and implant emitter
8	Wet oxidation to drive dopants
9	Etch contacts and metallize
10	→ Output structure file in PISCES-IIb format

in section 4.1.1. Grid spacings of deposited layers and exact vertices of etch corners all need extensive adjustments in order to retain correct grid spacings and triangle areas. The time of 10 minutes is used in the diffusion step assuming an approximate 0.1 μm/min SEG growth rate and 1.0 μm SEG thickness. Following SEG growth, the grid appears as in Figure 4.1(a). Immediately following the SEG growth, a thin thermal oxide was grown using a wet oxygen ambient in order to cap-off the central SEG region from further growth in later steps. At this point, the grid can be seen in Figure 4.1(b).

Next, the CLSEG cavity etch and growth was the largest group of commands due to the complexity of forming the CLSEG and its cavity. In this simulation, the via to the CLSEG layer from the structure's surface was located only 0.3 μm from the edge of the central SEG. This short spacing was used because the majority of the CLSEG region is simply a highly doped, low resistance contact region and does not appreciably affect the intrinsic device operation of interest. After depositing the in situ boron doped $10^{19}cm^{-3}$ CLSEG material, a diffusion step of 40 minutes was performed, again assuming an approximate 0.1 μm/min CLSEG growth rate and 4.0 μm of CLSEG lateral growth. The grid at this point can be seen in Figure 4.2(a).

(a)



(b)

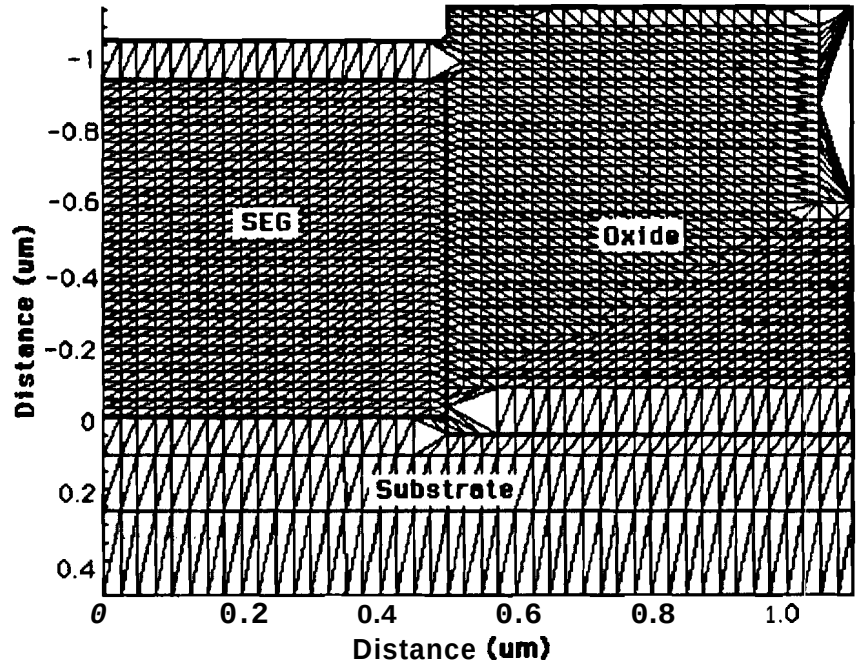
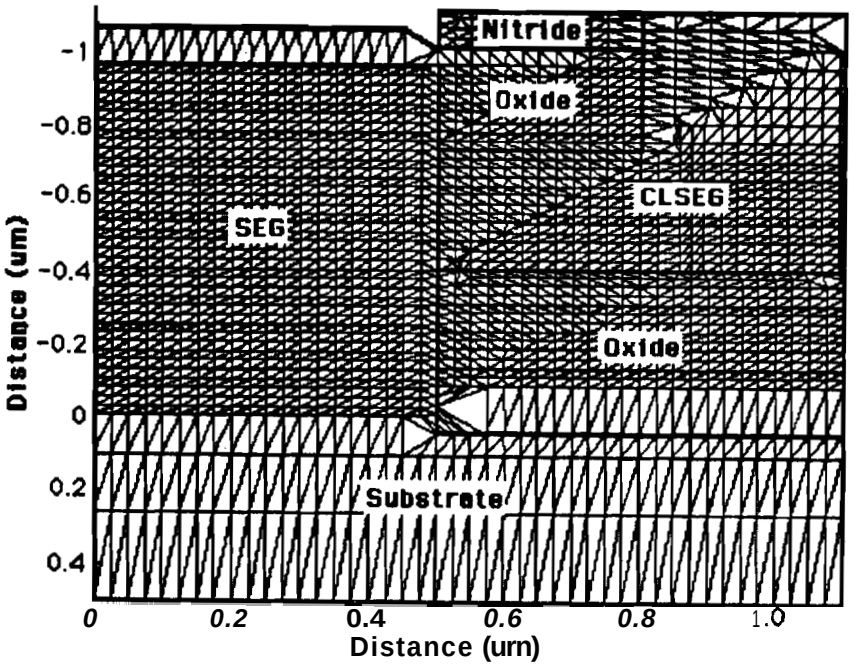


Figure 4.1. **Two-dimensional plots of intermediate TSUPREM-4 grids showing grid placement and density within various different materials as the simulation progresses: (a) after SEG growth, (b) after SEG capping oxide.**

(a)



(b)

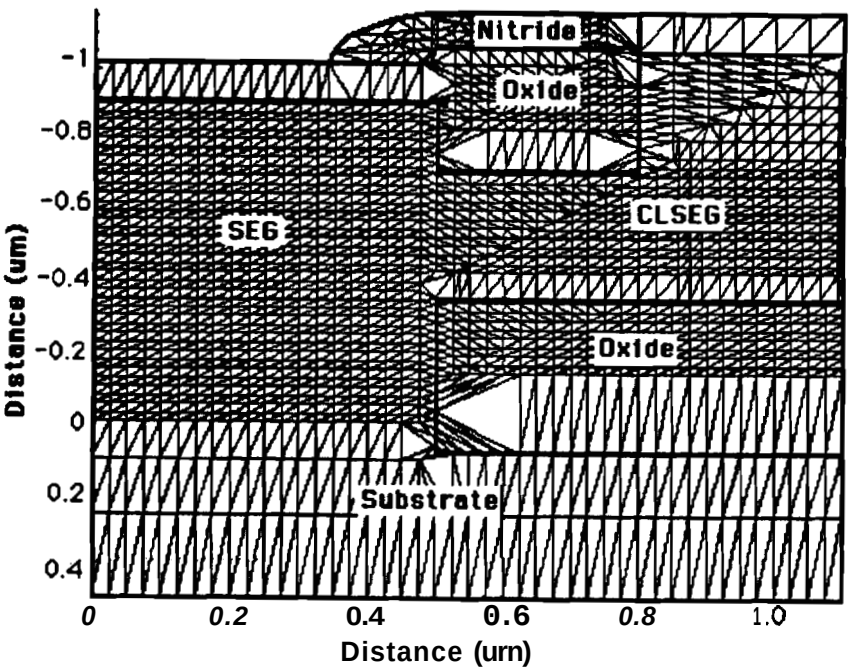


Figure 4.2. **Intermediate TSUPREM-4 grids: (a) after CLSEG growth, (b) after emitter/base implants and oxidation/drive.**

Once the CLSEG growth was finished, the central SEG oxide cap was removed by using the preferential dry etch command. The intrinsic base boron dopant was then blanket implanted at 100 KeV so that the base/collector junction is near the center of the CLSEG region and the base is then able to link-up with the boron doping of the CLSEG regions from the side. A conformal nitride was then deposited and dry etched. This procedure leaves a small sidewall spacer at the top of the SEG region near the sidewall interface. The spacer was used to reduce the amount of N+ emitter dopant near the oxide/SEG sidewall. An arsenic emitter was then implanted using a photoresist mask to protect the base CLSEG contacts. Finally, another wet oxidation was performed using the diffuse command to drive in the emitter and base dopings and seal the top of the central SEG surface as seen in Figure 4.2(b). This completed simulation of the high temperature processing steps.

4.1.3 Final Structure and Doping Profile

The final structure file output by the TSUPREM-4 simulator using the input file of Appendix B can be seen in Figure 4.3. The outlines of different material regions are bold lines, and contour lines delineate iso-concentration regions of net doping ranging from 10^{15} to $10^{19} cm^{-3}$. The majority of the doping contours reside in the central SEG region since this is where most doping levels are changing. The emitter N+ doping contours can be seen in the top of the SEG region. The horizontal area of few contour lines in the middle of the SEG about even with the CLSEG layer is the center of the base region. Just below this are the doping contours located at the base/collector junction. Near the bottom of the SEG are contours which show the out-diffusion of phosphorus from the heavily doped buried layer.

The majority of the CLSEG region is uniformly P+ boron doped and therefore devoid of any contour lines. However, along the right side of the SEG, there is out-diffusion of boron from the heavily doped CLSEG. This out-diffusion helps to link the extrinsic base CLSEG region to the intrinsic base region in the SEG and form a low resistance contact. However, at the same time, this heavily doped boron region moves toward the N+ doped emitter above and the N+ doped buried layer below. A tradeoff between reasonable emitter/base reverse junction breakdown voltages and a low resistance base link-up occurs with this out-

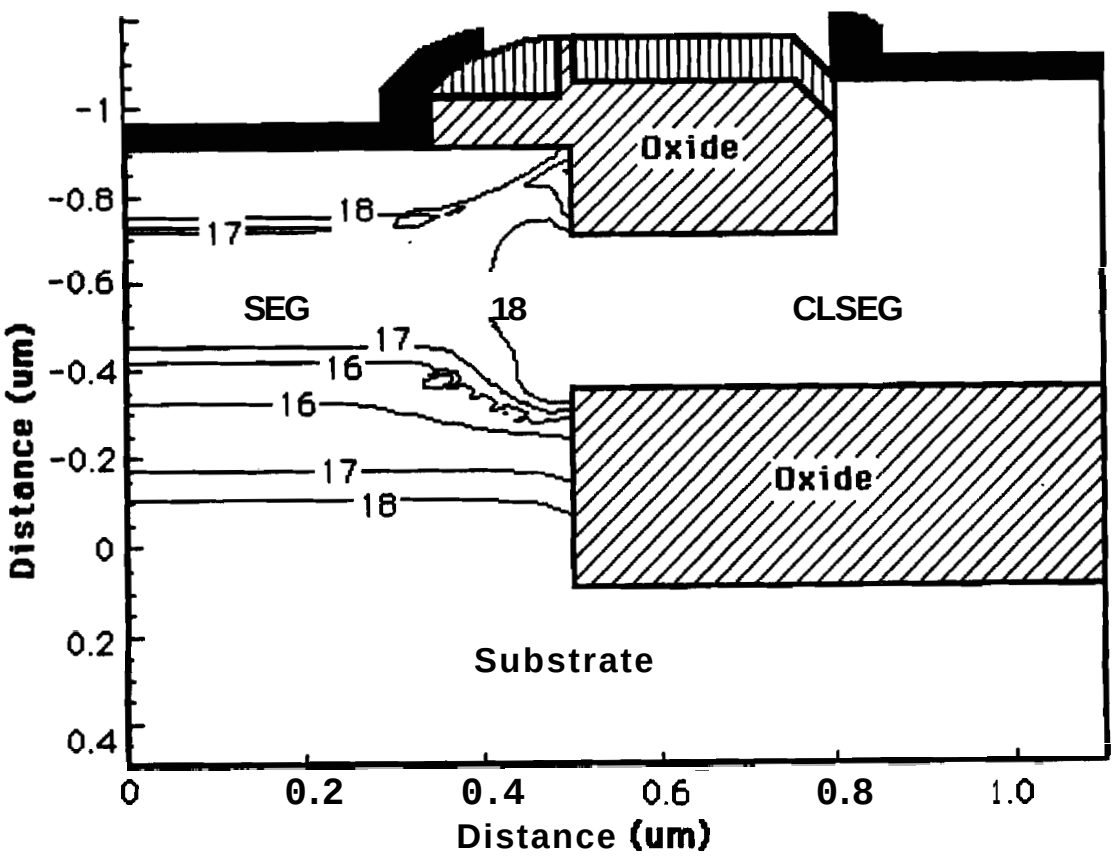


Figure 4.3. **Final TSUPREM-4 output structure file showing various material regions and doping iso-concentration curves.**

diffusion of boron into the intrinsic SEG region. Encroachment of the P+ doping on the emitter region also has ramifications on the forward biased switching speed of the device as documented by Chuang.[2]

A one-dimensional plot of the net doping concentration taken through the intrinsic device region at X=0.2 μm is shown in Figure 4.4(a). Directly below in Figure 4.4(b) is a similar plot of net doping concentration taken near the right edge of the central SEG region at X=0.45 pm. The emitter/base dopings in the intrinsic region are $2x10^{20}/5x10^{17}cm^{-3}$, whereas in the link-up region of Figure 4.4(b) they are $10^{20}/2x10^{18}cm^{-3}$. The link-up region will therefore be the limiting factor in determining emitter/base breakdown voltage.

4.2 Fabrication Studies

'This section details the process development of the physical ELOBJT-3 device structure. First, an investigation of materials for the CLSEG top cavity layer was performed to see if an all oxide CLSEG cavity was feasible. Next, the development of a suitable multi-layer trench etch was investigated.. CLSEG was then performed from a vertical seed (the sidewall of the intrinsic SEG growth) for the first time. Chemical mechanical polishing was investigated as a quick and reliable way around the faceting and non-uniform growth tendencies of both SEG and CLSEG. Finally, a simplified process was developed to more quickly and reliably fabricate the ELOBJT-3 physical structure.

4.2.1 CLSEG Cavity Etch and Top Layer Material

Schubert had considerable success in reliably fabricating uniformly thick, good quality, single crystal SOI films using the reported CLSEG process.[3] As shown in Figure 2.11, a layer of nitride approximately 1500 Å thick was used as a mechanical support for the thinner 1000 Å thick oxide which lined the inside of the CLSEG cavity. However, there are three significant differences between the reported CLSEG process and that needed for the ELOBJT-3 process as proposed in section 3.1.2. First, the cavity sacrificial layer would be etched out during the central SEG trench etch and the top cavity layer would subsequently be supported on only three sides during the central SEG growth as observed from Figure 4.5. Second, the top CLSEG cavity layer even after growth of SEG within

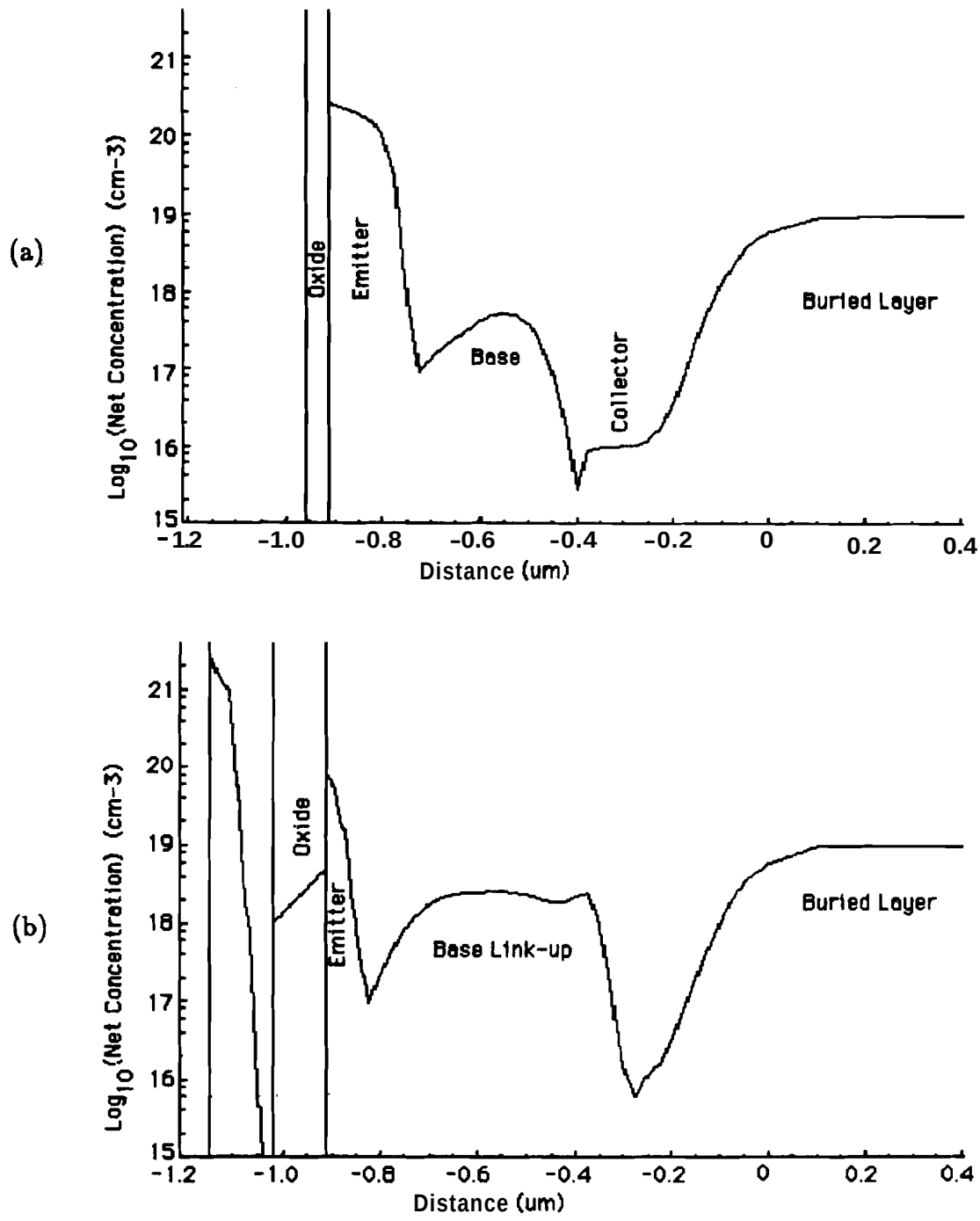


Figure 4.4. **Onedimensional plot of net doping concentration taken vertically through a line at (a) X=0.2 μm, and (b) X=0.45 μm in the final TSUPREM-4 structure file shown in Figure 4.3.**

the central trench would not be a continuous film from one side of the cavity to another. Finally, it was speculated that the top nitride layer might be eliminated if the underlying oxide was thickened.

The first step toward investigating these issues was the fabrication of a three level photomask set (JCM1) including various sized CLSEG structures. The baseline structure of Figure 4.5 shows the four parameters which were varied: SEG stripe width W,, CLSEG width to vias W_c, length of CLSEG parallel to the growth front L, and the size of the CLSEG vias. SEG width W_s was either 2, 4, or 6 pm, CLSEG width to vias W_c was varied from 4 to 9 in 1 μm increments, length of CLSEG parallel to the growth front L was either 10, 30, or 100 pm, and the sizes of the CLSEG vias were either 2x4 or 3x6 pm^2. The availability of a large number of different sized structures on the same mask allowed the investigation of many different effects and safeguarded against unknown limitations.

Logically, fabrication studies began with an investigation of the CLSEG cavity already established by Schubert. A layer of thermal oxide approximately 0.3 μm thick was grown on N-type (100) silicon wafers, upon which a 0.6 μm thick sacrificial polysilicon layer was deposited at 580° C and defined using JCM1-level #2. A 60 minute wet oxidation at 1000" C formed about 0.34 μm of polyoxide, leaving about 0.45 μm of polysilicon. Finally, a 0.15 μm LPCVD silicon nitride layer was deposited at 750" C over the entire top wafer surface. The central SEG trench was lithographically defined in the center of the cavity layer using the JCM.1-layer #1 mask. An RIE etch using Freon-115 (C_2ClF_5) at 750 watts in a DRY'TEK parallel plate reactor was used for 90 minutes to etch through the top cavity nitride/oxide, the cavity polysilicon, and partially through the bottom oxide. A scanning electron microscope (SEM) cross-section of the trench sidewall formed by the RIE is shown in Figure 4.6(a).

An isotropic R E polysilicon etch was envisioned in section 3.1.2 for removing the sacrificial cavity material. Sulfur hexafluoride (SF_6) was used in the R E reactor for 20 minutes at 500 watts power to etch the polysilicon layer back roughly 8 μm into the CLSEG cavity as shown in Figure 4.6(b). However, as can also be observed in the darker region surrounding the central trench, the SF_6 etched through the 1000 Å thick oxide in the trench bottom and isotropically etched a hole into the substrate. It was determined that SF_6 had an oxide etch rate of approximately 100 Å/min, and would therefore not be suitable for the

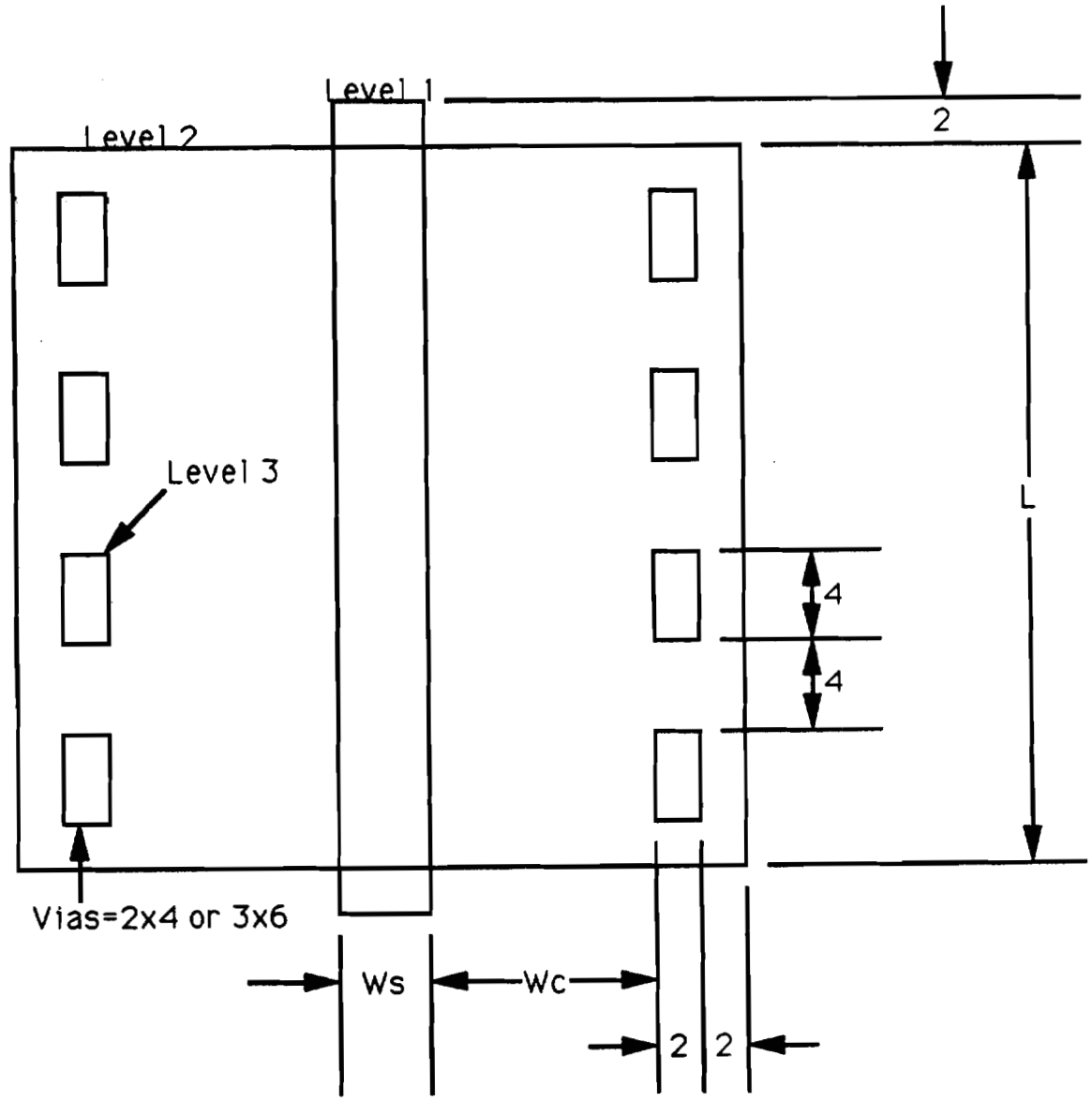


Figure 4.5. **Basic CLSEG structure from JCM1 photomask set showing the four parameters which were varied, SEG stripe width W_s, CLSEG width to vias W_c, length of CLSEG parallel to the growth front L, and the size of the CLSEG vias. All dimensions in μm.**

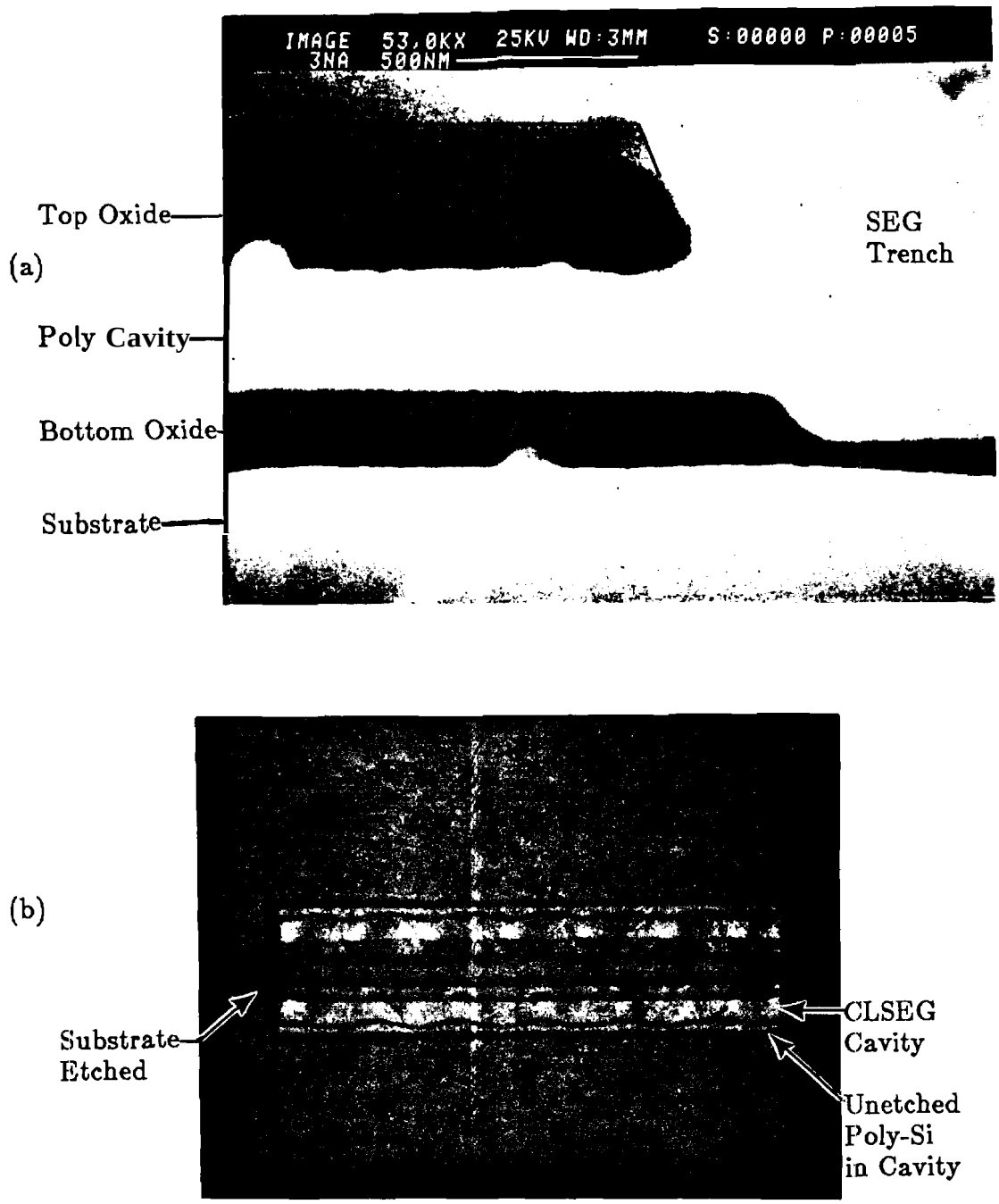


Figure 4.6. **Results of RIE etching the SEG trench and sacrificial cavity: (a) SEM micrograph of the sidewall cross-section of vertical trench formed in nitride/oxide/polysilicon/oxide stack by Freon-115 RIE etching, (b) top view optical photograph of 100 μm long CLSEG cavity following SF_6 etching to remove approximately 8pm of the sacrificial layer.**

sacrificial layer etch.

Although Schubert had successfully used the aqueous alkaline solution ethylenediamine ($NH_2(CH_2)_2NH_2$ or simply ED), to remove the polysilicon material, a safer alternative was desired. The purely inorganic KOH compound was chosen due to its relatively high etch selectivity of silicon to oxide (although not as great as ED), as well as being much safer and easier to use. [4]

Seidel states the following general reaction is responsible for the silicon etching,

$$Si + 2H_2O + 2OH^- \rightarrow Si(OH)_2O_2^{--} + 2H_2 \qquad (4.1)$$

The KOH solution is a very thin, non-viscous fluid (contrary to the rather thick ethylenediamine) and reportedly does not require stirring due to a very small diffusion dependence. Stirring on a magnetic hotplate was used however to maintain a constant temperature in the bath. Due to the less toxic nature of KOH, the bath was not covered and samples could be quickly removed from the solution and rinsed under a DI-water stream all within seconds affording precise control of the etching time. A 10 to 18 weight percent (w/o) KOH to DI mixture was used due to a Si/oxide etch selectivity of 1000 between 50 and 60 °C. At this temperature, the oxide etch rate was reported as 3-4 Å/min and silicon as 3000-4000 Å/min. KOH was then successfully used to remove about 8 μm of sacrificial cavity material in approximately 20 minutes. No problems with capillary action in the 8 μm deep by 0.5 μm thick cavities were encountered, even when terminating the etch early and re-starting it. In addition, the KOH solution did not affect the wafer masking surface in any way that increased spurious nucleation during selective epitaxy. This was determined with identical monitor wafers which did not receive any KOH etching and were inserted into SEG growths along with the KOH etched wafers.

The next task was to investigate the integrity of the top cavity layer. In figure 4.5(b), the optical micrograph shows a wave-like interference pattern in the remaining top cavity layer above where the sacrificial material had been removed. Cleaving the sample and observing the cross-section of a 1000 μm long device in the SEM showed a marked upward bend to the top cavity layer. However, it was uncertain whether this upward flare was inherent to the top cavity layer itself, or caused by the cross-sectioning process. Therefore, an unetched sample was cleaved and investigated before etching of the sacrificial layer. After about 8

minutes of 18 w/o KOH etching at 80°C, the sample showed the same upward bend indicating an inherent problem with the top cavity layer itself.

It was suspected that this upward bend was the result of having a combination nitride/oxide top layer. The coefficients of expansion of the two materials are different by about an order of magnitude, $4x10^{-6}/°C$ and $5x10^{-7}/°C$ for high-temperature nitride and thermally-grown oxide respectively.[5] As the high-temperature nitride layer is depositing on the oxide layer at the deposition temperature, mechanical equilibrium is maintained and there is no stress between the two layers. However, as the wafers are cooled to room temperature following nitride deposition, the different coefficients of expansion produce stress in the two layers. Because the nitride layer's coefficient is larger, it would want to shrink in size more than the underlying oxide layer. This produces a compressive stress in the oxide and an expansive stress in the nitride. But, as long as the underlying sacrificial layer is in place, all is constrained to follow the movement of the substrate. Finally, as the underlying sacrificial layer is removed, the layer bends upward till it finds a new equilibrium between the forces of the nitride and oxide.

High contrast SEM micrographs of the upward bending layer were extremely difficult to obtain due to intense electrical charging of the cantilevered oxide/nitride layer. However, viewing of the structures on the SEM screen was possiible because of the much higher scan rate than that used by the camera. Therefore, edge lines as seen on the console screen have been added to SEM micrograph of Figure 4.7 to aid the reader. It is important to note that the cross-sectioned structure was about 1000 μm in length, effectively making the top layer supported on only one side. In a real device, there would be support on all three sides except the edge along the central SEG trench and hence upward bending might not be a problem. However, some amount of bowing similar to figure 4.5(b) was observed in even the smallest structures (10 μm long x 8 μm wide) from a top view without cleaving through the structures. Although the bending might be minimized in ultra-small scaled devices, inherent stresses; in and around the device would still be present.

A new set of wafers was started which did not include the nitride layer and the top oxide thickness was increased to 0.42 pm. This time, no wave-like patterns were observed after removing the sacrificial layer, and the SEM photograph of Figure 4.8(a) shows an almost perfectly uniform cavity. However, Figure 4.8(b)

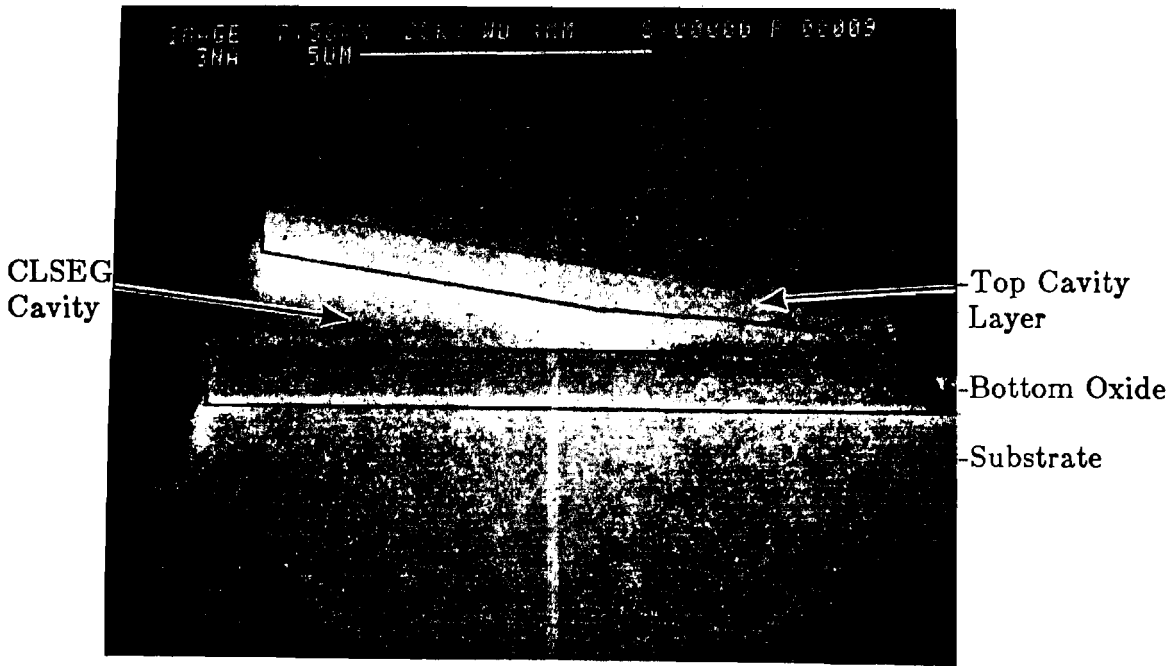
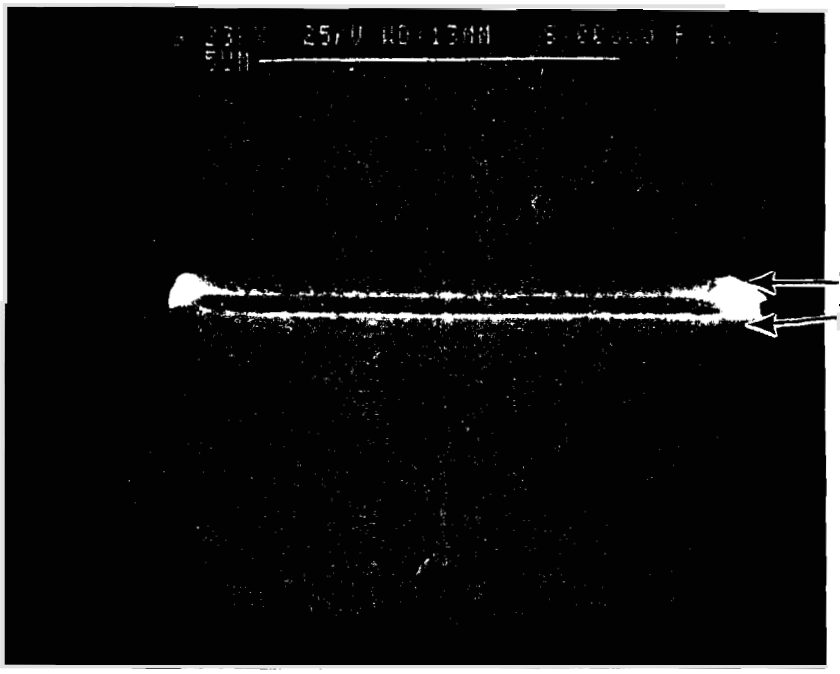


Figure 4.7. **SEM** micrograph of the upward bending top cavity layer after the underlying sacrificial layer had been removed.

shows an optical top view of a 100 μm long cavity which has had its sacrificial layer removed and a 20 second BHF dip to simulate the process needed before **SEG** growth within the trench. The top oxide cavity layer has cracked off and is missing on both sides of both ends of the structure. Although the all oxide top layer seems to fix the bowing problems caused by the nitride layer, it does not seem to be well enough **affixed** at its edges to support itself.

It was theorized that the poor connection at the cavity edge was due to the growth of the top oxide solely from the sacrificial polysilicon layer. As seen in Figure **4.8(a),** it appears there is a dividing line between the field oxide to the left and below the cavity, and the point where the polyoxide top cavity layer attaches to it. Therefore, a set of four wafers were fabricated which were identical except for their top cavity layers. The first group had a polyoxide of **0.4** μm grown completely from the polysilicon layer. The second group had a 0.13 μm thick LPCVD polysilicon layer deposited over the already defined polysilicon sacrificial layer. An oxidation was then performed to consume all of the top polysilicon and a small amount of the sacrificial layer to produce a total of 0.4 μm of oxide. This

(a)



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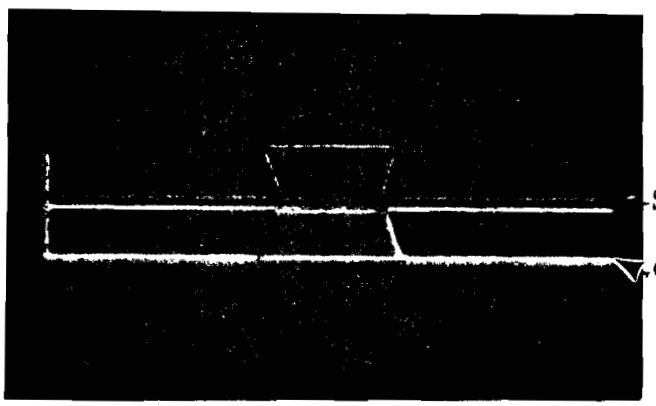

Figure 4.8. Results of all oxide top cavity layer: (a SEM cross-section of CLSEG cavity after sacrificial layer remova , (b) optical top view of top cavity layer broken away at ends of cavity.

combined 0.4 μm thick top cavity layer held up perfectly even through a 15 second BHF dip and 14 minute SEG growth as shown in Figure 4.9. The first

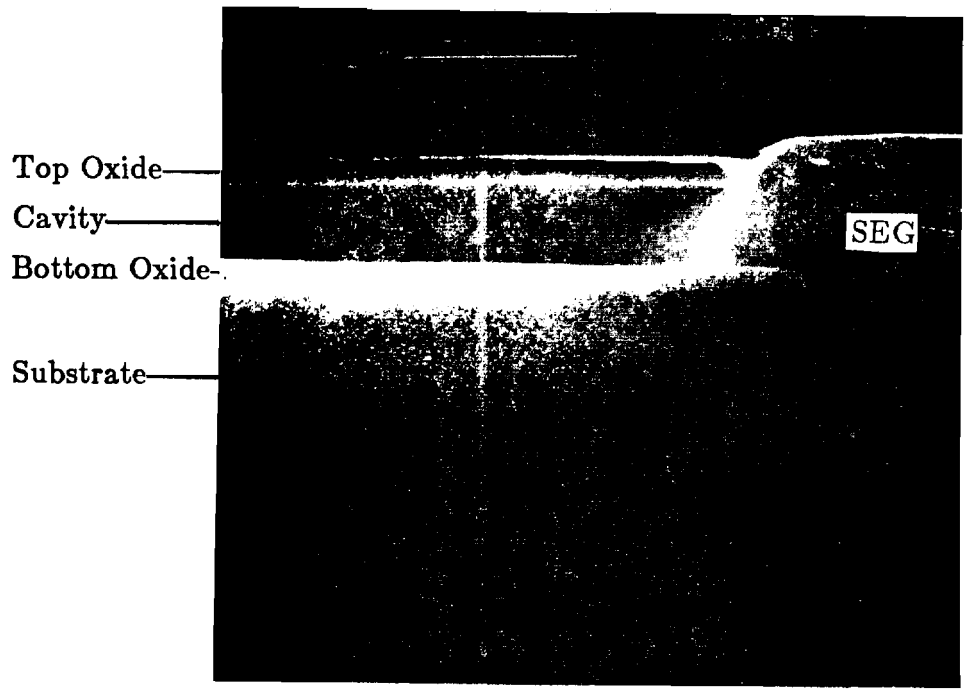

Figure 4.9. SEM cross-section of SEG growth next to oxide top cavity layer formed using continuous layer of oxidized LPCVD polysilicon.

group of wafers, similar to previous runs, showed breakaway of portions of the top cavity layer following sacrificial layer removal.

The cavity etch and optimum top layer material were therefore established. A successful technique for safely and easily etching the cavity with an aqueous KOH solution was also demonstrated. In addition, a thicker oxide layer which includes a continuous layer of oxidized LPCVD polysilicon was shown to adequately support itself even with its underlying sacrificial cavity material and one of its supporting sides removed. Also, the cantilevered top oxide layer withstood the rigors of normal wafer processing and a 970° C epitaxy growth. However, the question regarding CLSEG growth within the newly designed cavity still remained.

CLSEG was therefore attempted using one of the previously processed wafers. The wafer was first oxidized to protect the top of the already grown SEG

from further growth. Then, via holes were patterned and etched using RIE, and a quick 10 second BHF dip performed prior to a 50 minute selective epitaxy growth. The results showed no CLSEG grown within the cavity due to an unexpectecl oxide layer covering the SEG sidewall within the cavity. Longer BHF dips prior to growth could not be used without degrading the already thin seal between the top cavity oxide layer and the central SEG growth. It was believed that during the capping oxide growth, oxygen reactants diffused through or past the thin, sharp top oxide edge and an oxide was grown on the SEG sidewall inside the CLSEG cavity. The inherent problem seemed to be the non-vertical RIE etch being used to fabricate the central SEG trench. As observed in Figure 4.9, the edge of the top cavity layer is set back roughly 0.8 μm from the edge of the bottom oxide. If a more vertical trench etch could be found, the SEG would make a better seal with the top cavity layer and prevent inadvertent oxidation of the SEG sidewall within the cavity.

4.2.2 Development of Multi-Layer Trench Etch

Indeed it was recognized earlier by Liaw et al. that an almost perfectly vertical layered sidewall was needed before SEG growth to prevent formation of V-grooves at the SEG/sidewall edge.[6] In order to obtain a more vertical trench etch, two factors needed improvement. First, as no masking layer is completely impervious to RIE etching, the vertical profile of the masking photoresist itself plays a critical role in the final etched profile. Second, even if a perfectly square photoresist edge was obtained, a straight sidewall would not be etched without the proper RIE process. The photoresist process was investigated first.

4.2.2.1 Improvement of Photoresist Profile

The manufacturer suggested photoresist (PR) recipe[7] had long been used on faith with decent results for large resolution work. However, an investigation of the sidewall profile revealed shocking results, an approximate 40° slope as seen in Figure 4.10. Therefore, a detailed set of experiments were designed to develop a process sequence for obtaining the optimum photoresist profile, i.e. a square 90° edge.

The tests were arranged sequentially to individually optimize each process parameter due to their fairly dependent nature. The novolac resin based positive resist, AZ1350J, was chosen as the first constraint due to its simple processability

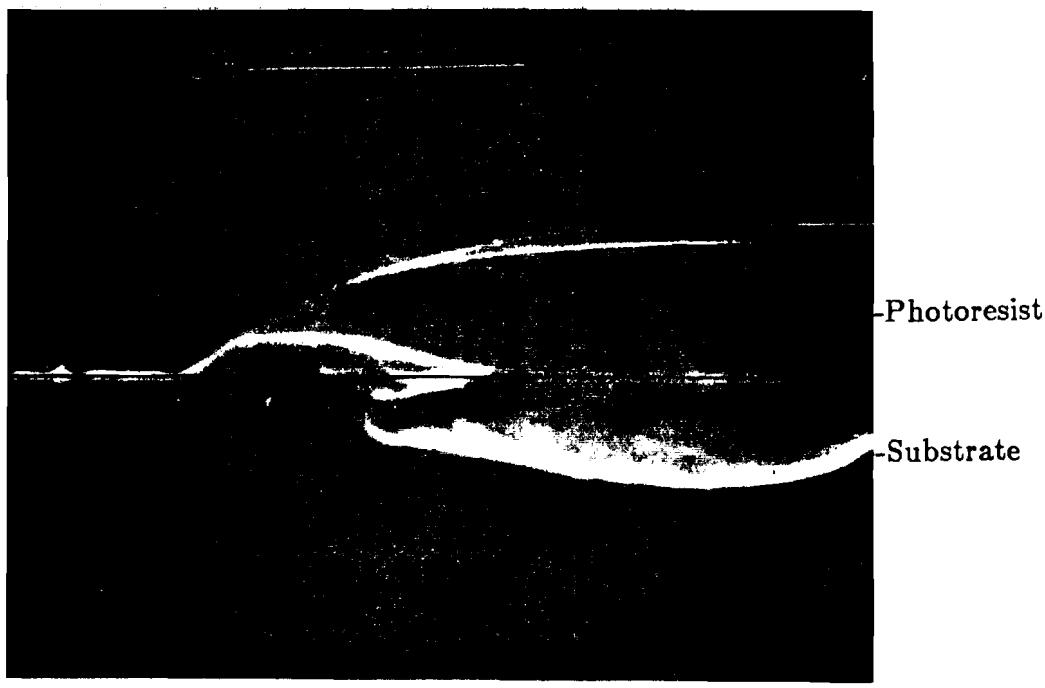

Figure 4.10. SEM cross-section of AZ1350J photoresist sidewall profile processed using standard parameters.

and reliable results. Second, a spin speed of 4000 RPM for 30 seconds providing a 1.72 μm thick layer was chosen to provide enough protection during RIE etching. A vacuum chamber, contact mask aligner with chrome on glass photoplates was chosen as the third constraint due to its relatively good performance, yet ease of usage compared to electron beam writing. An excellent reference on virtually all phases of photoresist processing provided an extensive background as well as practical recipes.[8]

Perhaps the most important parameter controlling sidewall PR profile is the prebake heat treatment before W exposure. Five different temperatures were investigated, 90, 100, 110, 120, and 140' C. Since the apparent photospeed is very sensitive to the prebake temperature, two different exposure times (energies) were tried for each temperature setting. All other parameters were left unchanged from the previous method. The results are listed in Table 4.2 where each sample was cleaved without postbaking and the sidewall profile investigated in the SEM. Apparently prebake temperatures above 120 ° C permanently link the

Table 4.2. Effect of Prebake Temperature on Photoresist Sidewall Profile.

Wafer#	Prebake Temp (°C)	Exposure Time (s) @23mW/cm^2	Results
1	90	5	60°, square
2	90	7.5	60°, slightly rounded
3	100	10	75°, square
4	100	25	70°, rounded
5	110	10	80°, square
6	110	30	85°, square
7	120	20	no image
8	120	60	no image
9	140	30	no image
10	140	90	no image

novolac resist so that photosensitivity is completely lost. Of the three temperatures that remain, 110°C provided the most vertical sidewall. This established the optimum prebake temperature at 110°C.

Next, the optimum exposure time (energy) was determined for the prebake temperature of 110°C. Four wafers were processed with exposure times of 15, 20, 25, and 30 seconds using the standard 23 mW/cm^2 W lamp intensity. The results after development with no postbake are listed in Table 4.3. An exposure time of 20 seconds at 23 mW/cm^2 was therefore chosen to obtain the best sidewall angle and maintain the drawn mask dimensions.

From here, two more experiments were run investigating the effects of high-temperature post-exposure bake (HTPEB), and developer concentration. A HTIPEB at 120°C for 2 minutes was shown to provide no advantage in sidewall profile. Also, the previously used developer concentration of 1:1 DI:AZ was shown to provide the best results compared to 1:2, 2:1, and 1:4 dilutions.

Finally, the effect of postbake temperature on sidewall profile was investigated. Elliott [8] stated that novolac based photoresists start to flow significantly around 110°C. This effect was verified by subjecting wafer #14 from Table 4.3

Table 4.3. Effect of Exposure Time on Photoresist Sidewall Profile. Prebake Temperature= 110 ° C.

Wafer#	Exposure Time (s) @23mW/cm^2	Angle	Lateral Size (pm) (2μm mask)
11	15	80 °	1.83
12	20	85 °	2.08
13	25	85 °	2.40
14	30	85 °	2.44

to a 30 minute postbake at 110 ° C. The sidewall angle changed from 85" to roughly 70" and the top edge rounded significantly. The postbake step is commonly used to remove any water added by the development step from the PR layer, and to increase adhesion to the substrate for subsequent wet chemical processing. However, it was determined that no postbake step was necessary when RIE etching, as opposed to wet etching, would be used and definitely not needed when the prebake was done at an elevated temperature such as 110 ° C.

An optimum photoresist process recipe was developed for producing almost perfectly vertical sidewall profiles. Following bakeout, application of HMDS adhesion promoter, and resist spinning at 4000 RPM for 30 seconds, a 110" C prebake was used with a 20 second W exposure. The image was developed in approximately 40 seconds using a 1:1 AZ:DI developer concentration. No postbake was performed as long as RIE etching was being used.

4.2.2.2 Investigation of RIE Process

Before the photoresist development project was finished, several attempts were made to obtain a vertical RIE trench etch using the existing DRYTEK DRIE-100 reactor and gases, Freon-115 (C_2ClF_5) and Freon-116 (C_2F_6). The Freon-115 plasma produces chlorine ions which are good etchants of silicon material, either single-crystalline or poly-crystalline. The plasma reaction is classified as ion-enhanced energetic or energy-driven anisotropic due to the need for the energetic bombardment to induce etching of the desired material. The DRYTEK reactor plate spacings and pump system were designed for using

Freon-115 to etch polysilicon very quickly (about 350 Å/min) and vertically.

Alternatively, Freon-116 with the addition of various other gases, reportedly provides a very anisotropic oxide etch.[9] However, the reactor's plate spacing and pumping system were not well suited to oxide etching with Freon-116. The Freon-116 etch is classified as ion-enhanced inhibitor or inhibitor driven anisotropic. As the fluorine based species are etching the oxide surface, unsaturated fluorocarbon species (CF_2) combine to form thin polymer layers on the vertical etched sidewall as it forms. This polymer inhibitor prevents the RIE's attack of the sidewall but not the horizontal surfaces.[10]

Logic suggested each gas should properly be used to etch through the material to which it was best suited. Therefore, an attempt was made to etch through the oxide/poly/oxide stack using a sequence of Freon-116, 115, 116 etching. This attempt met with considerable failure as observed in Figure 4.11. The 60 minutes of Freon-116 etching at 1000 watts produced a fairly vertical sidewall in the top oxide layer. However, Freon-116, because of its high propensity to polymerize,[11,12] formed an unusual tooth-shaped polymer deposit as it reached the polysilicon sacrificial layer. This polymer coating, approximately 0.5 μm wide, then prevented the 10 minute Freon-115 etch from attacking the polysilicon layer near the sidewall. This produced a 0.5 μm step in the sidewall profile. The final Freon-116 etch was only able to remove the bottom oxide where the sacrificial polysilicon layer had been opened.

Many techniques were attempted for removal of the tooth-shaped residue[13] including various combinations of the following, O_2 plasma, O_2 RIE, 400°C O_2 furnace burn,[12] and piranha and aqua regia wet acid cleans. However, only a one minute BHF etch would remove the deposit, indicating it was probably some type of C/F/Si/O mixture. The tooth-shape of the structure was probably caused by off-angle ion bombardment and reflection from the sidewall similar to that observed in substrate trenching during RIE.[14]

With the more vertical photoresist profile under control, Freon-116 was abandoned and a return was made to Freon-115 etching. The inherent problem was the relatively slow oxide etch rate with Freon-115 at 750 watts in this reactor configuration (about 70 Å/min), coupled with the non-negligible isotropic etch rate of the 1350 photoresist. Figure 4.12 illustrates the etching problem. As the top oxide layer is being etched at its relatively slow pace of 70 Å/min, the

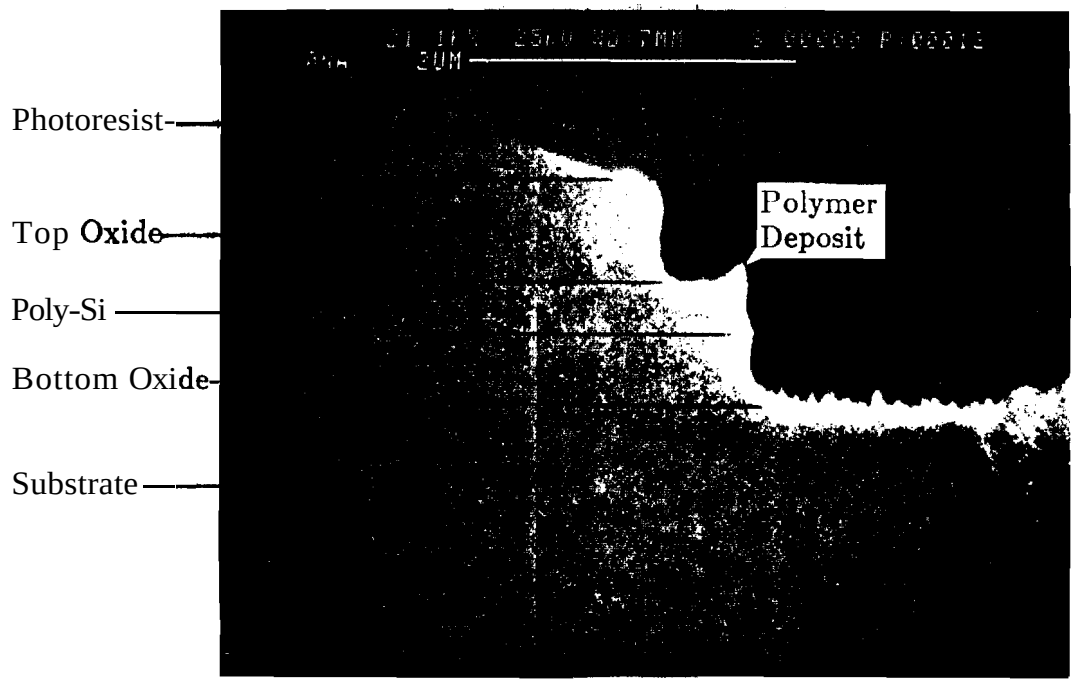

Figure 4.11. SEM cross-section of result of Freon-116, 115, 116 etching of oxide/poly/oxide stack.

photoresist recedes isotropically due to the action of the RIE plasma. This produces the slanted etch through the top cavity layer as seen in Figure 4.12(a). Next, the quick and efficient etch (about 10 minutes) through the sacrificial polysilicon layer leaves a very vertical profile because the photoresist does not have much time to recede (see Figure 4.12(b)). Finally, similar to the top layer, a long time is needed to etch through the bottom oxide layer. Consequently, the photoresist again recedes, and the entire profile is pushed back as the bottom layer is etched (see Figure 4.12(c)).

A reference [8] stated that for increased resistance to R E attack of 1350J photoresist, the bombarding voltage in the R E reactor should be limited to less than 700 volts. The bombarding voltage is controllable through the power setting of the reactor. Although reducing the power of the etch decreases the oxide etch rate even further, if the 1350J etch rate is reduced proportionally more, there might be an improvement in the sidewall profile. Therefore, a 180 minute

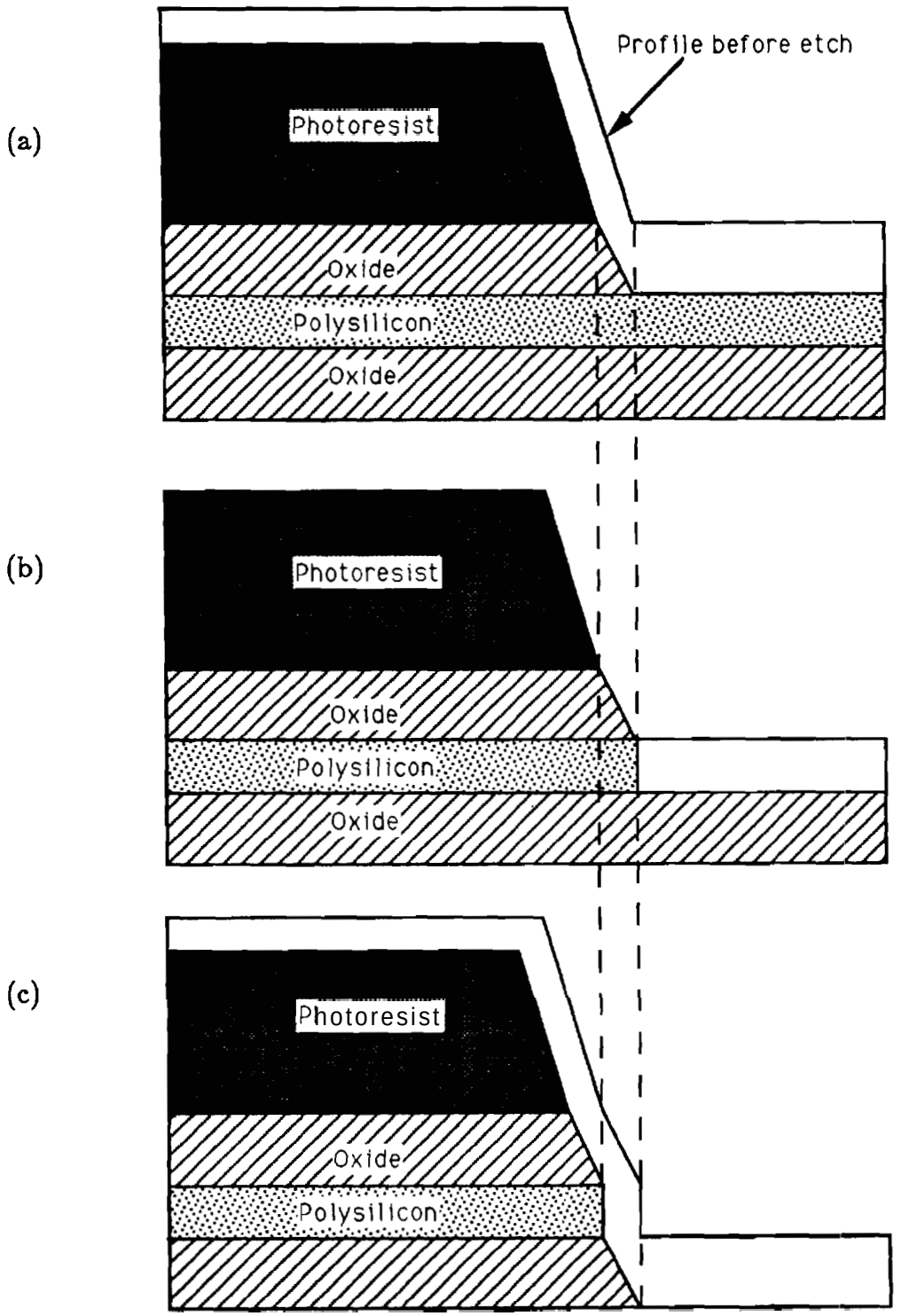

Figure 4.12. Problem encountered in etching of oxide/poly/oxide stack when RIE plasma is isotropically etching photoresist mask.

Freon-115 etch was attempted at 500 watts power instead of the standard 750 watts. The sidewall profile of Figure 4.13(a) is a marked improvement over the

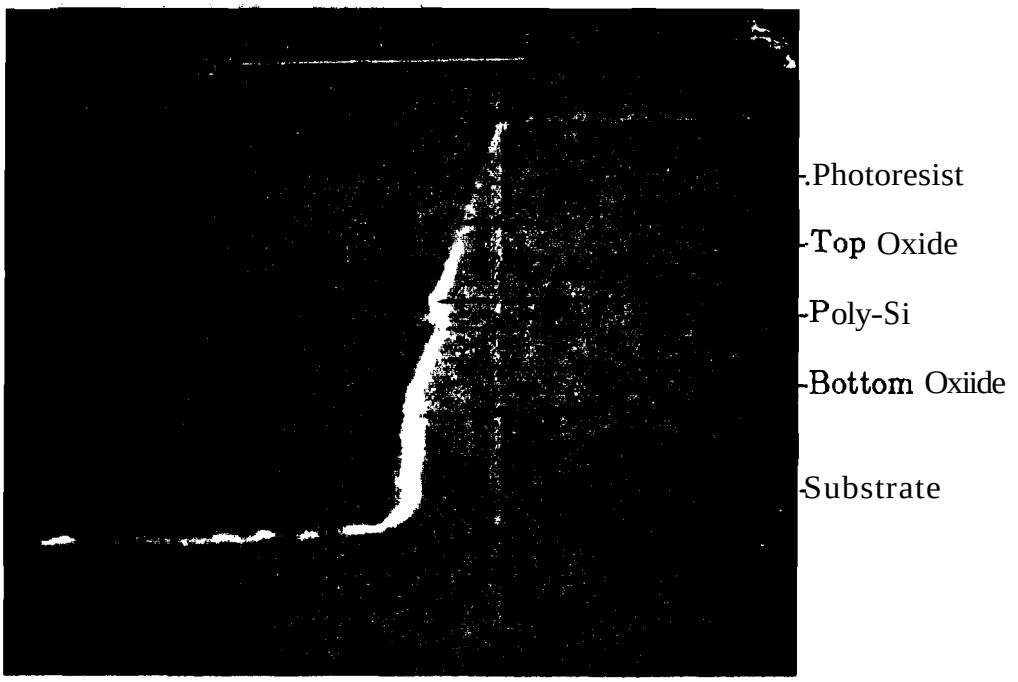

Figure 4.13. SEM cross-section showing the result of Freon-115 etching of the oxide/poly/oxide stack at 500 watts power.

highly sloped profile of Figure 4.6(a). However, etch uniformity at the lower power setting was markedly degraded. By the time the bottom of the trench was reached in the center of the wafer, other areas still showed roughly 2000 Å of oxide remaining. In addition, the various sized seed holes etched at different rates making the determination of etch completion difficult. However, although the etch was not optimum, it would have to suffice until a better etch could be developed.

4.2.2.3 Development of Sidewall Polyoxide

During preliminary attempts at CLSEG growth, it was decided that the proposed process sequence of section 3.1.2 would be too difficult to process and a new sequence should be investigated. The problems stemmed from oxide growth on the SEG sidewall inside the cavity and being able to reliably grow CLSEG

material. In addition, when the CLSEG via holes are being cut through the top oxide into the empty cavity, there is no etch stop for self-termination of the etch. For these reasons, the process was changed to leave the polysilicon sacrificial material inside the cavity until just prior to the CLSEG growth.

This new process necessitated the development of a sidewall polyoxide to prevent nucleation of SEG material on the exposed polysilicon in the trench. The new trench etch began with the previously developed 500 watt Freon-115 RIE for 200 minutes to etch through the tri-level oxide/poly/oxide stack. After stripping the photoresist, a 30 minute 1000°C dry oxidation produced about 400 Å of oxide on the substrate at the bottom of the trench and perhaps 500 Å of polyoxide on the exposed polysilicon. Another 5 minute Freon-115 RIE was used to remove most of the oxide at the bottom of the trench, without significantly affecting the polyoxide on the sidewall. SEG was then grown within the trench and a 0.15 μm capping oxide was grown on the surface of the SEG as seen in Figure 4.14. The SEG apparently made a good seal along the top oxide edge. However, the new trench etch technique did not work correctly across the entire wafer. Most structures showed highly defective material nucleated off the polysilicon at the edges of the trench.

A set of test wafers were subsequently used to find the best technique for forming a reliable sidewall oxide over the polysilicon to prevent nucleation. They were all identically RIE etched, but received different dry oxidations of 30, 50, and 75 minutes at 1000°C as listed in Table 4.4. The 75 minute growth with 15 minute RIE and 10 second BHF dip prior to growth produced the best SEG results. This new technique was adopted for producing good quality SEG within the multilayer trench. CLSEG could now be grown from the vertical side of the first, SEG within the cavity.

4.2.3 CLSEG Growth From a Vertical Seed

There was one major reservation in changing the trench etch technique to leave the sacrificial layer within the cavity during SEG growth. The sidewall of the SEG would be grown past the somewhat rough polyoxide layer as the SEG filled the trench. This perhaps rough surfaced SEG sidewall would then be the seed for CLSEG growth. The ELOBJT-3 device does not depend heavily upon perfect single-crystal CLSEG growth because no junctions are located within the

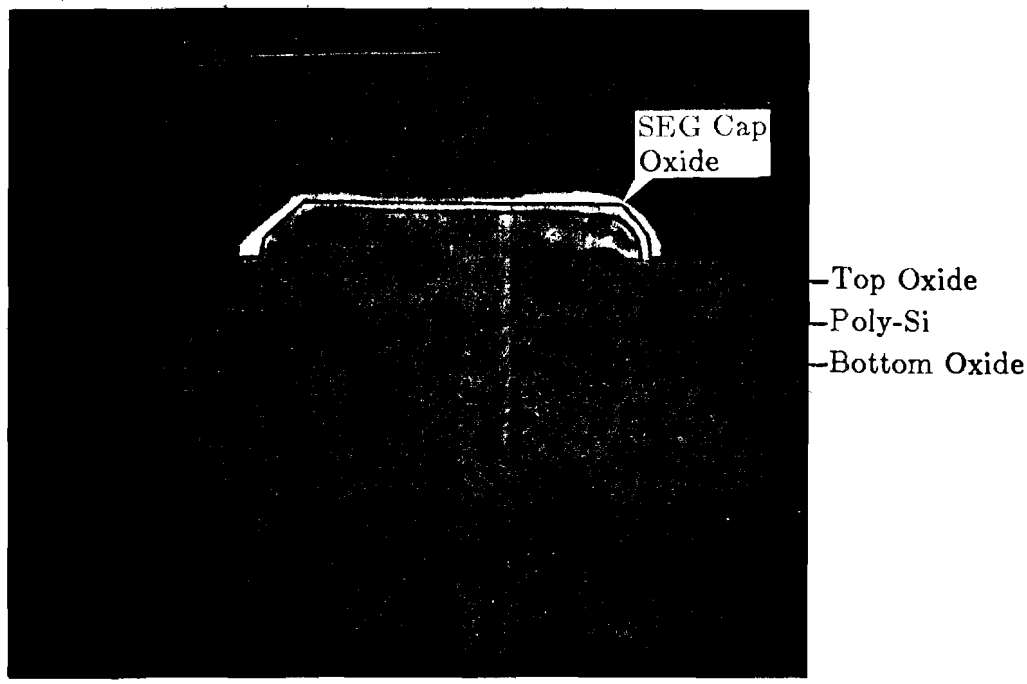

Figure **4.14.** SEM cross-section showing oxide-capped SEG grown within the trench formed using the new etch technique.

CLSEG itself. However, it does depend upon reasonably single-crystal CLSEG material for improvement of carrier mobility versus similar poly-contacted devices.

Wafer **#1** from Table **4.4** was patterned and via holes were etched in the top cavity oxide using BHF. An **18 w/o KOH** solution was used at 80°C for removing the sacrificial polysilicon material from inside the cavity. A 20 second BHF dip was used to clear the protective oxide off the SEG sidewall inside the cavity just prior to the growth. **115** minutes of CLSEG growth was then performed using the standard SEG parameters of 970°C and 40 Torr. The first successful CLSEG growth from a vertical seed is shown in Figure **4.15.** Although good CLSEG was grown within the cavity, unwanted growth was obtained on the top surface of the wafer, apparently nucleating at the edge between the central SEG

Table 4.4. Results of SEG Growth Within Trenches Which Received Different Sidewall Oxide Treatments.

Wafer#	Time (s) @1000 ° C	SUPREM3 Thick (Å)	RIE time @500W (s)	BHF dip time (s)	SEG Results
1	30	400	5	10	nucleation
3	50	550	10	10	some nucleation
			10	20	nucleation
2	75	700	15	10	no nucleation
3			15	20	nucleation

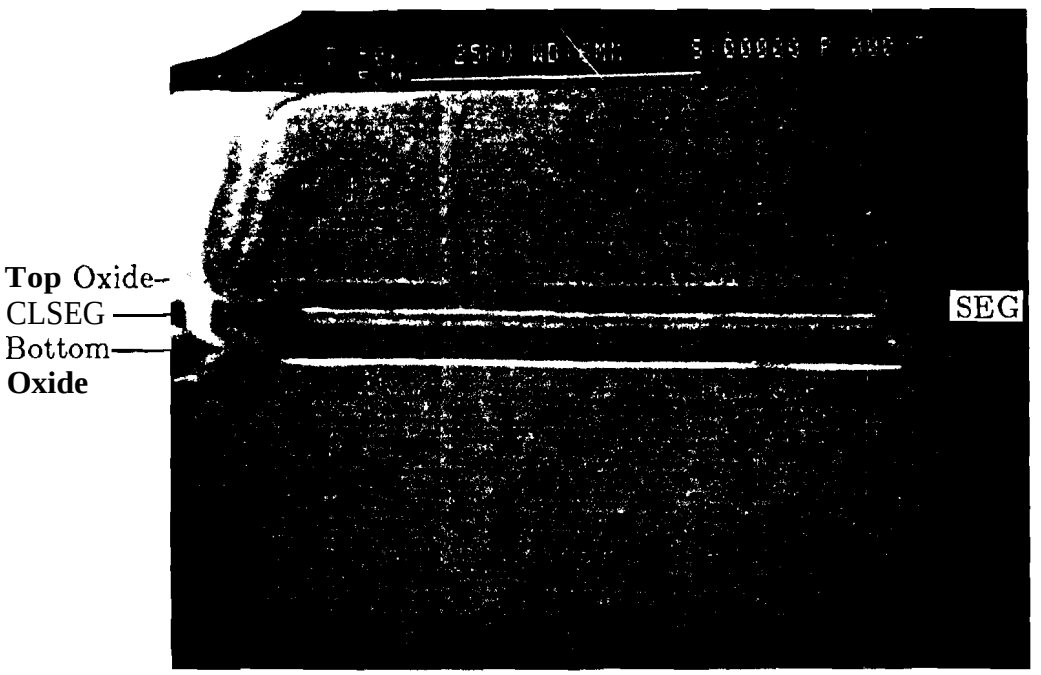

Figure 4.15. SEM cross-section of approximately 10 μm of laterally grown CLSEG seeded from a vertical SEG sidewall.

and the top cavity oxide. In this wafer, the SEG had been grown out of the multilayer trench and over the edge of the top oxide layer approximately 0.5 μm as shown in Figure 4.14. Therefore, the nucleation was presumably caused by micro-cracks at the SEG/top oxide interface due to thermal expansion during the SEG growth. Silicon nucleates were then able to grow from the SEG material at the bottom of these extremely small fissure cracks. A thicker capping oxide was used to correct this problem in later runs.

Another problem, was the non-planar surface created by the SEG overgrowth out of the central trench preventing fabrication of the transistor's intrinsic base and emitter regions. However, a new technology was emerging which showed promise for alleviating the growth uniformity and faceting problems of selective epitaxy.

4.2.4 The Nice Aspects of Chemical Mechanical Polishing

Chemical mechanical polishing (CMP) was added to the ELOBJT-3 process because of its ability to remove any non-uniformities of growth in both the SEG and CLSEG steps. Immediately following the central SEG growth, CMP was used to remove the excess material grown out of the trench and leave a smooth SEG surface planar with the top cavity layer. The SEG capping oxide was then grown, and the CLSEG step was performed. Any excess CLSEG growth out of the vias was polished back with a second CMP step. Typically, CMP was performed on a Buehler grinder with a Rodel type Suba H-1 12" pad, with a polish pad speed of 150 RPM, 15 lbs. force, and a head rotation of 30 RPM. The slurry used was a 15:1 mixture of DI:coloidal silicon compound (NALCO#2350). Following the polish, no striations or defects were identified using Nomarski spectroscopy in any of the CMP sessions performed.

Some useful facts regarding CMP were identified. Silicon is relatively soft and will etch quickly during CMP especially if the regions to be etched are raised up above the field level. However, if a bad SEG growth step produces silicon nucleation on more than 30-40% of the field, CMP will be ineffective in removing it. Also, oxide is a good etch stop material for the field, but it will be etched by CMP if it lies above the field surface. However, silicon nitride is very hard and makes an excellent etch stop material regardless of its level above or even with the field surface.

An example of CMP used to remove approximately 3 μm of excess ELO overgrowth from within a 40 x 44 pm^2 trench is shown in Figure 4.16. After the first two minutes of etching, the outline of the trench can be seen through the transparent SEG material in Figure 4.16(a). After another 2 minutes of etching, the overgrown material is very thin and the Nomarski spectroscopy highlights many dislocation defects in the overgrown material which seem to have propagated from the top edge of the trench in Figure 4.16(b). Finally, Figure 4.16(c) shows the smooth, planar surface of the SEG reduced to the level of the surrounding top cavity material with the ELO completely removed.

4.2.5 Final Self-Aligned Process

Even after several runs, there was still considerable difficulty in trying to obtain growth of SEG within the central trench without nucleating on the polysilicon in the sidewall. The sidewall polyoxide could not be thiclkened without requiring a longer BHF etch to remove the oxide before CLSEG. In addition, the very non-uniform etching results obtained with the 500 watt Freon-115 RIE produced wafers where only a few die were useful. Hence, a simpler, more reliable technique was necessary for etching the central SEG trench.

It was discovered that sulfur hexafluoride (SF_6) RIE produced a very quick and anisotropic etch through nitride material.[15] Also, if nitride was used for the top cavity layer, aqueous BHF could be used to etch the bottom oxide without harming the top cavity layer. Although an ultimate design would probably use oxide to obviate the need for nitride, due to the limitations of available etching equipment, nitride was added as the principal top cavity layer material because of its a'bility to be anisotropically etched with our RIE equipment.

The final ELOBJT-3 process sequence run sheet is listed in Appendix C. After growth of the 0.5 μm bottom/field oxide, the cavity amorphous silicon was deposited at 550 ° C to provide as smooth a surface as possible when recrystallized into polysilicon. The α-Si layer was defined and a thin 700 Å thermal oxide grown over the sacrificial layer. A blanket LPCVD nitride was then deposited at 800" C to a thickness of 0.35 pm, just below the thickness where stress cracking occurs. The central SEG trench was easily etched by using a sequence of SF_6 RIE, BHF dip, Freon-115 RIE, and BHF to cut through the nitride, thin oxide, polysilicon, and bottom oxide layers respectively. The fact that made the process

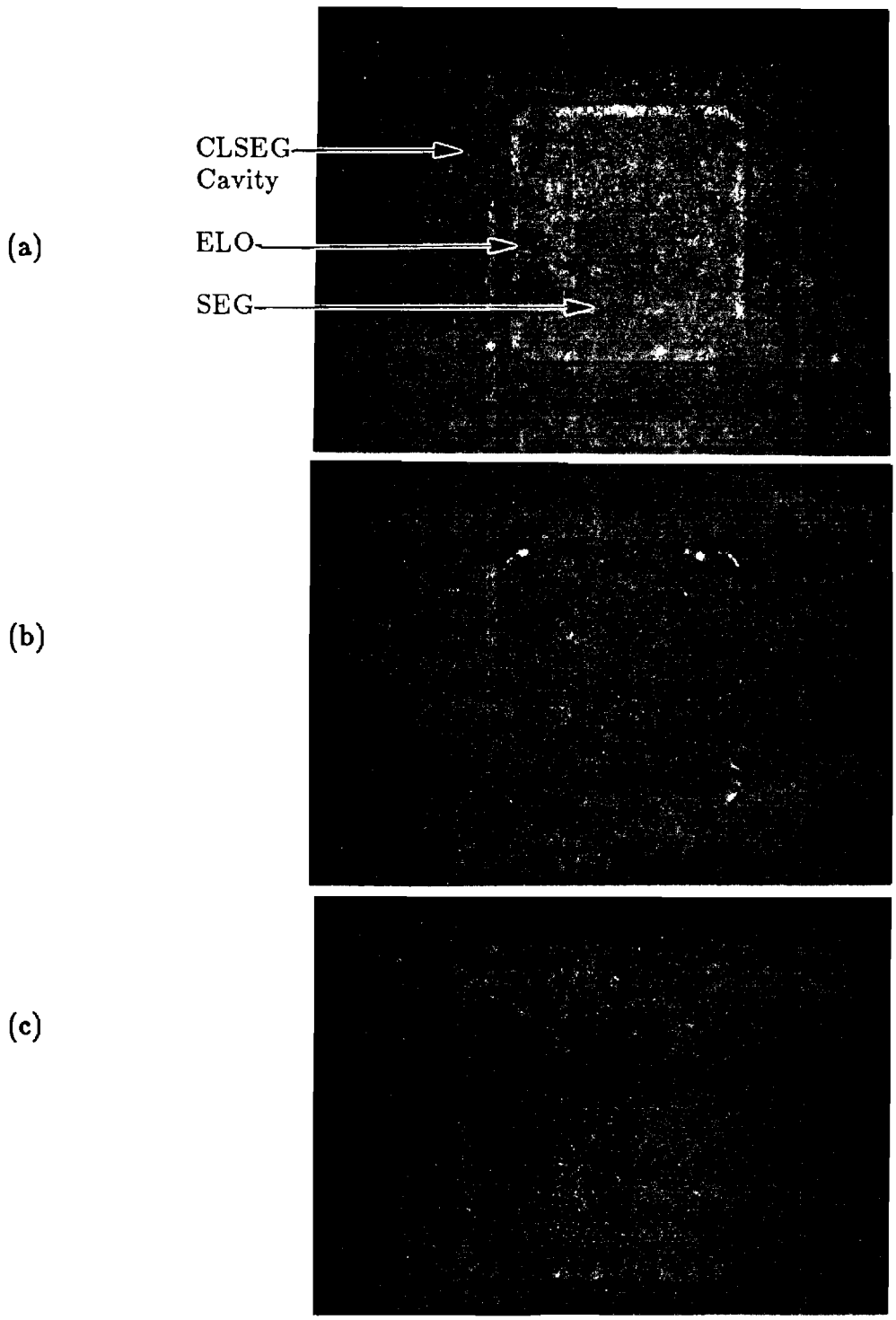

Figure 4.10. Optical micrographs of CMP performed on 40 x 44 μm^2 SEG growth: (a) after 2 minutes of etching, (b) after 4 minutes of etching, and (c) after 6 minutes of etching.

more uniform and controllable was that each of the four etches was selective over the next material as shown in Table 4.5. A 900° C wet oxidation for 30 minutes

Table 4.5. Etch Characteristics of the Four Etches Used to Form the SEG Trench.

Etchant	Target Matl -rate (Å/min)	Etch Stop Matl - rate (Å/min)	Selectivity
SF_6 RIE	nitride - 500	oxide - 100	5
BHF	oxide - 1000	polysilicon - $\cong 0$	∞
Freon-115 RIE	polysilicon - 350	oxide - 70	5
BHF	oxide - 1000	silicon - $\cong 0$	∞

was performed to grow the 700 Å sidewall oxide without appreciably recrystallizing the CLSEG cavity polysilicon. Next, a 12 minute Freon-115 RIE at 500 watts power removed most of the oxide at the bottom of the trench without appreciably etching the protective polyoxide on the sidewall. A quick 15 second BHF dip removed the rest of the oxide and prepared the wafer for SEG growth. The sidewall profile produced by this new etch sequence is shown in Figure 4.17.

During one of the CLSEG growths, an unusual nucleation phenomenon was observed. In the first group of wafers, the CLSEG via holes were etched with SF_6 RIE, and the standard KOH etch was used to remove the sacrificial polysilicon layer. The CLSEG growth step produced nucleation at each via hole which sealed off the hole and prevented further CLSEG from reaching the via holes. However, one wafer was subjected to a 15 minute dry oxidation at 900 ° C following the SF_6 via hole etch, and processed identically otherwise. This wafer showed no nucleation at all around the via holes and CLSEG growth occurred perfectly, emerging from the via holes as shown in Figure 4.18(a) and (b).

It is thought that the as-deposited silicon nitride has many dangling silicon bonds which are natural nucleation points during SEG. However, the nitride field surface usually does not nucleate because it is exposed to high-temiperature oxidations before SEG growth which passivate any dangling silicon bonds on the nitride surface. Upon RIE etching the via holes, dangling silicon bonds are once

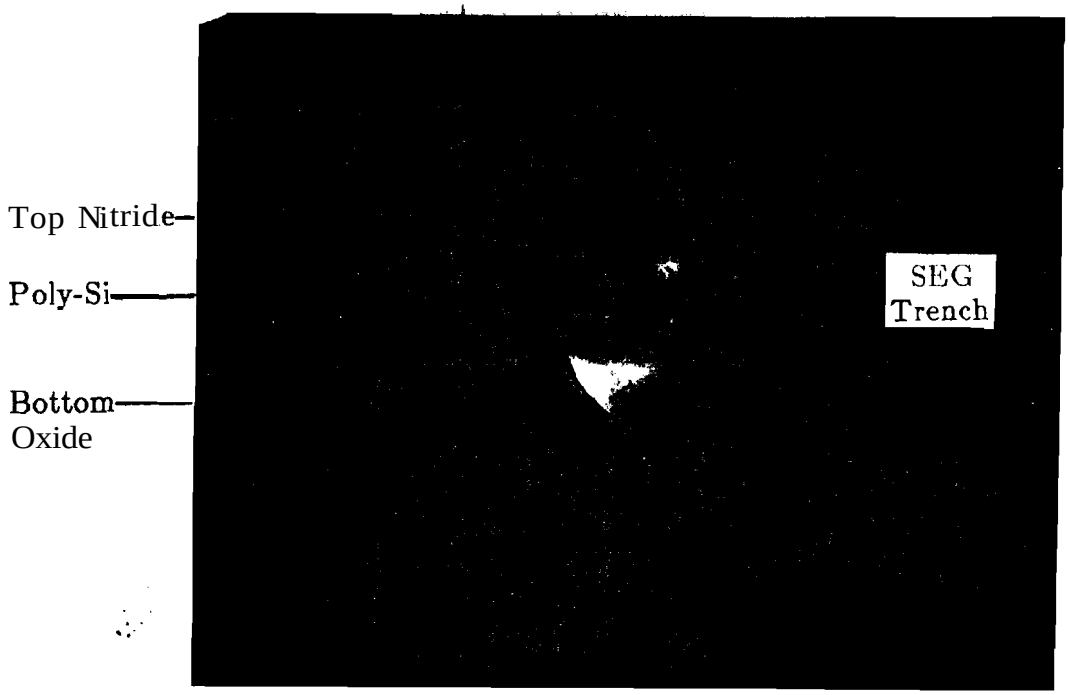

Figure 4.17. SEM cross-section of one side of the SEG trench sidewall produced by the final process sequence.

again exposed for nucleation unless another passivation is performed before CLSEG growth. The final ELOBJT-3 process for obtaining the physical device structure produced good quality, uniform SEG and CLSEG growths without heavy nucleation. Self-aligned PNP devices were then produced with these structures and their results detailed in Chapter 5.

4.2.6 Simplified ELOBJT-3 Process

It had been found that a greater number of processing steps leading up to an SEG growth led to greater nucleation and defects incorporated into the grown material. Therefore, although the previously described process produced the desired structure for fabrication of the self-aligned PNP devices, a quicker, easier process was necessary with fewer processing steps before the first selective epitaxy growth. This would theoretically lead to higher quality SEG and better operation of the intrinsic device regions.

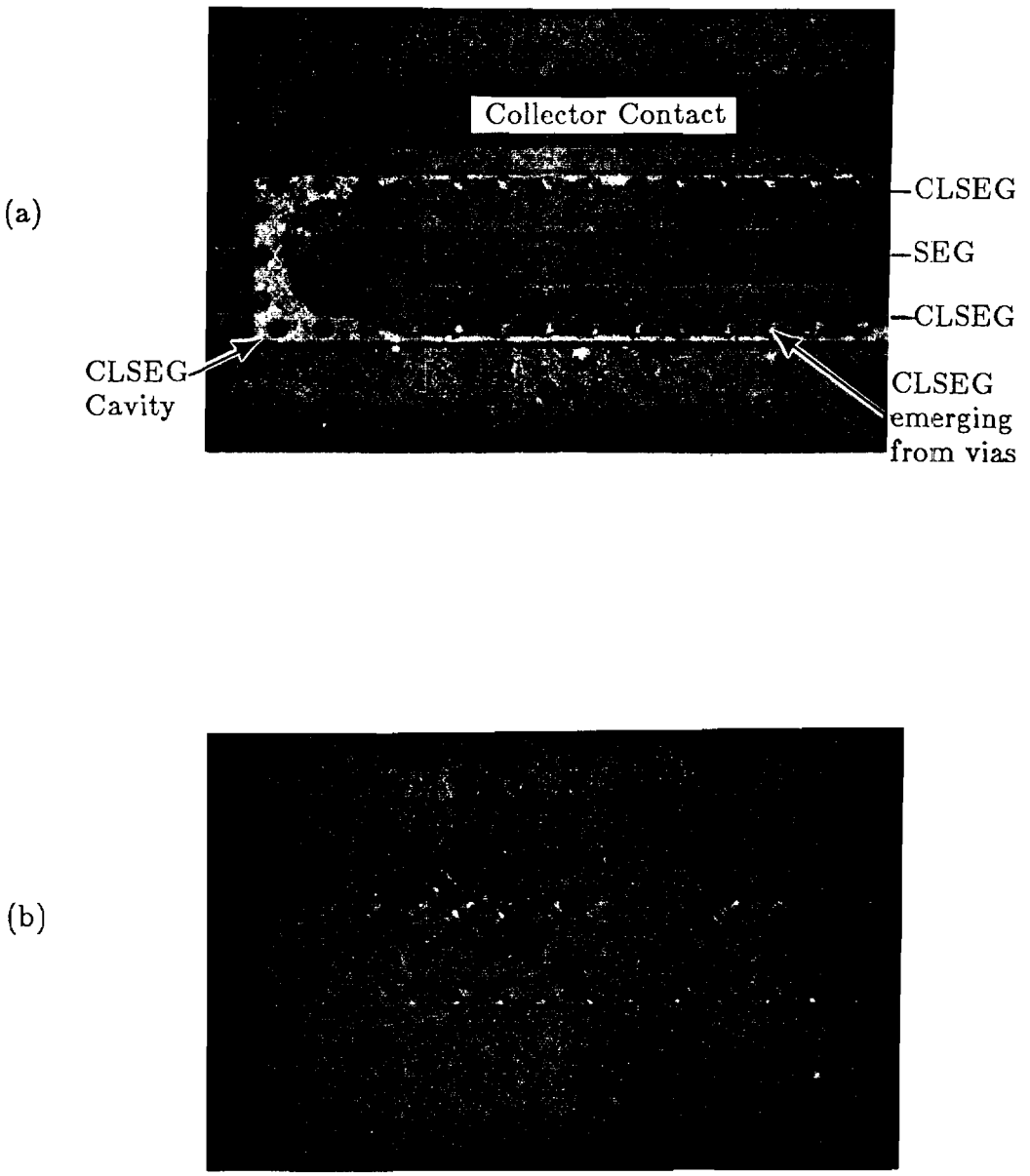

Figure 4.18. Optical micrographs of 8 μm of CLSEG growth in two different sized structures: (a) W_c=8 μm, and (b) W_c=4 μm.

The new process shown in Fignre 4.19 starts with the growth of N- doped SEG from a simple wet BHF etched field oxide to a height approximately 0.6 μm above the oxide surface. The SEG is of highest quality because of the absolute minimum of processing steps leading up to the SEG growth. A 15 minute 1000 ° C dry oxidation grows approximately 270 Å of high quality oxide on the smooth single crystal SEG surfaces. A 4000 Å LPCVD deposition of α-Si is followed by a 15 minute 900 ° C wet oxidation to grow a 700 Å oxide etch stop and cavity liner. Finally, 1500 Å of LPCVD nitride is deposited for the top cavity material as shown in Figure 4.19(b).

CMP is now used to planarize the central SEG pedestal with excellent uniformity due to the nitride field etch stop. A non-critical masking step is used to define the outer edges of the CLSEG cavity centered around the SEG growth, and Freon-115 R E is used to etch through the nitride/oxide/polysilicon stack. A 40 minute wet oxidation at 1100 ° C grows a 4000 Å capping oxide over the exposed central SEG and sides of the polysilicon cavity layer as seen in Figure 4.19(c).

The via holes are now defined and etched with SF_6 RIE and the via hole passivation performed as detailed previously. The cavity material can now be cleared out using EDP or KOH with confidence because of the high integrity of the 1000 ° C dry oxide grown following the SEG growth. In fact, cavities were etched using EDP for roughly 10 times the actual amount needed with absolutely no evidence of breaching the protective oxide. Following a quick 25 second BHF dip to remove the protective oxide, excellent quality CLSEG is grown across the entire wafer with very little nucleation on the field surface.

Finally, the excess CLSEG growth emerging from the via holes is removed with CMP as shown in Figure 4.19(d), and a hot phosphoric etch selectively removes the top cavity nitride. It should be mentioned that the results of section 4.2.1 indicate that an all oxide cavity can be used instead of the oxide/nitride combination used here. A blanket boron base implant and lithographically defined arsenic emitter are then added to produce the device structure of Figure 4.19(e).

The primary disadvantage of the structure is that the planarization step leading to Figure 4.19(c) removes all ability to self-align the emitter to the extrinsic base region. Therefore, the structure is not scalable to sub-micron dimensions and therefore not strictly capable of true high-speed operation. However, as a

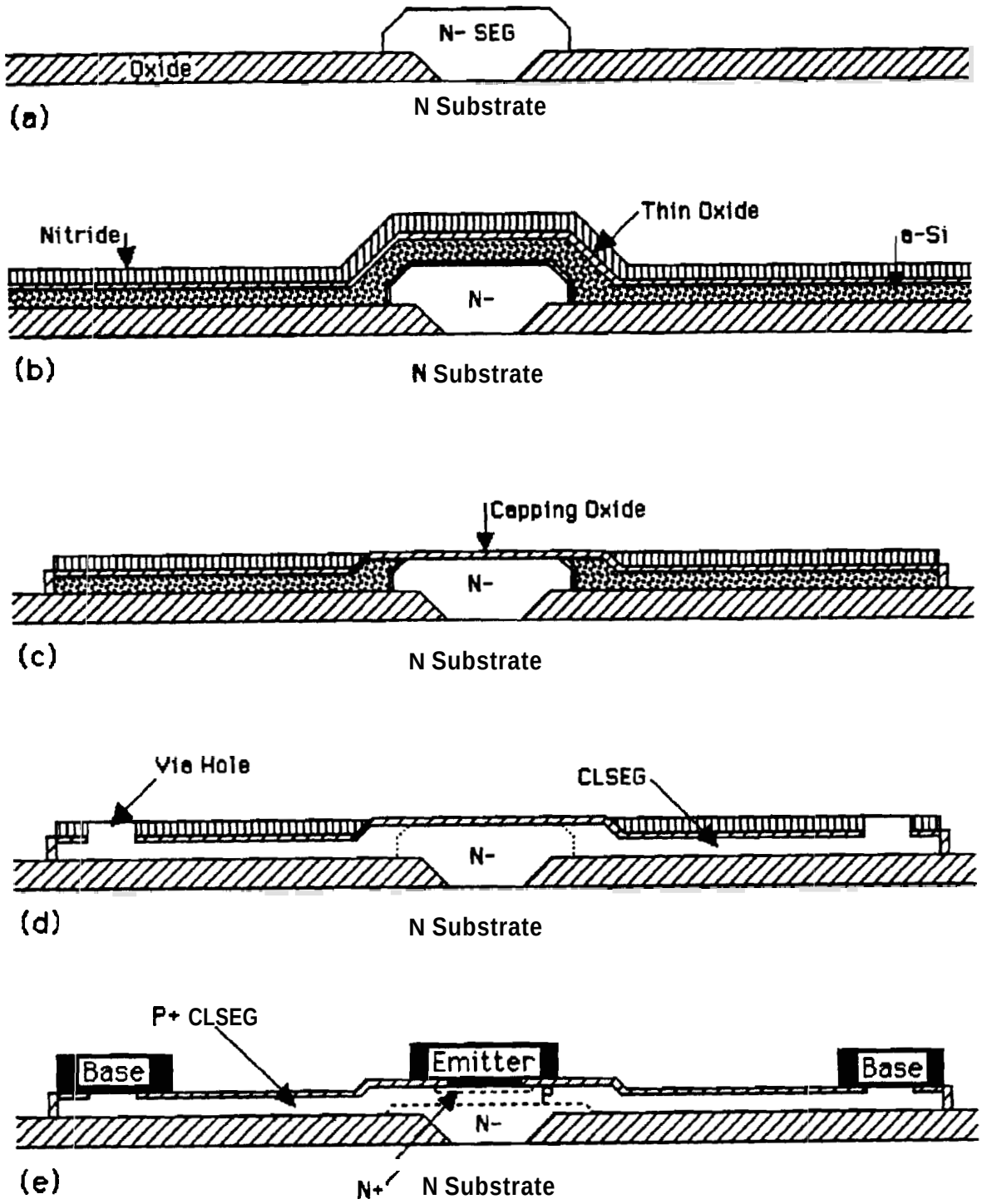

Figure 4.19. Simplified ELOBJT-3 process: (a) growth of SEG from wet BHF etched seed hole, (b) deposition of α-Si, thin oxide, and nitride layers, (c) planarization, definition of cavity and oxide capping, (d) via hole and cavity etch followed by growth of CLSEG, and (e) blanket base implant and lithographically defined emitter lead to contacts and metal.

means for investigating the material. quality of SEG and CLSEG for the ELOBJT-3 device, it is perfectly suited. The SEG grown from the BHF etched seed hole is probably more representative of the best growth obtainable in oxide/poly/oxide trenches when etched with the appropriate RIE equipment. More importantly, the new process produced excellent quality SEG and CLSEG, uniformly and reliably every time. A series of thin base NPN transistors were then fabricated using this process and their results detailed in Chapter 5.

4.3 Summary

Simulations of the ELOBJT-3 fabrication process for a scaled-down sub-micron device have been performed to verify its feasibility. Process simulations predict a normal bipolar doping profile in the intrinsic region of the device and a large out-diffusion of base boron dopant from the CLSEG region into the central SEG region for base link-up. By adjusting the start of P+ dopant during the CLSEG base contact growth, the positioning of the base link-up to emitter can be controlled.

Experimental fabrication required several problems to be solved in order to produce a workable process sequence for fabrication of the physical ELOBJT-3 structure. Growth of SEG and CLSEG in the proper configuration was demonstrated using both oxide and nitride top cavity layers. Finally, a simplified process for obtaining the SEG/CLSEG physical structure was developed.

4.4 References

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CHAPTER 5 - MEASUREMENT & ANALYSIS

Electrical characteristics of fabricated structures are tested and analyzed in this chapter. Collector-base capacitances are tested in a variety of large and medium scale structures and correlated with computer simulations. Similarly, extrinsic base resistance measurements are made and correlated with computer simulation. Finally, the full ELOBJT-3 transistor is tested and characterized to investigate the structure's potential as an ultimate high-speed sub-micron scaled BJT device.

5.1 Collector-Base Capacitance

The collector-base capacitance was investigated because of its critical effect on digital ECL bipolar circuit speed detailed in Chapters 2 and 3. Although computer simulations of the scaled down (A_e=0.35x4.0μm^2) ELOBJT-3 structure predicted significant reduction of the collector-base capacitance, validation of the computer simulation results was desired. However, sub-micron fabrication and testing was not feasible with the available facilities. Therefore, medium sized devices were fabricated and tested and comparisons made to appropriately scaled simulations.

5.1.1 Method and Testing

The collector-base capacitance of the proposed ELOBJT-3 device is a parallel combination of intrinsic junction capacitance and extrinsic oxide capacitance as shown in the diagram of Figure 5.1. It was known at the time of mask fabrication that a large device would be needed for reliable measurement of C_{cb} capacitance. If the capacitance of the device was not large enough (>1pF), it would be difficult to separate device capacitance from the stray capacitance caused by the probes and leads. Devices with SEG widths W_s no smaller than 6

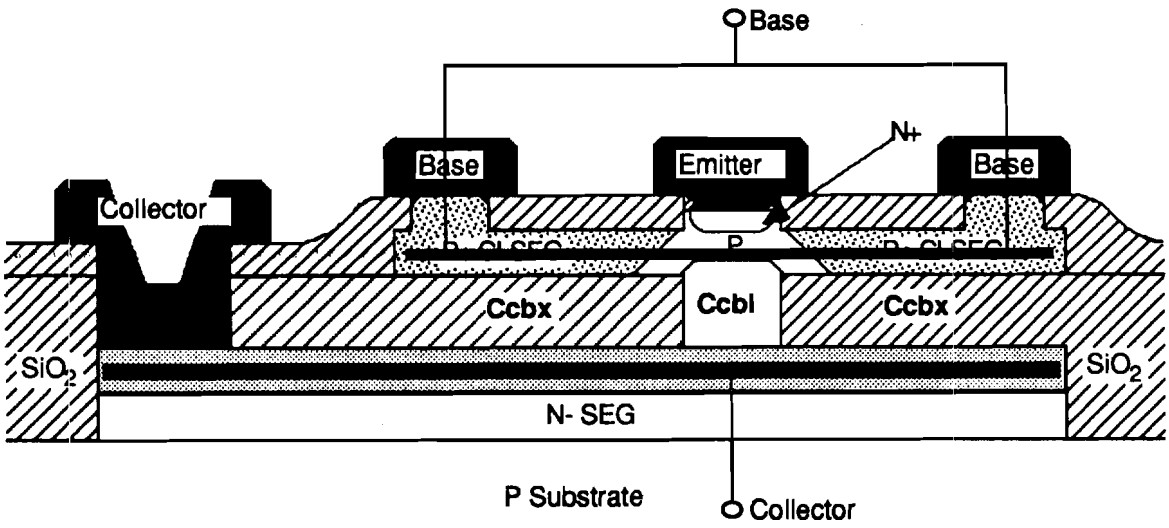


Figure 5.1. Diagram of imaginary capacitor plates superimposed on collector and base regions of the ELOBJT-3 device.

μm were made due to the difficulty of determining etching progress in the SEG trench with standard optical microscopy. However, this 6 μm width was ideal as it produced a roughly 1:1 ratio of intrinsic to extrinsic base/collector capacitance. This even ratio was important for validating the simulator's ability to predict botb oxide and semiconductor depletion capacitances.

The JWS1 photomask set included three specific devices for collector-base capacitance testing with sizes as shown in Table 5.1. Device A was made with a standard 8 μm CLSEG width and 6 μm SEG width, but with a length of 1072 μm in order to assure at least one large and therefore reliable capacitance measurement. Fabricating very long or interdigitated structures and dividing by length is a common method of measuring capacitances of modern sub-micron devices. Device B was similar to device A except that its length was only 296 μm. Device B was used to check the length scaling of the device by comparing its capacitance per unit length with device A. Finally, device C has a reduced CLSEG width W_C of 4 μm and is used to check the lateral scaling of the device.

Table 5.1. Sizes of Collector-Base Capacitance Test Structures. Parameters Correspond to Figure 4.5.

Device	SEG Width (W,) (μm)	Length (L) (μm)	CLSEG Width (W,) (μm)
A	6	1072	8
B	6	296	8
C	6	296	4

Measurements were made using an HP4275A multi-frequency LCR meter connected to an HP9000 computer for data collection. The device was probed with a Micro-Manipulator probe station using the chuck to make contact to the backside substrate collector. A probe tip was used to open-circuit the metal base and emitter contact lines leading to the probe pad, and the sensing probe was contacted to the 10 μm wide base line as close to the device as possible. After zeroing the LCR meter, all but 10-20 fF of stray capacitance was eliminated from the measurements. A standard 15 mV AC signal level was used in conjunction with a 100 KHz frequency for maximum sensitivity without high-frequency depletion effects.

New simulations were needed to predict the capacitances of these medium sized devices. PISCES-IIb was once again used to measure small-signal AC capacitances of appropriately sized structures. Doping levels and good approximations of lateral and vertical sizes were obtained from the fabricated devices of wafer lot#JWS26 due to its good quality CLSEG and well known SEG doping. However, the highly doped sub-collector of the proposed ELOBJT-3 device shown in Figure 5.1 was not simulated because it was not present in the fabricated JWS26 devices. Although the JWS26 wafers were not identical to the proposed device structure, the comparison of real data to computer simulation was sufficient for validating the accuracy of the simulator.

The PISCES-IIb input file for the A device simulation is listed in Appendix D. The substrate used was (100) P-type boron, approximately $7x10^{15}cm^{-3}$ doped. An N-type phosphorus SEG doped $1x10^{16}cm^{-3}$ was then grown within the trench

and N+ approximately $1x10^{18}cm^{-3}$ doped CLSEG was grown from the SEG sidewall. Finally, a P+ boron doped emitter was implanted in the top of the SEG region but was not simulated. Uniform dopings were used for all regions of the device because they reasonably approximated the dopings in the actual device. The ,simulations were of one side (1/2) of the structure due to its symmetry. Results were multiplied by 2 and by the length of the actual devices for comparison with the measured data.

5.1.2 Results

Results of the PISCES-IIb collector/base simulations are shown in Figure 5.2. The 0 volt reverse bias of Figure 5.2(a) shows the depletion region near the base-collector junction extending partially into the SEG base and partially into the substrate collector. It also shows that because a low doped substrate ($7x10^{15}cm^{-3}$) was used, the positive charge put on the N+ CLSEG base contact acts to slightly deplete the P-substrate below. Of course this depletion would not occur if the typical P+ doped buried layer collector had been used. The depletion region edge is seen to move farther into the SEG and substrate regions as a 10 volt reverse bias is applied in Figure 5.2(b). Here, the added depletion region below the CLSEG material acts to significantly decrease the CLSEG/oxide/substrate capacitance. However, it was interesting to see how the simulated and measured data correlated with this extra depletion region effect.

Figure 5.3 shows a plot of measured and simulated collector-base capacitance for a typical device A type structure over the reverse bias range of 0 to 30 volts. The correlation of simulated to tested data is remarkably good.. An error of about 4% is obtained at 0 volts and roughly 11% at 10 volts. Although the simulator predicted a capacitance drop around 12 volts which did not show up in the measured data, the correlation at 0 and -30 volts bias is still excellent. The jump in simulated capacitance near 10-12 volts is caused by the depletion region edge in the intrinsic base region reaching the top surface of the simulated grid area and being moved completely into the N+ CLSEG region. As charge can only be added and subtracted at the depletion region edge, the intrinsic region capacitance is quickly reduced causing the jump in Figure 5.3.

The next correlation checked was the scaling of the overall length, L. Figure 5.4 shows the same capacitance versus voltage plot as Figure 5.3 except that the measured data is for a typical type B device with L=296 μm. Once again, the

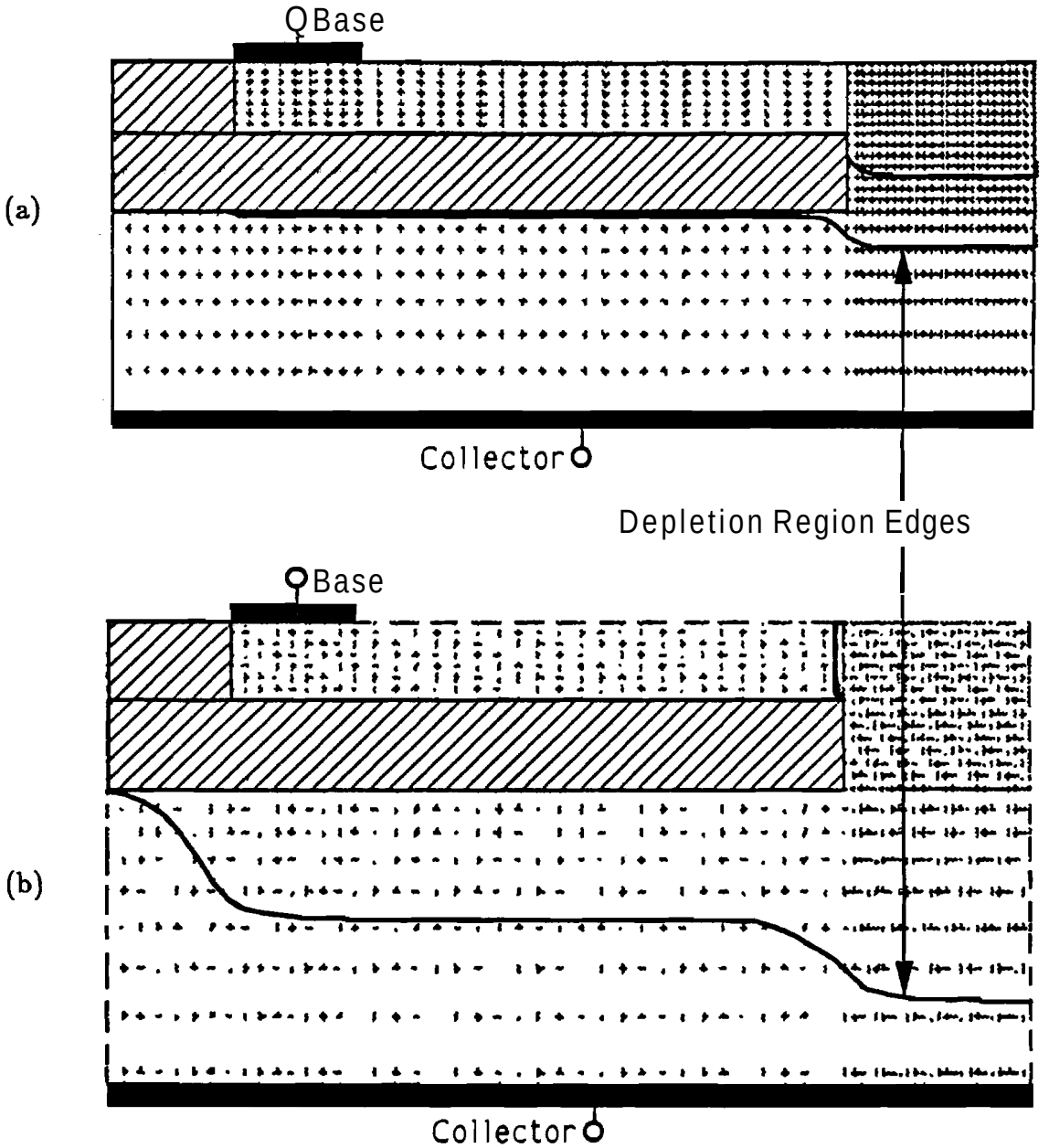


Figure 5.2. Two-dimensional PISCES-IIb grids showing depletion regions for applied reverse biases of (a) 0 volts and (b) 10 volts.

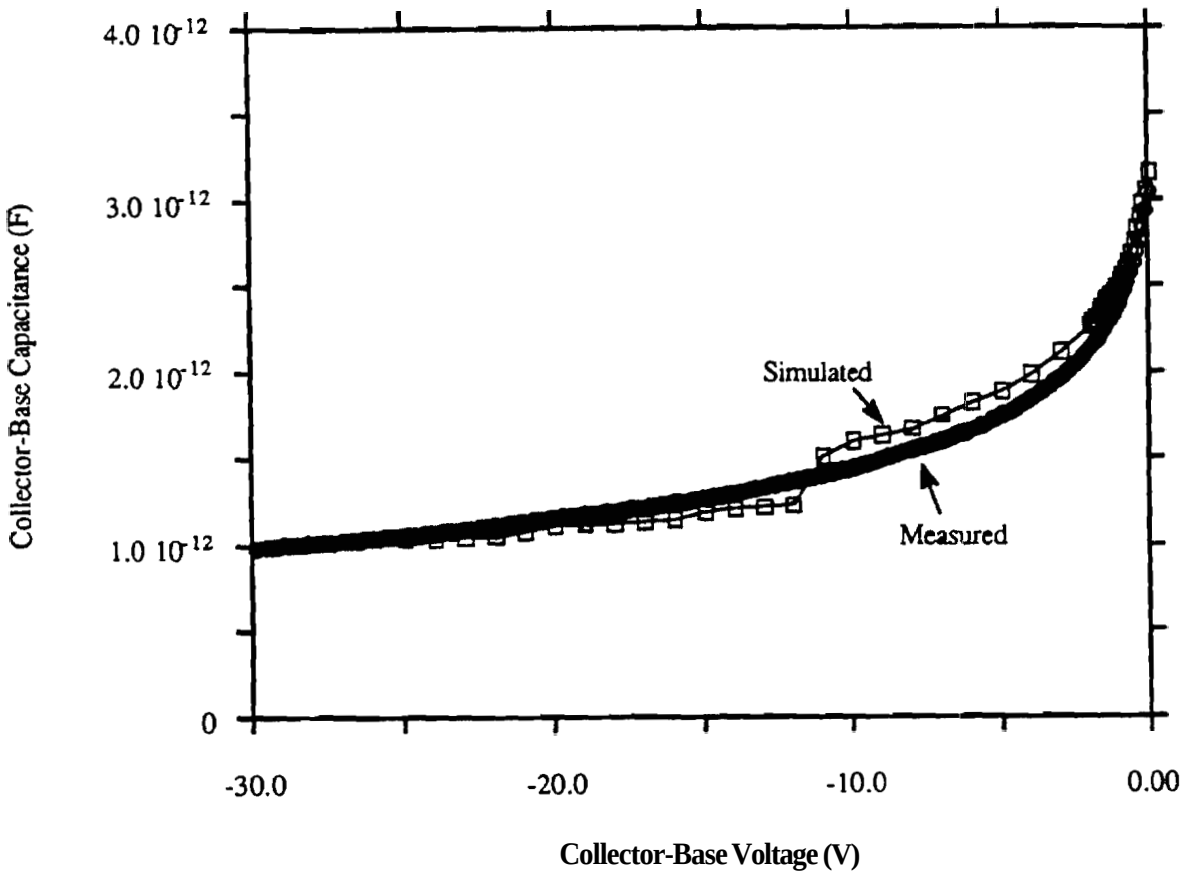


Figure 5.3. **Plot of measured versus simulated reverse bias collector-base capacitance for a type A device with L=1072 μm and W_c=8 μm.**

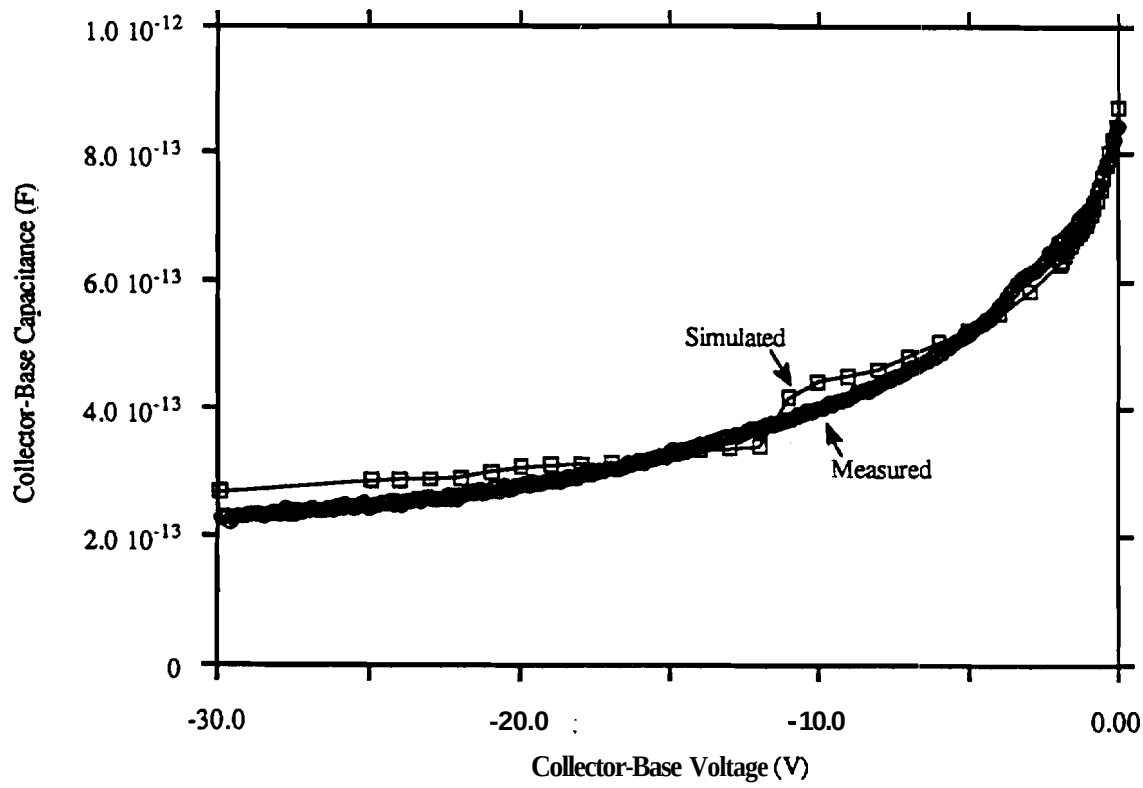


Figure 5.4. Plot of measured versus simulated reverse bias collector-base capacitance for a type B device with L=296 μm and W_c=8 μm.

simulated capacitance fit the measured data almost exactly. 'There was an approximate 4% error at 0 volts bias and roughly 10% error at 10 volts bias. At the 30 volt bias point, the simulated capacitance was about 19% greater than the measured data. However, it should be noted that the simulations were first run attempts to model the experimentally fabricated devices. No parameters were adjusted in the simulations to fit the data. The 19% error at 30 volts bias could easily be due to slight differences in oxide thicknesses, widths of SEG and CLSEG growth and doping levels. Also, the measured capacitance of roughly 220 fF at 30 volts was starting to approach the accuracy limits of the testing procedure. However, overall the comparison easily proves the validity of the length scaling of the devices.

Finally, scaling of the lateral dimension of the CLSEG region was tested with device type C. Figure 5.5 shows a comparison of measured versus tested data for a type C device with L=296 μm and CLSEG width W_c=4 pm. There was a 6.8% error at 0 volts bias and roughly 13% error at 10 volts bias. Again, the error is easily within expected limits given the accuracy of the capacitance measurement and uncertainty of the parameters used in the simulation. This validates the ability of the simulator to provide accurate capacitances for laterally scaled .devices.

The capacitance data is summarized in a per length format for two biases representative of high-speed bipolar operating conditions. Table 5.2 shows base-collector capacitance data for 0 and 2 volt reverse bias conditions. Simulated capacitances are shown to be within 10% of the measured values in the worst case and within 3% in the best case. The validity of computer simulations to accurately predict collector-base capacitances in scaled down devices has therefore been established.

5.2 Extrinsic Base Resistance

Next, it was important to investigate the expected improvement in the extrinsic base resistance of the new device structure. In Chapters 2 and 3, R_{bx} was shown to be the second most important parameter affecting digital ECL bipolar circuit speed. Computer simulation of the scaled down (A_e=0.35x4.0μm^2) ELOBJT-3 structure predicted a significant reduction in R_{bx} over a similar poly contacted

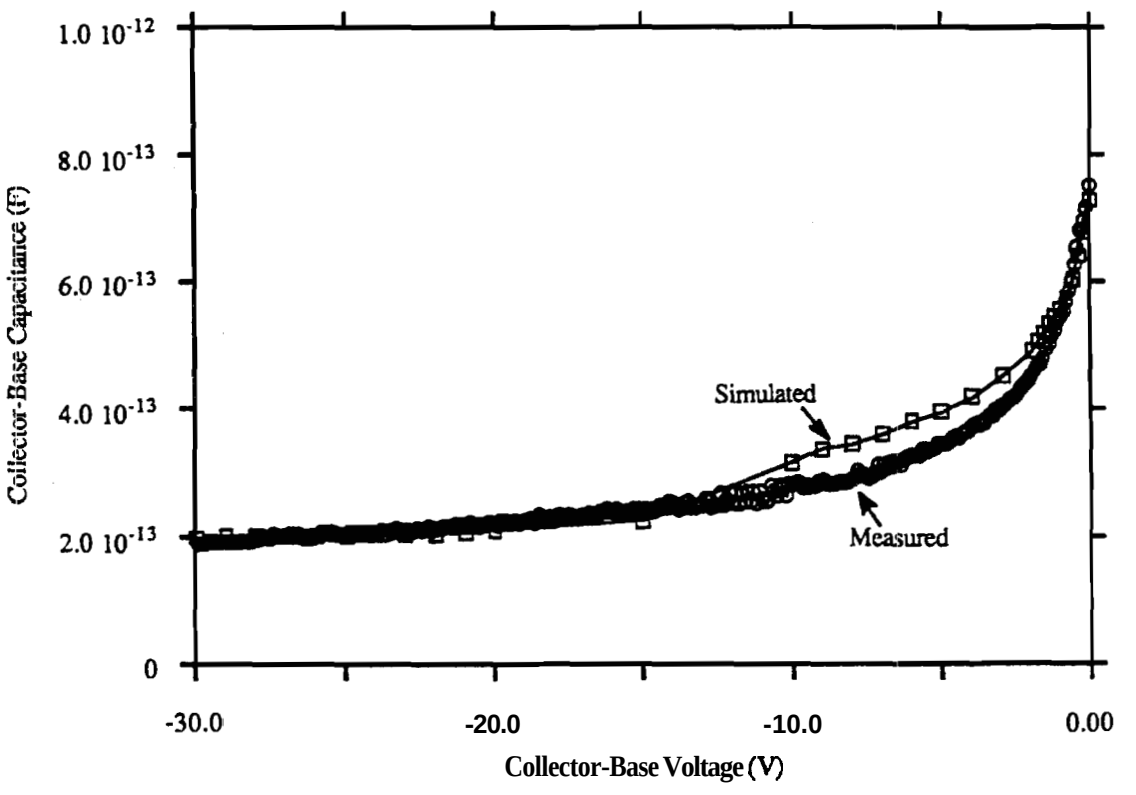


Figure 5.5. Plot of measured versus simulated reverse bias collector-base capacitance for a type C device with L=296 μm and W_c=4 μm.

Table 5.2. Summary of Normalized Collector-Base Capacitance Results for Both 0 and 2 Volt Reverse Biases.

Device	C/L @ 0V			C/L @ -2v		
	Meas. (fF/μm)	Simul. (fF/μm)	Error (%)	Meas. (fF/μm)		
A	2.84	2.95	+3.9	1.99	2.12	
B	2.85	2.95	+3.5	2.23	2.12	
C	2.54	2.46	-3.1	1.52	1.65	+8.5

structure. However, these claims needed to be verified. First, data from extrinsic base contact resistance test structures fabricated with in situ doped CLSEG material was correlated with computer simulations. Secondly, a new technique was (employed to measure the extrinsic base resistance in fully functioning ELOBJT-3 devices. Two independent methods could therefore more conclusively validate the computer simulations of Chapter 3.

5.2.1 R_{bx} Resistance Structures

5.2.1.1 Method and Measurements

Extrinsic base resistance R_{bx} is commonly defined as the bias independent portion of the total base resistance R_{bT}. More specifically, it is defined as the resistive region which lies between the base contact and an imaginary plane surface located at the exact edge of the emitter region. Several dynamic measurement:: have been developed for extracting parasitic bipolar resistances from functioning bipolar transistors.[1,2] However, these methods require almost ideally functioning junctions and become less accurate as the resistances become smaller.

A much simpler method was chosen for validating the resistance predictions of the PISCES-IIb simulator. Test structures were fabricated using a self-aligned PNP device and a heavy N+ arsenic implant in place of the P+ boron emitter to form very low resistance contacts at the ends of the N+ CLSEG layer as shown in

Figure 5.6. These structures then enabled the exact measurement of the bias-independent R_{bx} resistance without having to perform detailed curve fitting of the emitter-base junction.

Additional simulations were performed for correlation to the medium sized devices of Table 5.3. Contrary to the R_{bx} simulation of section 3.2.1, a plan view instead of cross-section was simulated as shown in Figure 5.7.. This change was necessary due to the contacting used in the actual fabricated structure. Lengthwise symmetry was lost because the metal contact to the CLSEG was made at the via holes only, not in a continuous contact along the length of the CLSEG. A cross-sectional simulation would not be able to take into account the roughly 2x3 μm^2 via hole contacts and would therefore have under-estimated the CLSEG resistance. A Spreading Resistance Profile (SRP) measurement was used to determine the roughly $10^{18} cm^{-3}$ in situ phosphorus doping of the CLSEG material. Finally, as the via hole contacts were placed every 8 μm along the length of the CLSEG, an 8 μm length with one centered via hole was simulated and its resistance divided by the CLSEG thickness and number of via holes to obtain the resistance of the real structure.

Several problems were encountered in measurement of the fabricated devices. First, it was discovered that the contact resistances obtained using approximately 1000 Å of Aluminum-1%Silicon alloyed at 400 °C were greatly over-shadowing the desired resistance measurement. The solution was found in depositing 2500 Å of metal to obtain better step coverage into the via hole contact and alloying the metal at 500" C to ensure a very low resistance contact at the metal/semiconductor junction. Although the higher alloy temperature probably caused deeper sintering of the aluminum into the contacts, it produced no ill effects as there were no shallow junctions underneath the contact. Finally, the non-negligible resistances of the metal lines and probe pads were the only parasitic resistances left to be determined.

It was found that a correction factor (CF) for each device could be developed to account for the parasitic resistance of the metal lines. The micromanipulator probe station was used to probe each metal line segment and the combination of series elements formed the CF for each device structure. The CF's for each of the five resistor structures are listed in Table 5.4.

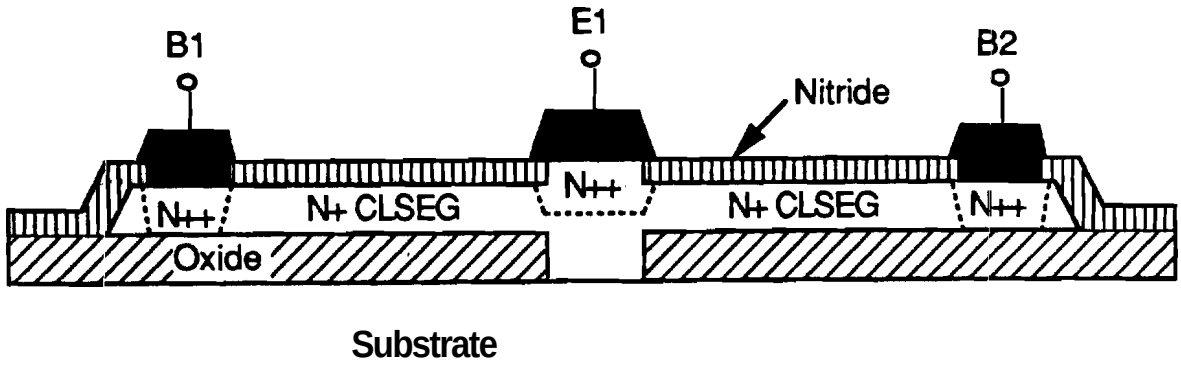


Figure 5.6. Cross-section of resistance structure used to verify accuracy of simulations.

Table 5.3. **Sizes of R_{bx} Test Structures. Parameters Correspond to Figure 4.5.**

Device	SEG Width (W,) (μm)	Length (L) (μm)	CLSEG Width (W,) (μm)
L276W8	6	276	8
L276W4	6	276	4
L200W8	6	200	8
L128W8	6	128	8
L28W8	6	28	8

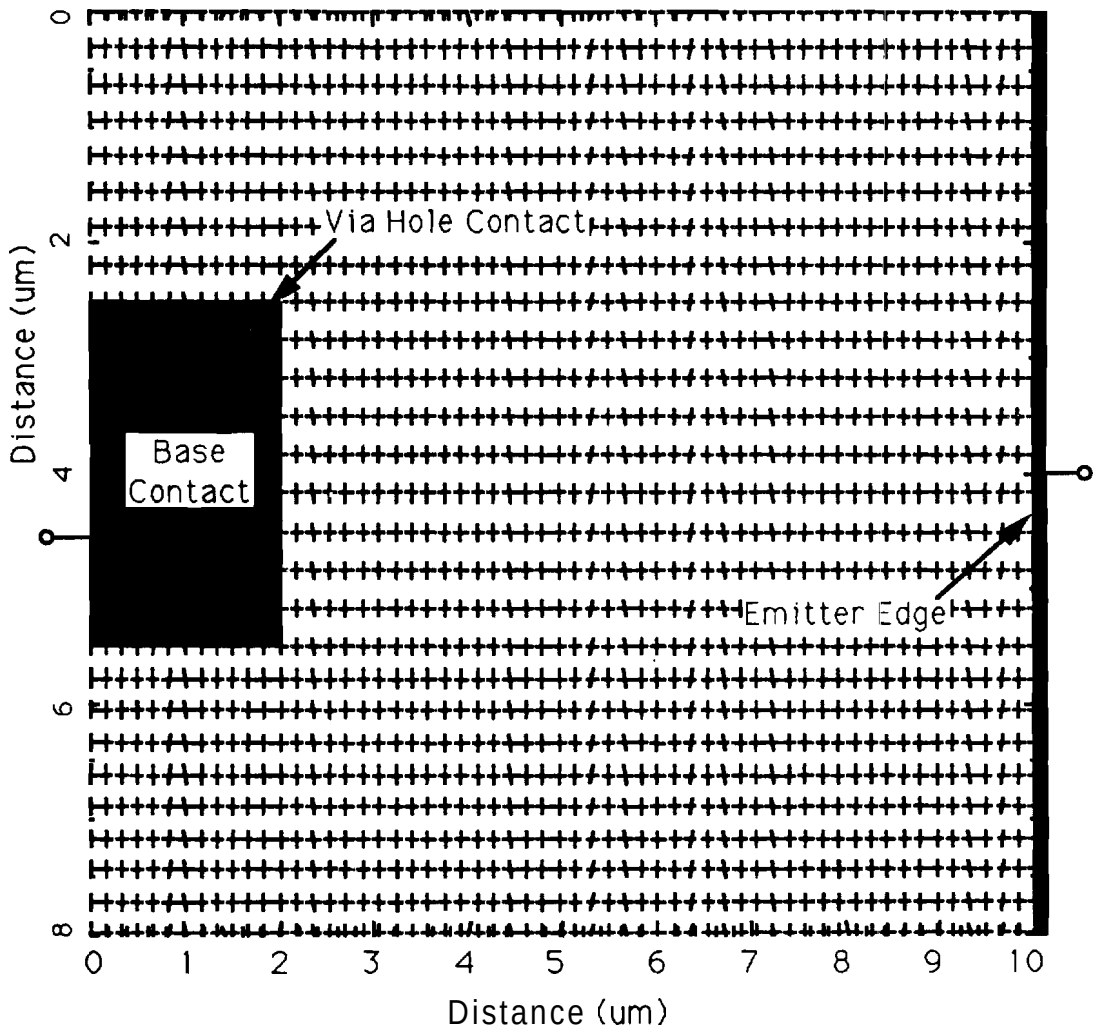


Figure 5.7. Plan view of PISCES-IIb **grid used in** R_{bx} **simulations.**

5.2.1.2 Results and Discussion

The first two structures measured were the L276W8 and L276W4, both having identical CLSEG lengths but different widths between contacts. 6 to 8 devices of each type were measured and the uncorrected values plotted in Figure 5.8. Although two data points, 4 μm and 8 μm do not indicate a linear fit, it can be reasonably assumed due to the simple linear nature of fixed geometry resistors. The clata clearly shows a scaling of resistance with CLSEG width in close approximation to the PISCES-IIb predictions for 4 μm and 8 μm width structures. The 0 width offset of 19.4 Ω is obviously the parasitic resistance associated with the probe lines and matches within 5% the metal line resistance measured with the micromanipulator. Although more data points in the width dimension would have been desirable, more than 8 μm of CLSEG would have been difficult to obtain due to difficulties in long selective epitaxy growths. Similarly, a width smaller than 4 μm was virtually impossible due to limited lithography resolution. However, the data does establish the width scaling of the CLSEG resistance.

Next, scaling of the CLSEG resistance was verified in the length dimension. Figure 5.9 shows resistance data for each of the 4 different length structures. This time, the metal line CF has been subtracted from the data and the solid and dashed lines indicate the data average and computer simulation respectively. The difference between computer simulation and real data is greatest at the longest 276 μm length because the resistance is smaller and somewhat obscured by the parasitic resistance. Also, it should be noted that Figure 5.9 is not linear because the resistance varies inversely with the length of the structure. However, the correlation between the averaged data and simulation clearly establishes the length scaling of the resistance structure.

Table 5.4 shows the data from both the width and length scaled devices and how they correlated with computer simulation. The remarkable agreement with simulated values should be kept in perspective. With the many uncertainties used in forming the simulations and measuring the devices, it is only relevant that there was correlation within 20-30%. That is, the 0.2% error for the L28W8 devices is far beyond the measurement and simulation accuracy of the test. Ultimately, scaling of the extrinsic base resistance in both the width and length dimensions has been established, as well as correlation of the scaled dimensions to computer simulation,

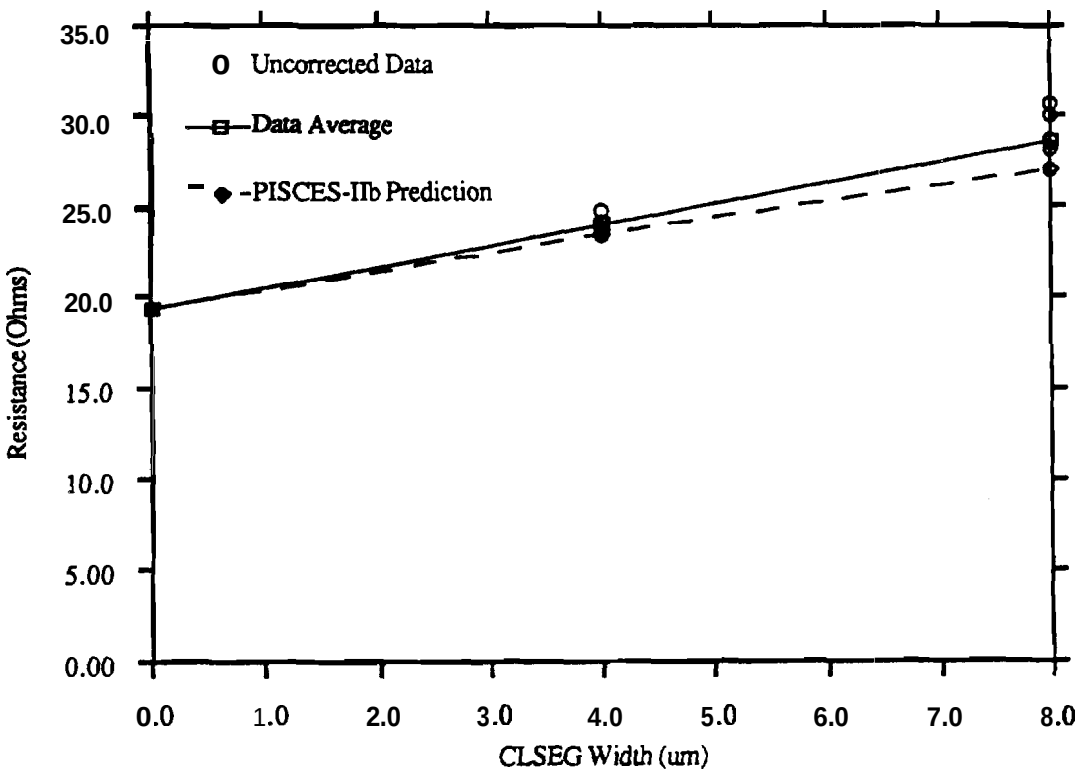


Figure 5.8. Plot of uncorrected resistance data from 4 and 8 μm CLSEG width structures. Solid line denotes average of data and dashed line denotes PISCES-IIb with approximation for metal line resistance added.

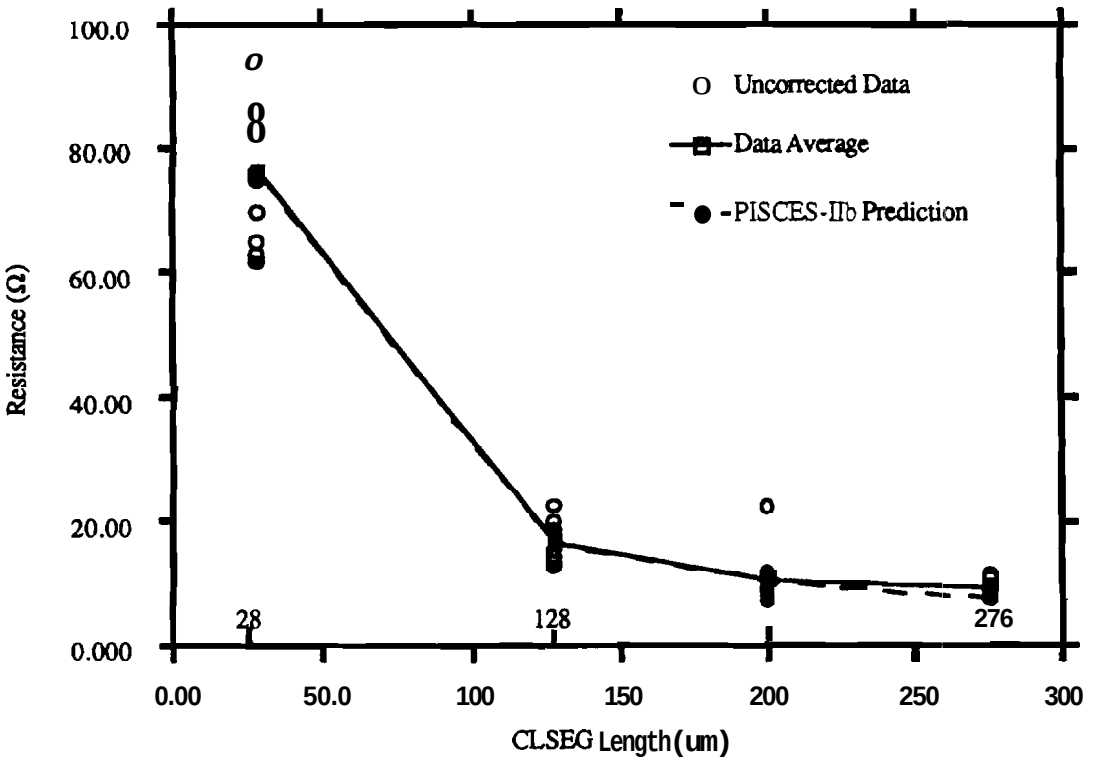


Figure 5.9. Plot of corrected resistance data from 276, 200, 128, and 28 μm CLSEG length structures. Solid line denotes average of data and dashed line denotes PISCES-IIb approximation.

Table 5.4. Summary of Measured Resistance Data of N+ Doped CLSEG Structures.

Device Name	Raw Data (Ω)	CF (Ω)	Corr. Data (Ω)	PISCES (Ω)	%Error
L276W8	28.6	19.4	9.2	7.7	16.3
L276W4	24.0	19.4	4.6	4.1	10.8
L200W8	26.8	16.0	10.8	10.5	2.8
L128W8	30.9	14.1	16.8	16.5	1.8
L28W8	88.5	12.3	76.2	76.0	0.2

5.2.2 Dynamic R_{bx} Measurement

5.2.2.1 Method and Testing

A new dynamic measurement technique for measuring base resistance[3] was performed as a second method for validation of the R_{bx} simulations. A device with two separate base contacts as shown in Figure 5.10 was used to extract the extrinsic base resistance in the following way. A forward bias voltage and current is applied between the emitter and one of the base contacts, V_{B1}. At the same time, a very low current voltage sense is made at the opposite base contact, V_{BS}. .Assuming there is very little current and therefore voltage drop across the intrinsic base due to current crowding at the edge of the emitter, the second base tap senses the approximate potential at the interface between the B1 extrinsic region and the emitter. The difference between this voltage, V_{BS}, and the B1 terminal voltage, V_{B1}, is the voltage drop across the extrinsic base region, and can be divided by the known current flow to obtain the extrinsic base resistance.

This technique was applied to several functioning double base contact NPN bipolar devices. The double base devices were identical in size to the L276W8 devices except that their R_{bx} resistances would be larger due to current flow through only one base contact instead of two. In addition, these measurements were taken on NPN devices which received a light intrinsic base boron implant. TSUPREM-4 simulations predicted a roughly $1x10^{18}cm^{-3}$ concentration of boron

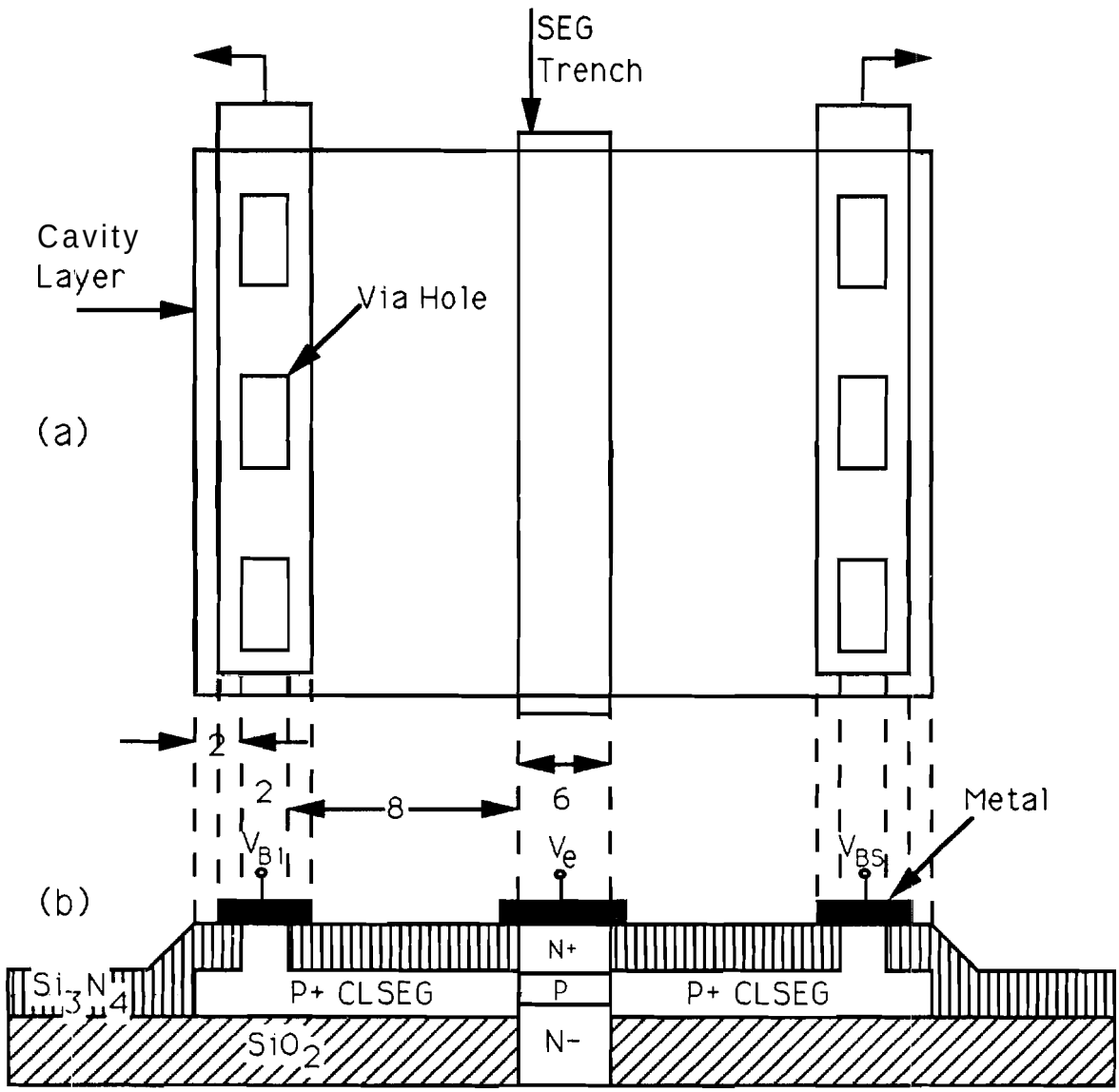


Figure 5.10. Double opposing base contact device: (a) top view of layout, (b) cross-section of structure.

in the 0.3 μm CLSEG extrinsic base contacts. The R_{bx} simulation of section 5.2.1.1 was repeated this time using a P-type doping of $1x10^{18}cm^{-3}$ for the extrinsic base CLSEG material.

5.2.2.2 Results and Discussion

Figure 5.11 shows a typical double base contact measurement. In the 0 to 1 volt range, a normal diode curve is seen with current flow quickly increasing. However, above 1 mA, resistance effects start to significantly limit the total current flow and the curve bends over toward the horizontal. In the same plot, the total base resistance is calculated at each point as the difference between the base terminal voltage and base sense voltage, divided by the emitter current. As the current increases, current crowding at the edge of the emitter reduces the intrinsic base portion of the total base resistance plotted in Figure 5.11. The asymptotic value of the total base resistance is then the actual extrinsic base resistance.

An average R_{bx} of 38.3 Ω was measured over 7 typical devices. After a correction of approximately 12.8 Ω due to the parasitic metal line resistance of the base contact, an average R_{bx} of 25.5 Ω is indicated. PISCES-IIb simulations ,predicted a one-sided extrinsic base resistance of 31.6 Ω for a 296 μm long by 8 μm wide CLSEG region. The 19.3% error is well within the accuracy of the simulation and measurement techniques and independently validates the R_{bx} simulations of Chapter 3.

5.3 Transistor Measurements

In addition to capacitance and resistance test structures, full ELOBJT-3 devices were fabricated in both the NPN and PNP configurations. Several modifications however were used in order to simplify the processing of the full device and eliminate unwanted variations in the process. First, the N-/N+ doped SEG subcollector of Figure 3.1 was not attempted due to its relative ease of incorporation. N-type <100> substrates were used instead and collector contact was made to the backside of the wafers for ease of testing. Secondly, the emitter sidewall spacer technique shown in Figure 3.1 was not used due to the difficulty and time required to establish a reliable sidewall spacer technique. Finally, a new SEG/CLSEG growth technique detailed in section 4.2.6 was used to obtain the

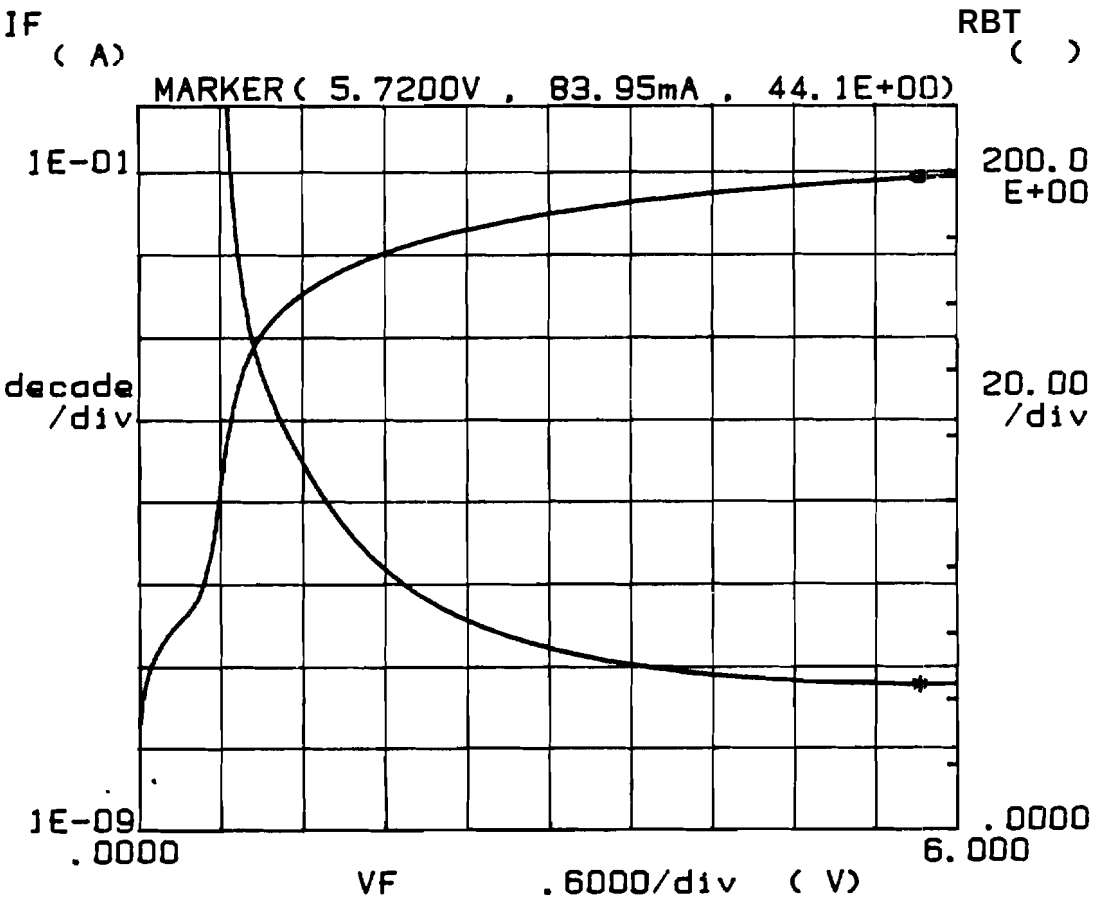


Figure 5.11. **Plot of forward biased base/emitter characteristic of double base contact device with calculated total base resistance.**

physical device structure for a final set of NPN devices.

5.3.1 Self-aligned PNP Device

5.3.1.1 Fabrication

The first set of ELOBJT-3 devices were self-aligned PNPs with an epitaxially grown base. P-type 1-5 Ω-cm <100> substrates were prepared with a 1.5 μm thick oxide/poly/oxide/nitride stack and the SEG seed hole etched as detailed in section 4.2.5. Approximately 4.0 μm of SEG was then grown in 20 minutes using standard selective epitaxy parameters, 970 °C, 40 Torr, 60 slpm H_2, 0.22 slpm DCS, and 0.66 slpm HCl in a Gemini-I reactor. The growth was preceded by a 5 minute H_2 prebake to remove native oxides on the seed regions and a 30 second HCl etch to clean the silicon surfaces, both done at growth temperature and pressure. Using no intentional phosphine flow into the reactor, the SEG grew approximately $5x10^{15}cm^{-3}$ N-type due to residual background phosphorus doping in the reactor. Following SEG growth, 6 minutes of CMP (see section 4.2.4) easily removed the 2.5 μm of excess SEG grown out of the trench to leave a smooth planar top surface. 30 minutes of wet oxidation at 1100 °C grew a 4600 Å thermal capping oxide on the top of the planarized SEG.

The CLSEG via holes were then lithographically defined and etched using an SF^6 RIE, via hole passivation performed (section 4.2.5), and the cavity polysilicon removed using a 10 wt% KOH solution. After a 75 second BHF dip to remove the sidewall oxide, 110 minutes of in situ N+ doped ($1x10^{18}cm^{-3}$ phosphorus) CLSEG material was grown to a lateral distance of approximately 9 μm to (emergefrom the 8 μm wide cavity. Once again, 9 minutes of CMP removed the excess 1 μm of CLSEG grown out of the via holes. Since $10^{18}cm^{-3}$ N-type doping would not be sufficient to ensure a good ohmic contact, a non-critical masking and heavy N+ arsenic implant was used to ensure sufficient N+ doping of the CLSEG at the via holes. This step would not be required for CLSEG grown with the maximum available dopant incorporation.

Finally, a non-critical mask was used to cover the CLSEG via holes, and a wet BHF etch removed the capping oxide over the central SEG pedestal. A $3x10^{15}cm^{-2}$ boron implant at 25 KeV was used to dope the P+ emitter in the top of the SEG region. A 20 minute 1000 °C wet O_2 drive diffused the P+ emitter approximately 0.4 μm into the SEG, leaving the in situ doped phosphorus base

region approximately 0.8 μm thick. Low gain PNP devices were therefore expected as the metallurgical base width was relatively thick.

5.3.1.2 Results and Discussion

The non-optimized, wide-base, self-aligned PNP process produced the first functioning ELOBJT-3 devices with DC gains greater than one. Generally, gains were low and the devices suffered from excessive base current in the low forward bias regime due to recombination at the emitter/base junction. Figure 5.12 shows a typical Gummel plot of collector and base current versus applied base/emitter voltage. Below approximately 1 μA, base current exceeds collector current presumably due to excess recombination at the base/emitter junctiion. Table 5.5 summarizes the measured data from the self-aligned ELOBJT-3 PNP devices and from large area bulk SEG PNP monitor devices. Fabrication of substrate monitor devices was not possible due to the extra masks required and amount of additional process complexity. Therefore, monitor devices were built in large area ($60x350\mu m^2$) SEG regions with the same epitaxially grown base, but with a lithographically defined emitter. Collector/base junction characteristics of the ELO and SEG monitor devices compared reasonably with average forward ideality factors of about 1.35 and reverse leakage current densities J_{cbo} about a factor of 20 higher in the ELOBJT-3 devices.

The self-aligned walled emitter/base junction of the ELOBJT-3 devices were of significantly lower quality with average forward ideality factors of 1.73 versus 1.00 in the SEG monitor devices (see Figure 5.13). Also, the reverse leakage currant densities J_{ebo} in the ELOBJT-3 devices were 3 orders of magnitude higher than the non-walled emitters in the bulk SEG devices. Increased low current recombination in the walled emitter/base junction explains the non-ideal base current in the low bias region of the Gummel plot of Figure 5.12. The increased recombination is apparently caused by the junction's intersection with or proximity to the SEG/oxide sidewall interface.

The wide, epitaxially grown base produced low emitter-collector leakage currents in the ELOBJT-3 devices. However, it also produced very low DC curnmt gains, 6.1 in the SEG monitor devices and about 4 in the ELOBJT-3 devices. The slightly lower gains in the ELOBJT-3 devices must be attributed to increased minority carrier recombination in the base near the SEG/oxide sidewall due to lower material quality, However, positive current gain was obtained over

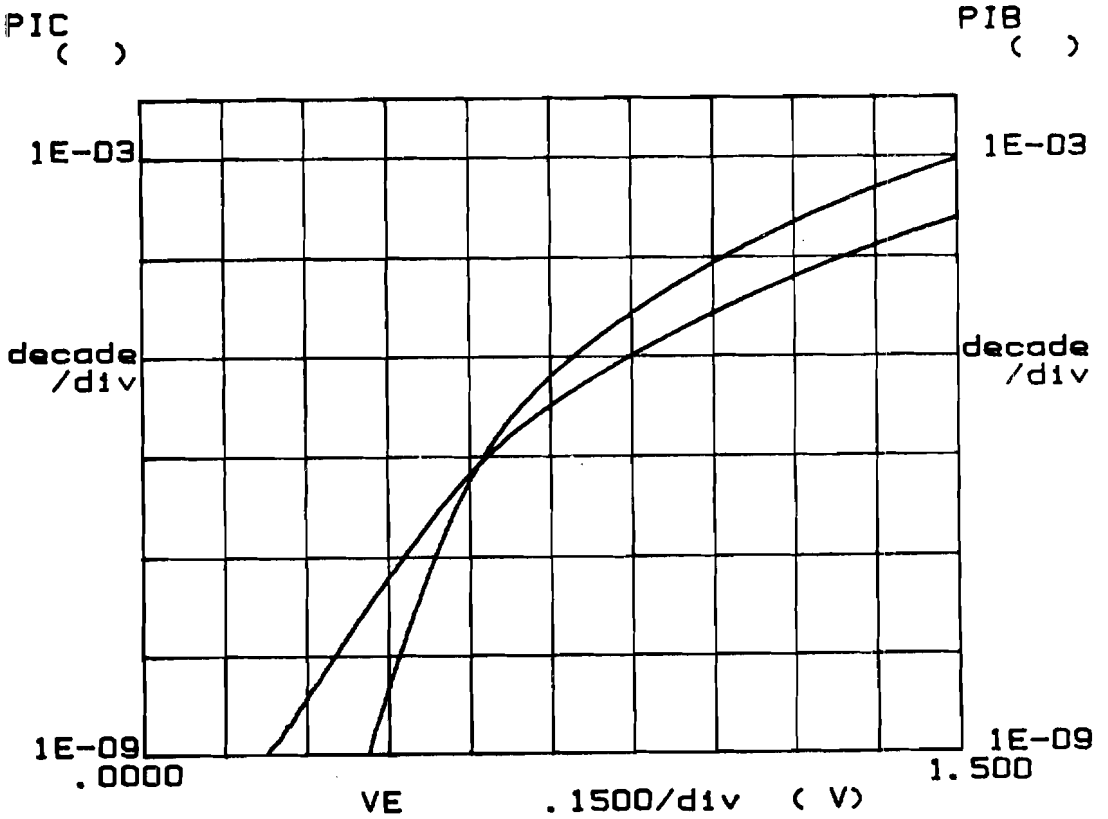


Figure 5.12. Gummel plot of typical PNP ELOBJT-3 transistor. Collector and base current are shown versus applied base/emitter voltage with the base and collector terminals shorted. Emitter area is 20x80 ym^2.

Table 5.5. Summary of Measured Data From ELOBJT-3 PNP and Bulk SEG Monitor Transistors. Averages are Taken Over 5 Devices.

Parameter	Average ELOBJT-3	Best ELOBJT-3	Average Bulk SEG
η_{be}	1.73	1.57	1.00
J_{ebo}@3V(A/cm^2)	6.0×10^{-3}	6.1×10^{-4}	4.2×10^{-6}
η_{bc}	1.38	1.24	1.35
J_{cbo}@3V(A/cm^2)	5.3×10^{-4}	6.7×10^{-5}	2.6×10^{-5}
J_{ceo}@4V(A/cm^2)	3.7×10^{-4}	3.6×10^{-4}	2.0×10^{-5}
β_{max}	3.85	4.03	6.10

about 3 decades of collector current as seen in Figure 5.14.

Overall, the fabricated PNP ELOBJT-3 devices satisfied the first major goal. Basic BJT operation was demonstrated for the self-aligned ELOBJT-3 device using in situ doped CLSEG extrinsic base contacts. The low gains are easily explained by the wide base width. An investigation was begun to develop a thin base PNP process to produce higher current gains. Unfortunately, ion implantation of phosphorus was needed but not available to produce shallow base diffusions for a thin base PNP profile. Therefore, having demonstrated the self-aligned in situ doped CLSEG base contacts, work returned to NPN devices to obtain more reasonable current gains.

5.3.2 Baseline NPN Devices

During initial fabrication attempts of the first NPN ELOBJT-3, poor quality SEG bulk monitor devices were obtained indicating a problem with the baseline NPN process. Fabrication of substrate NPN transistors in a separate wafer confirmed these problems. First, poor quality emitter/base junctions exhibited emitter/base shorts in roughly 95% of the devices. Secondly, an exorbitant

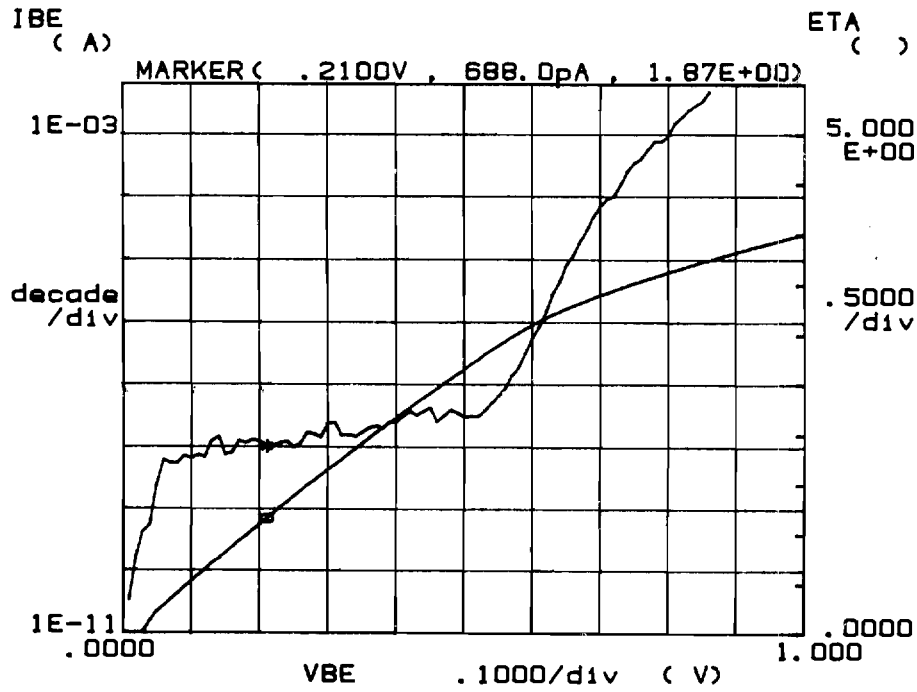


Figure 5.13. Forward diode characteristics of the emitter/base junction of a typical PNF ELOBJT-3 transistor.

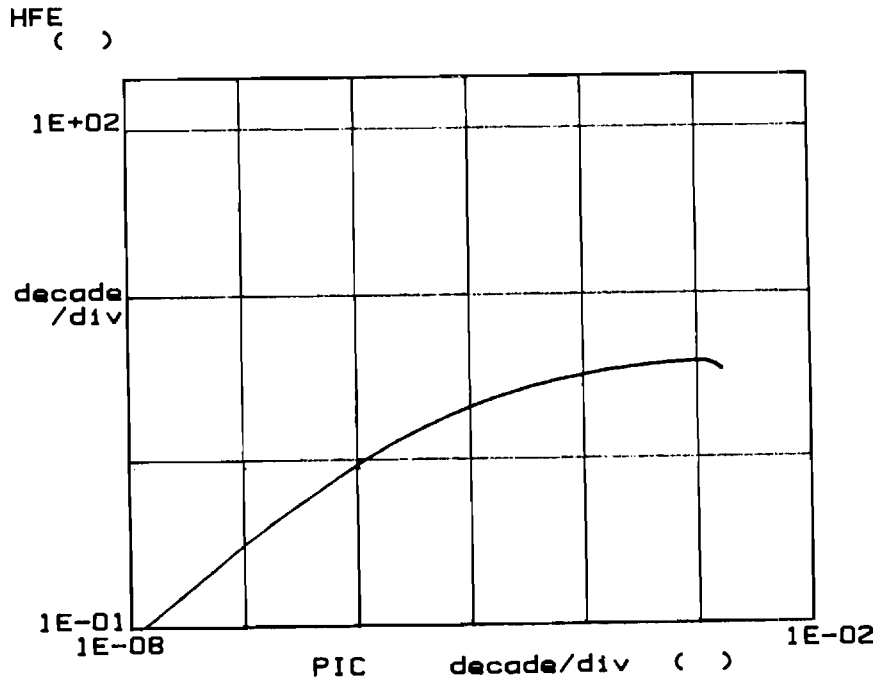


Figure 5.14. DC current gain versus collector current for a typical PNP ELOBJT-3 transistor.

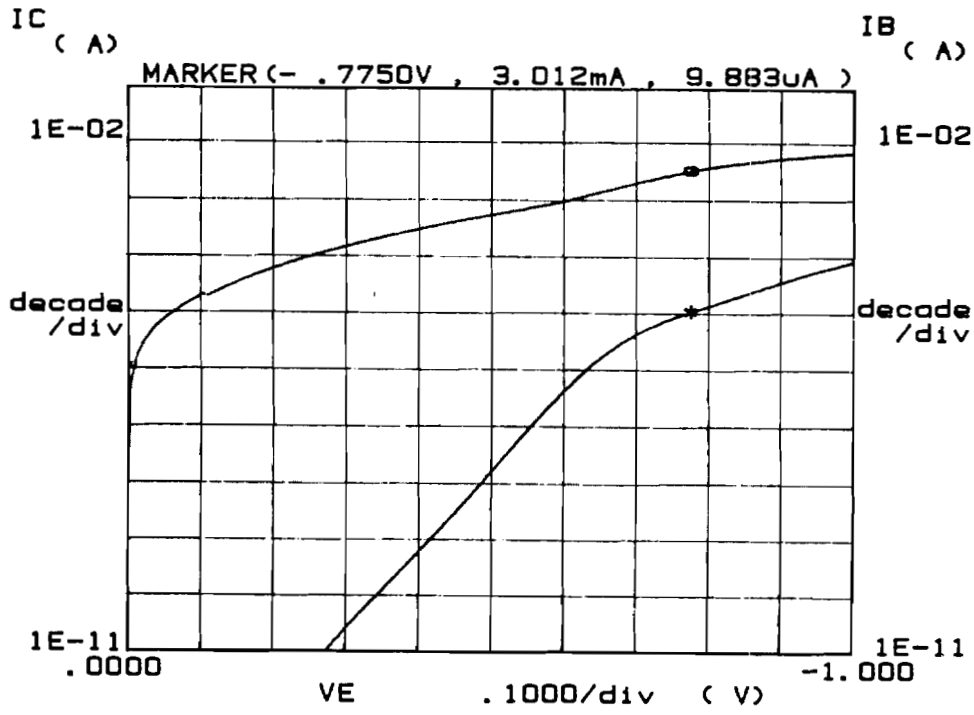
amount of emitter-collector leakage current was present as seen in a typical substrate device Gummel plot of Figure 5.15(a). Finally, a current gain higher than 60 was desired for demonstration of material quality capable of reasonable BJT characteristics.

A set of 10 different wafers were processed as seen in Table 5.6 to investigate the baseline NPN process on simple substrate BJTs. Table 5.6 details only the parameters of the process which were altered in the experiment. A base oxidation/drive of 15 minutes at 1000 ° C in wet oxygen was perfornned on all the wafers immediately following the base implant. Similarly, all wafers received the same emitter implant dose of arsenic at $3x10^{15}cm^{-2}$ and 25 KeV acceleration. Contacts were etched following the emitter oxidation/drive and 1000-2500Å of Al-1%Si was sputter deposited and alloyed at 415 ° C, except for wafer#1 which was alloyed at 450 ° C.

The first wafer's emitter/base short problem was solved in the next group of wafers by driving the emitter slightly deeper with a 20 minute oxidation/drive, and by using a lower metal alloy temperature of 415 ° C to reduce sintering into the emitter. However, wafers #2 and #3 still exhibited unacceptable emitter-collector leakage. There were only two reasonable explanations for this large leakage current. The first, crystal dislocations leading to emitter-collector pipes, was ruled out due to the use of high quality substrate wafers. Thus, the leakage must have been caused by a surface N-type channel through the base region. This condition is caused by the opposite nature of dopant segregation with phosphorus and boron. Boron from the extrinsic base segregates into the oxide and tends to deplete the boron concentration at the surface oxide/silicon interface. Oppositely, the background phosphorus doping of the wafer tends to accumulate at the oxide/silicon interface. If the phosphorus concentration exceeds the boron base concentration at the surface, a leakage path is formed between the emitter and collector.

First, wafers #4 and #5 were processed with all diffusions performed in the relatively dopant free H_2 Burn tube instead of the highly phosphorus contaminated Phosphorus Drive tube. This produced a roughly 3:1 recluction in the leakage current between wafers #4 and #2. However, the leakage current was still far above usable limits. Next, wafers #6 and #7 were processed with lower boron implant energies, 25 KeV, and #7 received a heavier $6x10^{13}cm^{-2}$ boron

(a)



(b)

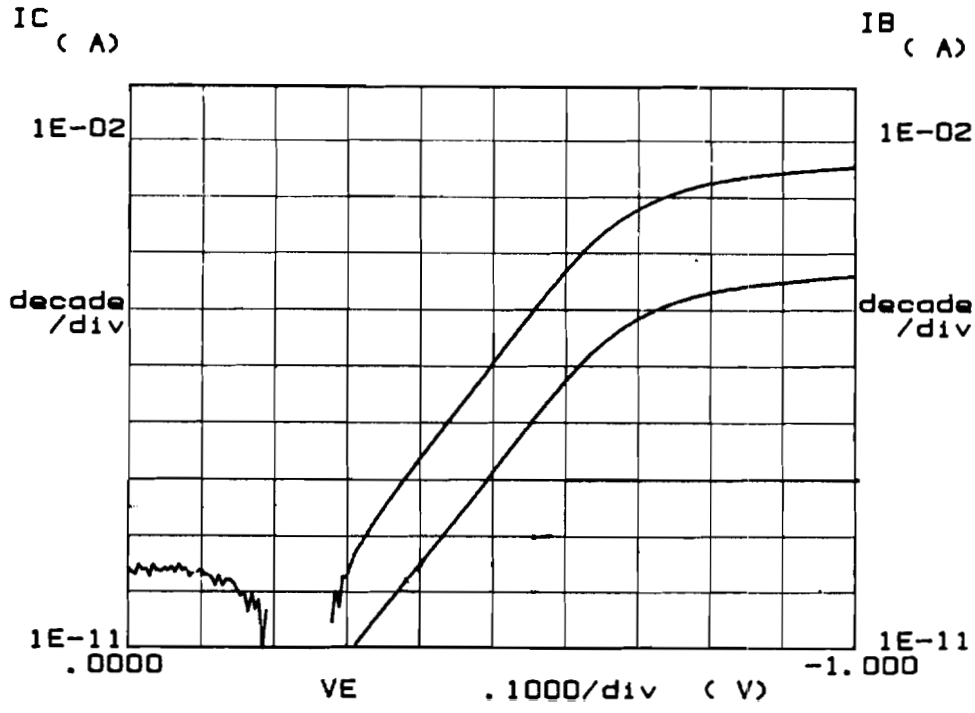


Figure 5.15. Gummel plots of typical NPN substrate transistors fabricated with processes listed in Table 5.6: (a) Wafer #3, (b) Wafer #10.

Table 5.6. Summary of Process Variations Made to the Baseline NPN Process.

Wafer #	B11 Impl. #/cm^2-KeV	Emit. Drive wetO_2	Tubes Used	PR Imp?	Results J_{eco}(A/cm^2)	Results β_{max}
1	4313-50	15m-1000C	2&3	Yes	E/B Short	34
2	3313-35	20m-1000C	2&3	Yes	6.1	70
3	3313-35	30m-1000C	2&3	Yes	60	150
4	3313-35	20m-1000C	4	Yes	1.8	150
5	3313-50	20m-1000C	4	Yes	3.7	80
6	3313-25	20m-1000C	4	Yes	1.2	125
7	6E13-25	20m-1000C	4	Yes	0.2	62
8	1314-25	30m-1000C	4	Yes	12	63
9	2314-25	30m-1000C	4	Yes	1.4	33
10	6313-25	20m-1000C	4	NO!	0.001	80

implant dosage. Once again, the leakage was reduced, but still not below acceptable limits. Finally, wafers #8 and #9 were processed with even higher boron implant dosages, $1x10^{14}$ and $2x10^{14}cm^{-2}$. A longer emitter oxidation and drive of 30 minutes was used to combat the wide base widths and lower gains expected with. the larger boron implant dosages. Emitter-collector leakage increased in these wafers, completely against expectations.

One last change was made in the NPN device process. Standard AZ1350J-SF photoresist had been used throughout and developed with AZ developer. Following the wet BHF etch of the underlying oxide, the photoresist was left on the wafer during the base and emitter implants to provide additional masking against the implant. Wafer #10 was processed identically to #7, except that following the BHF etch of the base and emitter oxide openings, the resist was removed and

a piranha clean performed prior to the implants. In wafer #10, the emitter-collector leakage current was reduced by a factor of 200 over the resist implanted wafer #7. A normal Gummel plot could finally be obtained as seen in Figure 5.15(b), and the true cause of the leakage current was now known. AZ developer is a sodium based chemical which is known to leave sodium contamination in the developed resist film. It is suspected that the heavy dosage emitter implant was driving sodium ions into the underlying base oxide. During the 20 minute 1000" C emitter diffusion, sodium diffused down to the oxide/silicon interface and easily caused an N-type inversion channel to form at the silicon surface. This N-type channel was the cause of the extraneous emitter-collector leakage current.

5.3.3 ELOBJT-3 NPN Devices

Having now solved the substrate device leakage current problem, ELOBJT-3 devices could be processed. Having already estbblished the self-aligned device concept with the PNP devices detailed in section 5.3.1, the simplified non-self-aligned process detailed in section 4.2.6 was used for fabrication of the NPN ELOBJT-3 physical device structure. Then, the NPN process :sequence developed in wafer #10 of Table 5.6 was used to form the base and emitter regions of the BJT device, with one exception. The base implant dosage was lowered to $5x10^{13}cm^{-2}$ from $6x10^{13}cm^{-2}$ to give slightly higher current gains than the 80 produced in wafer #10.

The first wafer was processed with a standard lithographically defined emitter region spaced approximately 0.5 μm inside the SEG/bottom oxide sidewall interface. However, because of the sharper emitter diffusion corners compared to the more rounded shape of the SEG trench definition, the emitter diffusion lied directly over the SEG edge in the corners. Data from ELOBJT-3 devices was compared to data from devices fabricated in large area bulk SEG material, all processed side by side on the same wafer. A summary of device measurement results averaged over 5 typical devices is shown in Table 5.7.

The ELOBJT-3 devices showed slightly lower quality forward bias ideality factors of 1.16 for the emitter/base junction in comparison to 1.04 for the bulk SEG devices. Reverse leakage current densities were all within about the same range of $1-5x10^{-5}A/cm^2$. These results would seem to indicate that spacing the emitter diffusion edge in slightly from the SEG edge would :produce reasonable

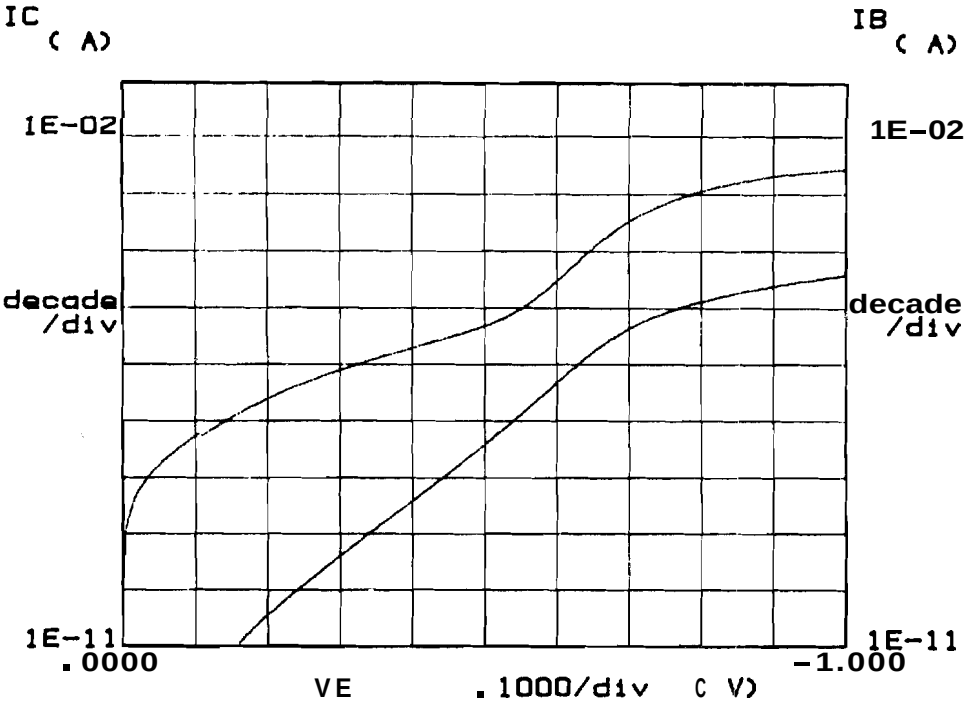
Table 5.7. Summary of Measured Data From ELOBJT-3 NPN and Bulk SEG Monitor Transistors. Averages are Taken Over 5 Devices.

Parameter	Average ELOBJT-3	Best ELOBJT-3	Average Bulk SEG
η_{be}	1.16	1.11	1.04
J_{ebo}@3V(A/cm^2)	1.3×10^{-5}	0.8×10^{-5}	5.6×10^{-5}
η_{bc}	1.09	1.07	1.08
J_{cbo}@3V(A/cm^2)	1.4×10^{-5}	1.1×10^{-5}	4.5×10^{-6}
J_{ceo}@4V(A/cm^2)	4.7	2.8	0.01
β_{max}	86.5	121	130

quality emitter/base junctions. Next, the base/collector junctions showed identical forward ideality factors as the bulk SEG monitor devices, and reverse leakage current densities were within a factor of 3 of the bulk SEG devices. This data indicates that placement of the base/collector junction up and away from the SEG/bottom oxide sidewall as proposed in Figure 3.1 does minimize the effect of SEG/oxide sidewall defects on the base/collector junction. Finally, lower average current gains of 86.5 were obtained for the ELOBJT-3 devices in comparison with 130 for the bulk SEG devices. Since the bulk SEG material is probably of equal quality in both devices, increased edge defects in the ELOBJT-3 devices must account for the lower current gains. However, the material was of sufficient quality for fabrication of BJTs with current gains as high as 121.

Although both emitter/base and base/collector junctions seemed of reasonable quality in the ELOBJT-3 devices, one major problem was holding back normal BJT operation. All ELOBJT-3 devices exhibited sizable emitter-collector leakage currents which prevented normal operation in the low current region as seen in the Gummel plot of Figure 5.16(a). A Gummel plot of a similar sized bulk SEG device is shown in Figure 5.16(b) where no emitter-collector leakage is

(a)



(b)

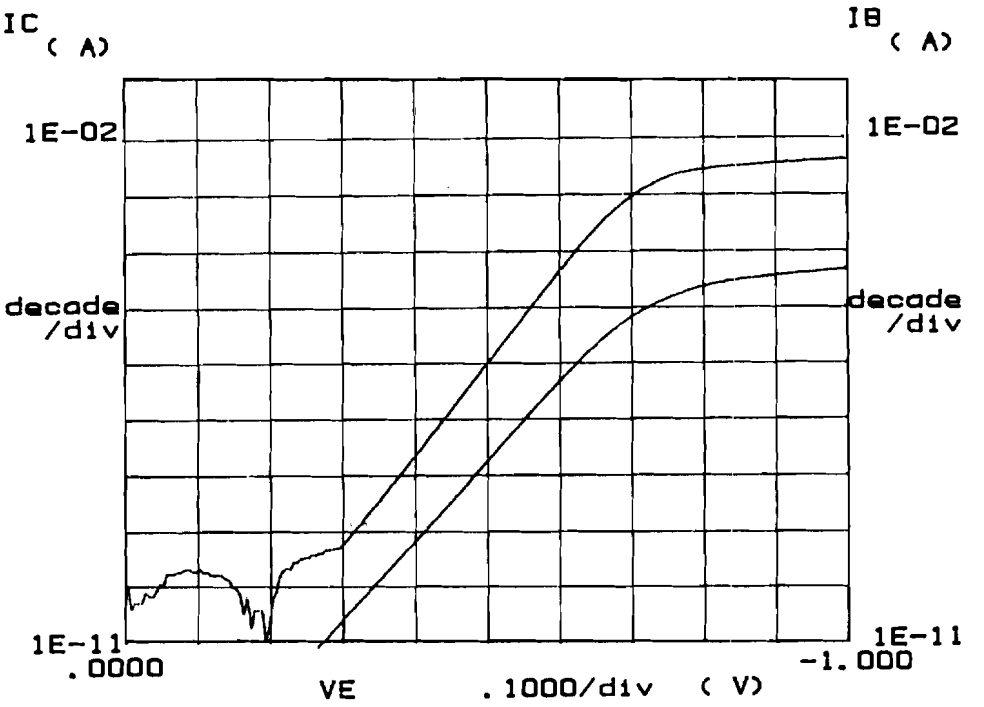


Figure 5.16. Gummel plots of typical NPN transistors: (a) ELOBJT-3 device, and (b) bulk SEG device. Both devices have identical emitter areas of 1760 μm^2.

evident. The leakage in the ELOBJT-3 devices was probably caused by emitter-collector diffusion pipes formed at material dislocations at the SEG/oxide sidewall edge. Diffusion pipes in bipolar transistors are characterized by local. retardation of the boron base diffusion in conjunction with accelerated arsenic emitter diffusion, causing conduction paths from the emitter to the collector through the base as seen in Figure 5.17. Pipes are generally caused by crystal dislocations and

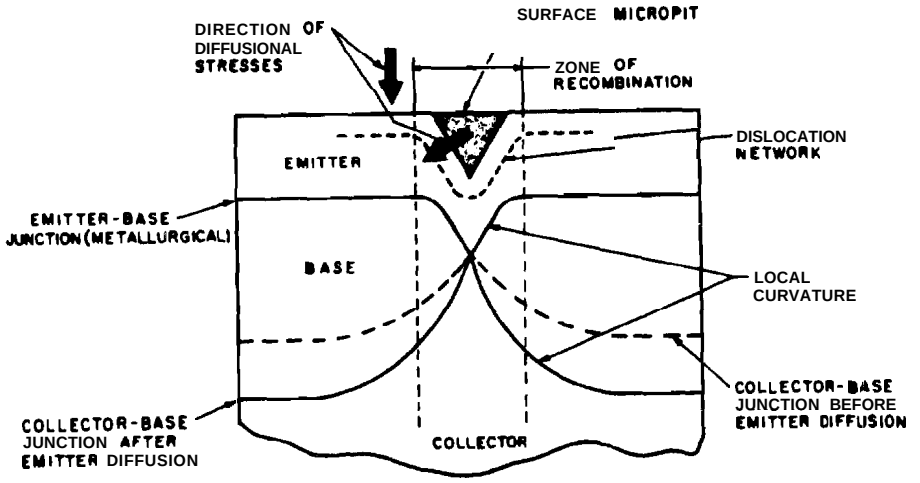


Figure 5.17. Diagram of emitter-collector diffusion pipes in a bipolar transistor caused by a dislocation defect.[4]

frequently exhibit non-linear resistive behavior. It is curious however that both junctions could display nearly ideal single junction behavior, yet low current bipolar device operation was not possible due to emitter-collector leakage pipes.

Measurements were taken to establish the location of the emitter-collector leakage problem. Devices were included in each die which had identical emitter areas of 1760 μm^2, but different perimeter lengths ranging from 168 to 600 pm.

Approximately 60 devices of each type were tested for emitter-collector leakage at V_{ce}=4 volts. The average values for each perimeter length are plotted in Figure 5.18 where leakage current magnitude is seen to scale linearly with perimeter

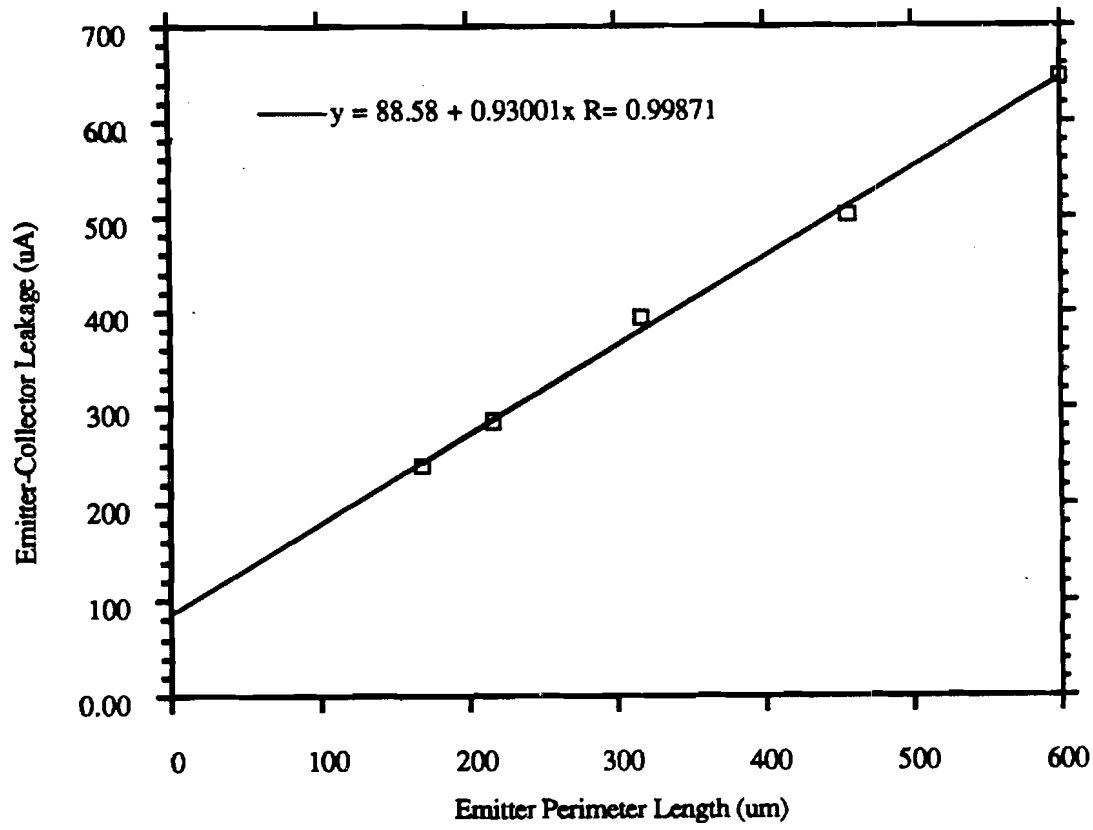


Figure 5.18. Plot of emitter-collector leakage versus emitter perimeter length. All devices have identical emitter areas of 1760 μm^2.

length. The normal leakage current expected for all the devices having the same emitter area, $I_{eco}=I_{cbo}(\beta+1)$, is roughly 22 nA. Therefore, the Y-intercept leakage current value of 88.6 @ is probably the constant leakage associated with the four emitter corners preseht in all the devices. The correlation of average leakage data with perimeter length identifies the pipe location at the ledge of the emitter, near the SEG/oxide sidewall.

A final ELOBJT-3 wafer was processed using an alternate mask for the emitter diffusion. The mask spaced the emitter approximately 1.5 μm inside the

SEG/oxide sidewall edge, about 1 μm further than the previously processed wafer.. Table 5.8 summarizes the measured data from this wafer which produced

Table 5.8. Summary of Measured Data From ELOBJT-3 NPN Devices With Emitter Diffusion Spaced 1.5 μm Inside the SEG/Oxide Sidewall. Averages are Taken Over 6 Devices.

Parameter	Average ELOBJT-3	Best ELOBJT-3
η_{be}	1.03	1.00
J_{ebo}@3V(A/cm^2)	4.1x10^{-4}	1.0x10^{-4}
η_{bc}	1.03	1.00
J_{cbo}@3V(A/cm^2)	8.8x10^{-7}	4.5x10^{-7}
J_{ceo}@4V(A/cm^2)	0.2	0.1
β_{max}	65	90

remarkably well functioning ELOBJT-3 devices. Unfortunately, bulk SEG monitor clevices were not functional due to the alternate emitter mask used. Both emitter/base and base/collector junctions exhibited excellent forward ideality factors of 1.03 or less as shown by typical forward bias diode curves of Figure 5.19. Base/collector reverse leakage current densities were also improved over the previously processed wafer, with an average value of 8.8x10^{-7}A/cm^2. Emitter-collector leakage currents were reduced by a factor of 23 which was sufficient to allow normal low current operation of the devices as seen in the Gummel plot of Figure 5.20. Common emitter collector curves modulated with 500 nA base steps show quick turn-on and an Early voltage of approximately 15 volts as seen in Figure 5.21(a). Typical maximum current gains of 65 were obtained over 5-6 decades of collector current as shown in Figure 5.21(b). Overall, the devices exhibited normal BJT operation with characteristics similar to the bulk SEG devices listed in Table 5.7.

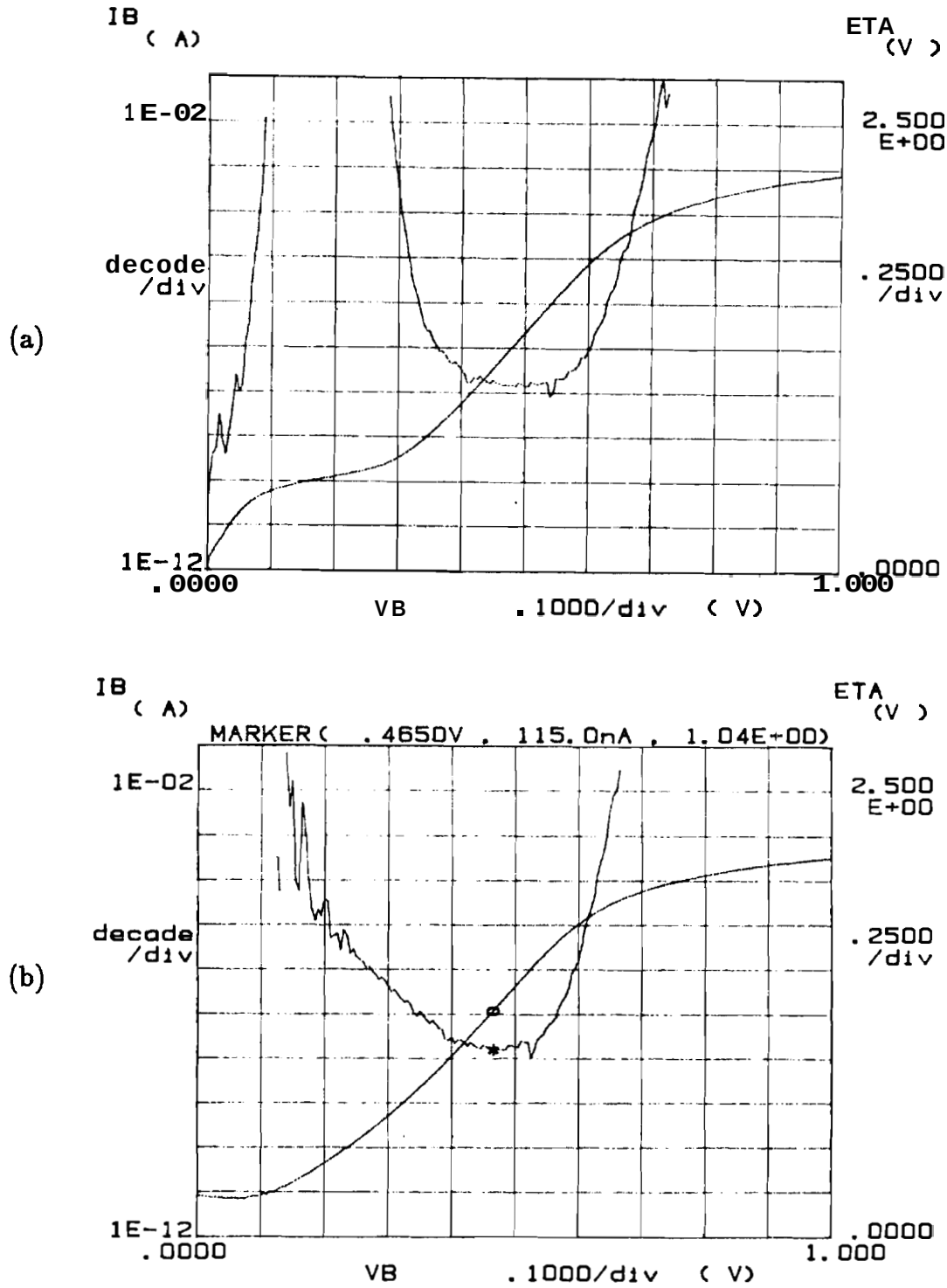


Figure 5.19. Forward bias characteristics of typical ELOBJT-3 devices with emitter spaced 1.5 μm from SEG edge: (a) emitter/base, (b) base/collector. Instantaneous ideality factor is also shown.

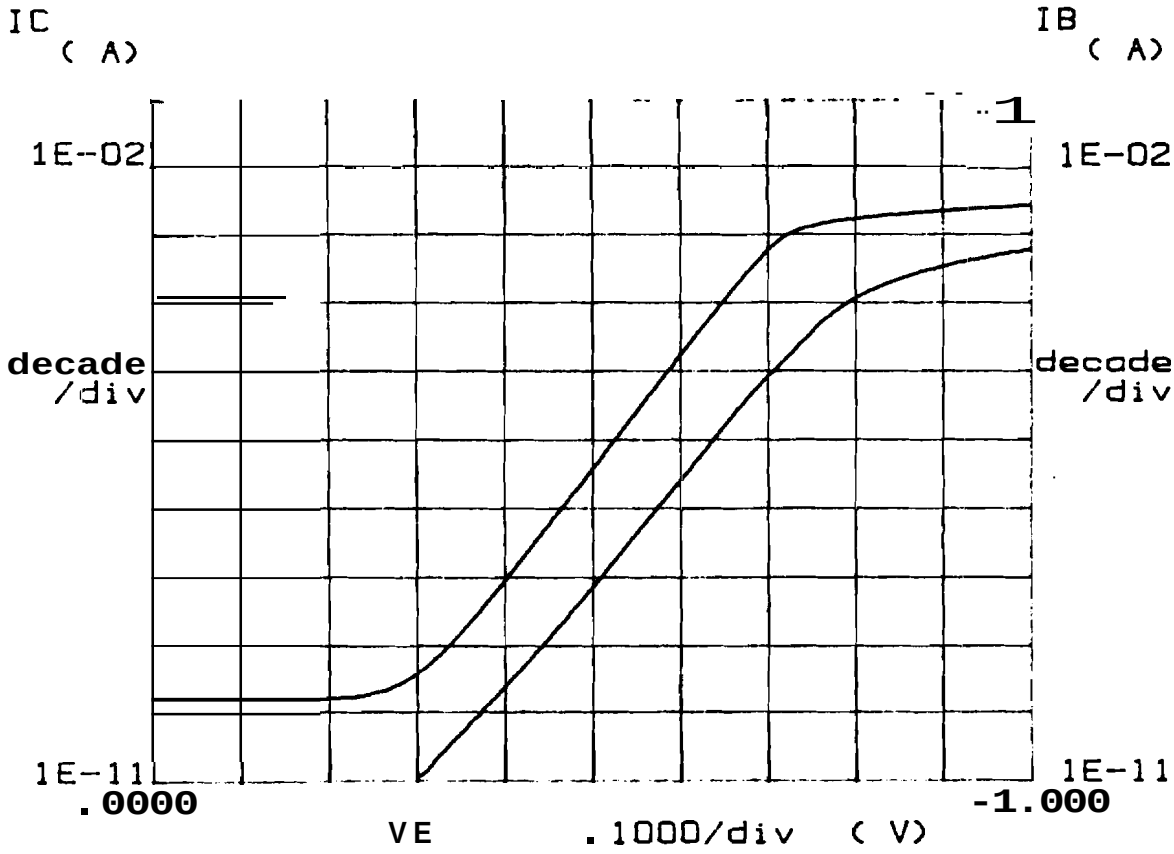


Figure 5.20. Gummel plot of typical ELOBJT-3 device with emitter spaced 1.5 μm from SEG edge.

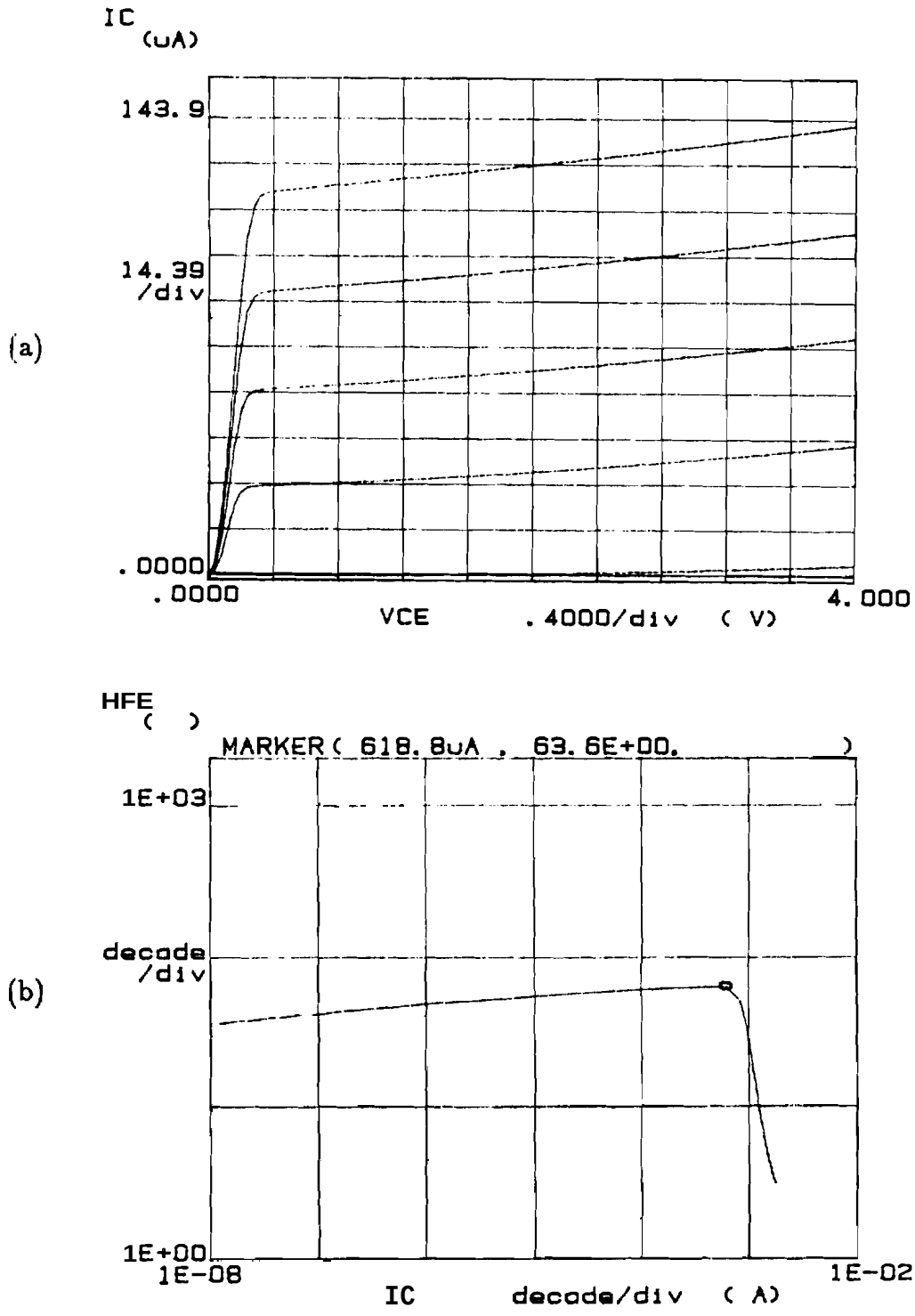


Figure 5.21. Modulation characteristics of typical ELOBJT-3 device with emitter spaced 1.5 μm from SEG edge: (a) common emitter collector curves, (b) current gain versus collector current.

5.4 Summary

Capacitance and resistance data from fabricated ELOBJT-3 devices was shown to scale in width and length, validating the computer simulations of Chapter 3. A new dynamic method of measuring extrinsic base resistance was used to independently validate the R_{bx} test structures and simulations. Finally, actual ELOBJT-3 devices were fabricated and tested and found to exhibit reasonable device characteristics except for unwanted emitter-collector leakage currents. It was established that the leakage currents were originating at the perimeter of the emitter near the SEG/oxide sidewall. However, it was found that the leakage currents could be reduced below acceptable limits by moving the emitter region away from the SEG/oxide sidewall. In this way, ELOBJT-3 devices with junction ideality factors of 1.03 or less were obtained with DC current gains up to 90.

5.5 References

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4. K.V. Ravi, Imperfections and Impurities in Semiconductor Silicon, pp. 262-278, Wiley Interscience, New York, NY, 1981.

CHAPTER 6 - CONCLUSIONS & RECOMMENDATIONS

6.1 Conclusions

The objective of the proposed research project was the development of a novel advanced high-speed bipolar transistor structure, utilizing selective and confined lateral epitaxial growth. The significance of the project was to produce a new high-speed bipolar structure with significantly reduced parasitics, as well as advance the state-of-the-art in SEG/CLSEG technology. A side issue was establishing the usefulness of computer simulations in predicting the fabrication and operation of a new bipolar process and device.

A suitable trench etch technique was developed using a combination of RIE and wet BHF etching, and aqueous KOH was employed for etching the CLSEG cavity. SEG was grown within the central trench and followed by 8-10 μm of 'horizontal CLSEG growth seeded off the SEG sidewall. This is the first known instance of CLSEG growth from a vertical SEG sidewall, not a substrate surface. The ELOBJT-3 self-aligned pedestal structure was therefore successfully produced even though the trench profile was not optimized due to insufficient RIE equipment. A further development was the growth of CLSEG within an all oxide cavity without the use of nitride as a top cavity material. However, when nitride was used, a technique was developed for passivating the RIE etched nitride which virtually eliminated the frequently encountered problem of nucleation and clogging at the via holes.

Although the ELOBJT-3 would logically be built as an NPN for ultimate high-speed applications, the structure was first built in the PNP configuration to establish feasibility of the ELOBJT-3 self-aligned sidewall contacted structure. N+ doped CLSEG was grown for the PNP's extrinsic base, and a self-aligned emitter was implanted into the top of the central SEG trench. The PNP devices established the feasibility of the self-aligned ELOBJT-3 structure although low

current gains were present due to a wide, non-graded base doping. Next, a series of NPN devices were built in the simplified ELOBJT-3 structurt: with current gains up to 90 due to a thin graded base doping. Results showed acceptable single junction characteristics even when the base/emitter junction was spaced down to 0.5 μm from the SEG sidewall. However, dislocations and defects at the edge produced emitter-collector leakage currents which spoiled the BJT' device operation. It was found that movement of the base/emitter junction 1.5 μm from the SEG sidewall edge significantly reduced the leakage current and produced ideally functioning ELOBJT-3 devices. Finally, it was found that the reported problems with base/collector junctions located at SEG sidewalls could be avoided by moving the junction out of the sidewall area as seen in Figure 3.1.

The final task involved correlating the measured DC parameters of the fabricated devices with predicted values provided by computer simulation. C_{cb} capacitance and R_{bx} resistance data from fabricated ELOBJT-3 devices was shown to closely scale in width and length with computer predictions, validating the usefulness of the computer simulations for predicting device parameters. In addition, a new dynamic method of measuring extrinsic base resistance was used to independently validate the R_{bx} test structures and simulations. The parameter comparison simulations between similarly sized sub-micron ELOBJT-3 and SST devices predicted a 77%, 58%, and 43% improvement in R_{bx}, C_{cb}, and C_{cs}, respectively. Circuit simulations predicted the reductions in base/collector parasitics would produce a roughly 37% reduction in digital ECL circuit propagation delay.

6.2 Recommendations

Although feasibility of fabrication and operation has been shown for the ELOBJT-3 device, much work remains to be done. In the future, continued investigation should focus on the quantification of defects near the SEG/oxide sidewall interface. This problem area is crucial to all devices employing selective epitaxy technology, especially as device dimensions are shrunk into the submicron level. However, the results of this work seem to indicate that poor quality single junction characteristics in walled SEG applications is not the limiting factor in BJT device applications. Actually, enhanced diffusion and piping problems at the SEG/oxide sidewall is the most serious problem. Lower temperature SEG

growths, various annealing and passivation techniques, and different masking material etches need to be investigated for improvement of the SEG/oxide sidewall problem.

Finally, a sub-micron sized ELOBJT-3 device could be fabricated with the E-beam facility so that exact measured parameters could be matched to sub-micron scaled computer simulations. Eventually, a ring oscillator circuit could be built to test the actual circuit propagation speed and check its correlation with computer simulation. In the future, as selective epitaxy technology advances and t'he sidewall material problems are overcome, pedestal-type devices such as the ELOBJT-3 will become the ideal bipolar structures for high-speed circuits.

APPENDICES

Appendix A - Tspice ELOBJT-3 Device Input File

```
clear
title ECL Inverter String (ELOBJT-3)
autoprobe=on
autopage=on
circuit
vcc 1 0 v:dc=3.0
vref 2 0 v:dc=2.0
vcs 3 0 v:dc=1.226
vin 4 0 v:dc=dcin tran=pulse(1.0 3.0 100p 5p 5p 1500p 3000p)
;gate #1 and 2 are drive gates
gate1 1 2 3 4 5 inv
gate2 1 2 3 5 6 inv
;gates #3-7 are averaging gates
gate3 1 2 3 6 7 inv
gate4 1 2 3 7 8 inv
gate5 1 2 3 8 9 inv
gate6 1 2 3 9 10 inv
gate7 1 2 3 10 11 inv
;gate #8 is load gate
gate8 1 2 3 11 12 inv
rload 12 0 r:r=50k
;*****************************************************************
;inverter gate
model inv subckt: nodes=(1,7,8,6,9)
r1 1 2 r:r=625
r2 1 3 r:r=625
r3 5 0 r:r=500
r4 9 0 r:r=50k
q1 2 6 4 6 elobjt3
q2 3 7 4 6 elobjt3
q3 4 8 5 6 elobjt3
q4 1 2 9 6 elobjt3
;*********************************************
;model for ELOBJT-3 0.35u X 4u emitter high frequency
;bipolar device from PISCES simulations.
model elobjt3 subckt: nodes=(1,2,3,4) $
kelvin=temp+273.160 $
rat=(temp+273.160)/300.16 $
k=1.38e-23 $
q=1.6e-19 $
eg=1.160 $
nlvje=350.000m $
nlmje=400.000m $
eg1=1.160-(7.02e-4*(temp+273.160)^2)/(temp+273.160+1108) $
tcrepi=5.796m-11.760u*temp
x1 1 2 3 4 level1
;----------------
model level1 subckt: nodes=(1,2,3,4) $
arg=-3*(k*kelvin/q)*log(rat)+eg1-1.1151*rat $
ist=2.53e-17*(rat^3)*exp(q*eg*(rat-1)/k/kelvin) $
```

```
rct=1+tcrepi*(temp-27) $
tft=exp((temp-27)/(90-27)*log(19.000p/16.000p)) $
xtft=exp((temp-27)/(90-27)*log(5.000/3.000)) $
itft=exp((temp-27)/(90-27)*log(364.000u/45.796m)) $
vtft=exp((temp-27)/(90-27)*log(400.000m/1.000))
x2 1 2 3 4 level2
;-----------------
model level2 subckt: nodes=(1,2,3,4) $
vt=log(ist)/log(2.53e-17)-arg/rat/nlvje
x3 1 2 3 4 level3
;-----------------
model. level3 subckt: nodes=(1,2,3,4)
ql 6 5 3 z15
;the extrinsic parasitic parameters
rbx 2 5 r: r=76 tc1=0
rcx 1 6 r: r=80 tc1=5.796m
dsub 4 6 s15: state=off
Ccbx 5 6 c: c=0.7f
;finally the actual gummel-poon 2 model, all intrinsic parameters
model z15 gp2: pol=npn $
cje=2.9f/(1+nlmje*(4e-4*(temp-27)+1-rat-arg/vt/nlvje))/rat $
cjc=0.46f $
re=12.5 rb=84 rc=rct*375.5 $
ikf=20.902m ikr=9.256m is=2.53e-17 bf=100 xtb=1.9 $
br=2.5 vaf=18.7 var=4 $
ise=5.051f isc=2.53e-17 ne=2 nc=2 tf=tft*9.3p $
xtf=xtft*3.000 vtf=vtft*1.000 itf=itft*45.796m ptf=25.000 $
tr=1.200n vje=vt*0.350015 mje=0.4 vjc=0.65 mjc=0.4 $
eg=1.16 xti=3 kf=6.6e-16 af=1 fc=0.35
;more parasitic devices (diodes) added extrinsically to device
;parasitic substrate/collector capacitance
model s15 d: is=1e-29 cjo=4.48f pb=0.65 $
m=0.4 eg=1.16 pt=3 rs=200.000
endm level3
endm level2
endm level1
endm elobjt3
;*********************************************
endm
;************************************************************
endc
```

Appendix B - TSUPREM-4 Input File for ELOW-3 Process

```
Comment ELOBJT-3 Process Simulation 05AUG90
Comment The real full process w/ output in pisces readable mesh file
Comment changed from in8-poly layer not simulated, removed poly diff
Comment Changed to remove heavy N+ doping at base CLSEG contact
Comment Changed from in11 to make process more realistic
Comment Changed from in12 to make boron diffuse farther in active area
Comment from CLSEG region, and make intrinsic base and emit impl deeper.
Comment changed from in13 by mving implants back after CLSEG and using
Comment a pr mask.

Comment Preliminary set-up.
option  echo device=4100

Comment Grid definition:
line    x loc=0 spacing=0.025 tag=left
line    x loc=0.6 spacing=0.025 tag=mid
line    x loc=1.1 spacing=0.025 tag=right
line    y loc=0 spac=0.1  tag=top
line    y loc=0.5 spac=0.3 tag=bottom

Comment Now define the entire structure as silicon
:region silicon xlo=left xhi=right ylo=top yhi=bottom

Comment Define substrate (buried layer) doping.
initial <100> phosph=1e19

Comment Deposit the SEX; pedestal layer
Comment Easier to deposit 1.1, and etch off 0.1 to get final 1.0 height
deposit silicon thick=1.1 spaces=44 phos=1e16 conc

Comment Etch roam on right side for oxide/clseg/oxide/nitride stack
etch start x=0.5 y=-2
etch continue x=0.5 y=0.0
etch continue x=2 y=0.0
etch done x=2 y=-2

Comment deposit the bottom oxide of the oxide/clseg/oxide/nitride stack
deposit oxide thick=0.5 spaces=20
deposit oxide thick=0.6 spaces=12

Comment etch off oxide and excess Si from top of seg structure
etch oxide start x=0 y=-1.1
etch continue x=2 y=-1.1
etch continue x=2 y=-3
etch done x=0 y=-3
etch silicon start x=0 y=-1
etch continue x=2 y=-1
etch continue x=2 y=-3
etch done x=0 y=-3
```

```
Comment Simulate dopant diffusion during the pedestal SEX; growth.
diffuse time=10 temp=950 inert

Comment Save the structure to a file after SEX; growth diffusion.
structu outf=out14.str1

Comment Perform epi-cap oxide growth
method  erfc
diffuse time=20 temp=950 weto2

Comment Save the structure to a file after epi-cap oxide
structu outf=out14.str2

Comment etch off excess oxide to form the bottom oxide structure
etch oxide start x=0.5 y=-2
etch continue x=0.5 y=-0.4
etch continue x=2 y=-0.4
etch done x=2 y=-2

Comment deposit the main portion of the CLSEG
deposit silicon thick=0.35 spaces=14 boron=1e19 conc
etch silicon start x=0 y=-1
etch continue x=1.5 y=-1
etch continue x=1.5 y=-3
etch done x=0 y=-3
etch silicon start x=0.5 y=-2
etch continue x=0.5 y=-0.75
etch continue x=1.5 y=-0.75
etch done x=1.5 y=-2

Comment Deposit the top cavity oxide
deposit oxide thick=0.25 spaces=10
etch oxide start x=0.0 y=-1.05
etch continue x=0.5 y=-1.05
etch continue x=0.5 y=-1
etch continue x=1.5 y=-1
etch continue x=1.5 y=-2
etch done x=0.0 y=-2

Comment Deposit the overlying nitride (again)
deposit nitride thick=0.1 spaces=4
etch nitride start x=0.0 y=-1
etch continue x=0.5 y=-1
etch continue x=0.5 y=-2
etch done x=0 y=-2
etch nitride start x=0.0 y=-1.1
etch continue x=1.5 y=-1.1
etch continue x=1.5 y=-2
etch, done x=0 y=-2

Comment Deposit the rest of the CLSEG region (contact via)
etch. start x=0.8 y=-2
```

```
etch continue x=0.8 y=-0.75
etch continue x=1.8 y=-0.75
etch done x=1.8 y=-2
deposit silicon thick=0.35 spaces=7 boron=1e19 conc
etch silicon start x=0 y=-1
etch continue x=0.7 y=-1
etch continue x=0.7 y=-1.1
etch continue x=1.5 y=-1.1
etch continue x=1.5 y=-2
etch done x=0 y=-2

Comment Simulate CLSEG growth diffusion
cliffuse time=40 temp=950 inert

Comment Save the structure to a file
structu outf=out14.str3

Comment etch off epi-cap oxide
etch oxide start x=0.0 y=-0.9
etch continue x=0.5 y=-0.9
etch continue x=0.5 y=-3
etch done x=0.0 y=-3

Comment Perform base implant:
implant boron dose=1e13 energy=130 pearson

Comment Form sidewall spacer before emitter implant
deposit oxide thick=0.01 spaces=1
deposit nitride thick=0.15 spaces=6
etch    nitride dry thick=0.15

Comment use PR mask to protect base CLSEG contacts from emitter implants
deposit photores thick=1.5
etch photores start x=0.0 y=-0.9
etch continue x=0.7 y=-0.9
etch continue x=0.7 y=-3.9
etch done x=0.0 y=-3.9

Comment Perform emitter implant:
implant arsenic dose=1e16 energy=70 pearson
etch    photores all

Comment Perform dry etch to clear surface of any straggling uglies
etch    dry thick=0.01

Comment Perform epi-cap oxide growth
method  erfc
deposit oxide thick=0.001 spaces=1
diffuse time=20 temp=950 weto2

Comment Save the structure to a file after implant drive oxide
structu outf=out14.str4
```

```
Comment etch contacts
etch    oxide start x=0 y=-0.8
etch    continue x=0.34 y=-0.8
etch    continue x=0.34 y=-2
etch    done x=0 y=-2
etch    oxide start x=0.8 y=-1
etch    continue x=1.4 y=-1
etch    continue x=1.4 y=-2
etch    done x=0.8 y=-2

Comment deposit aluminum for contacts
deposit aluminum thick=0.05 spaces=2

Comment etch off aluminum in middle to delineate two distinct contacts
etch    aluminum start x=0.4 y=-0.8
etch    continue x=0.8 y=-0.8
etch    continue x=0.8 y=-1.8
etch    done x=0.4 y=-1.8

Comment Save the finished structure to a file
structu outf=out14.str5
structu pisces=out14.pis
```

Appendix C - Final ELOBJT-3 Process Sequence Run Sheet

ELOBJT-3 - Process Flow Sheet
Mask Set: JWS1 - Process: ED:bjt/xjs2/flow.1
Wafer Set - JWS29

Original: J. W. Siekkinen (11MAY92)

wafer #'s Date Step Completed

1) STARTING MATERIAL
   * 3 inch _-type ( ) _____ Ohm-cm <100> with flat on <110>
   # Date process flow started: _____
   # wafers:_____

2) COLLECTOR N+ IMPLANT
   * Implant Arsenic @ 25 keV, dose=1E14 cm**-2 x_____
   # Beam current:-----,-,-,--
   * piranha clean x_____

3) FIELD THERMAL OXIDE
   * Oxidation in Tube #2 (Phos) x_____
   - 60 min wet oxidation @ 1100 C
   Field color: _____/_____ (5400)

4) SEG SEED LITHOGRAPHY
   * Use Mask #JWS1-3, darkfield: x_____
   # HMDS, AZ-1350J resist-spin: 30sec @ 4000 RPM
   # Softbake: ____min @ ____C # Aligner:_____
   # Mode: ..... Exp: ____sec @ _____mW/cm**2
   # Develop: ____sec, 1:1 DI:AZ developer
   * BHF through field oxide: time:_____
   * 2xPirhanna clean (1:1 H2SO4:H2O2) x_____
   * BHF dip ____sec @ individual rinse x_____

5) CENTRAL PEDESTAL SELECTIVE EPITAXY
   - EPI PARAMETERS Target thickness: ____ microns
   # Date:_____ Run:_____ program:-,---,-,-
   # Bake:____min ____H2, ____DCS, ____HCl; ____C; ----T
   # Etch:____min ____H2, ____DCS, ____HCl; ____C; ____T
   # Grow:____min ____H2, ____DCS, ____HCl; ____C; ____T
   # Epi Height:_____ Oxide:_____A

6) CAVITY FORMATION
   * Oxidation in Tube #4 (H2 Burn Ox) x_____
   * - 15 min H2 burn oxidation @ 1000 C
   * a-Si LPCVD dep ~ 4000A x_____
   - _____min, ___sccm SiH4, ___mT, ____C
   * Oxidation in Tube #4 (H2 Burn Ox) x_____
   - 15 min H2 burn oxidation @ 900 C
   Polyox color: _____/_____ (690)
   * LPCVD Nitride Deposition - 1500A x_____

- _____min, ___DCS/___NH3, ___mT, ____C

7) CHEMICAL-MECHANICAL POLISH
   * RPM=_____, Force=_____lbs, Time=_____min x_____
 * Piranha Clean x_____

8) CAVITY POLY DEFINITION
   * Use Mask #JWS1-2, lightfield: x_____
      # HMDS, AZ_____ resist-spin: ....sec @ ____
 # Softbake: ____min @ ....C # Aligner:_____
 # We : ________, Exp: ____sec @ _____mW/cm**2
 # Develop: ____sec, __:__ DI:____developer
 # Postbake ____min @ C
 * RIE through nitride layer: x_____
 # ....min ....., ___W, __sccm,____mT, color.....
 * RIE thru oxide/poly layer, x_____
 # ....min,Fr115, 750W, ...sccm,____mT,color_____
 * remove resist with ACE,ACE,METH, DI, pirhanna (2:1) x_____

9) EPI CAP OXIDE AND CAVITY SIDEWALL
   * Oxidation in Tube #4 (H2 Burn Ox) x_____
 - 90 min dry oxidation @ 1100 C
 - 25 min wet oxidation @ 1100 C
 # Oxide color: _____/_____ (2784)

10) CLSEG VIA LITHOGRAPHY
   * Use Mask #JWS1-4, darkfield: x_____
 # HMDS, AZ_____ resist-spin: ....sec @ _____
 # Softbake: ____min @ 87__C # Aligner:_____
 # We : _____, Exp: 15.0sec @ _____mW/cm**2
 # Develop: ____sec, __:__ DI:____developer
 # Postbake _____

11) CAVITY VIA ETCH
 * RIE etch w/SF6 through top nitride: _____min x_____
 * BHF dip ____sec through thin oxide x_____
   * strip resist: ACE, Meth, pirhanna x_____
   * Oxidation in Tube #4 (H2 Burn Ox) x_____
 - 20 min dry oxidation @ 900 C
 * BHF dip 15__sec through very thin oxide x_____
 * Wet etch with EDP @ 90C--8-12 min:_____ x_____
 * Piranha Clean x2 x_____
 * BHF dip ____sec (____), x_____
 * Forever rinse, careful blow-dry x_____

12) CLSEG GROWTH
 - EPI PARAMETERS Target thickness: 8.0u
 # Date:_____ Run:_____ Program:_____
 # Bake:____min ....H2, ...DCS, ...HCl; ....C; ____T
 # Etch:____min ____H2, ____DCS, ____HCl; ____C; ____T
 # Grow:____min ____H2, ____DCS, ____HCl; ____C; ....T
 # Grow:____min ____H2, ____DCS, ____HCl; ____C; ____T

```
 #  Lateral Growth:_____ Oxide:_______A

13) EXCESS GROWTH REMOVAL
 *  SF6 RIE @ 500W: _________min                x_________
 *  CMP: RPM=_____, Force=_____lbs, Time=_____min    x_________
 *  ACE, Meth, Piranha Clean                     x_________

14) INTRINSIC BASE IMPLANT
     +  Implant Boron @ 25 keV, dose=5E13 cm**-2          x_________
      #  Beam Current:__________uA
 *  piranha clean                                x_________

15) BASE OXIDE AND DRIVE
     *  Oxidation in Tube #4 (H2 Burn)                    x_________
    -  15 min burn oxidation @ 1000 C
 #  Oxide color:     ________/________ (1275)

16) BACKSIDE ETCH
 +  AZ_______ resist-spin: ____sec @ _______ front!
 *  Postbake ____min @ ....C
 *  ______min SF6 RIE to remove nitride/poly          x_________
 *  remove resist, piranha clean                 x_________

17) EMITTER LITHOGRAPHY
     *  Use Mask #JWS1-6, darkfield:                      x_________
 #  HMDS, AZ_______ resist-spin: ....sec @
 #  Softbake: ____min @ ____C  #  Aligner:__________
 #  Mode: ________, Exp: ....sec @ _____mW/cm**2
 #  Develop: ____sec, ..... DI:____developer
 #  Postbake ....min @ ....C
     *  BHF etch to remove base oxide:_______min     x_________
 +  remove resist, piranha clean               x_________

18) EMITTER IMPLANT
 +  Implant Arsenic @ 25 keV, dose=3E15 cm**-2       x_________
       #  Beam current:__________
 *  piranha clean                                x_________

19) EMITTER DRIVE-IN
     +  Oxidation in Tube #4 (H2 Burn)                  x_________
    -  20 min wet oxidation @ 1000 C
 #  Oxide color:     ________/________ (2700A)

20) CONTACT LITHOGRAPHY (DO EXTRA EXPOSE WITH:#4!!!)
     +  Use Mask #JWS1-7, darkfield:                   x_________
 #  HMDS, AZ_______ resist-spin: ____sec @ _____
 #  Softbake: ____min @ ____C  #  Aligner:__________
 #  Mode: ________, Exp: ____sec @ _____mW/cm**2
 #  Develop: ____sec, ..... DI:____developer
 #  Postbake ____min @ ....C
 +  BHF etch thru base and emitter oxides:______min    x_________
 +  Strip resist (ACE, Meth, Piranha)            x_________
```

21) *METAL* LITHOGRAPHY
* Use Mask #JWS1-8, darkfield: x_____
# NO HMDS!!!!!
# AZ_____ resist-spin: ____sec @ -------
# Softbake: 15 min @ 85 C # Aligner:_____
# Mode: St, Exp: ____sec @ _____mW/cm**2
# Develop: ____sec, __:__ DI:____developer
* BHF dip 5sec x_____
- Do not look for dewet

22) METAL DEPOSITION
* Sputter deposit Al-1%Si x_____
- 40min, 100watts, 8mTorr
Metal thickness:_____

23) METAL LIFTOFF
* ACE in Glass beakers in Ultrasonic Cleaner x_____
- DI rinse

24) METAL ANNEAL
* Anneal in Tube #8 x_____
- 20 min N2 @ 415C (dial=400)!

Appendix D - PISCES-IIb ELOBJT-3 Input File

```
Title Simulation of ELOBJT-3 collector-base capacitance
Comment  Easy method-block uniform doping densities
mesh rect nx=64 ny=25 outfile=out1.msh
x.m n=l l=0
x.m n=8 l=2
x.m n=16 l=4
x.m n=40 l=12
x.m n=64 l=15
y.m n=l l=0
y.m n=8 l=0.4
y.m n=15 l=0.85
y.m n=25 l=3 r=1.15
Comment  N+ CLSEG Base Region
region num=1 ix.l=8 ix.h=40 iy.l=1 iy.h=8 silicon
Comment  Intrinsic Base Region
:region num=2 ix.l=40 ix.h=64 iy.l=1 iy.h=15 silicon
Comment  Collector Region
:region num=3 ix.l=1 ix.h=64 iy.l=15 iy.h=25 silicon
Comment  Oxide Regions
:region num=4 ix.l=1 ix.h=40 iy.l=8 iy.h=15 oxide
region num=4 ix.l=1 ix.h=8 iy.l=1 iy.h=8 oxide
Comment  Assign electrodes
elec num=1 ix.l=1 ix.h=16 iy.l=1 iy.h=1
elec num=2 ix.l=1 ix.h=64 iy.l=25 iy.h=25
Comment  Assign doping to region
profile region=1 n-type n.peak=1e18 uniform
profile region=2 n-type n.peak=1e16 uniform
profile region=3 p-type n.peak=7e15 uniform
Comment  solve reverse bias DC analysis at Vcb=0.3V reverse bias since
symb newton carr=2
method rhsnorm xnorm autonr itlimit=70
models temp=300 conmob
log outf=out1.log
solve init v1=0 v2=0
Comment  Plot the depletion region at 0 volts
plot.2d crosses bound depl 1.b=3 1.d=4 dev=4100
log acfile=out1.aclog
solve v1=0 v2=0 elect=1 ac freq=1e5 vss=0.015 outf=out1.slva
solve v1=0.1 v2=0 elect=1 vstep=0.1 nsteps=18 ac freq=1e5 vss=0.015 terminal
Comment  Plot the depletion region
plot.2d crosses bound depl 1.b=3 1.d=4 dev=4100
solve v1=2 v2=0 elect=1 vstep=1 nsteps=9 ac freq=1e5 vss=0.015 terminal=1
solve v1=12 v2=0 outf=out1.slvb
Comment  Plot the depletion region at 12 volts
plot.2d crosses bound depl 1.b=3 1.d=4 dev=4100
solve v1=12 v2=0 ac freq=1e3 fstep=10 mult nfst=4 vss=0.015 terminal=1
end
```