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MODELING OF GROWTH RATES OF SELECTIVE EPITAXIAL GROWTH (SEG) AND EPITAXIAL LATERAL OVERGROWTH (ELO) OF SILICON IN THE SiH_2Cl_2 -HCL- H_2 SYSTEM

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MODELING OF GROWTH RATES OF
SELECTIVE EPITAXIAL GROWTH
(SEG) AND EPITAXIAL LATERAL
OVERGROWTH (ELO) OF SILICON
IN THE $\text{SiH}_2\text{Cl}_2\text{-HCl-H}_2$ SYSTEM

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TABLE OF CONTENTS

	Page
LIST OF FIGURES	v
LIST OF TABLES	ix
ABSTRACT	xi
1. INTRODUCTION	1
1.1 Background	1
1.2 Statement of Purpose	2
2. LITERATURE REVIEW	5
2.1 SEG/ELO: Technology and Applications	5
2.1.1 Novel Isolation Method	7
2.1.2 Silicon on Insulator(SOI)	7
2.1.3 3-D Insulated Gate Bipolar Transistor(3-D IGBT)	10
2.1.4 Quasi-Dielectric Isolated BJT(QDI-BJT)	11
2.1.5 ELO-BJT(Triple Self-Aligned BJT)	12
2.1.6 Bridge Type Piezoelectric Accelerometer	12
2.2 SEG/ELO: Mechanisms and Models for the DCS-HCl-H ₂ System	15
2.2.1 A Fundamental Model for Silicon Epitaxy	15
2.2.2 The DCS-HCl-H ₂ system: Constituents and Adsorbed Species	17
2.2.3 Effect of varying Gas Concentrations on SEG/ELO	20
2.2.4 Effect of varying Temperature on SEG/ELO	22
2.2.5 Effect of varying Pressure on SEG/ELO	22
2.2.6 Effect of varying Oxide Thickness and Coverage on SEG/ELO	23
2.2.7 Growth Rate Models for SEG/ELO	24
3. PROCESS CONSIDERATIONS	29
3.1 Reactor Description	29
3.2 Reactor Drift	32
3.2.1 Temperature Drift	32
3.2.2 Oxide Coverage/Thickness effect	33

	Page
3.2.3 Wafer Thickness	33
3.2.4 Mass Flow Controller Drift	34
3.3 :Process Steps	35
3.3.1 Oxidation	35
3.3.2 Photolithography	36
3.3.3 Selective Epitaxy	36
3.4 Measurement Techniques	37
4 1 Profilometer	37
3.4.2 Nomarski	37
4. MODELING OF GROWTH RATE OF SEG/ELO	39
4.1 Selection of Expression to Model Growth Rate of SEG/ELO Silicon	39
4.2 Fitting of Growth Rate Expression to Experimental Data	46
4.3 Application to TSUPREM4	54
4.4 Suggested Tuning Procedure for Individual Reactors	55
4.5 Modeling of Oxide Coverage Effect on Growth Rate	58
5. CONCLUSION	61
5.1 Summary of Work	61
5.2 Recommendations	62
APPENDIX	63
LIST OF REFERENCES	69

LIST OF FIGURES

Figure	Page
2.1 SEG/ELO and CLSEG	6
2.2 3-dimensional stacked CMOS inverter	8
2.3 Formation of Large Island/Full Wafer SOI	9
2.4 3-Dimensional Insulated Gate Bipolar Transistor	10
2.5 Quasi-Dielectric Isolated BJT(QDI-BJT)	11
2.6 ELO-BJT	12
2.7 Bridge Type Piezoelectric Accelerometer	13
2.8 a)Flat Top MELO b)MELO-Si Diaphragm	14
2.9 Variation of growth rates of Silicon epi with Temperature. A is surface reaction rate limited and B is mass transfer limited.	17
2.10 Thermochemical data for Si-H-Cl system for a) increasing temperature b) increasing HCl/DCS flow ratio	18
2.11 Nonselective Growth. Selective Growth. and Etch Regions	21
2.12 Effect of Masking Oxide Coverage on Selective Epitaxial Growth Profile	23
3.1 Reactor Cross section	30
3.2 Reactor Block Diagram	31
3.3 Overall Reactor Drift from Baseline Runs	35
3.4 Error due to Stylus Dimension in Profilometer Width Measurements . .	38
3.5 Facet Formation during ELO as seen through Nomarski	38

Appendix Figure	Page
4.1 Growth/Etch Threshold shift with pressure	42
4.2 Selectivity Threshold at 50 Torr: HCl/DCS=3	43
4.3 Selectivity Threshold at 100 Torr: HCl/DCS=4	43
4.4 Effect of Changing Hydrogen Partial Pressure on Growth Rate	44
4.5 Growth Rate Variation with Temperature at HCl=0 slpm	47
4.6 Choice of model to describe growth rate variation with HCl	49
4.7 Choice of model to describe growth rate variation with doubling of HCl, DCS flow rates	49
4.8 Fit of model to data: growth rate variation with HCl at 920°C, 40 Torr .	51
4.9 Fit of model to data: growth rate variation with temperature at 40Torr .	51
4.10 Fit of model to data: growth rate variation at 150 Torr	52
4.11 Fit of model to data: growth rate variation with temperature at 1.24 slpm HCl, 150 Torr	52
4.12 Fit of model to data: growth rate variation at 95 Torr	53
4.13 Fit of model to data: growth rate variation at 40 Torr	53
4.14 Approximation of ELO profile by growth rate model	54
4.15 Model Tuning Flow Chart	57
4.16 Comparison of Oxide Coverage model to normalised data	60
4.17 Variation of Growth Rate with Oxide Thickness at 150 Torr	60

Appendix Figure	Page
.1 Tube 1	65
.2 Tube 2	65
.3 Tube 3	66

Appendix Figure	Page
.4 Tube4	66
.5 Tube 5	67
.6 Tube6	67

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|

LIST OF TABLES

Table	Page
4.1 Variation in Critical Pressure with a change in Temperature	41
4.2 Effect of Doubling HCl,DCS Flows on Growth Rate, T=970°C,P=40 Torr,H ₂ =60slpm	45
4 . Tuneable Parameters and Default Values	55
4.4 Increase in Growth Rate with Oxide Coverage at P=150 Torr	58
Appendix	
Table	
.1 Oxidation Tube Function	63

ABSTRACT

Kongetira, Poonacha. MSEE., Purdue University, August 1994. Modelling of Selective Epitaxial Growth(SEG) and Epitaxial Lateral Overgrowth(ELO) of Silicon in $\text{SiH}_2\text{Cl}_2\text{-HCl-H}_2$ system. Major Professor: Gerold W. Neudeck.

A semi-empirical model for the growth rate of selective epitaxial silicon(SEG) in the Dichlorosilane-HCl-H₂ system that represents the experimental data has been presented. All epitaxy runs were done using a Gemini-I LPCVD pancake reactor. Dichlorosilane was used as the source gas and hydrogen as the carrier gas. Hydrogen Chloride(HCl) was used to ensure that no nucleation took place on the oxide. The growth rate expression was considered to be the sum of a growth term dependent on the partial pressures of Dichlorosilane and hydrogen, and an etch term that varies as the partial pressure of HCl. The growth and etch terms were found to have an Arrhenius relation with temperature, with activation energies of 52kcal/mol and 36kcal/mol respectively. Good agreement was obtained with experimental data. The variation of the selectivity threshold was correctly predicted, which had been a problem with earlier models for SEG growth rates. SEG/ELO Silicon was grown from 920–970°C at 40 and 150 torr pressures for a variety of HCl concentrations. In addition previous data collected by our research group at 820–1020°C and 40–150torr were used in the model.

1. INTRODUCTION

1.1 Background

Market forces have conspired to create a demand for better and faster electronic products at constantly cheaper prices. The semiconductor industry has met this challenge by an increase in volume production. This in turn has been made possible by a reduction in the minimum feature size, and an increase in integration density, and in wafer size. Currently 6"-8" wafers are in production, and minimum feature sizes of MOS transistors have shrunk to 0.5 μ m at some of the state of the art fabrication laboratories, with plans to attain 0.25 μ m devices.

Smaller devices would imply that device parasitics are decreased leading to faster response time and hence faster chips, computers etc. Smaller minimum feature sizes are governed in part by the isolation technology in use. It is generally accepted that Local Oxidation of Silicon(LOCOS) cannot be extended to the sub half micrometer range due to the bird's beak effect [1]. Alternative processes like trench isolation do provide finer linewidths with a high aspect ratio, but suffer from process complexity and thermal defect generation [2].

Silicon on Insulator(SOI) is another favoured technology not only with the capability to support small devices, but also with the promise of radiation hardness, immunity from latch up and lowered parasitic capacitances . A long range vehicle for an increase in integration density is 3-dimensional integration. This could take place with either 3-dimensional devices being fabricated on the substrate or as vertically stacked circuits formed in layers of silicon separated by amorphous Silicon Dioxide [3]

The importance of Selective Epitaxial Growth(SEG) and Epitaxial Lateral Overgrowth(ELO) of Silicon stems from the fact that the above goals of more efficient

isolation, SOI and 3-dimensional integration are all perfectly compatible with the technology of SEG/ELO [4, 5, 6, 7, 8]. Originally reported by Joyce and Bradley [25] in 1962, it has come a long way in terms of material quality, selectivity and surface morphology. Much of this is due to the reduced pressure epitaxial reactors used in the SEG/ELO process development. At small device sizes, it becomes necessary to have sharp doping profiles and therefore low thermal budgets in processing. SEG/ELO has been successful as a low temperature process ($T < 1000^{\circ}\text{C}$) when done at low pressures. Present Reduced Pressure Chemical Vapour Deposition (RPCVD) or Low Pressure Chemical Vapour Deposition (LPCVD) reactors operate between 800° – 1000°C temperature and 5–760 Torr pressure ranges. Good quality SEG Silicon has been achieved at temperatures as low as 550°C with the use of Ultra High Vacuum Chemical Vapour Deposition (UHVCVD) systems [10].

A parallel development, due to the effort to reduce fabrication costs, has been the reliance on computers to reduce cycle and development time. This takes the form of an ever increasing use of computer simulations in the use of fabrication process development and in device design. Faster computers with expanded memory capabilities have made it possible to run exhaustive simulations of fabrication processes. Device doping profiles, structures, and device electrical characteristics can be extracted without actually going through the fabrication process. These simulators give the process or device engineer a very good idea of where to begin and which parameters to vary to get close to the required device structure or performance. They allow the observation of how the fabrication process affects the device performance. Simulators are thus useful since they save a lot of iteration time, and lead to a better understanding of how the device works.

1.2 Statement of Purpose

The main objective of this work was to develop a model to predict closely the growth rate of Silicon when grown selectively in an environment of Dichlorosilane, Hydrogen Chloride, and Hydrogen, in a reduced pressure CVD reactor. It is desired

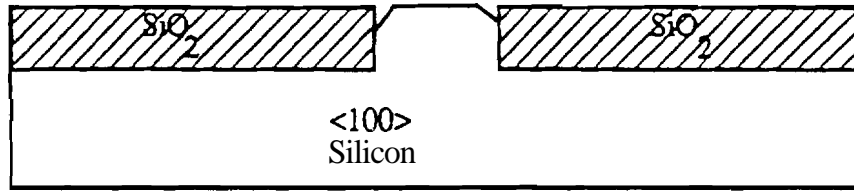
that the model be accurate but not very computationally intensive, so that it can be used in an application such as a commercial process simulator.

Selective epitaxial Silicon films will be deposited at various conditions of temperature and pressure and reactant gas concentrations. This will provide information towards the etching effect of HCL, the growth effect of Dichlorosilane and the variation of growth with temperature and pressure. An analysis of the (chemical reactions occurring in the Dchlorosilane-HCL-H₂ system has been performed. The dominant reactions have been used to formulate a kinetic expression relating the growth rate to the above mentioned process parameters. The experimental data collected, in combination with growth rate data taken previously by our research group, will be used to extract the rate parameters for the theoretical kinetic expression. The final expression should be the required model for Selective Epitaxial Growth.

2. LITERATURE REVIEW

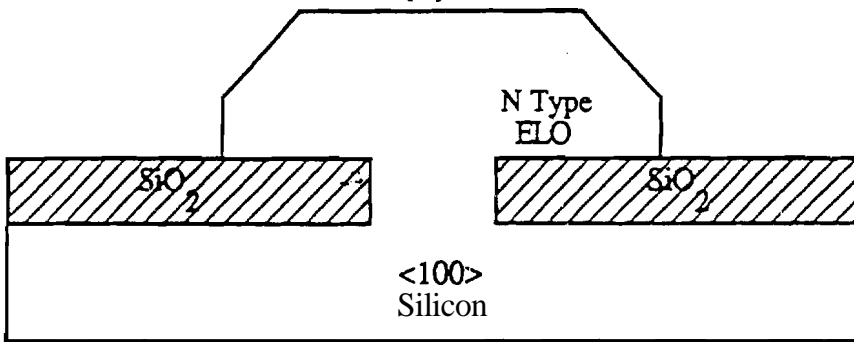
2.1 SEG/ELO: Technology and Applications

SEG is formed by opening seed windows on an oxidized Silicon substrate which is typically $\langle 100 \rangle$ in orientation. The seed window edges are aligned at 45° to the wafer flat, and are along the [100] direction. Epitaxial growth is initiated selectively in the seed windows on the exposed regions(Figure 2.1(a)). The growth is referred to as SEG when the Silicon is confined within the oxide walls, and until it reaches the level of the oxide. If the growth is continued, the Silicon grows out of the seed hole and laterally over the masking oxide to produce a single crystal layer of Silicon called Epitaxial Lateral Overgrowth(ELO). The vertical to lateral ratio of ELO is about unity, as illustrated in Figure 2.1(b). Thus ELO does not result in thin slabs of SOI. A Chemical Mechanical Polishing(CMP) process is used to planarize ELO to a desired final thickness. This works by taking advantage of the differences in etch rates between Silicon and either oxide or nitride. The oxide or nitride is grown or deposited on the wafer to a desired thickness, followed by SEG/ELO growth. The CMP process then is used to etch away the Silicon until the etch stop(oxide/nitride) is reached. At this point the etch rate decreases by as much as a factor of 20–50, effectively stopping the etch and leaving a thin layer of SOI. An alternative method of achieving thin films of SOI is Confined Lateral Selective Epitaxial Growth(CLSEG) [11] . A lateral cavity with the walls of oxide, and roof of nitride, is constructed over the seed window. Selective growth of Silicon is initiated. As usual SEG Silicon grows until the level of the oxide surface. Further growth of Selective Silicon leads to the cavity being filled as illustrated in



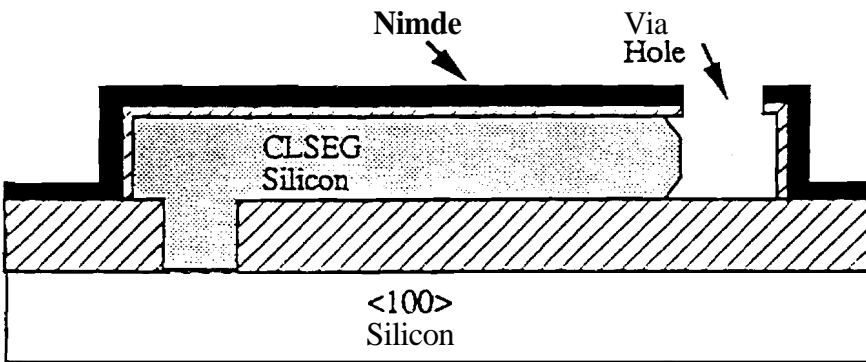
SELECTIVE EPITAXIAL GROWTH (SEG)

(a)



EPITAXIAL LATERAL OVERGROWTH (ELO)

(b)



CONFINED LATERAL SELECTIVE EPITAXIAL GROWTH (CLSEG)

(c)

Figure 2.1 SEG/ELO and CLSEG of Silicon [22]

Figure 2.1(c). When the nitride is stripped off, a layer of SOI remains which has the dimensions of the nitride cavity.

Several applications have been found for SEG/ELO in SOI, 3-dimensional devices and isolation techniques by our research group; some of which are detailed below.

2.1.1 Novel Isolation Method

Minimum feature sizes and integration densities are to a certain extent dependent upon the the isolation techniques used. The industry standard LOCOS is fast approaching its limits because of the well known “bird’s beak” effect. SEG provides an isolation method that does not suffer from the same limitations: [12, 13, 14]. Seed windows are opened in a thick field oxide covering the wafer. SEG is grown until the exposed surface is level with the surface of the wafer, providing device fabrication areas that are dielectrically isolated from each other. If the SEG does grow out of the seed windows, it can be planarised the field oxide acting as the etch stop. This technique is limited only by the resolution of the photolithographic technology available to produce sufficiently small seed windows.

2.1.2 Silicon on Insulator(SOI)

Most SOI technologies have not advanced much beyond the research stage because of the difficulty of forming quality single crystal Silicon over the amorphous insulating material. SEG/ELO is formed by selective nucleation of Silicon on the exposed bulk Silicon areas defined by the seed windows. ELO is formed again by selective nucleation on the SEG silicon. Thus at all times, nucleation is taking place on crystalline Silicon—resulting in device quality monocrystalline Silicon being formed over the insulator. The two approaches followed in obtaining SOI have been; a) device island SOI and b) full wafer/large island SOI.

a) Device Island SOI

SOI islands are formed with each island of SOI extending a few device areas over the insulator, with seeding being done individually for each device island. This has

been used to fabricate a CMOS inverter with the PMOS device stacked on top of the NMOS device with a shared gate sandwiched in between [15, 16]. A top gate can also be formed for the PMOS transistor. Since the PMOS transistor thus has two channels formed (top and bottom), the differences in hole and electron mobility are compensated for, without the need for a much larger PMOS transistor width. The 3-d stacked CMOS inverter is shown in Figure 2.2.

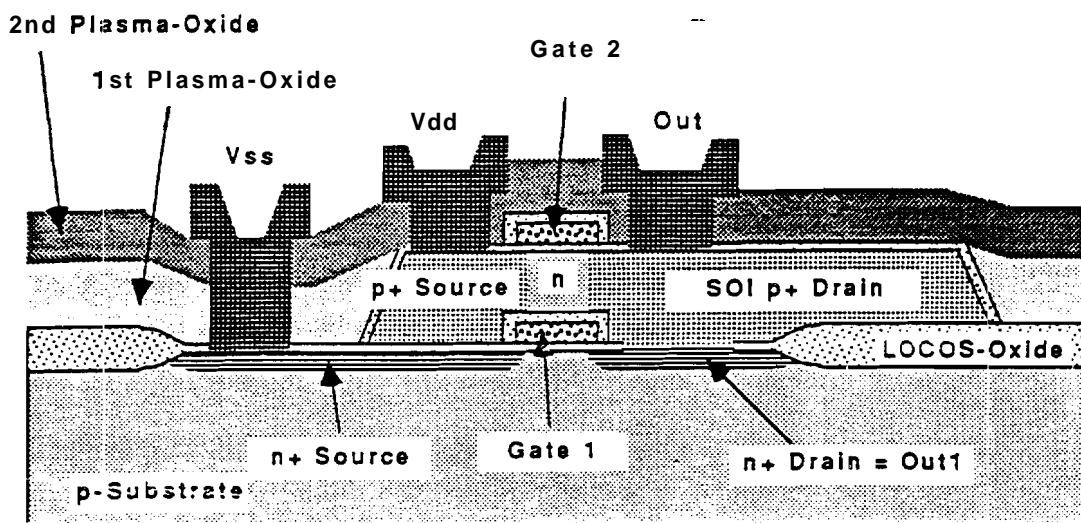


Figure 2.2 3-dimensional stacked CMOS inverter [15]

b) Large Island/Full Wafer SOI. Large island SOI can be achieved by the merging of ELO growth fronts from adjacent seed holes (Fig. 2.3(a-c)) [17, 18]. This is called Merged ELO (MELO). Full wafer SOI can be achieved by etching back the Silicon over the seed windows, to the level of the field oxide (2.3(d)). An oxidation is done that causes an oxide layer to form over the seed window area. The vertical sides of the etched back SOI are used as the seed for ELO. Selective deposition is done until the growth fronts merge, leading to full wafer SOI (2.3(e),(f)).

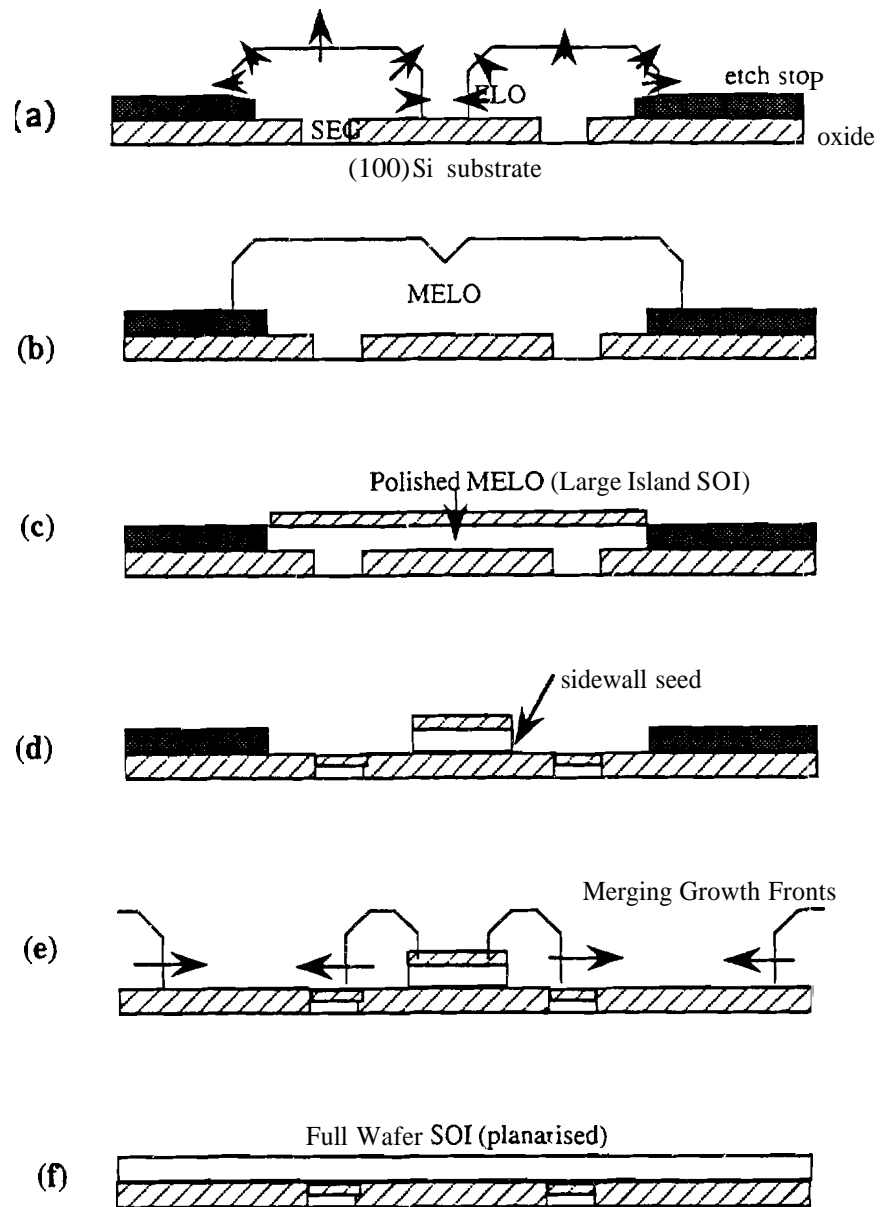


Figure 2.3 Formation of MELO Large Island/Full Wafer SOI [17]

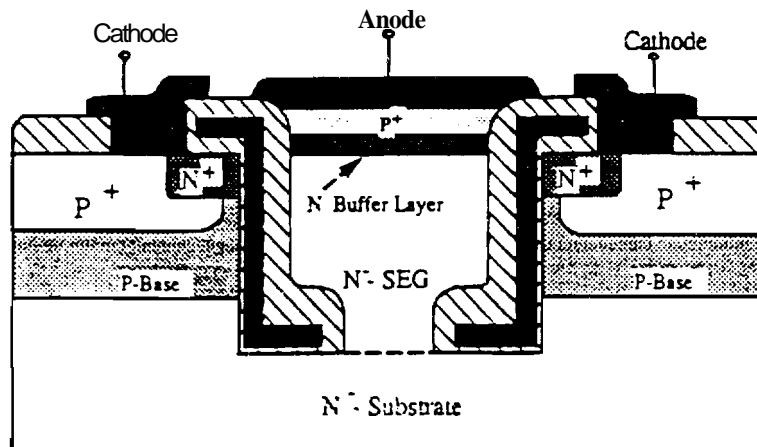


Figure 2.4 3-Dimensional Insulated Gate Bipolar Transistor [19]

2.1.3 3-D Insulated Gate Bipolar Transistor(3-D IGBT)

The insulated gate bipolar transistor combines the advantages of the power MOS-FET with those of the High Power Bipolar Transistor(HBT). The device has a large drift region typically $50\text{--}70\mu\text{m}$ long, that is used to block large voltages. If this is laid out horizontally, it results in poor area utilization of Silicon. The drift region can be laid out vertically with the anode(drain) contacted at the bottom surface while the gate and source are contacted at the top surface. The problem here is that two different devices on the same wafer must perform the same function because of the common back contact--essentially two devices in parallel. The 3-D IGBT (Figure 2.4)combines the above two schemes [19, 20] . A trench is etched into the wafer, and the sidewall is oxidized to form a vertical gate. SEG Silicon is grown out of the trench until it is level with the surface of the wafer. After planarization, the anode: contact is formed at the top of the SEG region. Thus vertical current flow is maintained while all contacts are formed at the top surface. This paves the way for higher integration levels of power devices.

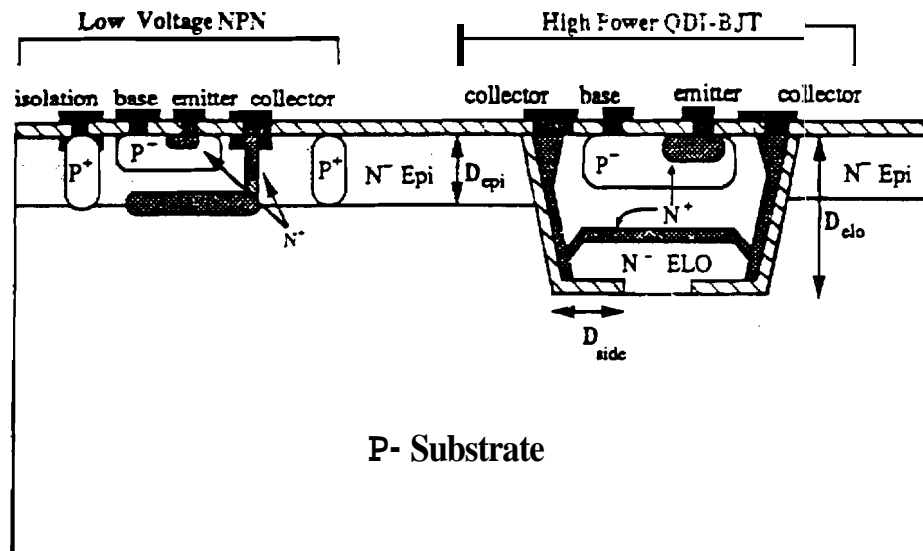


Figure 2.5 Quasi-Dielectric Isolated BJT(QDI-BJT) [19]

2.1.4 Quasi-Dielectric Isolated BJT(QDI-BJT)

In Smart Power technology various isolation schemes are used to combine high voltage devices with low voltage control circuits. A new isolation scheme called **Quasi-Dielectric Isolation** has been proposed for the integration of high voltage devices with low voltage control circuits [19, 21]. Using a combination of Junction Isolation and Dielectric Isolation, the QDI process was achieved by SEG of Silicon in an oxide lined trench. Figure 2.5 shows the high power device fabricated in the QDI tub, while the low power device is made in the adjacent thin epi layer. The QDI process allows separate epitaxial thicknesses and resistivities in the control and power device areas. Therefore it allows separate independent optimisations of control and power devices. The QDI process allows a denser packing of IC's than Junction Isolation and will be useful in the emerging area of High Power ICs.

2.1.5 ELO-BJT(Triple Self-Aligned BJT)

A triple self aligned BJT requiring only one critical mask to make all the active device areas [22, 23] is illustrated in Figure 2.6. A photoresist mask is used to define the buried layer of the transistor, by etching through a thick field oxide. N^+ poly is deposited to form the buried layer contact. SEG is grown out of the seed window defined by the oxide and the poly. This forms the N^- self aligned collector pedestal. Base contacts are from the monocrystalline ELO grown from the sidewalls of the collector pedestal that shows above the field oxide and is doped P^+ . The intrinsic base and emitter regions are also self aligned. This scheme results in reduced device parasitics, and better silicon area utilization.

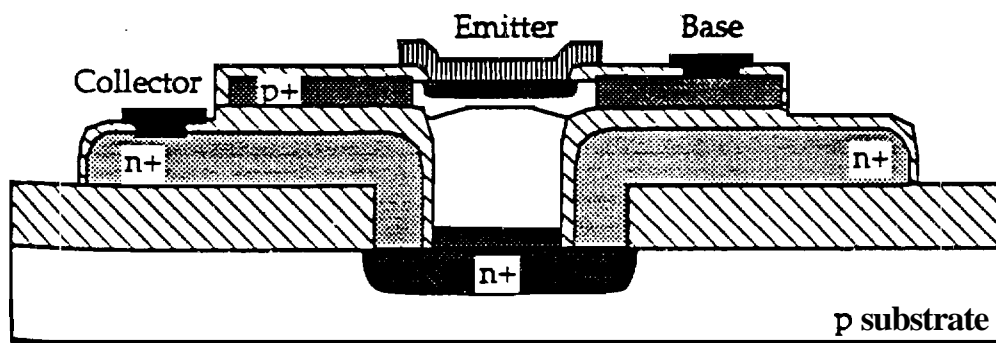


Figure 2.6 ELO-BJT [22]

2.1.6 Bridge Type Piezoelectric Accelerometer

The fabricated silicon Accelerometer [24] consists of a seismic mass and four supporting Silicon diaphragm bridges, that, are completely surrounded by a thick frame. Two stress sensing piezoresistors are placed on each bridge, so that when the central mass experiences an acceleration, the piezoresistors experience the maximum stress (one stress is tensile, and the other compressive) on the bridge and generate an electrical resistance change. From Figure 2.7 it can be seen that the most critical portion

of the process would be the fabrication of the high sensitivity thin Silicon diaphragm. A robust, high quality single crystal Silicon diaphragm was fabricated by Merged Epitaxial Lateral Overgrowth (MELO). Figure 2.8(a) shows flat top MELO-Si grown by the same technique detailed in 2.1.2. The backside of the wafer is then patterned and the Silicon etched away till the buried oxide strips, which act as near perfect etch stops (Figure 2.8(b)). The MELO remaining over the oxide strips forms the diaphragm. The fabricated single crystal Silicon membrane had a thickness of $9\mu\text{m}$, and length and width of $1000\mu\text{m} \times 250\mu\text{m}$. Very good thickness control of the membrane was obtained by the Chemical Mechanical Polishing (CMP) method. Better membrane crystal quality is obtained by orienting the oxide strips in the $\langle 100 \rangle$ direction on a (100) wafer. The SEG/ELO approach has a distinct advantage as the structure can be fabricated not only by passive etching but also by the selective growth of Silicon, providing an extra degree of freedom to the designer.

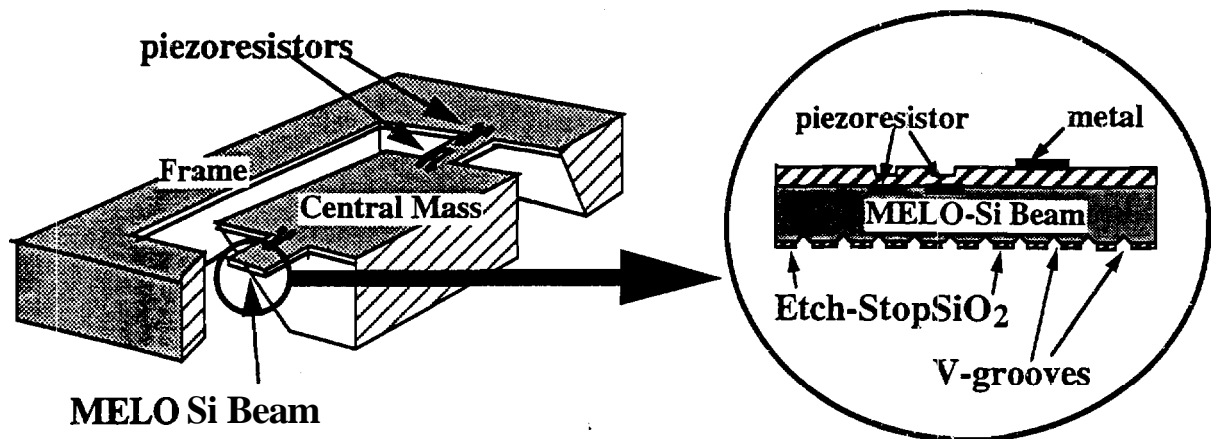


Figure 2.7 Bridge Type Piezoelectric Accelerometer [24]

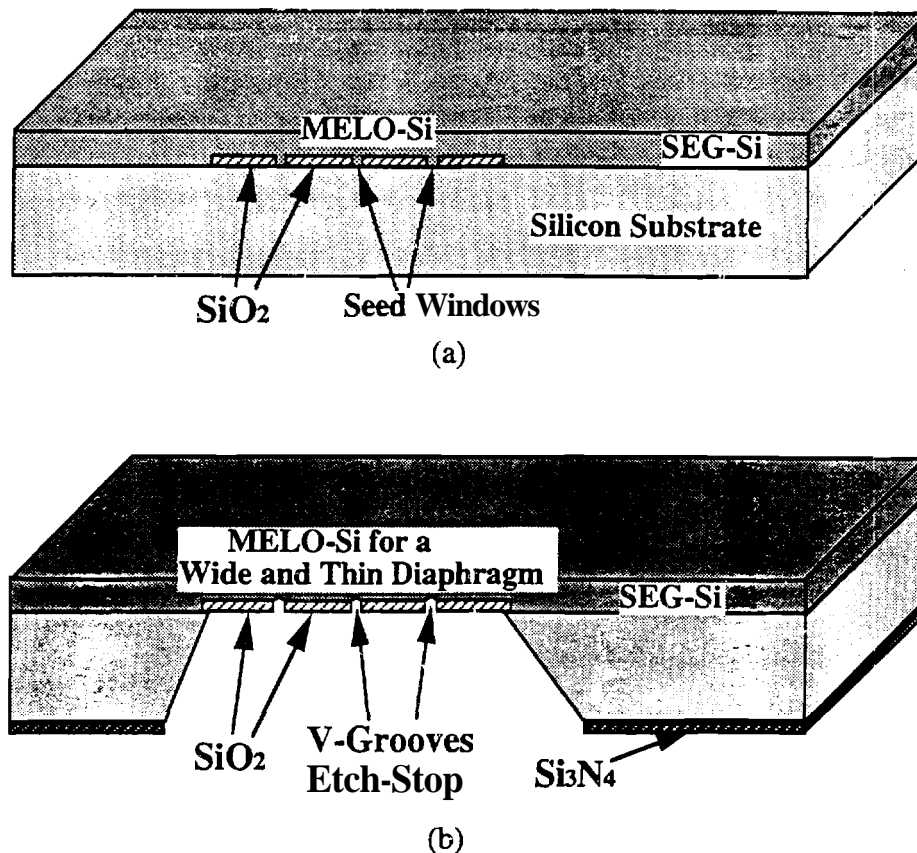


Figure 2.8 a) Flat Top MELO b) MELO-Si Diaphragm [24]

The scope of SEG/ELO technology is readily estimated from various applications that it has been used for. The main problem it faces is the material quality along the SEG/Oxide interface, however bulk Selective Silicon has been found to be of device quality. Its growth rate which is $0.1\text{--}0.2\mu\text{m}/\text{min}$ is sufficient for $5\text{--}8\mu\text{m}$ of growth. To date BJTs, Diodes, Bulk MOSFETs, and fully depleted SOI MOSFETs have been fabricated in SEG/ELO with near bulk quality.

2.2 SEG/ELO: Mechanisms and Models for the DCS-HCl-H₂ System

SEG was first reported by Joyce and Bradley [25] in 1962 using the SiCl₄-H₂ system at 1200°C, and atmospheric pressure. The present low thermal budget for small device processing requires that SEG be conducted at temperatures below 1000°C. Originally, as the growth temperatures were reduced, the epi quality was degraded—largely due to the increase in the partial pressures of water vapour and oxygen [10]. This led to the development of LPCVD and RPCVD reactors operating in the 800–1200°C and 5–760 Torr ranges. Considerable improvements in thickness uniformity and surface morphology, selectivity, sidewall defects and faceting were reported for P < 80 torr and T < 1000°C. SEG has been reported using a variety of source gases and systems; DCS-HCl-H₂, DCS-H₂, SiH₄-HCl-H₂, SiH₄-H₂. A range of different CVD reactors have also been used for SEG, including cold-wall, hot-wall, and Rapid Thermal CVD types.

In this work the primary concern is the modelling of the growth rate of SEG Silicon in the DCS-HCl-H₂ system at reduced pressure.

2.2.1 A Fundamental Model for Silicon Epitaxy

Nonselective Silicon Epitaxy is widely used in industry in bipolar processing for buried layer devices and in CMOS processing as a means to prevent latch up. Consequently there is a large body of work in this field, which serves as a useful starting point for any work on Selective Epitaxy of Silicon. This section deals with a simple model for Si-epitaxy, after which some of the notable efforts in modelling Selective Epitaxy of Silicon will be reviewed.

Silicon Epitaxy is done by the Chemical Vapour Deposition of Silicon from source gases like Silane, and chlorosilanes like SiCl₄, SiHCl₃, SiH₂Cl₂ (DCS) and SiH₃Cl. Of these Dichlorosilane is the most efficient in terms of Silicon deposited per unit mass of the gas used. A simple model for epitaxy was suggested by Grove [26]. Though

there are: models that are more accurate and involved, the Grove model effectively describes the process mechanism.

Since epitaxy takes place by the incorporation of Silicon atoms into the lattice from the Silicon source, it was said to depend upon the flux of Si-atoms at the surface (J_s).

$$J_s = k_s N_s \quad [2.1]$$

where $k_s = A \cdot \exp(-E_A/kT)$ and N_s is the surface concentration of the reactant species. E_A is the Activation Energy for the growth. A small value of E_A would mean that the dependence is weak while a large E_A implies a strong temperature dependence. Assuming that the flow is laminar, a boundary layer of thickness δ exists next to the wafer surface where the gas is stationary. Molecules from the main gas flow diffuse across this boundary layer with a flux J_g where

$$J_g = D_g \frac{N_g - N_s}{\delta} \quad [2.2]$$

and D_g is the diffusion coefficient. At steady state the two fluxes are equal. Equating the above expressions, the surface concentration of reactant species can be expressed in terms of the gas concentration of reactant species N_g .

$$N_s = \left(\frac{h_g}{h_g + k_s} \right) N_g \quad [2.3]$$

By using equations 2.1 , 2.3 the growth rate of the epitaxial Silicon layer can now be expressed as

$$GR = \left(\frac{k_s h_g}{h_g + k_s} \right) \left(\frac{N_g}{N} \right) \quad [2.4]$$

where N is the total number of Silicon atoms incorporated per unit volume of film and $h_g = \frac{D_g}{\delta}$, and is called the mass transfer coefficient. Both k_s and h_g have an Arrhenius relation with temperature. Two special cases for the growth rate expression are:

$$h_g \gg k_s, GR = k_s \frac{N_g}{N} \quad [2.5]$$

$$k_s \gg h_g, GR = h_g \frac{N_g}{N} \quad [2.6]$$

In the first case the growth is said to be surface reaction rate limited, and in the second case is said to be mass transfer limited. In the surface reaction limited regime, the growth rate follows an Arrhenius relation with temperature while the mass transfer regime is relatively temperature independent, due to a small activation energy. This is borne out by Figure 2.9.

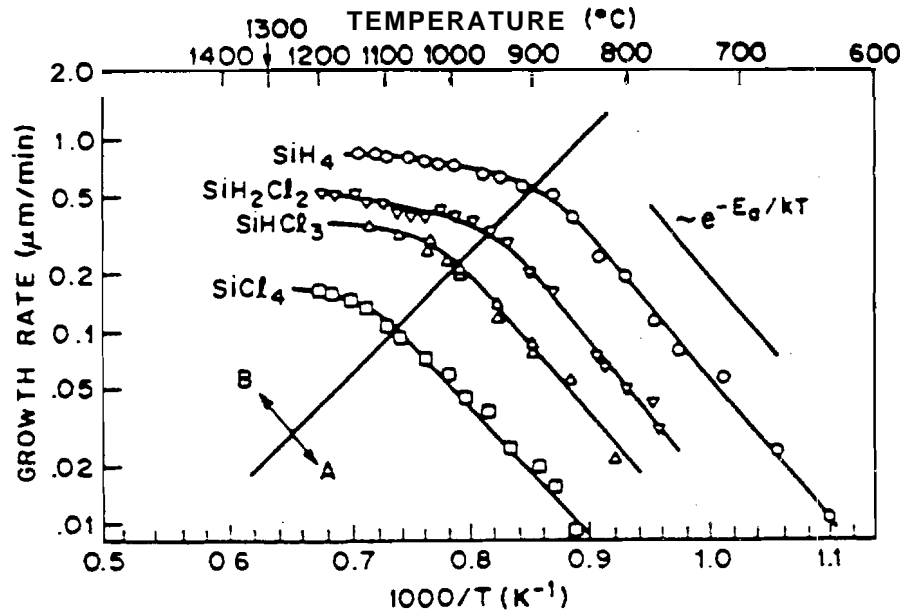


Figure 2.9 Variation of growth rates of Silicon epi with Temperature. A is surface reaction rate limited and B is mass transfer limited.[45]

2.2.2 The DCS-HCl-H₂ system: Constituents and Adsorbed Species

Figure 2.10(a) is a representation of the concentration of various species in the DCS-HCl-H₂ system with 0.1% volume of HCl. The partial pressure of hydrogen can be seen to be invariant with an increase in temperature. This is because hydrogen is present in overwhelming quantity as the carrier gas. Though the inlet partial pressure of DCS is comparable to the partial pressure of HCl, in the figure P_{DCS} is seen to be much smaller than P_{HCl} . This has been explained by a number of researchers [10, 27, 28] as being due to the immediate thermal dissociation of DCS to yield H₂ and SiCl₂. As temperature increases, the partial pressure of SiCl₂ is seen to increase and that of DCS is seen to decrease, further corroborating the above view. The

chemical equation for decomposition of DCS is :



Figure 2.10(b) is another representation of the partial pressures of the gas phase constituents as a function of increasing HCl/DCS ratio, at 0.45 lpm DCS flow, 150 lpm H₂ flow, while temperature and pressure are kept constant. The partial pressures of DCS, SiCl₂, and H₂ are relatively constant while P_{HCl} and P_{SiHCl₃} increase with increasing HCl flow. The increase of P_{HCl} is expected, but the increase in P_{SiHCl₃} is explained by the reaction



which becomes more likely with an increase in HCl.

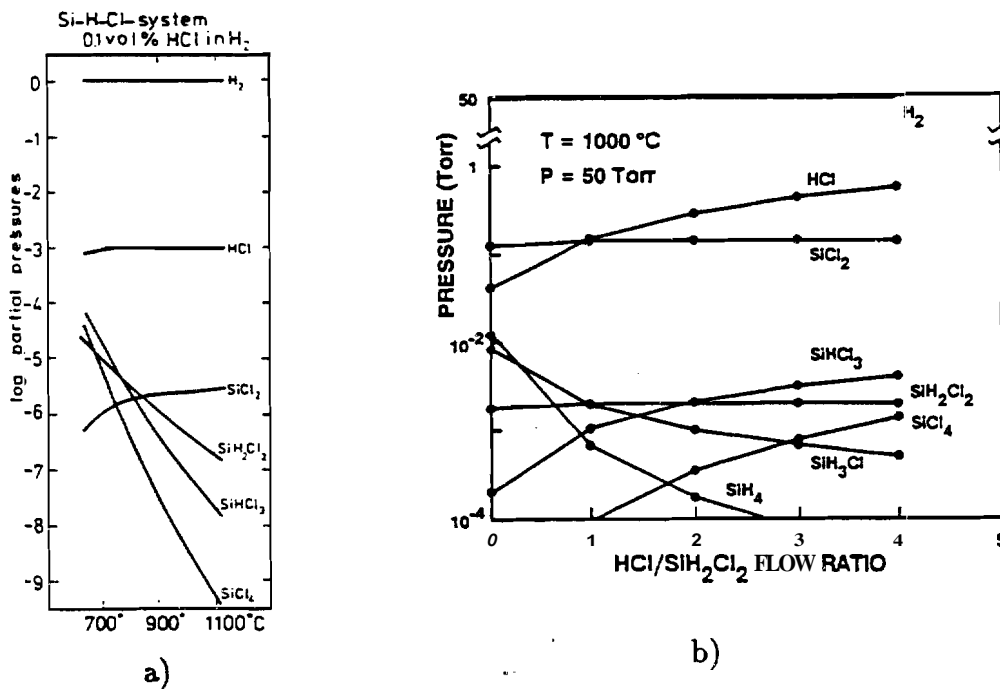


Figure 2.10 Thermochemical data for Si-H-Cl system for a) increasing temperature [27] b) increasing HCl/DCS flow ratio [34]

Since SEG is normally a low temperature process, the growth is considered to be in the surface reaction limited regime. Growth is also expected to be proportional

to the concentration of Silicon containing species that are adsorbed onto the wafer surface [10]. From the thermodynamic data in Figure 2.10, it was seen that the most abundant Silicon containing species was SiCl_2 . The likelihood of saturated molecules like H_2 , HCL , SiCl_4 , SiHCl_3 being adsorbed on to the surface is low because they can be physisorbed with an adsorption energy of about 50KJ/mol [28]. Adsorption of unsaturated species like SiCl_2 , SiCl etc. is more favourable because of the high adsorption energies involved ($\approx 250\text{KJ/mol}$). It has been generally agreed [28, 27, 29] that the main adsorbing species is SiCl_2 . The adsorption reaction being:



*: Free surface site.

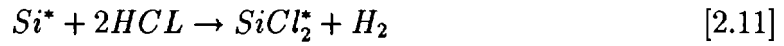
An interesting claim was made by Ho and Brieland [30] who detected HSiCl in the gas phase in the CVD of Silicon from DCS using laser excited fluorescence. They compared their results with an earlier study by Sedgwick et. al [31] that used a similar method to find SiCl_2 as the main species. It was found by Ho and Brieland that the spectrum for both the cases was essentially the same, indicating that HSiCl was actually the fluorescing species. This was cited as a reason to re-evaluate the importance of SiCl_2 as the main adsorbing species.

Atomic Hydrogen and Chlorine, though found in very small quantities are considered to be important surface species due to their high adsorption energies of 310 and 370KJ [28]. The deposition of Silicon has been said to occur by the reduction of the adsorbed species SiCl_2^* by hydrogen:



The reverse reaction takes on a special significance for SEG, as explained by Goulding in [10]. Nucleation on the bulk Silicon in the seed windows was said to occur instantaneously. On the oxide, a delay time t_d elapses before spontaneous deposition occurs forming Silicon adatoms. These adatoms migrate along the surface and coalesce forming polysilicon nuclei. This process takes an additional time t_s .

The sum($t_1=t_c+ t_d$) of the two delays is called the critical or incubation time for nucleation on the oxide. As HCl is added to the system, conditions for the reverse reaction causing silicon etching



to occur become more favourable. If the quantity of HCl added to the system is optimised, the etching effect of HCl removes the Silicon adatoms on the oxide before they form stable polysilicon nuclei; i.e. in a time $< t_1$. The instantaneous nature of Si-nucleation in the seed windows however, allows deposition of Si faster than the HCl can remove it. SEG of Silicon can thus be visualised as a sum of the growth effect— dependent on the abundance of adsorbed $SiCl_2$ on the wafer surface, and the etching effect—dependent upon the partial pressure of HCl. As the HCl content is increased the system passes through three distinct regions; nonselective growth, selective growth, and net etching.

2.2.3 Effect of varying Gas Concentrations on SEG/ELO

In the DCS-HCL- H_2 system, various experiments have been carried out to determine the effect of varying gas composition of the flow on the growth rate. Claasen and Bloem [27] varied the DCS content of the flow at 3 different temperatures; 800,900, and 1000°C. They found that after an initial linear increase, the growth rate became independent of any increase in the DCS flow rate. This effect was more pronounced at lower temperatures. Similar findings were reported by Langlais and Morosanu [28, 29].

Claasen and Bloem also studied the effect of HCl concentration on growth rate. At a higher temperature(1000°C) they noticed a parabolic decrease in growth rate with an increase in HCl flow. Kastelic [32] also found the same behaviour for temperatures from 850–950°C, at 150torr. The same was seen from Mordaunt's data at 970°C, and 40torr. At lower temperatures($\leq 900^\circ C$), Claasen and Bloem found a linear variation with HCl flow. This was also exhibited by Mordaunt's data at 920°C. Drowley [34]

performed experiments for a variety of conditions from 850–1000°C and 50 and 100 Torr pressure, but reported only linear variations with HCl flow. It was also found that for different ratios of HCl/DCS, the DCS-HCl-H₂ existed in three different regions. When the difference in HCl/DCS ratios is between 3 and 4 for the conditions in Figure 2.11, selective growth takes place. Above HCl/DCS=4, net etching is expected, and below HCl/DCS=2, nucleation of Silicon takes place on the oxide. There is thus a 'selectivity window' in which SEG/ELO can take place.

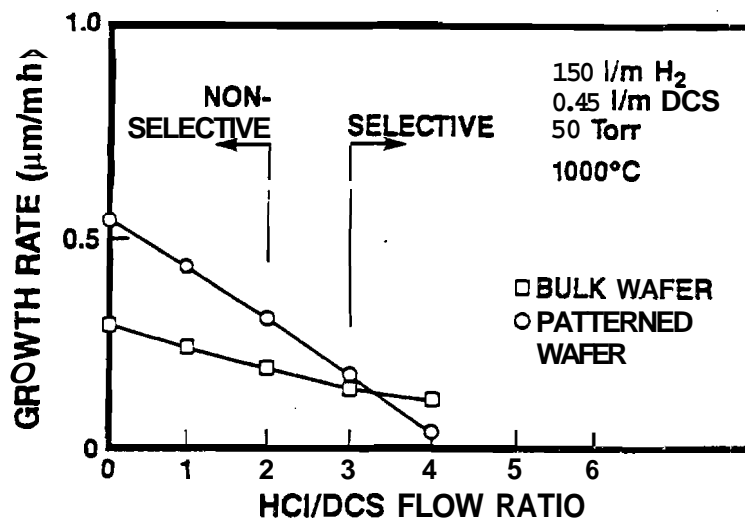


Figure 2.11 Nonselective Growth, Selective Growth, and Etch Regions [34]

Growth rate was also observed to increase linearly with the partial pressure of hydrogen, in DCS-HCl-H₂-N₂ [27] and in a DCS-HCl-H₂-Ar system [29], where the overall pressure was kept constant while varying the relative proportion of the carrier gases—which were a mixture of Hydrogen and Nitrogen in the first case and Hydrogen and Argon in the second. Langlais et. al. [28] plotted the natural log of the growth rate against the natural log of the partial pressure of hydrogen and found an slope of 0.5 at 850°C. This corresponds to a variation of growth rate with $\sqrt{(P_{H_2})}$. They also found that an increase in the total flow rate of gases correspond to an increase in

growth rate. At 850°C, a linear variation was reported, but at 1000°C the growth rate increase deviated from linearity. Similar behaviour was reported by Kastelic while varying the total gas flow rate from 30–90slpm while keeping their individual partial pressures constant.

2.2.4 Effect of varying Temperature on SEG/ELO

Fig. 2.1.1 shows the mass transfer and surface reaction limited regimes. Since much of SEG/ELO is done below 1000°C, the growth is considered to be in the surface reaction limited regimes. As expected, when the temperature increases the growth rate increases. This increase can be defined by an Arrhenius relationship with an activation energy E_A . Kastelic [32] extracted the activation energy for SEG/ELO of Silicon at 150 torr by varying the temperature from 900–1000°C, while keeping the gas concentration constant. Between 900–950°C E_A was 20kcal/mol, and between 950–1000°C E_A was 6kcal/mol, illustrating the difference between the 2 regimes. Similar studies by Zingg [35] yielded an overall E_A of 35kcal/mol.

Another effect of temperature was to move the location of the 'selectivity window' discussed earlier. For lower temperatures, the threshold between the selective and non-selective regions is at smaller HCl/DCS ratios. As the temperature is increased the threshold and window are shifted to higher HCl/DCS ratios [34]. Langlais et. al. found that E_A depended upon the ratio between the carrier gas (hydrogen) flow and the DCS flow; $a = \frac{Q_{H_2}}{Q_{DCS}}$. For smaller values of a , classical behaviour was exhibited with $E_A=40$ kcal/mol. For larger a values the growth rate exhibited a selective minimum at about 1000°C. Other studies [29] showed 23kcal/mol from 750–950°C, and 37kcal/mol from 950–1150°C as values of E_A .

2.2.5 Effect of varying Pressure on SEG/ELO

The effects of varying system pressure on the growth rate were investigated by Langlais et. al. For low temperatures (850°C) they reported a gradual increase with pressure. At 1000°C a very sharp increase in growth rate was observed for pressures

less than 2kPa. For pressures greater than 2kPa, the growth rate remained almost constant. Duchemin et.al.[36] found that for low pressures (10–30 Torr), the growth rate was proportional to $P_{H_2}^{-0.5}$, while from 30–500 Torr, it was proportional to $P_{H_2}^{-1}$. Kastelic [32] found the growth rate to increase as $P^{1/2}$ for a barrel reactor at 950°C.

2.2.6 Effect of varying Oxide Thickness and Coverage on SEG/ELO

Friedrich [46] performed extensive studies on the effect of oxide thickness and oxide coverage on the growth rate. The growth rate was found to drop off as the oxide thickness increased. As the oxide thickness increased, the effect on the growth rate began to decrease. Various researchers [34, 46, 38] have studied the effect of changing the wafer area covered by the oxide on the growth rate. Large differences in growth rate were found when the coverage was high, i.e. the differences in growth rate between a 95% and a 90% oxide covered wafer was larger than the growth rate differences between 30% and 50% wafers. Drowley [34] found that the selectivity threshold varied with oxide coverage. In a similar experiment to Friedrich's, he noticed that the threshold for a wafer with 90% coverage was at a lower HCl/DCS ratio than the threshold for 80% wafer coverage.

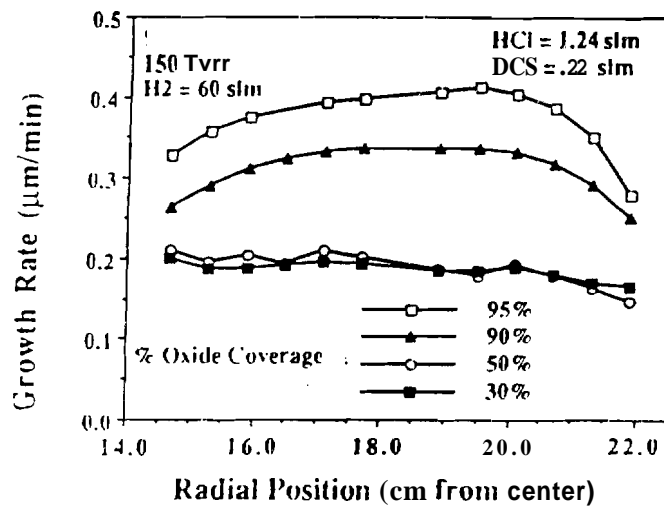


Figure 2.12 Effect of Masking Oxide Coverage on Selective Epitaxial Growth Profile [46]

Friedrich explained that variations in oxide thickness and surface coverage lead to differences in wafer surface temperatures. At steady state, heat was lost from the wafer surface by conduction, convection and radiation. Since convection would not be influenced by a difference in wafer coverage, the causes were limited to conduction and radiation. By a calculation Friedrich concluded that though conduction was affected by the masking oxide layer, the difference in wafer temperature was not significant. Thus the oxide mask was said to impede radiative heat transfer, and so cause the large difference in wafer surface temperature and consequently in growth rates.

2.2.7 Growth Rate Models for SEG/ELO

Claasen and Bloem in their studies on CVD of Si in the DCS-HCL-H₂ system postulated a detailed reaction mechanism that took into account reactions at the surface, surface steps etc. The expression for growth was found to be dependent on the concentration of ADSORBED SiCl₂, the fraction of free surface sites (8) and the partial pressure of hydrogen. The etch term was derived from Van der Putte's[42] analysis and was found proportional to the square of the HCl partial pressure and inversely proportional to H₂ partial pressure. The difference between the etch and growth terms was the net growth rate of Silicon.

$$GR = k_g P_{H_2} P_{SiCl_2} \theta - k_e \frac{P_{HCl}^2}{P_{H_2}} \quad [2.12]$$

where k_g and k_e are the Arrhenius rate constants for growth and etch respectively.

The reaction model consisted of about 15 steps. Using these, 8 was expressed in terms of the inlet gases to yield the final expression below:

$$GR = \frac{k_g P_{H_2} P_{SiCl_2}}{1 + k_s P_{SiCl_2} + k_{Cl} \frac{P_{HCl}}{\sqrt{(P_{H_2})}} + k_H \sqrt{(P_{H_2})}} - k_e \frac{P_{HCl}^2}{P_{H_2}} \quad [2.13]$$

$$\theta = \frac{1}{1 + k_s P_{SiCl_2} + k_{Cl} \frac{P_{HCl}}{\sqrt{(P_{H_2})}} + k_H \sqrt{(P_{H_2})}} \quad [2.14]$$

The numerical quantities for the reaction rate constants were not evaluated. The change of growth rate dependence on HCl flow from P_{HCl}^2 to P_{HCl} was explained

by suggesting that the etch term dropped out as k_e became very small at smaller temperatures. The linear decrease in growth rate was attributed to the variation in P_{SiCl_2} , since at lower temperatures some $SiCl_2$ is used up in the formation of $SiHCl_3$ (Equation 2.8) .

Morosanu et. al. modelled the DCS- H_2 system which is very close to the DCS-HCL- H_2 system, since in both cases HCl is released by the reduction of the surface adsorbed species(Equation 2.10). Considering a simplified reaction sequence and omitting expressions for the fraction of free surface sites (θ) taking part in the reaction, the expression arrived at for the growth rate was;

$$GR = k_g \frac{P_{SiCl_2}}{P_{H_2}} \quad [2.15]$$

Here the etching expression containing HCl was omitted as the HCl released when Silicon was deposited was considered to have negligible effect.

Langlais et. al. [28] working with the DCS- H_2 system and following a similar reaction sequence to Claasen and Bloem [27], but with fewer steps, obtained a general expression for growth rate given by

$$GR = \frac{k_g P_{H_2} P_{SiCl_2} - k_e P_{HCl}^2}{1 + k_s P_{SiCl_2} + k_{Cl} P_{Cl} + k_H P_H} \quad [2.16]$$

Two possible cases were considered where one of the three adsorbed species was predominant. Where $SiCl_2$ was present in the largest proportion, the growth rate was:

$$GR = k_g P_{H_2} - k_e \frac{P_{HCl}^2}{P_{SiCl_2}} \quad [2.17]$$

Where Cl was most abundant on the surface, the expression became;

$$GR = k_g \frac{P_{SiCl_2} P_{H_2}}{P_{Cl}} - k_e \frac{P_{HCl}^2}{P_{Cl}} \quad [2.18]$$

Langlais et. al then evaluated the surface coverage of each of the adsorbing species 800°C and 1000°C using thermochemical data. At 800°C $SiCl_2$ was predominant and

at 1000°C Cl coverage was greater. Thus for lower temperatures, equation 2.17, and for higher temperatures equation 2.18 were the logical choices.

Kastelic [32] developed a model for SEG growth rate along the same lines as Langlais. He went a step further by expressing P_{SiCl_2} in terms of P_{DCS} , and assumed that P_{SiCl_2} was the dominant surface species. The expression for growth rate in terms of the inlet species was:

$$GR = \frac{k_g P_{DCS} - k_e P_{HCl}^2}{1 + k_s P_{DCS}} \quad [2.19]$$

In the denominator the second term was then assumed to be larger, reducing the expression to:

$$GR = k'_g - k'_e \frac{P_{HCl}^2}{P_{DCS}} \quad [2.20]$$

$$k'_g = 2.02 \times 10^5 \exp\left(\frac{-31600}{kT}\right)$$

$$k'_e = 53.2 \exp\left(\frac{-12600}{kT}\right)$$

Mordaunt [33] did an extensive study of growth rates at temperatures: from 840–1020°C and at three pressures—40,95, and 150 Torr. He proposed an alternative two surface site reaction mechanism that finally yielded an expression of the form;

$$GR = \frac{k_g P_{DCS} - k_e P_{HCl}^2}{1 + \sqrt{(k_H P_{H_2})}} \quad [2.21]$$

$$k_g = 3.58 \times 10^7 \exp\left(\frac{-41000}{kT}\right)$$

$$k_e = 50 \exp\left(\frac{-16000}{kT}\right)$$

$$k_H = 1 \times 10^{-9} \exp\left(\frac{43.3}{kT}\right)$$

In this the main adsorbed species was taken to be Hydrogen. The accuracy of the model was enhanced by considering the surface, and not the inlet partial pressures,

since adsorption is more likely to be influenced by the partial pressures of the species at the wafer surface. An FEM program was used to calculate the surface partial pressures, and the rate constants were then evaluated. This model gave very good results at higher system pressures.



3. PROCESS CONSIDERATIONS

3.1 Reactor Description

All the Selective Silicon growth in this work was done in the Gemini-I LPCVD Reactor at Purdue University. A cross section appears in Figure 3.1. The reactor chamber consists of a quartz bell jar and a stainless steel bottom plate. Wafers are placed on a circular susceptor that is inductively heated by an R.F. coil below it. The bell jar has a height of 27 inches and a diameter of 21 inches. The susceptor is 18 inches in diameter. Gases are introduced into the reactor through the inlet nozzle in the center of the susceptor. Exhaust gases are removed through an outlet in the bottom plate, below the susceptor. Figure 3.2 shows a block diagram of the reactor system.

The heating and temperature control assembly consists of a frequency generator, pyrometer, temperature control unit, and induction coil. The 500KW frequency generator delivers power to the induction coil located below the susceptor. Temperature is sensed by a pyrometer that looks down onto the susceptor through a window at the top of the bell jar. Power supplied to the coil is regulated by the temperature control unit against the pyrometer readings. The minimum temperature that can be measured is 650°C. The distance between the induction coils and the susceptor can be optimised to obtain a uniform temperature profile across the susceptor.

The pressure can be reduced to a minimum of 40 Torr. This limit is dictated by the onset of arcing, and plasma generation of the carrier gas. For pressures of 150 Torr and above, the frequency used is 111KHz. From 40–150 Torr, a frequency of 87KHz is used to limit arcing.

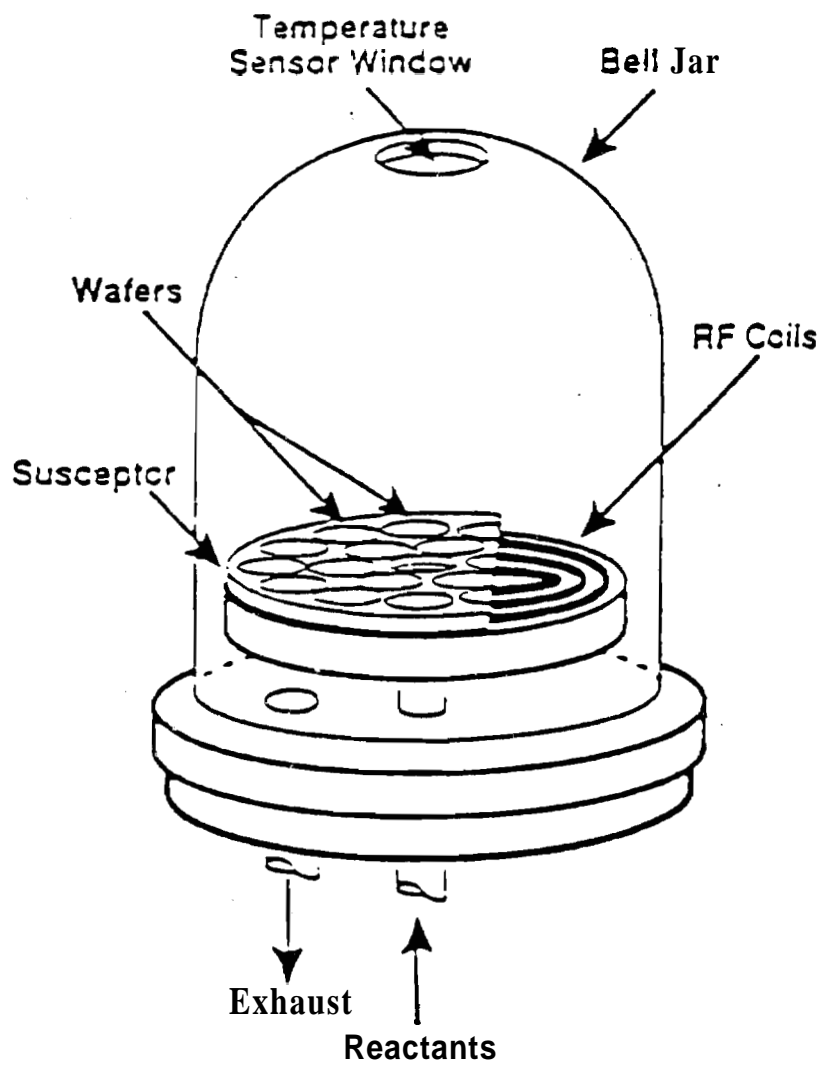


Figure 3.1 Reactor Crosssection [40]

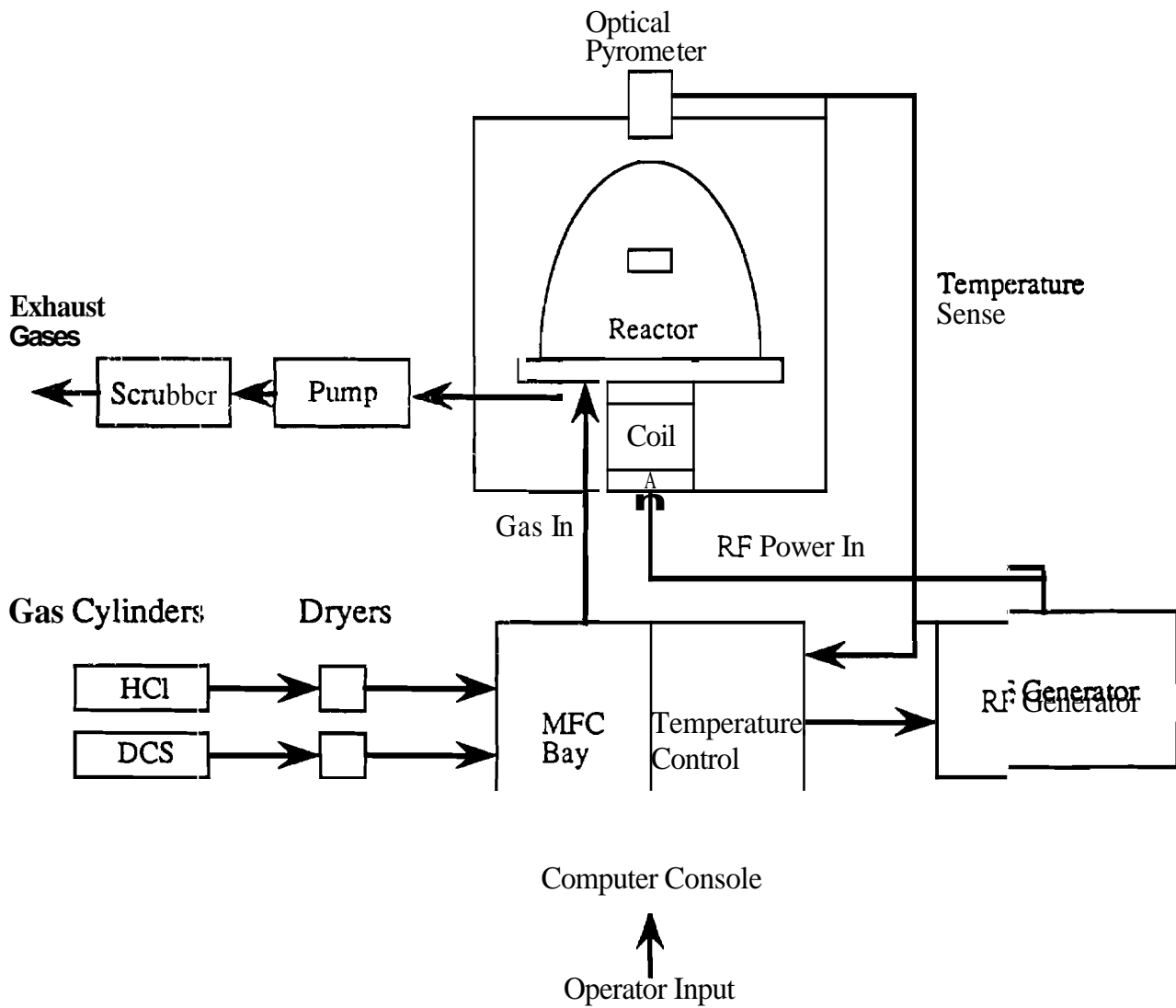


Figure 3.2 Reactor Block Diagram

The susceptor is made of graphite with a coating of Silicon Carbide. A further coating of polysilicon is used to reduce the outdiffusion of contaminants from graphite. The polysilicon coating is removed, and a new coat applied each time the reactor is cleaned. The susceptor is completely flat (no recessed pockets) so that wafers of any size (upto 6") can be placed anywhere on the surface. RF energy emitted by the coils is absorbed by the susceptor, which then heats up the wafers on the surface by conduction. To decrease the effects of local non-uniformities in temperature and gas flow, the susceptor rotates during operation at 8rpm.

Five gases are connected to the reactor: dry Nitrogen, Hydrogen, Dichlorosolane, Hydrogen Chloride, and Phosphene. Once admitted through the inlet nozzle, the gases flow up to the top of the bell jar, and then down the walls. The gas stream then splits into two; one that flows down to the outlet below the susceptor and the other that flows along the surface of the susceptor. Hydrogen is the carrier gas during operation. It is purified of Oxygen by passing it through a catalytic converter, that converts the oxygen to H_2O . This H_2O and any other moisture present in the gas is then removed by passage through a dryer. The other gases are introduced into the reactor from the cylinders. Mass Flow Controllers regulate the flow of the gases into the reactor chamber.

3.2 Reactor Drift

In developing a model for the growth rate of SEG Silicon, it was necessary to perform several experiments, if possible, without repeating many of the conditions for which growth rate data had already been collected. It was therefore required to adhere closely to the methodology used earlier, and also to quantify the reactor drift, if any. Reactor drift could occur due to the following reasons:

3.2.1 Temperature Drift

A temperature drift is possible between the set point and the actual temperature on the susceptor. The reactor had been recalibrated by matching the set point

temperature to the melting point of Germanium dots placed across the susceptor. A further reason for drift is the coating of the pyrometer window after a deposition run. The pyrometer senses temperature by the glow of the susceptor. Deposition on the pyrometer window decreases the light admitted to the pyrometer, which interprets it as a lower temperature. A spurious temperature increase follows that could increase the growth rate. A uniform procedure of removing the deposit from the pyrometer window after a fixed run time was followed. The reactor calibration and window deposition control procedures minimize the chances of temperature drift being a strong factor.

3.2.2 Oxide Coverage/Thickness effect

A difference in the masking oxide thickness, and surface coverage could also change the growth rate. The data points used from earlier runs were limited to those using oxide thicknesses of 800 Angstroms. All the subsequent runs were done with 800 Angstroms of oxide on the wafer. The variation of growth rate due to surface coverage was found to vary globally across the wafer; i.e. the growth rate for 95% coverage was about 20% higher than the growth rate for 90% coverage (Figure 2.12). Thus it is easier to factor in.

3.2.3 Wafer Thickness

The earlier study used wafers of 14–15 mils thickness, while 19–21 mils thick wafers were used for this study. Growth rate of Silicon depends on the surface temperature of the wafer. Heat transfer through the wafer would take place primarily through conduction. The difference in temperatures between the front and back surfaces of the wafer was expected to differ due to the wafer thicknesses. An expression for this difference is given below using the electrical analogue of the thermal system [47].

$$T_{bs} - T_{fs} = \left(\frac{T_b}{R_{wafer} + R_{reactor}} \right) R_{wafer} \quad [3.1]$$

where T_{bs} and T_{fs} are the temperatures at the back and front surfaces of the wafer, and $R_{reactor}$, R_{wafer} are thermal resistances. The thermal resistance of the wafer is likely to be much smaller than that of the reactor. We can thus make the assumption that $R_{wafer} \approx 0$. For two wafers of the same area but different thicknesses, the ratio between the front and back surface temperature differences is given by:

$$\frac{(T_{bs} - T_{fs})_{wafer1}}{(T_{bs} - T_{fs})_{wafer2}} = \frac{R_{wafer1}}{R_{wafer2}} = \frac{t_1}{t_2} \quad [3.2]$$

where t_1 , t_2 are the wafer thicknesses. For the present wafer thicknesses of 21 mils, the ratio of temperature differences would be;

$$(T_{bs} - T_{fs})_{21} = \left(\frac{21}{15}\right)(T_{bs} - T_{fs})_{15} = 1.4(T_{bs} - T_{fs})_{15} \quad [3.3]$$

The effect of this increased temperature difference would be to decrease the growth rate on the thicker wafer, as its surface temperature would be lower. To estimate this difference, SEG runs were done with wafers of average thickness 21 and 25 mils loaded simultaneously in the reactor. For two runs, growth rates on the thicker wafer were 0.142 and 0.12 $\mu\text{m}/\text{min}$, while for the thinner wafer the corresponding growth rates were 0.144 and 0.125 $\mu\text{m}/\text{min}$. As expected the growth rates on the thicker wafer are marginally lower. From this data it was possible to conclude that, (a) the effect of difference of wafer thickness could be neglected, and (b) the temperature difference between front and back surfaces is very small.

3.2.4 Mass Flow Controller Drift

The Mass Flow Controllers that regulate the flow of gases into the reactor are subject to degradation over a period of time. This causes a difference between the set point flow and actual flow. The critical MFC's are those for Dichlorosilane and HCL. An increase in the actual flow of DCS could cause an unexpected increase in the growth rate. An increase in flow of HCl would cause a decrease in the growth rate.

From the above analysis, it was clear that all the factors responsible for reactor drift were accounted for and found to have negligible effect, but for oxide coverage and MFC drift. To estimate drift due to these factors, a series of baseline runs were done and compared against previous data at 970°C and 40 torr. Figure 3.3 shows the earlier and baseline data, plotted on the same graph. The baseline data is seen to follow the same trend as earlier data. The difference is thought to be within the limits of error due to cleaning and processing techniques. It was concluded that the reactor drift was very small, and there was no need to include a correction factor to normalise the data.

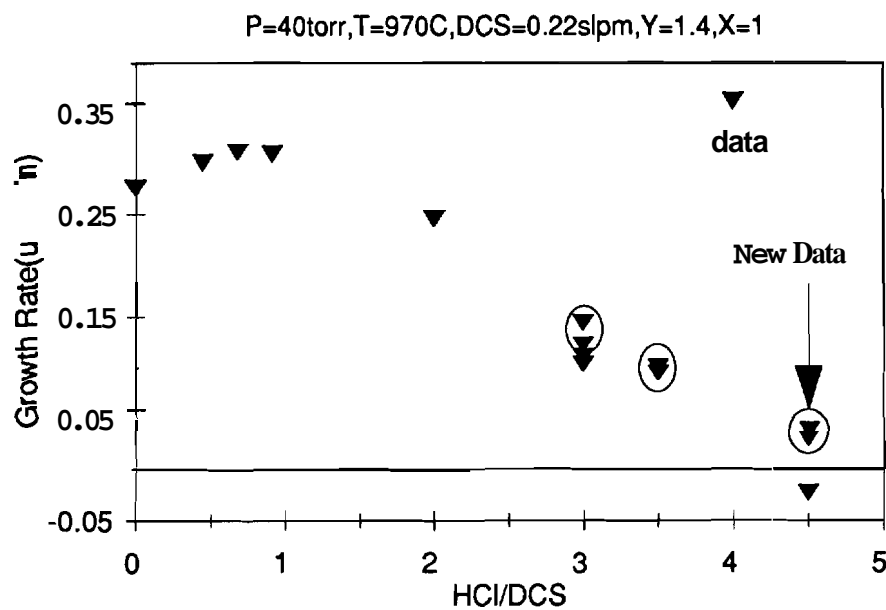


Figure 3.3 Overall Reactor Drift from Baseline Runs

3.3 Process Steps

3.3.1 Oxidation

The wafers were cleaned in piranha($\text{H}_2\text{SO}_4:\text{H}_2\text{O}$ in 1:1 ratio) for 12–14 minutes. They were then rinsed with DI and dipped in BHF for about 20 seconds. This was followed by a very thorough rinse in DI for 15 minutes. TSUPREM3 was used to simulate the oxidation. For a $< 100 >$ substrate doped to 10^{15} cm^{-3} , 18 minutes

in steam at 950°C resulted in 800 Angstroms of oxide. Nitrogen was chosen as the push/pull gas as very little nitridation of the oxide would take place at temperatures below 1000°C. The time for oxide growth was later optimised to 19 minutes. Less spotting on the wafers occurred when they were faced backwards in the furnace tube—facing away from the gas stream.

3.3.2 Photolithography

The wafers were hardbaked for 10 mins to remove any traces of moisture and then coated with a monolayer of HMDS to improve photoresist adhesion. AZ 1350-JF positive resist was used because of finer linewidths afforded, and for better compatibility with the mask aligner. Spin-on time used was 30s at a speed of 4400 rpm, to yield an expected thickness of 1.7 μm . Mask #1 of the "standard mask" set was used for seed window definition. The seed window edges were aligned at 45° to the wafer flat to minimise defect generation. The Karl Suss mask aligner was used in the High Precision mode to expose the photoresist for 7.5s. The seed windows were wet etched using BHF. Epi quality was found to be better when the photoresist was stripped off immediately after the etch.

3.3.3 Selective Epitaxy

Wafers were loaded into the reactor at atmospheric pressure. A hydrogen purge is done to remove any oxygen and water vapour that may have entered the bell jar. Temperature is ramped up to the set point, and the system pressure reduced to the desired value. A hydrogen bake is performed for 5 minutes at 970°C to remove any native oxide that may be present on the seed windows. Hydrogen Chloride gas is vented into the system, and an HCL etch performed for 30s. This removes a few atomic layers of Silicon in the seed windows to remove any surface on the substrate. DCS and HCl are then introduced into the reactor in the required proportion with hydrogen as the carrier gas for selective epitaxial growth. At the end of the deposition period HCl, DCS, and the RF generator are switched off and the system is allowed

to cool down to 650°C. Nitrogen is used to purge out the hydrogen and the wafers unloaded after the system is brought back to atmospheric pressure.

3.4 Measurement Techniques

3.4.1 Profilometer

SEG film thicknesses were measured using a Tencor Alpha Step 200 profilometer. A mechanical stylus runs over the wafer recording the differences in elevation of the features on the surface. A video microscope and 9" monitor screen are used to position the stylus over the region to be scanned. Though step heights are easily measured, features widths are more difficult to measure. The physical diameter of the stylus point (≈ 1600 Angstroms) causes the measured step profile to be different from the actual (Figure 3.4). For the stylus used, the width loss due to the stylus would be about $0.6\mu\text{m}$.

For all runs the wafers were placed in the centre region of the susceptor. Measurements were made at 5 points on the wafer, and averaged to eliminate any local non-uniformities.

3.4.2 Nomarski

An Olympus BH-2 microscope with magnifications of 150 and 750 were used to study the surface morphology of SEG. In the Nomarski technique, plane polarised light is produced and split up by a modified Wollaston prism. The two wavefronts produced are at right angles to each other. A variable optical path difference can be introduced between the two beams before they are recombined at the wafer surface. For no path difference, the edges appear bright against a dark background. For $\lambda/2$ path difference, dark edges are produced against a light background. By this 'shadowing' technique, step heights of 30–50 Angstroms can be detected. Thus any etch pits stacking faults, dislocations or facets can be observed. Nucleation on the oxide can also be observed. Examples of the facet formation in ELO is shown in Figure 3.5.

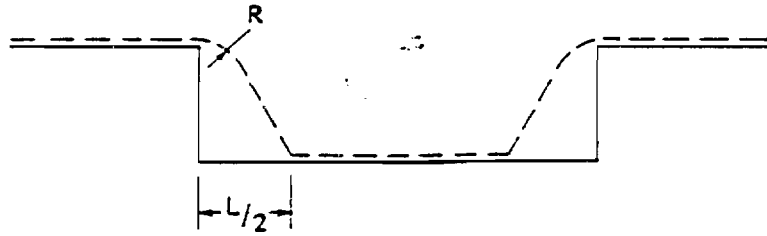


Figure 3.4 Error due to Stylus Dimension in Profilometer Width Measurements [48]

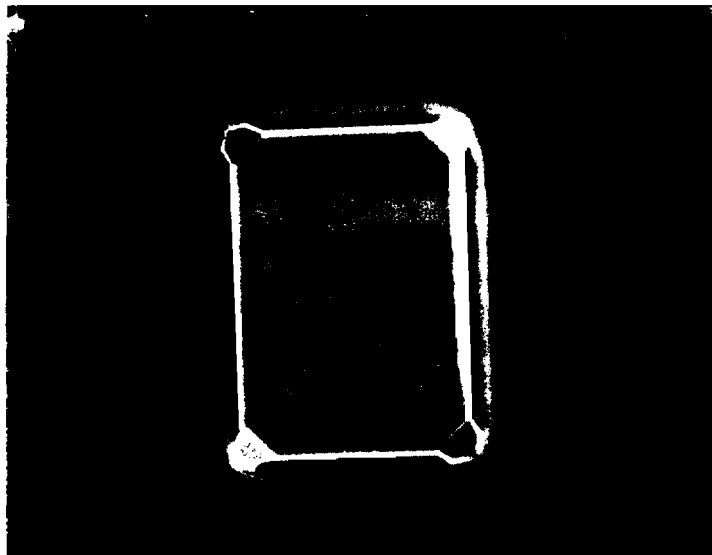


Figure 3.5 Face' Formation during ELO as seen through Nomarski

4. MODELING OF GROWTH RATE OF SEG/ELO

4.1 Selection of Expression to Model Growth Rate of SEG/ELO Silicon

The basic equation that has been used to describe the growth rate of SEG Silicon by several researchers, has been;

$$GR = \frac{\hat{k}_g P_{SiCl_2} P_{H_2} - \hat{k}_e P_{HCl}^2}{1 + k_H P_H + k_{Cl} P_{Cl} + k_{DCS} P_{DCS}} \quad [4.1]$$

The partial pressure of a constituent 'i' of the system, is given by;

$$P_i = X_i P \quad [4.2]$$

where X_i is the molefraction of 'i', and P is the system pressure.

$$k_j = A_j e^{\frac{-E_{A_j}}{RT}} \quad [4.3]$$

k_j is an Arrhenius reaction rate constant with an Activation Energy E_{A_j} . SEG is a low temperature process, and is normally carried out in a range of 850–1000°C. It is possible that one of the surface species is predominant in this temperature range. This is indicated in a study by [49], in which the ranges of dominance for each species on the surface is; $T < 800^\circ\text{C}$ for H^* , $800 < T < 1000^\circ\text{C}$ for $SiCl_2^*$, and $T > 1000^\circ\text{C}$ for Cl^* . The denominator of the expression above can thus be simplified to a quantity 'A', that is dependent on the surface concentration of the dominant surface species. The expression then reduces to:

$$GR = \frac{\hat{k}_g P_{SiCl_2} P_{H_2} - \hat{k}_e P_{HCl}^2}{\Delta} \quad [4.4]$$

The temperature and pressure dependence of A will be investigated . The quantity P_{SiCl_2} can be expressed in terms of inlet gases by the relation,

$$P_{SiCl_2} = k_1 \frac{P_{DCS}}{P_{H_2}} \quad [4.5]$$

reducing Equation 4.4 to:

$$GR = \frac{k'_g P_{DCS} - \hat{k}_e P_{HCl}^2}{\Delta} \quad [4.6]$$

An alternative form of Equation 4.6 in terms of the inlet gas mole fractions, and system pressure is:

$$GR = \frac{k'_g P X_{DCS} - \hat{k}_e P^2 X_{HCl}^2}{\Delta} \quad [4.7]$$

Figure 4.1 shows the shift in the growth/etch threshold for data taken at 40 Torr, and at 150 Torr. The 'y' axis shows the amount of HCl flow required to get to the Growth/Etch threshold. All other conditions such as Temperature, Hydrogen flow, and DCS flow are kept the same. This data indicates that the growth/etch(G/E) threshold occurs at an HCl flow of 0.66slpm for 40 Torr, and at an HCl flow of 1.24slpm for 150 Torr. The selectivity threshold was also found to shift in the same direction as the G/E threshold. This is seen in Figures 4.2 and 4.3. The selectivity threshold shifts from HCl/DCS=3 for 50 Torr, to HCl/DCS=4 for 100 Torr.

Equation 4.7 can be tested against the above behaviour. The G/E threshold is determined by the relative magnitude of the growth and etch terms. If the growth term is larger than the etch term, net growth is indicated, while net etching is indicated when the etch term is larger. The common denominator Δ only affects the overall magnitude, and can be neglected while computing the G/E threshold. Δ always remains positive and thus can never cause the expression to become negative (net etching). The expression was fitted to data at 40 Torr, and the effect of changing the pressure on the G/E threshold was determined. The expression used to compute the G/E threshold was:

$$GR = 2.8 \times 10^9 * e^{\left(\frac{-26000}{T}\right)} P_{DCS} - 1.36 * 10^8 \times e^{\left(\frac{-23100}{T}\right)} P_{HCl}^2$$

Figure 4.1 shows that the above expression predicts a G/E threshold shift to lower HCl flow rates as the system pressure is increased; a behaviour that is opposite to

what is expected. This does not necessarily mean that the theoretical expression is wrong, but that it is a special case. For the model to follow the data, the expression must have a positive slope with pressure. The condition for this to hold true is can be determined by using the first derivative of the numerator of the growth rate expression.

$$f = k_g(X_{DCS})P - k_e(X_{HCl})^2 P^2 \quad [4.8]$$

$$\frac{\delta f}{\delta P} = k_g(X_{DCS}) - 2k_e(X_{HCl})^2 P > 0 \quad [4.9]$$

$$P < P_{critical} = \frac{k_g(X_{DCS})}{2k_e(X_{HCl})^2} \quad [4.10]$$

The system pressure must thus be less than the critical pressure for this model to work. $P_{critical}$ itself is a function of the reaction rate constants. The method used to fit the data yields a unique set of numbers for the reaction rate constants. $P_{critical}$ was calculated using these values, and the HCl flow rates at the G/E threshold, to take into account the selectivity shift with temperature. In the table below, $P_{critical}$ can be seen to be smaller than the system pressure (40 Torr), which implies that the theoretical expression is invalid. As system pressure is increased, the $P_{critical}$ further decreases, since X_{HCl} increases due to the selectivity shift. Therefore for our range of system parameters, it is necessary to modify the theoretical expression.

Temperature(C)	P-critical (Torr)	HCl Flow(slpn)
970	14	0.99
920	30	0.66

Table 4.1 Variation in Critical Pressure with a change in Temperature

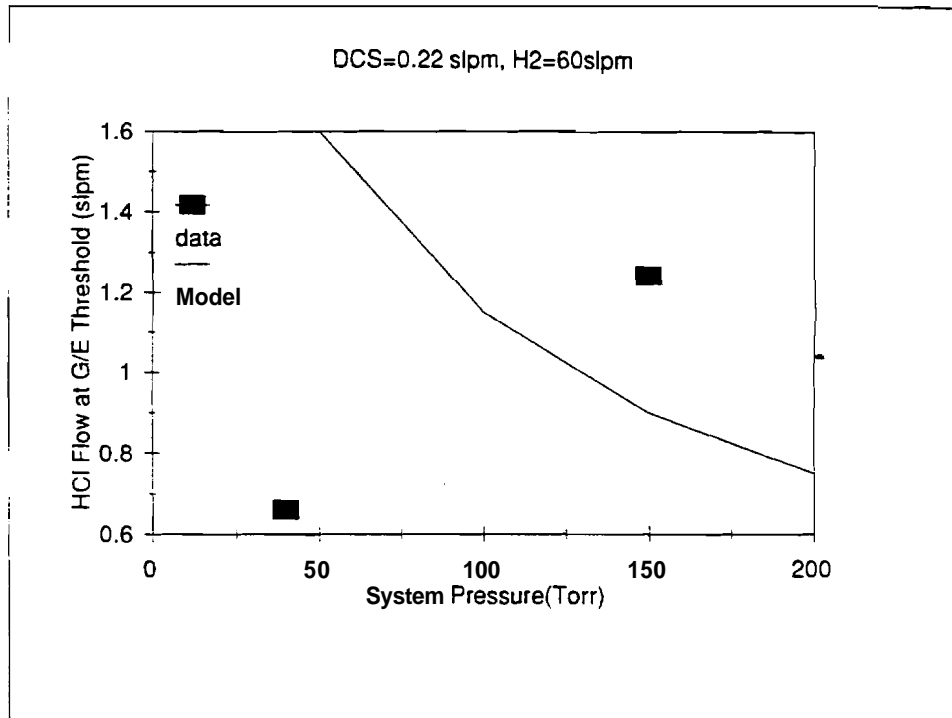


Figure 4.1 Growth/Etch Threshold shift with pressure

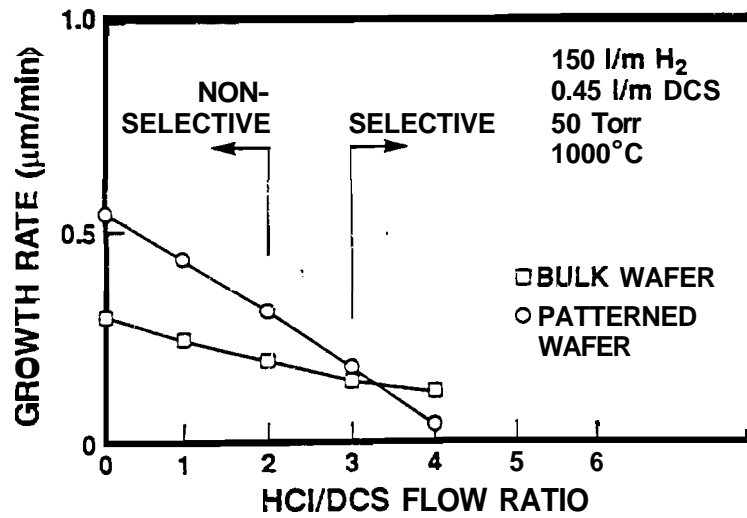


Figure 4.2 Selectivity Threshold at 50 Torr: HCl/DCS=3 [34]

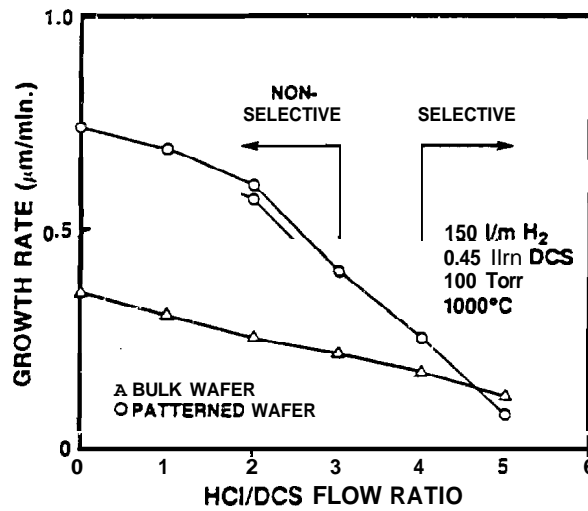


Figure 4.3 Selectivity Threshold at 100 Torr: HCl/DCS=4 [34]

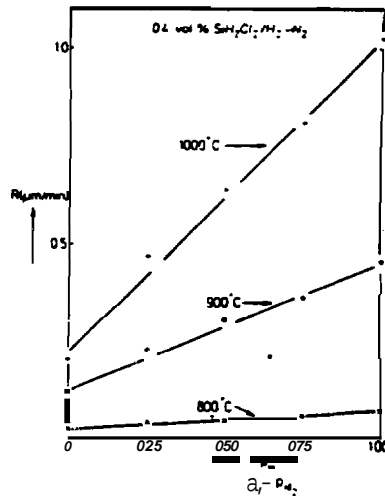
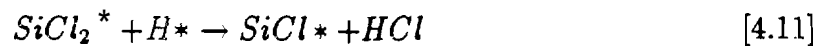


Figure 4.4 Effect of **Changing** Hydrogen Partial Pressure on Growth Rate [27]

The reduction of SiCl_2^* by HCl was considered to be a single step reaction in the derivation of Equation 4.1. Morosanu [29] has proposed a two step reduction reaction of the form;



Equation 4.11 was considered to be the rate-determining step. If this **approach** is used, the kinetic expression for growth rate obtained would be:

$$GR = \frac{k_g'' P_{DCS} - k_e' P_{HCl}}{\Delta} \quad [4.13]$$

$$= P \left[\frac{k_g'' X_{DCS} - k_e' X_{HCl}}{\Delta} \right] \quad [4.14]$$

By inspection Equation 4.14 predicts that the G/E threshold would remain at the same HCl/DCS ratio with changing pressure, with all other parameters **being** constant. This expression, although closer to the **experimental** results is **still** not accurate. At this point it **becomes** necessary to use a more empirical **approach**.

Figure 4.4 shows the effect on growth rate when the partial **pressure** of H_2 is increased from 0-1 in a $\text{SiH}_2\text{Cl}_2\text{-H}_2\text{-N}_2$ system. By Equation 4.11 or **Equation** 4.14, there **should** be no change in the growth rate **when** the H_2 flow is varied, if the overall pressure is kept constant. However, the growth rate is seen to **increase** with

an increase in P_{H_2} . To account for this increase, P_{H_2} is introduced in the growth term. The expression for growth rate now becomes:

$$GR = \frac{k_g''' P_{DCS} P_{H_2} - k_e' P_{HCl}}{\Delta} \quad [4.15]$$

By inspection the above equation predicts that the G/E threshold moves to higher HCl/DCS ratios as pressure increases. However, it also predicts that if the mole fractions of both HCl, and DCS are increased by the same factor 'F', the growth rate is also increased by a factor F (P,T,Hydrogen flow are kept constant).

Run	HCl(slpn)	DCS(slpn)	GR(um/min)
1	0.66	0.22	0.12
2	1.32	0.44	0.04

Table 4.2 Effect of Doubling HCl,DCS Flows on Growth Rate, T=970°C,P=40 Torr,H₂=60slpm

This was tested by choosing F=2. Two runs were done using the flows in the table above. The growth rate is decreased. Rewriting Equation 4.15 as shown below;

$$GR = \frac{k_g(P_{DCS})^z(P_{H_2})^x - k_e(P_{HCl})^y}{\Delta} \quad [4.16]$$

It is evident from the data in Table 2, that $y > z$ as the etch term is seen to increase faster than the growth term for the same factor of increase in DCS, and HCL. At the same time, to allow the G/E threshold to move to higher HCl/DCS ratios with increasing pressures, the growth term must increase faster than the etch term when the system goes to larger pressures; i.e $x+z > y$. It now remains to find a workable combination of empirical constants to predict the growth rate. The following section describes the method used to evaluate the rate constants, and exponents for this final expression for growth rate.

4.2 Fitting of Growth Rate Expression to Experimental Data

At the growth/etch threshold, growth rate is effectively 0. We can therefore rewrite Equation 4.16 as;

$$k_g(P_{H_2})^x(P_{DCS})^z - k_e(P_{HCl})^y = 0 \quad [4.17]$$

For two different pressures, P_1 and P_2 , while keeping temperature constant, k_g and k_e remain the same. The growth rate expression at the G/E threshold, at two different pressures can be written as:

$$\begin{aligned} k_g(P_{H_2})_1^x(P_{DCS})_1^z - k_e(P_{HCl})_1^y &= 0; \text{ at } P_1 \\ k_g(P_{H_2})_2^x(P_{DCS})_2^z - k_e(P_{HCl})_2^y &= 0; \text{ at } P_2 \end{aligned}$$

Dividing one equation by the other, we obtain the following relationship:

$$\begin{aligned} \frac{(P_{H_2})_1^x (P_{DCS})_1^z}{(P_{H_2})_2^x (P_{DCS})_2^z} &= \frac{(P_{HCl})_1^y}{(P_{HCl})_2^y} \\ &= \frac{(P_2)_1^x (X_{DCS})_1^z P_1^z}{(P_2)_2^x (X_{DCS})_2^z P_2^z} = \frac{(X_{HCl})_1^y P_1^y}{(X_{HCl})_2^y P_2^y} \end{aligned}$$

P replaces P_{H_2} as the flow is overwhelmingly Hydrogen. The mole fraction of DCS remains nearly the same at both pressures as the DCS flow is kept constant. With these assumptions, the relationship is modified to:

$$\left(\frac{P_1}{P_2}\right)^{x+z-y} = \frac{(X_{HCl})_1^y}{(X_{HCl})_2^y} \quad [4.18]$$

From experimental data at 920°C, we know the HCl flow rate at the G/E threshold for 40 Torr, and 150 Torr. By choosing 'y' and 'z', 'x' can be evaluated.

Once x,y, and z are fixed, the rate constant k_g can be evaluated by using growth rate data at 0 slpm HCl (Figure 4.5), taken for temperatures ranging from 820°C–970°C at 40 Torr. The etch term in Equation 4.16 drops out. Taking the natural log of both sides, we get:

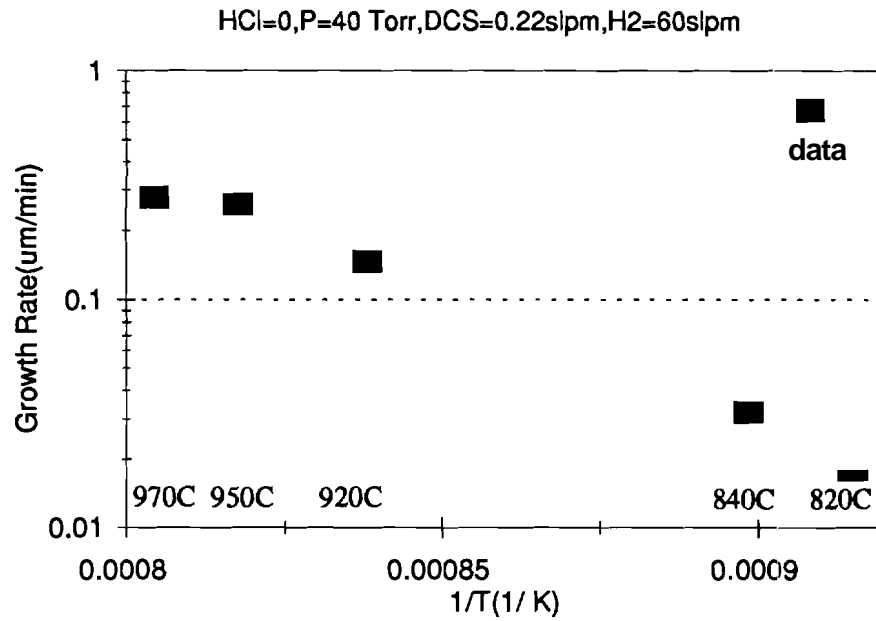


Figure 4.5 Growth Rate Variation with Temperature at HCl=0 slpm

$$\ln(GR) = \ln\left[\frac{A_g}{A} e^{\frac{E_{A_g}}{kT}} (P_{DCS})^z (P_{H_2})^x\right]$$

$$\ln(GR) = \frac{-E_{A_g}}{kT} + \ln\left[\frac{A_g}{A} (P_{DCS})^z (P_{H_2})^x\right] \quad [4.19]$$

By regression, the activation energy, and A , can be extracted from the experimental data. For 40 Torr, $A = 1$ was used.

Now, K_e can be found from the data collected in the presence of HCl. For this data set, temperature was varied from 970–920°C at 40 Torr, while keeping HCl, DCS, and H_2 flows constant. k_e can be written as:

$$k_e = A_e e^{\frac{-E_{A_e}}{kT}} = \left[\frac{GR - k_g (P_{DCS})^z (P_{H_2})^x}{(P_{HCl})^y} \right]$$

Taking the natural log of both sides;

$$\ln(A_e) + \frac{-E_{A_e}}{k} \left(\frac{1}{T}\right) = \ln\left[\frac{GR - k_g (P_{DCS})^z (P_{H_2})^x}{(P_{HCl})^y} \right] \quad [4.20]$$

Since we know the growth rate from the experimental data, the RHS is completely determined. By a regression fit, activation energy and A , can be estimated.

The numbers obtained by this method complete the expression for growth rate. This was tested against two groups of data. At 970°C and 40 Torr, HCl/DCS was varied from 0–4.7. The variation in growth rate is plotted in Figure 4.6, along with two versions of the growth rate model; (A) $x=1, z=1, y=1.5$, and (B) $x=1, z=0.7, y=1.2$. Figure 4.7 shows the variation in growth rate when the flow rates of HCl, and DCS are doubled. Both models are seen to follow the data in Figure 4.7 within limits of error. In Figure 4.6, it is seen that model A tends to fall off very rapidly as the HCl/DCS ratio is increased, while the data exhibits a more linear decrease. Since the region between HCl/DCS of 3–4 is where selective growth occurs, the correct trend must be predicted by the model here. The better choice would be model B.

The same numbers were used to fit the data at 95, and 150 Torr. For higher pressures, the model predicted uniformly higher growth rates than seen in the experimental data. The ratios between actual and predicted growth rates were evaluated for different growth conditions, at each pressure. It was found that for each pressure, the ratios at different temperatures and HCl flows were close. This would indicate that \mathbf{A} changes significantly when the system pressure is changed, but does not change very much when temperature, and HCl flow are changed. \mathbf{A} was found to have an average value of 4.0 at 95 Torr, and 7.5 at 150 Torr. Approximating \mathbf{A} as being solely a function of system pressure P , the best correlation was found for a linear relation between Δ and P . The slope m and the intercept C can be found by regression.

$$\Delta = mP + C$$

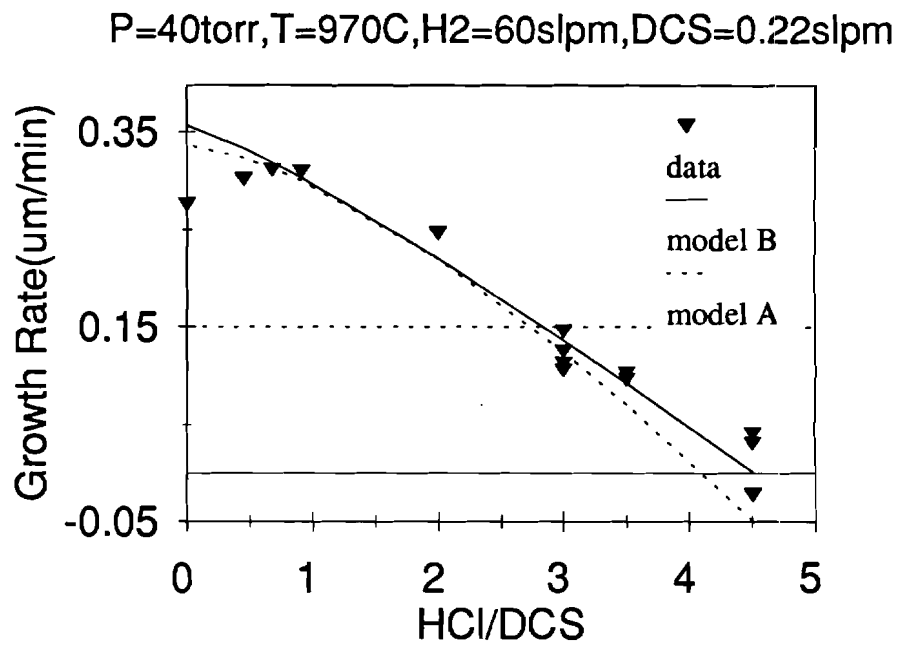


Figure 4.6 Choice of model to describe growth rate variation with HCl

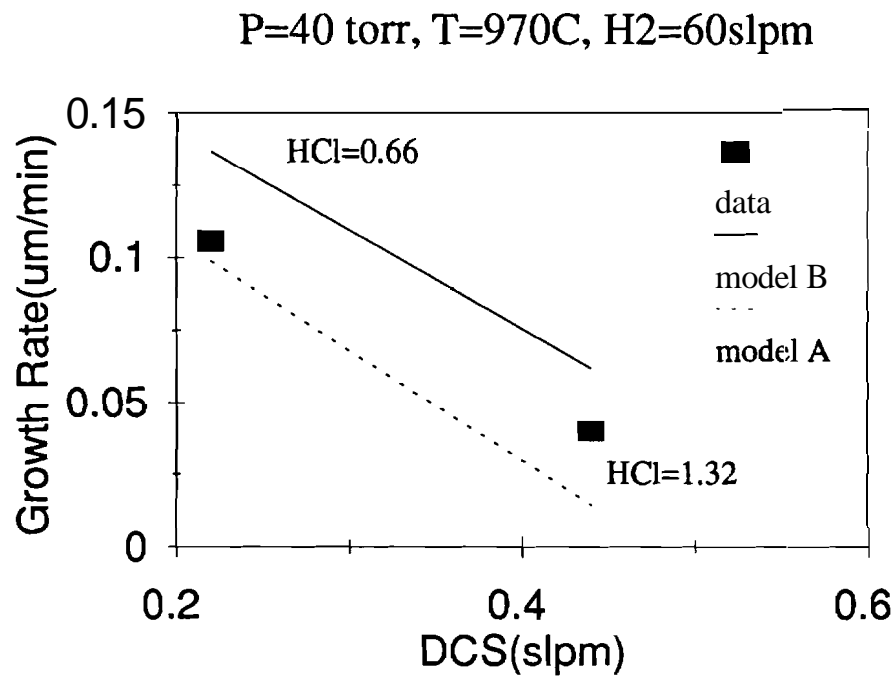


Figure 4.7 Choice of model to describe growth rate variation with doubling of HCl, DCS flow rates

Using these methods, the final form of the model for SEG-Silicon growth, fitted to the experimental data obtained at Purdue University was:

$$GR = \frac{5.3 \times 10^7 e^{-\frac{26300}{T}} (P_{DCS})^{0.7} (P_{H_2}) - 176000 \times e^{-\frac{15660}{T}} (P_{HCl})^{1.2}}{0.06P - 1.4} \quad [4.21]$$

The fit of this model to various data points is shown in Figures 4.9–4.14. Excellent agreement is found for all conditions. The model predicted the G/E threshold for 95 Torr, and 920°C to be at 1 slpm HCl flow. An SEG run at these conditions found a growth rate of 9nm/min; very close to etching. Other trends found in literature are also predicted.

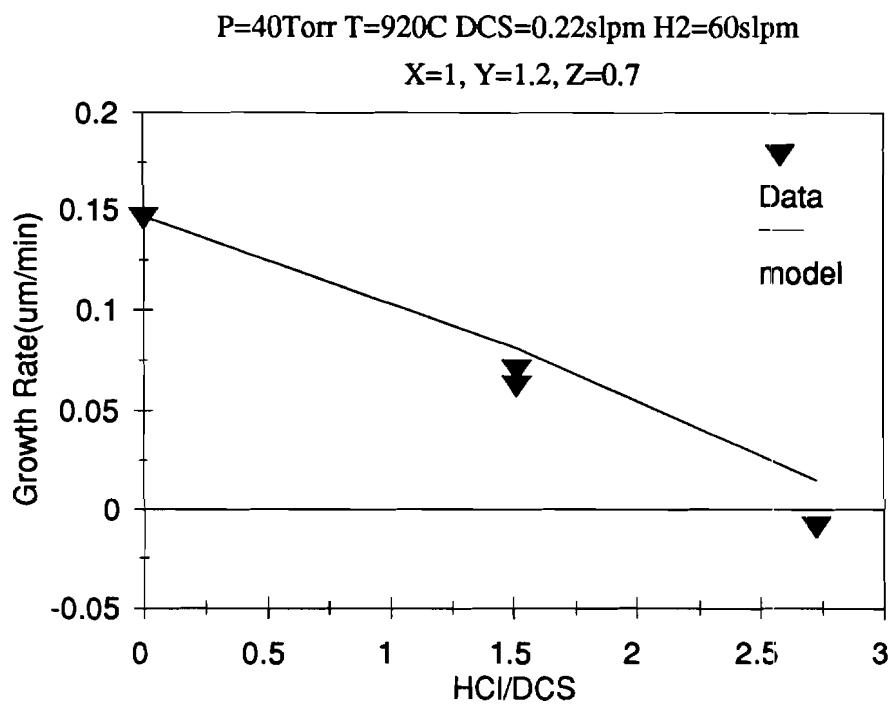


Figure 4.8 Fit of model to data: growth rate variation with HCl itt 920°C, 40 Torr

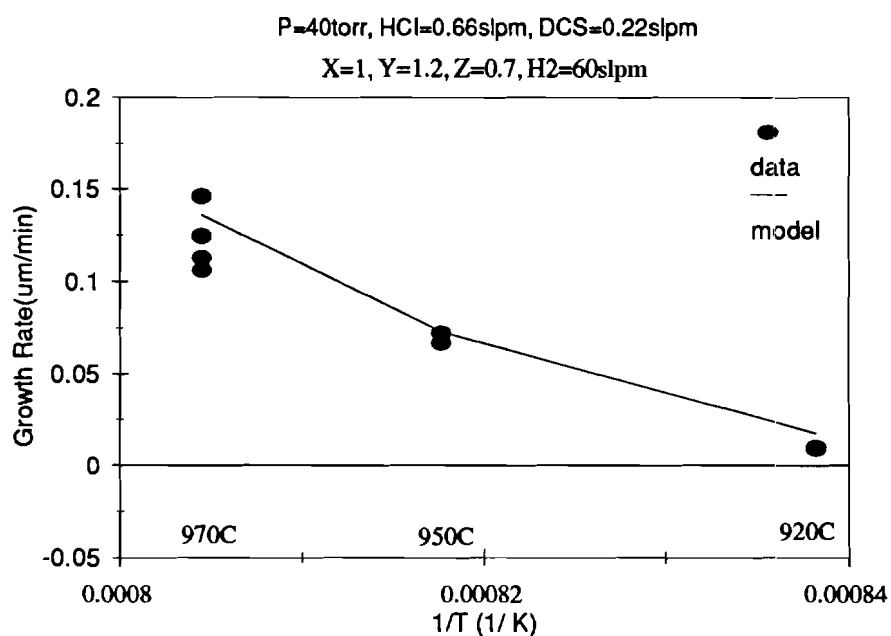


Figure 4.9 Fit of model to data: growth rate variation with temperature at 40Torr

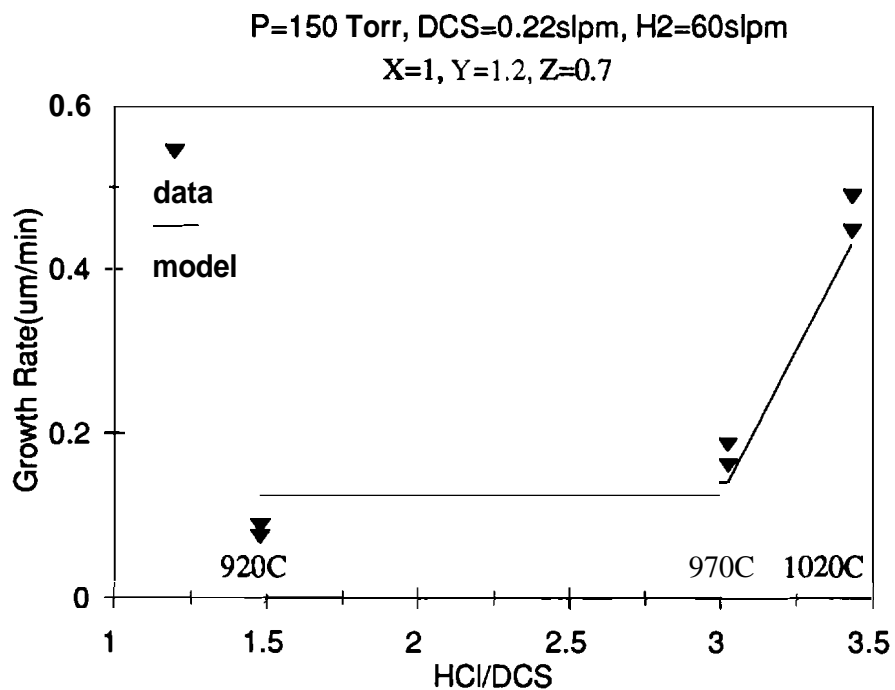


Figure 4.10 Fit of model to data: growth rate variation at 150 Torr

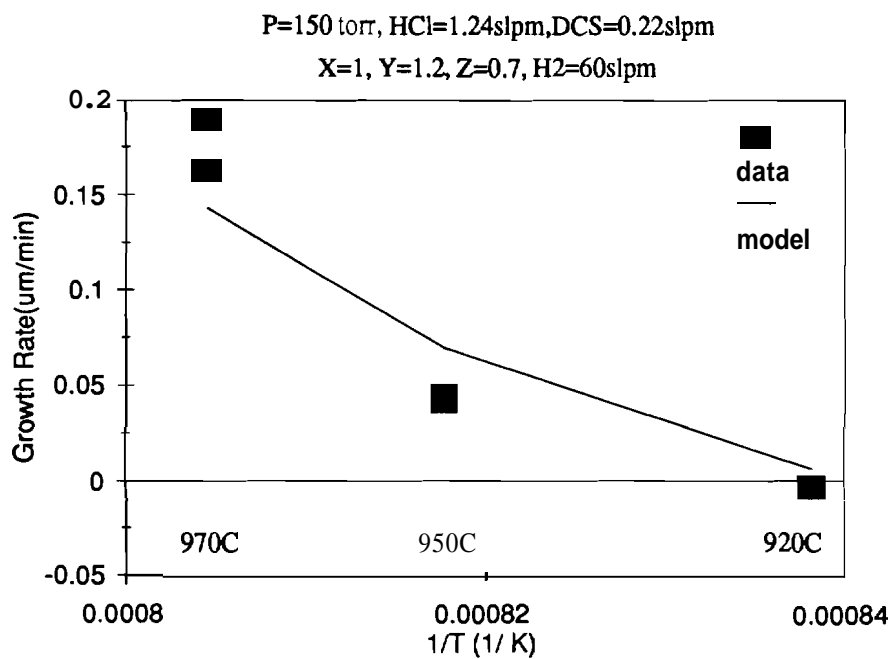


Figure 4.11 Fit of model to data: growth rate variation with temperature at 1.24 slpm HCl, 150 Torr

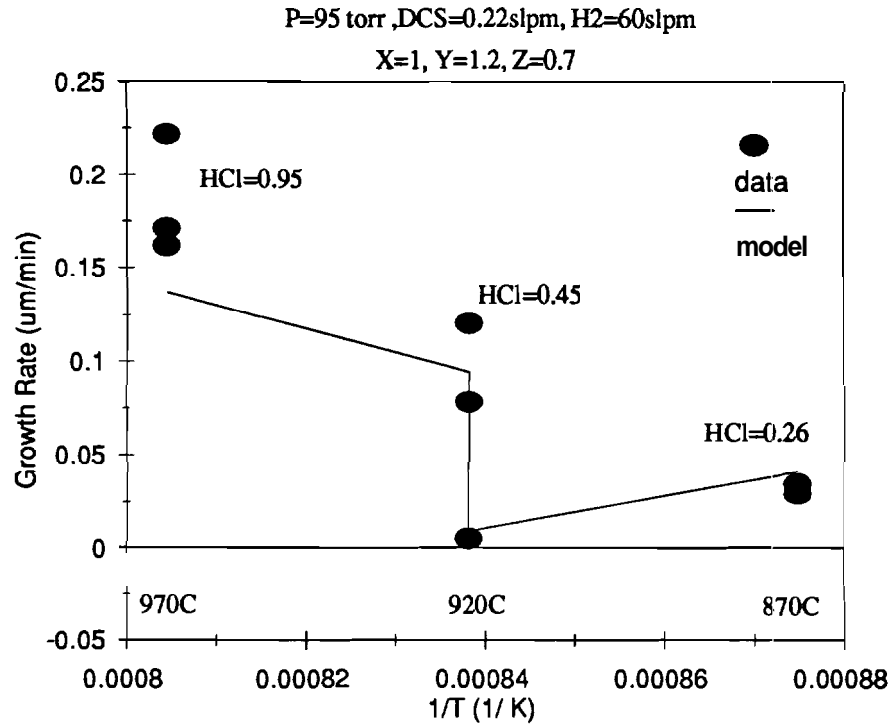


Figure 4.12 Fit of model to data: growth rate variation at 95 Torr

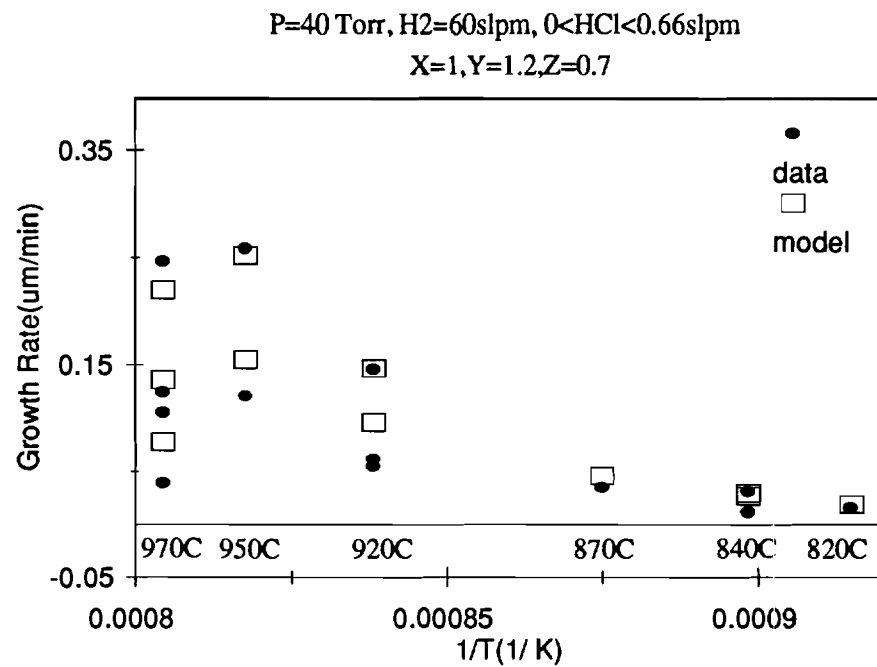


Figure 4.13 Fit of model to data: growth rate variation at 40 Torr

4.3 Application to TSUPREM4

All the SEG runs used in this work have been done with the seed window edges oriented along the $\langle 100 \rangle$ direction; i.e. at 45° to the (100) wafer flat. This orientation results in reduced stacking faults and dislocations along the SEG/Oxide interface. SEG/ELO growth results in the formation of (100), and (110) facets. The vertical and horizontal extent of the ELO growth is determined by the growth rate of the (100) plane. Consequently all growth rates are with respect to the (100) plane.

When SEG is grown out of a trench, there is one growth front; (100) for trench widths greater than $5\text{--}10\mu\text{m}$ (Figure 2.1(a)). Equation 4.21 can be used to predict this growth. On reaching the level of the oxide, two growth fronts are present (Figure 2.1(b)). From experimental data, the aspect ratio for ELO grown under different conditions has been found to be ≈ 1 . Therefore ELO growth may be simulated by applying the growth rate model in both the horizontal and the vertical directions. The model would approximate the actual faceted growth profile in by the rectangular profile in 4.15.

From a processing and device fabrication standpoint, facet formation is not critical. After SEG/ELO growth, planarization of ELO is normally done. This removes all facets, and leaves behind a thin sheet of SOI or a filled trench, depending upon the height of the etch stops used (Figure 2.3(c,d)). The present model thus accomplishes

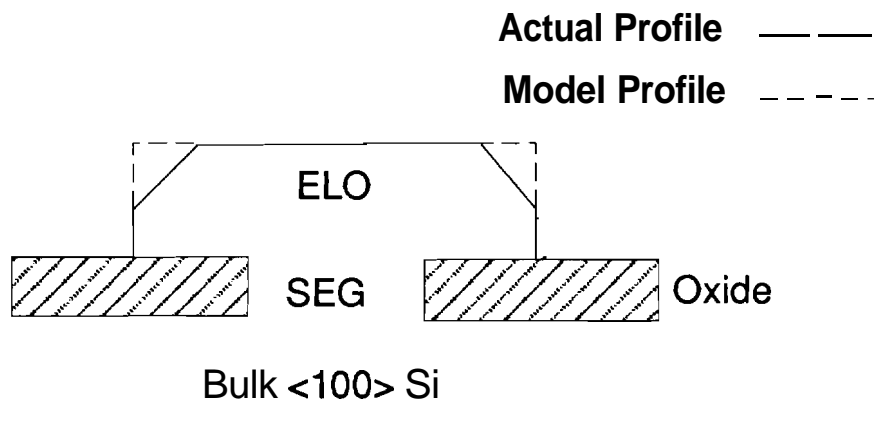


Figure 4.14 Approximation of ELO profile by growth rate model

its two main objectives; it is able to simulate the growth of SEG to fill a trench, and the horizontal growth of ELO to ultimately yield thin planar sheets of SOI.

Provisions have been made to leave the model flexible. It can be tuned to fit a specific reactor by changing empirical constants. The list of tuneable parameters and their default values are listed in Table 5.3. In most cases where the flow is

Emp. Const.	Description	Default Val.
x	Exponent:DCS term	0.7
y	Exponent:HCl term	1.2
z	Exponent: H2 term	1
Ag	Pre-exp. Const.: Growth	53000000
Ae	Pre-exp. Const.: Etch	17600
EAg	Act. Energy: Growth	52260 Kcal/mol
E Ae	Act Energy: Etch	31120 Kcal/mol
m	Slope: Press. Sca. Factor	0.06
C	Intercept: Press. Sca. Fact	-1.4

Table 4.3 Tuneable Parameters and Default Values

overwhelmingly Hydrogen, P_{H_2} can be replaced by system pressure P. The suggested tuning method for the model is described in the following section.

4.4 Suggested Tuning Procedure for Individual Reactors

A few runs at $HCl=0$ could be done to isolate the growth parameters from the etch parameters. A wide range of temperatures 800-1000°C would ensure a more accurate representation of k_g . Some runs at constant HCL, DCS, H_2 , and P values, for a range of temperatures could be done to extract k_e . The model tuning method follows the flow chart in Figure 4.15.

1. y, z are chosen if different from the default values, and x evaluated. Using the $HCl=0$ runs, k_g is extracted. $HCl \neq 0$ data can be used to estimate k_e .
2. These numbers must be checked against any other data at the same pressure. If the fit is not a good one, y, z must be chosen again.

3. If the fit is good, the model should be tested against data at other pressures. A may be re-evaluated by the method used in Section 5.2 if the correspondence is poor.

4. After modifying A, it is possible that the model does not completely follow the full swing; of the data at different pressures; i.e. $GR(\text{model}) < GR(\text{high T data})$, and $GR(\text{model}) > GR(\text{Low T data})$. In this case, E_{A_g} has to be increased, and A, has to be correspondingly modified. On the other hand the model may overestimate the data swing; i.e. $GR(\text{model}) > GR(\text{high T data})$, and $GR(\text{model}) < GR(\text{Low T data})$. Now E_{A_g} is too large and may have to be decreased. For the model fitted in this work, a change of 1.2% in the E_{A_g} obtained by regression was necessary.

Though error estimates for individual reactors may vary, 5% could be a reasonable estimate for any change in E_{A_g} . Another alternative is to try a different combination of x,y, and z.

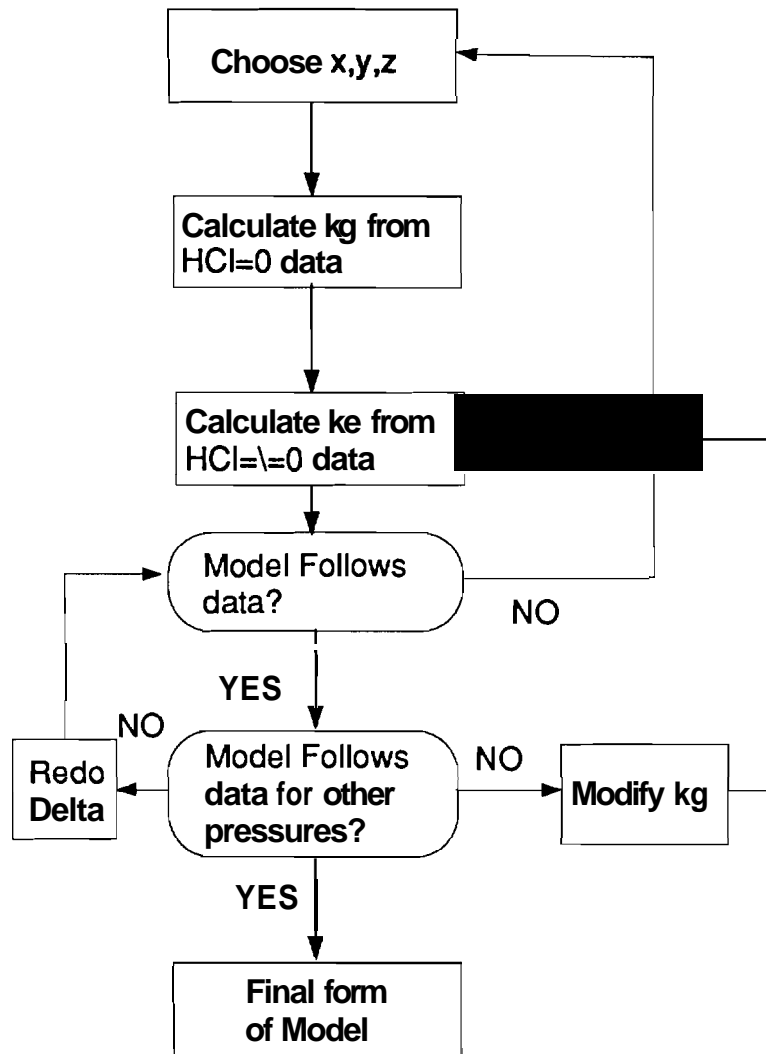


Figure 4.15 Model Tuning Flow Chart

4.5 Modeling of Oxide Coverage Effect on Growth Rate

In Section 2.2.6, the effect of oxide coverage on growth rate was of SEG Silicon was discussed. In Figure 2.12, it was seen that for a low percentage of oxide coverage on the surface, the variation in growth rate was small. At higher percentage coverages the difference in growth rates were more significant. Friedrich's data [46] was expressed. as shown in Table . The growth rates at 30% coverage was taken to be the 'baseline' measurement. Growth rates at the other data points were divided by this 'baseline' value to yield the factor by which the growth rate changed for increased oxide coverage.

% Coverage	GR(um/min)	GR Multiplication Factor(F)
95	.4	2.12
90	.34	1.8
50	0.2	1.05
30	0.19	1

Table 4.4 Increase in Growth Rate with Oxide Coverage at P=150 Torr

The increase was modeled as an exponential function. Excellent agreement was obtained for an expression of the form;

$$Increase = e^{0.9(\%Coverage)^3} \quad [4.22]$$

where % coverage is 0.3 for 30%, 0.5 for 50% etc. This model is plotted against normalised data in Figure 4.16. 99.5% correlation was obtained between the model and the normalised data. Since this is a global effect evident over the whole wafer surface, the growth rate expression can be simply multiplied by the 'Increase' factor to predict growth rates when the oxide coverage is greater. In keeping with the practice of leaving; the model flexible to individual user needs, the expression can be written

as;

$$Increase = e^{k_{ox}(\%Coverage)^p} \quad [4.23]$$

where k_{ox} and 'p' are the modifiable constant and exponent respectively.

The effect on growth rate of different oxide thicknesses is less predictable(Figure 4.17). At smaller mole fractions, Friedrich found the growth rate reaching a minimum before increasing again. At larger mole fractions, for thicknesses below 1000 Angstroms, the decrease in growth rate was monotonic for increasing oxide thickness. The variation is seen to be more significant at thicknesses below 200 Angstroms. Since field oxides are normally in the realm of 1000 Angstroms thickness (or greater), it is expected that the variations are smaller, and may be neglected.

The modified expression for growth rate can thus be written as:

$$GR = e^{k_{ox}(\%Coverage)^p} \left(\frac{k_g(P_{DCS})^z(P_{H_2})^x - k_e(P_{HCl})^y}{\Delta} \right) \quad [4.24]$$

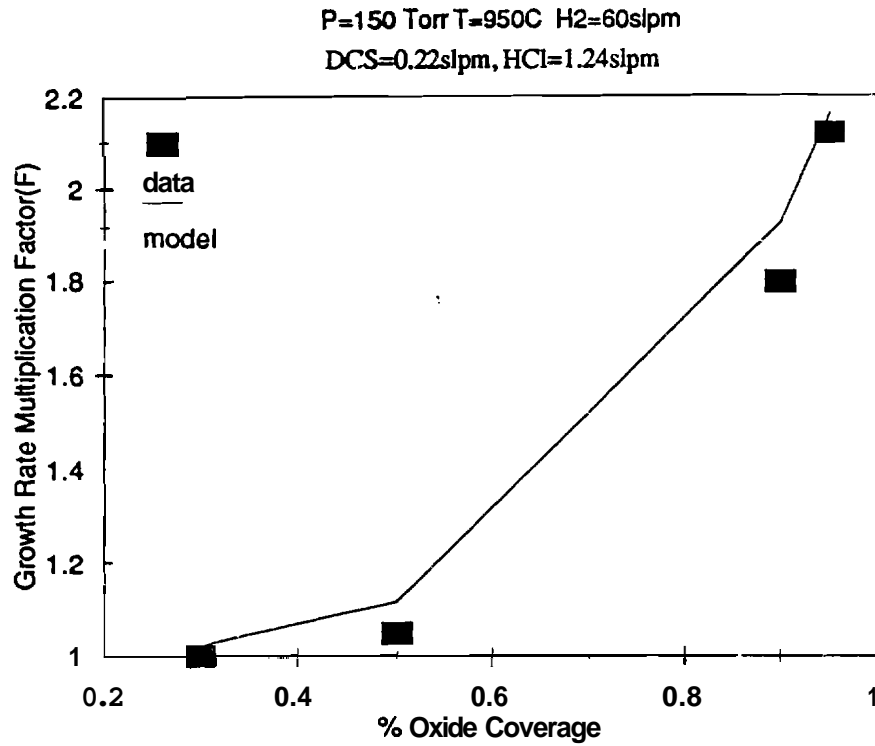


Figure 4.16 Comparison of Oxide Coverage model to normalised data

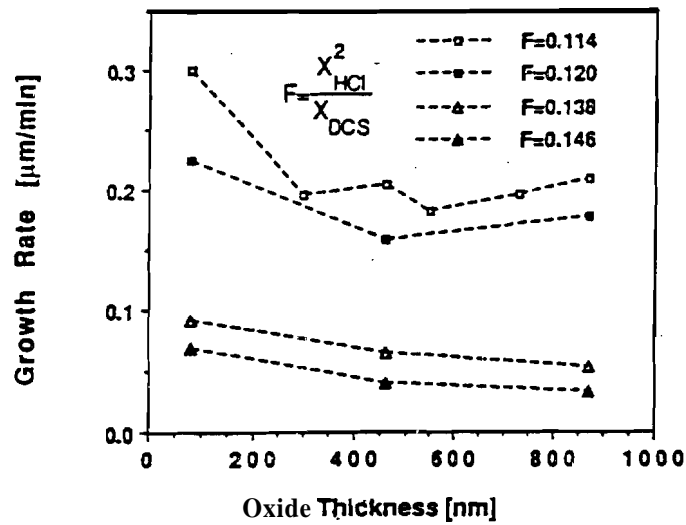


Figure 4.17 Variation of Growth Rate with Oxide Thickness at 150 Torr [46]

5. CONCLUSION

5.1 Summary of Work

In this work an effort has been made to model the growth rate of selective epitaxial Silicon in a DCS-HCl-H₂ system using a Gemini-I pancake reactor in the Purdue University Laboratory. A detailed study of the reactions and mechanisms involved in selective silicon deposition was undertaken. A number of models for Silicon growth in the existing literature were adapted for growth conditions at Purdue University, and tested against experimental data. A new semi-empirical model for Selective Epitaxial Growth(SEG) was created that provided the best fit to our experimental data.

A number of selective epitaxy runs were carried out at 40 and 150 torr pressures, and temperatures ranging from 970–920°C. HCl/DCS ratios were varied from 3–7 and the growth rates at all the above conditions were measured. This data was used in conjunction with growth rate data for more than 50 epitaxy runs at temperatures from 820–1020°C, and pressures from 40–150 torr, that had been carried out previously. Experiments were done to determine the reactor drift in the time intervening between the two sets of runs. The drift was found to be negligible. Varying wafer thicknesses from 20mil–25mil were found have no significant effect on the growth rate.

The model for SEG growth rates was expressed as a sum of growth and etch terms. Earlier the theoretical models had expressed the growth term as being dependent on the system pressure(P), while the etch term varied as P². This was found to predict that the growth-etch threshold for SEG moved to lower HCl/DCS ratios as the pressure increased, while experimental evidence indicated a move to higher HCl/DCS ratios. The present model corrects this by making the etch rate dependence on system pressure smaller than the growth rate pressure dependence. The activation energies

of growth and etch were found to be **52.3 kcal/mol** and 31.1 kcal/mol respectively. The activation energies, pre-exponential constants, and pressure dependent scaling factor were all set up to be varied, so that the model can be tuned to give the best fit possible for individual reactor data.

5.2 Recommendations

At this time there is some uncertainty about which surface species dominates coverage at different temperature ranges. If this is determined, different versions of the present expression can be used in each temperature range, where a certain surface species is dominant. It has also been indicated that the activation energies are dependent upon the flow rate of HCl in the system. The ratio of Hydrogen flow to DCS flow is also found to cause some anomalies in the growth. If these observations are investigated and quantified, there is room for more accurate modeling of SEG/ELO of Silicon. It would seem that the growth rate of $\langle 110 \rangle$ facets have a different energy of activation, from the $\langle 100 \rangle$ facets. Further work to determine $\langle 110 \rangle$ plane growth rates could lead to prediction of gradually sloping, or abrupt ELO profiles at different growth conditions.

APPENDIX



Characterization of Oxidation Furnaces

The six oxidation furnaces normally used for Silicon Dioxide growth at Purdue University, have slightly different growth characteristics, as they are used for differing purposes. The oxidation tubes numbered 1–6 have functions as below:

Tube Number	Tube Function
1	Wet/Dry 0 2
2	Phosphorous Drive
3	Boron Drive
4	Steam
5	Gate Oxides(Dry/TCA)
6	Phosphorous Predep

Table .1 Oxidation Tube Function

The reasons for differing growth characteristics could be (a) due to a variation in temperature profiles, and (b) due to contamination of the tube. The second would occur because Tubes 2 and 6 can have some Phosphorous deposited on the walls, which could alter the oxide growth rate on the wafer. Similarly oxidation in Tube 3 may be influenced by Boron contamination. It would be desirable to characterize oxide growth in each furnace, so that oxidation could be predicted more accurately in each tube.

It was appropriate to characterize the tubes at 950°C and at 1050°C , as these temperatures are commonly used for oxide growth. Using this data, oxide growth at intermediate temperatures can also be estimated. Two oxide thicknesses were picked for Wet and Dry oxidation. Values of $600 / \text{AA}$ and $1500 / \text{AA}$ were chosen for Wet oxidation, and $250 / \text{AA}$, and $500 / \text{AA}$ were chosen for Dry oxidation. These values were picked so that very long oxidation times were avoided for the two temperatures. TSUPREM3 was used to come up with an estimate of the times required for each thickness.

3" N-type $\langle 100 \rangle$ wafer quarters were used for each condition. The standard run sheet was followed. Average push and pull times were kept to 3 minutes. At

950°C, push and pull steps were done in Nitrogen while dry Oxygen was used for 1050°C. Thicknesses were measured at 4 points on the wafer [50], and averaged. The following graphs indicate the average thicknesses obtained for each of the conditions in the table above, for every tube. Using these graphs an estimate of the process parameters may be made for oxide growth.

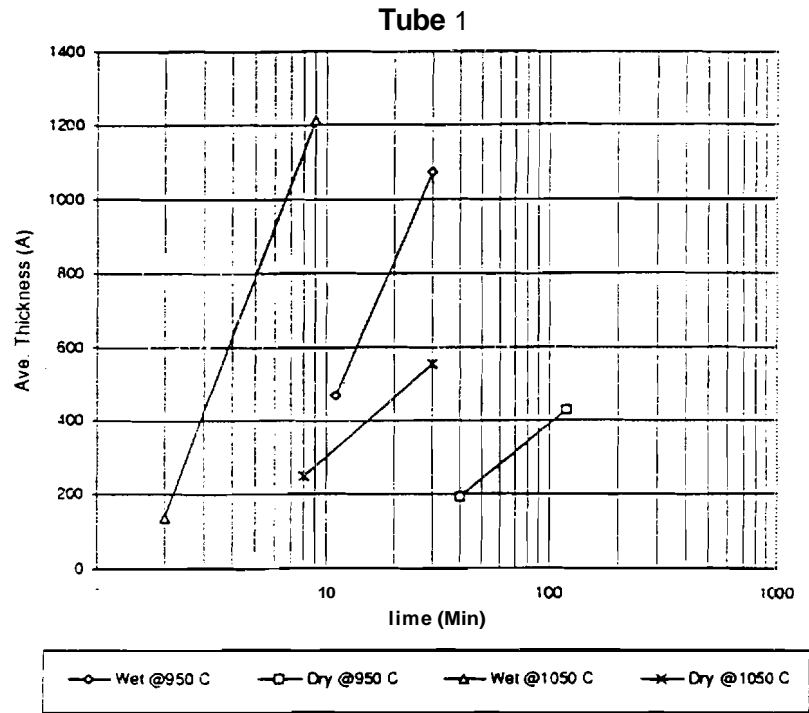


Figure .1 Tube 1 [50]

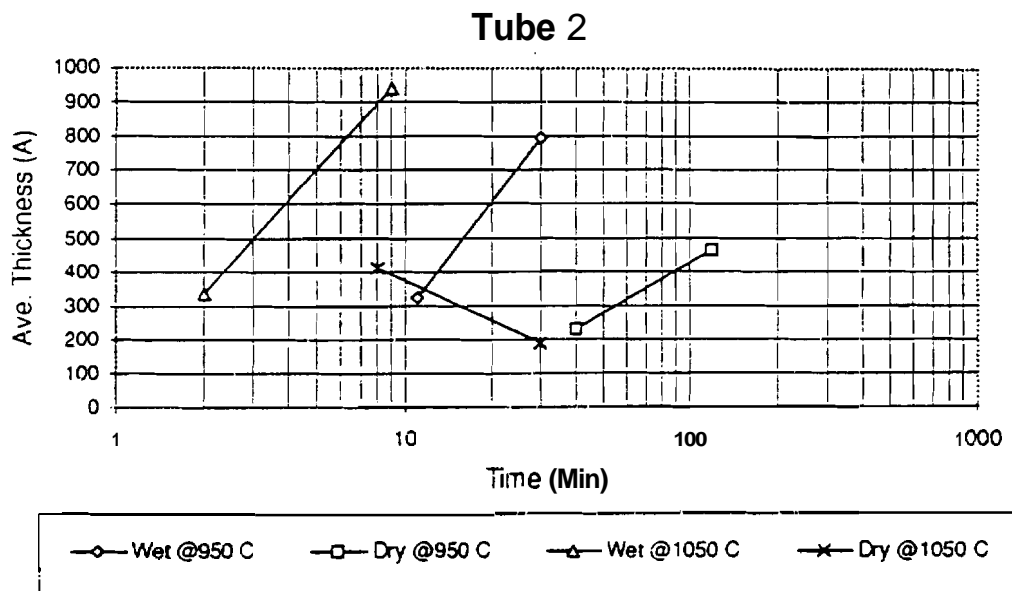


Figure .2 Tube 2 [50]

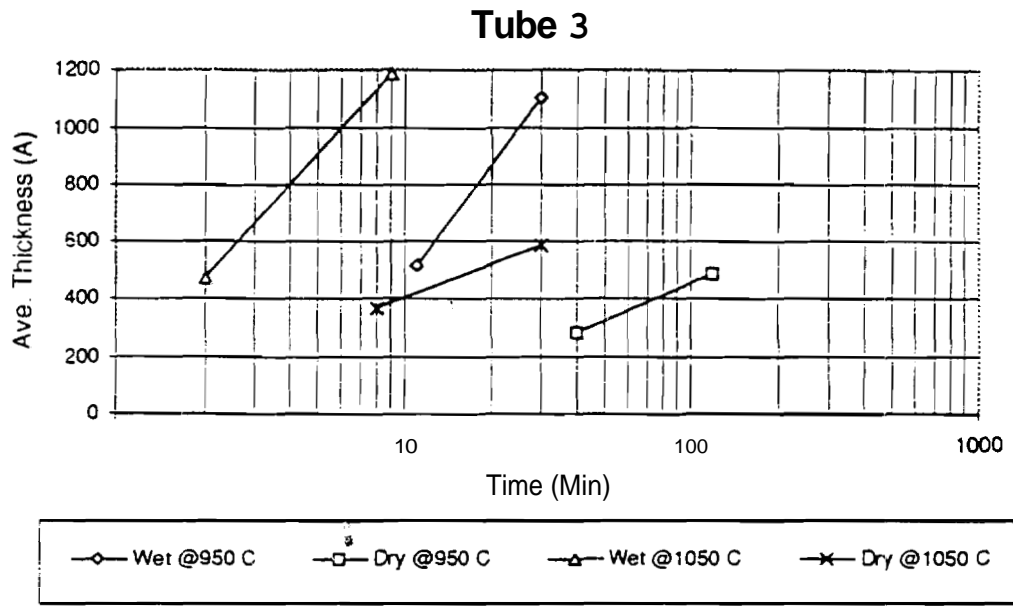


Figure .3 Tube 3 [50]

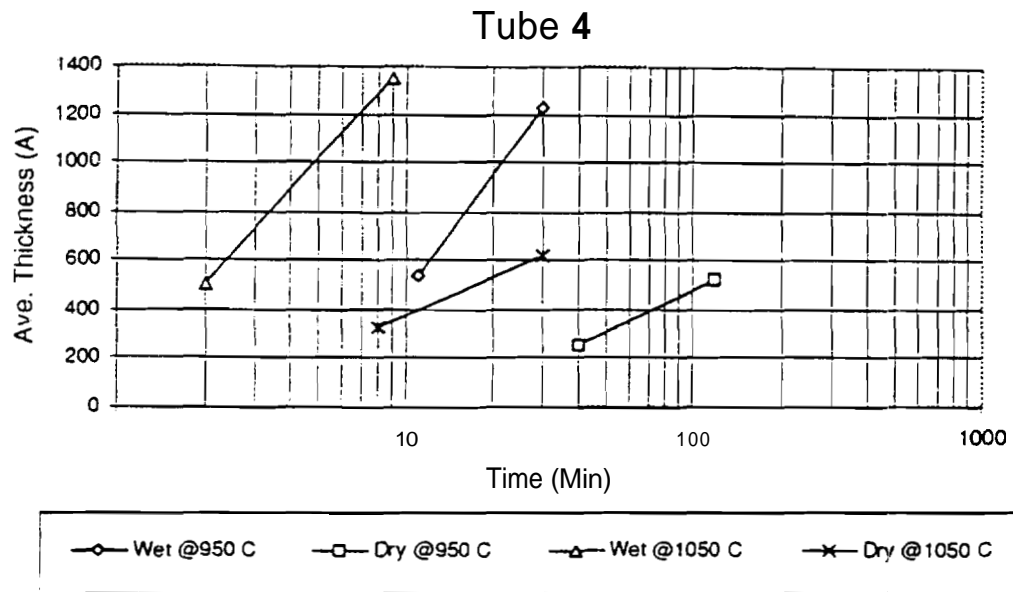


Figure .4 Tube 4 [50]

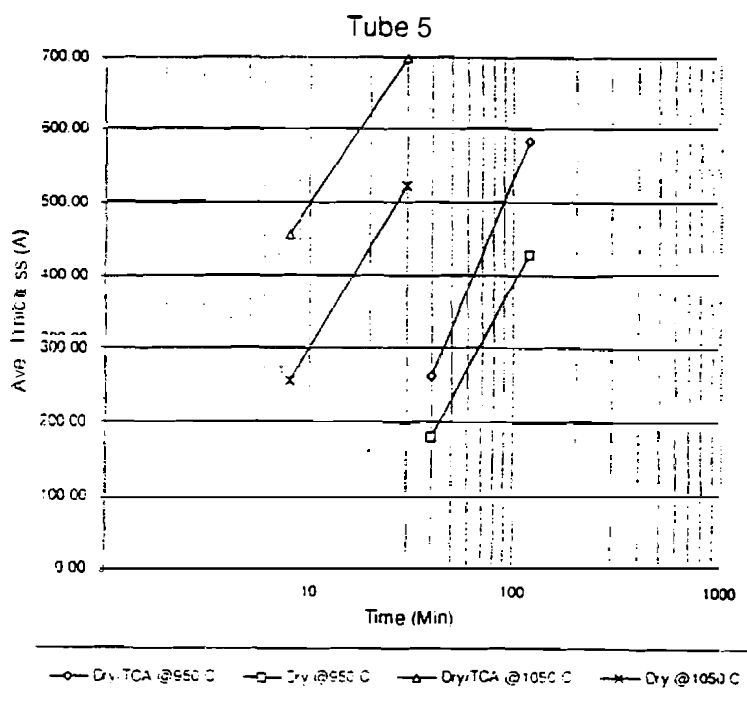


Figure .5 Tube 5 [50]

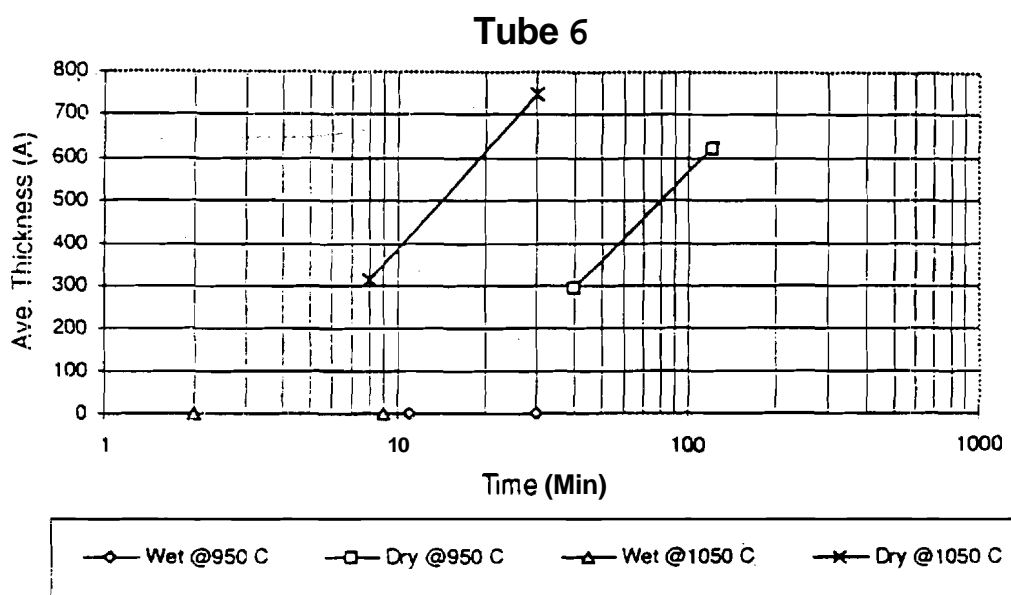


Figure .6 Tube 6 [50]

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LIST OF REFERENCES

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