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TECHNICAL REPORT

AN INVESTIGATION OF FLICKER REDUCTION USING AN ADAPTIVE VAR COMPENSATOR

by

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ABSTRACT

A detailed computer model of a three-phase power network which includes inductive loads, resistance welders and an Adaptive Var Compensator (AVC) has been developed. The system configuration and parameters correspond to an industrial customer served by a large electric utility. Welder operation produces severe cyclic flicker which leads to customer complaints. Computer studies have been conducted to determine the effectiveness of the AVC on the reduction of observable flicker at neighboring loads. Flicker severity was determined using the UIE / IEC flickermeter technique adopted for 120-V incandescent lamps. Different control strategies involving the AVC have been considered and compared with respect to flicker reduction. An innovative: Flicker Adaptive Control (FAC) strategy is proposed for the AVC. The control algorithm requires knowledge of the system line impedance; however, it can be used for both power factor correction and flicker reduction, which is an advantage over previous control methods. The measurement technique used in the FAC is accurate even in presence of heavy system distortion.

1. INTRODUCTION

1.1 Power System Description and Statement of the Problem

Welders, used in a variety of industrial applications, are well-known as one of the causes of voltage fluctuations in electrical networks. In this thesis, an industrial plant which includes large resistance welders is investigated. A simplified one-line diagram of the utility network studied, which is typical of many industrial loads, is shown in Figure 1.1. The welding load includes three welders that are connected line-to-line at the 480-V utility bus forming a **A** - configuration. In the given plant, all three welders are fired concurrently for several electrical cycles with a repetition or duty interval of approximately one second between welds. Since the power rating of the welders represents a major portion of the total power demand, the bus voltage experiences substantial distortion in the form of RMS dips. At the high-voltage bus, or Point of Common Coupling (PCC), the utility serves other commercial customers who complain about light fluctuation and visually noticeable changes in lamp brightness.

The solution to this type of power quality problem, in general, can be very costly and may even require installation of a substation closer to the load. Alternative solutions may be achieved by considering devices such as Static Var Compensators (SVC's), converter-based devices such as the Static Condenser (STATCON) or Static Compensator (STATCOM), or hybrid devices such as the Power Quality Manager (PQM) [1 - 2]. These devices involve high-frequency semiconductor switching devices such as GTOs or IGBTs and, therefore, may be very expensive. Even though a device such as the PQM may solve the power quality problem, its installation may not be justified financially for the utility.

A more affordable solution, however, may be achieved by reducing rather than completely eliminating the flicker in order to reduce the hardware costs. In this thesis, an Adaptive Var Compensator (AVC), which is a bank of thyristor-switched shunt-connected capacitors operating on a cycle-by-cycle basis [3 - 8] was investigated.

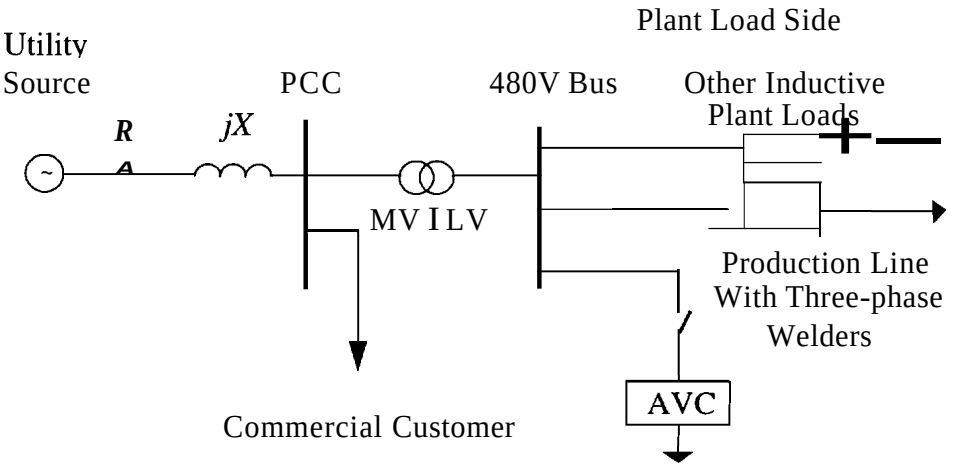

Figure 1.1: Simplified one-line diagram of the utility power system.

To determine the overall effectiveness of the AVC and its control strategy on the reduction of the level and severity of the flicker, a detailed computer model of the system was developed. Moreover, a method of quantifying the observable flicker was implemented so as to evaluate the effectiveness of the AVC and to set the stage for the comparison of alternative solutions.

1.2 Application of the AVC for Flicker Reduction

Sudden changes in load will cause a corresponding deviation in voltage at the load bus and the PCC which is a function of system impedance. In this regard, the welders, whose KVA requirements are significant when compared to the system capacity, have been recognized as a major cause of flicker. The repetitious welding operations will result in RMS voltage dips and, in turn, in cyclic flicker. The other significant characteristic of arcing loads, such as welders and furnaces, is that the major portion of the power drawn during operation is reactive. The dominant reactive current needed for the electric arc stabilization results in a corresponding voltage drop in the line impedance. Thus, the RMS voltage dip can be reduced by compensating the reactive demand during welding. Overcompensation can even boost the system voltage, and may, therefore. be used as a mea-

sure of compensation for the part of voltage drop due to the active current. This reasoning makes an AVC appropriate not only for power factor correction but also for voltage regulation and flicker reduction. In particular, [8] provides an algorithm for flicker reduction so that AVC operates in mode of a flicker controller.

1.3 Flicker Phenomena and Terminology

The use of rapidly varying loads such as electric furnaces, arc welders, large motors, etc. have generated the need for the evaluation of their effect on the power system, especially in the present-day marketplace, wherein electric utilities are faced with the competitive challenge to provide high-quality power to all customers. The term "flicker" is strongly associated with the operation of varying loads. Flicker involves voltage fluctuation and its effect on the lighting system resulting in changes in luminance and consequent irritation of human vision. The flicker problem is common to many utilities and, therefore, it is indeed an important issue in today's competitive environment.

The type of voltage fluctuation associated with lighting is commonly termed "voltage flicker", which can be divided into two general categories, namely, cyclic and non-cyclic. The cyclic voltage flicker results from periodic loads such as welders as in the given system. Non-cyclic voltage flicker, on the other hand, may be caused by a motor starting or breaking on a random schedule. The operation of an arc furnace is commonly followed by a mixture of both cyclic and non-cyclic voltage flicker.

Considering the filament lamps in the lighting system, cyclic voltage flicker can be conveniently expressed as the RMS value of the modulating waveform divided by the RMS value of the fundamental voltage. For a non-cyclic case, it also can be expressed as the change in voltage divided by the average voltage. This ratio can then be multiplied by 100, so that the result would represent a percent of change. The measurement of the voltage flicker involves the determination of the system RMS voltage variation and the frequency, or even a band of frequencies, at which it occurs. The maximum permissible voltage disturbances that the system can tolerate without complaints about light flicker and annoyance is termed ***"Light Flicker Voltage Requirements".*** Unfortunately, as yet there are no established standards defining acceptable voltage flicker levels that are used

consistently and uniformly in the power industry today in North America. Each utility uses its own recommendations based on their individual experience in flicker or chooses from the variety of perceptible limit curves that are published. These curves can be used as general guidances in determining whether flicker is a problem. Among them, the IEEE Standard 141-1986, ***Recommended Practices for Electric Power Distribution for Industrial Plants,*** IEEE Standard 519-1992, ***Recommended Practices and Requirements for Harmonics Control in Electric Power Systems, Section 10.5,*** *"Flicker"*, and the well-known ***General Electric Flicker Curve*** are notable.

It is important to distinguish "Light Flicker" as a subjective impression of luminance fluctuation of light emanation or gleams from a lamp. The fluctuation qualities resulting from changes in brightness, modulation of intensity, or variation in color may be sufficient to be perceptible to the human eye. The human vision, in turn, is a very complex system consisting of optical, neurological and cognitive elements, which provide the eye with the ability to adapt to illumination over a wide range of intensities..The smallest stimulus capable of producing a recognizable sensation with 50% probability of detecting the presence of this stimulus is called the ***Visual Threshold.*** Tests have shown that the human eye is most sensitive to light modulating frequencies in range the of 8-10 Hz. In this band, even a very slight voltage flicker of about 0.3-0.4% in a system with incandescent lamps is noticeable and can be even annoying to certain individuals. The permissible amount of voltage fluctuation to avoid complaints about the light flicker is very difficult to determine succinctly or precisely for many reasons. The light fluctuation depends to a great extent on the type of lamps used, their wattage, design, etc. The method used to predict light flicker from an incandescent lamp may not be the same as it would be for a fluorescent lamp, which, in turn, depends on the type of ballast circuit. Finally, the reaction of human observers is a subjective matter, and varies quite widely from person to person.

1.4 Objective Method of Determining Flicker Sensation and Severity

The International Electrotechnical Commission (IEC) and the 'Union International for Electroheat (UIE) have developed both a flicker standard and a precise technique for flicker evaluation presented in IEC Publication 868 and its amendment [12 - 15]. Origi-

nally designed for application in European countries or other countries with 230-V service, the UIE / IEC flickermeter incorporates incandescent lamp characteristics (60-W 230-V standardized filament gas-filled lamp) through a weighting filter curve, and evaluates short- and long-term flicker severity by well-defined models and :statistical methods. This method provides more consistency in meanings and results of its application than other published curves. That explains why, recently, a substantial research effort has been devoted to worldwide application of the UIE / IEC Flickermeter and in particular for 120-V lamps used in North America.

Further adoption of the device for use in North America and worldwide [18 - 20], along with its modification for discharge fluorescent-type lamps with magnetic or electric ballasts, and establishing better flicker standards represent joint research efforts on the part of the IEEE PES task force on light flicker [10], (Working Group on Voltage Quality), the Electric Power Research Institute (EPRI), the Power Electronics Application Center (PEAC), the Hydro-Quebec, Canada, the Canadian Electrical Association (CRA), the University of Technology, Graz, Austria, the University of Pennsylvania, and Purdue University among others. The number of utilities involved in the development of such standards is also growing with today's ever increasing requirements for power quality.

2. ADAPTIVE VAR COMPENSATOR (AVC)

2.1 AVC General Description

The AVC was initially developed by researchers at the University of Washington as an Adaptive Power Factor Controller (APFC) to provide of a device which would automatically compensate for rapidly varying reactive power demands frorn low power factor equipment in electrical systems. Later, the APFC evolved into a device having much wider application in the power quality area by introducing new modes of operation and control strategies. The voltage class of AVCs lies in the range of 480 V to 15 KV, and the capacitor size ranges from 50 Kvar to several Mvar to serve the needs of various utilities on different levels of electrical networks. Subsequently, many modifications have been developed to enhance the AVC's functionality and to address some specific on-site requirements.

The main features of AVC are as follows. It is an electronically switched shunt capacitor bank. The AVC compensates each phase locally and independently, which makes it applicable to unbalanced systems. The three phases of the AVC can be Y - connected with or without grounded neutral. Alternatively, the phases can be A - connected. The amount of reactive power provided to the system is determined on a cycle-by-cycle basis, so that it can adapt to rapid load variations. Further AVC design modifications include possible half-cycle resolution. Parallel capacitors or bits are arranged in a binary ratio to minimize quantum effects and provide more-or-less linear resolution. Each capacitor bit is pre-charged to the peak value of the phase voltage. In most cases, a negative precharge is used for all capacitors. The solid-state switches are protected by snubbing circuits against high $\frac{dv}{dt}$ and $\frac{di}{dt}$, which also provides damping in case of false triggering. Capacitor bits are switched on when the voltage across the thyristor-diode pair is zero, and are switched off when the current crosses zero in a negative half-cycle voltage peak. That

condition minimizes transients and harmonics due to the fast switching. Reactive currents are measured directly by sampling the phase currents at the positive-to-negative zero-crossing of the phase voltage.

The AVC can operate in one of the following modes:

Reactive Power Compensation (RPC) mode: maintaining unity or other desired power factor at the point of installation, within accuracy of the smallest capacitor bit and with the limitation of total capacitance of the AVC per phase.

Voltage Support mode (VS) or voltage control: regulating the voltage at the point of installation at some pre-specified level using under- and over-compensation.

Flicker Control (FC) mode: used to reduce the fast voltage fluctuatiion at the place of installation.

The AVC can implement any of the above modes according to a user-specified time-table or schedule, remotely or manually.

The 480-V version of the AVC studied herein has a capacitor bank which consists of three switched capacitor bits rated 46.8 Kvar, 93.6 Kvar, and 187.2 Kvar, implying that it can deliver 327.6 Kvar independently per phase in 46.8-Kvar steps. A modification involves installation of a fourth capacitor bit of the same size as the largest bit, but pre-charged to a positive value, which would permit control on a half-cycle basis that may be useful in certain conditions.

2.2 Structural Configuration and Operation

A somewhat simplified functional diagram of the AVC is shown in Figure 2.1 which illustrates one phase of the AVC with three capacitor bits. All three phases are identical and are Y - connected with the neutral grounded.

In the given AVC configuration, each solid state switch (thyristor-diode pair) may represent many such pairs stacked on top of each other in a series string in order to withhold the required maximum voltage. Because the bit capacitors are pre-charged, the voltage applied to the switch is equal to the peak-to-peak value of the corresponding phase voltage.

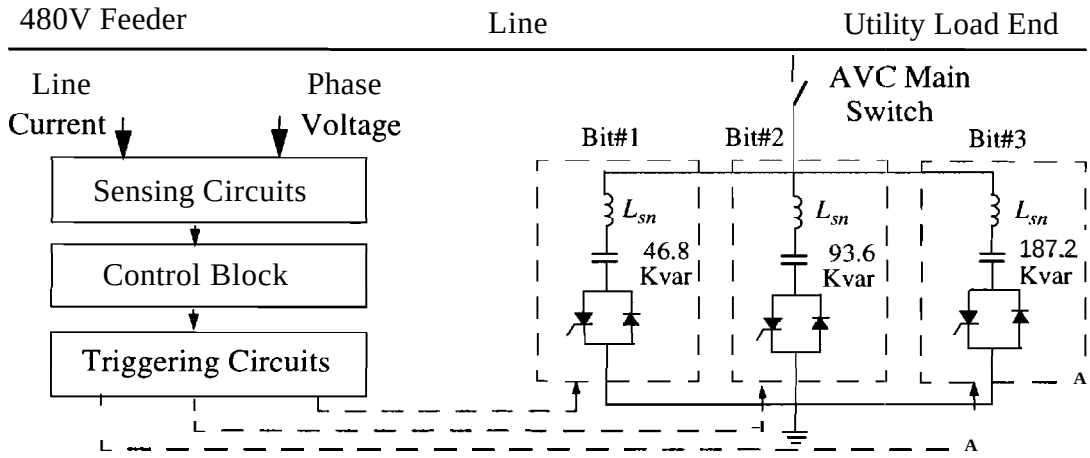

Figure 2.1: Basic structure of the AVC (per phase).

The switch-diode modules, the parameters, and the number used in series depend on the size of the capacitor, the class of voltage where the AVC is to be used, the availability of such devices and, finally, economic factors. The snubber circuit in each string is needed for several reasons. The main purpose is to limit the $\frac{di}{dt}$ and $\frac{dv}{dt}$, and, therefore, to protect the thyristor against false triggering and breakdown by damping the current. It also provides balanced voltage sharing when more than one switching moclule is used in the string. An AVC bit is shown in somewhat more detail in the Figure 2.2. Operation under normal conditions implies switching "in" and "out" of capacitors only at the instant the voltage across the switch and the current are zero. Since the main capacitors are negatively pre-charged through the diodes, that instant occurs when the corresponding phase voltage goes though its negative peak. Therefore, any combination of capacitor bits can be activated on a cycle-by-cycle basis at a point which minimizes transients. Switching at any other moment causes false triggering, which is followed by current oscillations. The magnitude of this transient oscillation can be quite large depending on system parameters, and can overstress the solid-state switching devices to the point of damage.

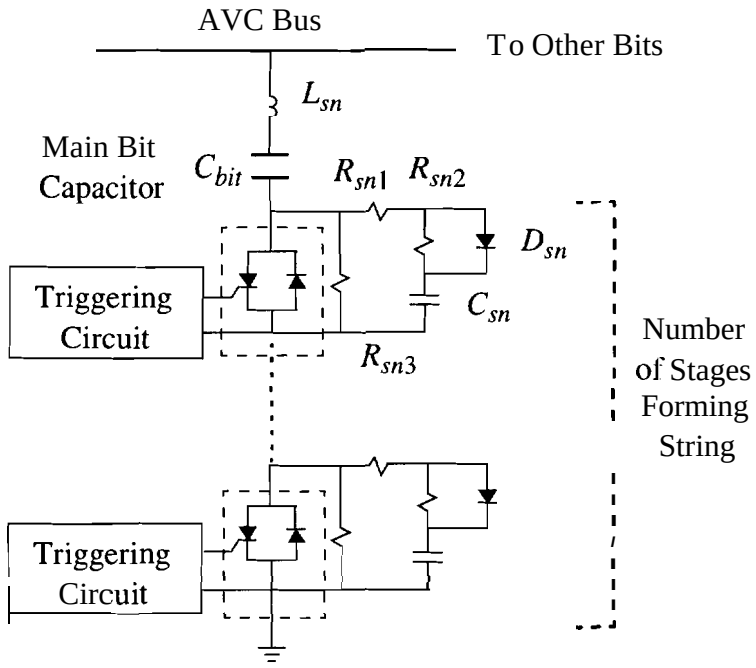

Figure 2.2: AVC bit diagram showing possible stages and snubber circuits.

Such false triggering, which may happen in the presence of large disturbances in the system, can make the situation even worse by introducing oscillations of large currents. Such events, naturally, are very undesirable.

The snubber circuit depicted in Figure 2.2 provides high impedance in the reverse direction and somewhat lower impedance in the forward direction. The resistor R_{sb2} and the capacitor C_{sn} provides damping and allow the capacitor to discharge slowly in the forward direction. The small discharge of the capacitor to a value somewhat smaller then the peak voltage is needed for a voltage zero-crossing to occur across the ,thyristorand therefore soft switching. Otherwise, if the capacitor becomes slightly over-charged, for instance due to possible voltage disturbances, there will be a transient. In some cases, the control logic can skip firing for several cycles, thereby missing the zero-crossing signals. In some AVCs, instead of monitoring the voltage across the switch, a phase voltage zero-crossing with a 90° time-delay filter is used to generate the signals for triggering. The

inductor L_{sn} limits $\frac{di}{dt}$, and the resistors R_{sn3} distribute the shared voltage when the thyristors are off. Thus, the overall strategy is to switch in and out a necessary combination of capacitor bits for any number of complete electrical cycles without injecting harmonics due to commutating transient. The triggering circuits, as a rule, consist of two sections separating the switching circuitry on the high-voltage side from the low-voltage control side through either an optical or a magnetic link.

2.3 Binary and Non-binary Capacitor Sizing

Each phase of the AVC, in general, may contain several capacitor bits which are similar in structure. The capacitor bits, however, differ in size. All possible combinations of capacitors provide discrete levels of reactive power that the AVC can deliver. The three-bit AVC, with capacitors arranged in a binary manner as shown on the Figure 2.1, is widely used in many applications because of the simplicity of its control implementation. The capacitor sizes for bits 1, 2 and 3 are 46.8 Kvar, 93.6 Kvar and 187.2 Kvar, respectively. The binary sizing allows an evenly-spaced range of capacitance in discrete steps, which are quantized within the size of the smallest bit, from zero up to the sum of all available capacitors. The number of possible combinations in a binary structure is 2^n, where n is the number of bits. Thus, the number of active steps, not including the zero combination, is 2^n - 1. Therefore, the number of capacitance steps N_c for the three-bit AVC can have any of the values

$$N_c = \{0, 1, 2, 3, 4, 5, 6, 7\} \tag{2.1}$$

The capacitors combination evaluation in this case can be easily implemented by a look-up table, which would have as an input the number of capacitance steps, N_c, and three outputs: the control signals for each of the bits. In a symbolic notation, the combination evaluation can be expressed

$$B_s = \begin{bmatrix} b1 \\ b2 \\ b3 \end{bmatrix} = T(N_c) \tag{2.2}$$

where, $T(N_c)$ is a look-up table function; $\boldsymbol{B}$, is a vector of bit control signals.

The control signal N_c is received from the control block of the AVC, and the vector $\boldsymbol{B}$, is then passed to the triggering circuits. An example of the table function $T(N_c)$ that implements the linear relationship between N_c and the activated capacitance is illustrated in Figure 2.3.

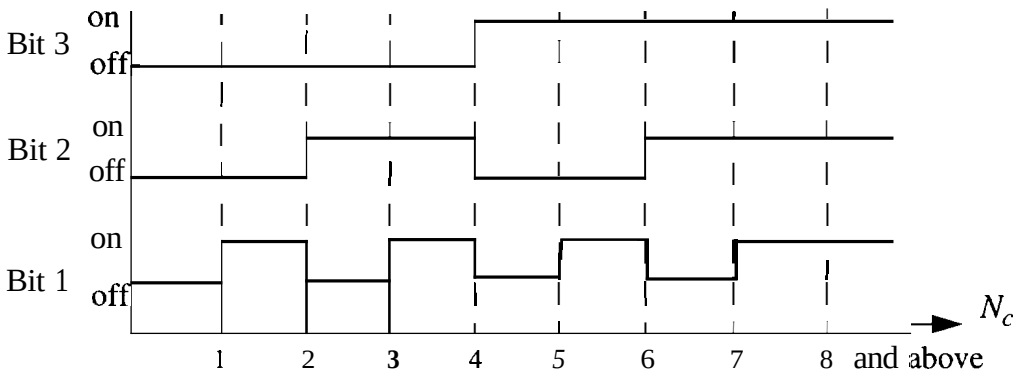

Figure 2.3: Look-up table for three-bit AVC with binary capacitor sizing.

Similarly, for four binary bits, there will be sixteen total combinations and fifteen linearly spaced active steps. The table function $T(N_c)$ for this case can be obtained by corresponding modification of the three-bit table. It is also important to note that the accuracy of compensation directly depends on the step size, which is the size of the smallest bit - 46.8 Kvar. The resolution, which is the average expected error in compensation, is equal to a half-step.

In AVC applications, it is desirable to have the total installed Kvar sufficient for compensation for the maximum expected reactive demand, and for sufficient over-compensation where it is needed for voltage regulation. The best resolution, which is the smallest change in effective capacitance per step, is obtained if the total capacitor bank is sized in a discrete number of bits, which are, in turn, sized in binary ratio. However, if resolution is not the main issue, and the AVC is used to compensate a larger inductive demand, additional bits can be installed without resizing the existing capacitor banks. If

the capacitance rating of the expansion does not fit into existing binary structure, but is still rated in similar sizes, the bit arrangement can be modified to a non-binary structure with the same resolution determined by the smallest bit. An example of such an expansion is the AVC considered in this thesis, wherein the three-bit version has a total installed capacitance of 327.6 Kvar, with cyclically changing reactive power demand of 500 to 540 Kvar per phase, respectively. In this situation, it is appears reasonable to expand the system to 514.8 Kvar, by adding one more capacitor bit rated 187.2 Kvar. This would fulfill the increased demand within the resolution accuracy. The following table function can be used to implement the proportional relation between N_c and activated capacitance

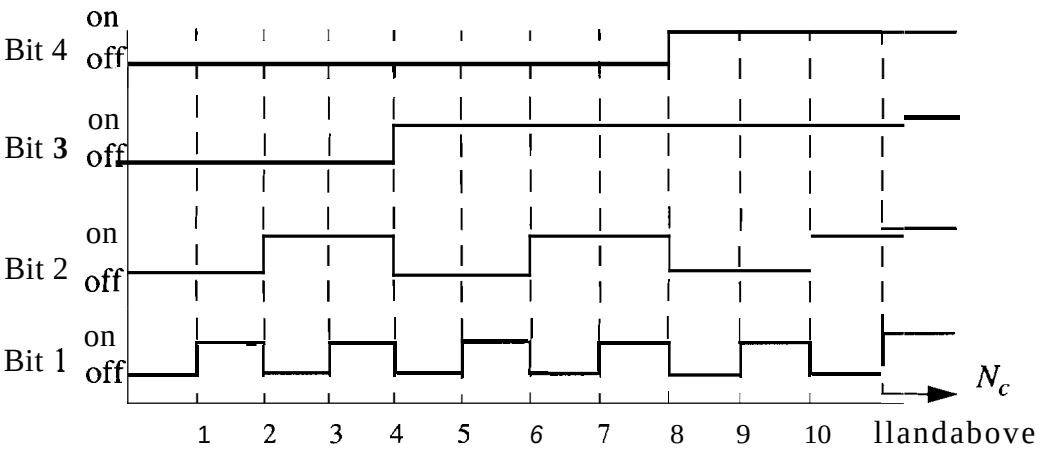

Figure 2.4: Look-up table for the four-bit AVC with non-binary capacitor sizing.

Evenly-spaced gradually-increasing steps are preserved up to eleventh, after which all bits are turned on. The table function (2.2) in this case will have four discrete (0 - for off, and 1 - for on) output signals B_s for each capacitor which are defined for any positive value of input N_c. The rounding technique [8] may be implemented as

$$B_S = T(N_C + 8) \tag{2.3}$$

Equation (2.3) can be used to implement both a "traditional" technique if $6 = \frac{1}{2}$, which would provide an average symmetrical compensation, and a "hysteresis" technique if 6 depends on whether N_c is increasing or decreasing. In some applications, such as flicker reduction, where it is desirable to have the maximum possible capacitance steps available for compensation of expected demands, a "conservative" strategy with $6 = 0$ may be used. In any event, the variable or defined threshold can be adjusted for the desired performance of the AVC with three or four bits.

2.4 Control Modes

The control block of the AVC, depending on strategy used, performs the necessary measurements based upon the current cycle, and produces the number $N_c(n+1)$ which represents the number of capacitance steps to be activated for the next up-coming cycle. In this regard, there exists several control modes.

2.4.1 Reactive power compensation

The Reactive Power Compensation (RPC) mode is perhaps the most simple to implement and therefore widely used, primarily for its direct purpose, namely power factor correction. The capacitive current that the AVC adds into the system is proportional to the capacitance steps being activated; therefore, it can be expressed in term of N_c as

$$I_c = \frac{Q_{st}}{V_{rms}} N_c \tag{2.4}$$

where, Q_{st} is the reactive power in Kvar per step, or the rating of the smallest capacitor bit, V_{rms} is the RMS value of the corresponding phase voltage.

The RPC control provides compensation of the inductive component of the phase load current. When the load current and voltage are not distorted and therefore sinusoidal, the current at the instant when the voltage goes through zero is purely reactive. This fact is used for the measurement of reactive current by simply sampling the phase current at the

positive-to-negative voltage zero crossing. At this instant, the phase current is equal to the peak value of its reactive component. Thereafter, the number of steps for the compensation $N_c(n+1)$ can be evaluated by the following equation

$$N_c(n+1) = \frac{V_{rms}}{Q_{st}\sqrt{2}} I_q(n) \tag{2.5}$$

where, $I_q(n)$ is the sampled current.

Even though such measurement may not be accurate in networks with large disturbances, the fact that it is reasonably fast and easy to implement makes it attractive. The information about the reactive demand becomes available at the beginning of each cycle, and, since the sampling is performed at the positive-to-negative voltage zero crossing, the control system makes its decision and sets the new bit combination through the triggering circuits at the coming negative peak. A diagram of the RPC control is given in the Figure 2.5.

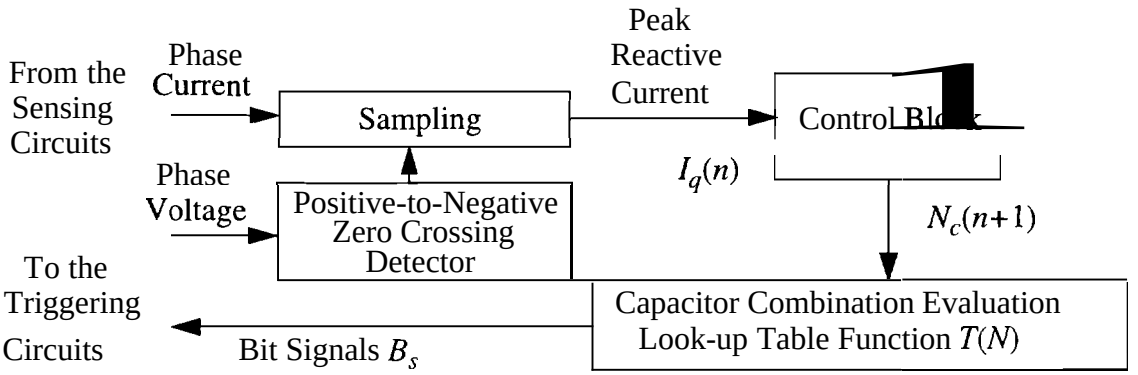

Figure 2.5: Functional diagram of the reactive power compensation.

This type of measurement results in a possible delay, between the instant of time the load has changed and the earliest instant that action can be taken, within a range of 90 to 450 electrical degrees in the best and worst cases, respectively.

2.4.2 Voltage support algorithm

The goal of the Voltage Support Algorithm (VSA) is to maintain the voltage at the point of installation at some pre-specified level known as the reference voltage, and allowing under- and over-compensation. This mode makes the AVC applicable for voltage regulation in electrical networks and does not require any knowledge about the system parameters. However, it requires measurement of RMS voltages for each cycle. The algorithm assumes that the amount of capacitance steps needed to be added or subtracted from the actual combination for voltage regulation, is proportional to the difference between the reference voltage and the currently measured RMS voltage. The reference voltage V_{ref} is also assumed to be expressed as an RMS value. Therefore, this difference can be divided by the voltage-change per step $\frac{dV}{dN_c}$, and then added to the number of capacitance steps previously activated $N_c(n)$. The corresponding equation can be written as

$$N_c(n+1) = N_c(n) + (V_{ref} - V_{rms}(n))\left[\frac{dV}{dN_c}\right]^{-1} \tag{2.6}$$

The corresponding diagram representing the VSA according to (2.6) is given in Figure 2.6.

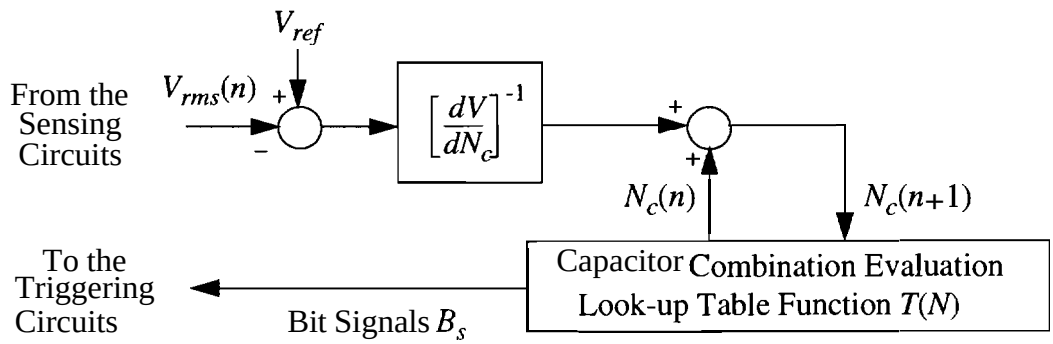

Figure 2.6: Functional diagram of the voltage support algorithm.

The quantity $\frac{dV}{dN_C}$, in general, depends on system parameters and perhaps load, and is not easy to establish precisely. Authors of [8] investigating several methods including the neural network, came to the conclusion that simple averaging can be sufficient. That is, whenever bits are switched on or off, the resulting RMS voltage change per step is computed taking into account of the average $\frac{dV}{dN_C}$. However, for cyclically changing loads, with good approximation, (2.6) can be rewritten even more explicitly

$$N_c(n+1) = N_c(n) + (V_{ref} - V_{rms}(n))\left(\frac{Nc(k-1) - Nc(k)}{Vrms(k-1) - Vrms(k))}\right) \tag{2.7}$$

where n represents cycles counting, and k stands for each change in voltage that causes the AVC to switch bits. This means that $\frac{dV}{dN_C}$ calculated from the previous change can be used to determine approximately the capacitance steps to be activated when the next change occurs.

2.4.3 Flicker control algorithm

The Flicker Control Algorithm (FCA) strategy was set forth in [8] by the original developers of the AVC. As in the case of VSA, the FCA does not require information about the system parameters such as line impedance, etc. The goal of this control is to compensate for fast voltage changes while allowing long-term voltage deviations such as steady-state daily variations. This can be achieved by modifying the VSA, as was described previously, but making the reference voltage floating and keeping track of the long-term voltage variation. Thus, the reference voltage may be expressed as a function of the actual system voltage using Laplace notation as

$$V_{ref}(s) = G(s)V_{rms}(s) \tag{2.8}$$

In (2.8), the transfer function $G(s)$ represents the first-order low-pass filter

$$G(s) = \frac{1}{\tau s + 1} \tag{2.9}$$

The time constant τ can be selected so that allowable voltage variations will not produce

an impact on the flicker; therefore, its reasonable value may lie in the range of one to several seconds, and may need to be adjusted on site. Incorporating this modification into (2.7) yields expression for the FCA.

$$N_c(n+1) = N_c(n) + (G(s) - 1)V_{rms}(n)\left(\frac{N_c(k-1) - N_c(k)}{V_{rms}(k-1) - V_{rms}(k))}\right) \qquad (2.10)$$

A block diagram illustrating the implementation of (2.10) is shown in Figure 2.7

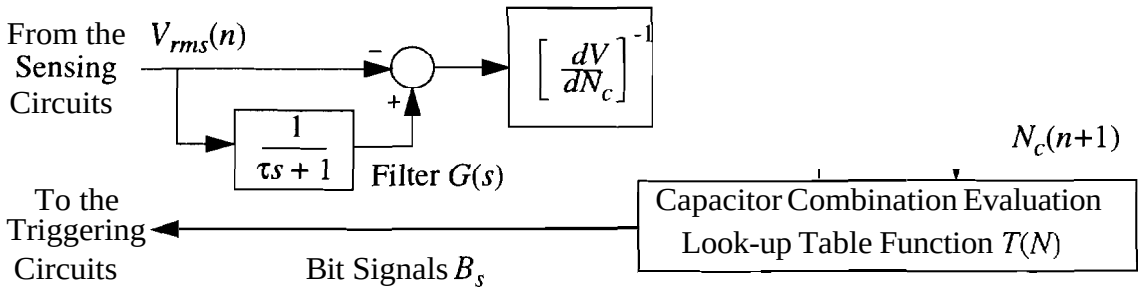

Figure 2.7: Functional diagram of the flicker control algorithm.

The quantity $\frac{dV}{dN_c}$ may be evaluated based upon averaging over many changes, or based upon the previous change as in (2.7) and (2.10). Since the FCA. compensates only for the voltage fluctuation, (i.e. it evaluates the difference in the capacitance steps N_c), the AVC may need to have some standby number of steps for compensation of a fixed amount of reactive power. However, since the ability of the AVC to compensate for flicker will depend on the available capacitance, activating bits for long-term compensation may impact the ability to reduce flicker. Moreover, with this type of control, the AVC does not keep track of power factor even in the long term. Manual control of the standby capacitance is probably not the best way of handling power factor regulation in applications where the AVC is installed for flicker reduction.

2.4.4 Flicker adaptive control strategy

The Flicker Adaptive Control (FAC) introduced herein bring some innovation into the AVC control strategies introduced earlier. The original features of the AVC with a variety of control approaches such as RPC, its applicability to flicker reduction with FCA, and its relative cost make this device attractive for many utilities with different problems in power quality. The accuracy of the RPC may suffer in systems with large rectifier loads or any other highly distorting loads due to its measurement technique. Therefore, alternatives to RPC sampling should be considered such that control is less sensitive to system harmonics. On the other hand, utilities may want to install the single unit AVC for flicker reduction as well as for power factor control, since the need to deal with both types of problems is very likely.

The idea behind the FAC is as follows. Since the AVC is to be used for two purposes, flicker reduction and power factor regulation, the control should also be split to follow these two targets, and the number of capacitance steps for each coming cycle, therefore, should be evaluated on the basis of both factors - voltage flicker and reactive demand. This strategic approach distinguishes the FAC from the others. Symbolically,

$$N_c(n+1) = N_f(n+1) + N_q(n+1) \tag{2.11}$$

In this regard, FCA can be modified to provide for the power factor correction. A block diagram of the proposed modification is shown in Figure 2.8. The branch of the control corresponding to flicker reduction is preserved from FCA. Tht: new branch being added for power factor control, however, uses reactive power to determine necessary compensation rather than sampled current. The measurement of reactive power, shown on the diagram as Q-meter, would involve many samples per cycle and then require integration, so that a more accurate measure can be achieved even in the presence of harmonics and distortions.

The measurement of RMS values on a cycle basis in the VSA as well as in FCA and FAC could be obtained by employing A/D converters and performing necessary numerical computations.

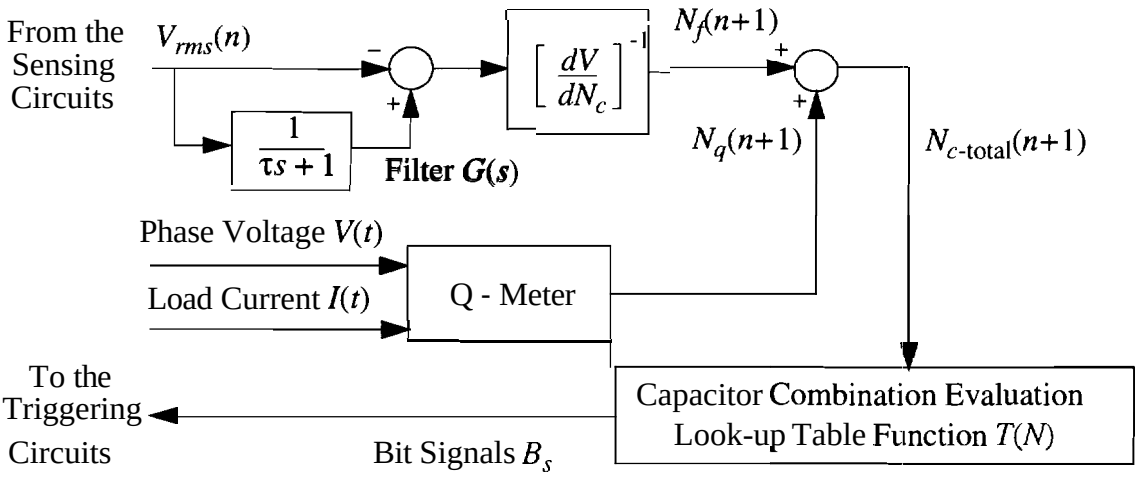

Figure *2.8:* Functional diagram of the modified flicker control algorithm.

In particular, the RMS value of the voltage can be evaluated using a moving average integrator as follows

$$V_{rms}(t) = \sqrt{\frac{1}{T}\int_{(t-T)}^{t} V^2(t)dt} \tag{2.12}$$

where T is the period of one electrical cycle.

Equation *(2.12)* can also be modified for measurement of the RMS voltage on a half- and even quarter-cycle basis using the symmetry of the voltage, and resultant prediction of the RMS value for some time ahead. The technique of moving the "measuring window" may, in addition, be used for computing and monitoring the active power on a corresponding time basis

$$P(t) = \frac{1}{T}\int_{(t-T)} V(t)I(t)dt \tag{2.13}$$

Using the same method as in *(2.12)* for evaluating the RMS value of current, the reactive power needed for the Q-meter can be calculated as

$$Q(t) = \sqrt{V^2_{rms}(t)I^2_{rms}(t) - P^2(t)} \tag{2.14}$$

The approach of FAC introduced in (2.11) can be developed even further. Since the $N_q(n+1)$ is evaluated on a cycle basis, it takes care of the part of the voltage drop due to the increased reactive component of the current. The drop due to the corresponding change in the active component of current represents the potential voltage flicker, and therefore should be compensated by $N_f(n+1)$. It follows that both components N_q and N_f can be evaluated from reactive and active powers Q and P, or from conresponding components of the load current I_q and I_p, respectively.

As an example, it is instructive to consider a simple case where the line impedance $z = r + jx$ is loaded with inductive current $\tilde{I} = I_p + jI_q$. The voltage at the source end is $\tilde{V}_S$, and at the load end is $\tilde{V}_L$. The corresponding phasor diagram is shown in Figure 2.9. In phasor notation,

$$\tilde{V}_S = \tilde{V}_L + (r + jx)\tilde{I} = \tilde{V}_L + (rI_p - xI_q) + j(xI_p + rI_q) \tag{2.15}$$

From the phasor diagram, when the angle between voltages α is negligibly small, which is normally a good assumption for short lines, the voltage drop ΔV is mostly determined by the active part of the phasor difference in $\tilde{V}_S$ and $\tilde{V}_L$. Thus, ΔV can be approximated

$$\Delta V \approx rI_p - xI_q \tag{2.16}$$

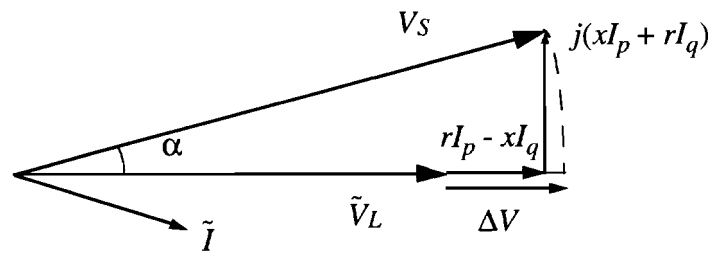

Figure 2.9: Phasor diagram illustrating voltage dip ΔV.

Recalling that the goal of the FAC, in regard to (2.16), is to keep AV constant for short-term transients, which would minimize the flicker, it is reasonable to base the control strategy on the assumption made in (2.16).

It is assumed here that the primary objective of the AVC is for flicker reduction and that the phasor diagram of Figure 2.9 and approximation (2.16) are valid. If a sudden change in reactive demand occurs, the corresponding change in voltage may be expressed

$$\Delta V_1 - \Delta V_2 = r(I_{p1} - I_{p2}) - xI_{q1} + xI_{q2} = 0 \tag{2.17}$$

Assuming that before the change in load the AVC was successfully compensating for unity power factor, $xI_{q1} = 0$, we can express the previous equation as

$$r\Delta I_p = -xI_{q2} \tag{2.18}$$

Equation (2.18), may be used to establish the value of reactive (capacitive) current that AVC should provide, in addition to the correction of the power factor, in order to compensate for the voltage flicker. Equation (2.18) may be rewritten as

$$I_q = -\frac{r}{x}\Delta I_p \tag{19}$$

The negative sign implies that this current should be capacitive, which is consistent with the notation set forth above. Since the compensation for flicker is needed only in short term, we can use the same filter $G(s)$, introduced in (2.9), and (2.5) to obtain the expression for the corresponding portion of the capacitor steps

$$N_f(n+1) = (1 - G(s))\frac{V_{rms}}{Q_{st}\sqrt{2}}\frac{r}{x}I_p \tag{2.20}$$

Incorporating (2.5), (2.11), and (2.20), the complete equation for the FAC can be written as

$$N_c(n+1) = \frac{V_{rms}}{Q_{st}\sqrt{2}}\left(I_q + (1-G(s))\frac{r}{x}I_p\right) \tag{2.21}$$

This type of control would, of course, require knowledge of the system impedance, which is in general is not a problem for any specific utility or site where the AVC is to be installed. The measurement technique involved for determining current components

is somewhat more complicated; however, it is realizable using current digital technology. In fact, current components I_p and I_q can be evaluated as projections of the actual phase current onto an orthogonal rotating q-d-coordinate system [29]. A phasor interpretation of such a rotating frame of reference with one of the axes synchronized and aligned with corresponding vector of phase voltage is shown below

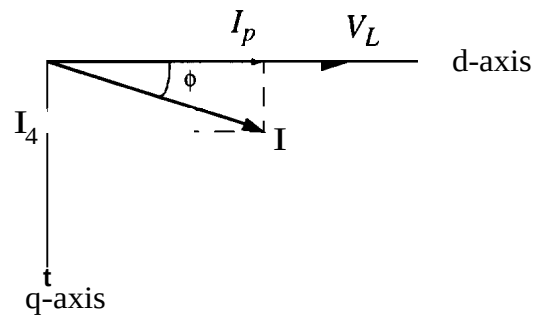

Figure 2.10: Phasor diagram illustrating rotating q-d reference frame.

This approach alone would not prevent the possible error due to harmonics and phase deviation of the system voltage. An improved technique based on similar approach of rotating coordinates and Fourier series is described below. In particular, the first terms of the series are needed, since only the first harmonic is required for control purposes. If the periodic function $f(t)$ (either $V(t)$ or $I(t)$) is symmetric with respect to the t-axis (ignoring dc terms), the first two terms of the Fourier series may be expressed

$$f(t) \approx a_1 \cos \omega_1 t + b_1 \sin \omega_1 t \tag{2.22}$$

where, a_1 and b_1 are the amplitudes of the orthogonal trigonometric components.

These amplitudes, which are of prime interest, are evaluated as corresponding integrals over the period T as

$$a_1 = \frac{2}{T}\int_0^T f(t) \cos \omega_1 t dt \tag{2.23}$$

$$b_1 = \frac{2}{T}\int_0^T f(t)\sin\omega_1 t dt \tag{2.24}$$

Using (2.23), (2.24), and applying the moving average technique of integration, (2.12) and (2.13), expressions for the moving average filters (MAF) for cosine and sine components of voltage and current may be established as

$$V_c = \frac{2}{T}\int_{(t-T)}^{t} V(t)\cos\omega_1 t dt \tag{2.25}$$

$$V_s = \frac{2}{T}\int_{(t-T)}^{t} V(t)\sin\omega_1 t dt \tag{2.26}$$

$$I_c = \frac{2}{T}\int_{(t-T)}^{t} I(t)\cos\omega_1 t dt \tag{2.27}$$

$$I_s = \frac{2}{T}\int_{(t-T)}^{I} I(t)\sin\omega_1 t dt \tag{2.28}$$

where, $\omega_1 = \omega_e$ fundamental frequency.

Equations (2.25) - (2.28) represent magnitudes of the cosine and sine components of the voltage and current. It is possible to define a matrix transformation K onto the voltage vector p-axis, and its quadrature q-axis, such that

$$\begin{bmatrix} I_q \\ I_p \end{bmatrix} = \mathbf{K}\begin{bmatrix} I_c \\ I_s \end{bmatrix} \tag{2.29}$$

This transformation is similar to that defined in [29] except that p and q subscripts are used to distinguish the real and reactive components of current. The expression (2.29) represents the phase-resolver, which is shown in Figure 2.11.

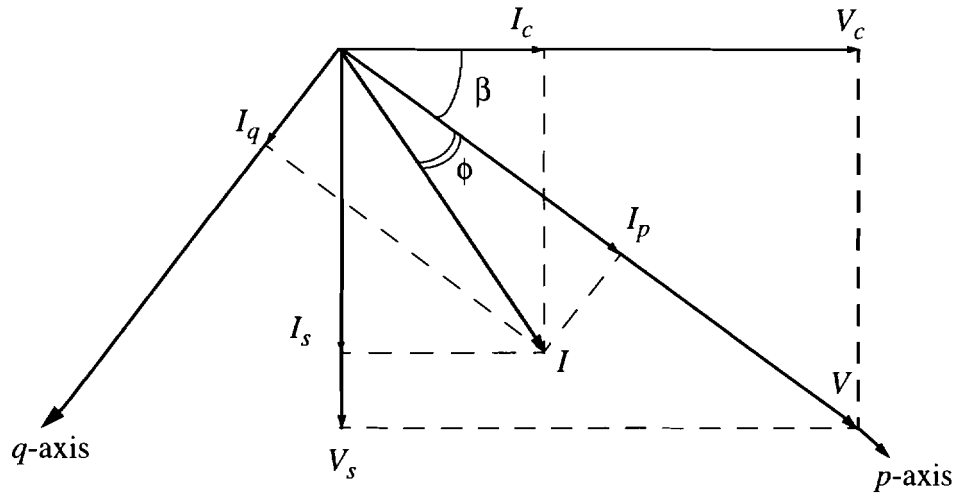

Figure 2.11: Phase-resolver diagram.

The angle ϕ is the power factor angle. The transformation angle β between the cosine and p-axis can be evaluated as

$$\beta = \operatorname{atan}\frac{V_c}{V_s} \tag{2.30}$$

The transformation matrix K is defined as

$$\mathbf{K} = \begin{bmatrix} -\sin\beta & \cos\beta \\ \cos\beta & \sin\beta \end{bmatrix} \tag{2.31}$$

Finally, the overall phase-resolver equation becomes

$$\begin{bmatrix} I_q \\ I_p \end{bmatrix} = \begin{bmatrix} -\sin\beta & \cos\beta \\ \cos\beta & \sin\beta \end{bmatrix} \begin{bmatrix} I_c \\ I_s \end{bmatrix} \tag{2.32}$$

Combining equations (2.21), (2.25) - (2.28), (2.30) and (2.32) :yields the modified FAC algorithm. Implementation of (2.25) - (2.28) requires a synchronized signal for generating cosines and sines; however, this signal is readily established using phase-locked-loop techniques. The final diagram of the FAC algorithm is given in Figure 2.12.

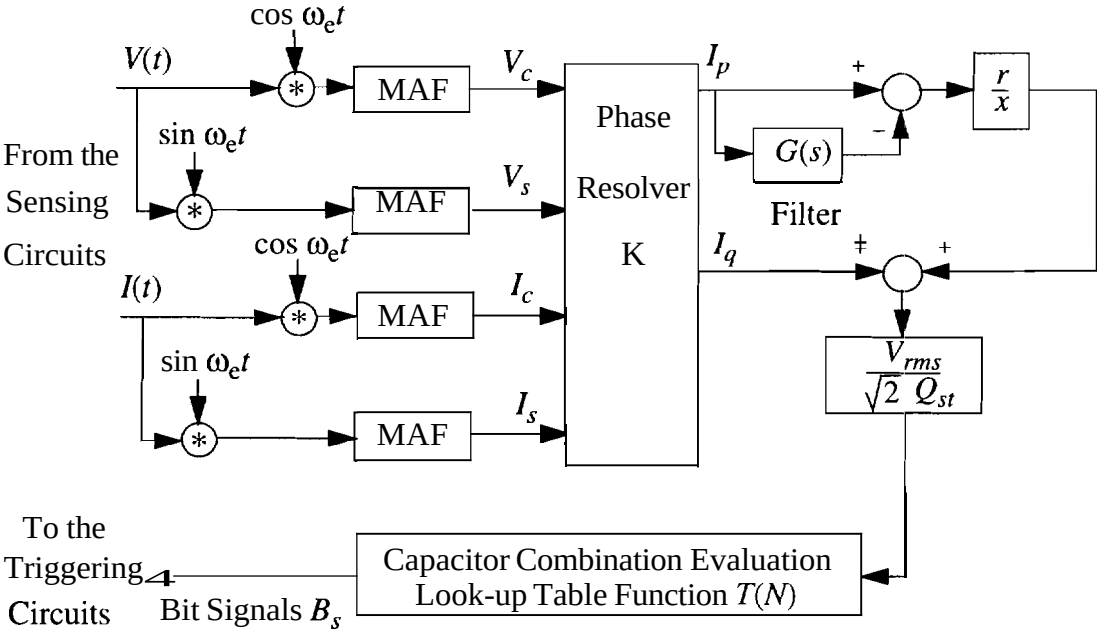

Figure 2.12: Functional diagram of FAC.

The MAFs can also be implemented on a half-cycle basis by reducing the size of moving window in the integration to a half period of the 60-Hz cycle.

3. UIE / IEC FLICKERMETER FOR NORTH AMERICA

3.1 Introduction

The International Union for Electroheat (UIE) and International Electrotechnical Commission (IEC) set forth the methodology for determining flicker from incandescent lamps in electrical networks caused by voltage disturbances of an arbitrary form. This work, presented in IEC publication 868 and its amendments, resulted in worldwide acceptance of the measurement approach and its resulting application of the flickermeter and corresponding flicker-related curves. First used in European countries with 230-V customer supply voltage, the method now is under adoption in North America where 120-V is the rating standard.

The flickermeter involves measuring of network voltage fluctuation and filtering it with respect to lamp-eye frequency characteristics, as well as to human brain reaction and sensitivity to the irritation. Consequential evaluation on a time-varying statistical basis can then be made. The flickermeter accepts the supply voltage or its running RMS value as an input, determines the effect of these fluctuations using standardized references to lamp, eye and brain responses of an average person-observer (producing the equivalent level of visual sensation and annoyance), and then statistically evaluates the flicker severity over some period of time. Thus, one of the outputs of the flickenmeter monitors the instantaneous flicker sensation, and the other represents annoyance severity evaluated as a final judgment or criteria over a specified time. The flicker sensation given in units of perceptibility is proportional to the square of equivalent voltage change passed through the lamp-eye filter, since it is assumed that the fluctuating luminance is determined by the instantaneous power supplied to the lamp [17].

3.2 Demodulation

As mentioned previously, the flickermeter accepts as an input the system voltage. The actual device, of course, would have the necessary input voltage isolation and scaling to ensure that the input voltage is within suitable range of the flickermeter. The voltage flicker, expressed as the percent of change in RMS $\frac{\Delta V}{V} 100\,\%$, is filtered or demodulated. The method used in the UIE flickermeter [12 -15] is based on square law demodulation of the input signal. With this method, the input voltage is squared by a multiplier and then suppressed by a sixth-order Butterworth filter with a band pass from 0.05 - 35 Hz, so that the dc offset and high-order harmonics associated with this method of demodulation will not be present in the output signal of this block. Only the frequencies of RMS fluctuation relevant to the flicker are passed to the next stage. Furthermore, this signal can be related to the average RMS voltage over a reasonably longer period (one minute is suggested), and the percentage of voltage fluctuation can be calculated by multiplying this ratio by 100. A more detailed description of demodulation using this method can be found in [17]. A computationally more efficient method of recovering voltage flicker, however, is proposed below. The necessary demodulation can be implemented using the integrators with running limits introduced in (2.12) and (2.13). Setting sizes of the moving window to the period of one cycle and to one minute, respectively, the expression for the recovered voltage flicker evaluated in percent can be written as

$$\frac{\Delta V}{V} = \frac{\sqrt{\frac{1}{T}\int_{(t-T)}^{t} V^2(t)dt} - \sqrt{\frac{1}{1\min}\int_{(t-1\min)}^{t} V^2(t)dt}}{\sqrt{\frac{1}{1\min}\int_{(t-1\min)}^{t} V^2(t)dt}} 100 \quad \% \tag{3.1}$$

Implementation of (3.1) digitally would require only two integrators, whereas a sixth-order suppressing filter requires six integrators. This method of handling demodulation is far preferable not only for computational ease and accuracy, but also in terms of linearity of the band-pass characteristic, especially in low-frequency fluctuations which have a significant impact on flicker.

3.3 Adoption of Weighting Filter for 120-V Incandescent Lamp

It is well known that the light flicker caused by the same voltage fluctuation may differ depending upon the type of lamps used. In the case of incandescent lamps, it may be suspected that the lamp wattage, construction of filament, its mass, and thermal capacity will determine the flickering characteristic of the lamp. In the original UIE flickermeter, therefore, the weighting filter that represents the frequency characteristic of the lamp-eye chain was derived for the 230-V 60-W standardized filament lamp since it is the most commonly used type of lamp in Europe. The lamp-eye transfer function incorporates the relative luminance fluctuation of the lamp due to the voltage fluctuation, and eye frequency sensitivity to this luminance variation. For 230-V lamp, the lamp-eye transfer function in terms of Laplace variable s can be expressed as

$$H_{230}(s) = H_{\text{eye}}(s)L_{230}(s) \tag{3.2}$$

The 230-V UIE filter transfer function $H(s)$ is plotted and defined in [12] as a combined fourth-order transfer function. It was assumed in [18] that the filter $H(s)$ for any other incandescent lamp can be obtained by exchanging only the lamp filter $L(s)$ without human experiments, which seems to be reasonable since these lamp frequency characteristics are similar. However, since the $H_{230}(s)$ is given as a combined filter, the corresponding filter for 120-V 60-W lamp may be expressed

$$H_{120}(s) = H_{230}(s)\frac{L_{120}(s)}{L_{230}(s)} \tag{3.3}$$

The incandescent lamp transfer function, with a good approximation, can be represented as a first-order low-pass filter of the form

$$L(s) = \frac{K_L}{1 + sT_L} \tag{3.4}$$

where, K_L is a gain factor and T_L is a time constant for a 10% step change in voltage.

The standard lamp parameters found by measurement [18] are given in Table 3.1.

. Table 3.1: Standard lamp parameters

Lamp type	K_L	T_L, ms
230 V	3.25	19.6
120 V	3.07	28.9

Equation (3.3) results in a filter of higher order but can be approximated using fitting techniques as a fourth-order transfer function similar to the original $H_{230}(s)$. The combined lamp-eye transfer function is given as

$$H_{120}(s) = \frac{k\omega_1 s}{s^2 + 2\lambda s + \omega_1^2} \frac{1 + \frac{s}{\omega_2}}{\left(1 + \frac{s}{\omega_3}\right)\left(1 + \frac{s}{\omega_4}\right)} \tag{3.5}$$

The corresponding filter coefficients are given in Table 3.2 and the transfer function is plotted in Figure. 3.1.

Table 3.2: Parameters for 120-V UIE weighting filter $H(s)$

k	λ	ω_1	ω_2	ω_3	ω_4
1.6357	2π4.167375	2π9.077169	2π2.939902	2π1.394468	2π17.31512

3.4 Brain Model and Normalized Flickermeter Response

After the fluctuation signal is weighted, or referred to 8.5-Hz sinusoidal voltage fluctuation, it proceeds to the Rashbass brain reaction model. In this block, the weighted signal is squared so as to represent non-linear visual perception, and supplied to a first-order low-pass filter $H_b(s)$ with gain factor K_b and time constant $T_b = 0.3$ sec to represent the build-up effect in the brain.

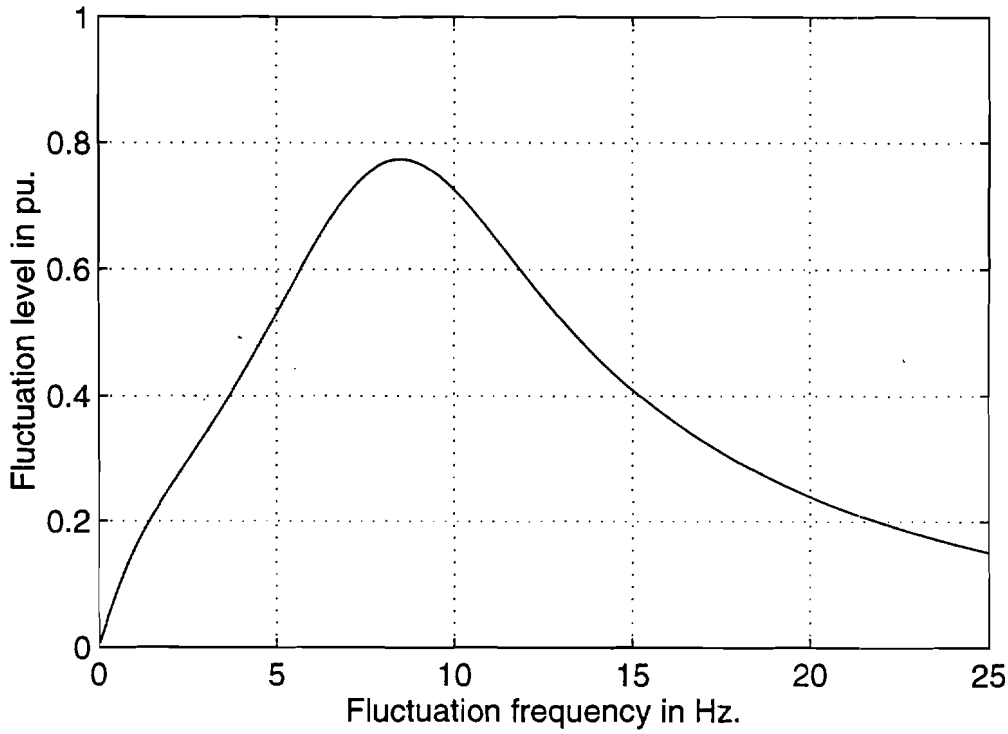

Figure 3.1: UIE/IEC weighting filter curve for 120-V 60-W lamp.

The transfer function may be expressed

$$H_b(s) = \frac{K_b}{1 + sT_b} \tag{3.6}$$

The design of the original 230-V flickermeter involved experiments with human subjects. There, parameters of the Rashbass model, as well as parameters of the weighting filter, were selected so that the threshold of perceptibility was defined as the sensitivity borderline recognized by 50% of the subjects tested for each frequency. The derivation of the 120-V weighting filter parameters, however, were based on certain approximations based on similarity of lamp frequency characteristics. Thus, the output signal of this block represents the immediate flicker sensation in the units of perceptibility proportional to the square of the voltage fluctuation.

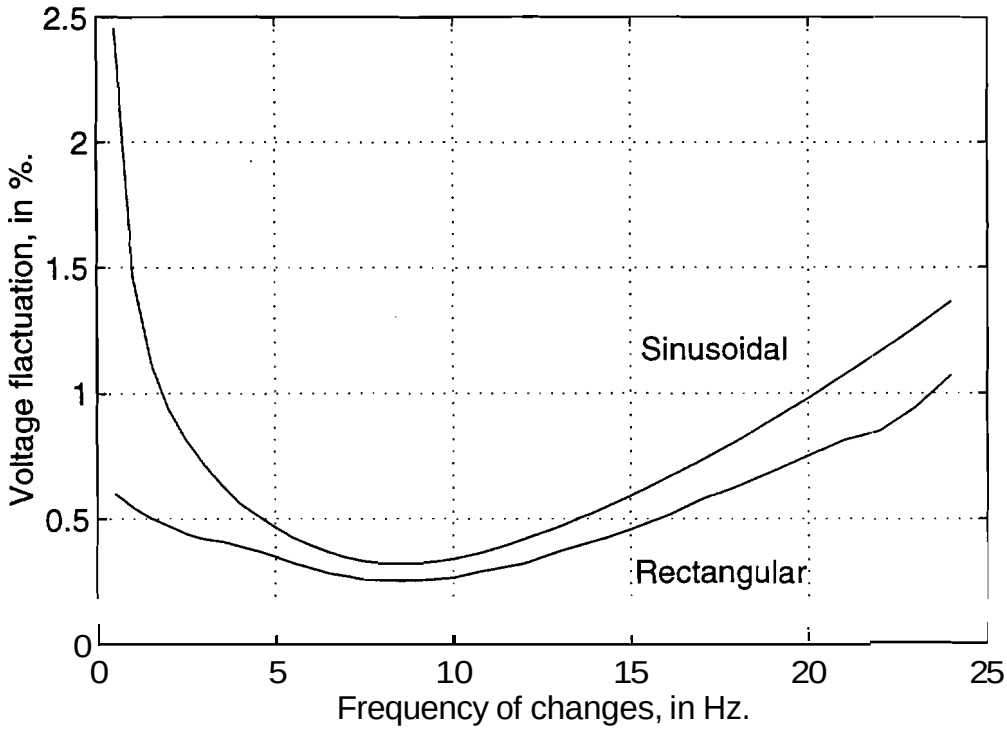

Figure **3.2:IEC** - 868 for 120-V, normalized flickermeter response curves.

As may be expected, the resulting flicker sensation depends not only on the amplitude of the voltage change, but on its waveshape as well. In this regard, the flickermeter has been subjected to tests by sinusoidal and square wave voltage flicker. The tables defining the voltage fluctuation magnitude that produce the unit of perceptibility of the flicker sensation are known as "*IEC* 868for *120-V, Normalized flickermeter* responsefor sinusoidal *and* rectangular voltagefluctuation", and are given in [20]. The two corresponding curves are shown in Figure **3.2.**

3.5 Statistical Evaluation and P_{st} = 1 pu Curve

A subjective feelings of annoyance occurs when light flicker irritates the human vision system over a certain time. In some cases, observable flicker may be very irregular with vast deviation of its peaks over long periods. Depending on the type of loads and

their mutual work schedule, the flicker will vary in its level over a wide range of time. However, a unique method equally applicable to any fluctuating load was proposed by UIE, in which the flicker sensation is statistically evaluated over some representative observation period as a measure of its severity. In this regard, the observation period of 10 minutes and 2 hours is recommended for the short- and long-term evaluation.

The instantaneous flicker is discretized so that a particular flicker level is assigned to each of the evenly spaced moments in time. A sampling of the flicker signal at a fixed rate, usually more frequent then the fundamental frequency of the source, would provide sufficient input data for statistical evaluation. In particular, accumulating the number of samples at each level of the flicker over the observation period should result in corresponding probability distribution function ***(PDF).*** Integrating flicker distribution over the flicker range would give a cumulative probability function (*CPF*) which represents the flicker level that was exceeded during a certain percent of the time of observation period. This method of classifying the flicker samples according to their value and counting the final number of such samples that are greater than or equal to a certain class level, is called the time-at-level classification, which defines the ***CPF.***

To establish the ***CPF*** on-line, the total number of classes and their levels must be pre-specified. For this case, the minimum number of such classes should not be less then 64; however, the classification may be linear or non-linear depending upon the flicker expected. The example illustrating the ***CPF*** and classes for the on-line measurement with linear classification is shown in Figure 3.3. The ***CPF*** may or may not approach 100% depending upon the minimum flicker sensation observed. The shape of ***CPF*** will differ very widely depending upon the flicker variation in time. Therefore, a meaningful and objective method should be used to value each ***CPF*** and quantitatively evaluate the flicker severity. If the flicker ***PDF*** were a standard type of distribution, such as Gaussian or any other well-known distribution, the characteristic parameters such as expectation and standard deviation could be used. However, since the flicker distribution is unknown, the multipoint method for characterizing the ***CPF*** is used.

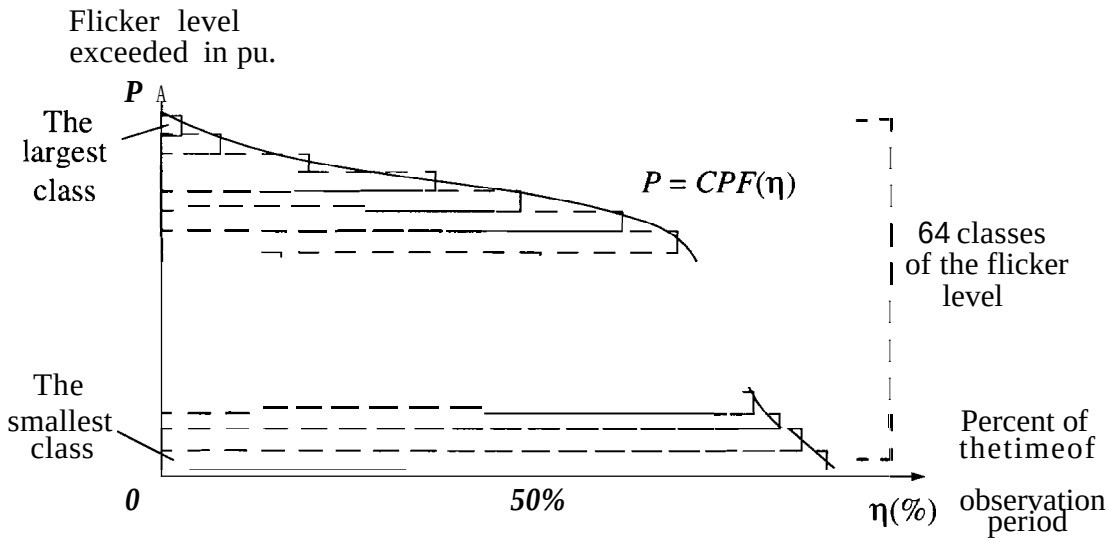

Figure ***3.3:*** Example of the ***CPF*** with level classes.

According to this method, the flicker severity over the short-term with known ***CPF*** can be expressed as

$$P_{st} = \sqrt{\sum_{i=1}^{n} k_i P_i} \tag{3.7}$$

where P_i is the flicker level exceeded during a particular percent of the time of ***10*** minutes of the observation period, k_i is the corresponding weighting coefficient. The flicker level exceeded can be found from the ***CPF*** as

$$P_i = CPF(\eta_i) \tag{3.8}$$

where η_i is a particular percent of the observation period.

Originally only five points (n = ***5)*** on ***CPF*** were used for evaluation of the short-term flicker severity according to ***(3.7)*** and ***(3.8).*** That seemed to provide a reasonable accuracy and mutual correspondence between different measurements in a wide range of voltage fluctuation. The percentile levels η_i and weighting coefficients; k_i were chosen to represent high- and low-frequencies of fluctuation. The percentiles and corresponding coefficients are summarized in Table ***3.3.***

Table 3.3: Percentiles and weighting coefficients for the five-point method

Point on *CPF* P_i	Percent of the time η_i	Weighting coefficient k_i
P_1	0.1%	0.0314
P_2	1%	0.0525
P_3	3%	0.0657
P_4	10%	0.2800
P_5	50%	0.0800

It was noted in [14] that in loads with repetitive on/off duty cycles, a small change in work schedule may cause a significant change in flicker level of one of the five percentile points which, in turn, impacts the flicker severity P_{st}. More stable and accurate results can be achieved by using smoothing values for the last four percentile points [14]. These can be defined as

$$P_{2s} = \frac{CPF(0.7) + CPF(1) + CPF(1.5)}{3} \tag{3.9}$$

$$P_{3s} = \frac{CPF(2.2) + CPF(3) + CPF(4)}{3} \tag{3.10}$$

$$P_{4s} = \frac{CPF(6) + CPF(8) + CPF(10) + CPF(13) + CPF(17)}{5} \tag{3.11}$$

$$P_{5s} = \frac{CPF(30) + CPF(50) + CPF(80)}{3} \tag{3.12}$$

where the subscript s denotes smoothed values. The first point $P_1(0.1)$, however, can be used without change since the time constant in the brain model T_b is large enough so that it will not result in an abrupt change of the flicker level at this percentile. The smoothing technique increases the number of points used to characterize the CPF from five to fifteen evaluated at the percentiles shown in parenthesis in (3.9) - (3.12). Taking into consideration (3.9) - (3.12), the resulting percentile points and weighting coefficients can be summarized as depicted in Table 3.4.

Table 3.4: Percentiles and weighting coefficients for the smoothed method

Point on *CPF* P_i	Percent of the time η_i	Weighting coefficient k_i
P_1	0.1%	0.0314
P_2	0.7%	0.0175
P_3	1.0%	0.0175
P_4	1.5%	0.0175
P_5	2.2%	0.0219
P_6	3%	0.0219
P_7	4%	0.0219
P_8	6%	0.0560
P_9	8%	0.0560
P_{10}	10%	0.0560
P_{11}	13%	0.0560
P_{12}	17%	0.0560
P_{13}	30%	0.0267
P_{14}	50%	0.0267
P_{15}	80%	0.0267

Thus, (3.7) may be rewritten as

$$P_{st} = \sqrt{\sum_{i=1}^{15} k_i CPF(\eta_i)} \tag{3.13}$$

where weighting coefficients k_i and percentiles η_i are defined in Table 3.4.

The method of flicker severity evaluation proposed above results in a corresponding flicker curve or curve of equal severity obtained for sinusoidal and rectangular voltage

fluctuation. These curves are known as "UIE - ***120V*** - $P_{,,} = 1$ ***pu*** *borderline of irritation"*. Authors of [19] comparing all well-known flicker curves (recommended IEEE standards such as IEEE - 519, IEEE - 141, etc.) used in North America found that the $P_{„} = 1$ pu curves is an excellent compromise among all of them. Furthermore, the UIE flickermeter automatically covers all possible waveshapes of the voltage fluctuation which makes it universally applicable. The $P_{st} = 1$ pu borderline of irritation curve for rectangular voltage fluctuation is plotted in Figure 3.4.

The short-term flicker severity evaluated over 10 minutes acicording to (3.13) would provide representative information in cases where the disturbances are caused by cyclical loads such as welders and motors with duty cycles much shorter then the observation period.

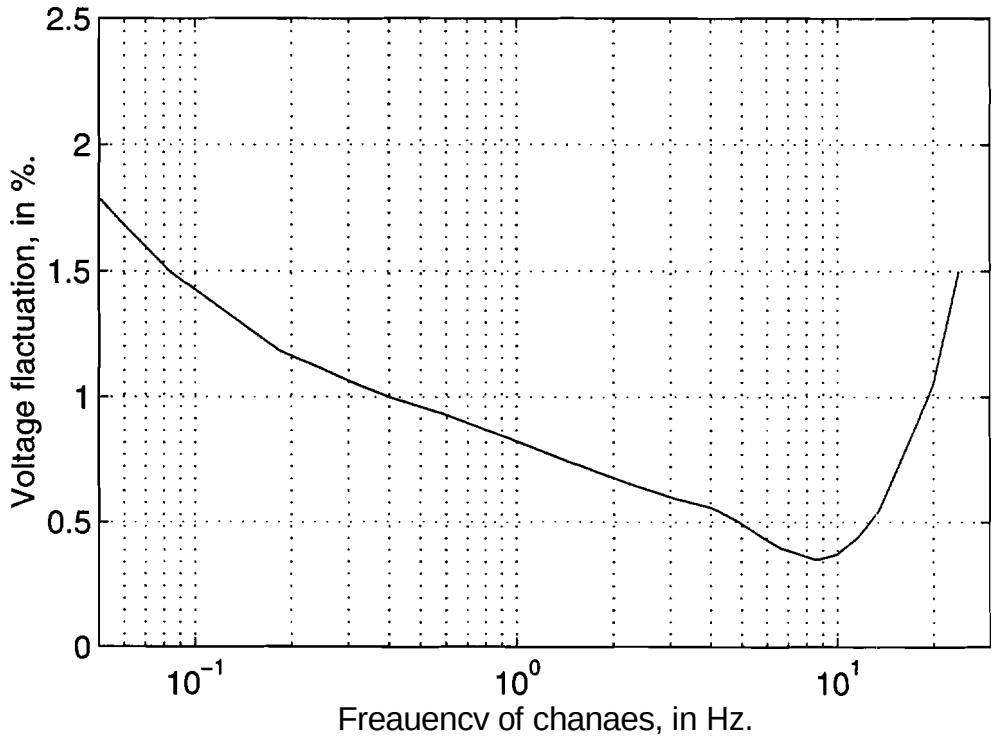

Figure 3.4: UIE - 120V - $P_{,,} = 1$ pu borderline of irritation for rectangular voltage fluctuation.

However, in some cases, when there are many flicker sources operating randomly with long and variable duty schedule, the flicker severity should be evaluated over a significantly longer period. For this purpose, a long-term flicker severity P_{lt}, for which a two hour observation period, is recommended. The long-term flicker severity can be derived from consequentially measured short-term flicker severity P_{st} as

$$P_{lt} = \sqrt[3]{\frac{\sum_{i=1}^{N} P_{st}^3}{N}} \tag{3.14}$$

where N denotes the number of short-term measurements in the corresponding long-term observation period. The cubic law is recommended for cases with relatively small chance of coincidence in load operations [15].

The overall diagram showing signal flow in the flickermeter based on information presented in this chapter is given in Figure 3.5. Each flickermeter for 120-V, or its digital implementation, should be subjected to tests for correspondence of its normalized response as well as equal-severity curves to the corresponding UIE /IEC standard curves, within a maximum 5% difference. For instance, at the frequency of 10-Hz, an increase in rectangular voltage fluctuation from 0.371% to 1.113% (three times) should result in a linear increase in flicker severity P_{st} from 1.0±5 % to 3.0±5 %. Similarly, for the same frequency and waveshape, a three times increase in voltage fluctuation from 0.264% to 0.792% should result in a quadratic increase in flicker sensation P_f, from 1.0±5 % to 9.0±5 %.

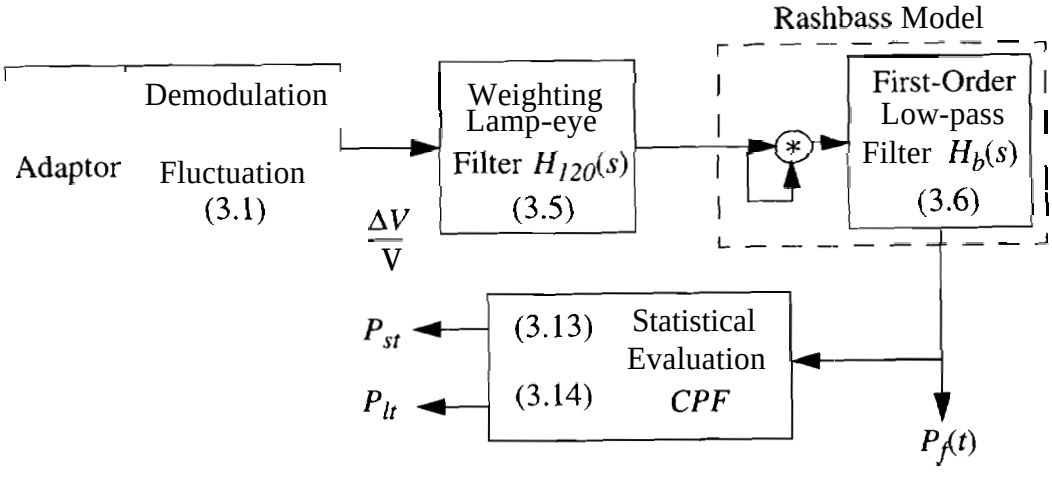

Figure 3.5: Signal flow diagram for the UIE / IEC flickermeter.

4. COMPUTER IMPLEMENTATION

4.1 General Considerations.

The primary objective of the computer studies described in the next chapter is to determine the effectiveness of the AVC, with its different control strategies, to reduce the flicker in the power system shown in Figure 1.1. For computational convenience, the computer model is divided into two parts. The first part includes the three-phase power system, the AVC and its controls, and three resistance welders. The second part is the UIE 120-V flickermeter, which measures the flicker severity at the PCC, where the commercial customer is connected.

The typical duty period of the welder represents a relatively short (4-cycle) but severe change in the power demand. The RMS voltage dip and the following transient caused by this change is expected to be within a similar range. The performance of the AVC during this period may also be effected by transient and high-frequency oscillations. The implementation of a computer model which accurately portrays these transients requires a relatively small ($1.0*10^{-4}$ to $1.0*10^{-9}$ sec) integration step size. For purposes of comparison, the power system with AVC was simulated using two commercially available platforms, namely Matlab/Simulink, and Advanced Continuous Simulation Language (ACSL) which is a Fortran-based compiled language. The ACSL simulation was found to be much faster then the Matlab, even when the Simulink moclel was accelerated using Matlab's "mexsol" facility. Therefore, ACSL was chosen as the computer program for the power system simulation.

On the other hand, the flickermeter includes low-frequency filters and involves statistical evaluation over relatively long period of time. Although it is possible to implement the flickermeter model using the same computer language as the power system model, the large time constants associated with the flickermeter coupled with the small time steps associated with the power system transients would give rise to prohibitive run

times. Consequently, the approach taken was to calculate and store the power system transients for a finite set of welding events and to use these events as inputs to a flickermeter model. Implementation of the flickermeter permits a relatively large integration step-size ($5.0*10^{-3}$ to $1.0*10^{-3}$ sec) due to large time constants. Thus, the flickermeter simulation may even outrun the real time. The computer program used to implement the flickermeter should include tools for statistical analysis. Therefore, Matlab was selected for the flickermeter part of the simulation.

Each part of the overall simulation can be viewed as a subsystem with corresponding inputs and outputs. The transient model is used to establish the electrical response which is stored in a file the and then post-processed by the flickermeter simulation. Taking advantage of the fact that welder operation produces cyclic voltage flicker with relatively large periods between sequential welds, it is convenient to view the RMS voltage dip as a discrete event which is an output of the transient model. Such events can then be passed to the flickermeter simulation, where they can be normalized in order to obtain voltage fluctuation expressed in percent, and processed further according to the UIE flickermeter methodology resulting in statistical evaluation of flicker severity. The diagram illustrating the overall simulation evaluation process is shown in Figure 4.1.

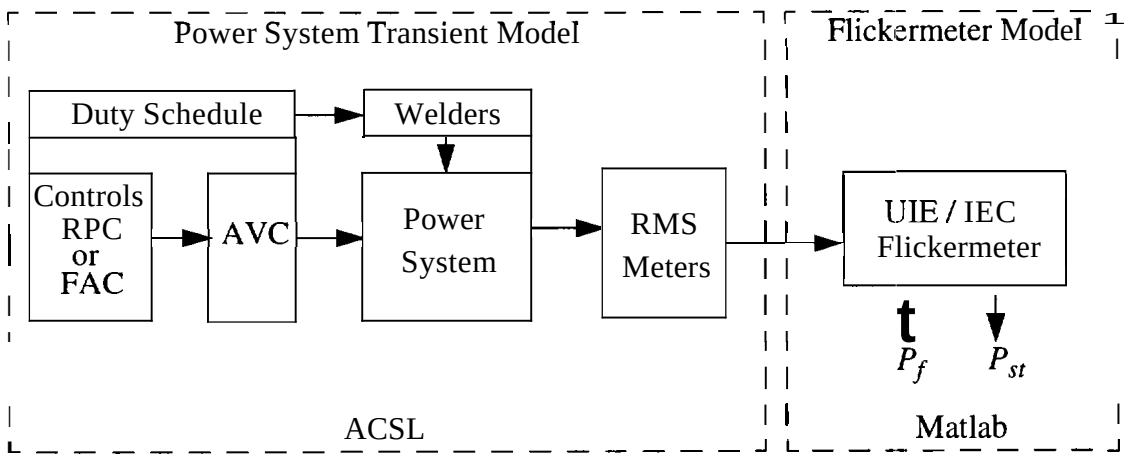

Figure 4.1: Overall simulation and analysis block diagram.

4.2 Implementation of Power System Transient Model

The Automated State Model Generation Algorithm (ASMGA) set forth in [22] was used to implement the transient model in ACSL. The ASMGA provides the ability to automatically formulate equations describing a composite system in the form of a state space model. ASMGA assumes that a complex power system can always be viewed as a circuit, or a graph, consisting of connecting nodes-vertices and branches-edges. Each such branch may contain a resistor, inductor, capacitor, back emf, current source and/or switch. Thus, the system is defined by the user in terms of its topology and corresponding branch data. This information used by ASMGA to automatically derive the state equations. The resulting state space model (linear or non-linear, time-varying or time-invariant) has its standard form

$$p\mathbf{x} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{4.1}$$

$$\mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u} \tag{4.2}$$

The model (4.1), (4.2) then can be simulated using any appropriate integration algorithm according to the technique set forth in [22]. An important advantage of this systematic approach is that once the state space model is established, a variety of useful techniques such as eigenvalue based analysis, linearization, stability theory, state space averaging, multi-rate integration, etc. become applicable to the system simulation, study and analysis. Therefore, ASMGA can be successfully applied to a wide variety of different problems [22], [32].

In order to gain familiarity with ASMGA, it is instructive to review some of its fundamentals. In particular, for a vast variety of power systems for which the state space model can be derived in its standard form (4.1) and (4.2), a branch can be represented as some variation of the general branch model shown in Figure 4.2.

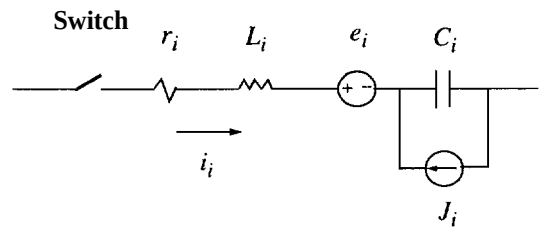

Figure 4.2: Branch model.

Depending on the setting of the switch, each branch may be active or inactive thereby changing the topology of the system. Logical control of the switch based on branch voltage, current and time can be used to represent diode, thyristor or any other type of controllable commutator. This approach is convenient for modeling of switching networks where system topology is a function of system states and time. Thus, any system can be defined in the form of a list of branches, where each branch is specified by a statement containing its topological properties as well as its parameters. For example, in ACSL the branch statement has the following form

BRANCH(b#, p#, **n#, r, L,** pL, **P,** e, J)

where: b# is the branch number in the list; p# and n# are the numbers of the positive and negative nodes, respectively. Branch emf and current source are represented as **e** and J. Parameters **r,** L, pL and P are the resistance, inductance, rate of change of inductance and reciprocal of the branch capacitance $P_i = \frac{1}{C_i}$. The operators p denotes differentiation with respect to time. Thus, any variation of the branch can be defined by setting appropriate branch parameters to zero. Moreover, similar definition statements can be made to represent circuit elements such as diodes, thyristors etc., or even mutual inductances between magnetically coupled branches, if required. In any event, the first three numbers in the definition statement fix the complete topological structure of the systenn (i.e. the topological layout including all branches).

The overall ACSL simulation was represented in the form of functionally connected blocks - macros [30] with ACSL's graphical user interface, or "Graphic Modeller" (GM). The translator expands macros and generates the code for further compilation. Thus, the ASMGA was used inside macro acsys.gsl to implement the ac part of the power system. The topological diagram of the system (depicted in Figure 1.1), implemented in ASMGA is shown in Figure 4.3. Each welder is represented as a corresponding branch and modeled as a switched inductor as depicted in Figure 4.4.

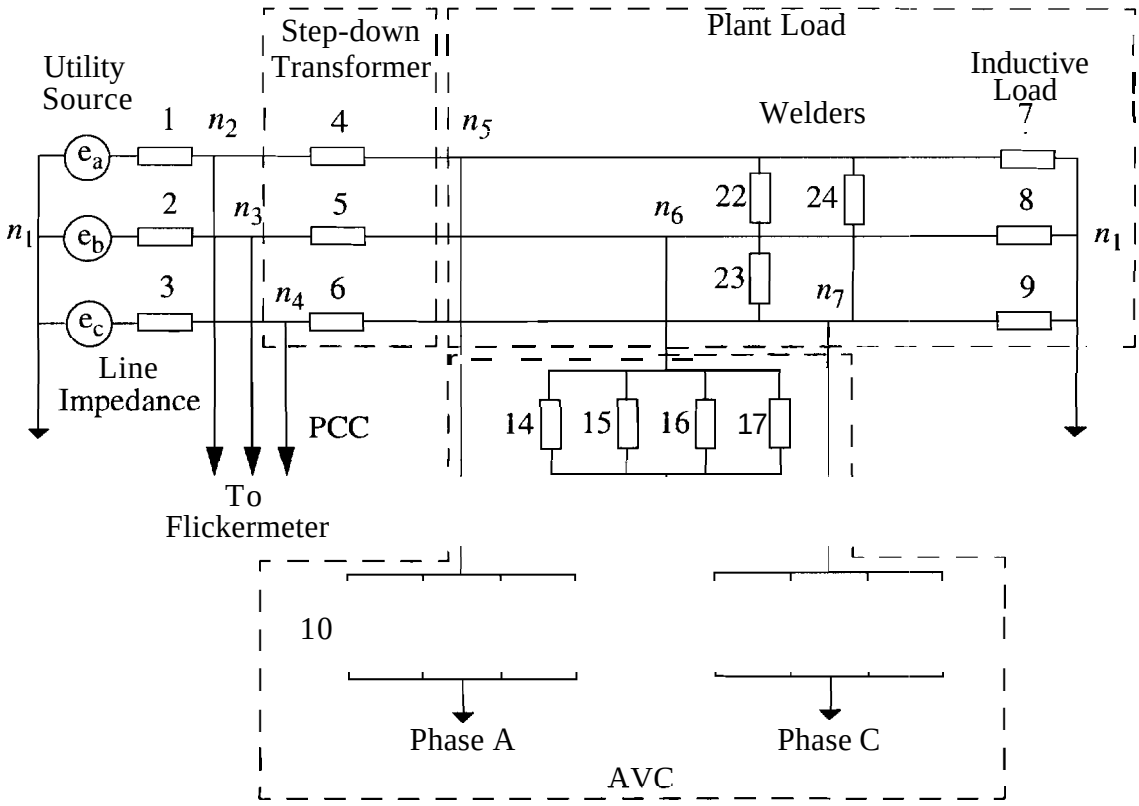

Figure 4.3: Topological diagram of the ac system for ASMGA implementation.

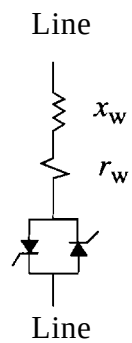

Figure 4.4: Per-phase welder representation.

In this representation, the welder is allowed to switch on and off for any number of half-cycles with any desired delay in the firing angle of the thyristors, so that the effect of harmonics may also be included.

An example of the GM interface of the 4-bit AVC with the RCP control is shown in Figure 4.5. A fragment of the file in which the power system is defined in terms of branch statements in given in Figure 4.6. The look-up table $T(N)$ introduced in (2.2) was also implemented as a macro `control.mac` and used inside of the control block in GM.

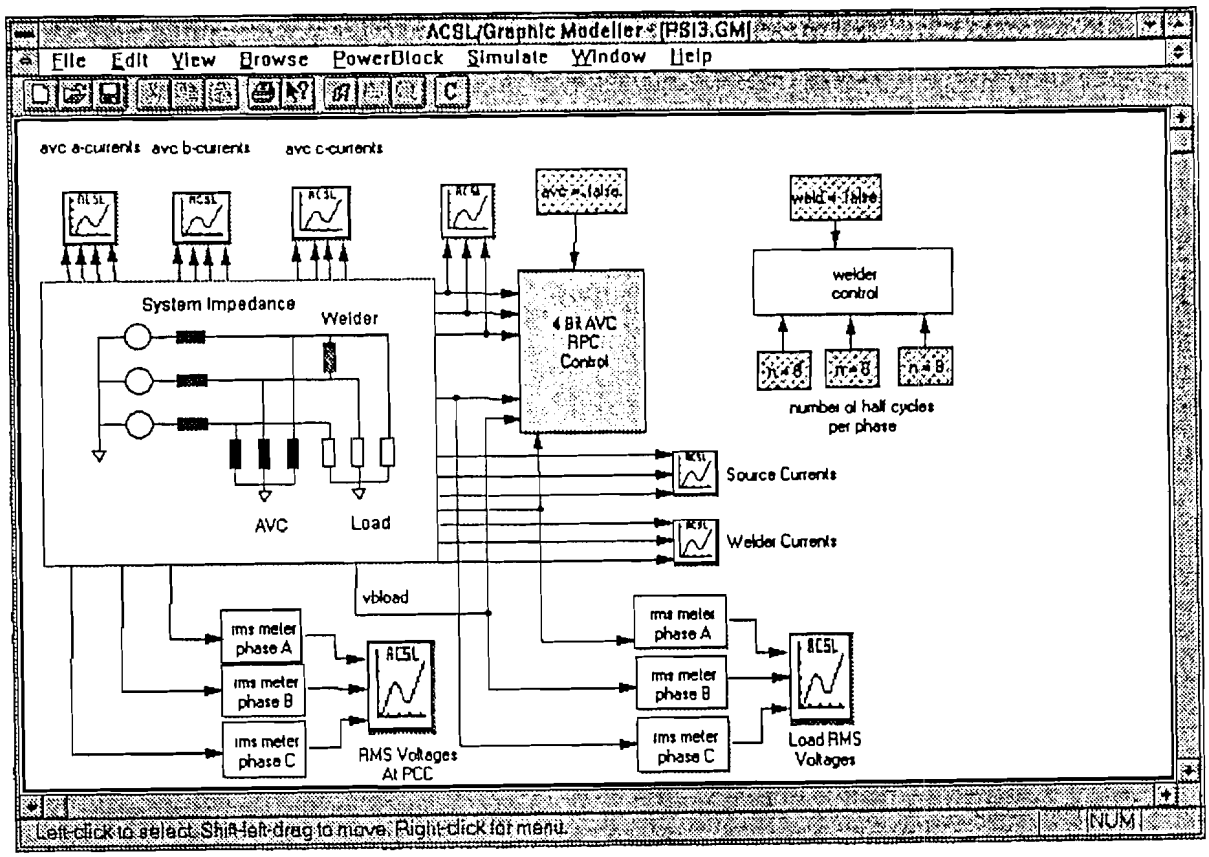

Figure 4.5: GM user interface of the 4-bit AVC computer model.

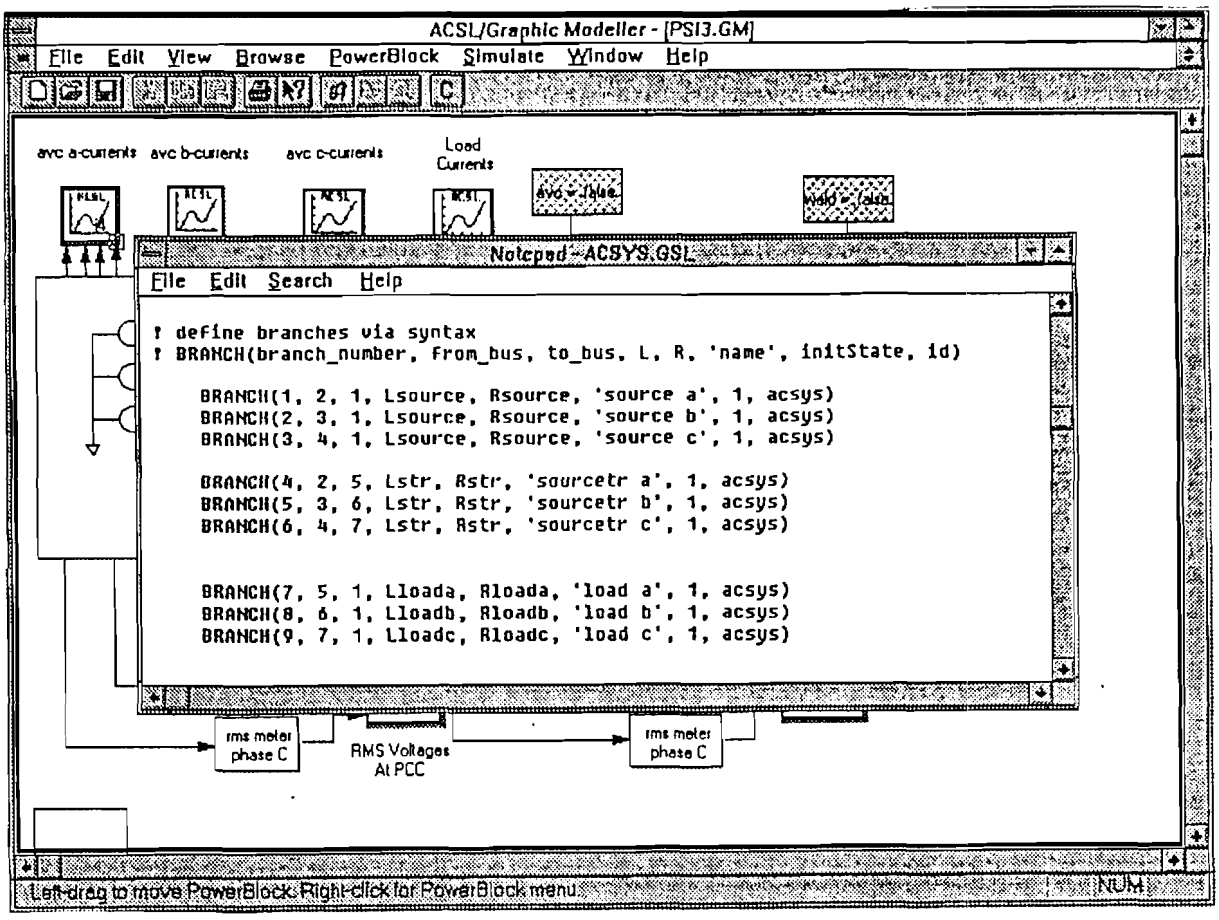

Figure 4.6: Fragment of the file showing branch statements.

The other control functions of RPC and FAC were built in GM from standard blocks available in the GM library. The RMS meters (2.12) were also rnodeled in GM as depicted in Figure 4.7.

4.3 Flickermeter Implementation.

As noted previously, when the load duty cycle is much shorter then its rest interval, it is computationally more efficient to run the transient simulation only to capture the short-term transient. Thus, for the 4-cycle weld, it was considered sufficient to run the ACSL simulation for only 0.3 sec for each event and to store the RMS value of the voltages.

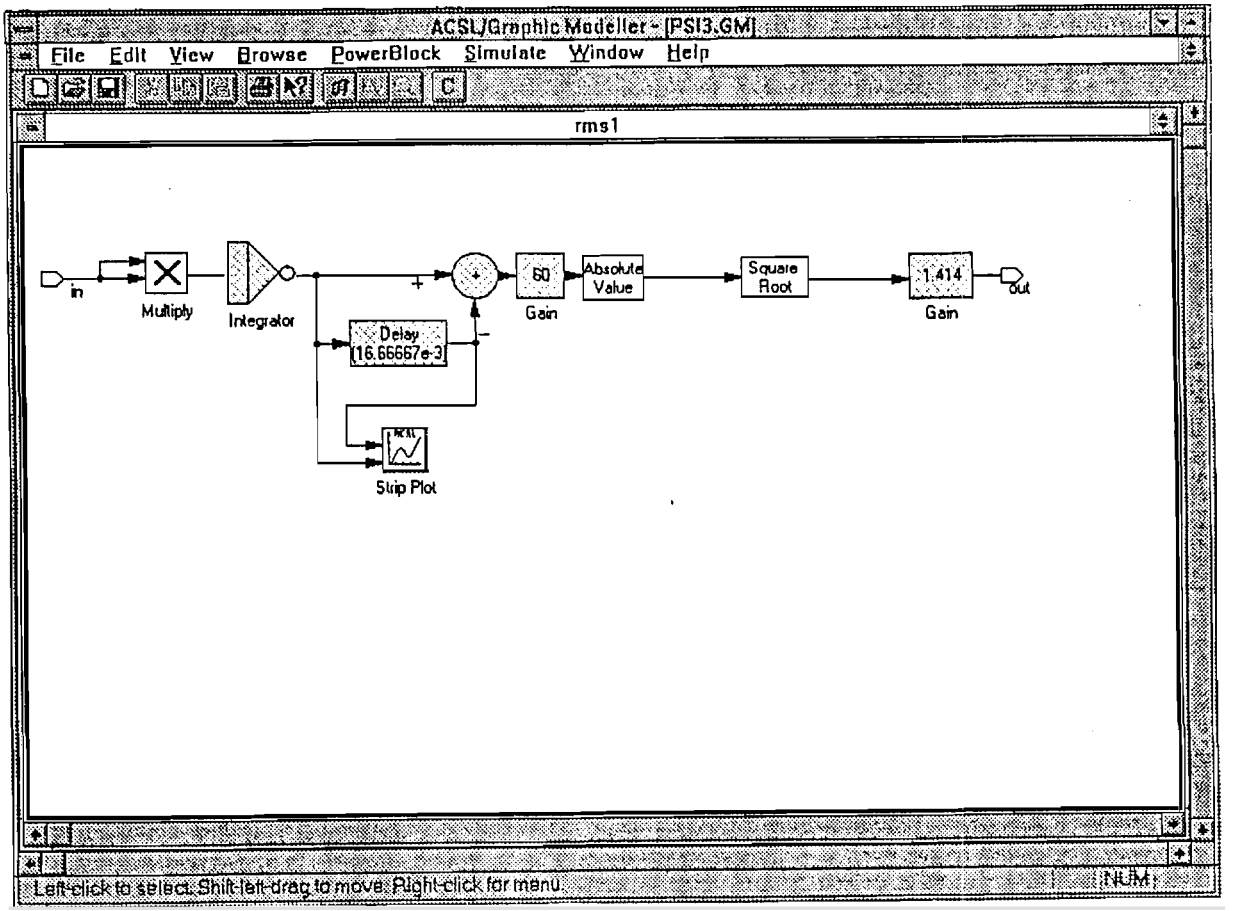

Figure 4.7: GM user interface of RMS meter.

The RMS dip caused by the weld, therefore, represents the corresponding event in time. The model simulation can be run many times so that events corresponding to different welding conditions may be recorded. Each RMS event is normalized so that it is expressed in percent of change with respect to the RMS value before and after the weld. The collection of such normalized events for all allowable welding operations thus can form an event library. Once the library is formed and stored, these events can be superimposed in the time domain in any desired way without ever again running; the transient simulation. Thus, for a given welder operation schedule, the RMS time history may be restored by combining the appropriate events from the library and superimposing them in time according to the schedule. This concept is depicted in Figure 4.8.

In the ACSL simulation, the RMS value of the voltages were sampled each 0.002 sec and written into the Raw Run Record (RRR) file. After each simulation run, this data file was transferred into Matlab, where all events were normalized and stored forming the event library. The two user inputs shown in Figure 4.8 permit two different types of event schedules. In the first case, the events could be scheduled by specifying the characteristic of each weld and its starting time according to the operating specification of the production line. Using this input, welding events may be scheduled in any desired sequence (even at random) covering the 10-minute observation period. The second input assumes cyclical welding, in which case the type of weld, its length in half-cycles, and the repetition rate are the two parameters to be specified.

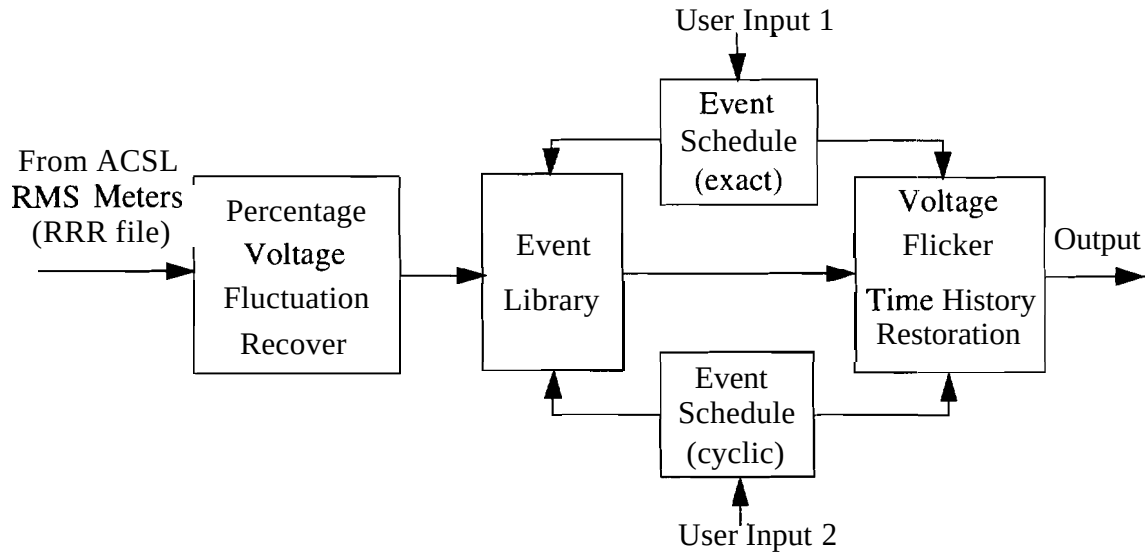

Figure 4.8: Voltage fluctuation time history restoration (in Matlab).

In the restoration block, the event schedule is expanded into a vector with two columns; one for time and the other for the restored time history of the voltage flicker. The length of this vector is equal to the observation period with evenly spaced time intervals. For welding with long rest intervals, this vector will be sparse. Once the voltage flicker vector is formed, it can be passed directly to the weighting filter (3.5) following the signal

flow diagram shown in Figure 3.5. The time interval of 0.002 sec would correspond to a 500-Hz sampling rate of the flicker sensation signal as an output from the $H_b(s)$ filter (3.6). Thus, in order to reduce the number of points taken for statistical evaluation without sacrificing accuracy, it was considered sufficient to use only each third point (sampling frequency of 167 Hz) of the output signal from (3.6). The vector of the sampled flicker sensation would contain a maximum of 100, 000 points for the observation period of 10 minutes. The vector of this size in Matlab can be processed explicitlly using percentile function [33] so that for the time-at-level classification, there may be as many level-classes as there are points. The resulting CPF can be evaluated at each of the fifteen percentile points specified in Table 3.4, and the flicker severity P_{st} is then computed according to (3.13).

5. COMPUTER STUDIES

5.1 Results

The power system depicted in Figure *1.1* was simulated for study purposes in accordance with the topological configuration shown in Figures *4.3* and *4.4*. The parameters used in the computer studies described herein are given in Table *5.1* and are based upon data provided by Cinergy. All parameters were converted to per unit with a base power $P_b = 3\ MVA$. The impedance data given in Table *5.1* are in accordance with the branch numbering specified in Figure *4.3*.

Table 5.1: System parameters

Element description	Branch number as specified in Fig.4.3	Value in pu for $P_b = 3\ MVA$	Original data (impedances are in pu with $P_b = 100\ MVA$)
Phase *A*, voltage source	E_a	*1*	*480-V* line-to-line
Phase B, voltage source	E_b	*1*	*480-V* line-to-line
Phase C, voltage source	E_c	*1*	*480-V* line-to-line
Phase *A*, source impedance	*1*	*0.0108* + *j*0.0306	*0.360* + *j1.020*
Phase B, source impedance	*2*	*0.0108* + *j0.0306*	0.360 + *j*1.020
Phase C, source impedance	*3*	*0.0108* + *j0.0306*	*0.360* + *j1.020*
Phase *A*, transformer impedance	*4*	*0.0060* + *j*0.*1083*	*0.200* + *j3.6*10
Phase B, transformer impedance	*5*	*0.0060* + *j*0.*1083*	0.200 + *j*3.610
Phase C, transformer impedance	*6*	*0.0060* + *j0.1083*	*0.200* + *j3.610*
Phase A, load impedance	*7*	*5.6940* + *jl.7794*	*160* Kw / *50* Kvar
Phase B, load impedance	*8*	*3.7572* + *j0.5780*	*260* Kw / 40 Kvar
Phase C, load impedance	*9*	*4.7591* + *j1.0708*	200 Kw / 45 Kvar

Element description	Branch number as specified in Fig.4.3	Value in pu for P_b = 3 MVA	Original data (impedances are in pu with P_b = 100 MVA)
AVC, first bit	10, 14, 18	-j21.3675	46.8 Kvar
AVC, second bit	11, 15, 19	-j10.6838	93.6 Kvar
AVC, third bit	12, 16, 20	-15.3419	187.2 Kvar
AVC, fourth bit	13, 17, 21	-j5.3419	187.2 Kvar
Welder, connected to A-B	22	3.0204 + j3.9946	375 Kw /450 Kvar
Welder, connected to B-C	23	2.9046 + j4.3816	330 Kw /490 Kvar
Welder, connected to C-A	24	3.3643 + j4.0975	330 Kw /450 Kvar

The computer studies are based upon a 4-cycle weld, where all three welders are fired concurrently with a negligible delay in firing angle. A repetition rate of 1 sec is assumed for the purpose of study which is of the same order of magnitude as the actual duty schedule of the welders installed at the given plant. Two control strategies, namely RPC and FAC, were considered with both the 3-bit AVC and the 4-bit modified version. The flicker severity P_{st} was evaluated at the PCC as well as at the welder location.

The results of the studies are summarized in Tables 5.2 through 5.6. The corresponding examples of time-domain responses and *CPF*s are given in Figures 5.1 through 5.28. For convenience, the computer traces are provided at the end of this chapter. The flicker severity in Table 5.2 was calculated assuming that the AVC is not activated. In Tables 5.3 and 5.5, it was assumed that the AVC is operating using the RPC control based on phase current sampling as described Chapter 2. In Tables 5.4 and 5.6, the AVC was assumed to be operating with FAC. The FAC was simulated according to the diagram depicted in Figure 2.12.

According to the results in Table 5.2 and 5.3, the 3-bit AVC using RPC strategy reduces the flicker severity at the PCC as well as at the load end. However, based on the flicker severity results shown in Tables 5.4 though 5.6, it appears that the 4-bit AVC, with

either RPC or FAC, does not provide a significant improvement when compared to the original 3-bit AVC, nor does the FAC when used in the 3-bit AVC instead of the RPC. A detailed explanation of these results is given in the next section.

Table 5.2: Flicker severity without AVC.

Flicker severity	Phase A, at PCC	Phase B, at PCC	Phase C, at PCC	Phase A, load end	Phase B, load end	Phase C, load end
P_{st} in pu	1.0856	1.0395	1.0395	4.2286	4.2832	4.0102

Table 5.3: Flicker severity with 3-bit AVC with RPC control.

Flicker severity	Phase A, at PCC	Phase B, at PCC	Phase C, at PCC	Phase A, load end	Phase B, load end	Phase C, load end
P_{st} in pu	0.8572	0.6672	0.7350	3.1631	2.3712	2.8986

Table 5.4: Flicker severity with 3-bit AVC with FAC.

Flicker severity	Phase A, at PCC	Phase B, at PCC	Phase C, at PCC	Phase A, load end	Phase B, load end	Phase C, load end
P_{st} in pu	0.8524	0.8290	0.7735	3.1641	3.1243	3.0243

Table 5.5: Flicker severity with 4-bit AVC with RPC control.

Flicker severity	Phase A, at PCC	Phase B, at PCC	Phase C, at PCC	Phase A, load end	Phase B, load end	Phase C, load end
P_{st}, in pu.	0.8406	0.5542	0.7014	3.3420	2.1830	2.9712

Table 5.6: Flicker severity with 4-bit AVC with FAC.

Flicker severity	Phase A, at PCC	Phase B, at PCC	Phase C, at PCC	Phase A, load end	Phase B, load end	Phase C, load end
P_{st} in pu	0.8325	0.7350	0.6909	3.4179	2.9398	3.0246

5.2 Analysis of Results

In the computer studies involving the 3-bit AVC, all capacitor:; are activated during the weld in the RPC and FAC strategies. I in both the 3- and 4-bit versions with the RPC strategy, none of the capacitors are turned on in phase B before and after the weld, as shown in Figures 5.6 and 5.20, due to the fact that the load reactive demand in this phase is on the borderline of the lowest threshold. In the 4-bit version, the RPC control activates bits 2, 3 and 4, leaving the first bit off (Figure 5.19 through 5.21), whereas the FAC (Figure 5.24 through 5.26) activates all available capacitors.

It is important to note that in the 3-bit version of the AVC, the amount of reactive power that can be supplied to the system with all capacitors turned on (327.6 Kvar per phase), is somewhat less then the load VAR demand during the welding operation. In the 4-bit version, the total installed VARs (514.8 Kvar per phase), within the resolution of the control, is just enough to compensate for the reactive demand of the welders and the base load. Over-compensated operation during welding is not possible due to this sizing limitation. Since the total capacity of the AVC is just enough to compensate the load and given the system impedance is primary reactive ($r/x = 0.12$), there is no advantage in this system to take into account the RMS drop due to both active and reactive currents. Furthermore, since the welders are fired with almost no delay in firing angle, the total load current has no significant distortion. Consequently, for the given system, the simple RPC control provides a reasonable measure of the load VARs.

The traces obtained from computer simulation of the 3-bit AVC with RPC control are in good agreement with the measured responses as established by Cinergy. The recorded and simulated events are compared Figure 5.10. This agreement provides confidence in the given computer studies.

An important aspect of the given system is that the welding event is very brief - only 4 electrical cycles per weld. In order to better understand the results of the previous computer studies, it is useful to break up the event (Figure 5.10), as measured by the RMS voltage dip, into three consecutive stages:

1. When the welder is first turned on, the voltage decreases for approximately one cycle before the AVC control has the opportunity to become effective. After the correct capacitor combination is set, the **RMS** value of the phase voltage recovers within the next cycle to a steady level.

2. From this point, the **RMS** voltage is relatively flat until the end of the weld. Ideally, if the AVC capacity is sufficient, the level of this flat section is close to the original value of the **RMS** voltage before the weld.

3. After the welder is turned off, the activated AVC capacitors remain on until the next capacitor current zero-crossing which occurs when voltage is at its negative peak. This results in a worst case of one cycle over-compensation. This, in turn, causes an overshoot in the **RMS** voltage which exceeds the prior-weld level. After the capacitors are reset to their pre-weld combination, the RMS voltage recovers within the next cycle.

As a result of these three stages, and due to the fact that **RMS** voltage is measured on a cycle basis, the total event length from beginning to end is approximately six full cycles for a four cycle weld. It also appears that since the length of each stage of the welding event is of the same order of magnitude, they all can have a significant impact upon the observable flicker. In the studies presented here, however, it is important to note that the AVC response delay of one cycle and weld length of four cycles are very comparable in the time scale, and as a result the time length of each stage is approximately two cycles. Consequently, the first and the last stage of each weld have a significant impact on flicker severity assuming that full compensation is achieved in the second stage. In the case of the 4-bit AVC, where full compensation in the second stage of the welding event is achieved within device resolution, the first and the last stages are, indeed, the most important in determining the flicker level. In the first stage, the magnitude of the **RMS** dip is determined by the welder power demand, and the level of the **RMS** increase in the third stage due to over-compensation depends on the number of capacitance steps activated during

the weld. Consequently, if full compensation is achieved in the second stage, thereby reducing its impact on flicker, the corresponding over-compensation in the last stage adds distortion. This explains why adding a fourth capacitor bit does not result in any tangible improvement in flicker severity. The simulation results of the short-term flicker severity P_{st} for 3-bit AVC given in Tables 5.3 and 5.4 and for the 4-bit version in Tables 5.5 and 5.6 seem to agree with this consideration. It appears that, regardless of control strategy, the AVC with its 1-cycle delay in response, is limited in its effectiveness in reducing flicker due to cyclically varying load with very short duty intervals. In a cyclic load with a duty interval of one electrical cycle, the AVC may even make flicker worse, mostly due to the overshoot in the RMS voltage in the third event stage. It also appears that the installation of an additional 187.2 Kvar capacitor bank may not reduce the flicker significantly when compared to the original 3-bit version of the AVC. The same conclusion, however, may not apply if the welding intervals are longer.

If the duty interval of the load is sufficiently longer than the one-cycle response delay of the AVC, and if the system r/x ratio is somewhat higher than 0.12 (in some cases, the equivalent of this ratio may be higher due to the power-factor correction capacitors installed), and the total installed capacitance of the AVC allows over-compensation, the advantage of the FAC would become more noticeable. In the studies involving the 4-bit AVC, the differences between the two controls resulted in one more capacitance step activated in the case of the FAC. If the load current is heavily distorted as in non-sinusoidal loads such as resistance welders operating with large delay in firing angle, arc furnaces, or rectifier loads, significant errors may exist if the sampled current is used to measure the load VARs. In fact, the AVC with RPC may even increase flicker in such loads. On the other hand, the measurement technique associated with FAC would provide an accurate measurement even in the presence of heavy distortion.

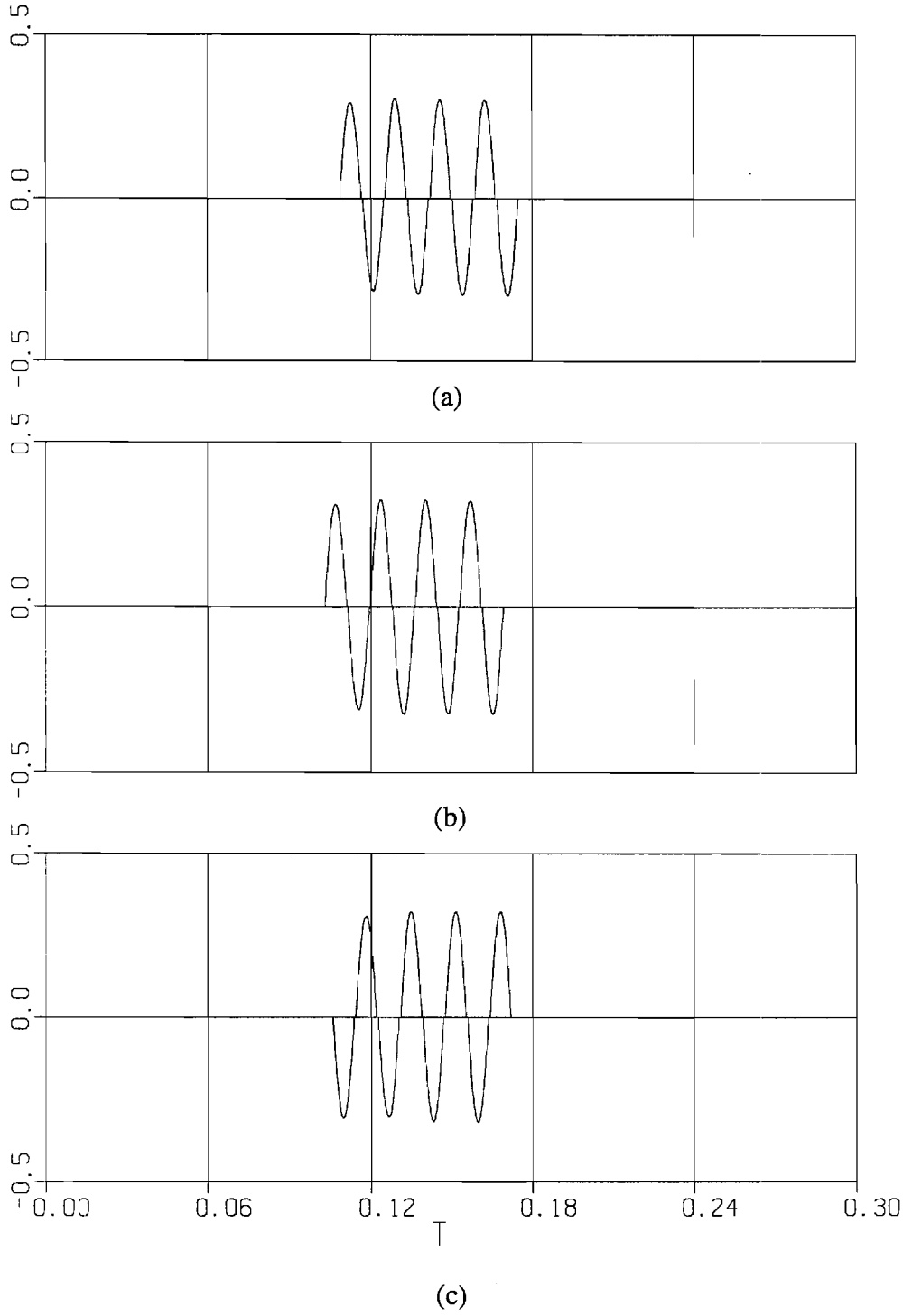

Figure 5.1: Welder currents; (a) current of the welder connected to **A-B,** (b) current of the welder connected to B-C, (c) current of the welder connected to **C-A.**

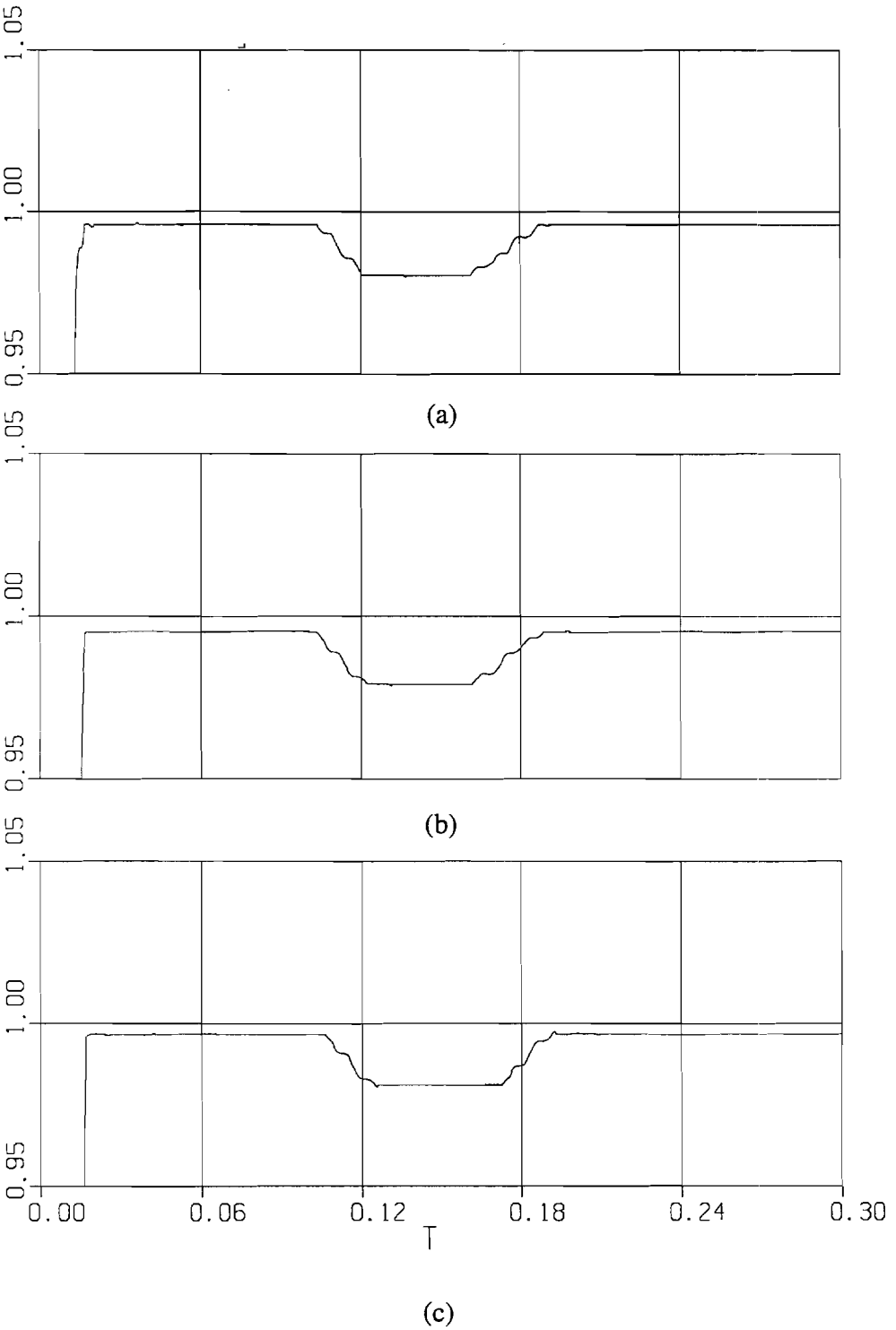

Figure 5.2: RMS voltages at the PCC with AVC disabled; (a) phase A, (b) phase B, (c) phase C.

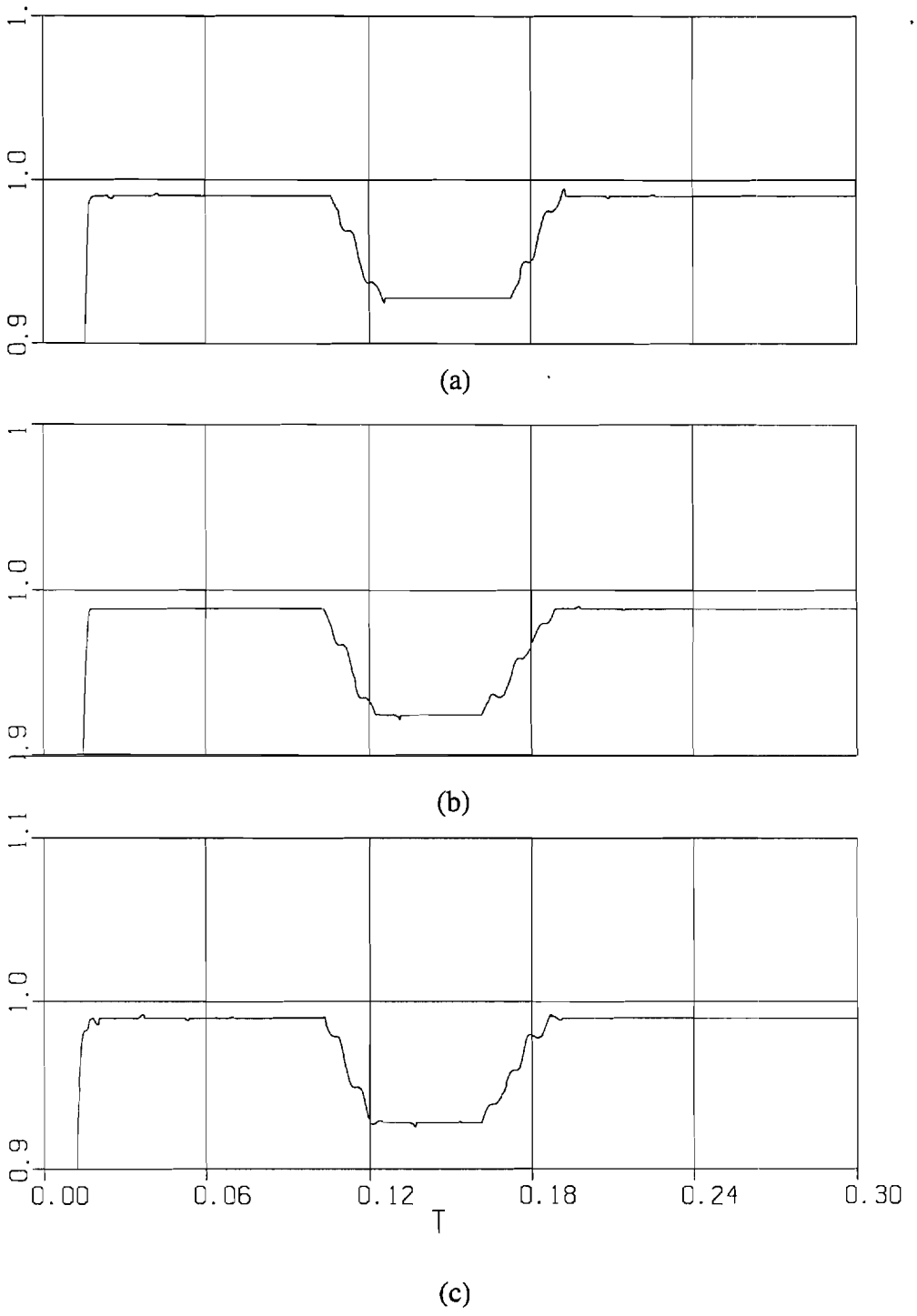

Figure 5.3: RMS voltages at the load end with **AVC** disabled; (a) phase **A,** (b) phase B, **(c)** phase **C.**

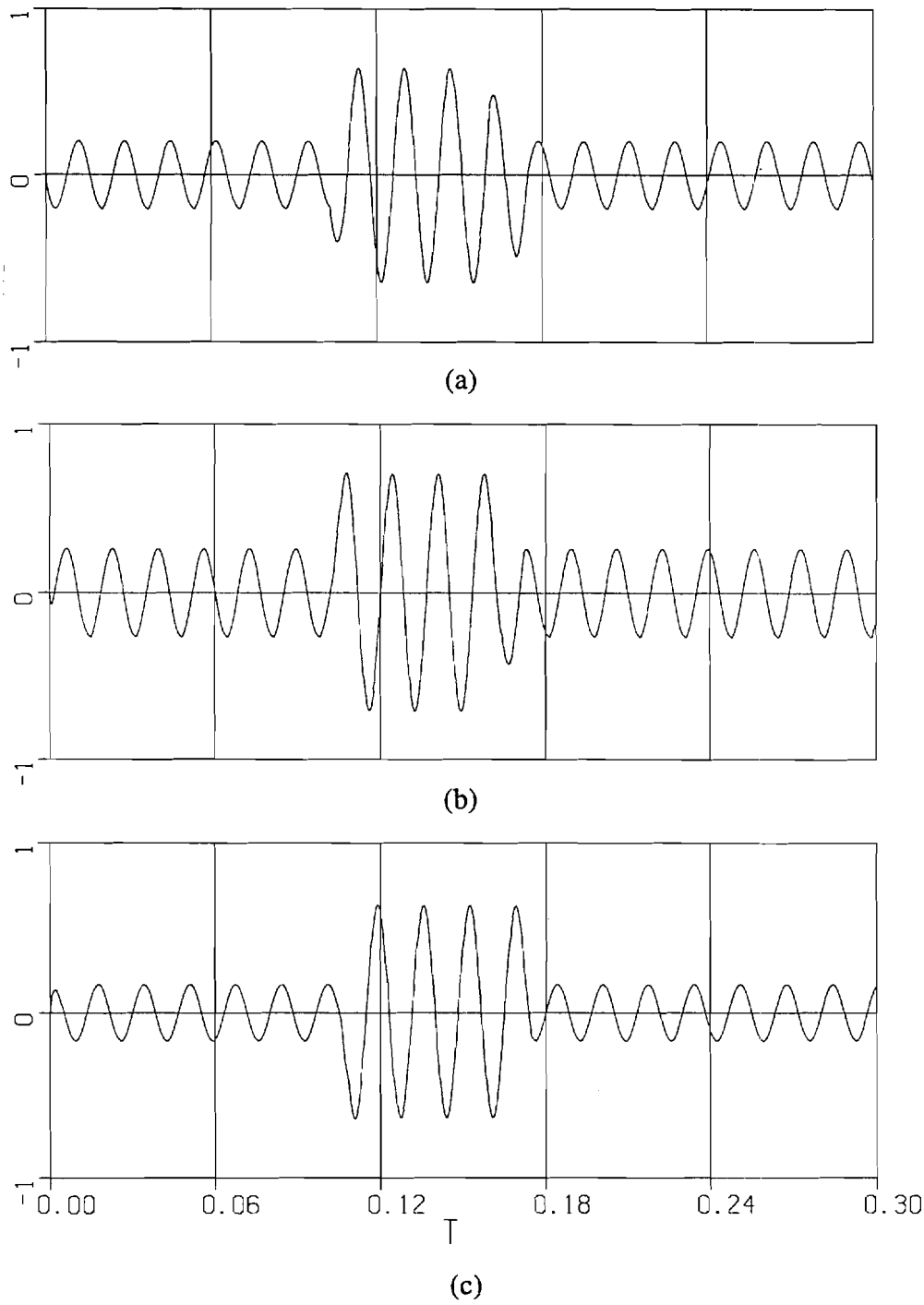

Figure 5.4: Total load currents with AVC disabled; (a) phase C, (b) phase B, (c) Phase **A.**

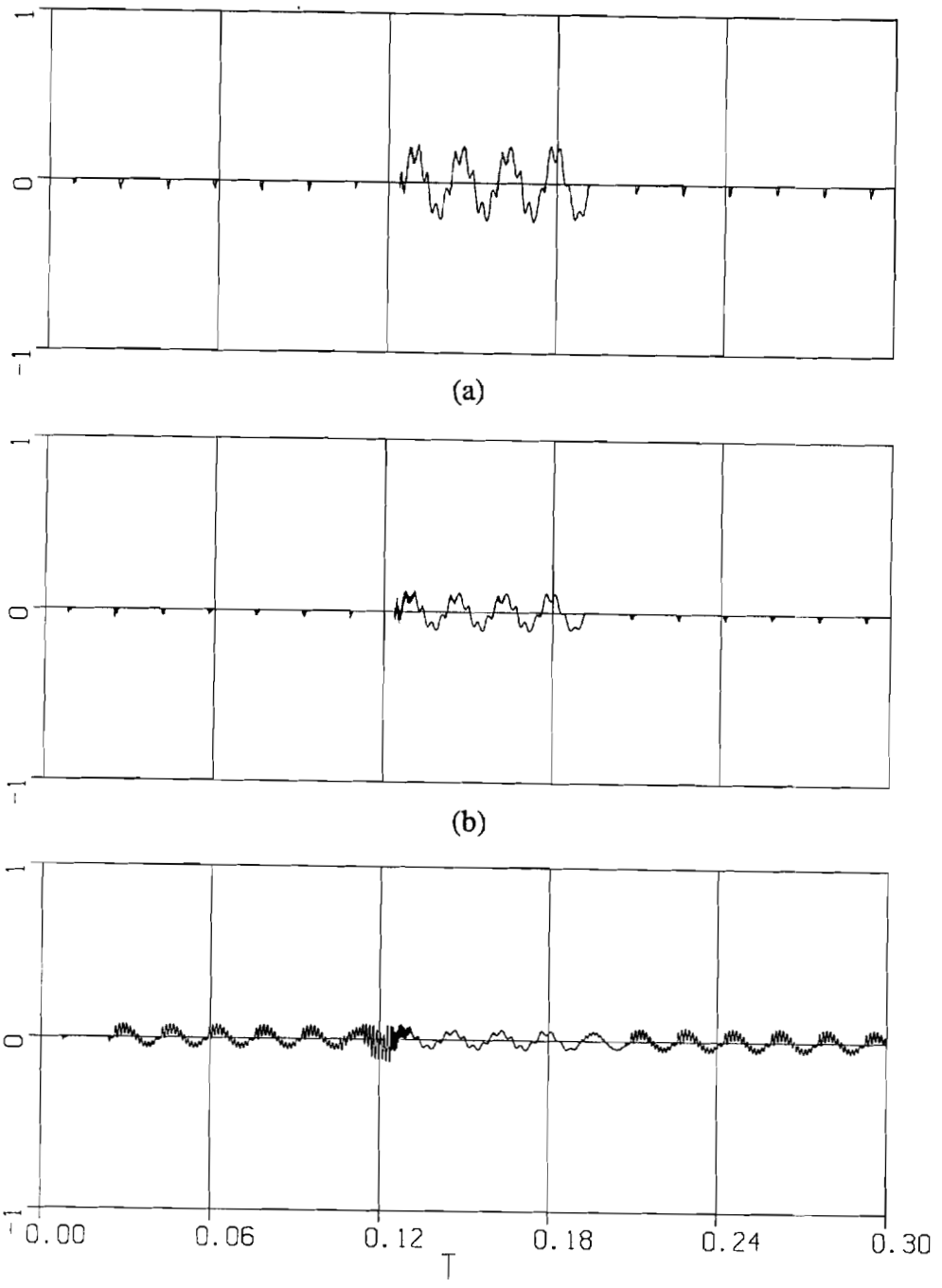

Figure 5.5: System response using 3-bit AVC with RPC control.
Capacitor currents in phase A; (a) Bit 3 current, (b) Bit 2 current,
(c) Bit 1 current.

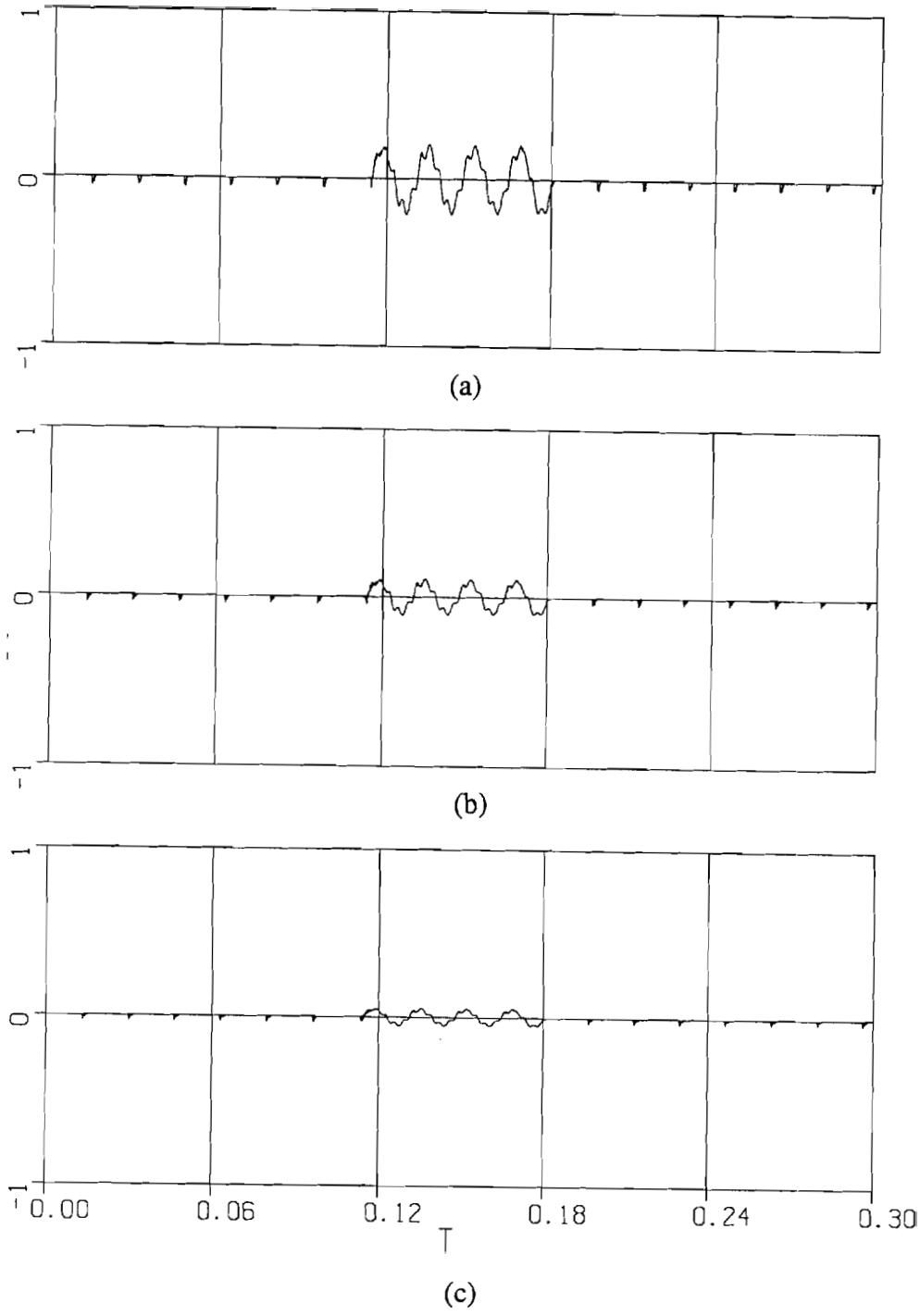

Figure 5.6: System response using 3-bit AVC with RPC control.
Capacitor currents in phase B; (a) Bit 3 current, (b) Bit 2 current,
(c) Bit 1 current.

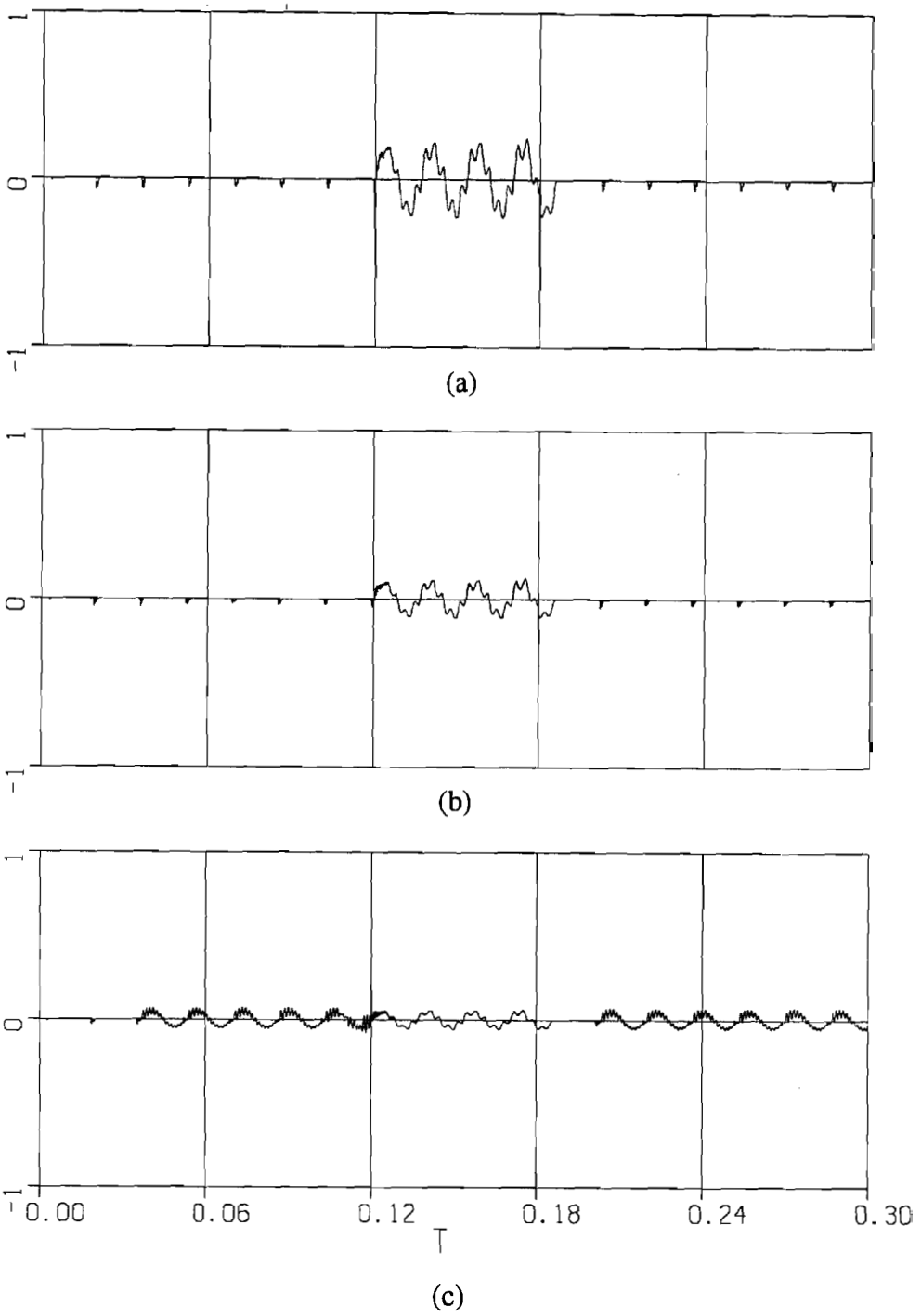

Figure *5.7:* System response using 3-bit AVC with RPC control. Capacitor currents in phase C; (a) Bit 3 current, (b) Bit 2 current, (c) Bit 1 current.

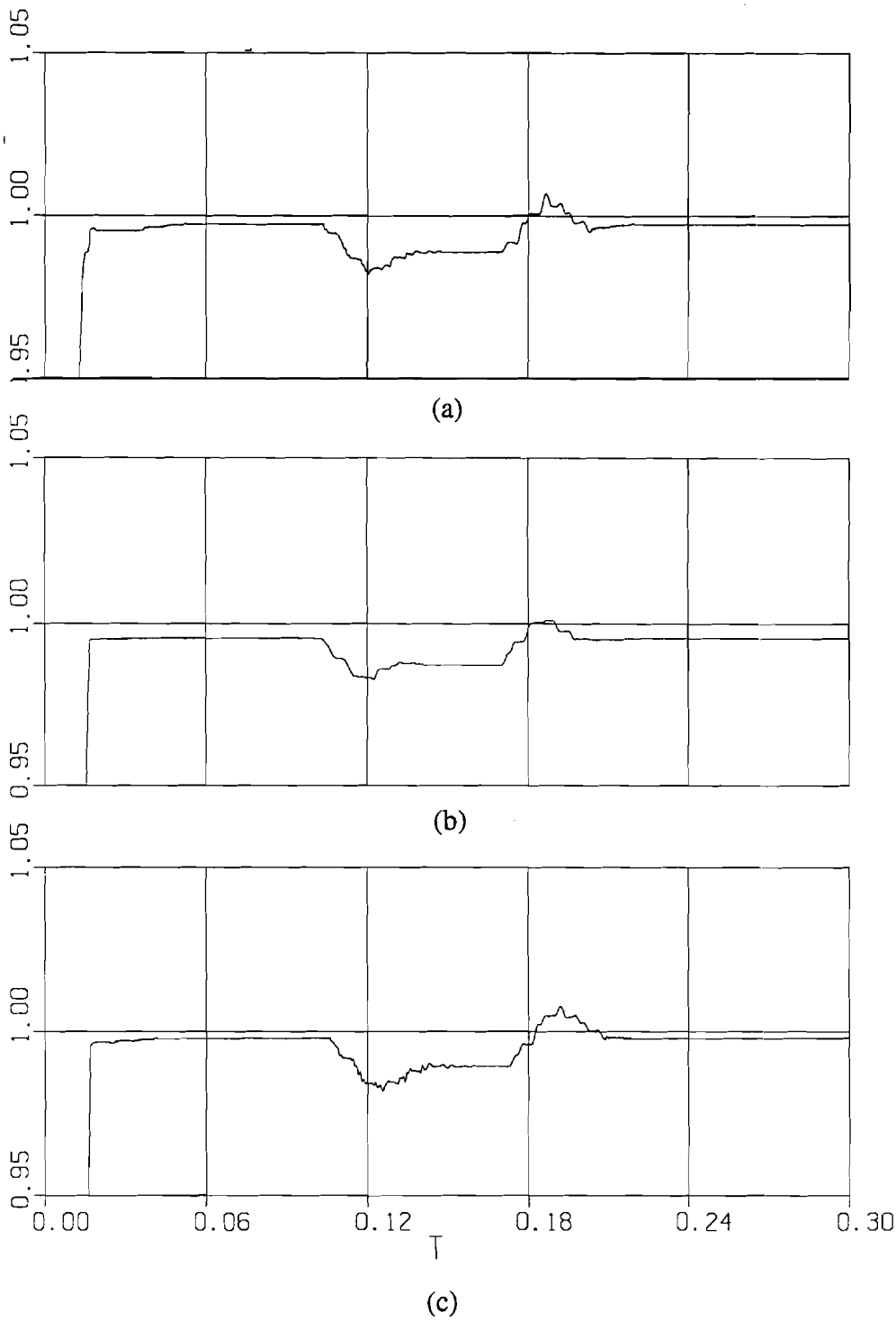

Figure 5.8: RMS voltages at the PCC using 3-bit AVC with RPC control; (a) phase A, (b) phase B, (c) phase C.

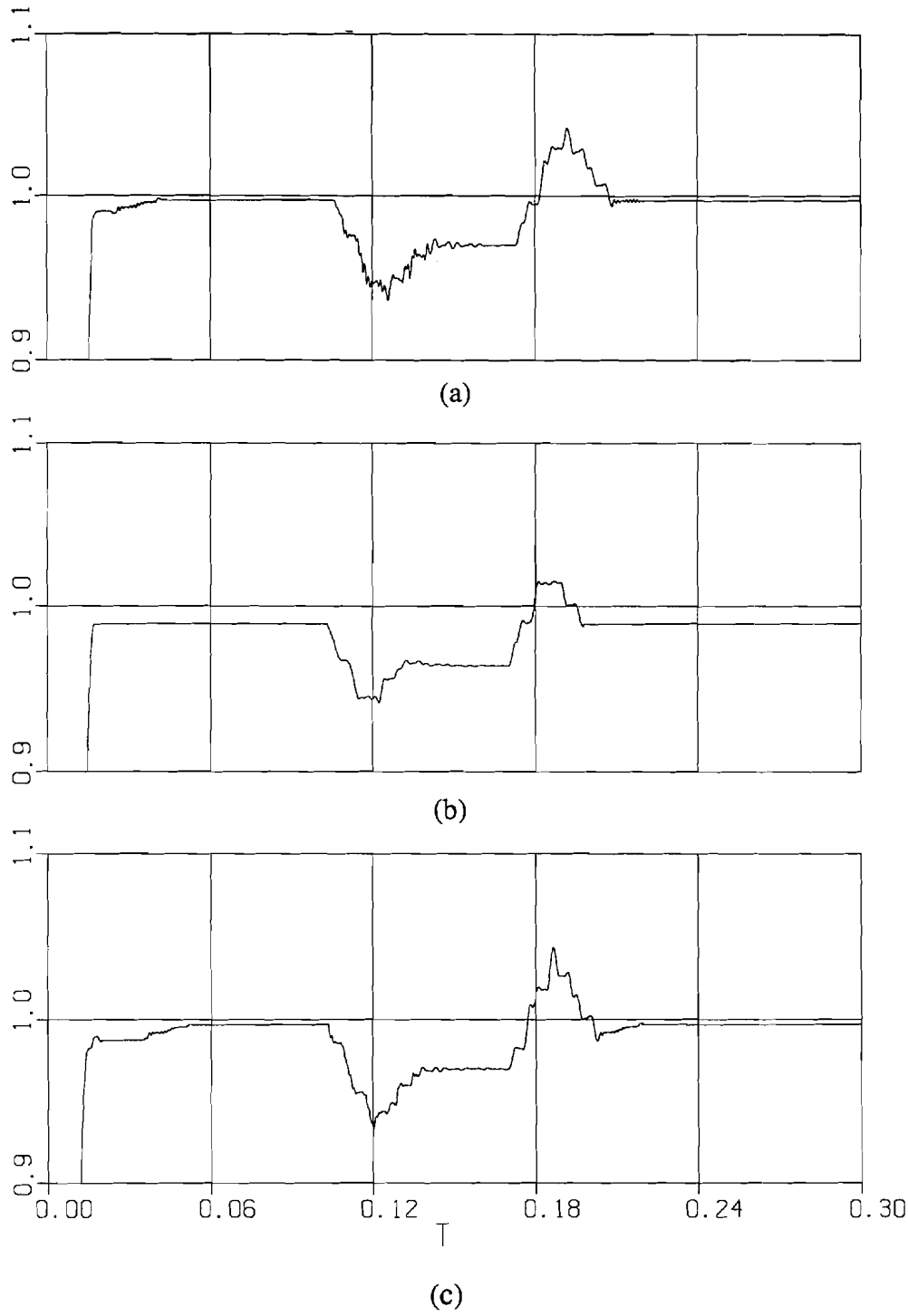

Figure 5.9: RMS voltages at the load end using 3-bit **AVC** with RPC control; (a) phase **A,** (b) phase **B,** (c) phase **C.**

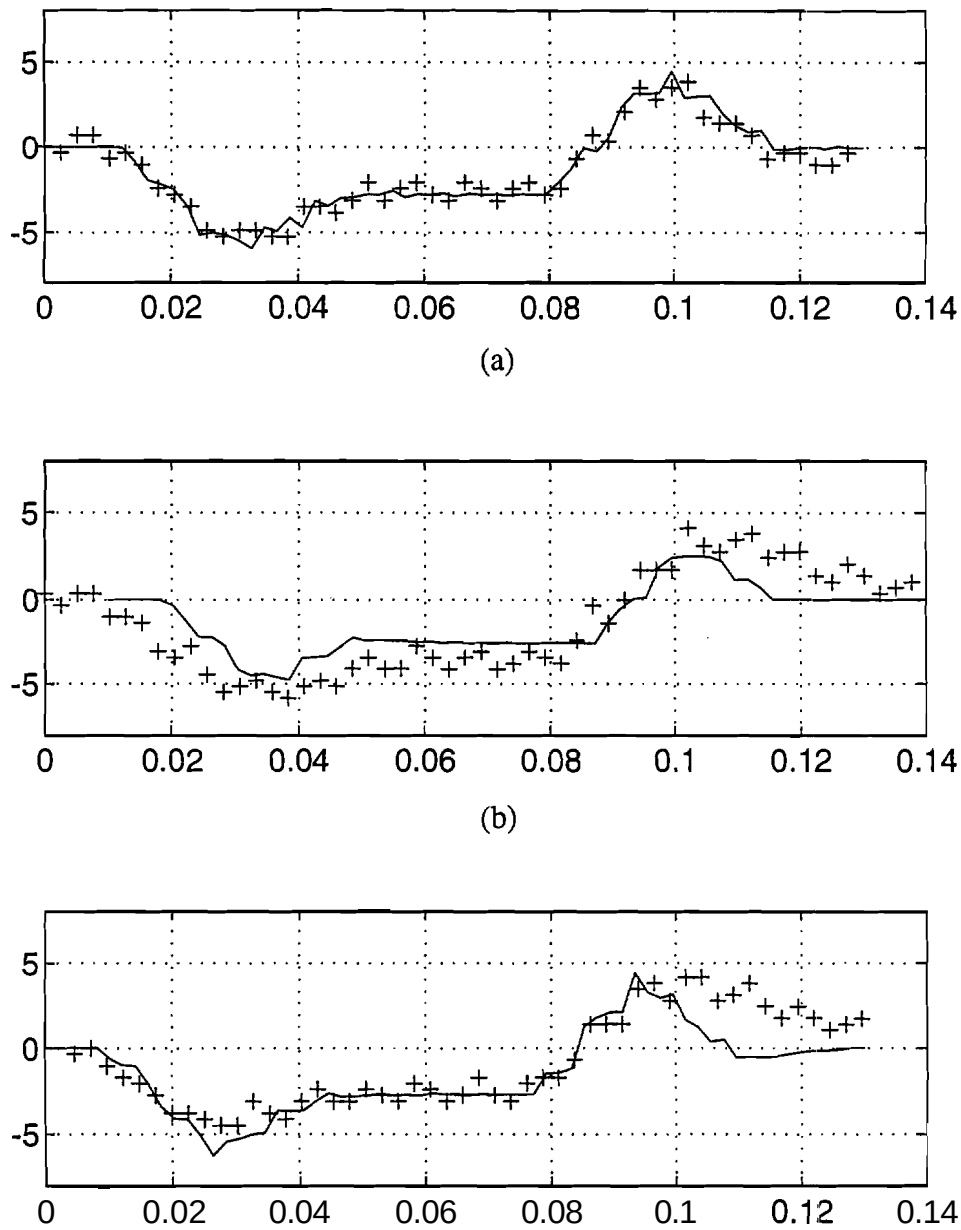

Figure 5.10: RMS voltages at the load end using 3-bit **AVC** with **RPC** control. Comparison of measured and simulated fluctuation of RMS voltages; (a) phase **A,** (b) phase **B,** (c) phase **C.**

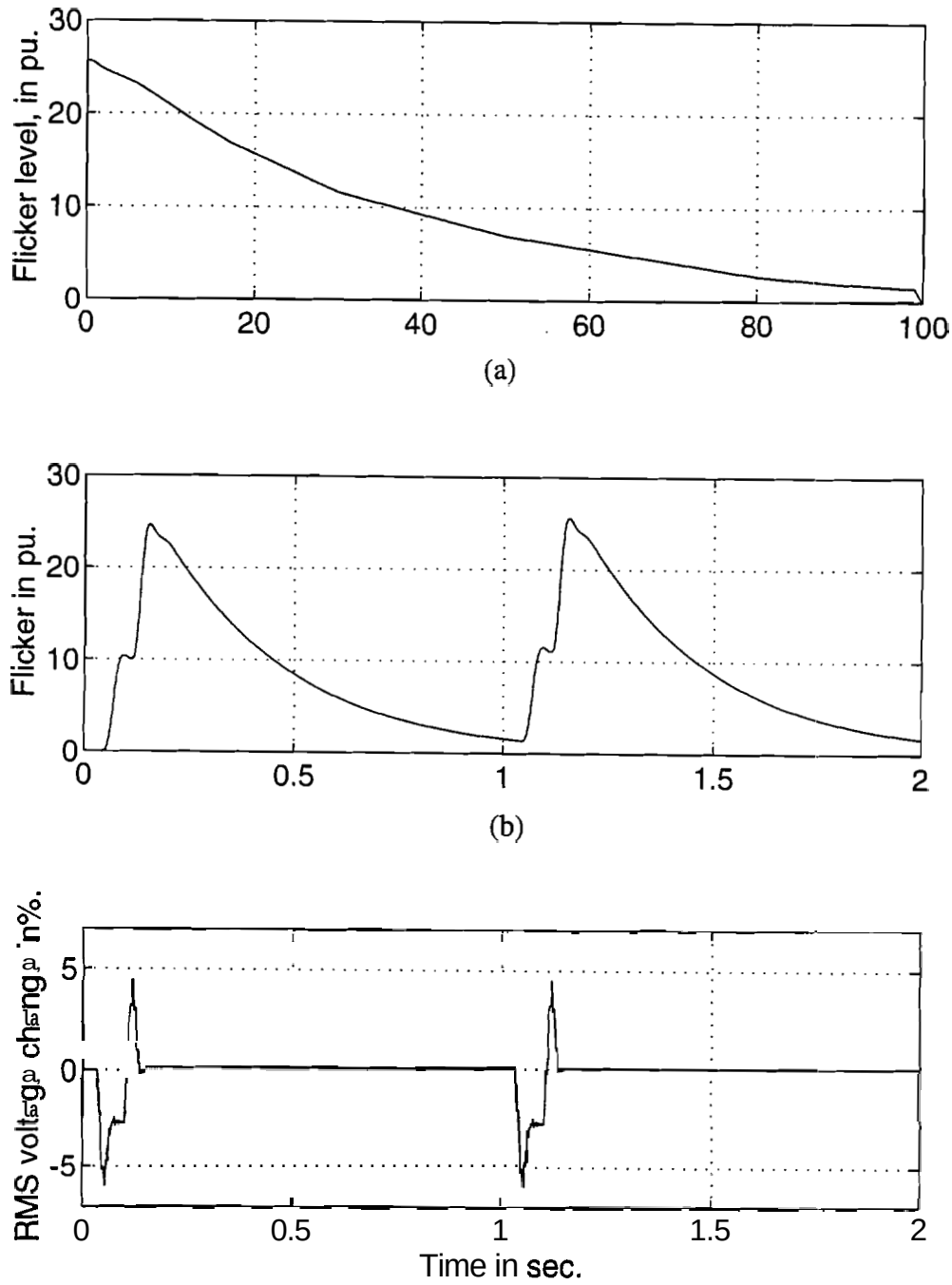

Figure 5.11: Examples of flickermeter studies. System with 3-bit AVC using RPC. Phase A at the load end; (a) CPF, (b) fragment of instantaneous flicker sensation, (c) fragment of voltage fluctuation.

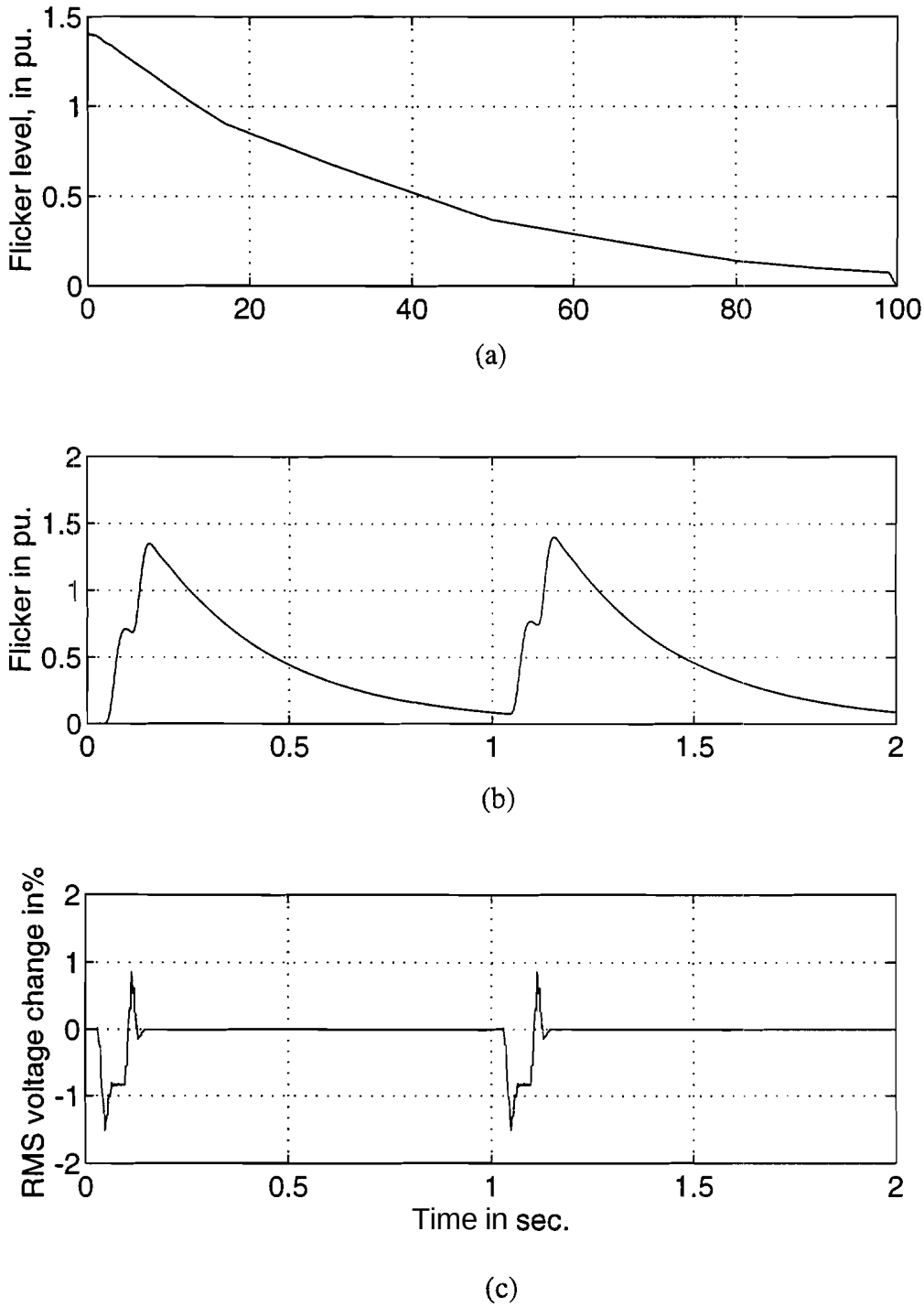

Figure 5.12: Examples of flickermeter studies. System with 3-bit AVC using RPC. Phase A at the PCC; (a) CPF, (b) fragment of instantaneous flicker sensation, (c) fragment of voltage fluctuation.

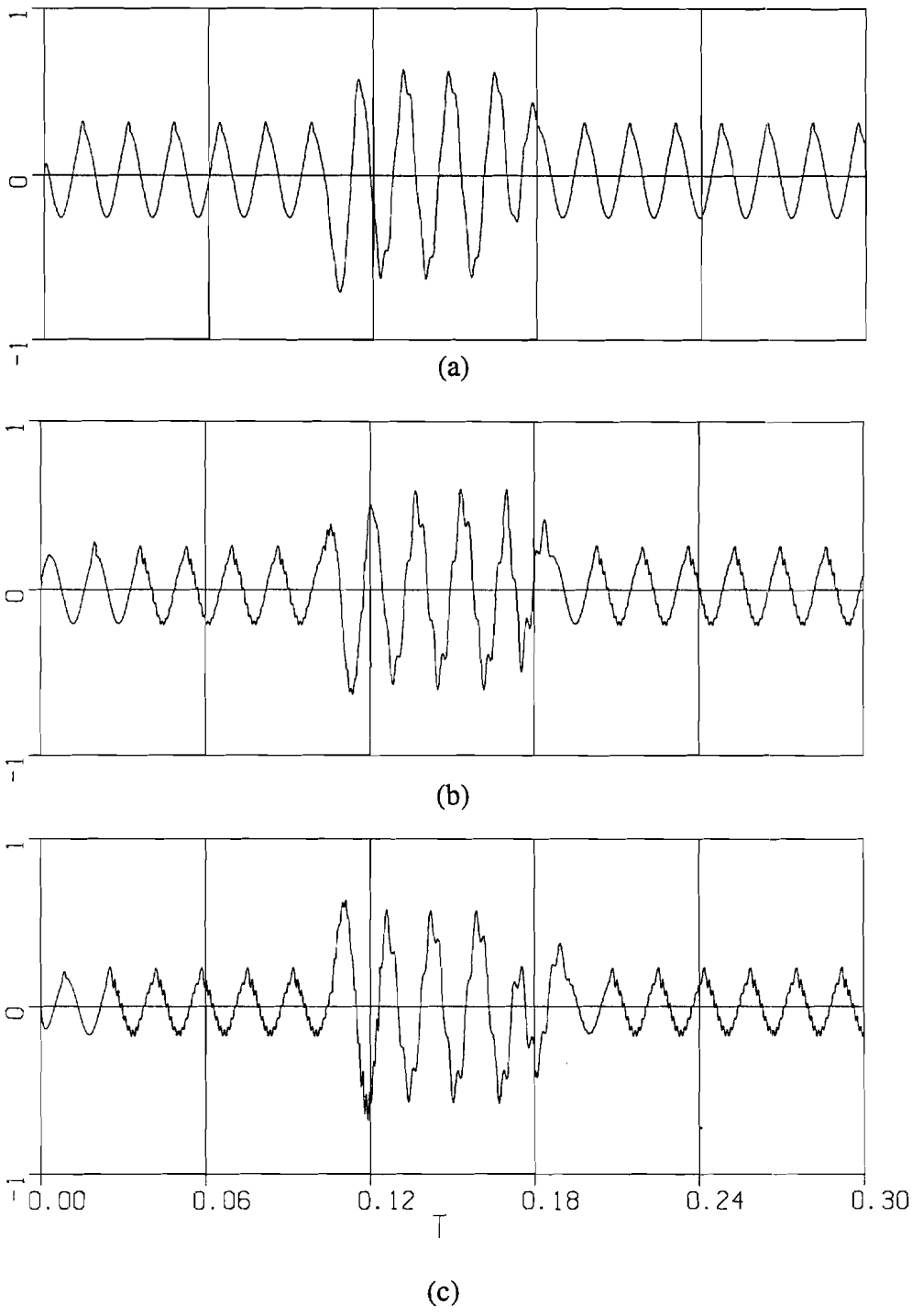

Figure 5.13: Source currents using 3-bit AVC with RPC control.; (a) phase A, (b) phase B, (c) phase C.

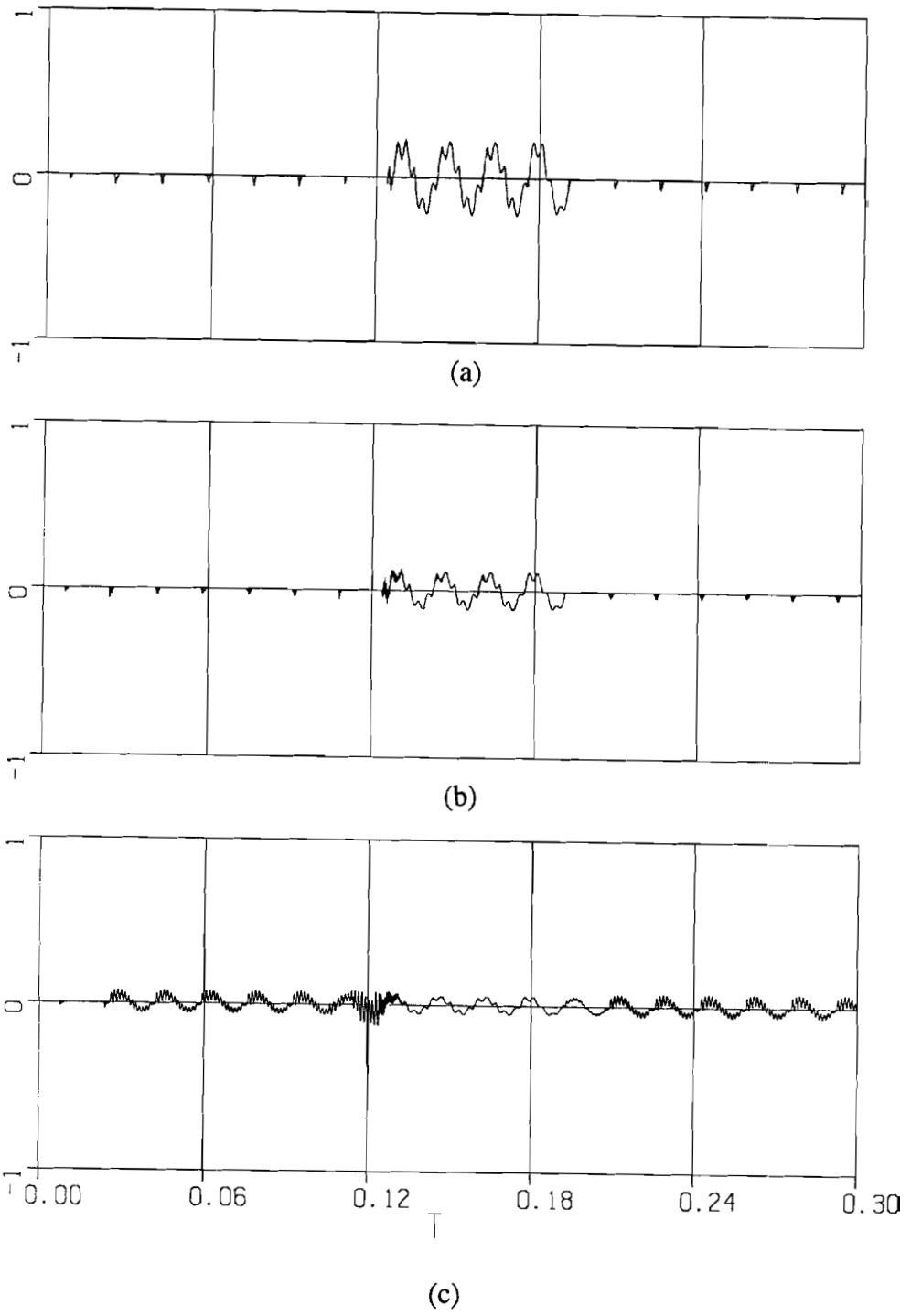

Figure 5.14: Capacitor currents in phase A using 3-bit AVC with FAC; **(a)** Bit 3 current, (b) Bit **2** current, (c) Bit 1 current.

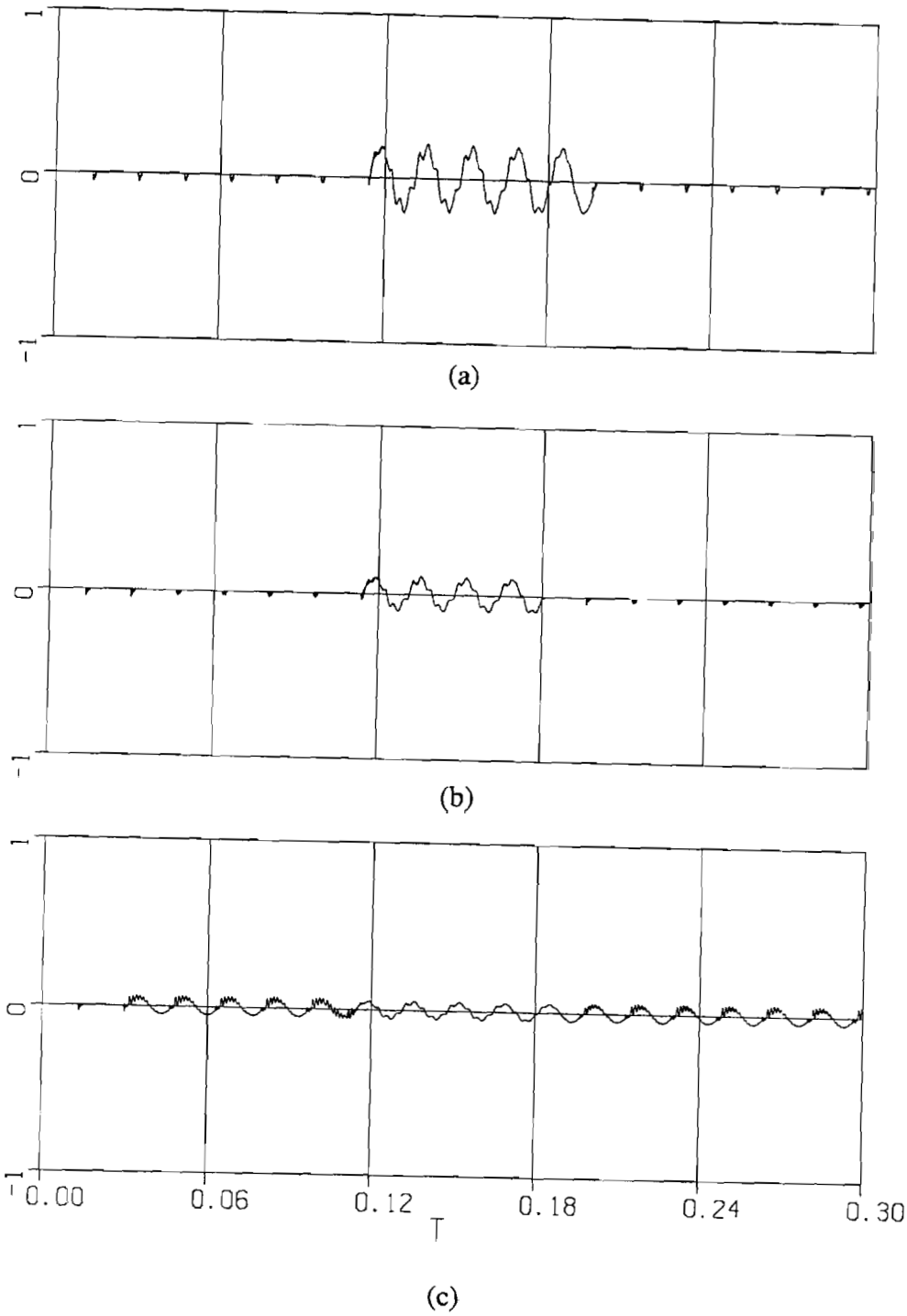

Figure 5.15: Capacitor currents in phase B using 3-bit AVC with FAC;
(a) Bit 3 current, (b) Bit 2 current, (c) Bit 1 current.

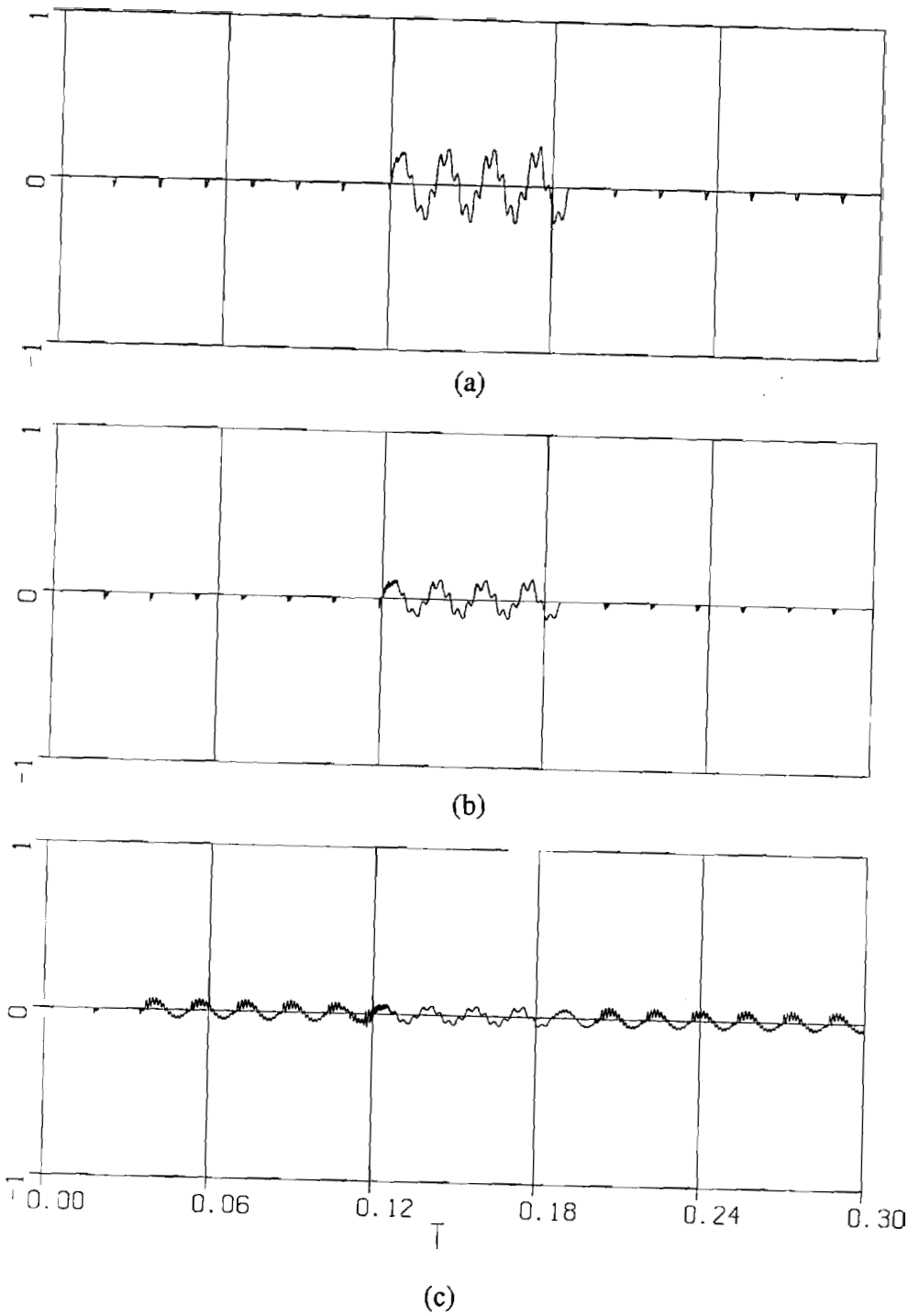

Figure 5.16: Capacitor currents in phase C using 3-bit AVC with FAC;
(a) Bit 3 current, (b) Bit 2 current, (c) Bit 1 current.

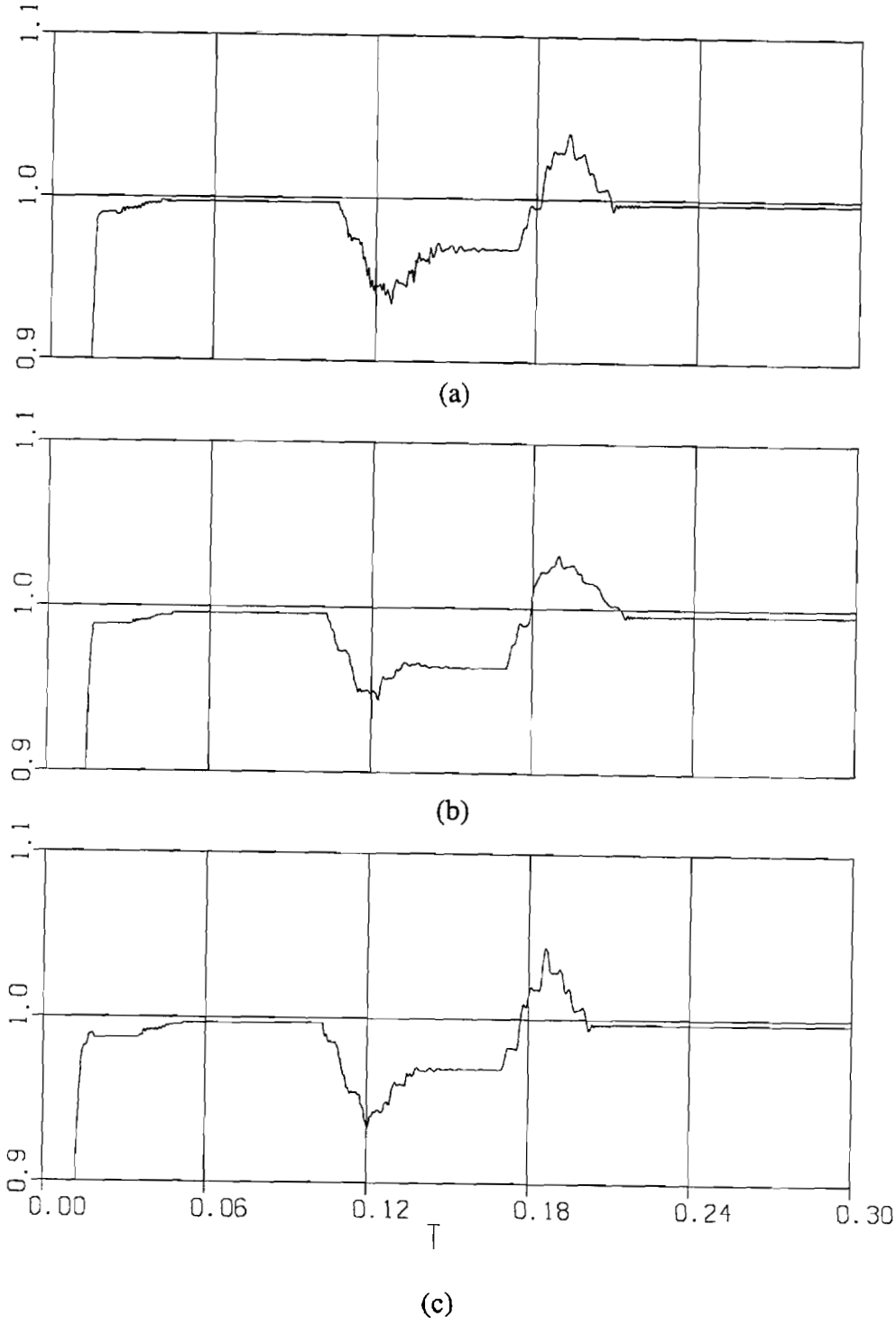

Figure 5.17: RMS voltages at the load end using 3-bit AVC with FAC; (a) phase **A,** (b) phase B, (c) phase C.

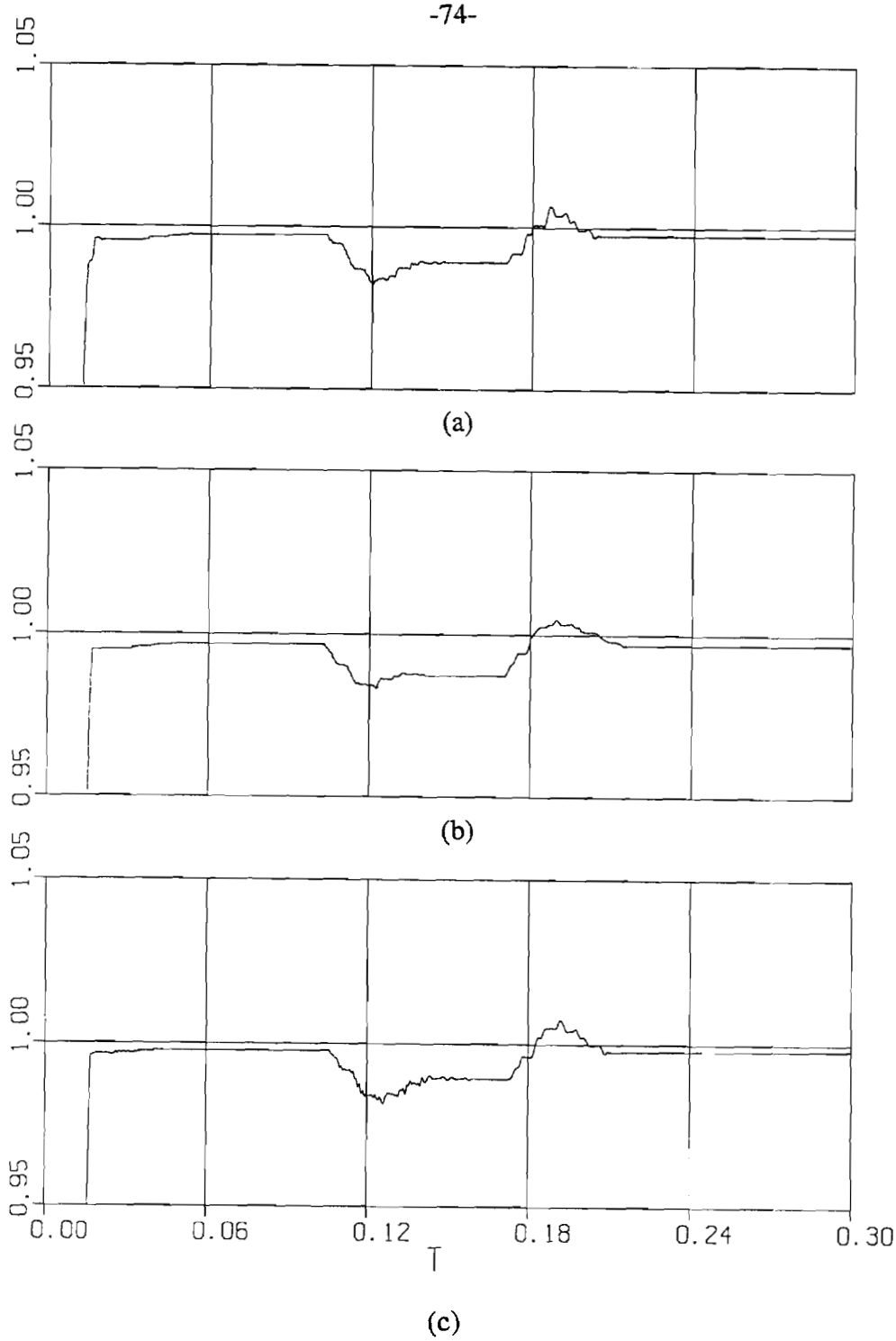

Figure 5.18: RMS voltages at the PCC using 3-bit AVC with FAC; (a) phase A, (b) phase B, (c) phase C.

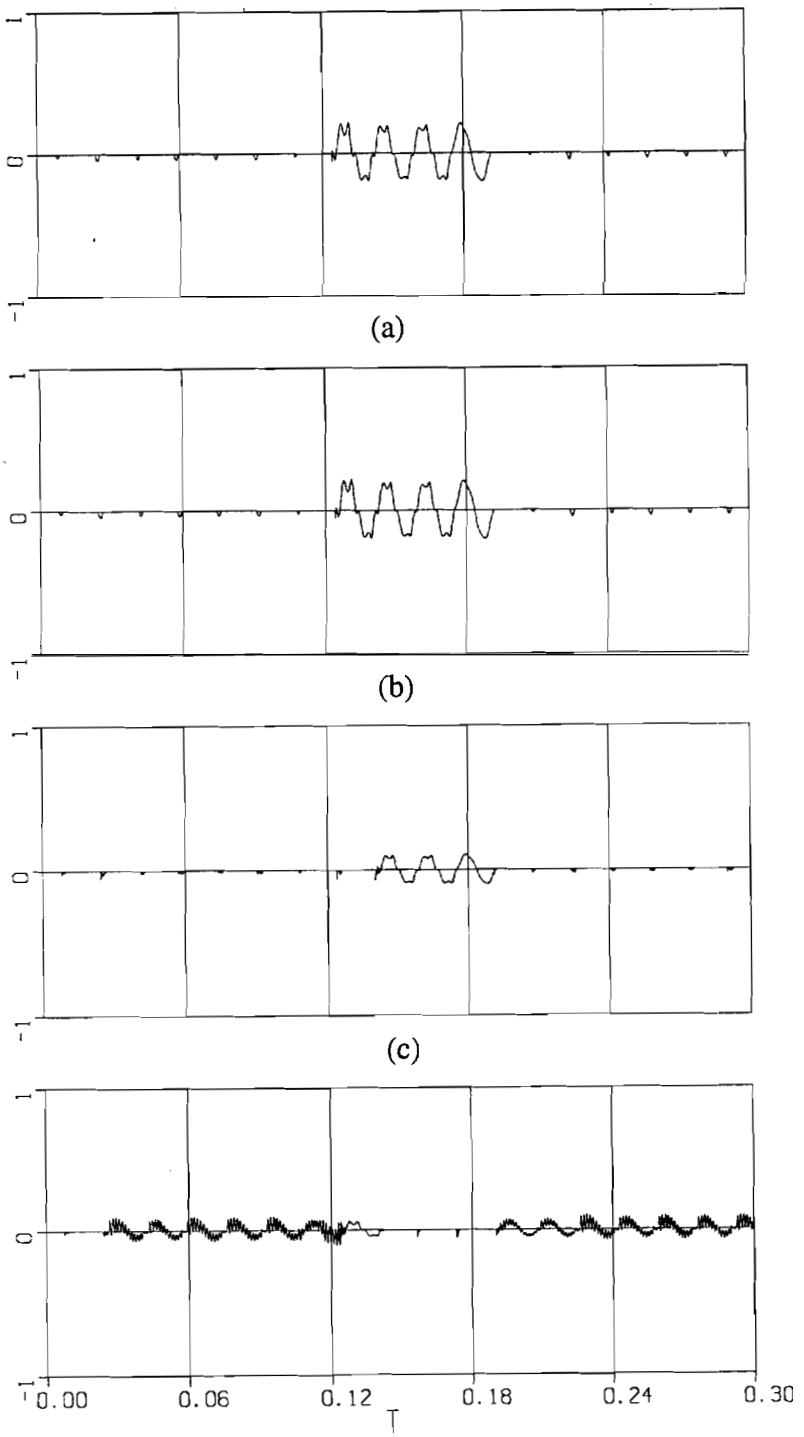

Figure 5.19: Capacitor currents in phase A using 4-bit AVC with RPC control;
(a) Bit 4 current, (b) Bit 3 current, (c) Bit 2 current,
(d) Bit 1 current.

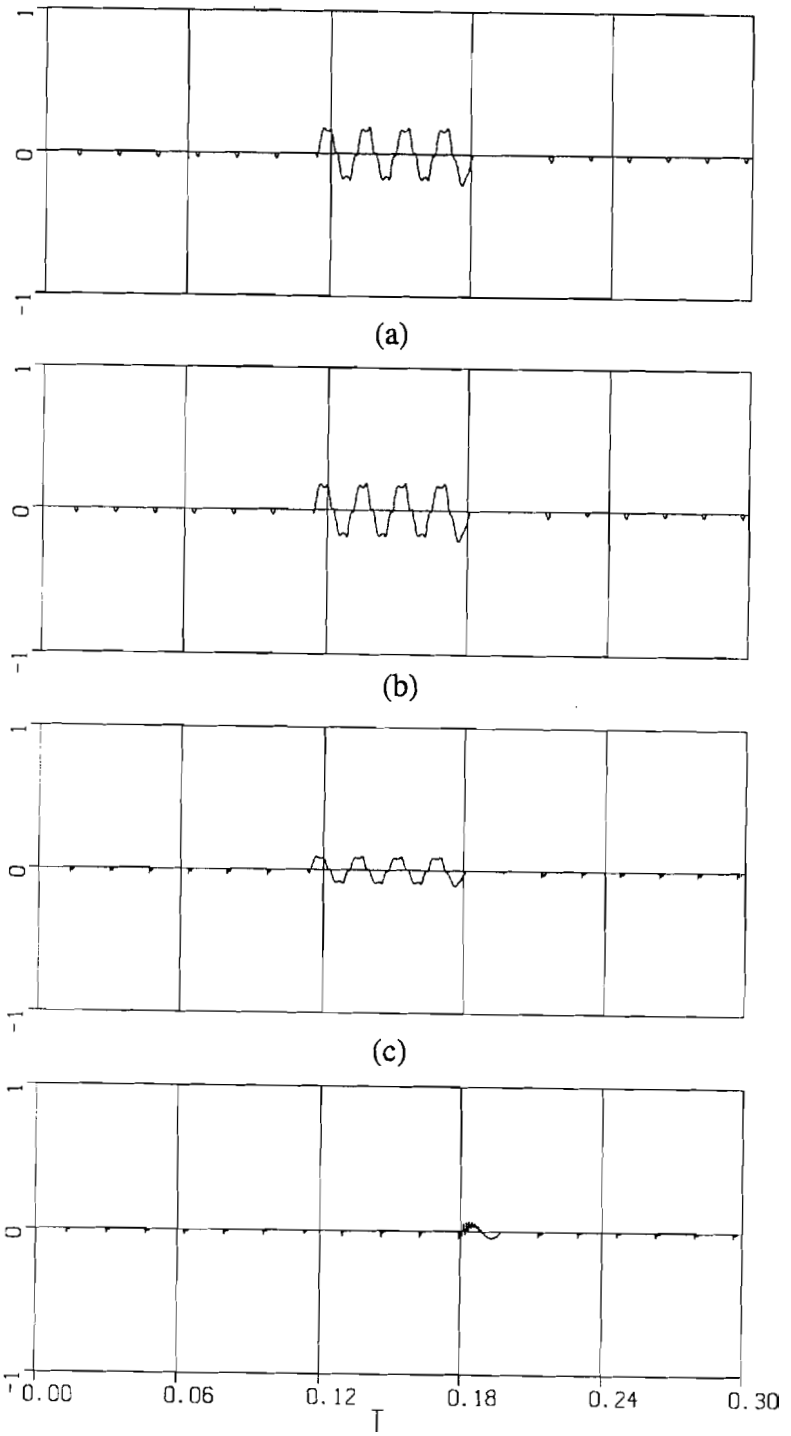

Figure 5.20: Capacitor currents in phase B using 4-bit AVC with RPC control;
(a) Bit 4 current, (b) Bit 3 current, (c) Bit 2 current,
(d) Bit 1 current.

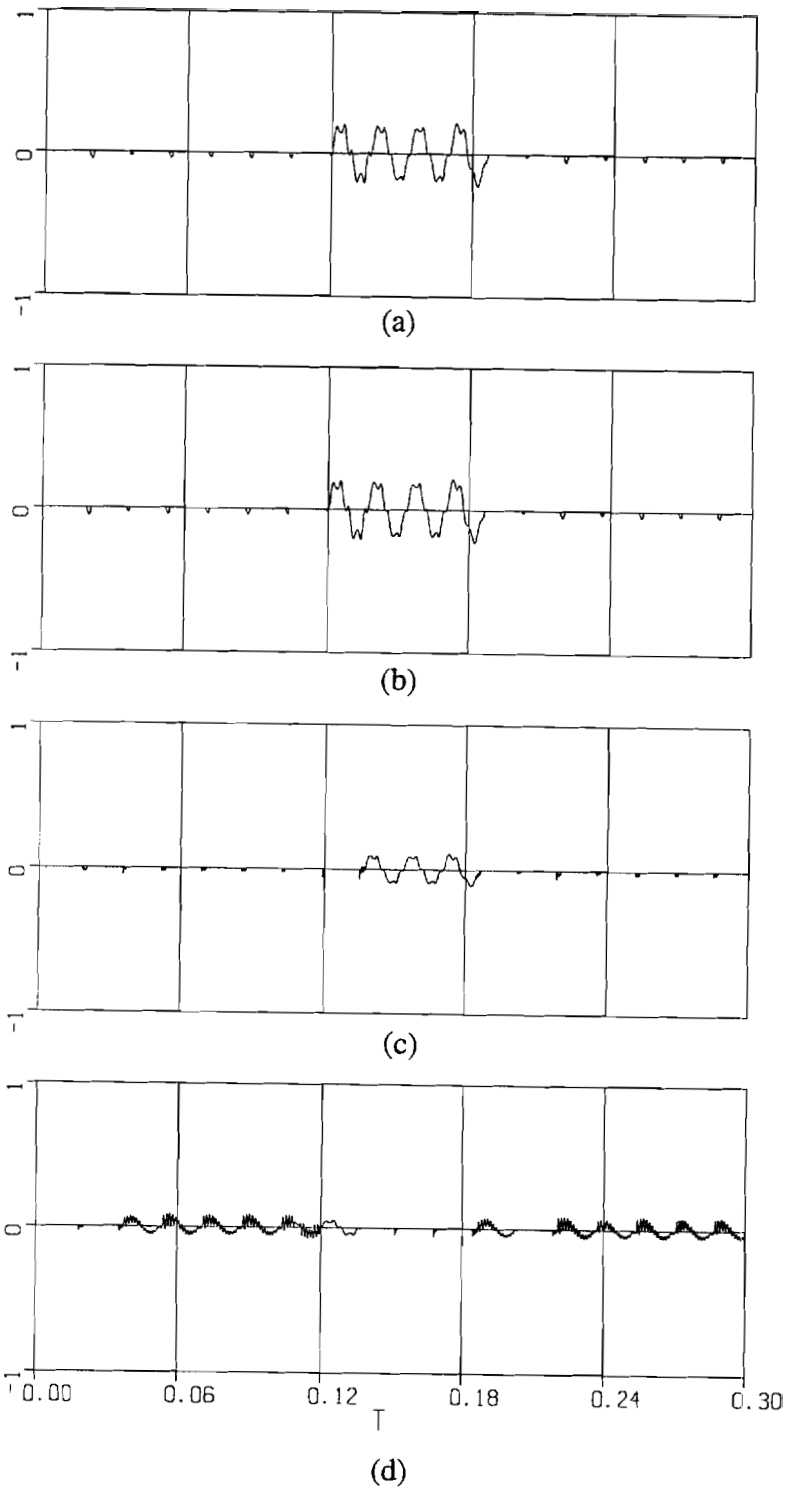

Figure 5.21: Capacitor currents in phase C using 4-bit AVC with RPC control;
(a) Bit 4 current, (b) Bit 3 current, (c) Bit 2 current.,
(d) Bit 1 current.

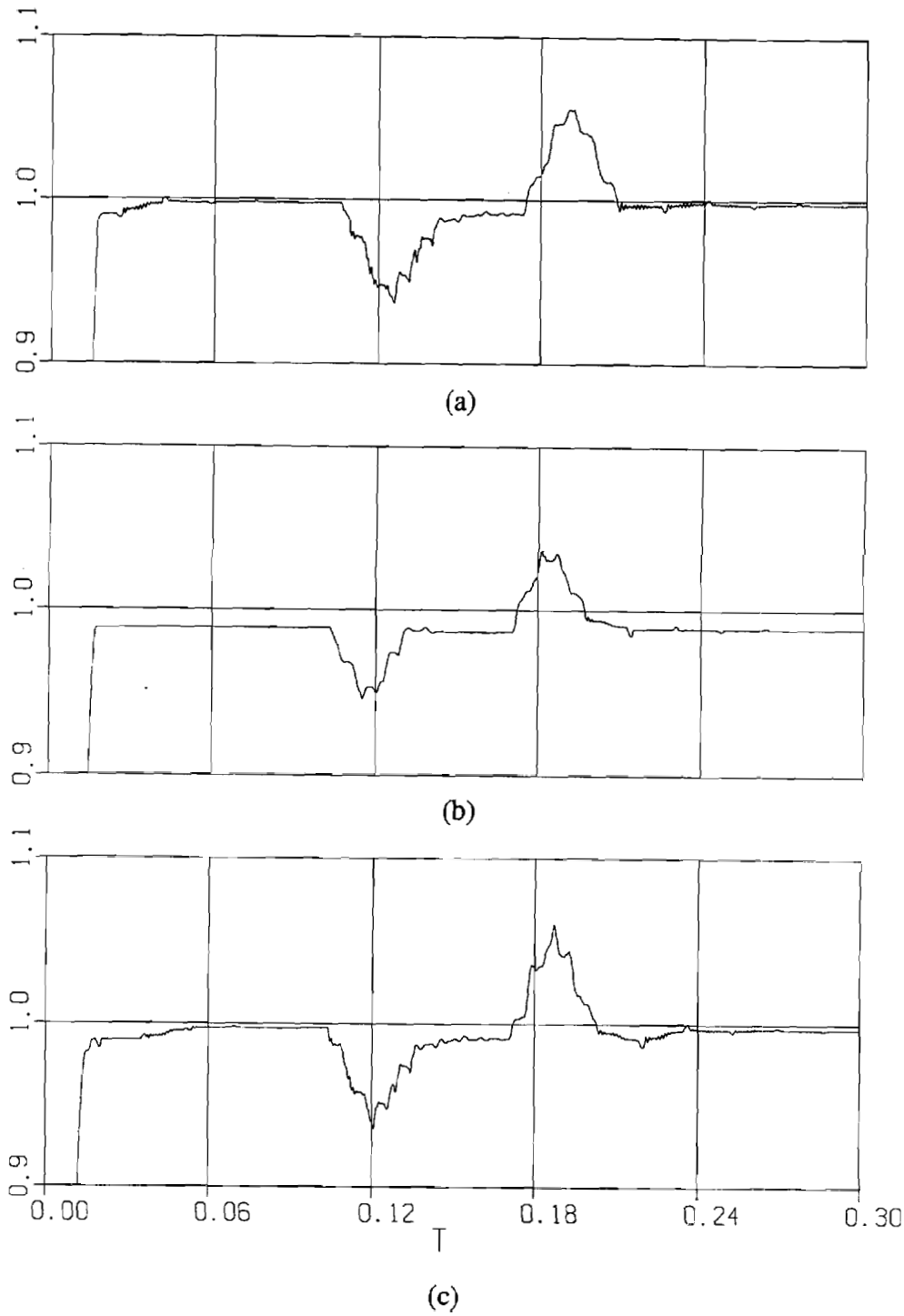

Figure 5.22: RMS voltages at the load end using 4-bit **AVC** with RPC control; (a) phase **A,** (b) phase **B,** (c) phase **C.**

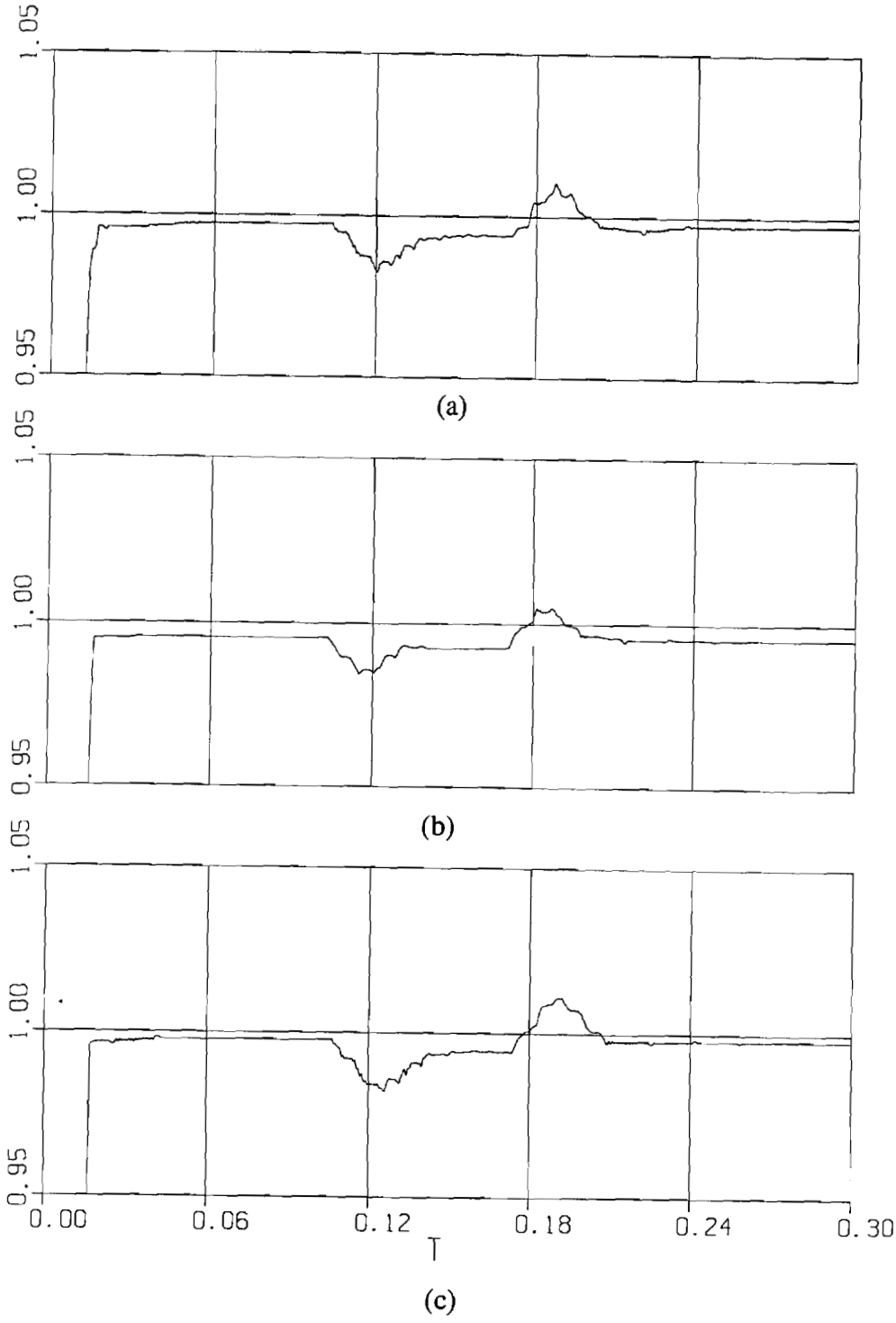

Figure 5.23: RMS voltages at the PCC using 4-bit AVC with RPC control; (a) phase **A,** (b) phase B, (c) phase C.

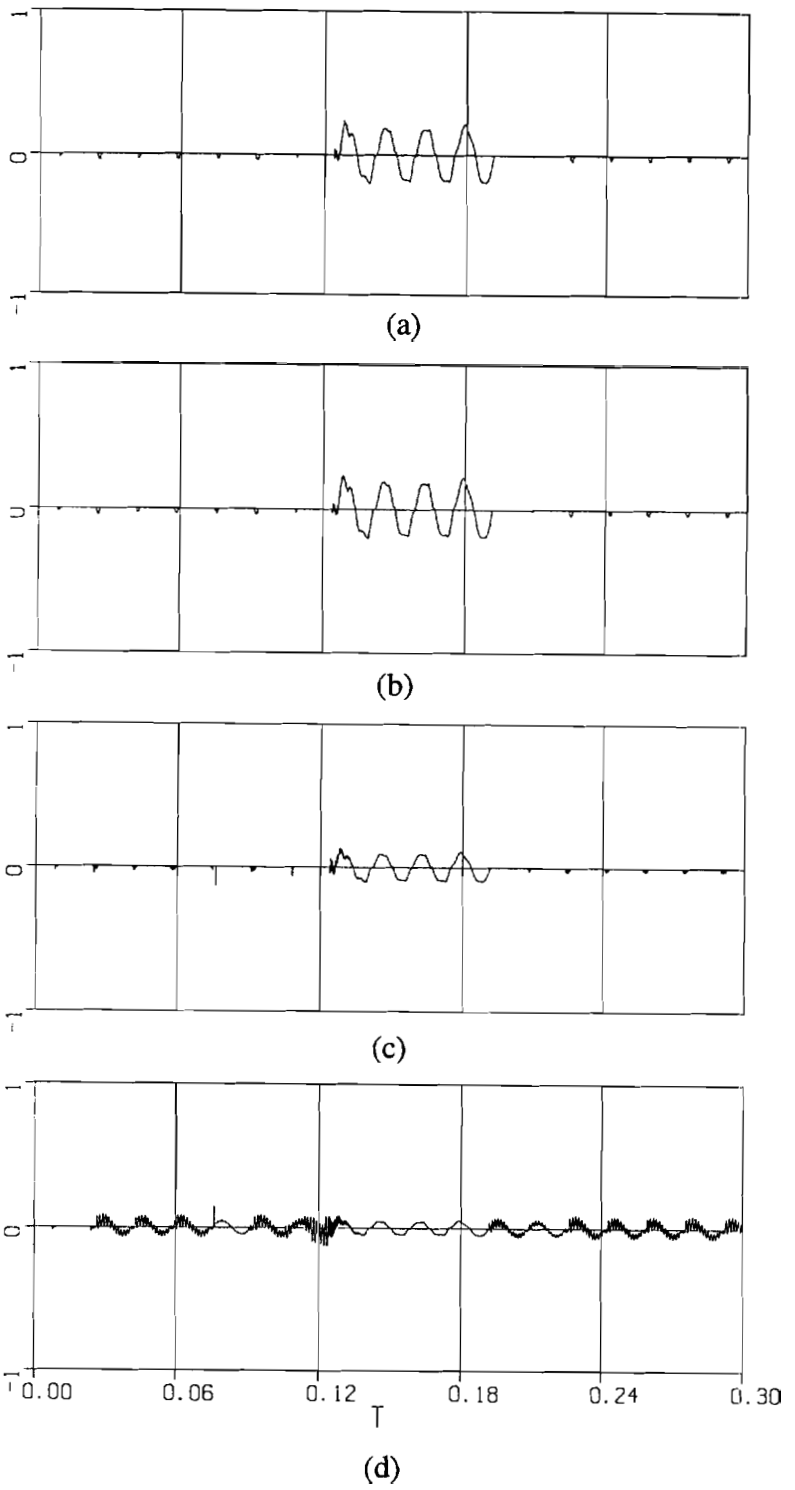

Figure 5.24: Capacitor currents in phase A using 4-bit AVC with FAC;
(a) Bit 4 current, (b) Bit 3 current, (c) Bit 2 current,
(d) Bit 1 current.

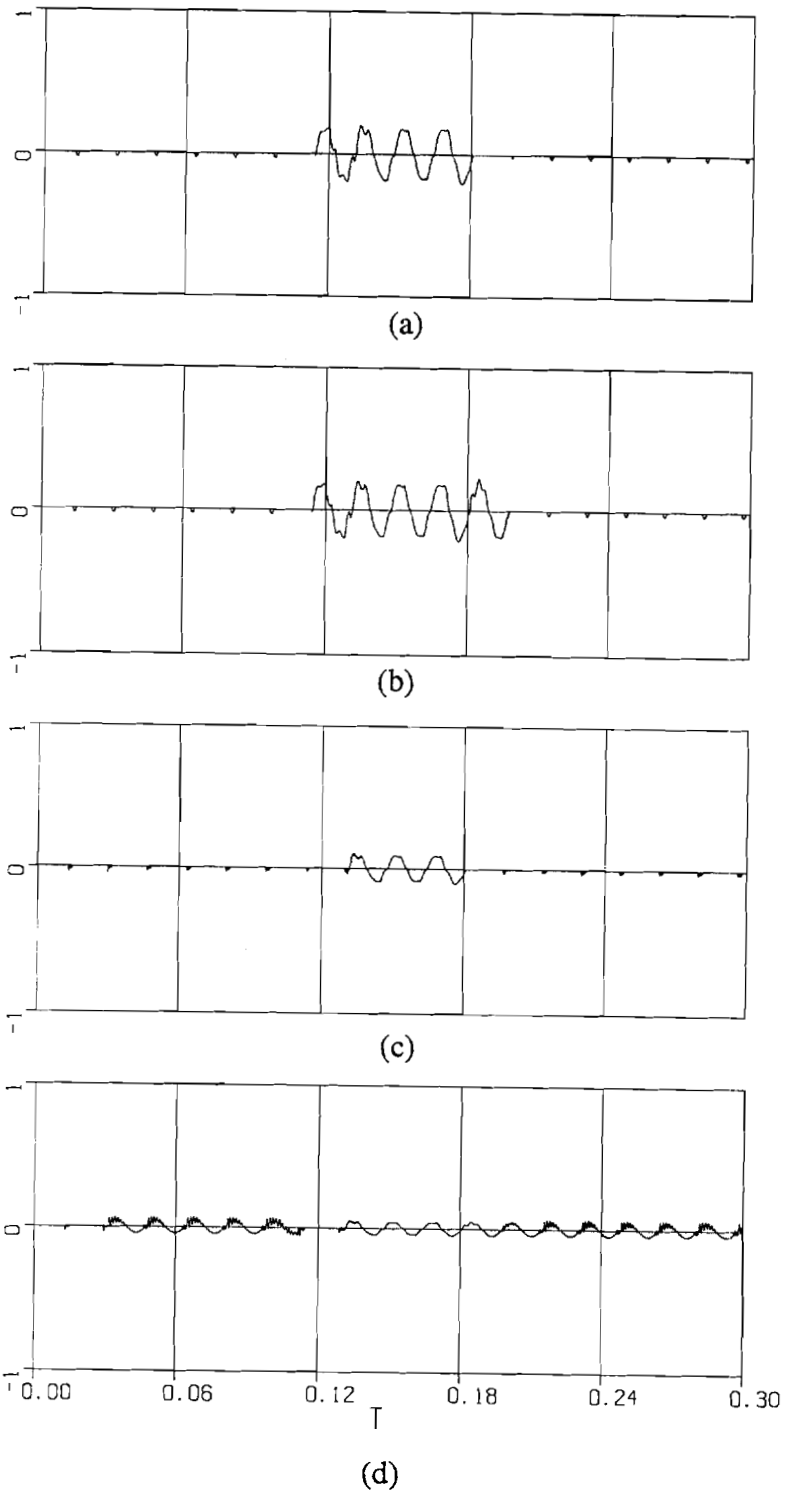

Figure 5.25: Capacitor currents in phase B using 4-bit AVC with FAC;
(a) Bit 4 current, (b) Bit 3 current, (c) Bit 2 current.,
(d) Bit 1 current.

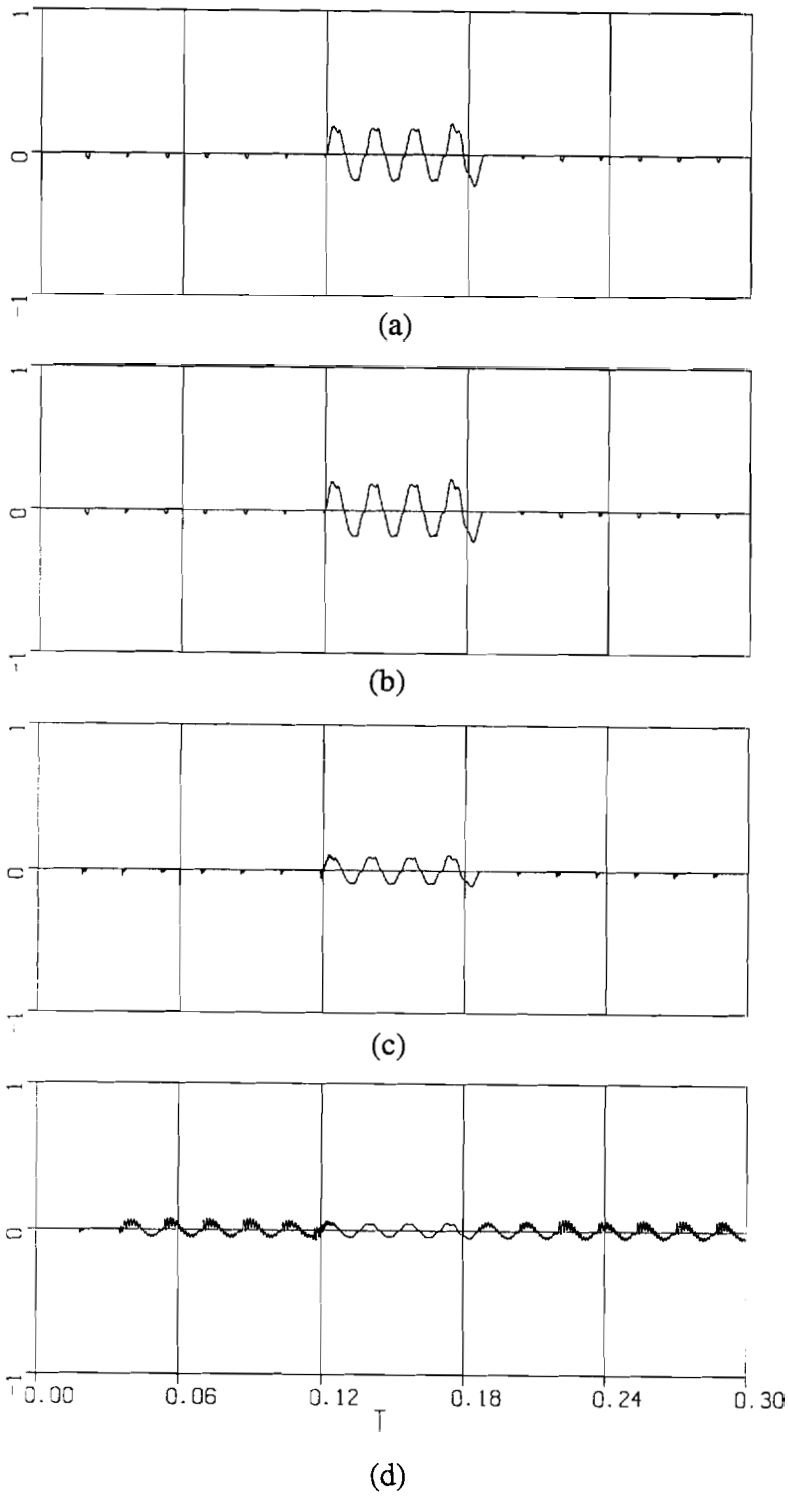

Figure 5.26: Capacitor currents in phase C using 4-bit AVC with FAC;
(a) Bit 4 current, (b) Bit 3 current, (c) Bit 2 current,
(d) Bit 1 current.

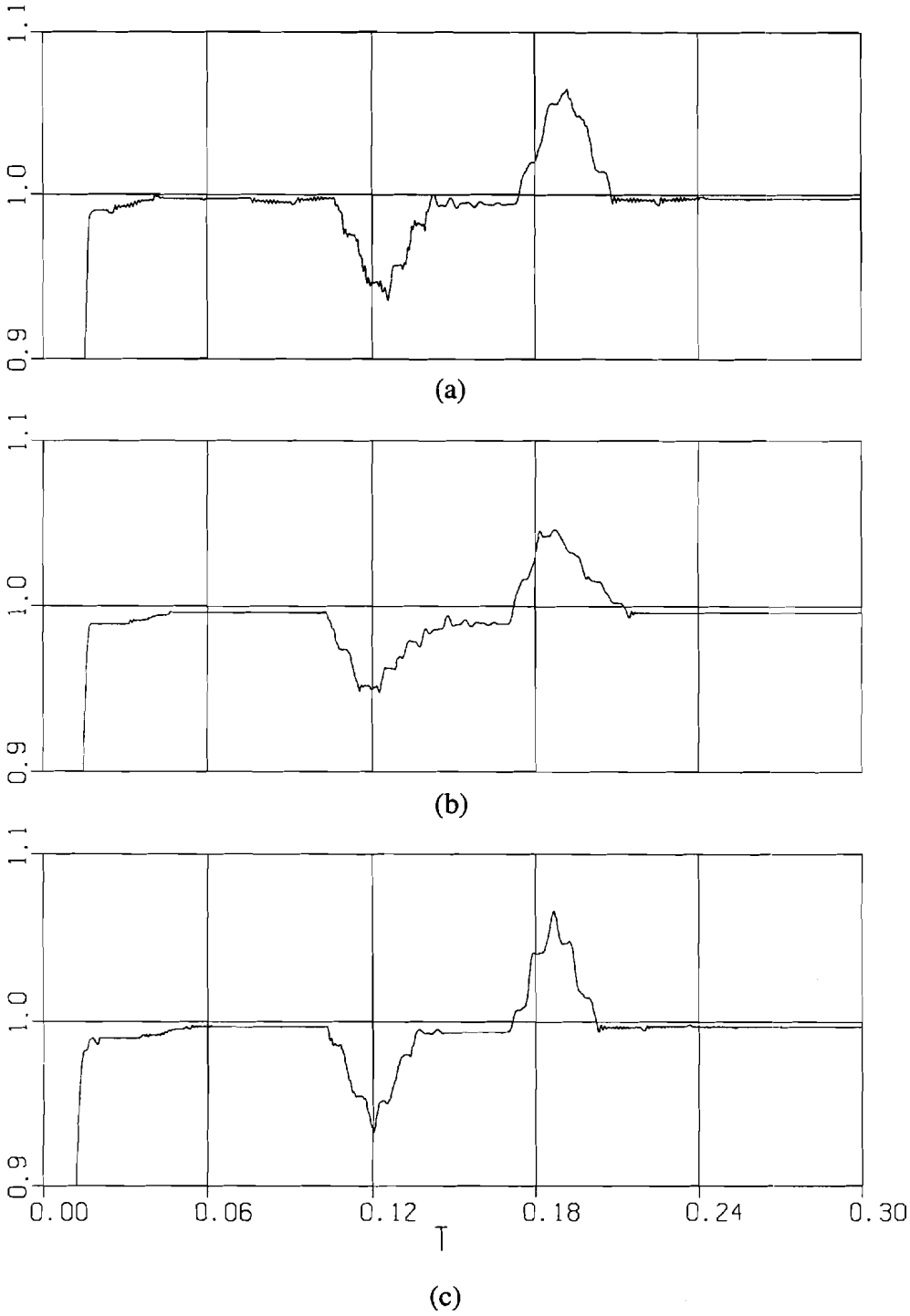

Figure 5.27: RMS voltages at the load end using 4-bit **AVC** with **FAC;** (a) phase **A,** (b) phase B, (c) phase C.

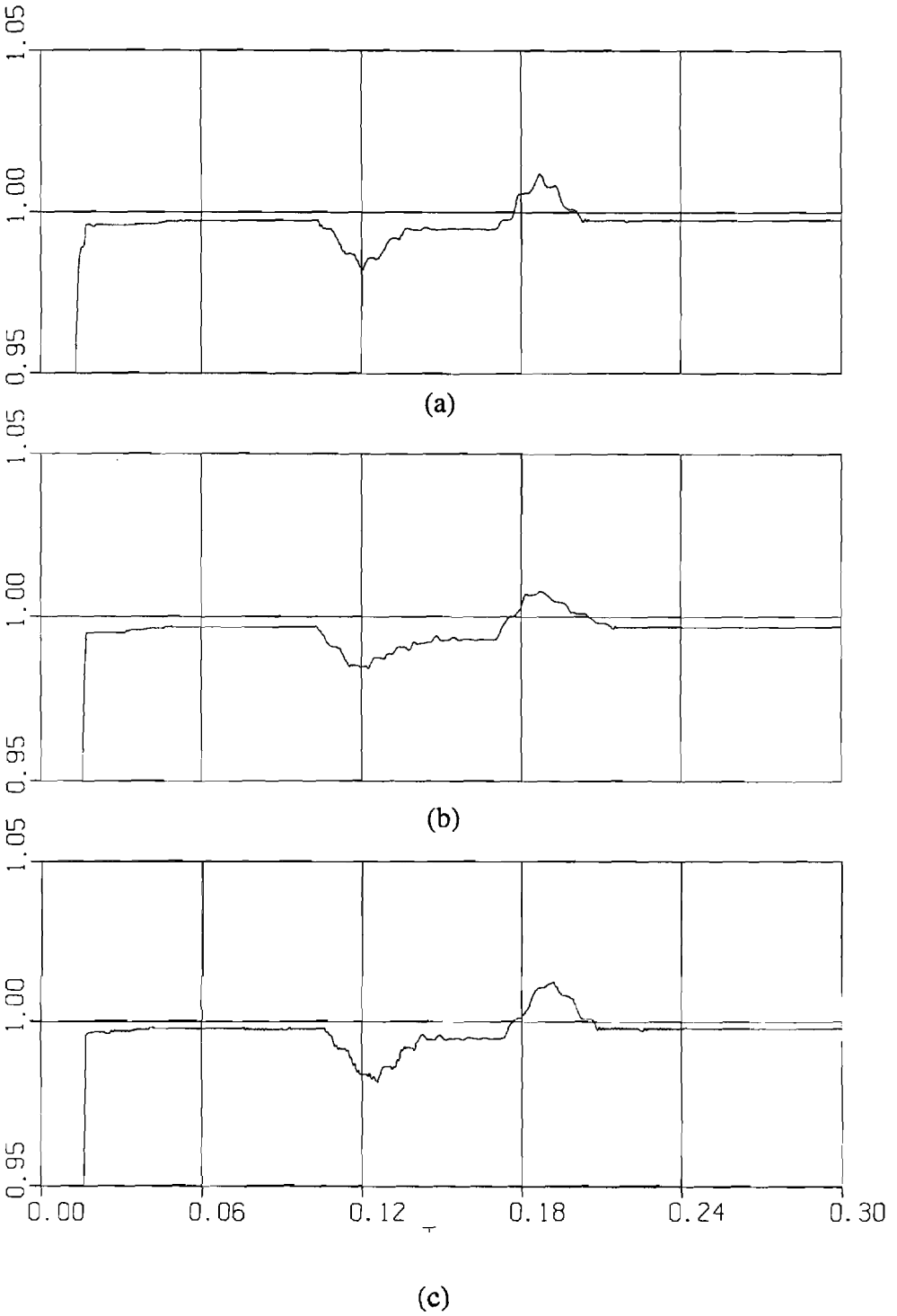

Figure 5.28: RMS voltages at the PCC using 4-bit AVC with FAC;
(a) phase A, (b) phase B, (c) phase C.

6. CONCLUSION

A detailed computer model of a three-phase power network which includes inductive loads, arc welders and an AVC has been developed for computer-based analysis of a flicker problem. Computer studies have been conducted to determine the effectiveness of the AVC on the reduction of observable flicker at neighboring loads. Different control strategies involving the AVC have been discussed and compared with respect to flicker reduction. An innovative Flicker Adaptive Control (FAC) strategy is proposed for the AVC. The control algorithm requires knowledge of the system line impedance; however, it can be used for both power factor correction and flicker reduction, which is an advantage over previous control methods. The flicker reduction is achieved by compensation for the RMS voltage drop due not only to a reactive, but also to an active component of the load current. The measurement technique used in the FAC is accurate even in the presence of heavy system distortion, which may be a desirable feature in electrical networks with rectified loads. The AVC has a potential limitation in its ability to reduce flicker caused by very brief disturbances such as 4-cycle welds. This limitation becomes noticeable when the duty interval of the load disturbance is of the same time scale as the AVC's natural response delay which is approximately one electrical cycle.

For determining of the flicker severity, the UIE / IEC flickermeter technique adopted for 120-V incandescent lamp was used. This method allows measurement of both instantaneous flicker level and flicker severity in a precise and unique way, superior to existing flicker-related curves and standards. Therefore, the UIE / IEG flickermeter was found to be worthwhile for further development and wider adoption in establishing flicker standards in North America.

The separation of the overall system into a transient model and a flickermeter with its library of events provides a computationally efficient and flexible method for modeling of power systems for flicker study and prediction. The simulation technique

developed in this thesis, therefore, can be useful for a computer-based analysis of power systems with flicker-related problems caused by other loads or to evaluate the effectiveness of alternative flicker-reduction strategies.

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