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2-7-2006

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Kulkarni, Jaydeep Prakash and Roy, Kaushik, "A Low Power High Performance Multiplexed Keeper Technique" (2006). *ECE Technical Reports*. Paper 331.  
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**ECE Technical Report**

# **A Low Power High Performance Multiplexed Keeper Technique**

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February, 2006

## **Abstract**

This paper presents a technique to improve the performance of wide dynamic circuits by efficiently using the conditional keeper. PMOS transistor which is used to charge the dynamic node in the precharge phase is also used as a conditional keeper in the evaluation phase. The keeper functionality is merged in precharge PMOS. It is found that at same DC noise robustness; this technique gives 9% improvement in delay, 14% improvement in power and 18% improvement in clock load compared to conditional keeper technique. Further, this technique gives zero delay penalties but higher noise immunity compared to conventional dynamic circuits.

## Introduction

Wide dynamic circuits are used for high performance digital applications. However, a dynamic circuit has poor noise tolerance compared to its static counterpart. To improve the noise immunity, weak keeper transistors are used to pull-up the floating dynamic node. Due to process variations keeper transistor need to be upsized to maintain the required DC noise robustness. However, increased keeper size affects the performance of the circuit at slow NMOS corners. Conditional keepers are used to improve the noise immunity of wide dynamic circuits [1]. In the evaluation phase, stronger keeper is conditionally used by monitoring the dynamic node voltage (Fig.1). Though conditional keeper achieves improved noise immunity compared to the conventional keeper, it adds extra capacitance at the dynamic node increasing the delay. In this work, we propose multiplexed keeper technique which gives lower delay, lower power dissipation and lower clock load compared to conditional keeper technique.

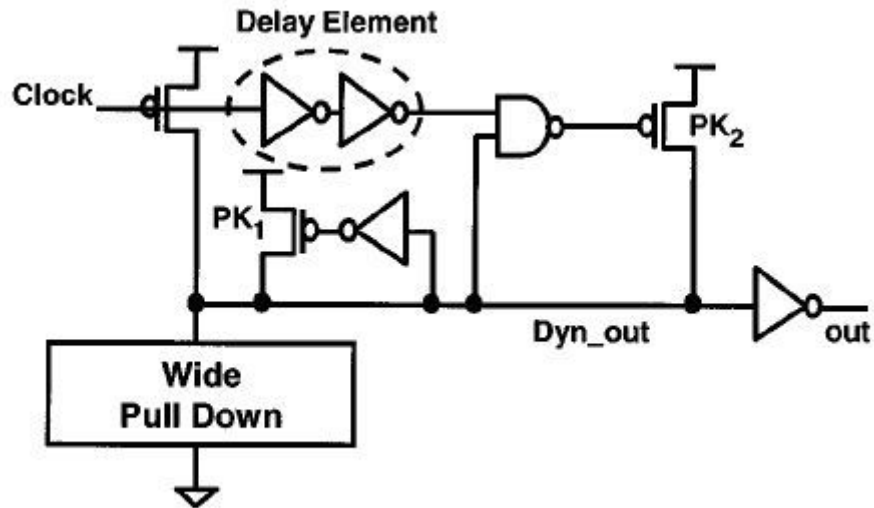


Figure 1: Conditional Keeper Technique

## Multiplexed Keeper Technique

Conceptually, PMOS functionality is multiplexed as a precharge transistor in the precharge phase and as a conditional keeper in evaluation phase. (Fig.2). Clock and delayed inverted clock signals act as control signals for the multiplexer. During precharge phase, PMOS, P1 acts as a precharge transistor and in evaluation phase, same PMOS, P1 acts as a conditional keeper.

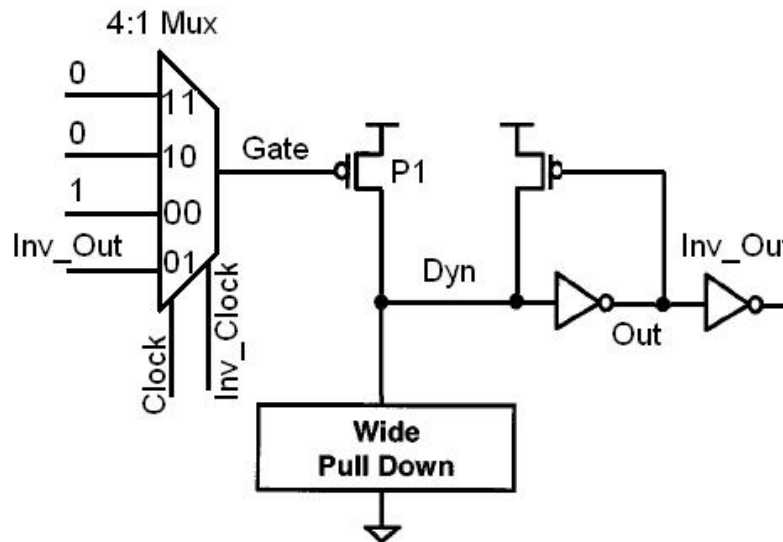


Figure 2: Conceptual Multiplexed Keeper

Fig.3 shows the circuit diagram for the proposed multiplexed keeper technique. When Clock is high, NAND gate is disabled. 'Gate' node is pulled down precharging 'Dyn' and 'Inv\_out' nodes to  $V_{DD}$ .

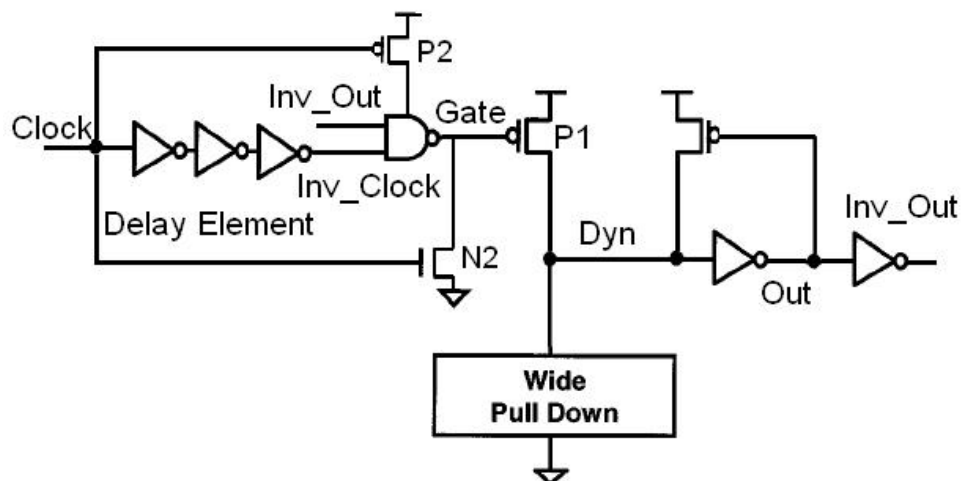


Figure 3: Multiplexed Keeper Circuit

As soon as clock goes low, NAND is enabled. 'Inv\_clock' signal continues to remain low for the time governed by the delay element. During this time, 'gate' node is pulled high and PMOS, P1 is cutoff. At the same time 'Dyn' node is either discharged to ground or stays at  $V_{DD}$  depending on the PDN logic. If 'Dyn' gets evaluated as low, 'Inv\_out' signal also goes low. The output of the NAND gate still remains high and PMOS, P1 continues to be in cutoff for the remaining period of the evaluation phase. In this case, PMOS, P1 acts as conditionally OFF keeper (Fig.4). However, if 'Dyn' node remains high, 'Inv\_out' signal also stays at high, and NAND output is pulled low after the 3 inverter delays. In this case, PMOS, P1 is turned ON for the remaining portion of the evaluation phase. Here, it acts as conditionally ON keeper (Fig.4).

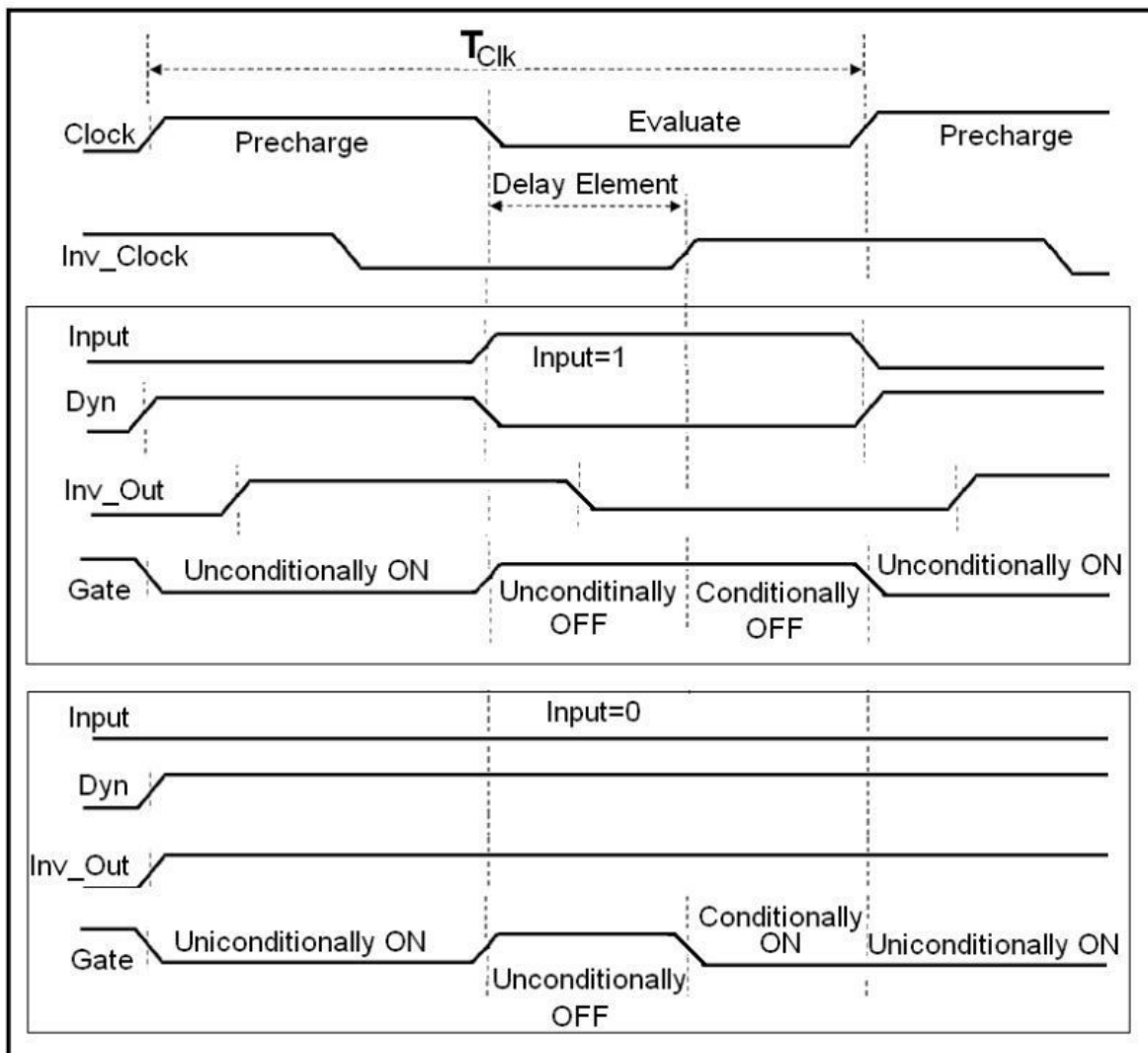


Figure 4: Multiplexed Keeper Timing Diagram

## Simulation Results

HSPICE simulations for 16-input wide OR gate are done using 130nm, 1.2V  $V_{DD}$  logic process technology. Two identical designs featuring conditional keeper and multiplexed keeper are compared for the power and performance. The conditional keeper size is kept same as the precharge PMOS in order to have same DC noise robustness. Table 1 shows the comparison between two techniques. Conditional keeper incurs delay penalty due to increased load at dynamic node. Extra capacitance at dynamic node is drain diffusion capacitance of the conditional keeper and input gate capacitances of NAND gate. In the proposed technique, there is no extra load at dynamic node. It is found that multiplexed keeper technique gives 9% lower delays compared to conditional keeper technique (Fig. 5).

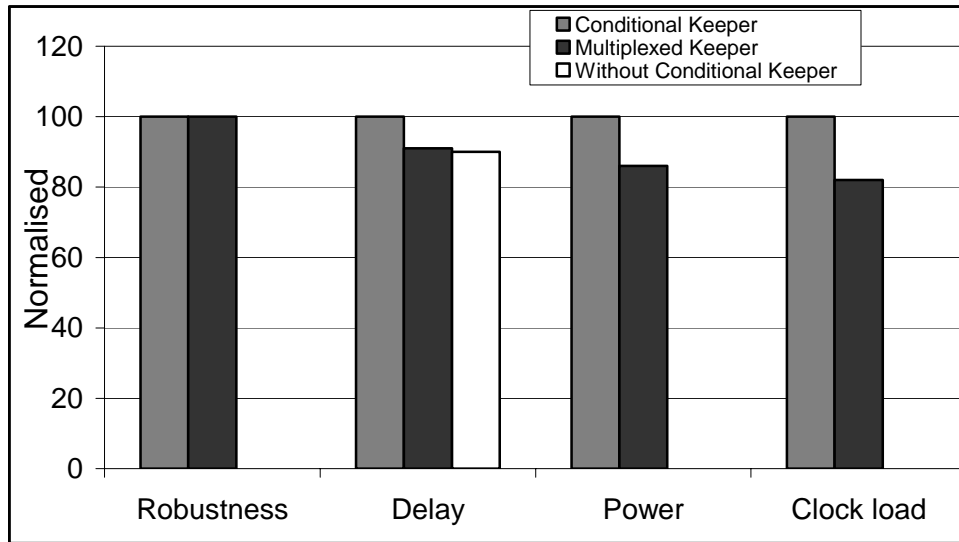


Figure 5 : 130nm Technology, Conditional Keeper Vs Multiplexed Keeper

Also, this technique is compared with conventional domino circuit without any conditional keeper (so that dynamic node capacitance is same in both cases). It is found that this approach gives virtually zero delay penalties but improved DC noise robustness compared to the conventional one. Due to reduced capacitance at dynamic node, power consumption is reduced by 14 % in multiplexed keeper technique (Fig. 5). Minimum sized inverters are used for delay element and generating inverted output. Extra inverters tend to offset the improvement in power at lower switching activity (Fig.6). It is found that for switching activities below 0.4, multiplexed keeper consumes more power.

However, in wide OR circuits, even though switching probability of the individual input can be low, overall switching activity of the dynamic node is pretty high. In this technique, clock signal drives an inverter unlike the precharge transistor in conditional keeper technique. The inverter (P2-N2) is downsized to meet the required timing constraints thus lowering the clock load by as much as 18 % (Fig 6). This technique is also verified in 70nm Berkeley Predictive Technology (BPTM) [2]. It is found that delay improvement in multiplexed keeper is marginal (Fig. 7). However, we still achieve 20 % improvement in power dissipation (Fig. 8). Note that, inverted output is not available in conditional keeper circuit. In this approach, ‘Gate’ node can be used as output of wide OR gate. Further, this technique can be used for Burn-In similar to conditional keeper technique by adding Burn-In control signal in the multiplexer [1].

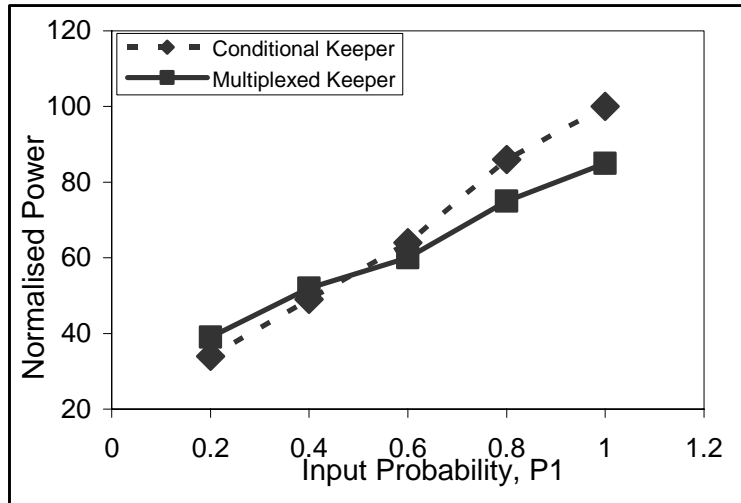


Figure 6: 130nm Technology, Power Dissipation

Parameter	Conditional Keeper	Multiplexed Keeper
Extra Transistors	9	14
Dynamic node extra capacitance	Yes	None
Delay penalty	Yes	Zero
Clock Load	Precharge Transistor + 1 Inverter	2 Inverters
Power	1.0	<1.0 at higher switching probability
Area	1.0	>= 1 due to extra inverters
Inverted output	No	Yes
Burn-In	Can be used	Can be used

Table 1: Comparison between conditional keeper and multiplexed keeper technique.



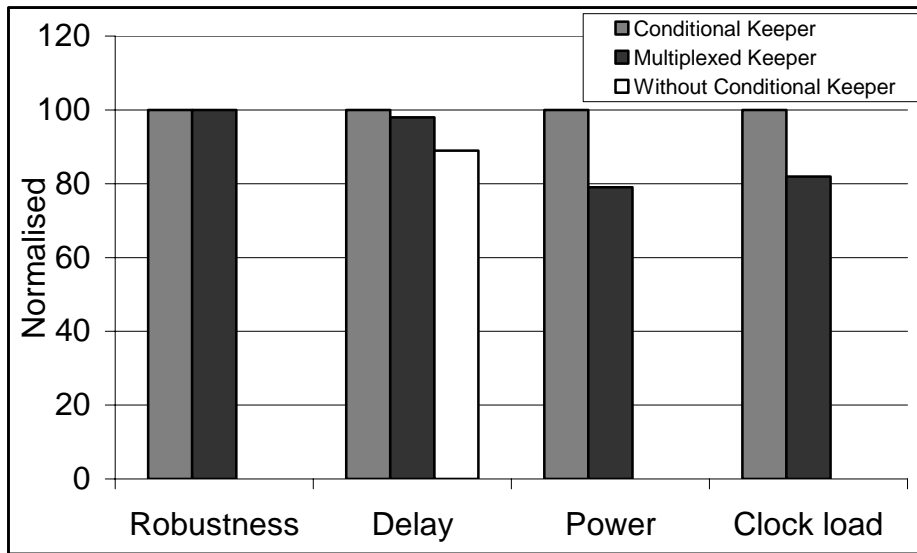


Fig.7: 70nm BPTM, Conditional Keeper Vs Multiplexed Keeper

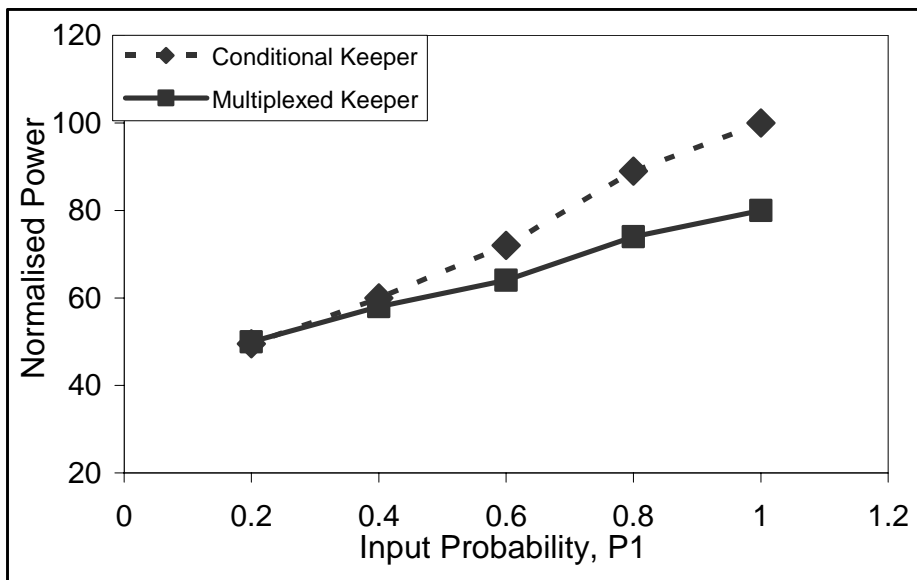


Fig.8: 70nm BPTM, Power Dissipation.

## Conclusions

A multiplexed keeper technique is proposed that gives zero delay penalty, but improved noise immunity compared to conventional dynamic circuits. At same DC noise robustness, it gives lower delay, lower power consumption and lower clock load compared to conditional keeper technique.

## References

- [1] A. Alvandpour, *et.al* "A sub-130-nm conditional keeper technique," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 633–638, May 2002.
- [2] UC Berkeley Predictive Technology: <http://www.eas.asu.edu/~ptm/>