September 2007

Indium selenide nanowire phase-change memory

Bin Yu
NASA Ames Research Center

Sanghyun Ju
Purdue University

Xuhui Sun
NASA Ames Research Center

Garrick Ng
NASA Ames Research Center

Thuc D. Nguyen
NASA Ames Research Center

See next page for additional authors

Indium selenide nanowire phase-change memory

Bin Yu[a),b)]
NASA Ames Research Center, Moffett Field, California 94035, USA

Sanghyun Ju
Birck Nanotechnology Center, School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, USA

Xuhui Sun,[a),c)] Garrick Ng, Thuc Dinh Nguyen, and M. Meyyappan
NASA Ames Research Center, Moffett Field, California 94035, USA

David B. Janes
Birck Nanotechnology Center, School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, USA

(Received 12 August 2007; accepted 12 September 2007; published online 28 September 2007)

Nonvolatile memory device using indium selenide nanowire as programmable resistive element was fabricated and its resistive switching property was studied as functions of electrical pulse width and voltage magnitude. The nanowire memory can be repeatedly switched between high-resistance ($\sim 10^{11}\ \Omega$) and low-resistance ($\sim 6\times 10^{5}\ \Omega$) states which are attributed to amorphous and crystalline states, respectively. Once set to a specific state, the nanowire resistance is stable as measured at voltages up to 2 V. This observation suggests that the nanowire can be programed into two distinct states with a large on-off resistance ratio of $\sim 10^{5}$ with significant potential for nonvolatile information storage. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2793505]

The concept of using material phase change of certain chalcogenides for information storage was introduced by Ovshinsky[1] in 1968. Resistive switching phase-change random access memory (PRAM) features faster write/read, improved endurance, and simpler fabrication, compared to conventional transistor-based nonvolatile memories. Nevertheless, progress has been slow with the use of thin-film phase-change materials (PCMs) such as $Ge_2Sb_2Te_5$, due to high programing current and intercell thermal interference that prevent memory scaling down. More recently, the possibility of growing PCMs in the form of nanowires[2–7] promises the potential of PRAMs to be realized in the future, thus renewing interest in this area. The use of PCM nanowires instead of thin films reduces the programmable cell volume which, combined with a reduction in melting point of nanoscale materials, is expected to reduce the programing current. Indeed, demonstrations of reduction in melting point[5,6] as well as programming current[3,4] have been reported recently for both GeTe (GT) and $Ge_2Sb_2Te_5$ (GST). Among PCMs, In_2Se_3 is more promising since it exhibits four orders of magnitude higher resistivity than GT or GST and its resistivity can be varied by a factor of 10^5, depending on the degree of crystallization.[3,4] Highly resistive PCMs help to reduce the programing current in PRAM switching. Here, we report resistive switching results for In_2Se_3 nanowire-based PRAM.

Our approach to grow In_2Se_3 nanowires has been described previously.[7] The growth follows a vapor-liquid-solid mechanism in a physical vapor deposition system. Figure 1 shows a typical transmission electron microscopy (TEM) image of an In_2Se_3 nanowire. The nanowires have a diameter of 60–120 nm and are up to 100 μm in length. The selected area electron diffraction (SAED) pattern shows regular spot patterns, confirming the single crystalline nature of the nanowire. The memory devices were fabricated by transferring the nanowires onto a SiO_2-coated silicon substrate with a prepatterned molybdenum (Mo) pad array prepared by optical lithography. Focused ion beam technique was used to directly write 150-nm-thick Pt interconnect lines between the nanowire and Mo probing pads. A Ga ion beam (30 kV and 30 pA) was used to decompose the organometallic Pt precursor (trimethyl-methylcyclopentadienyl-platinum) to form metallic Pt. The scanning electron microscope image of the fabricated memory device is shown in Fig. 1(b). The diameter and length of the In_2Se_3 nanowire between the two Pt lines are 50 nm and 7 μm, respectively. The current-voltage (*I-V*) and resistance-voltage (*R-V*) characteristics were measured using a probe station with a HP4156A semiconductor parameter analyzer. The voltage pulses for set and reset operations were generated by an Agilent 33250A pulse generator.

To explore the resistive switching behavior, the In_2Se_3 nanowire device was subjected to a series of individual voltage pulses of constant width and varying magnitude, and the device resistance was measured at 0.2 V after each pulse. The devices were initially in a low-resistance state (LRS); for the representative device described in Fig. 2, the initial resistance was $\sim 4.4\times 10^{5}\ \Omega$. Starting with the device initially in the LRS [Fig. 2(a)], pulses with 20 ns fixed width and very sharp fall-down edge (3 ns) were applied. The resistance was stable for pulse voltages up to 4.5 V, then began increasing with increasing voltage until reaching a high-resistance state (HRS) of $\sim 10^{11}\ \Omega$ for a 7 V pulse. For the case in which the device was initially in the HRS [Fig. 2(b)], pulses with 100 μs fixed width were applied. In this case, the nanowire resistance was stable for pulse voltages up to 4.5 V, then dropped to a LRS of $\sim 6\times 10^{5}\ \Omega$ for a pulse of 5 V. The two identified turning points represent the memory

[a)]Authors to whom correspondence should be addressed.
[b)]Electronic mail: byu@arc.nasa.gov
[c)]Electronic mail: xsun@arc.nasa.gov

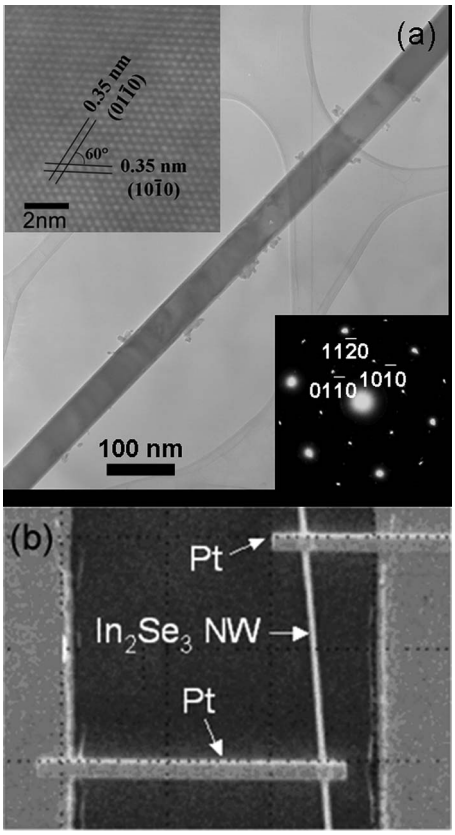

FIG. 1. (a) TEM image of an In_2Se_3 nanowire grown on SiO_2 substrate using 20 nm gold nanoparticles as catalyst. Top left inset shows the nanowire crystalline lattice structure and bottom right inset shows the SAED pattern. (b) Top view of the fabricated In_2Se_3 nanowire memory device. Pt interconnection lines were deposited by focused ion beam, linking the In_2Se_3 nanowire with prepatterned Mo probing pads.

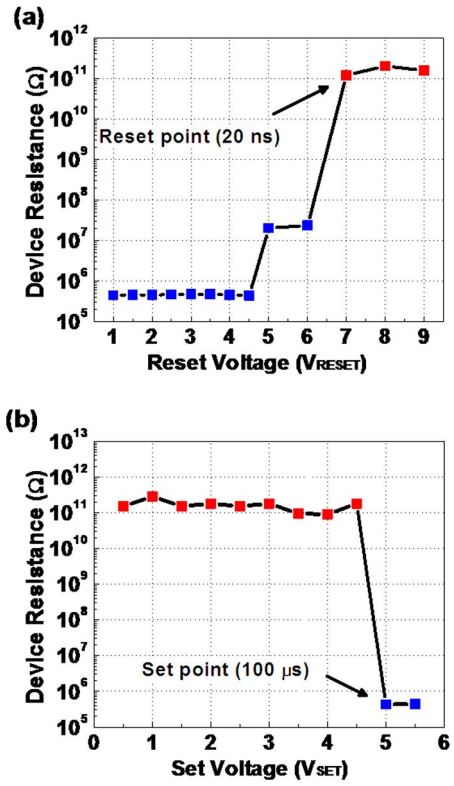

FIG. 2. Resistance of In_2Se_3 nanowire memory (measured at a small read voltage of 0.2 V) as a function of applied voltage in a pulse-mode test. (a) Switching from low-resistance state to high-resistance state with a fixed pulse width of 20 ns. The reset starts to occur at 7 V. (b) Switching from high-resistance state to low-resistance state with a fixed pulse width of 100 μs. The set starts to occur at 5 V.

reset (from LRS to HRS) and set (from HRS to LRS) conditions.

Once the nanowire is set to a specific resistive state, its resistance is stable and the storage of data, represented by the resistance value, is nonvolatile. Figure 3 shows the *I-V* and *R-V* characteristics of the device in either high- or low-resistance states with successive measurement sweeps. The device exhibits stable resistive behavior over the voltage range of 0–2 V. The dynamic switching ratio (on-to-off resistance) is about 10^5, which is sufficiently large for nonvolatile memory applications.

Figure 4 illustrates the measured nanowire memory resistance for successive programing cycles, in which the device is alternately set to LRS and reset back to HRS. For this study, the device was set to LRS using a 100 μs/5 V pulse, and reset to HRS using a 20 ns/7 V pulse. As shown, the repeatable memory switching between the high- and low-resistance states is clearly observed, although some variation in the measured data is observed among testing cycles.

The presence of high- and low-resistance states, as well as the qualitative nature of the electrical pulse-induced resistive switching behavior, are similar to prior reports of phase-change memories using thin-film In_2Se_3 material,[8] and GT or GST nanowires.[3,4] The phase of the nanowire can be reversibly switched between crystalline and amorphous through a current induced joule heating process, resulting in the change of electrical resistance. By applying a high and short pulse, the nanowire can be rapidly heated up to its melting point and then quickly quenched. Thus, the nanowire switches to

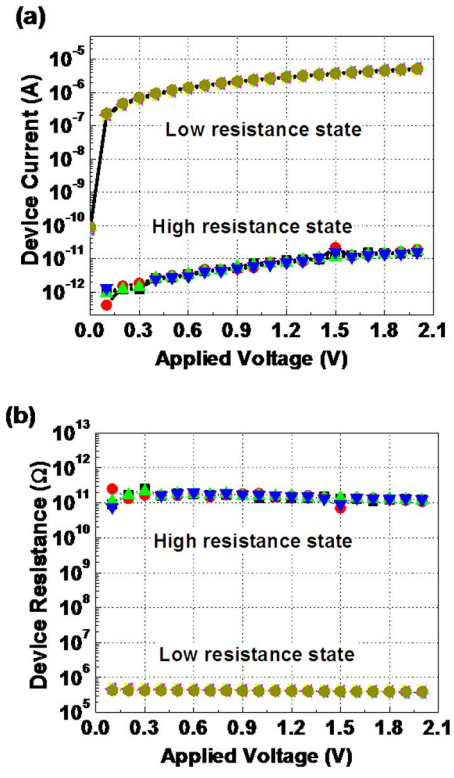

FIG. 3. (a) Measured *I-V* characteristics and (b) *R-V* characteristics of In_2Se_3 nanowire memory, both plots showing four successive testing sweeps after nanowire was either set to low-resistance state or reset to high-resistance state.

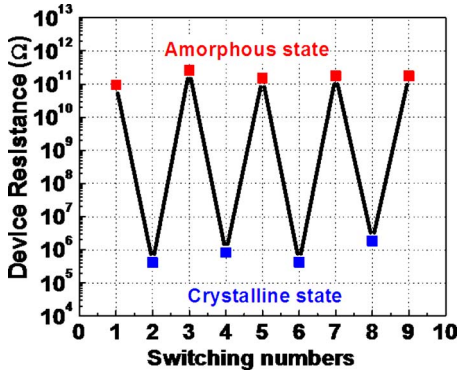

FIG. 4. Measured In_2Se_3 nanowire device resistance for a series of high and low resistance states after repeated reset-set programing cycles. Device was switched from LRS to HRS using a 7 V/20 ns reset pulse (with 2 ns sharp fall-down edge), and from HRS to LRS using a 5 V/100 μs set pulse.

an amorphous phase (high resistance). By applying a low and relatively long pulse, the nanowire is heated up to below its melting point and recrystallizes spontaneously back to a crystalline phase through annealing (low resistance). It is observed that the dynamic resistive switching ratio for In_2Se_3 nanowire ($\sim 10^5$) is much larger than that reported for thin-film In_2Se_3 devices ($\sim 10^3$) as well as for other nanowire devices (10^3 and 10^2 for GT and GST nanowires, respectively). Since In_2Se_3 is a single-phase binary compound, it is relatively easy to convert between crystalline and amorphous states, compared with other complex compounds such as $Ge_2Sb_2Te_5$. It should be also noted that an intermediate resistive level ($\sim 2 \times 10^7\ \Omega$) was reached at a resetting voltage of 5–6 V, as shown in Fig. 2(a), which could possibly associated with a secondary metastable phase other than the as-synthesized β-In_2Se_3 phase.[9]

Compared with thin-film memory, In_2Se_3 nanowire has much larger resistance in each corresponding material phase (factors of 10^2 for LRS and 10^6 for HRS), which results in more effective delivery of the programing energy. Consider the energy input during memory switching. For the reset operation, the nanowire self-heating power, given by V^2/R, is about 80 μW at 7 V. This corresponds to a total input energy of 1.6 pJ for the 20 ns pulse duration. For the set operation, the power is about 0.25 nW at 5 V, and the total input energy is 25 fJ for the 100 μs pulse duration. In the case of thin-film In_2Se_3 memory,[8] the corresponding self-heating power/energy in the reset and set operations are 16 mW/1.12 nJ and 14 μW/140 pJ, respectively. Obviously, the nanowire memory uses orders of magnitude lower input power and energy to switch between the two material phases. The results here are more favorable than GT and GST nanowires[3,4] as well, which are at milliwatt levels.

Based on typical thermal conductivities of semiconductor materials and the physical dimensions of the nanowire, it is estimated that the nanowire structures (crystalline phase) have thermal resistances on the order of 10^7 °C/W. Assuming that a static condition is reached within the pulse period, this would yield an estimated maximum temperature due to self-heating of approximately 800 °C for the reset operation at 7 V, close to the bulk In_2Se_3 melting point (890 °C). Note that a reduction in melting point has been reported for In_2Se_3 (Ref. 7) and other PCM nanowires,[5,6] which could further reduce the input energy for reset operation. Also, the thermal conductivity of the nanowire typically decreases due to low dimensionality,[10] which promotes self-heating effect by suppressing thermal dissipation along the nanowire. These two phenomena, showing strong size dependency, could lead to a nonvolatile memory design with lower input energy by employing smaller-diameter phase-change nanowires. Indeed, one order of magnitude reduction in reset current has been shown possible by reducing the GT nanowire size from 200 to 28 nm.[3]

In summary, we have demonstrated nonvolatile phase-change memory using In_2Se_3 nanowire as programmable element. A resistance switching ratio of 10^5 has been obtained and the nanowire memory reversibly switches at much reduced input power/energy compared with the reported In_2Se_3 thin-film memory. The power needs are also lower than those for GT and GST nanowire devices. The results indicate that In_2Se_3 nanowire can be an excellent candidate for applications in nonvolatile data storage. Moreover, phase-change nanowire memory potentially allows very-low-power information storage through physical geometry scaling.

This research work was supported by a NASA contract to UARC and URETI (NCC 2-1363). Two of the authors (G.N. and T.D.N.) are graduate students at SJSU, supported by NASA Ames Associate Program. The authors would like to thank Professor T. Fisher for helpful discussions.

[1] S. R. Ovshinsky, Phys. Rev. Lett. **21**, 1450 (1968).
[2] S. Meister, H. L. Peng, K. McIlwrath, K. Jarausch, X. F. Zhang, and Y. Cui, Nano Lett. **6**, 1514 (2006).
[3] S. H. Lee, D. K. Ko, Y. Jung, and R. Agarwal, Appl. Phys. Lett. **89**, 223116 (2006).
[4] Y. Jung, S.-H. Lee, D.-K. Ko, and R. Agarwal, J. Am. Chem. Soc. **128**, 14026 (2006).
[5] X. H. Sun, G. Ng, M. Meyyappan, and B. Yu, J. Phys. Chem. C. **111**, 2421 (2007).
[6] X. H. Sun, B. Yu, and M. Meyyappan, Appl. Phys. Lett. **90**, 183116 (2007).
[7] X. H. Sun, B. Yu, G. Ng, T. Nguyen, and M. Meyyappan, Appl. Phys. Lett. **89**, 233121 (2006).
[8] H. Lee and Y. Kim, IEEE Trans. Magn. **41**, 1034 (2005).
[9] H. Okamoto, J. Phase Equilib. Diff. **25**, 201 (2004).
[10] S. G. Volz and G. Chen, Appl. Phys. Lett. **75**, 2056 (1999).