5-1-2007

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N-Type Field-Effect Transistors Using Multiple Mg-Doped ZnO Nanorods

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***Abstract*—Nanorod field-effect transistors (FETs) that use multiple Mg-doped ZnO nanorods and a SiO_2 gate insulator were fabricated and characterized. The use of multiple nanorods provides higher on-currents without significant degradation in threshold voltage shift and subthreshold slopes. It has been observed that the on-currents of the multiple ZnO nanorod FETs increase approximately linearly with the number of nanorods, with on-currents of $\sim$ 1 μA per nanorod and little change in off-current ($\sim 4 \times 10^{-12}$). The subthreshold slopes and on–off ratios typically improve as the number of nanorods within the device channel is increased, reflecting good uniformity of properties from nanorod to nanorod. It is expected that Mg dopants contribute to high n-type semiconductor characteristics during ZnO nanorod growth. For comparison, nonintentionally doped ZnO nanorod FETs are fabricated, and show low conductivity to compare with Mg-doped ZnO nanorods. In addition, temperature-dependent current–voltage characteristics of single ZnO nanorod FETs indicate that the activation energy of the drain current is very low (0.05–0.16 eV) at gate voltages both above and below threshold.**

***Index Terms*—Multiple, nanorod, transistor, ZnO.**

I. Introduction

TRANSISTORS composed of nanobundles of single-wall carbon nanotubes (SW-CNTs) [1]–[5] or silicon nanowires (Si-NWs) as active materials have been the focus of intense research as a higher performance alternative to a-Si thin film transistors (TFTs) and poly-Si TFTs [6] with possible applications in microelectronic display devices, electron transport media for solar cells, chemical sensors, light-emitting diodes, and laser diodes [7]–[11]. Nanowires have electrical and mechanical merits, physical flexibility, and transparency. One promising candidate that satisfies these requirements is ZnO nanowire field-effect transistors (FETs) or ZnO nanorod FETs because ZnO is a transparent material and nanowires are known to have inherent flexibility. Wurtzite structure ZnO is one of the most important II–VI group semiconductors with a direct and wide bandgap of 3.37 eV, large exciton binding energy of 60 meV (28 meV for GaN), and high optical gain of 300 cm^{-1} (100 cm^{-1} GaN) at room temperature [12]–[14]. It is of interest for low-voltage and short wavelength (green or green/blue) electrooptical devices such as light emitting diodes and laser diodes. It also can be widely used as transparent ultraviolet (UV) protection films, transparent conducting oxide materials, piezoelectric materials, electron-transport medium for solar cells, chemical sensors, photocatalysts, and so on [11]–[15]. Since the first report of ZnO nanowires in 2000 [17], a great deal of attention has been focused on the study of 1-D ZnO nanomaterials such as nanowires [12], [16]–[18] or nanorods [19]–[23] for their great prospects in fundamental physical science, novel nanotechnological applications, and significant potential for nanooptoelectronics. Nano-ZnO has been described as the next most important nanomaterial after carbon nanotubes [24].

In light of the limited current drive per nanowire, significant issues for nanowire transistor devices include how to obtain relatively large levels of on-current and how to adjust the drive current capability of various devices. Low voltage operation and low power consumption are required in order to replace technologies such as a-Si TFTs and poly-Si TFTs which are mainly used to thin-film transistor liquid crystal display (TFT-LCD) devices or active matrix organic light-emitting diode (AMOLED) display devices. The mobility and gating efficiency clearly play a key role in maximizing the drive capability per nanowire. In order to achieve the drive current levels required for applications such as microwave circuits or display drivers, it will be necessary to develop approaches in which a number of nanowires can be integrated within a single device. There are a number of issues that must be addressed in order to maintain high performance within multinanowire structures. Since wire-to-wire variations can degrade important performance metrics such as subthreshold slope and on–off ratios, it is important to develop and characterize multinanowire FETs in order to understand the performance characteristics that can be achieved.

In this study, we report the development of FET devices using multiple Mg-doped ZnO nanorods as the channel material and SiO_2 as the gate insulator. The on-current is observed to scale approximately linearly with the number of nanorods within a device. In addition, on–off ratios improve as the number of nanorods is increased without degrading the subthreshold slope and the threshold voltage, indicating good uniformity of nanorod electrical properties. Investigations of the temperature dependence of the current–voltage characteristics of the devices provide insights about the conduction mechanism.

Manuscript received August 31, 2006; revised January 11, 2007. This work was supported in part by the NASA Institute for Nanoelectronics and Computing under Grant NCC-2-1363. The review of this paper was arranged by Associate Editor C. Zhou.

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Digital Object Identifier 10.1109/TNANO.2007.893148

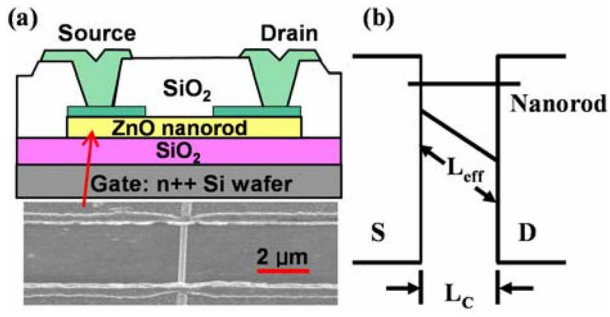

Fig. 1. (a) Cross-sectional view of SiO_2-based ZnO nanorod FET device structure, along with top-view scanning electron micrograph. (b) Top view schematic of the nanorod FET illustrating that the effective channel length of each nanorod depends on its orientation.

II. Experiment

The ZnO nanorods reported here were grown via a vapor transport method [25] in a horizontal fused quartz tube inside a tube furnace [25]. The raw material was a mixture of ZnO (99.999%, Alfa Aesar), graphite carbon powders (99.9995%, Alfa Aesar) and Mg_3N_2 (99.6%, Alfa Aesar). Graphite carbon powders were used to lower the vaporizing temperature of source material [26]. The substrates were catalyst-patterned polished amorphous silicon dioxide wafers treated as follows: First, polished amorphous silicon dioxide wafers (silicon wafers with 1 μm thick amorphous thermal oxide) were cleaned using piranha solution (1 : 3 conc. hydrogen peroxide; conc. H_2SO_4), and then the catalyst regions were physically written on the wafer surface by an iron rod coated with Ni $(NO_3)_2$ solution [26]. The raw material and the catalyst-patterned substrates were loaded into a fused quartz boat with a separation of 11–16 cm, and the boat was placed into the quartz tube, with the raw material located at the center (highest temperature zone) of the tube furnace. The furnace was heated under a steady flow of argon (ultrahigh purity, Airgas) of about 50 standard cubic centimeters per minute (sccm). When 930 °C was reached, the temperature was kept constant for 5–8 h. The furnace was then switched off and allowed to cool to room temperature quickly. A representative field emission scanning electron microscopy (FESEM, Hitachi S-4500 cFEG SEM) image of the as-grown ZnO nanorods reveals that the ZnO nanorods are uniform, with smooth surfaces, and diameters ranging from several tens of nanometers to 300 nm.

Mg-doped multiple ZnO nanorod FETs devices were fabricated on a 60 nm-thick thermally grown SiO_2 layer used as the gate insulator. A heavily doped n-type Si substrate ($\rho \sim 0.01$ Ω-cm) was used as a back gate. Fig. 1 shows the cross section of the SiO_2-based ZnO nanorod FET device. The ZnO nanorods were dispersed in very large scale integrated circuit (VLSI) grade 2-propanol, and transferred onto the SiO_2 gate insulator after completely cleaning the SiO_2 surface. The average diameter and length of ZnO nanorods in this study is 300 nm and 5 μm, respectively. Aluminum source/drain contacts (150 nm) were deposited by e-beam evaporation (deposition rate = 0.3 Å/s). Interdigitated source/drain electrodes were used to contact a number of nanorods in parallel within each device. Devices were observed with 1–22 nanorods in the channel region without overlap between the ZnO nanorods. The number of nanorods within a device was determined by imaging in a Hitachi S-4800 FESEM following electrical characterization. In order to protect the nanorods from H_2O, O_2, and N_2 ambient, the devices were passivated with SiO_2 (300 nm) before electrical characterization. Electrical measurements were performed using a Keithley 4200 semiconductor characterization system. Variable temperature measurements were performed in vacuum using a MMR variable temperature probe station. The temperature was swept from 300 K to 180 K with 25 K step.

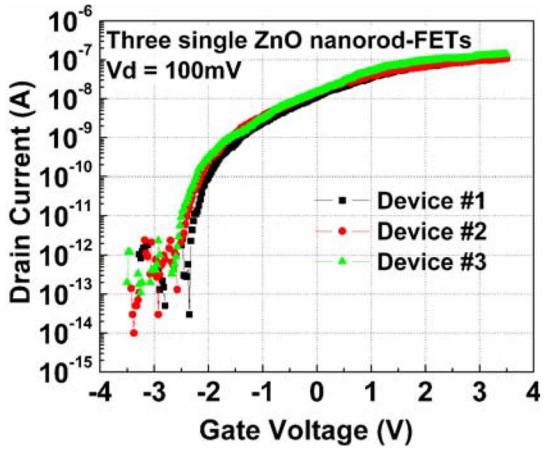

Fig. 2. Drain current versus gate-source voltage (I_{ds}-V_{gs}) for three single ZnO nanorod FETs.

III. Results and Discussion

The characteristics of FETs containing single nanorods were initially studied. Fig. 2 shows the measured drain current versus gate voltage characteristics for three FETs, each containing a single Mg-doped ZnO nanorod. The devices display drain current versus gate voltage (I_{ds}-V_{gs}) characteristics which are typical of n-type FETs. The substitution of O by Mg should result in acceptor doping, so the Mg-doped nanorods should yield p-channel conduction, or at least less efficient n-channel conduction. However, n-type conduction was observed in our study. It is possible that the Mg dopant may contribute to n-type semiconductor characteristics during ZnO nanorod growth [27]. It should also be noted that oxygen vacancies act as donors in ZnO, and may account for the n-channel behavior. For comparison, nonintentionally doped ZnO nanorod FETs have also been fabricated, and show low conductivity (∼1 nA at $V_{ds} = 1.2$ V, $V_{gs} = 3.0$ V) compared with Mg-doped ZnO nanorods. (∼ 0.6 μA at $V_{ds} = 1.2$ V, $V_{gs} = 3.0$ V).

In order to understand the conduction mechanisms in these devices, the temperature-dependent I_{ds}-V_{gs} and the drain current versus drain-source voltage (I_{ds}-V_{ds}) characteristics of a single ZnO nanorod FET were measured at temperatures ranging from 275 K to 200 K in 25 K steps and an Arrhenius plot (Fig. 3) was generated at $V_{ds} = 1$ V. The linear characteristic confirms the validity the relationship ($I \sim I_0 e^{-E/kT}$) between current and thermal energy. The extracted activation energies at three different gate biases ($V_{gs} = -1$, 0, and 1 V) are 0.16, 0.08, and 0.05 eV, respectively. The activation energy is very low (0.05 to 0.16 eV) at gate voltages both above and

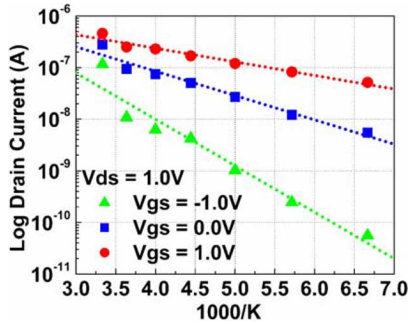

Fig. 3. Arrhenius plot of a single ZnO nanorod FET.

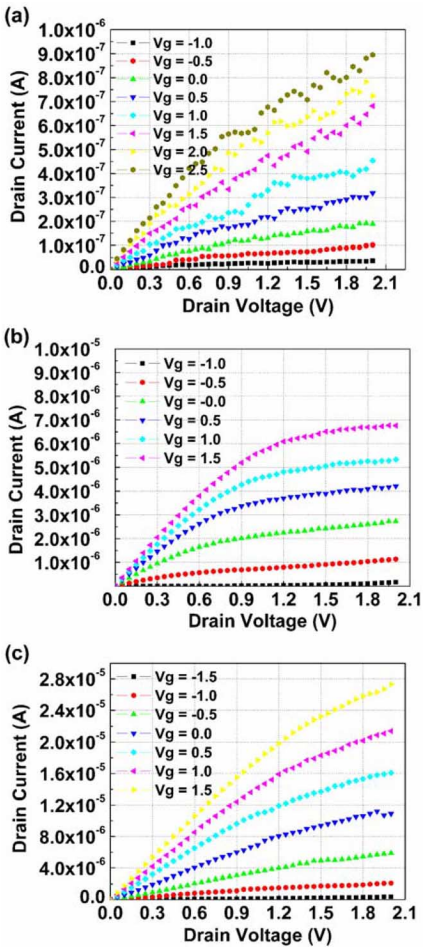

Fig. 4. Drain current versus drain-source voltage ($I_{\rm ds}$-$V_{\rm ds}$) characteristics ZnO nanorod FETs containing: (a) a single nanorod, (b) 9 nanorods, and (c) 20 nanorods.

below threshold. The electron affinity of ZnO, $\div_{\rm ZnO}$, is 4.29 eV, yielding an effective work function $\Phi_{\rm ZnO} = 4.45$ eV for moderately doped n-type material. Based on the work function of Al ($\Phi_{\rm Al} = 4.28$ eV), it is expected that aluminum source/drain contacts form relatively low barrier height interfaces to n-type ZnO. For a FET with low-barrier source/drain contacts, the electron barrier height (Φ_B) should be small in the "on" region, and positive gate bias should decrease Φ_B, whereas negative gate bias should increase Φ_B. These trends are consistent with the trends in extracted activation energy values.

The $I_{\rm ds}$-$V_{\rm ds}$ characteristics of representative multiple SiO_2-based ZnO nanorod FETs ($L \sim 2.2$ μm) are shown in

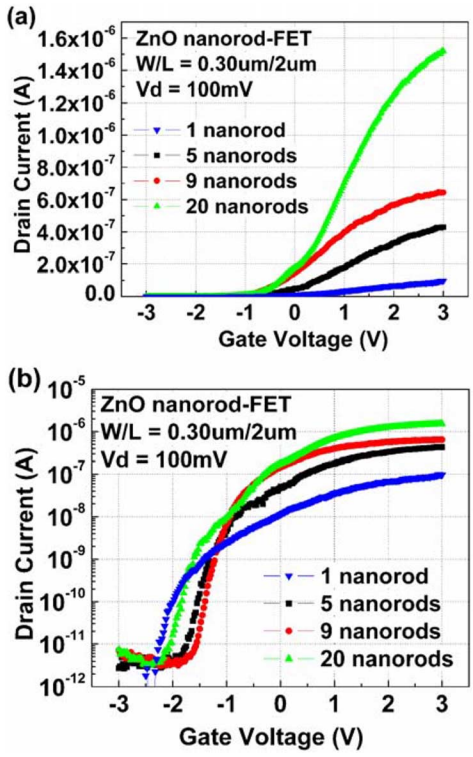

Fig. 5. Drain current versus gate-source voltage ($I_{\rm ds}$-$V_{\rm ds}$) for ZnO nanorod FETs with indicated number of nanorods. (1, 5, 9, and 20 nanorods). (a) linear-scale drain current. (b) Log-scale drain current.

Fig. 4(a)–(c). For the single-nanorod device [Fig. 4(a)], the on-current is ~ 0.6 μA at $V_{\rm ds} = 1.2$ V, $V_{\rm gs} = 3.0$ V. The 9-nanorod device [Fig. 4(b)] and 20-nanorod device [Fig. 4(c)] show on-currents of $\sim$7.0 μA (at $V_{\rm ds} = 1.8$ V, $V_{\rm gs} = 1.5$ V) and $\sim$ 20.0 μA (at $V_{\rm ds} = 1.8$ V, $V_{\rm gs} = 1.5$ V), respectively. The devices exhibit typical long-channel FET behavior, with clear saturation in the drain current, and do not reflect behavior associated with contact resistance limited current.

Fig. 5 shows the $I_{\rm ds}$-$V_{\rm gs}$ characteristics for representative single and multiple ZnO nanorod FET devices, with the current axis shown on a linear scale in Fig. 5(a) and a log scale in Fig. 5(b). SiO_2-based ZnO nanorod FETs composed of 1, 5, 9, and 20 nanorods exhibited on-currents at $V_{\rm gs} = 3$ V of 0.094, 0.43, 0.64, and 1.8 μA, respectively. The measured off-currents of the devices remain around $\sim 4 \times 10^{-12}$ A which is found to be approximately constant for various devices and is a lower limit of the current measurement apparatus, yielding on–off ratios varying from $\sim 10^4$ for the single-nanorod device to $\sim 10^6$ for the device with 20 nanorods. The devices with 1, 5, 9, and 20 nanorods have field-effect mobilities ($\mu_{\rm eff}$) of 12, 14, 11, and 13 cm^2/V-s, and subthreshold slopes of 900, 300, 250, and 300 mV/dec. The $\mu_{\rm eff}$ values are calculated using the capacitance estimated using the cylinder over plate model, multiplied by the number of nanowires in a given device. The observation that the subthreshold slope does not degrade with increasing number of nanorods, along with the scaling of on-currents, indicates good uniformity of device properties from nanorod to nanorod. Specifically, variations in threshold voltage would be expected to smear out the near-threshold

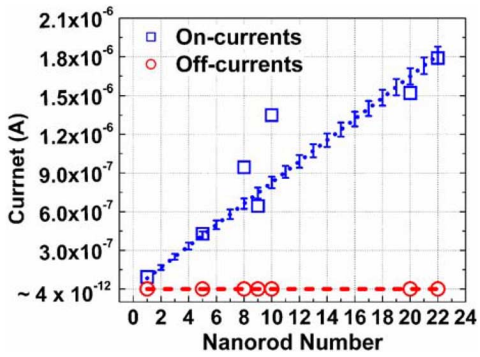

Fig. 6. Measured on-current and off-current of nanorod transistors versus number of nanorods (1, 5, 8, 9, 10, 20, and 22 nanorods). Dashed lines for on-current is a result of theoretical calculations [28] and the error bar is corresponding theoretical prediction of the variation in current purely based on random nanorod orientations, but there could be some more effects causing additional variation in current.

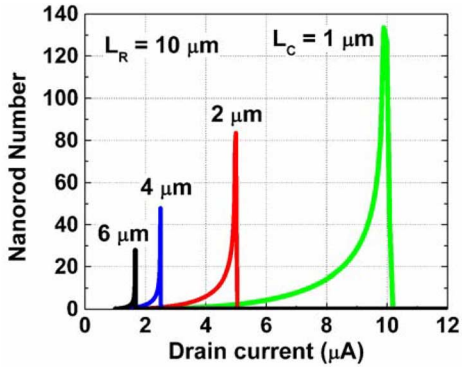

Fig. 7. Simulated number of nanorods versus drain current for nanorod length of LR $= 10\ \mu$m and channel length of LC $= 1, 2, 4, 6\ \mu$m. The drain current is inversely proportional to nanorod length. The variation of current for any given channel length is purely due to the different orientations of the nanorods with respect to channel axis.

characteristics, resulting in a poorer subthreshold slope. In addition, significant variations in threshold voltage from nanorod to nanorod would result in different effective gate potentials in each wire, which would yield on-currents that did not scale with the number of nanorods. The threshold voltages of the devices using 5 nanorods, 9 nanorods, and 20 nanorods are comparable ($V_{\rm th} \sim -0.5$ V). The transfer curve of the single nanorod transistor is not a scaled version of the transfer curves for the transistors containing 5, 9, and 20 nanorods; this may be due to the effects of defects or interface traps. Furthermore, the interface traps present at the gate oxide–nanorod interface degrade the device subthreshold slope [28], so we anticipate that the subthreshold characteristics can be improved further by modifications in processing conditions.

With these results, we can observe that the transistor characteristics improve as the number of nanorods is increased. These results indicate that multiple nanorod ZnO nanorod FETs can be used for devices which require high on-currents while maintaining high on–off ratios. Fig. 6 displays the measured on-currents and off-currents versus the number of nanorods (1, 5, 8, 9, 10, 20, and 22) within the device. The dashed line shows the result of theoretical calculations where the absolute value of current per unit length of tube is scaled to fit the experimental data. The theory shows that the on-currents of the devices scale approximately linearly with the number of nanorods, meaning that each wire contributes a comparable amount to the device conductance. The on-currents of the devices are observed to linearly increase with the number of nanorods, but the off-currents of the devices remain at approximately 4×10^{-12}. The reason that the on-current level is not exactly proportional to the number of nanorods can be associated with variations of conductivity and threshold voltage from nanorod to nanorod, or with possible high-resistance contacts to a fraction of the nanorods. Theoretically some variation is also introduced in the drain current by statistical variations in the orientation of the nanorods in the channel, as shown in Fig. 1(b). For a nanorod aligned to the channel axis (perpendicular to source/drain boundary), the effective channel length (the length intercepted by source/drain) is smaller and current is higher than a nanorod making an angle with the channel axis. Analytical calculations can be used to calculate an expected distribution for the number nanowires corresponding to a given current level, assuming that all the nanorods are randomly arranged on the substrate [29]. Fig. 7 shows the number of nanorods versus current for nanorod length of $L_R = 10\ \mu$m and various channel lengths. Note that the maximum current is inversely proportional to the channel length. Based on the relatively small variation in the drain current observed in this study, it appears that a large portion of the nanorods are oriented close to perpendicular to the channel [29, Fig. 7]. The figure shows that about $\sim 90\%$ of the nanorods that bridge source/drain are within $\sim 15\%$ of the maximum current. The error bar in the on-current of Fig. 6 shows the variation introduced by orientation for multiple nanorods.

The development of devices in which the on-current levels can be controlled by increasing the number of nanorods, while still maintaining good uniformity in subthreshold slope and off-currents, also provides the ability to realize transistors with varying current drive capabilities. Although the increments in on-current level for the nanorod transistors are discrete (corresponding to the integer number of nanorods), this control provides a capability comparable to width scaling of conventional transistors. The current devices are not optimized for high speed operation, but the development of devices with sufficiently low parasitic capacitances to allow GHz operation appears feasible.

IV. Conclusion

Mg-doped multiple ZnO nanorod FETs with SiO_2 as a gate insulator were demonstrated to achieve higher on-currents without significant degradation in on–off ratio, in threshold voltage shifts, or in subthreshold slopes. Mg doping provides more robust n-type conduction than is observed in nominally undoped devices. This is believed to correspond to the doping effects of Mg, which may induce a net donor density in spite of the fact that Mg substitution for O would result in acceptor doping. Increasing the number of nanorods significantly increased current level in ZnO nanorod FETs without sacrificing the low-voltage operation. These results indicate that the low on-current deficiencies of nanorod devices can be corrected

by using multiple ZnO nanorod FET devices. It demonstrates that multiple ZnO nanorod FETs can be adapted as driving transistors and switching transistors for display applications. In addition, current–voltage measurements at different temperatures (300 K–180 K, 25 K step) of SiO_2-based single ZnO nanorod FETs show low activation energies, reflecting low barrier injection from the contacts to the channel.

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