

Purdue University Purdue e-Pubs

Birck and NCN Publications

Birck Nanotechnology Center

June 2008

High performance In₂O₃ nanowire transistors using organic gate nanodielectrics

Sanghyun Ju

Department of Physics, Kyonggi University

Fumiaki Ishikawa

Department of Electrical Engineering, University of Southern California

Pochiang Chen

Department of Electrical Engineering, University of Southern California

Hsiao-Kang Chang

Department of Electrical Engineering, University of Southern California

Chongwu Zhou

Department of Electrical Engineering, University of Southern California

See next page for additional authors

Follow this and additional works at: <http://docs.lib.purdue.edu/nanopub>

Ju, Sanghyun; Ishikawa, Fumiaki; Chen, Pochiang; Chang, Hsiao-Kang; Zhou, Chongwu; Ha, Young-geun; Liu, Jun; Facchetti, Antonio; Marks, Tobin J.; and Janes, David B., "High performance In₂O₃ nanowire transistors using organic gate nanodielectrics" (2008). *Birck and NCN Publications*. Paper 155.
<http://docs.lib.purdue.edu/nanopub/155>

This document has been made available through Purdue e-Pubs, a service of the Purdue University Libraries. Please contact epubs@purdue.edu for additional information.

Authors

Sanghyun Ju, Fumiaki Ishikawa, Pochiang Chen, Hsiao-Kang Chang, Chongwu Zhou, Young-geun Ha, Jun Liu, Antonio Facchetti, Tobin J. Marks, and David B. Janes

High performance In_2O_3 nanowire transistors using organic gate nanodielectrics

Sanghyun Ju,¹ Fumiaki Ishikawa,² Pochiang Chen,² Hsiao-Kang Chang,² Chongwu Zhou,² Young-geun Ha,³ Jun Liu,³ Antonio Facchetti,³ Tobin J. Marks,³ and David B. Janes^{4,a)}

¹Department of Physics, Kyonggi University, Suwon, Kyonggi-Do 442-760, Republic of Korea

²Department of Electrical Engineering, University of Southern California, Los Angeles, California 90089, USA

³Department of Chemistry and the Materials Research Center, and the Institute for Nanoelectronics and Computing, Northwestern University, Evanston, Illinois 60208-3113, USA

⁴School of Electrical and Computer Engineering, and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, USA

(Received 20 December 2007; accepted 7 May 2008; published online 2 June 2008)

We report the fabrication of high performance nanowire transistors (NWTs) using In_2O_3 nanowires as the active channel and a self-assembled nanodielectric (SAND) as the gate insulator. The SAND-based single In_2O_3 NWTs are controlled by individually addressed gate electrodes. These devices exhibit *n*-type transistor characteristics with an on-current of $\sim 25 \mu\text{A}$ for a single In_2O_3 nanowire at $2.0V_{\text{ds}}$, $2.1V_{\text{gs}}$, a subthreshold slope of 0.2 V/decade, an on-off current ratio of 10^6 , and a field-effect mobility of $\sim 1450 \text{ cm}^2/\text{V s}$. These results demonstrate that SAND-based In_2O_3 NWTs are promising candidates for high performance nanoscale logic technologies. © 2008 American Institute of Physics. [DOI: 10.1063/1.2937111]

Recently, there have been several studies of nanowire transistors (NWTs) aimed at achieving high performance and reliable transistor response characteristics. One potential application of NWTs is to replace polysilicon (poly-Si) or amorphous-silicon (α -Si) thin-film transistors (TFTs) currently used in displays, sensors, solar cells, and other optoelectronic devices.¹⁻⁴ NWTs have several attractions versus poly-Si TFTs and α -Si TFTs, in terms of high mobility, optical transparency (for large band-gap nanowires), and mechanical flexibility. These characteristics could allow higher frequency TFT operation and enable flexible/transparent electronics. For instance, future light-emitting diode-based displays could be integrated with optically transparent windows and/or operate at far lower power by enhancing the pixel aperture ratio. The latter parameter can be increased, for a given pixel spacing, by either stacking transparent TFT layers or significantly reducing the area required for the drive transistor. However, consideration of the NW-based device performance metrics reported to date reveals that there is significant room for improvement before NWT-derived driving and switching elements can be assembled into useful electronic circuits. Among several possible semiconducting nanowire materials, In_2O_3 is one of the most promising because of its easy access, chemical stability, and wide band gap (3.6 eV).⁵⁻⁸ This combination of unique materials properties and the fundamental advantages of the quasi-one-dimensional nanowire electronic structure underscore the potential of In_2O_3 NWTs for advanced electronic applications requiring high transistor performance, optical transparency, and mechanical flexibility. In this study, we report significantly enhanced performance metrics for NWTs consisting of individual In_2O_3 nanowires as channels combined with a self-assembled organic nanodielectric⁹ (SAND) as the gate insulator. The present SAND-based In_2O_3 NWTs demon-

strate considerable advances in performance over previously reported NWTs employing In_2O_3 or other mid/wide bandgap NWTs, especially in terms of greatly improved field-effect mobility and high on-current densities.¹⁰⁻¹⁶

A cross-sectional view of the present NWT structure is shown in Fig. 1(a). Starting with a Corning 1737 glass substrate coated with a 500 nm SiO_2 buffer layer, individually addressable, transparent indium tin oxide (ITO) bottom-gate electrodes were deposited by ion-assisted deposition and photolithographically patterned. This individually addressable gate structure affords a high level of circuit integration

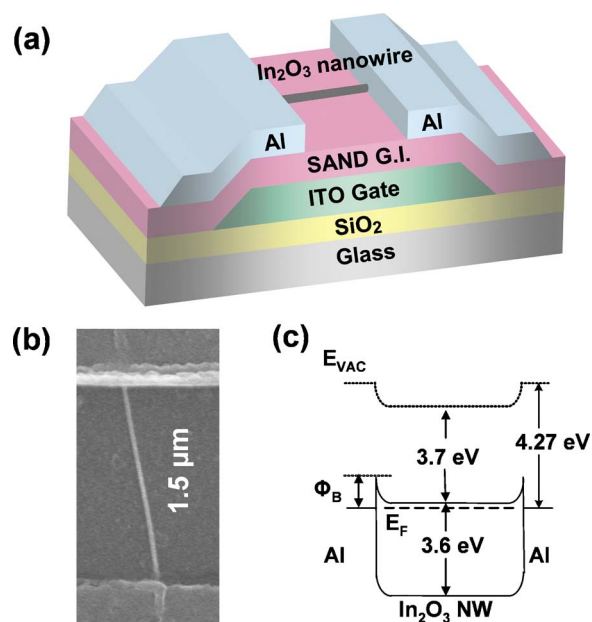


FIG. 1. (Color online) SAND-based In_2O_3 NWTs. (a) Cross-sectional view of the device structure. (b) Top-view FE-SEM images of the device region. Scale bar = 1.5 μm . (c) Source/nanowire/drain cross-section band diagram at $V_{\text{gs}}=0 \text{ V}$.

^{a)} Author to whom correspondence should be addressed. Electronic addresses: janest@ccn.purdue.edu and david.b.janes.1@purdue.edu.

using NWTs. The SAND gate dielectric (~ 15 nm) was then deposited using a layer-by-layer wet chemical process and provides a large capacitance of ~ 180 nF/cm² with an electric breakdown field of ~ 7 MV/cm. The conformal SAND provides excellent edge coverage, resulting in low interlayer leakage in the gate and source-drain overlap regions. This high performance gate dielectric allows the channel potential to be modulated at relatively low gate voltages. The In₂O₃ nanowires, which were synthesized via laser ablation,¹⁰ are not intentionally doped, but are believed to be lightly *n* type. The nanowires were suspended in isopropanol solution and then deposited onto the patterned substrates. Aluminum source/drain electrodes (~ 130 nm) were then deposited by electron-beam evaporation. Figure 1(b) shows a field-emission scanning electron (FE-SEM) micrograph of a single In₂O₃ nanowire confined between the source/drain electrodes. The diameter and length of the In₂O₃ nanowires are 20 nm and 1.5 μ m, respectively. The corresponding band diagram (source/NW/drain cross section for an aluminum contact structure) for a NWT at $V_{gs}=0$ V is shown in Fig. 1(c). The electron affinity of In₂O₃ ($\chi_{\text{In}_2\text{O}_3}$) is 3.7 eV, and the bulk Fermi level position for moderate doping is estimated to be $(E_e-E_f)=0.6$ eV, yielding an effective work function $\Phi_{\text{In}_2\text{O}_3}=4.54$ eV for *n*-type material. Al source/drain contacts ($\Phi_{\text{Al}}=4.28$ eV) are therefore expected to form relatively low interface barrier heights to *n*-type In₂O₃ NWs.

The present In₂O₃ NWTs exhibit excellent *n*-type transistor characteristics. All the NWT performance parameters reported here correspond to devices treated with ozone on the nanowire regions¹⁷ with O₂ plasma polishing on the source-drain contact region to maximize device performance. Figure 2(a) shows the drain current versus gate-source voltage ($I_{ds}-V_{gs}$) characteristics for a representative single In₂O₃ NWT, on both linear and semilog scales, as well as the measured field-effect mobility inferred from the transconductance (g_m) at the respective gate voltage. The device exhibits a subthreshold slope (S) of 0.2 V/decade, an on-off current ratio (I_{on}/I_{off}) of 10⁶, and a threshold voltage (V_{th}) of 0.0 V. The drain current versus drain-source voltage ($I_{ds}-V_{ds}$) characteristics of a representative NWT are shown in Fig. 2(b). These devices exhibit no evidence of saturation of the I_{ds} in the investigated potential bias range and exhibit an $I_{on} \sim 25$ μ A for the single In₂O₃ nanowire at $V_{ds}=2.0$ V, $V_{gs}=2.1$ V, respectively. Although a possible mechanism for the nonideal $I_{ds}-V_{ds}$ curve at high gate voltages might be ascribed to nanowire body leakage, in fact the measured leakage current through the SAND layer is only 30–40 pA at 4 V, indicating negligible leakage current through the gate dielectric. In order to allow direct comparison to other reported transistor performance data, including other NWTs, I_{on} can be expressed in terms of a current density of $\sim 8 \times 10^6$ A/cm², assuming uniform current flow throughout the nanowire cross section. The current per unit channel width is greater than 1 mA/ μ m, considering only the diameter of the nanowire. Importantly, this current level for a single nanowire is sufficient to drive a 176×54 μ m² size AMOLED pixel at 300 cd/m² in current-generation electroluminescent technologies.

The field-effect mobility is extracted from the measured g_m and the calculated gate-to-channel capacitance ($C_i = 2\pi\epsilon_0 k_{\text{eff}} L / \cosh^{-1}(1 + t_{ox}/r)$) using $\mu = dI_{ds}/dV_{gs} \times L^2/C_i \times 1/V_{ds}$, where the effective dielectric constant of

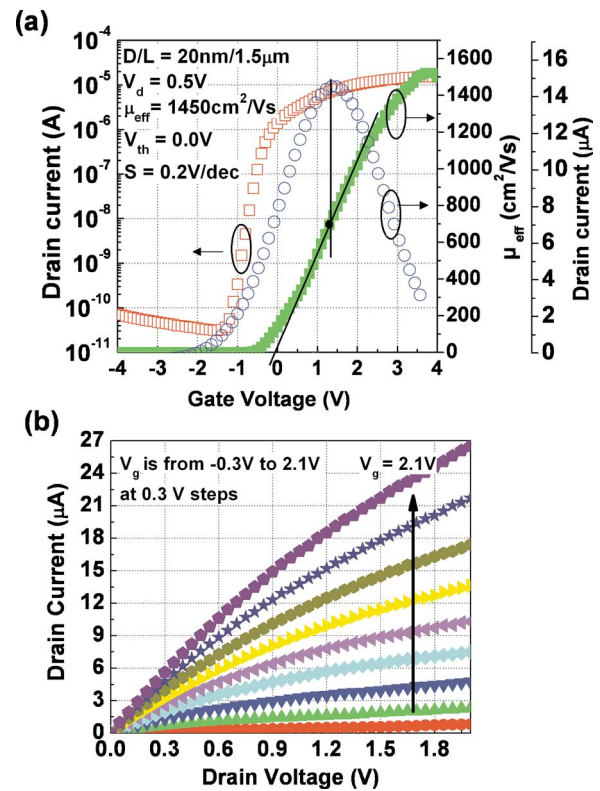


FIG. 2. (Color online) Measured characteristics of a representative SAND-based In₂O₃ NWT. (a) Drain current versus gate-source voltage ($I_{ds}-V_{gs}$) characteristics at $V_d=0.5$ V. Green, red, and blue data points correspond to linear-scale $I_{ds}-V_{gs}$, log-scale $I_{ds}-V_{gs}$, and mobility μ . (b) Drain current vs drain-source voltage ($I_{ds}-V_{ds}$) characteristics for various values of V_{gs} (-0.3 to 2.1 V in 0.3 V steps).

SAND (k_{eff}) is ~ 3.0 , the device channel length (L) is ~ 1.5 μ m, and the radius (r) of the In₂O₃ NW is 10 nm. The measured g_m at $V_d=0.5$ V, along with a Gaussian fit to the data, is illustrated in Fig. 3(a). The g_m peaks at ~ 5.87 μ S, at $V_g \sim 1$ V, and falls off with increasing gate voltage. The corresponding μ is plotted versus gate bias in Fig. 2(a) and varies from ~ 1450 cm²/V s to ~ 300 cm²/V s over the measured gate bias range. The peak mobility values of two other devices with from the same sample batch, with nominally identical structures, are ~ 1200 and 1170 cm²/V s. The peak value, which is typically quoted as the mobility in comparable devices, significantly exceeds In₂O₃ NW mobilities ($\mu=6.93-279$ cm²/V s) reported in other devices¹⁰⁻¹³ and in single-crystal In₂O₃ (~ 160 cm²/V s).¹⁸ It is expected that the NW single-crystal nature along with the quasi-one-dimensional electronic structure, which inhibits low-angle scattering, contributes to the very large FET mobility. In addition, the SAND gate dielectric has previously been found to enable high performance in other oxide NWs.¹⁹

Several aspects of the observed current-voltage characteristics can be attributed to the effects of the contacts. While an ideal long-channel metal-oxide-semiconductor field-effect transistor (MOSFET) model describes the low V_{ds} data, the behavior at large V_{ds} deviates from the ideal MOSFET model both in terms of the nonsquare law relationship versus V_{gs} and the relatively large drain conductance. Based on calculated electrostatic screening lengths,²⁰ the characteristic length over which the bands bend at the metal-semiconductor (M-S) contact interface, as illustrated in Fig. 1(c), is estimated to be ~ 30 nm. This characteristic length

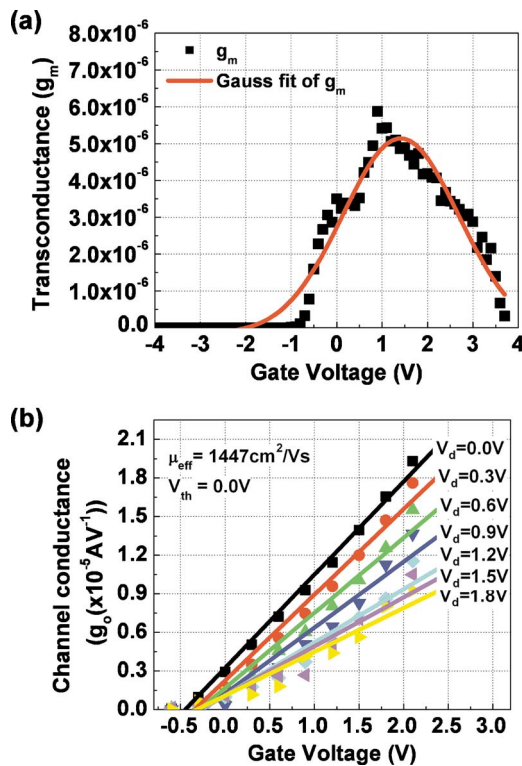


FIG. 3. (Color online) (a) Measured transconductance (g_m) at $V_{ds}=0.5$ V, along with a Gaussian fit to the data. (b) Measured channel conductance (g_d) vs V_{gs} , with various curves corresponding to steps in V_{ds} from 0.0 to 1.8 V.

would be reduced by channel charge induced by the gate potential or due to donor doping, which typically arises from oxygen vacancies in metal-oxide semiconductors. For this range of barrier thicknesses, it is expected that the contact behavior would be dominated by thermionic-field emission,²¹ which would yield a nonlinear current-voltage characteristic for the M-S contacts. A prior study on NW transistors indicated that the effects of such a barrier in series with the channel included a roll-off in transconductance with increasing gate bias,²² comparable to that observed in the present study. Figure 3(b) shows the measured channel conductance (g_d) versus gate voltage for various values of V_d . Linear series/contact resistance effects, would be expected to result in a saturation of g_d with increasing V_g .²³ However, no saturation is observed, indicating that linear series resistance effects are not dominant factors in the current-voltage (I - V) characteristics over the present bias range. The curves in Fig. 3(b) for low V_d values are somewhat superlinear, likely due to increasing conductance of the M-S contact barriers with increasing gate bias. These observations are consistent with the modest, but nonzero, M-S contact barrier illustrated in Fig. 1(c).

In conclusion, high performance, transparent NWTs have been fabricated using single In_2O_3 nanowires as the active channel, a SAND layer as the gate insulator, alumi-

num as source-drain electrodes, and ITO as the gate electrode. The single In_2O_3 NWTs were operated by individually addressable gate electrodes, which represents a significant advance toward circuit fabrication, and outstanding NWT device performance metrics were obtained using a SAND gate dielectric and proper processing of the In_2O_3 nanowire. As a result, we achieved significantly enhanced In_2O_3 NWT device performance and a significantly greater mobility than observed in poly-Si TFTs and α -Si TFTs. Since it is desirable to obtain high μ and a steep S to fabricate rapid-switching transistors and high-speed logic circuits, these results indicate that SAND-based In_2O_3 NWTs can support the requirements of such devices.

This work was supported in part by the NASA Institute for Nanoelectronics and Computing under Grant NCC-2-1363.

- ¹J. Xiang, W. Lu, Y. Hu, Y. Wu, H. Yan, and C. M. Lieber, *Nature (London)* **441**, 489 (2006).
- ²Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, *Nano Lett.* **3**, 149 (2003).
- ³S. N. Cha, J. E. Jang, Y. Choi, G. W. Ho, D.-J. Kang, D. G. Hasko, M. E. Welland, and G. A. J. Amarantunga, Proceedings of the 38th European Solid-State Device Research Conference, 2005 (unpublished), Vol. 217.
- ⁴W. Kim, A. Javey, R. Tu, J. Cao, Q. Wang, and H. Dai, *Appl. Phys. Lett.* **87**, 173101 (2005).
- ⁵K. Sreenivas, T. S. Rao, and A. Mansingh, *J. Appl. Phys.* **57**, 384 (1985).
- ⁶Y. Shigesato, S. Takaki, and T. Haranoh, *J. Appl. Phys.* **71**, 3356 (1992).
- ⁷J. Tamaki, C. Naruo, Y. Yamamoto, and M. Mastuoka, *Sens. Actuators B* **83**, 190 (2002).
- ⁸M. Liess, *Thin Solid Films* **410**, 183 (2002).
- ⁹M.-H. Yoon, A. Facchetti, and T. J. Marks, *Proc. Natl. Acad. Sci. U.S.A.* **102**, 4678 (2005).
- ¹⁰C. Li, D. Zhang, S. Han, X. Liu, T. Tang, and C. Zhou, *Adv. Mater. (Weinheim, Ger.)* **15**, 143 (2003).
- ¹¹B. Lei, C. Li, D. Zhang, T. Tang, and C. Zhou, *Appl. Phys. A: Mater. Sci. Process.* **79**, 439 (2004).
- ¹²D. Zhang, C. Li, S. Han, X. Liu, T. Tang, W. Jin, and C. Zhou, *Appl. Phys. Lett.* **82**, 112 (2003).
- ¹³N. Pho, H. T. Ng, T. Yamada, M. K. Smith, L. Jun, H. Jie, and M. Meyyappan, *Nano Lett.* **4**, 651 (2004).
- ¹⁴S. N. Cha, J. E. Jang, Y. Choi, G. A. J. Amarantunga, G. W. Ho, M. E. Welland, D. G. Hasko, D.-J. Kang, and J. M. Kim, *Appl. Phys. Lett.* **89**, 263102 (2006).
- ¹⁵T.-H. Moon, M.-C. Jeong, B.-Y. Oh, M.-H. Ham, M.-H. Jeun, W.-Y. Lee, and J.-M. Myung, *Nanotechnology* **17**, 2116 (2006).
- ¹⁶Y. W. Heo, L. C. Tien, Y. Kwon, D. P. Norton, S. J. Pearton, B. S. Kang, and F. Ren, *Appl. Phys. Lett.* **85**, 2274 (2004).
- ¹⁷S. Ju, K. Lee, D. B. Janes, M.-H. Yoon, A. Facchetti, and T. J. Marks, *Nanotechnology* **18**, 155201 (2007).
- ¹⁸R. L. Weiher, *J. Appl. Phys.* **33**, 2834 (1962).
- ¹⁹S. Ju, K. Lee, D. B. Janes, M.-H. Yoon, A. Facchetti, and T. J. Marks, *Nano Lett.* **5**, 2281 (2005).
- ²⁰R.-H. Yan, A. Ourmazd, and K. F. Lee, *IEEE Trans. Electron Devices* **39**, 1704 (1992).
- ²¹F. A. Padovani and R. Stratton, *Solid-State Electron.* **9**, 695 (1966).
- ²²J. Appenzeller, J. Knoch, E. Tutuc, M. Reuter, and S. Guha, Proceedings of 2006 Intl. Elect. Dev. Meeting (IEDM), IEEE, 2006 (unpublished), Vol. 1.
- ²³Z. Yu and P. J. Burke, *Proc. SPIE* **5790**, 246 (2005).