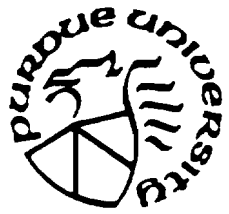
4-1-1992

Low Temperature Silicon Selective Epitaxial Growth(SEG) and Phosphorous Doping in a Reduced-Pressure Pancake Reactor

Weichung Wang
Purdue University School of Electrical Engineering

Jack Denton
Purdue University School of Electrical Engineering

Gerold W. Neudeck
Purdue University School of Electrical Engineering



Low Temperature Silicon Selective Epitaxial Growth (SEG) and Phosphorous Doping in a Reduced-Pressure Pancake Reactor

Weichung Wang
Jack Denton
Gerold W. Neudeck

TR-EE 92-13
April 1992

This work was supported by Business Modernization and Technology Corporation and Delco Electronics.

TABLE OF CONTENTS

Page

LIST OF TABLES

LIST OF FIGURES

Figure Page

ABSTRACT

Pancake reactors operated at low temperatures and reduced-pressures have been used for silicon selective epitaxial growth (SEG). In general, dichlorosilane (DCS) is the silicon source gas, hydrogen is the carrier gas, and HCl prevents the formation of polysilicon on the silicon dioxide. An investigation of growth rate, uniformity, and doping characteristics of SEG silicon grown at reduced pressures between 40 and 150 Torr and temperatures between 820°C and 1020°C in a pancake reactor is presented.

The dependences of growth rates and uniformities on growth temperatures, pressures, and doping were studied. Improvement in thickness uniformity across the wafer was achieved by lowering the deposition temperature and pressure. In-situ phosphorus doping in the range of 10^{16}-10^{18} P atoms/cm^3 was accomplished by introducing phosphine (PH_3) gas into the reactor during epitaxial deposition. Doping concentration, which was determined by three different methods, increased with phosphine inject set point. Also, higher phosphorus concentrations were obtained at lower deposition temperatures and/or pressures. Diodes and bipolar transistors identically fabricated in undoped SEG and in bulk silicon were used to characterize the SEG material quality. Since average ideality factors, leakage currents, breakdown voltages, and current gains extracted from 970°C-40T SEG devices were similar to those of substrate devices, the material quality of the SEG deposited at 970°C and 40 torr was indicated to be as good as the bulk silicon.

CHAPTER 1: INTRODUCTION

1.1 Purpose of Work

Silicon Selective Epitaxial Growth (SEG) is to deposit silicon only at selective locations where the silicon substrate is exposed on an oxide-patterned wafer. This technique is attractive because of its applications in the area of advanced bipolar, CMOS, BiCMOS, and other novel devices. Hence, the material quality of the selective epitaxial silicon is an important issue for utilizing SEG technology.

The objective of this research work is to determine epitaxial growth conditions in a Gemini-1 pancake reactor. A fabrication process for test devices and a test mask set were designed and implemented. Selective epitaxial silicon films were deposited under various growth conditions to investigate the growth rate and uniformity dependances on deposition temperature, reactor pressure, partial pressures of the reactant species, and the injection rate of phosphine (PH_3) dopant gas. Then test devices were fabricated on the SEG/ELO materials and tested. After physical and electrical characterization for the SEG/ELO films grown at different conditions, appropriate operation regions for the Gemini-1 pancake reactor were defined. The results are helpful to obtain selective epitaxial silicon with desired growth rate, uniformity, and doping characteristics.

1.2 Overview of Thesis

This thesis describes the fundamentals of silicon selective epitaxial growth, device fabrication, testing procedures, as well as physical and electrical test results. A literature review is presented in the second chapter to provide background information on epitaxial growth theory, epitaxial reactors, common defects, properties, and growth considerations for SEG/ELO, and in-situ doping as well. Chapter three describes in detail the fabrication and testing procedures for the test devices fabricated on SEG materials. Mask layout, SUPREM-III simulations, and many commonly used evaluation methods for SEG

materials are presented in this chapter. Chapter four presents the characterization results of this work; and is divided into growth rate studies and electrical evaluations. Finally, a conclusion is discussed in chapter five.

CHAPTER 2: BACKGROUND

2.1 Silicon Epitaxy

The silicon epitaxy is to grow a thin single crystal silicon layer upon a single crystal substrate. During the growth, the epitaxial layer can be in-situ doped with n-type or p-type dopants. Silicon epitaxial growth is widely used in the bipolar fabrication processes and is becoming important for MOS technologies [1-3]. It is also used in discrete power devices and CCD technology [4-6]. For bipolar, a lightly doped silicon epitaxial layer upon a substrate with higher concentration can isolate the substrate and reduce the collector series resistance. On the other hand, epitaxial structures are used to enhance the performance of DRAMs and CMOS ICs and to reduce the soft errors and alleviate the latchup problem [7-9].

Silicon epitaxy can be achieved in various systems. Among these, chemical vapor deposition (CVD) epitaxy is by far the most important if we consider its usage, processing speed, and control of the impurity concentration [10]. Silicon CVD has been accomplished with silane (SiH_4), dichlorosilane (SiH_2Cl_2), trichlorosilane ($SiHCl_3$), and silicon tetrachloride ($SiCl_4$). The progress towards reduced pressure and low temperature epitaxy produces epitaxial layers with low defect levels and can reduce pattern shift and autodoping [11-14].

2.1.1 Fundamentals of Epitaxy

CVD epitaxy of silicon films can be represented schematically as shown in Figure 2.1 [15]. The reactants diffuse through the carrier gas to the surface. They are absorbed on the substrate surface where chemical reactions take place. Then the reaction by-products are desorbed from the surface and diffuse away into the carrier gas. In this section, the basic principles, including kinetics and transport, of silicon epitaxy will be discussed.

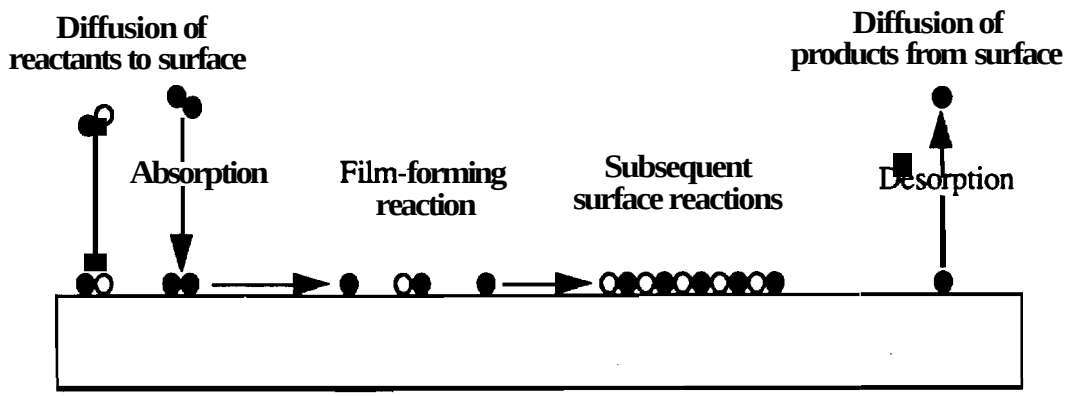


Figure 2.1 Schematic of CVD reaction steps [15].

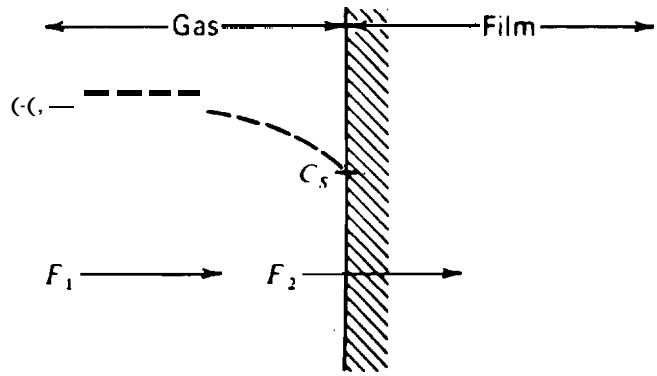


Figure 2.2 Basic model for the epitaxial growth process [16].

2.1.1.1 Kinetics of Growth

Grove [16] developed a simple model to study the kinetics of epitaxial film growth. The model as shown in Figure 2.2 explains many phenomena observed in the epitaxial growth process. As shown, the concentration of the reactant species in the bulk of the gas is Cg but becomes Cs at the surface of the substrate. The reactant gas for silicon epitaxy may be one of the following: SiH_4; SiH_2Cl_2; $SiHCl_3$; or $SiCl_4$. Note that the flux of reactants towards the interface is F_1 and the flux of reactants consumed in the epitaxial reactions is F_2.

We assume that the flux F_1 can be expressed by the linear formula

$$F_1 = h_g(C_g - C_s) \tag{2.1}$$

where h_g is the gas-phase mass transfer coefficient. The flux F_2 is assumed to be linearly proportional to C_s and expressed by

$$F_2 = K_s C_s \tag{2.2}$$

where K_s is the surface reaction rate constant. In steady state, $F_1 = F_2 = F$ and therefore

$$C_s = \frac{C_g}{1 + \frac{K_s}{h_g}} \tag{2.3}$$

The growth rate of silicon epitaxial film, V, is given by

$$V = \frac{F}{N_1} = \frac{K_s h_g}{K_s + h_g}\left[\frac{C_g}{N_1}\right] \tag{2.4}$$

where N_1 is the number of silicon atoms incorporated into a unit volume of the film which is 5×10^{22} atoms/cm^3. Since $C_g = YC_t$, where Y is the mole fraction of the reactant species and C_t is the total number of molecules per cubic centimeter in the gas, the expression for the growth rate is:

$$V = \frac{K_s h_g}{K_s + h_g}\left[\frac{C_t}{N_1}\right] Y \tag{2.5}$$

Equation 2.5 states that the growth rate is proportional to the mole fraction Y of the reactant species. The growth rate at a given mole fraction is determined by the smaller value of K_s or h_g. This corresponds to the limiting cases of mass-transfer controlled and surface-reaction controlled conditions. In these two cases, the growth rates are given by

$$V = K_s\left[\frac{C_t}{N_1}\right] Y \quad \text{[surface reaction-controlled]} \tag{2.6}$$

or

$$V = h_g\left[\frac{C_t}{N_1}\right] Y \quad \text{[mass transfer-controlled]} \tag{2.7}$$

The temperature dependence of growth rates of silicon films for various silicon gas sources is shown in Figure 2.3 [17]. The growth rate is proportional to $\exp(-E_a/KT)$ in region A, while it is almost independent of temperature in region B. Since chemical reaction rate constants generally follow an exponential temperature dependence while mass-transfer coefficients are independent of temperature, region A is referred to as surface reaction-controlled. Region B (higher temperature) is referred to as mass transfer-controlled.

This simplified model neglects the flux of reaction products and assumes a linear approximation for the surface reaction. In spite of these, the Grove model still describes the two regions of the growth process and gives an estimate of K_s and h_g from the growth rate data.

2.1.1.2 Gas Phase Mass Transfer [18,19]

Equation 2.1 assumed the flux from the gas bulk to the surface by $F_1 = h_g(C_g - C_s)$. The simplest model used to approximate the value of h_g is the stagnant-film model which is shown in Figure 2.4. The gas is divided into two regions. In one region the gas is well mixed and is moving past the surface with a constant velocity. The other region is a stagnant film region of thickness δ next to the substrate. Mass transfer of the reactant species across the stagnant film to the substrate proceeds only by diffusion. Let D_g be the diffusivity of the active species, then flux F_1 can be written as

$$F_1 = D_g\frac{C_g - C_s}{\delta} \tag{2.8}$$

Comparing Equation 2.1 and Equation 2.8, we obtain

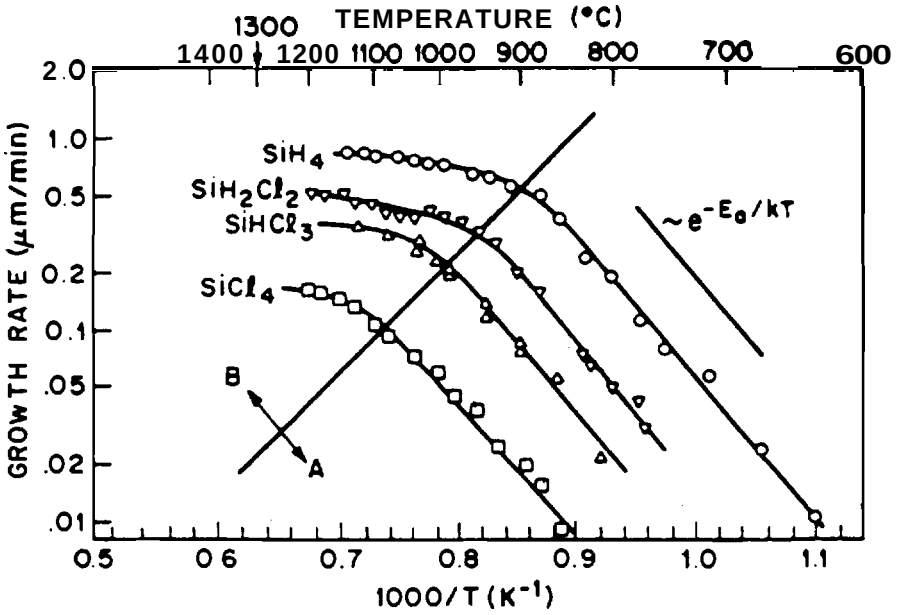


Figure 2.3 Temperature dependence of growth rates for various silicon gas sources [17].

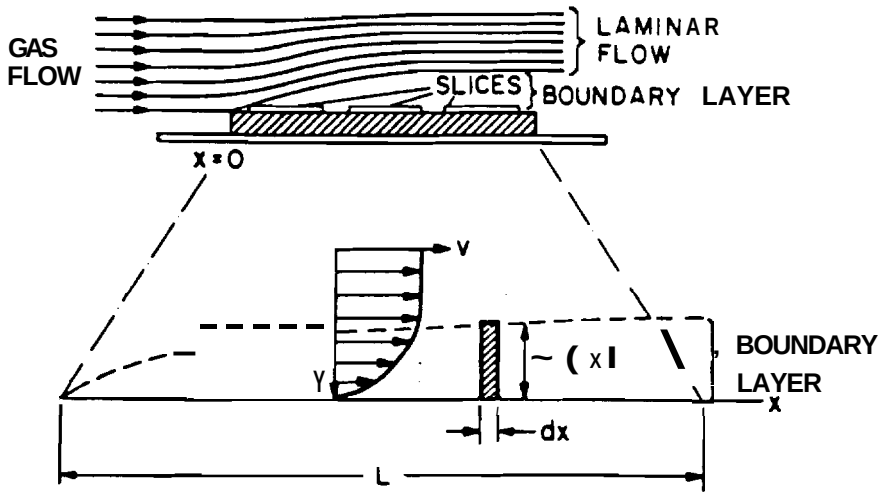


Figure 2.4 Development of a boundary layer in gas flow over a flat plate and expanded view of the boundary layer [18].

$$h_g = \frac{D_g}{\delta} \tag{2.9}$$

Fluid mechanics is able to provide a more realistic and accurate estimate of the mass-transfer coefficient h_g. Boundary layer theory developed by Prandtl is used for this problem. It describes a boundary layer is a transition region between the substrate and the free gas stream. At the substrate, the velocity is zero because of friction. In the boundary layer, the reactant species must diffuse to reach the substrate surface. Above the layer, the gas stream flows with a uniform velocity U as shown in Figure 2.4. The boundary layer thickness $\delta(x)$ is defined as the distance between the surface and the point at which the velocity is $0.99U$.

The thickness can be calculated from [18]

$$\delta(x) \cong \sqrt{\frac{\mu x}{\rho U}} \tag{2.10}$$

where μ, ρ are the viscosity and density of the gas, respectively. The average boundary layer thickness δ over the whole plate is given as

$$\bar{\delta} = \frac{1}{L}\int_0^L \delta(x)dx = \frac{2}{3}\sqrt{\frac{\mu L}{\rho U}} \tag{2.11}$$

or

$$\bar{\delta} = \frac{2L}{3}\sqrt{\frac{\mu}{\rho UL}} = \frac{2L}{3\sqrt{Re_L}} \tag{2.12}$$

where Re_L is the Reynolds number. Now if we substitute $\bar{\delta}$ for the thickness of the stagnant film 6 in Equation 2.9, the mass-transfer coefficient h_g is:

$$h_g = \frac{D_g}{\bar{\delta}} = \frac{3}{2}\frac{D_g}{L}\sqrt{Re_L} \tag{2.13}$$

We can notice that h_g is proportional to $\sqrt{U}$. Hence in the mass-transfer controlled regime, the growth rate should be a function of gas flow rate in the reactor. This is in agreement with Theuerer's data in the vertical reactor [20]. A number of researchers have analyzed the transport phenomena in epitaxial reactors [21-25] . In order to calculate gas phase mass transport accurately, it is necessary to take more factors into account instead of the simplifying assumptions. For example, temperature variation above the susceptor, gas

phase reactions, and nonlinear reactant concentration gradient in the boundary layer, all of which could affect the accuracy. In addition, it is necessary to use numerical methods to precisely simulate mass transport for advanced reactors [26].

2.1.2 Silicon Source Gases and Chemical Reactions

Silicon tetrachloride ($SiCl_4$), trichlorosilane ($SiHCl_3$), dichlorosilane (SiH_2Cl_2), and silane (SiH_4) are four major gas sources which have been used for silicon epitaxy. $SiCl_4$ has been widely used in the past for silicon epitaxial growth. It is chemically stable and has a rather low vapor pressure, and it usually leaves very little silicon coating on the reactor walls. The disadvantage of using $SiCl_4$ is that it requires a high deposition temperature (1100°C - 1300°C). The overall reaction is a hydrogen reduction of the gas, written as

$$SiCl_4 + 2H_2 \rightarrow Si + 4HCl \tag{2.14}$$

SiH_2Cl_2 and $SiHCl_3$ have similar characteristics to that of $SiCl_4$ except that they can be used at lower deposition temperatures for comparable growth rates and crystal quality. Since lower temperatures reduces autodoping and diffusion, SiH_2Cl_2 is widely used in low temperature silicon epitaxy. At Purdue University, a Gemini-1 reactor uses SiH_2Cl_2 as the silicon source gas. It has been shown that SiH_2Cl_2 has the highest efficiency of the reaction, i.e., the ratio of the amount of deposited silicon to the amount of reactant gas entering the reactor, while $SiCl_4$ is the lowest.[27]

Compared to chlorosilane chemistries, SiH_4 is not widely used for silicon epitaxy though the deposition temperature for SiH_4 is lower. The disadvantages of using the SiH_4 reaction are that homogeneous gas phase reaction could occur and no HCl is set free. SiH_4 is not a stable gas and reduces in the gas phase and forms silica dust. The wafers could be contaminated and the walls of the reactor need frequent cleaning because of the heavy deposition. Silicon deposition reaction using silane is different from those using chlorosilane since no HCl is present in the decomposition of silane. Therefore, no Cl can be used to removed metallic impurities from silicon. Silane used to form silicon by the pyrolytic decomposition is given by the reaction

$$SiH_4 \rightarrow Si + 2H_2 \tag{2.15}$$

while the reactions using DCS are

$$SiH_2Cl_2 \rightarrow SiCl_2 + H_2 \quad (2.16)$$

$$SiCl_2 + H_2 \rightarrow Si + 2HCl \quad (2.17)$$

where HCl is a decomposition by-product. HCl will etch any silicon atoms which nucleate on the oxide surface and therefore prevent further nucleation by the reaction

$$Si + 2HCl \rightarrow SiCl_2 + H_2 \quad (2.18)$$

By adjusting the HCl amount in the entering gases, good selectivity is obtained. Continually increasing the HCl amount, growth eventually enters the etching regime where etching of the silicon substrate surface will occur and no longer permit silicon epitaxy.

2.1.3 Epitaxial Reactors

Figure 2.5 illustrates typical epitaxial reactor configurations which are used in the microelectronics industry. The horizontal, vertical or pancake, and barrel reactors are all cold-wall reactors. Reactor walls are cooled to minimize deposition on the walls while the susceptors are heated by rf induction coils or by high-intensity radiation lamps.

The simplest is the horizontal reactor which consists of a horizontal quartz tube. Wafers are placed horizontally on a graphite susceptor in the tube. The wafers are heated by the susceptor that is rf power coupled. Gases used for growing epitaxial silicon enter at one end of the tube and are exhausted from the other end. The flow of gas is parallel to the wafer surface and the reactant species are supplied to the growth interface via diffusion through the boundary layer on the surface. This kind of reactor offers lower construction cost, but controlling the deposition over the entire susceptor is a problem. It is difficult to get good temperature, thickness, and doping uniformities within a wafer and from wafer to wafer.

In the vertical pancake reactor, the wafers are placed on the silicon carbide coated graphite susceptor which is heated by the underlying rf coils. The susceptor is near the bottom of the quartz bell-jar. The reactant gases enter from the center of the circular susceptor, rise to the top of the bell-jar and then spread downward. Some gas exits to the exhaust in the bottom while some flows over the susceptor. The gases are distributed evenly across all wafers and the susceptor rotates to further smooth out any nonuniformity in flow. Thus, good thickness and doping uniformities are obtained. The vertical pancake

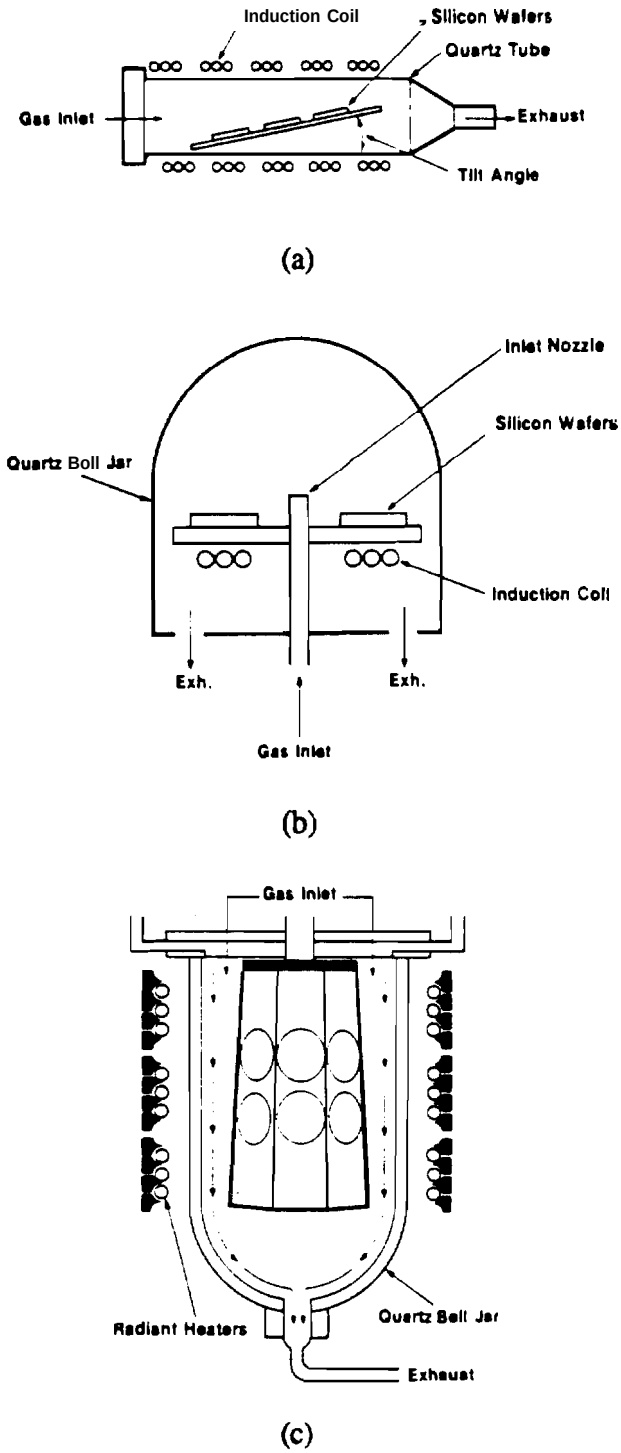


Figure 2.5 (a) Horizontal, (b) pancake, and (c) barrel reactors commonly used for vapor-phase silicon epitaxy [30].

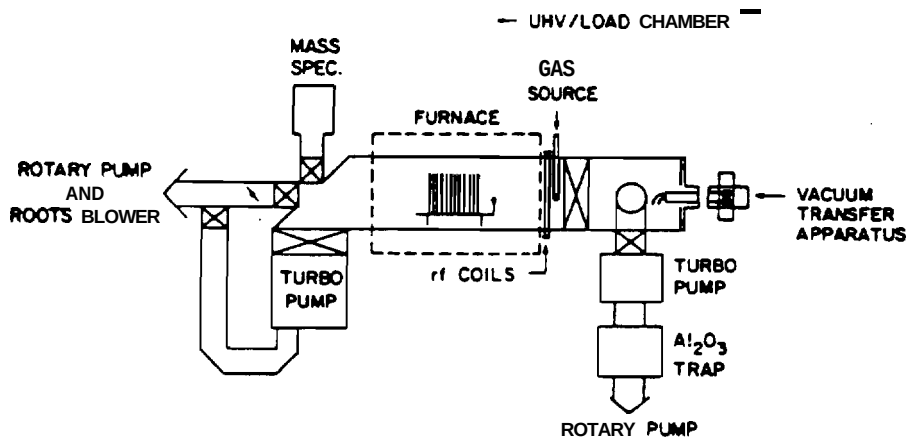


Figure 2.6 UHV/CVD system schematic [13].

system is capable of running at reduced pressure as well as at atmospheric pressure to minimize autodoping effects and pattern shift.

In the barrel reactor, the graphite susceptor has a hexagonal cross-section. The wafers are held about 2.5' to the vertical on the susceptor in the bell-jar to compensate for boundary layer and reaction depletion effects [28]. The gases flow parallel to the wafer surface. Wafers are radiantly heated so that it is easy to get good temperature uniformity. The flow pattern of gases in the barrel reactor is quite complex [29]. Gases are injected from the top of the reactor through a pair of nozzles and the flow is directed down one side of the chamber. The susceptor rotates to average out the differences in growth rate. Thickness uniformity is comparable to that in vertical reactors and it can operate at reduced or at atmospheric pressure.

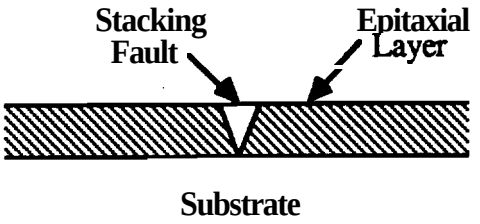
Epitaxial silicon layers can also be deposited by ultrahigh vacuum/chemical vapor deposition (UHV/CVD) [13,31]. Meyerson has demonstrated that device quality material can be obtained at temperatures as low as 750°C in this kind of system. The key requirement for successful silicon epitaxy is to keep the silicon surface clean and atomically bare at the time epitaxial growth begins. In order to keep the silicon surface bare, the temperature must be high enough or the partial pressure of water vapor must be low enough. Figure 2.6 shows a UHV/CVD apparatus. The vacuum level in the apparatus can bring silicon wafers rapidly into an environment that maintains the bare surface. The UHV section is pumped, baked, and hydrogen plasma scoured until the base pressure is about 10^{-9} tom. The wafer carrier is prebaked in the load chamber before transfering it into the UHV system via a magnetically coupled load lock. Wafers are placed coaxially in the growth chamber. The mass spectrometer in the UHV section allows in-situ diagnostics of the system.

2.1.4 Common Defects

A number of different defect types have been observed in silicon epitaxial films. The most typical two are growth stacking faults and dislocations. Sometimes other gross defects are found that usually resulted from improper cleaning or handling procedures.

2.1.4.1 Stacking Faults

Stacking faults, as illustrated in Figure 2.7, are the most important types of defects that are found in silicon epitaxial growth [32,33]. Most of the work on defects in epitaxial growth is devoted to the study of stacking faults. In general, epitaxial growth requires



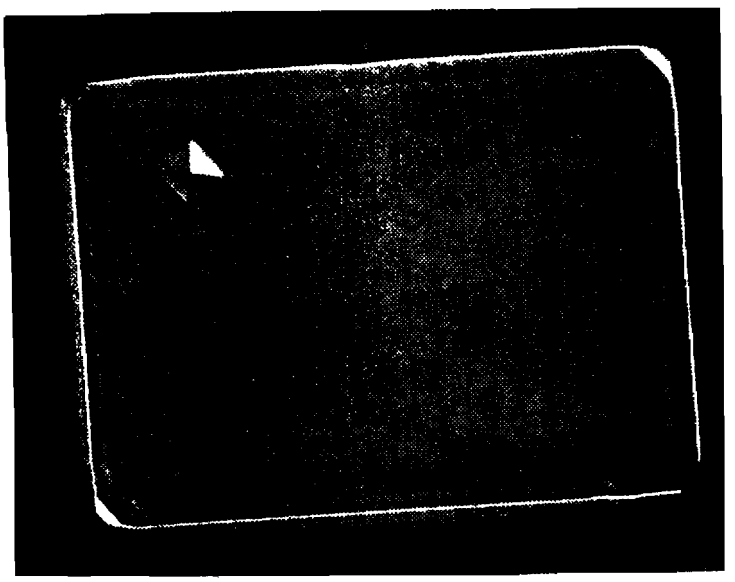


Figure 2.7 Epitaxial stacking fault in selective epitaxial growth, under Nomarski illumination on a (100) substrate.

atomic layers in a regular order, i.e., to form a new layer only after the last one has been completely formed. However, if there is a small area of mismatched stacking with respect to the substrate (e.g., by an impurity atom), the regularity of the atomic layers would be disturbed. The fresh successive layers will continue to grow in this new kind of sequence with the fault, hence the stacking fault occurs.

The stacking faults appear as equilateral mangles on the epitaxial layer surface when grown on {111) silicon wafers. Each side of the stacking fault is in a <110> direction. For {100) wafers, the shape of a stacking fault looks like a square in shape and each side of the stacking fault is along a <100> direction. Stacking faults in (100) silicon wafers propagate along (111)plane. Thus they are actually in the form of pyramids with a square base as shown in Figure 2.7. The length of each side is related to the thickness of epitaxial layer. Therefore, a rough estimate of epi thickness can be obtained from the width of the stacking fault.

Epitaxial stacking faults could be formed as a result of several factors. These include both external and internal factors, such as contaminants and mechanical damage on the substrate surface, contaminants introduced into the epitaxial reactor during deposition, the condition of deposition, and crystallographic defects of the substrate [33].

Contaminants on the substrate surface could nucleate stacking faults in the epitaxial layer [34]. Surface mechanical damage on the substrate in the form of scratches, saw marks, etc. and slip bands also are common reasons for obtaining stacking faults. Incomplete removal of oxide from the substrate before epitaxial growth is found to cause stacking faults in the epitaxial overgrowth. Stacking faults generated by the effects of gaseous contaminants such as carbon, oxygen, and metallic impurities have also been observed. Carbon can form silicon carbide precipitates to provide sites for nucleation of stacking faults [35]. The nucleation of growth stacking faults caused by bulk crystallographic defects in the substrate has also been demonstrated. Plastic deformation during film deposition can also give rise to stacking faults. It would occur when wafers are nonuniformly heated during epitaxy or when wafers are put in and withdrawn from the hot furnace at high rates during diffusion and oxidation . This is because thermal gradients are established between center and periphery.

Several electrical effects in devices are a result of stacking faults. These include the formation of emitter-collector pipes or shorts in bipolar transistors as well as the increase of the reverse leakage currents and breakdown voltage reduction in the p-n junction. The formation of pipes is because epitaxial defects will collect metallic impurities and allow

accelerated movement of dopants. These pipes can short the base-emitter and base-collector junctions of bipolar transistors.

2.1.4.2 Dislocations and Other Defects

During the epitaxial growth, wafers are placed on a graphite: susceptor which is subsequently heated to a high temperature. Nonuniform heating may occur because the susceptor is nonuniformly heated or because a lack of intimate contact between the susceptor and wafers [36]. This results in large temperature gradients. If temperature gradients are large enough, dislocations will be generated. In addition, propagation of substrate dislocations into the epi layer is also possible.

Some other gross defects caused by poor fabrication techniques may occur during the epitaxial growth process [37]. Orange peel appearance is sometimes caused by preferential etching during the in-situ cleaning step before growth. Pits, voids, growth hillocks or spikes result from small particles of silicon or oxide in the reactor during the growth. Haze is caused by a leaky system or by improper cleaning prior to epitaxial growth and can be avoided by taking proper precautions.

2.2 Selective Epitaxial Growth and Epitaxial Lateral Overgrowth

2.2.1 Introduction

The selective epitaxial growth (SEG) of silicon is a special epitaxy technique useful for small device isolation [38-40] and as epitaxial lateral overgrowth (ELO), for advanced device structures [41-44]. SEG allows the epitaxial silicon be grown only in selected regions on a wafer. These selected regions are usually photolithoghaphically opened windows in an oxide layer. SEG evolved from full-wafer silicon epitaxy and hence growth conditions are quite similar to those of full-wafer epitaxy. Though SEG was first reported in 1962 [45], it has only recently overcome problems with defects, selectivity, and growth uniformity by utilization of purified hydrogen, hydrogen chloride, and dichlorosilane gases at low temperatures (<1000°C) and at reduced pressure (10-200T) in cold-wall epitaxial reactors [38,46,47]. This technique has brought much attention for the development of various novel device structures.

Selective epitaxy is grown on the exposed silicon in the seed window, which are defined in a mask material. usually oxide, on a silicon wafer as depicted in Figure 2.8(a).

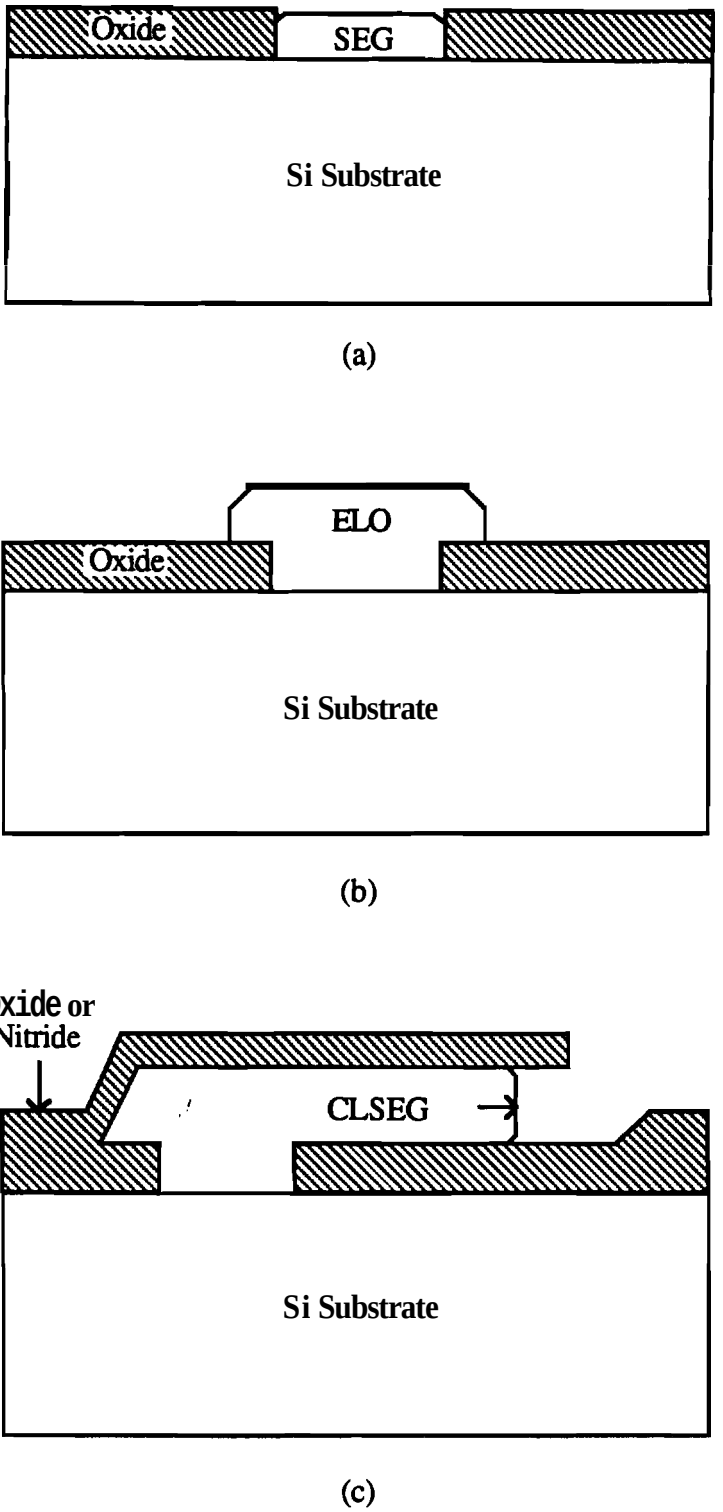


Figure 2.8 (a) Selective epitaxial growth (SEG), (b) Epitaxial lateral overgrowth (ELO), and (c) Confined lateral selective epitaxial growth (CLSEG).

The deposition conditions are adjusted to allow epitaxial growth only on the exposed silicon surface and not on the masking oxide. When the epitaxial silicon is grown for longer periods of time so that the growing surface is above the mask surface level, it will grow laterally over the oxide mask as well as growing vertically. This is shown in Figure 2.8(b) and is referred to as epitaxial lateral overgrowth (ELO). The overgrowth ratio is defined as a ratio between the lateral dimensions of the ELO film and its thickness over the oxide. Most reported ratios are about 1:1. Confined lateral selective epitaxial growth (CLSEG) [48] is grown using the same conditions as SEG, but the epitaxial silicon grows vertically and then laterally in a cavity or tunnel consisting of oxide or nitride walls as shown in Figure 2.8(c).

To keep initial growth surface clean and bare of oxide, SEG deposition begins with a high temperature H2 bake and an optional HCl etch. During the H2 bake, the reaction $Si + SiO_2 \rightarrow 2SiO_{(g)}$ will remove any native oxide (10-100Å thick) [49]. This etch competes with the oxidation of silicon by water vapor and oxygen and requires a very dry and oxygen free environment for removing the native oxide [50,51]. H2 is intraduced into the reactor during this etch since it is easily cleaned and dried with in-line filter. It will not react with the wafer and will displace or carry out the residual H_2O and O2. At the same temperature and pressure, the quality of SEG improves with the reduction of water vapor and O2 levels in the reactor. It was determined experimentally that the critical temperature, above which deposition of good quality epitaxial silicon is possible, is governed by the moisture and oxygen partial pressure during precleaning and growth processes. The HCl etch is usually performed after the native oxide has been removed with the H2 bake. This each will not etch the oxide but etches the exposed silicon surface. Hence it is used to remove surface impurities and damage to get an atomically clean surface for growth. However, if too much of HCl and too large a temperature is used, an undercut between silicon and oxide may occur which can lead to edge defects[40,52,53].

SEG/ELO is normally deposited in reduced-pressure reactors. It was a breakthrough in SEG technology to use reduced pressures (<200T) and low temperatures (<1000°C) as reported by Tanno et al. in 1982 [47]. The reduced pressures and temperatures result in improved surface morphology, improved selectivity, reduction in SEG/sidewall interface defects, and decreased undercutting of the masking material. Though any silicon source gas used for conventional epitaxy can be used for SEG/ELO, dichlorosilane (DCS) is the most common. A carrier gas of hydrogen is used to improve the uniformity of growth rates across a single wafer and from wafer to wafer without contaminating the chamber.

Nucleation of polysilicon on the masking material produces nonselective growth. Selectivity is affected by DCS and H_2 flow rates, the deposition temperature and pressure, and the masking material. To prevent the polysilicon nucleation, HCl gas is added into the deposition gases [46]. In addition, reduced pressure and low temperature are used to suppress the nucleation [46,47,52]. It has also been found that nucleation generally occurs less often on thermal silicon oxide than on silicon nitride.

The quality of SEG/ELO depends on several deposition conditions, such as temperature, pressure, seed orientation, masking materials, and contaminants in the reactor. For masking materials, oxide has been shown to be the better material than nitride because nitride generates more defects along the sidewalls. Therefore, oxide is generally used as the masking material. Lower deposition temperatures and reduced pressure improves the uniformity and selectivity. The lower temperature makes the surface reaction rate slow, and the reduced pressure increases the diffusion rate of silicon gaseous species to the wafer surface. These two effects will bring deposition into the surface reaction controlled regime [11,38,47,54,55]. In this regime, deposition of silicon is a function of temperature instead of gas flow. The temperature is more readily controlled than the gas composition. Therefore, the uniformity is improved when we use low temperature, reduced pressure deposition.

At higher temperatures and pressures, deposition is diffusion-limited, i.e., gas phase diffusion through the boundary layer controls growth. Because the steady state concentration of gaseous silicon species over the oxide is higher than that over the silicon surface, more silicon will grow at the edges of seed holes than in the center. This results in a concave upward SEG profile. We call this phenomenon smiley since it looks like a grin.

2.2.2 Growth Characteristics

The Gemini-1 silicon epitaxy reactor in the Purdue University Epitaxy Laboratory is a low temperature, reduced pressure, RF-induction heated pancake reactor. Hydrogen is the carrier gas, dichlosilane (DCS) supplies the silicon source and HCI provides in-situ cleaning and suppresses polysilicon nucleation. Generally, SEG and ELO were accomplished at 150 Torr and 970°C in Purdue. However, reduced the temperature and pressure for SEG/ELO to 840°C and 40 Torr is possible. In the following subsections, the characteristicsof SEGELO growth conditions and growth phenomenon are reviewed.

2.2.2.1 Seed Window Orientation and Faceting

The seed window orientation has an effect on the SEG quality. It was determined that seed windows oriented along <100> directions on a (100) substrate have the lowest density of defects [56-59] and give a uniformly flat top surface [40,57,59,60]. SEG grown on (100) substrates have much better quality than that grown on (111) substrates because of the lower probability of forming stacking faults [52]. Seed windows which are not aligned to <100> directions generate facets at the sidewall interface, thus reducing active device m a s and the integrity of metal interconnect lines. One solution to this problem is to use chemical-mechanical polishing method to planarize the surface.

Faceting is caused by different growth rates along the different crystal planes. The (100) planes have the highest growth rate, followed by the {110}, (111), and (311) planes [59]. The other planes have much lower growth rates. The problem with faceting isthat it forms a nonplanar surface. In addition to making seed windows aligned to <100> directions [40,59], faceting can be reduced by lowering the growth temperature, reducing the pressure, and increasing HCl concentration [11,38,47,53,61]. When the sidewall is along {110}, <311> facets are observed at the edge of the seed hole. As the growth surface is above the oxide, <111> facets will also appear on the ELO film as shown in Figure 2.9(a). However for (100) sidewalls, less faceting is observed on SEG and only (110) planes shown in Figure 2.9(b) would appear on the ELO film. Hence orient the rectangular patterns at 45° to the [110] flat on a (100) wafer to avoid the faceting as shown in Figure 2.9(b) [59].

2.2.2.2 HCl/DCS Flow Rate Ratio

SEG can be viewed as the result of a deposition reaction and a HCl etching reaction. The dependence of growth rate on the HCl/DCS flow rate ratio has been studied by various researchers. For the pancake reactors, Friedrich has investigated the HCl/DCS flow rate ratio dependence for a total gas flow of 60 standard liters per minute (slm) at 950°C and 150 Torr [63].

Generally, the growth rates decrease as HCl increases, and the growth rates increase as the DCS increases. Therefore it is expected that lower growth rates occur at higher HCl/DCS ratios. Most reported observations used a fixed DCS flow rate while varying the HCl flow rate and resulted in a linear dependence between growth rates and the HCVDCS ratios. However, if both HCl and DCS rates are changed in the experiments, sometimes a higher HCl/DCS ratio can result in a higher growth rate. Kastelic [64]

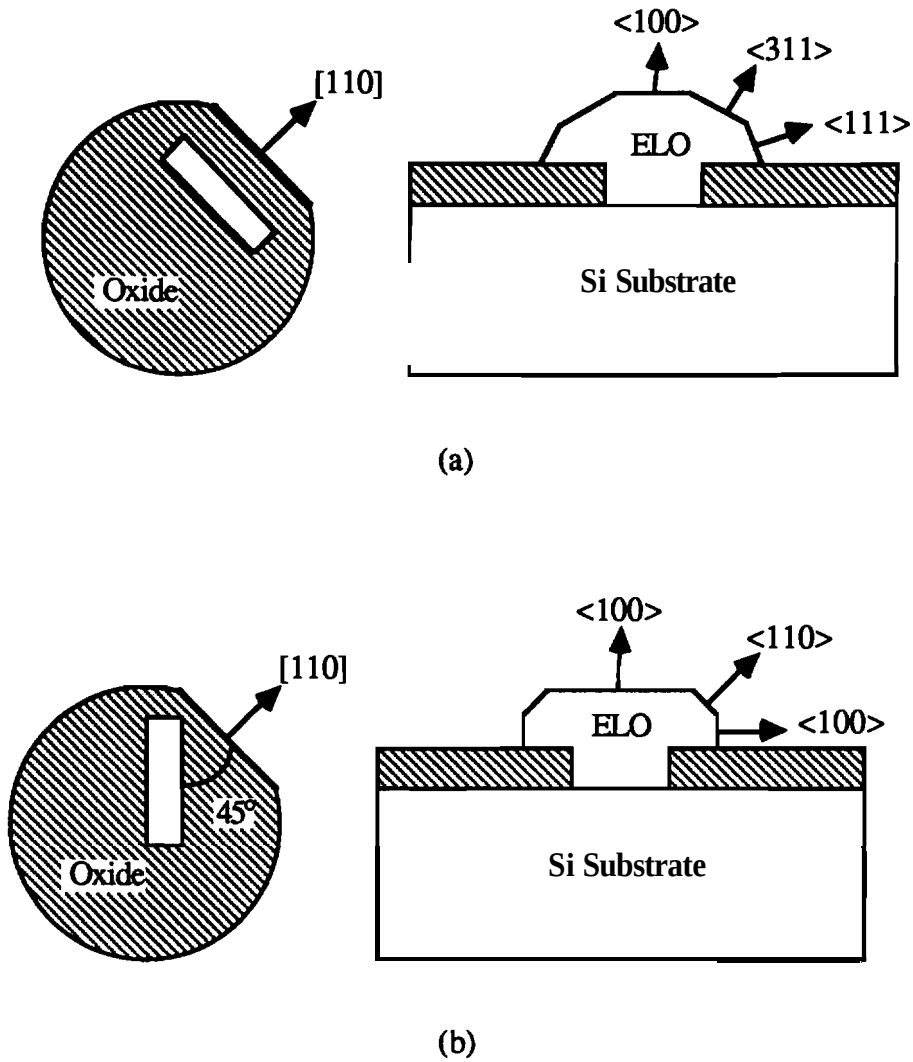


Figure 2.9 ELO facets : (a) Seed window is along <110> directions. (b) Seed window is along <100> directions [62].

suggested to use the quantity of HCl^2/DCS instead of HCl/DCS to get a more accurate and clear result to compare different experiment results.

For the Gemini-1 pancake reactor, Friedrich found that the change in growth rates along the radial direction across the susceptor was basically independent of the HCl and DCS composition. If non-uniformity is defined as

$$\text{Non-uniformity} = \frac{GR_{max} - GR_{min}}{GR_{max} + GR_{min}} \times 100\% \qquad (2.19)$$

where GR_{min} and GR_{max} are the lowest and highest growth rates which measured along the susceptor respectively. The amount of non-uniformity was found to decrease as growth rate increased. Hence the most uniform epi films were obtained near the transition region of selective growth and polysilicon nucleation on the oxide.

2.2.2.3 Temperature Dependence

The temperature dependence of silicon epitaxial growth from DCS has been investigated by many researchers. From Figure 2.3 in Section 2.1.1.1, the chemical reaction for low temperature silicon epitaxial growth is in the surface reaction-controlled region and will be sensitive to temperature. As shown in Table 1, the higher the temperature, the higher the growth rate expected.

Friedrich did a series of experiments to find out the temperature dependence of silicon epitaxial growth in the Purdue reactor. The germanium melt experiment was carried out first to calibrate the temperature controller of the reactor and the temperature uniformity across the susceptor. The uniformity for deposition on bulk wafers was better than that on the patterned wafers under selective conditions. For patterned wafers under selective conditions, lower deposition temperatures would provide better growth uniformity. Figure 2.10 shows the growth rate profile comparison with different temperatures. Intra-wafer and inter-wafer uniformities have been reported as 2-5% [46,61].

2.2.2.4 Oxide Area Dependence

The growth rates of SEG/ELO can be different depending on the ratio of exposed silicon to oxide covered area. This area dependence has been studied [65,66] and is not desirable because generally it will cause non-uniformity. This effect can be reduced by reducing pressure and temperature or by high HCl flows [65]. Table 2 and Figure 2.11 shows that growth rates increased as the exposed silicon area decreased. This can occur in

Table 1
Temperature dependence of growth from 0.36 vol.% DCS in H_2 at 150 Torr [63].

Temperature (°C)	Growth Rate (μm/min)
900	0.134
950	0.189
1000	0.209

Table 2
Masking oxide area dependence of growth.

Oxide %	Growth Rate (μm/min)	% Non-uniformity
0.95	0.353	19.3
0.90	0.300	14.8
0.50	0.179	17.8
0.30	0.176	9.6

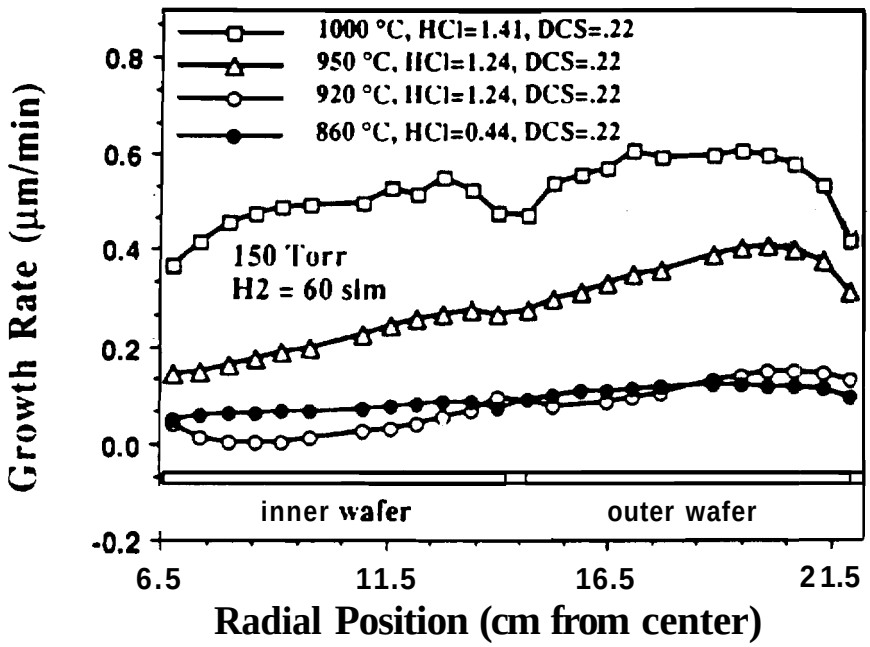


Figure 2.10 Growth rate profile on patterned wafers at different temperatures [63].

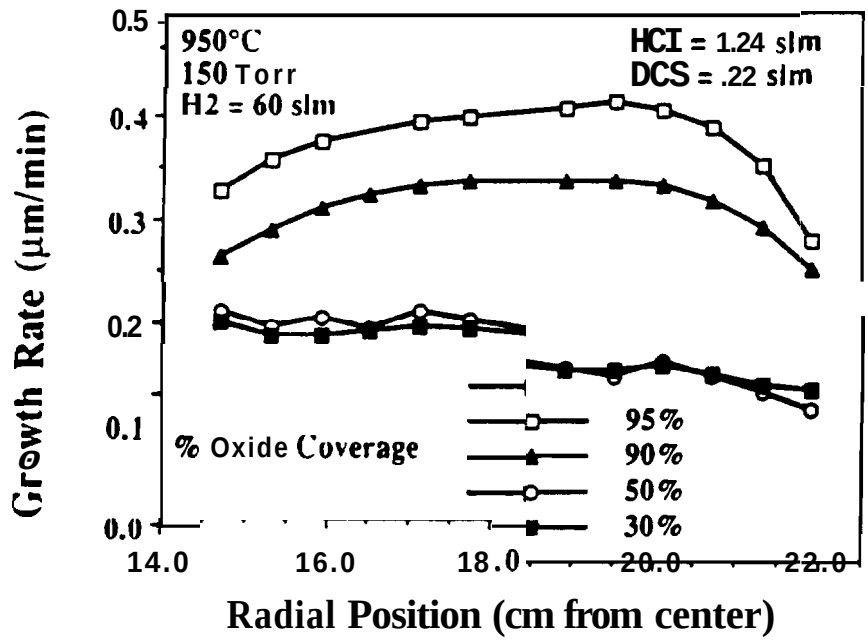


Figure 2.11 Masking oxide area dependence of growth [63].

the device scale or wafer scale. In addition, the uniformity within a run increased as the ratio of oxide area to silicon area fell below about 40%.

2.2.2.5 Oxide thickness

It has been reported that changes in masking oxide thickness affects growth rates. The wafer surface temperature is strongly influenced by the radiative heat transfer properties of the masking oxide layer. Wafers with thinner oxides have higher surface temperature due to decreased radiant heat transfer. This in turn affects the growth rates. For the pancake reactor, growth rate increases for thinner oxides [67]. The growth rates in this study appear to depend on the global average oxide thickness. Local variations in oxide thickness in the immediate vicinity of the seed window have little effect on growth rate. In addition, the absolute change in growth rate with oxide thickness is larger as the value of HCl^2/DCS is smaller, i.e. the growth rate is higher.

2.2.3 Doping

In order to control the conductivity type and carrier concentration of silicon epitaxial layers, gaseous dopants are intentionally introduced into the reactor along with the silicon source gas. Typically, dopants are introduced using their hydrides. Diborane (B_2H_6) is used to incorporate boron, phosphine (PH_3) to incorporate phosphorus, and arsine (AsH_3) to incorporate arsenic. Presently Purdue only has phosphine for n-type doping. There is no simple rule to relate the incorporation of dopant atoms from the gas phase into the silicon film. The dopant level in the epitaxial silicon film is controlled by the amount of dopant introduced into the reactor, by the dopant concentration in the substrate, and by how far the epitaxial layer has grown above the substrate. The intrinsic doping, with no intentional dopants introduced to the reactor and a lightly doped substrate, is about 50 Ω-cm and n-type.

The in-situ boron, arsenic, and phosphorus doping of silicon epitaxial films from silane by ultrahigh vacuum system (UHV/CVD), by low pressure chemical vapor deposition (LPCVD), or by plasma-enhanced chemical vapor deposition (PECVD) have been investigated by various researchers [68-70]. Arsine and phosphine are known to suppress polycrystalline silicon growth rates from silane while diborane enhances the polycrystalline silicon growth rates. Comfort and Reif [68,69] reported that the growth rate and uniformity of silicon epitaxial films deposited by LPCVD were degraded in the presence of arsenic. LPCVD growth rate decreases as the value of ppm AsH_3 in SiH_4

source increases. PECVD growth rates are reported less sensitive to arsine. LPCVD and PECVD arsenic incorporation increases with decreasing the deposition temperature or with increasing the gas-phase arsenic fraction. PECVD deposits exhibit superior morphology to LPCVD and show an increase in active dopant incorporation. There is no significant change in epitaxial growth rates in the presence of diborane. However, LPCVD and PECVD boron incorporation is observed to depend linearly on diborane partial pressures and LPCVD boron incorporation increases with increasing temperature. The n-type and p-type epitaxial silicon films with well controlled doping concentration in the range of 10^{14} - 10^{20} dopant atoms/cm^3 can be achieved.

The interaction between the substrate dopant concentration and the doping of the epitaxial layer will cause two problems, solid state diffusion and autodoping. Solid state diffusion is the diffusion of dopant along its concentration gradient. Autodoping refers to a transfer of dopants which are initially contained in the substrate to the growing epitaxial layers. It is a large problem at high deposition temperatures for which the rate of evaporation of the dopants and the rate of incorporation are significantly high. Using low temperature and reduced pressure conditions for selective silicon epitaxial growth couldminimize the these two problems.

CHAPTER 3: FABRICATION AND TESTING PROCEDURES

3.1 Introduction

The goal of growing SEG/ELO is to use this material for building high quality devices. Therefore without device quality material, fabrication of devices in SEG/ELO is irrelevant. In this work, silicon epitaxial layers grown under different conditions were characterized for (a) surface morphology, (b) growth rate and film thickness uniformity, (c) doping concentration, and (d) electrical properties. Device quality of SEG/ELO material was examined via electrical evaluation of devices built in SEG/ELO. These device characteristics were then compared to those measured on devices fabricated on bulk silicon. Mask layout and fabrication procedures for the test devices, as well as several common characterization techniques, are described in this chapter.

3.2 Mask Layout

Seven mask levels, as listed in Table 3, are designed and implemented for the entire process for all test devices. The first level mask contains a lot of seed windows with different shapes for observing the growth phenomenon and for growing SEG. The second and third levels are used to open windows for boron and arsenic implants, respectively. The optional fourth level is used for polysilicon gates only when it is desirable to make PMOS devices. If it is not necessary to make PMOS devices, then this level is skipped. Level five opens contact windows to the substrate for substrate MOS capacitors and for epi diodes. Level six is designed for contact windows to SEG, and the last level is used for metal definition.

The layout of a complete die for the test devices is illustrated in Figure 3.1. The dimension of each die is approximately 2600μm x 2800μm. Each die consists of different test devices, alignment marks, and strips for spreading resistance profiling (SRP). The test devices in the mask set include BJT transistors, PMOS transistors, E-B diodes, B-C

Table 3
Mask levels for test devices.

Mask Number	Region Defined
1	SEG seed windows
2	Boron implant
3	Arsenic implant
4	Poly gate
5	Contacts to substrate
6	Contacts to epi
7	Metal

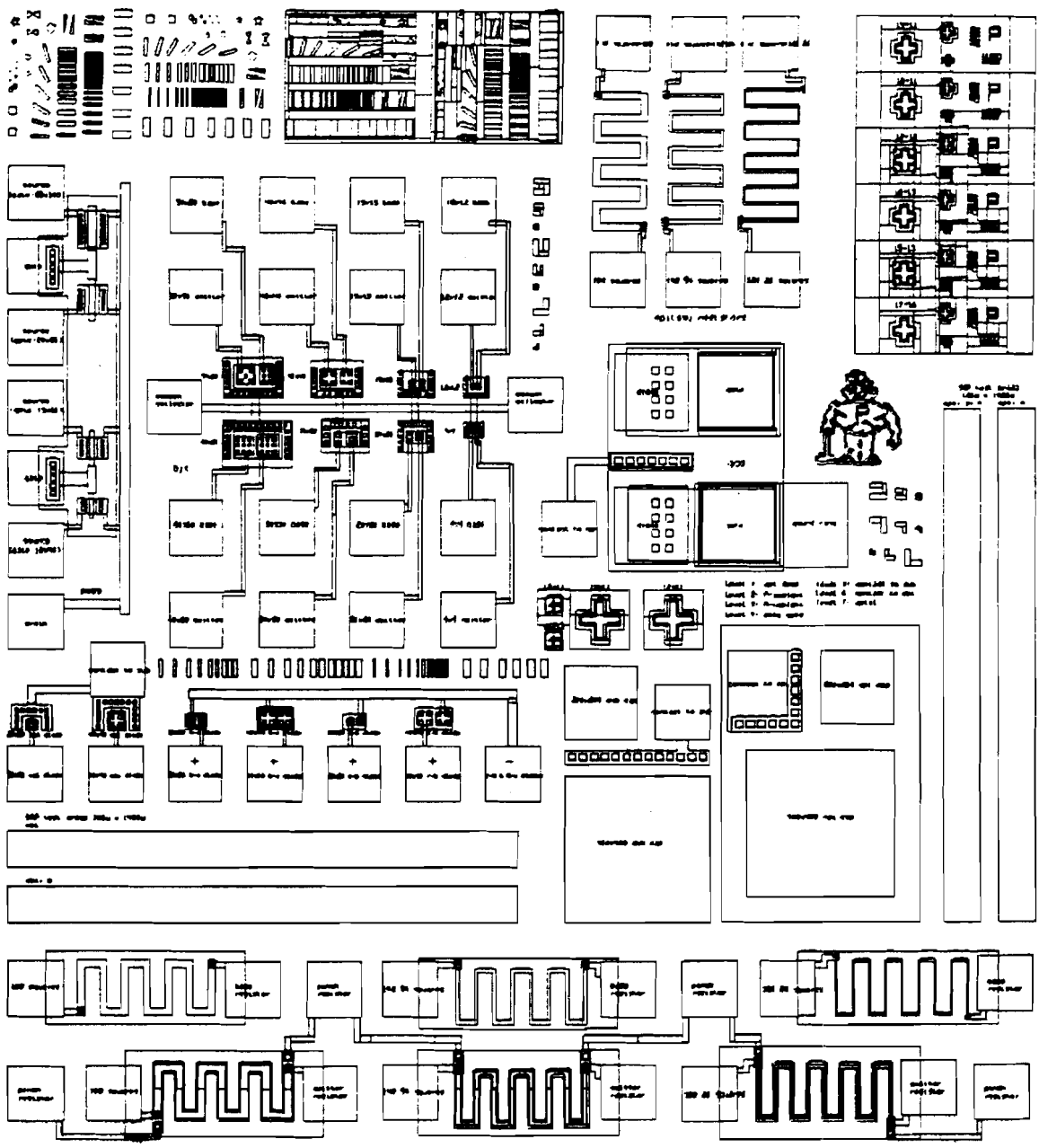


Figure 3.1 Layout of a complete die for test devices.

diodes, gate-controlled diodes, MOS capacitors, and resistors. These test devices fabricated in SEG islands are used to electrically characterize the quality of SEG material. For the diodes, ideality factors and breakdown voltages are used as criterion. In addition, BJT transistors are tested for forward dc current gains. There are two different sizes for each kind of individual diode. The dimensions for the p-type regions are 20μm x 20μm and 40μm x 40μm. There are six BJT transistors in each die with emitter sizes of 9μm x 9μm, 12μm x 12μm, 15μm x 15μm, 20μm x 20μm, 30μm x 30μm, 40μm x 40μm, 50μm x 50μm, and 60μm x 60μm. Metal pads of 150μm x 150μm are connected to contact windows for the electrical probe testing. MOS capacitors of sizes 200μm x 200μm and 400μm x 400μm can be used to verify doping densities, oxide thicknesses, and carrier lifetimes. The gate-controlled diode can be used to estimate the minority carrier lifetime. The resistors are used to evaluate resistivities and check the doping densities.

3.3 Processing

3.3.1 SEG/ELO Growth Condition

The Gemini-1 reactor at Purdue University is an induction-heated pancake reactor with capability for low temperature and reduced pressure operation. The reaction chamber mainly consists of the bell-jar and the susceptor. The quartz bell-jar measures about 21 inches in diameter and 27 inches in height. The round graphite susceptor which measures about 19 inches in diameter is located near the bottom of the bell-jar and is heated by rf induction from the coils below. Figure 3.2 shows a schematic representation of the reactor. During operation, the susceptor rotates counterclockwise at 8 rpm to smooth out any nonuniformity in gas flow, resulting in improved uniformity. Five gases are connected to the reactor: nitrogen, hydrogen, dichlorosilane, hydrochloric acid, and phosphine. The gas mixtures enter from the center of the susceptor and flow upward to the top of the bell-jar, then flow downward along the bell-jar wall. The computer-simulated streamlines in the reactor are shown in Figure 3.3 [26].

The growth experiments were carried out on p-type, 6.29 - 8.51 Ω-cm, (100) silicon substrates. Wafers were cleaned in a H_2SO_4/H_2O_2 solution, rinsed in de-ionized (DI) water, and dipped in a buffered hydrofluoric (BHF) solution. After a blow-dry with nitrogen, a 20 minute 1050°C H_2 burn oxidation produced 2100Å of oxide. Subsequently the wafers were patterned by the first-level mask. The rectangular seed patterns were

diodes, gate-controlled diodes, MOS capacitors, and resistors. These test devices fabricated in SEG islands are used to electrically characterize the quality of SEG material. For the diodes, ideality factors and breakdown voltages are used as criterion. In addition, BJT transistors are tested for forward dc current gains. There are two different sizes for each kind of individual diode. The dimensions for the p-type regions are: 20μm x 20μm and 40μm x 40μm. There are six BJT transistors in each die with emitter sizes of 9μm x 9μm, 12μm x 12μm, 15μm x 15μm, 20μm x 20μm, 30μm x 30μm, 40μm x 40μm, 50μm x 50μm, and 60μm x 60μm. Metal pads of 150μm x 150μm are connected to contact windows for the electrical probe testing. MOS capacitors of sizes 200μm x 200μm and 400μm x 400μm can be used to verify doping densities, oxide thicknesses, and carrier lifetimes. The gate-controlled diode can be used to estimate the minority carrier lifetime. The resistors are used to evaluate resistivities and check the doping densities.

3.3 Processing

3.3.1 SEG/ELO Growth Condition

The Gemini-1 reactor at Purdue University is an induction-heated pancake reactor with capability for low temperature and reduced pressure operation. The reaction chamber mainly consists of the bell-jar and the susceptor. The quartz bell-jar measures about 21 inches in diameter and 27 inches in height. The round graphite susceptor which measures about 19 inches in diameter is located near the bottom of the bell-jar and is heated by rf induction from the coils below. Figure 3.2 shows a schematic representation of the reactor. During operation, the susceptor rotates counterclockwise at 8 rpm to smooth out any nonuniformity in gas flow, resulting in improved uniformity. Five gases are connected to the reactor: nitrogen, hydrogen, dichlorosilane, hydrochloric acid, and phosphine. The gas mixtures enter from the center of the susceptor and flow upward to the top of the bell-jar, then flow downward along the bell-jar wall. The computer-simulated streamlines in the reactor are shown in Figure 3.3 [26].

The growth experiments were carried out on p-type, 6.29 - 8.51 Ω-cm, (100) silicon substrates. Wafers were cleaned in a H_2SO_4/H_2O_2 solution, rinsed in de-ionized (DI) water, and dipped in a buffered hydrofluoric (BHF) solution. After a blow-dry with nitrogen, a 20 minute 1050°C Hz bum oxidation produced 2100Å of oxide. Subsequently the wafers were patterned by the first-level mask. The rectangular seed patterns were

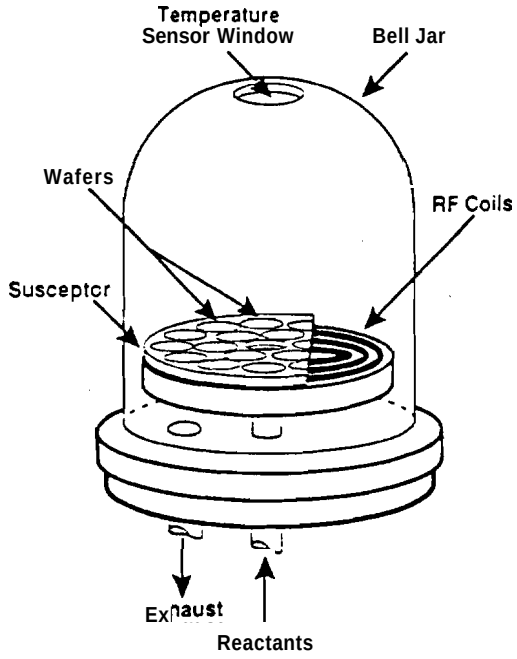


Figure 3.2 Schematic diagram of an induction heated pancake reactor [26].

Figure 3.3 Streamlines in the reactor for H_2 = 60 slm and SiH_2Cl_2 = 0.22 slm. The susceptor temperature is 950°C and the pressure is 150T [26].

Table 4
Process sequence for silicon epitaxial growth.

Process Step	Ambient	Comments
Load clean wafers into the reactor	Atmosphere	
Nitrogen purge and fill with hydrogen (pump down to the desired pressure)	Hydrogen	Remove all oxygen
Hydrogen bake	Hydrogen	Heat up to the bake temperature to remove native oxide
HCI etch	HCl in hydrogen	Expose atomically clean surface
Deposition	DCS and dopant in hydrogen	Deposit epitaxial film with optional in-situ doping
Cool-down	Hydrogen	DCS/HCl/rf generator are off
Purge out hydrogen and fill with nitrogen	Nitrogen	Remove all hydrogen
Unload wafers	Atmosphere	

final wet oxidation/drive was performed at 1000°C for 20 minutes. Figure 3.4 shows a SUPREM-III simulated n-p-n doping profile for the test bipolar transistor. SUPREM-III program was used to simulate the doping profiles and to estimate oxide thicknesses at various points in the process.

The contact windows to the silicon epitaxial layers were defined with AZ-1350 positive photoresist using mask level six, and these windows were opened by BHF wet etching. Then metal patterns were defined with the last (seventh) mask in AZ-1350 photoresist. Subsquently Al-1%Si was deposited over the wafer surface by sputtering in the Perkin-Elmer model 2400 sputtering system. This metallization step was toward the end of the process. The aluminum contains 1% silicon in order to prevent aluminum spiking. The metallization etch used the "lift-off' technique. After the lift-off etch in acetone, the metal was annealed at 400°C in nitrogen for 15 minutes to create good metal/silicon contacts. The test BJT process flow is illustrated in Figure 3.5.

3.4 Evaluation Methods for SEG/ELO

3.4.1 Morphology

Generally, the morphology of SEG/ELO structures can be observed by three techniques: optical microscopy, scanning electron microscopy (SEM), and transmission electron microscopy (TEM). The maximum magnification values of these three methods are 1000x, 100000x, and 500000x, respectively. Nomarski interference contrast microscopy and SEM were used in this epitaxial growth experiment to determine the surface morphology and imperfections.

3.4.1.1 Nomarski

Optical microscopy is one of the simplest methods to get valuable information of the surface morphology of SEG/ELO. An Olyrnpus BH-2 microscope whose magnification values are 150x and 750x is used in this experiment. The use of Nomarski illumination enhances the ability to observe surface morphology so that step heights as small as 30-50Å can be detected. Under illumination in the Nomarski contrast mode, light passes through a polarized prism and then through two connected birefringent (Wollaston) prisms positioned so that their optical axes are perpendicular. This configuration splits the illuminating beam into two mutually perpendicular polarized beams. The two beams strike the surface of the

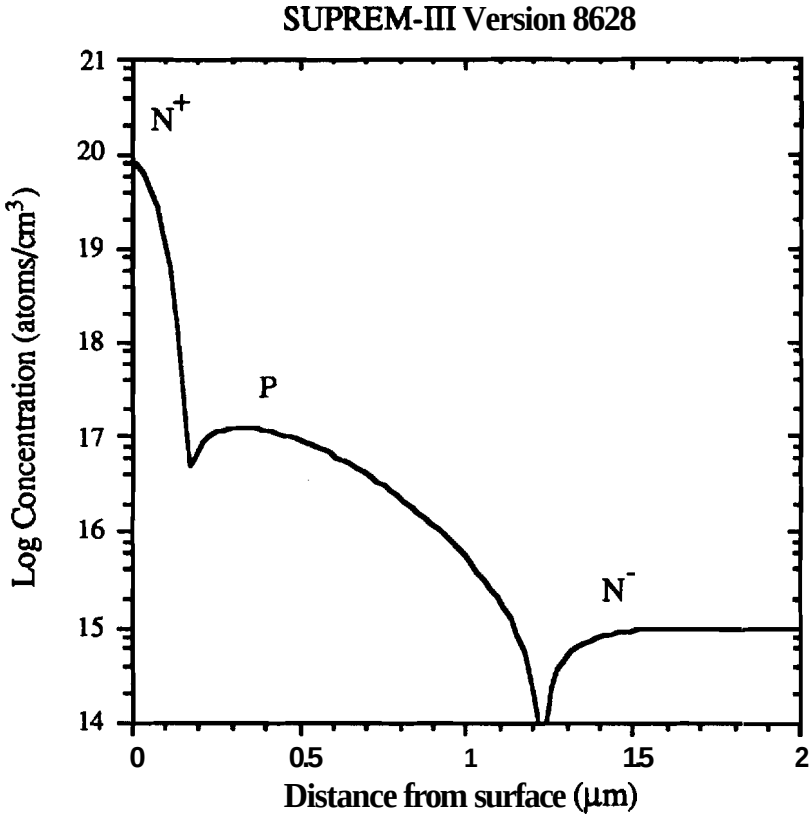


Figure 3.4 SUPREM III simulated plot of net chemical impurity concentration versus depth into the structure for the test device process.

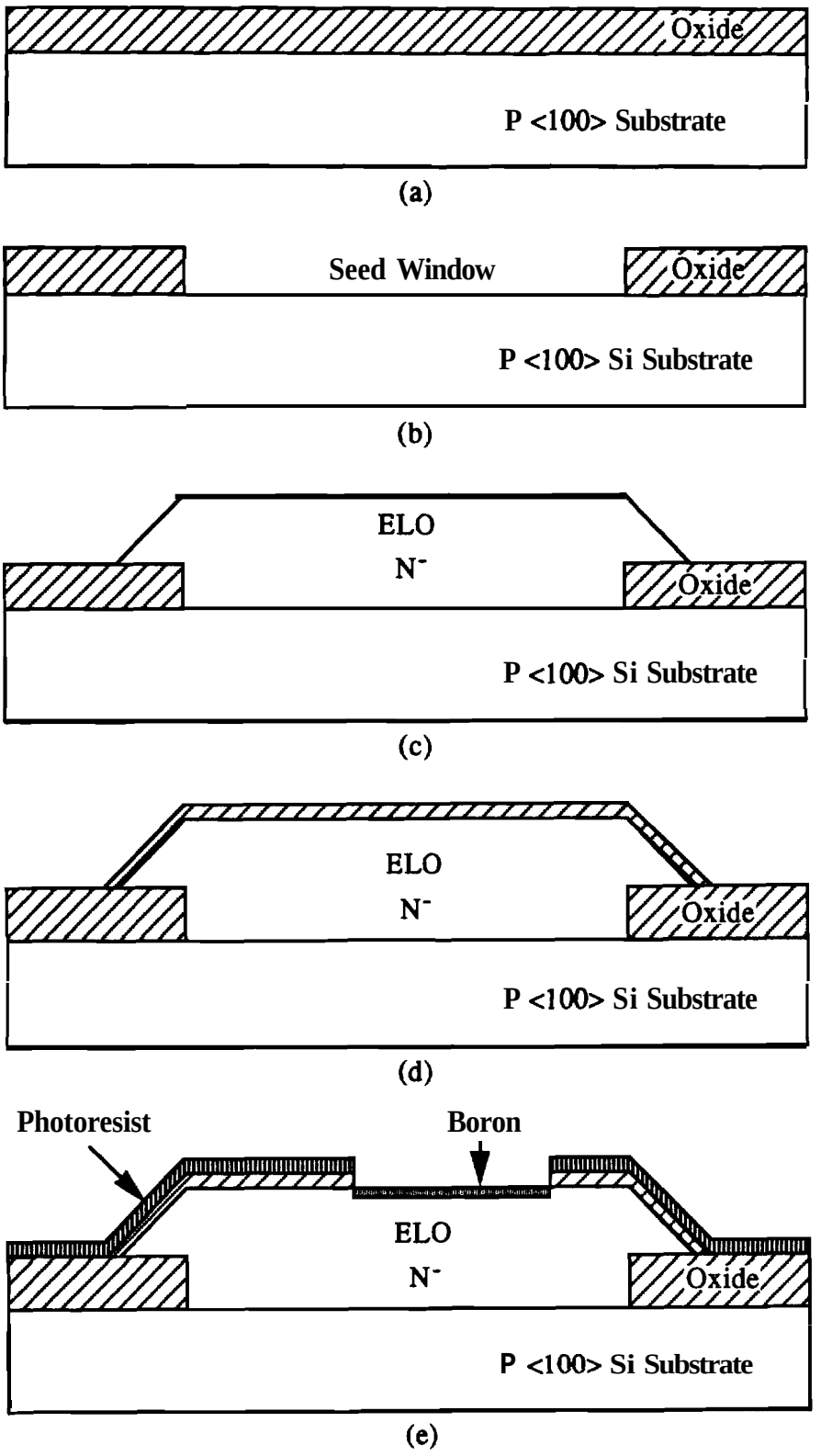
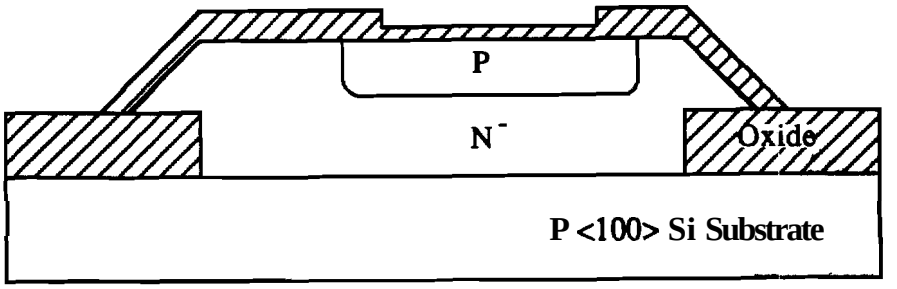
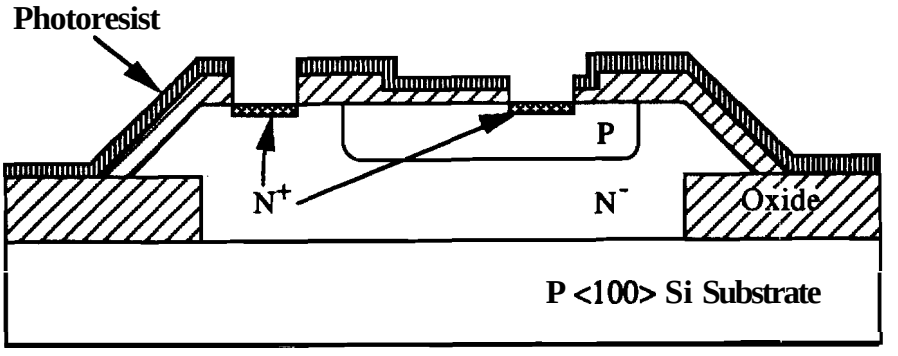


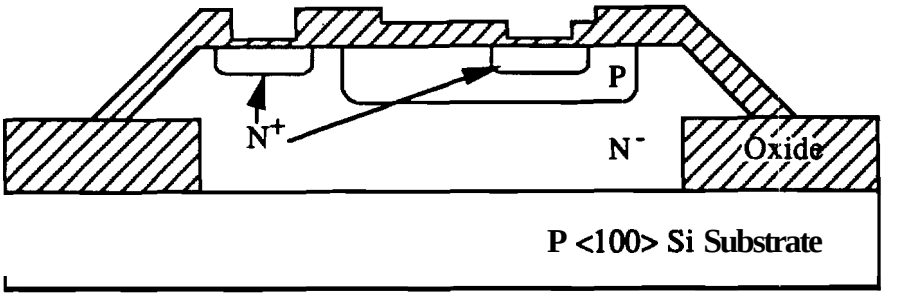
Figure 3.5 Test ELO BJT fabrication process flow.



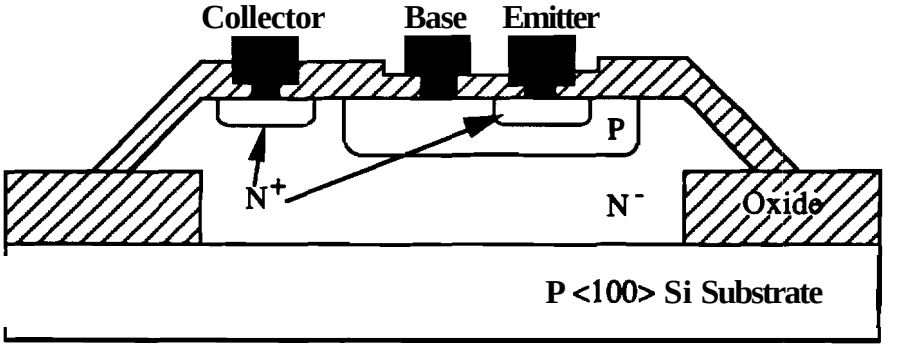
(f)



(g)



(h)



(f)

Figure 3.5 (continued)

wafer a short distance apart, and are then reflected back into the microscope and recombined by passing through the Wollaston prism again and through an analyzer. Different intensities can be detected if differences in optical path length of the two beams are encountered. Steps or refractive index changes can cause such differences. The Nomarski interference contrast microscopy is therefore used to view details on the SEG/ELO surface, such as stacking faults and pits which often cannot be observed in ordinary illumination. The adjustments of the polarizer, analyzer, and prisms can be set to produce maximum interference contrast for Nomarski illumination.

3.4.1.2 SEM

SEM is also an important technique and is widely used to analyze the surface morphology and structures of SEG/ELO samples. In SEM, a heated tungsten filament is used to create a beam of electrons that is accelerated, focused to a small diameter, and rastered across the surface of the sample while a cathode ray tube (CRT) is scanned in synchronism. Electrons striking the surface produce secondary electrons whose intensity pattern in displayed on the CRT. The image contrast between surface features is created due to differences in atomic number and work function as well as in surface morphology. SEM analysis can provide much higher magnification, better resolution, and depth of the field than optical microscopy.

3.4.2 Film Thickness

There are both destructive and nondestructive methods available for the accurate measurement of the thickness of the silicon epitaxial layer. Since there are steps in the oxide on ELO structures, nondestructive step-height measurements with a Tencor Alpha-Step 200 profilometer are used in this experiment. This simple and rapid method is to use a mechanical stylus to run across the step and measure the height. A video microscope and a 9" video monitor are used for precisely positioning the wafer under the stylus. The depth of the seed holes was measured prior to the epitaxial growth. Thus, the epitaxial layer thickness is the sum of the depth of the seed hole and the step height of the ELO over the oxide,

3.4.3 Diodes

Following fabrication, base-emitter and base-collector diodes were tested using an HP4145A Semiconductor Parameter Analyzer with a probing station. Reverse-bias and forward-bias I-V data characteristics were obtained. Ideality factors and reverse leakage currents of the diodes were measured and calculated to gain an insight into the material quality of SEG grown at different conditions. Junction reverse-bias leakage currents were measured at -1.5V. The slope of the forward-bias curve determines the junction ideality factor, η, by the relationship

$$I = I_0 e^{qV_A/\eta kT} \tag{3.1}$$

where I_0 is the saturation current, q is the electron charge, V_A is the applied voltage, k is the Boltzmann's constant, and T is temperature. Taking a natural logarithm yields

$$\ln I = \ln I_0 + \frac{qV_A}{\eta kT} \tag{3.2}$$

Hence ideality factor can be calculated from the slope of ln(I) versus V_A plot. Figure 3.6 shows a forward-biased current-voltage characteristics of a diode. η=1 indicates diffusion current domination over recombination current and leads to good material quality with low defect density. However, when η approaches 2, recombination current dominates and poor material quality with high defect density is indicated.

3.4.4 Bipolar Junction Transistor

For NPN bipolar transistors, ideality factors and reverse leakage currents of the base-emitter and base-collector junctions were tested first. Subsquently the transistors were tested in the common emitter configuration. The Early-voltages were measured by extrapolation from the common emitter curves. Then the forward DC current gain, β, over a range of collector currents were measured with V_{BC} =0 while incrementing V_{BE} from 0 to 1 volt. β can be calculated from the collector and base DC currents at each tested V_{BE} value as

$$\beta = \frac{I_C}{I_B} = \frac{I_C}{I_E - I_C} \tag{3.3}$$

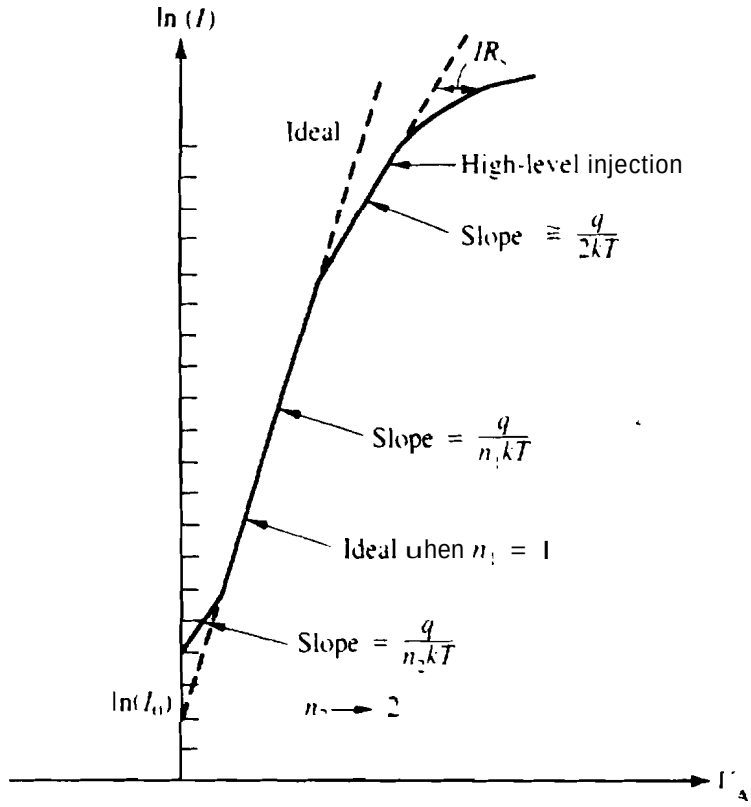


Figure 3.6 Forward-biased current-voltage characteristics of a diode [71].

The maximum beta of a transistors can be obtained from β versus $\ln(I_C)$ plot. Since breakdown has been shown to affect junction/oxide interface quality, the breakdown voltages of the base-emitter and base-collector junctions, BV_{EBO} and BV_{CBO} respectively, were measured from the reverse-biased I-V curves after all other measurements were taken.

3.4.5 Resistivity and Doping Concentration

The resistivity and doping concentration of the epitaxial layer are two of the primary concerns for the doping runs. Several measurement methods, such as four-point probe, capacitance-voltage, and spreading resistance profiling (SRP), are generally used to determine the doping concentration in the epitaxial layer.

3.4.5.1 Four-Point Probe Measurement

The four-point probe is the easiest and the most widely used method of measuring the doping concentration in the semiconductor materials. The sheet resistance of the n-type epitaxial layer grown on p-type substrate can be measured by the four-point probe. Since the epitaxial layer, R_s, is of opposite impurity type to the substrate, the current will be restricted within it. A four-point probe station and a Unicorp 1900 digital resistivity test set were used for measurements. Four equally spaced collinear probes are placed on the layer. A fixed current is passed through the two outer probes, and the resulting voltage across the outer probes is measured. Then sheet resistance reading is shown on the digital display. Since the thickness of the epitaxial layer, t, is known by a thickness measurement and is much smaller than the probe spacing, the resistivity, p, can be obtained from the product of sheet resistance by thickness of the epitaxial layer as

$$\rho = R_s t \tag{3.4}$$

Figure 3.7 gives the resistivity of n- and p-type silicon as a function of doping concentration [72]. Once the resistivity is obtained, Figure 3.7 is used to convert the resistivity to the corresponding doping concentration in the epitaxial layer.

3.4.5.2 Resistors

Three serpentine resistors of different dimensions in each die were fabricated. For each resistor, the resistance can be easily measured using an HP4145A with a probing

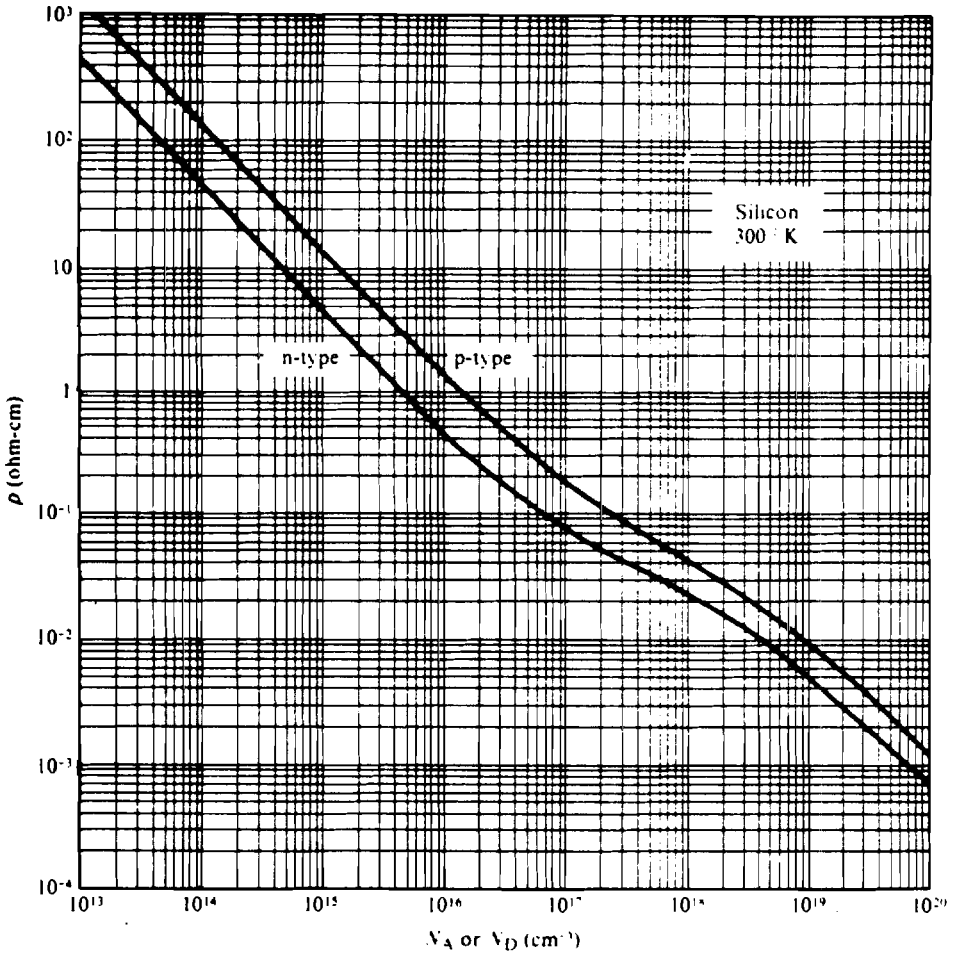


Figure 3.7 Resistivity versus doping concentration at room temperature for p-type (boron-doped) **and n-type (phosphorus-doped) silicon** [72].

station. The sheet resistance can be calculated by dividing the number of squares, and therefore resistivity and doping concentration of the epitaxial layer can be obtained.

3.4.5.3 Capacitance-Voltage Measurements

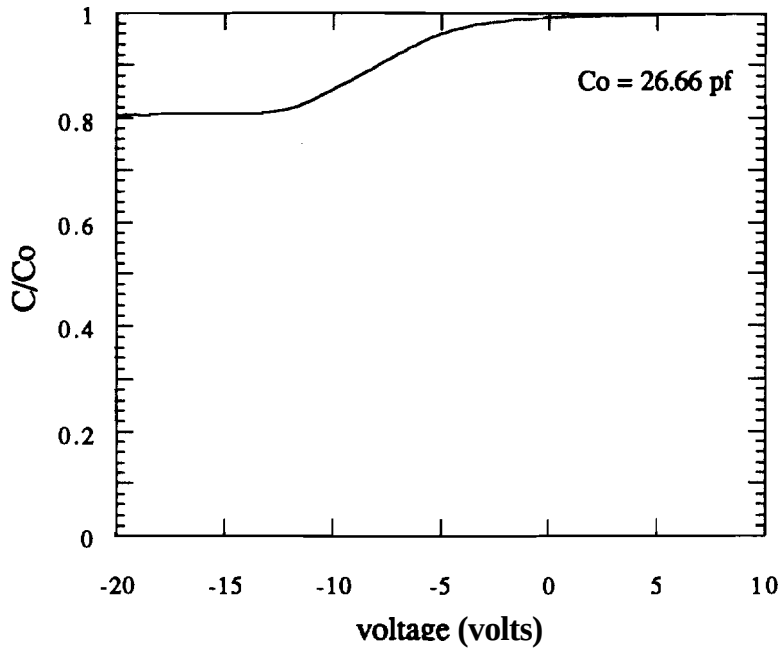
Two MOS capacitors of different dimensions, 200μm x 200μm and 400μm x 400μm, were fabricated on the epitaxial layer in each die. The doping concentration in the epitaxial layer can be determined by the C-V technique using the MOS capacitors. The capacitors were tested using a probing station and an HP4275A multi-frequency LCR meter which was controlled by an HP 9000 series 236 computer. The measured C-V data were then downloaded into a mainframe computer on the Purdue Engineering Computer Network (ECN). The relationship between the carrier concentration N and the capacitance C resulting from a reverse voltage V can be expressed as

$$N = \frac{2}{q\varepsilon A^2[d(1/C^2)/dV]} \qquad (3.5)$$

where q is the electric charge, ε is the dielectric constant, and A is the area of the capacitor. Figure 3.8 (a) shows C-V data characteristics derived from a representative MOS-capacitor. Then $1/C^2$ versus V curve was plotted and the slope of $d(1/C^2)/dV$ in the depletion biasing region was taken as shown in Figure 3.8 (b). Therefore, the doping concentration can be obtained from the slope of the $1/C^2$ versus V plot using Eq. (3.5).

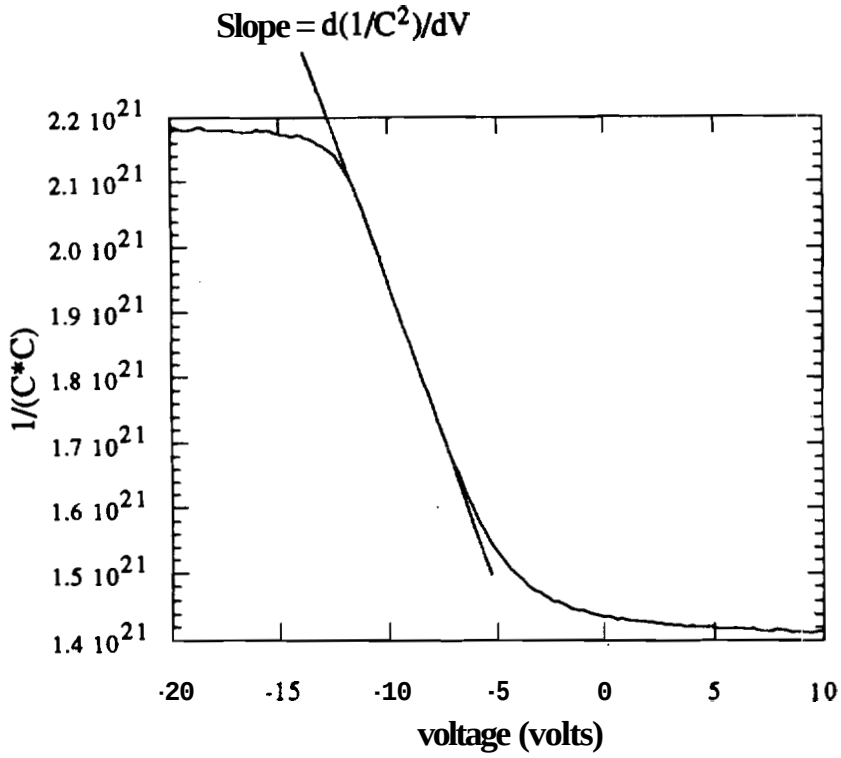
3.4.5.4 Spreading resistance profiling

Spreading resistance profiling (SRP) is a technique to generate a resistivity and a doping profile. It has applicability over a broad range of dopant concentration (10^{14}-10^{20} atoms/cm^3). Using this technique, the junction depth and doping concentration can be verified. The sample is mounted on a bevel block with melted wax. Bevel angles of 15' to 5° are typical. Two carefully aligned probes step along the sample surface and the resistance between the probes is measured at each location. Then the measured spreading resistance data can be converted to doping concentration. It is very useful to keep an oxide layer on the sample. The oxide provides a sharp comer at the bevel and clearly defines the start of the beveled surface because the spreading resistance of the oxide is very high [73].



(a)

Figure 3.8 (a) Measured capacitance-voltage characteristics of a representative MOS-C (#506-1).



(b)

Figure 3.8 (b) corresponding $1/C^2$ versus V curve.

CHAPTER 4: CHARACTERIZATION OF SEG/ELO

4.1 Introduction

The trend for growing SEG/ELO is toward lower deposition temperatures, shorter temperature cycles, and lower system pressures to get more uniform epitaxial films and to minimize autodoping and pattern shift. To obtain the characteristics desired in the SEG/ELO material, many considerations must be weighed in deciding the deposition parameters. SEG/ELO material quality, morphology, doping concentration, and the dependence of growth rates on deposition parameters such as temperature and pressure, are important factors which can affect the electrical characteristics of devices. More than fifty epitaxy runs, including both undoped and doped runs, have been accomplished using the Gemini-1 pancake reactor which is housed in the Purdue University Epitaxy Laboratory. By characterizing the SEG/ELO films grown at different conditions, regions of operation for this Gemini-1 pancake reactor can be defined. SEG/ELO growth rate characteristics, doping concentration, and electrical evaluation of the test devices built in SEG/ELO are presented in this chapter.

4.2 Growth Rate Characteristics

The primary parameters that are typically controlled during the silicon epitaxial growth are the thickness or its time derivative, growth rate, and resistivity of the layer. Therefore, the first attention is paid to the growth rate uniformity across a wafer at different deposition conditions in this work. The experiments discussed in this section attempted to investigate the dependence of growth rates on growth temperatures and pressures in order to get an optimum set of perimeters where non-uniformities could be minimized

Growth rate or thickness uniformity is generally imperative so that thickness dependent properties can meet specifications and so that the subsequent processes can be properly controlled. In epitaxial growth, the reactants must be transported to the exposed

silicon surface and then incorporated into the crystal lattice. The growth rate is limited by either the rate of transport or by the surface reaction rate. Therefore, the growth rate can be a function of temperature, pressure, gas composition, and substrate orientation.

In this experiment, silicon selective epitaxial growth was conducted in the $SiCl_2H_2$-HCl-H_2 system at temperatures ranging from 820° to 1020° C and with system pressure in the range of 40 to 150 Torr. Hydrogen is the carrier gas, dichlorosilane:(DCS) supplies the silicon source, and HCl provides in-situ cleaning to prevent the formation of polysilicon on the oxide. The growth was carried out on two-inch (100) p-type wafer!;. Wafer preparation and cleaning procedures before deposition as described in Section 3.3.1 were repeated for every epitaxy run. Oxide-patterned wafers were placed in the mid-point between the center and the perimeter of the susceptor with their rectangular seed patterns oriented along the radial direction of the susceptor. Figure 4.1 schematically shows the wafer location on the susceptor.

After epitaxial growth, thickness of the SEG/ELO films was measured using a Tancor Alpha-Step 200 profilometer. During deposition, the largest growth rate variation across a wafer was expected to exist in the radial direction of the susceptor since susceptor rotation could not smooth out any nonuniformity in this direction. Therefore, thickness measurements were taken at seven different points in this direction, as shown in Figure 4.2, to get a fairly representative of growth rate uniformity in a wafer. The seed window dimension and location within a die were chosen identical for each measurement point.

4.2.1 Dependence of Temperature

The temperature dependence of silicon epitaxial growth from DCS has been studied by many researchers. As discussed in Section 2.1.1, growth mechanism is surface reaction limited when temperature is below about 950°C. Therefore the growth rate of low temperature silicon epitaxial growth is limited by reaction kinetics at the: silicon surface and does depend on temperature. In general, growth rate decreases with decreasing temperature for low temperature silicon epitaxy.

In this epitaxy experiment, depositions conducted at different temperatures and system pressures required different HCl and DCS gas flow rates, as well as HCl/DCS ratio, in order to get good selectivity and device quality epitaxial films. Hence only the growth rate profiles across the wafer instead of absolute growth rates could be compared directly.

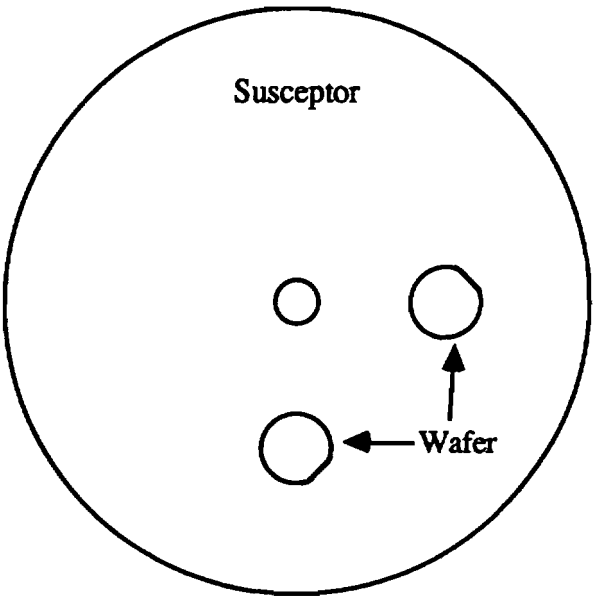


Figure 4.1 Wafer locations on the susceptor.

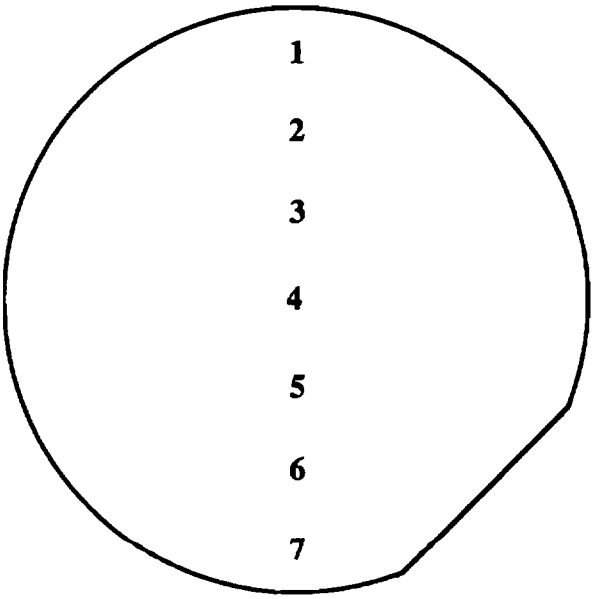


Figure 4.2 Positions of measurement points on a wafer.

Figure 4.3 (a)-(c) illustrate selective epitaxial growth rate profiles on oxide-patterned wafers at various deposition temperatures when system pressures were kept at 150 Torr, 95 torr, and 40 Ton, respectively. At same pressure, growth rate profiles were affected by temperature and the uniformity across the wafer was much better at lower deposition temperature. Since the low temperature epitaxial growth is in the reaction-controlled regime and lower deposition temperature slows the surface reaction rate, improvement in growth rate uniformity can be achieved by lowering the deposition temperature.

Growth rate change along the radial direction was observed. In general, growth rates dropped from inner positions towards the perimeter of the wafer. There was no masking oxide thickness dependence on these growth rate profile comparisons, because masking oxide thickness measured by profilometer was fixed at about 2100Å for each epitaxy run. In addition, since the seed window dimension at each measurement point was identical, there was no "loading effect" on these profile comparisons either.

4.2.2 Dependence of Pressure

Reduced-pressure silicon selective epitaxial growth has been accomplished in the pressure range from 40 Torr to 150 Torr in this experiment. It was observed that growth rate uniformity was influenced by the pressure. Figure 4.4 (a)-(c) present selective epitaxial growth rate profiles across the wafers obtained for depositions at various pressures while the temperatures were maintained at 970°C, 920°C, and 870°C, respectively. Growth rate profile was more planar and smoother as the deposition pressure decreased. The ratios of standard deviation to mean growth rate were normally less than ±3.3% for the 40 torr epitaxy runs. Surface morphology of the epitaxial films grown at 40 Torr looked good when observed using a microscope with Nomarski illumination or with SEM. No stacking faults were observed in these 40 Ton runs.

At the lower deposition pressure, gas density was lower and the diffusivities of the gaseous reactive species became substantially larger since diffusivities varied inversely with pressure. In addition, the gas flux associated with the deposition reaction at the surface was smaller than the diffusive flux of the reactants to the surface. Hence the epitaxial growth was controlled by the deposition reaction at the surface and became independent of the gas flow pattern. Consequently, better growth rate uniformity was achieved at lower deposition pressures.

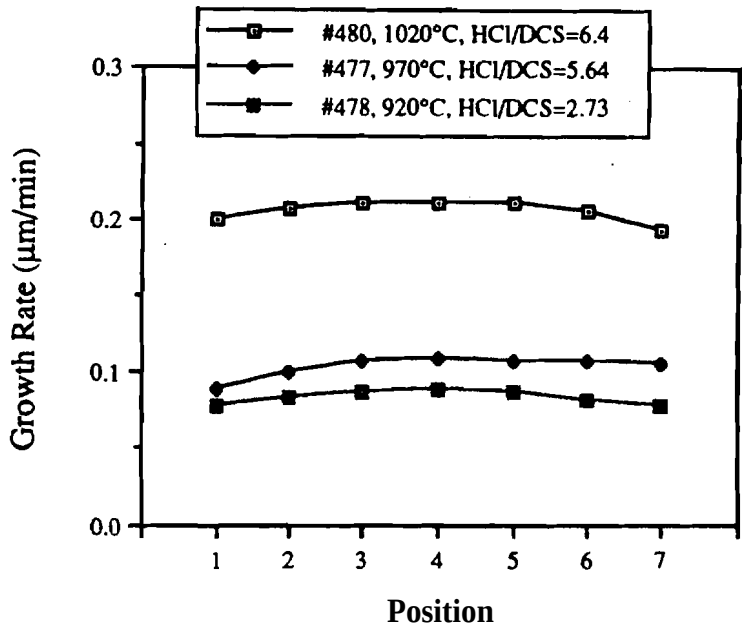


Figure 4.3 (a) Selective epitaxy growth rate profiles on oxide-patterned wafers at 150 Torr and various temperatures.

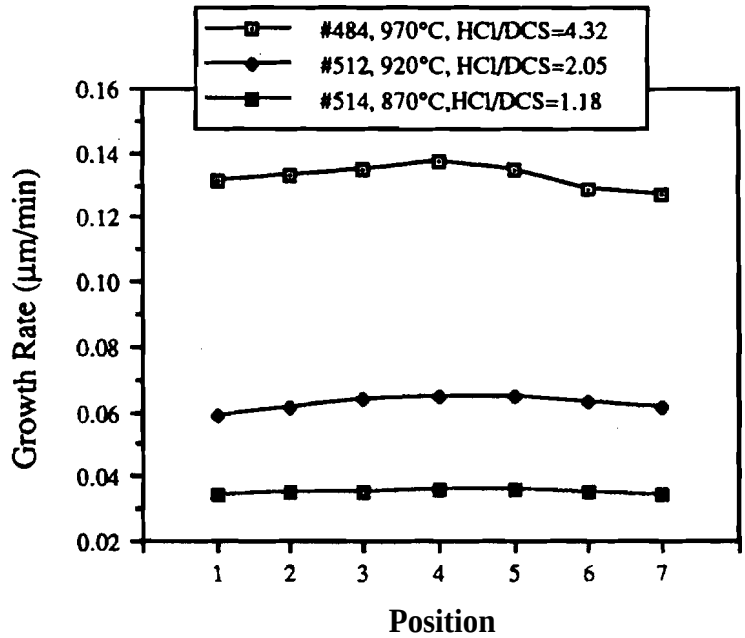


Figure 4.3 (b) Selective epitaxy growth rate profiles on oxide-patterned wafers at 95 Torr and various temperatures.

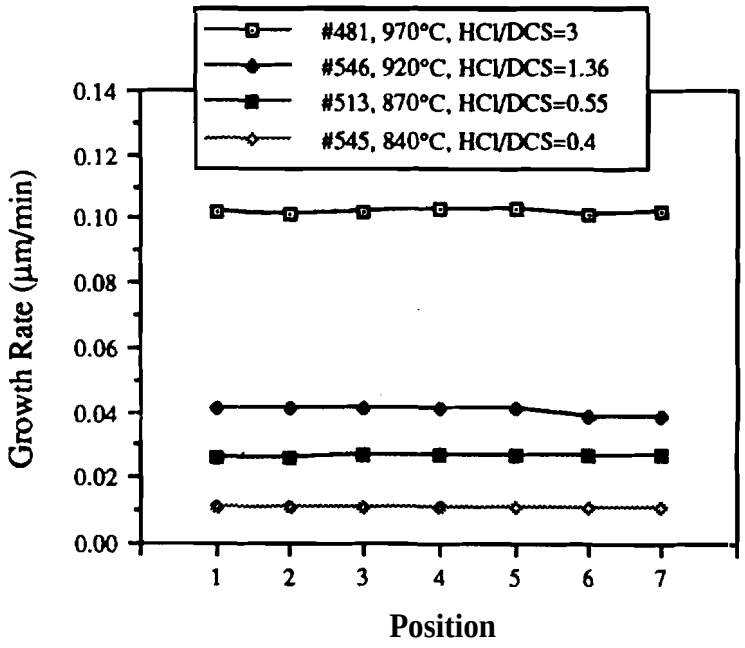


Figure 4.3 *(c)*Selective epitaxy growth rate profiles on oxide-patterned wafers at 40 Torr and various temperatures.

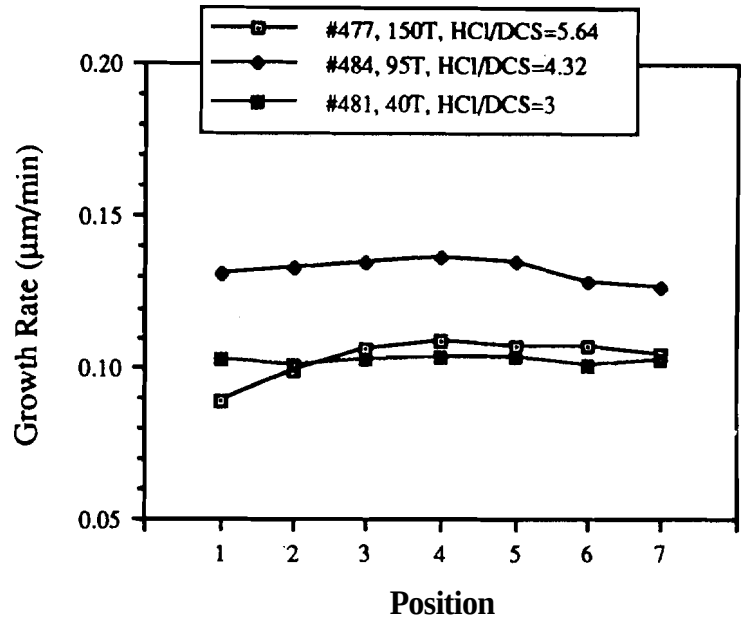


Figure 4.4 (a) Selective epitaxy growth rate profiles on oxide-patterned wafers at 970°C and various pressures.

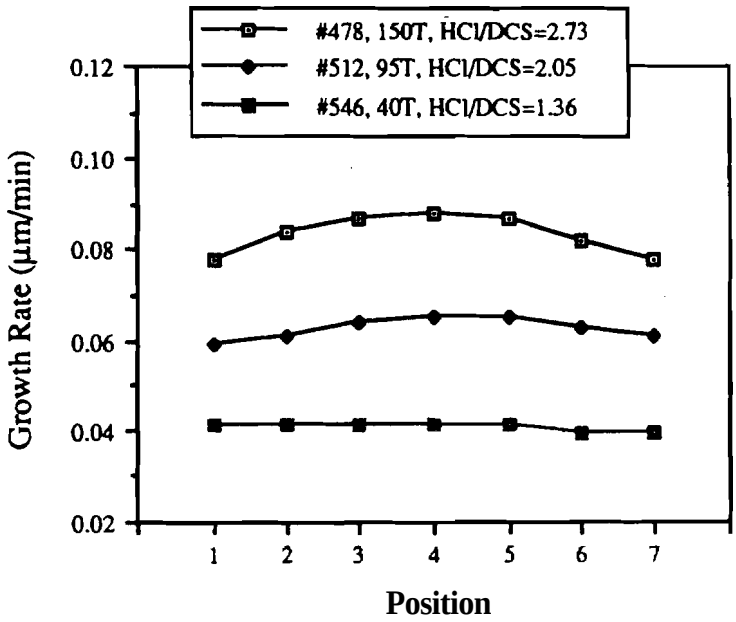


Figure 4.4 (b) Selective epitaxy growth rate profiles on oxide-patterned wafers at 920°C and various pressures.

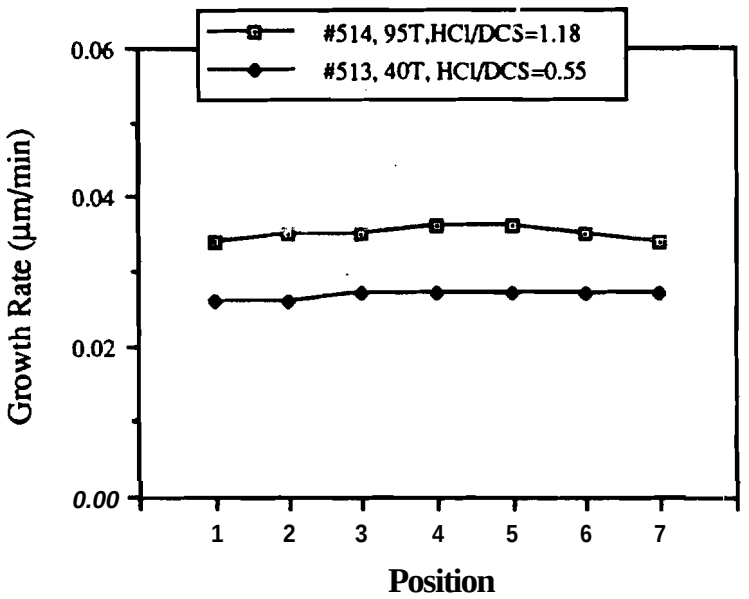


Figure 4.4 (c) Selective epitaxy growth rate profiles on oxide-patterned wafers at 870°C and various pressures.

Appendix-B presents a summary of all epitaxy runs which were conducted at low temperatures and reduced pressures. The mean value and the standard deviation of measured growth rates across a wafer were calculated. %Non-uniformity of each epi wafer was defined as

$$\%\text{Non-uniformity} = \frac{GR_{max} - GR_{min}}{GR_{} + GR_{min}} \times 100\% \qquad (4.1)$$

where GR_{max} and GR_{min} were the maximum and minimum growth rates across a wafer, respectively. From this definition and the ratio of standard deviation to mean growth rate, growth rate uniformities of different epitaxy run could be quantitatively compared.

4.2.3 Dependence of Inject Tube Size

In this experiment, a larger inject tube was used for several epitaxy runs to investigate the effect of inject tube size on growth rate. Growth rates and the ratios of standard deviation to mean growth rate using the large inject tube were compared to the average values of those using the regular inject tube. Lower growth rates and better growth rate uniformities were observed for using the large inject tube. A growth rate and uniformity comparison of using different size inject tubes at 970°C-40T was presented in Table 5, and the numbers were the average values over several runs. Since the total gas flow rate was fixed, the gas velocity decreased inversely proportional to the cross-section area of the inject tube. With lower gas velocity, the supply of the reactive species decreased, resulting in lower surface concentrations and lower surface reaction rates. Therefore, the growth rates were lower and better uniformities were obtained.

Table 5
Effect of inject tube size on growth rate.

Temp. (°C)	Press. (Torr)	HCl/DCS	Doping (%)	Ave.G.R. (μm/min)	Std.Dev./Ave.G.R. (%)	Comments
970	40	3	0	0.077	1.3	large inject tube
970	40	3	0	0.090	1.8	small inject tube

4.2.4 Wafer to Wafer Growth Rate Uniformity

Wafer to wafer growth rate uniformities were examined in this experiment. In each epitaxy run, two wafers were placed in the similar positions as shown in Figure 4.1. The selective epitaxial growth rates across each wafer were measured and the mean values were calculated. The average growth rate for each wafer in same run was compared. %Error was defined as

$$\%\text{Error} = \frac{\overline{GR_{max}} - \overline{GR_{min}}}{\overline{GR_{max}} + \overline{GR_{min}}} \times 100\% \qquad (4.2)$$

where $\overline{GR_{max}}$ and $\overline{GR_{min}}$ were the maximum and minimum average growth rates of wafers in the same run, respectively. Smaller %error value suggested better uniformity on the susceptor and better repeatability of the system. Table 6 summarized this wafer to wafer growth rate comparison at various deposition conditions. Especially at lower pressures, good wafer to wafer uniformities were observed. For 40 torr and 95 torr runs, wafer to wafer uniformities always varied less than ±4.7%.

4.2.5 Dependence of Doping

The Gemini-1 pancake reactor in the Purdue University Epitaxy laboratory is capable of growing in-situ n-type doped silicon epitaxial films. This is achieved by introducing phosphine (PH_3) gas into the reactor during epitaxial deposition, while hydrogen is the carrier gas and dichlorosilane (DCS) supplies the silicon source. This in-situ doping technique is attractive because it allows us to control doping profiles in silicon epitaxial structures. In addition, it eliminates a conventional doping step which is normally accomplished by post-deposition ion implantation or thermal diffusion.

An automatic dopant control system with three automatic flow controllers in the Gemini-1 reactor was utilized to control the dilution and injection rate of phosphine gas used during deposition. The dopant set point is a percentage of 300 sccm. Assuming system dopant set point is at 20%, the actual flow at this setting is calculated as:

$$\frac{\text{Inject Flow \&}}{\text{Source Flow}} = \frac{20}{100} \times 300 \text{ sccm} = 60 \text{ sccm} \qquad (4.3)$$

Table 6

Wafer to wafer growth rate comparison.

Run#	Temp (°C)	Press. (T)	HCl/DCS	Ave. G. R. (μm/min)	% Error
480	1020	150	6.4	0.214	3.7
533	1020	150	6.4	0.199	1.5
477	970	150	5.64	0.113	8.4
484	970	95	4.32	0.136	2.2
511	970	95	4.32	0.111	1.8
481	970	40	3	0.1	2.5
510	970	40	3	0.081	1.9
522	970	40	3	0.093	3.2
478	920	150	2.73	0.088	5.7
541	920	150	2.73	0.039	3.9
548	920	150	2.73	0.054	2.8
485	920	95	2.05	0.083	1.2
512	920	95	2.05	0.064	1.6
547	920	95	2.05	0.051	3.9
482	920	40	1.36	0.054	4.7
546	920	40	1.36	0.039	2.6
514	870	95	1.18	0.034	4.4
544	870	95	1.18	0.025	4
501	870	40	0.55	0.027	0
513	870	40	0.55	0.028	1.8
545	840	40	0.4	0.012	4.3

The doped epitaxy runs at 1020°C-150T, 970°C-150T, 970°C-40T, 920°C-150T, and 920°C-40T were carried out. The dopant set points of 20%, 40%, 60%, and 80% were used at each of these deposition temperatures and pressures. As same as the thickness measurements for the undoped runs, seven points on each wafer of these doped runs were measured using the profilometer. At each growth temperature and pressure, the HCl/DCS ratio was kept unchanged for various dopant set points. Hence the growth rates at different dopant set points were compared first to see the effect of doping on growth rate. A plot of growth rate versus dopant set point at different deposition conditions was shown in Figure 4.5. Dopant set point of 0% represented the undoped runs in this figure. It was seen that growth rates did not consistently vary with increases of phosphine (n-type dopant) percentage. No significant dependence of doping with phosphine on growth rate was observed. Therefore, in-situ n-type doped selective epitaxial films could be obtained at a growth rate similar to that of undoped epitaxy.

When PH3 dopant set points varied from 0% to 80%, the growth rate profiles for depositions at 1020°C-150T, 970°C-150T, 970°C-40T, 920°C-150T, and 920°C-40T were illustrated in Figure 4.6 (a)-(e), respectively. No significant deterioration of growth rate uniformities was found in the presence of phosphine. Growth rate uniformities of 40 torr undoped runs were observed slightly better than those of 40 torr doped runs. Morphology of doped SEG/ELO grown at 40 torr looked good under microscope with Nomarski illumination. For 150 torr runs, the surface of doped SEG/ELO did not look as good as that of undoped films. A few edge defects and stacking faults were seen on the n-type doped SEG/ELO deposited at 150 torr by using a Nomarski microscope.

4.3 Measurements of Doping Concentration

Most research on silicon epitaxial growth was focused on undoped deposition and limited results were published for in-situ phosphorus doping during selective epitaxial growth at low temperature and reduced pressure. Hence in addition to growth rate, doping concentration of SEG/ELO was another concern in this experiment. Doping concentrations of SEGELO grown at various deposition conditions were determined by resistors, capacitors, and four-point probe measurements. The results of these rneasurements were presented in this section.

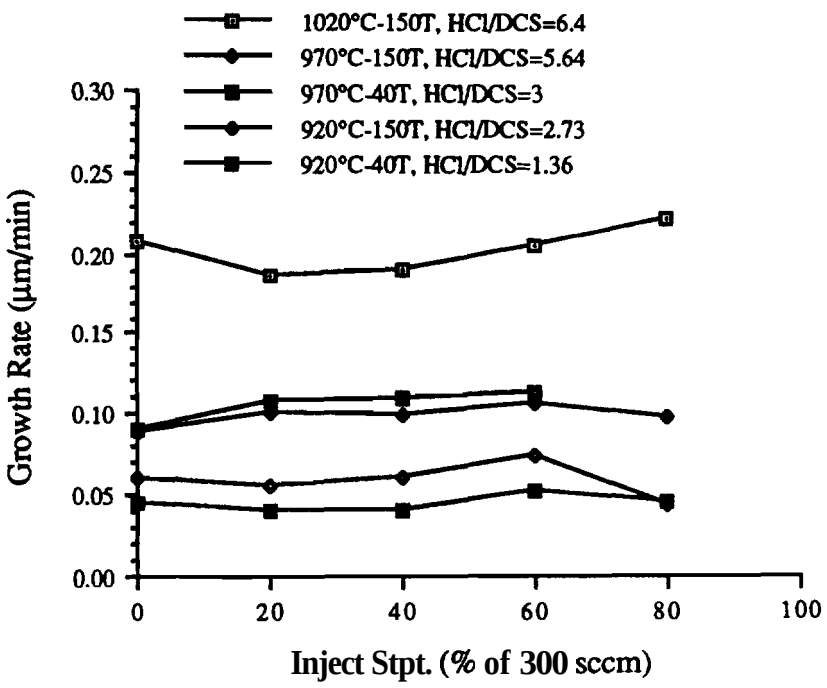


Figure 4.5 Silicon selective epitaxy growth rates vs. PH3 dopant set points at various deposition conditions.

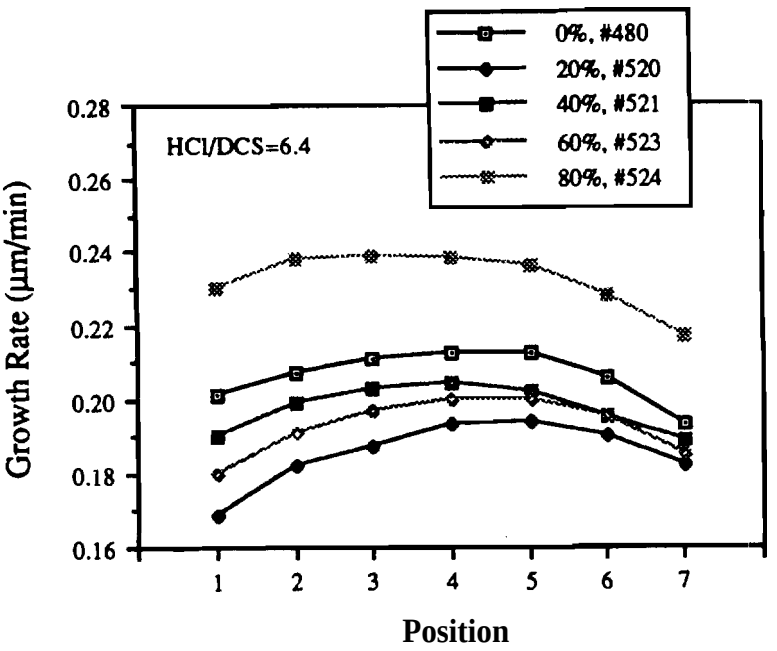


Figure 4.4 (a) Selective epitaxy growth rate profiles on oxide-patterned wafers at 1020°C, 150T, and various PH3 dopant set points.

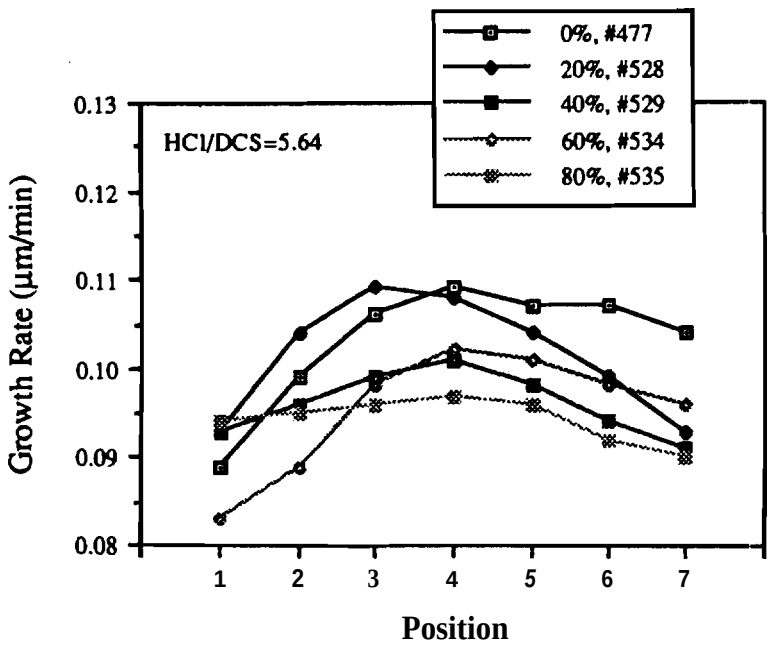


Figure 4.6 (b) Selectiveepitaxy growth rate profiles on oxide-patterned wafers at 970°C, 150T, and various PH3 dopant set points.

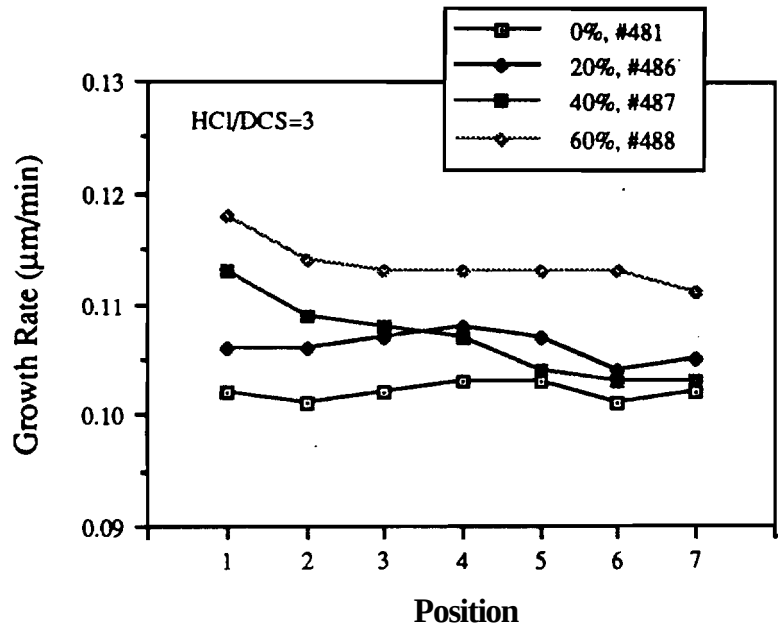


Figure 4.6 (c) Selective epitaxy growth rate profiles on oxide-patterned wafers.at 970°C, 40T, and various PH3 dopant set points.

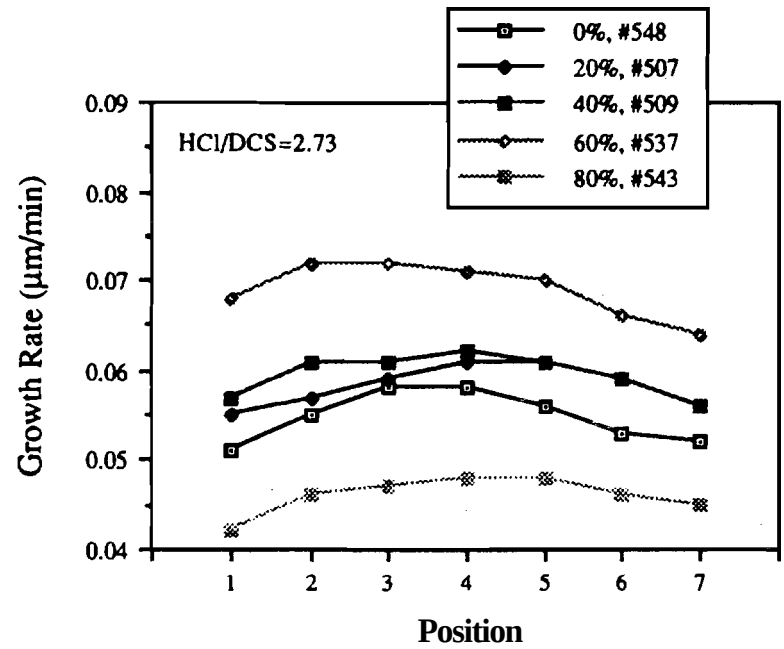


Figure 4.6 (d) Selective epitaxy growth rate profiles on oxide-patterned wafers at 920°C, 150T, and various PH3 dopant set points.

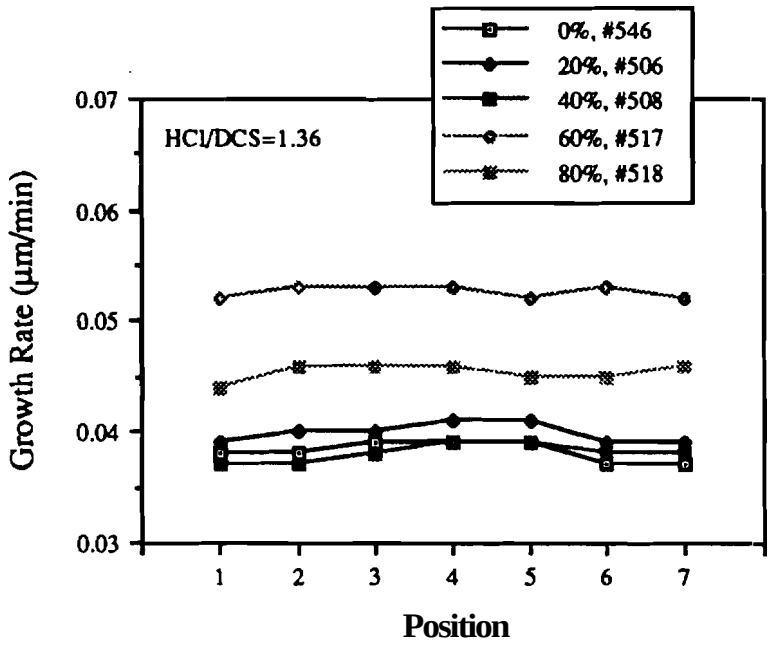


Figure 4.6 (e) Selective epitaxy growth rate profiles on oxide-patterned wafers at 920°C, 40T, and various PH_3 dopant set points.

4.3.1 Four-Point Probe Measurements

The easiest method to determine doping concentration of SEGELO is four-point probe measurement. Doped epitaxy runs of 1020°C-150T, 970°C-150T, 970°C-40T, 920°C-150T, and 920°C-40T were conducted in this experiment. Two-inch and three-inch oxide-patterned (100) wafers were used in each doped epitaxial run and were placed in the mid-point between the center and the edge of the susceptor. Since large area SEG/ELO was required in order to place four collinear probes on it, the three-inch wafers with less oxide coverage were used fur the four-point probe measurements after epitaxial growth. The sheet resistance were measured at seven points across the wafer where the thickness of the epitaxial layer had been determined. The resistivity was calculated as a product of sheet resistance and film thickness and then doping concentration was determined using Figure 3.8.

Figure 4.7 presented the combined effect of dopant set point, growth temperature, and pressure on phosphorus concentration in SEG/ELO determined by four point probe measurements, First, the dopant set point was the most significant factor. It is clear that phosphorus concentration increased dramatically with increasing dopant set point. Second, higher phosphorus concentration was observed at lower pressure and/or at lower temperature as shown in Figure 4.8 (a)-(d). Probably because low temperature permitted the gaseous boundary layer next to the silicon surface to be more stable and the diffusivities of the reactive species became larger at a lower deposition pressure, phosphorus incorporation in SEG/ELO was enhanced with decreasing temperature and/or decreasing pressure.

4.3.2 Resistance Measurements

Serpentine resistors were fabricated on ELO grown at 1020°C-150T, 970°C-40T, and 920°C-40T with various dopant set points. Resistors fabricated in the same dies where the thickness measurements have been taken before fabrication were measured. Resistance measurements of these resistors were taken using a probing station and an HP4145A Semiconductor Parameter Analyzer. Referring to Section 3.4.5.2, the sheet resistance was calculated by dividing the number of squares and thus resistivity was the product of sheet resistance and SEG/ELO thickness.

Since ELO has a mushroom shape on the oxide as shown in Figure 4.9(a), a simple

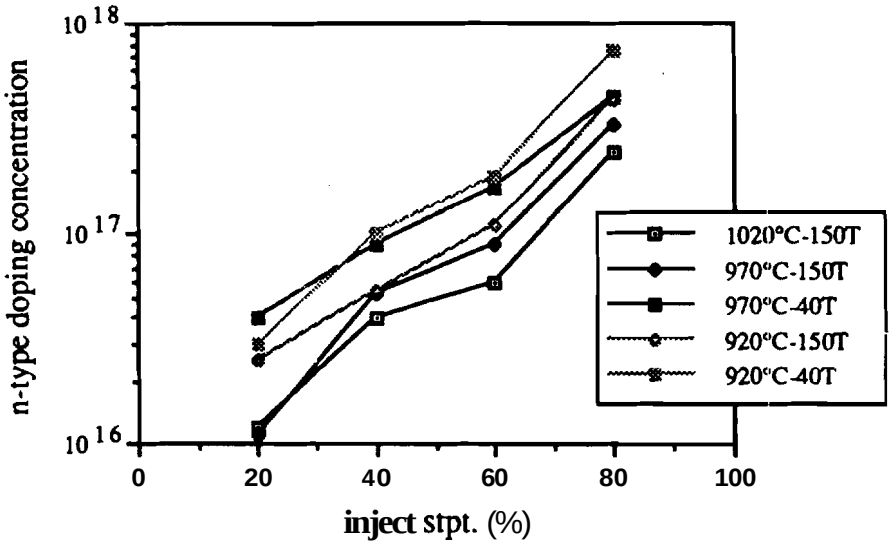


Figure 4.7 Phosphorus concentration determined by four point probe measurements vs. dopant set point at various growth conditions.

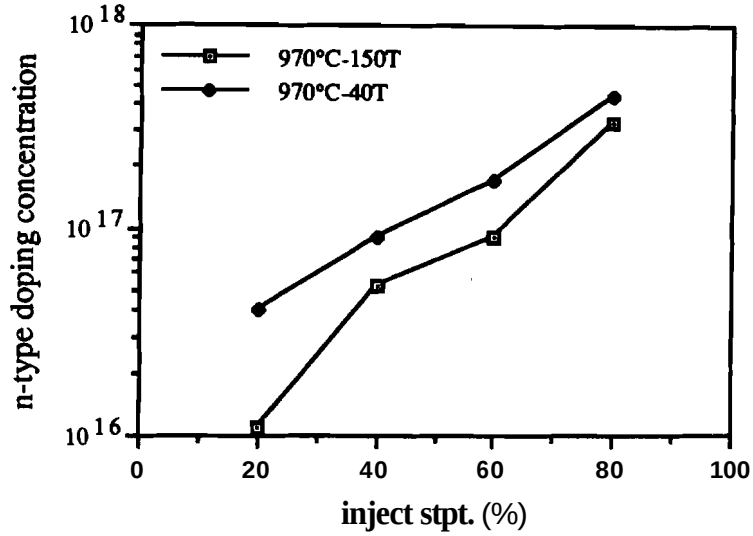


Figure 4.8 (a) Phosphorus concentration vs. dopant set point at 970°C as determined by four point probe measurements.

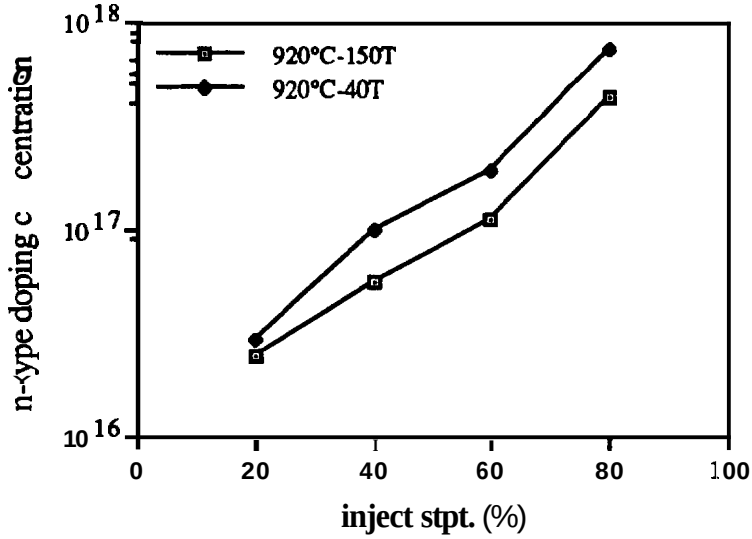


Figure 4.8 (b) Phosphorus concentration vs. dopant set point at 920°C as determined by four point probe measurements.

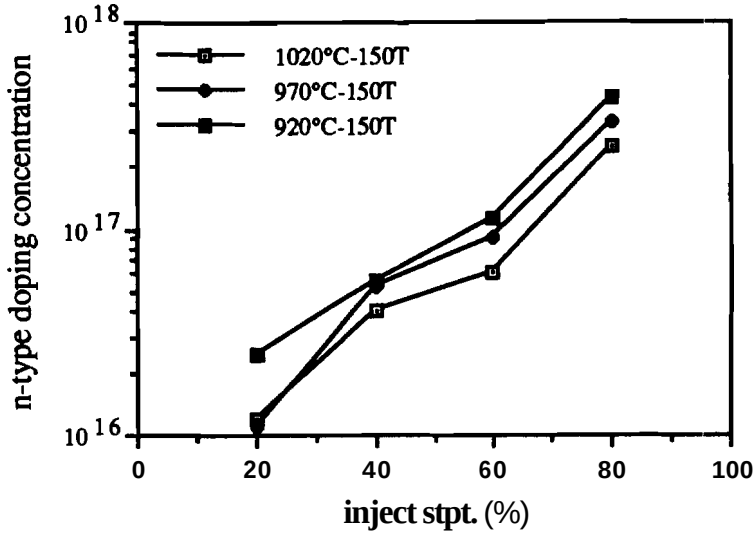


Figure 4.8 (c) Phosphorus concentration vs. dopant set point at 150 tom as determined by four point probe measurements.

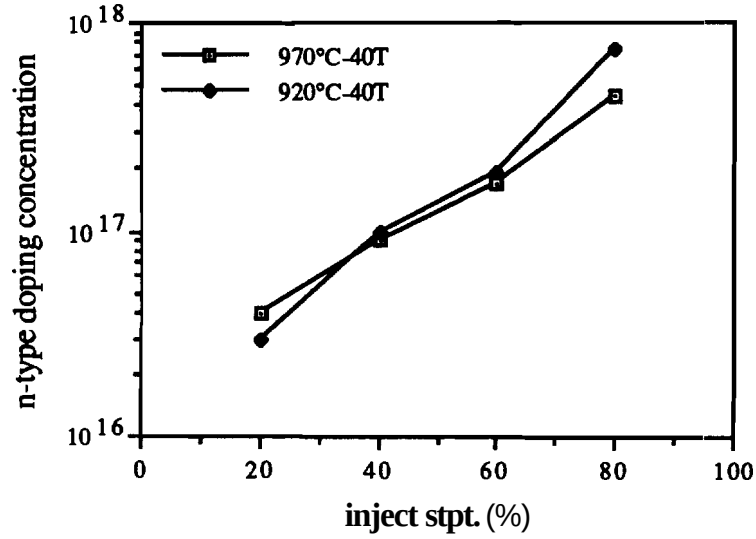


Figure 4.8 (d) Phosphorus concentration vs. dopant set point at 40 torr as determined by four point probe measurements.

modification was made for calculating the resistivity. In this modification structure model, the ELO resistor was composed of three parallel resistors as illustrated in Figure 4.9(b). Therefore, the measured resistance was the parallel sum of these three resistors, i.e., $R_{measured} = R1 // R2 // R2$. The aspect ratio was defined as 1:1 and thickness of resistor R1 was the sum of oxide thickness and ELO thickness over the oxide. Since the thickness was known, material's resistivity, which was same in each resistor, was easily obtained. By using Figure 3.8, phosphorus concentration in ELO material was determined.

Doping concentration determined by resistance measurements was found to be different from that determined by four point probe measurements. However, similar trends in phosphorus concentration in SEG/ELO were observed. Figure 4.10 presented the doping concentration determined by resistors versus dopant set point at various growth conditions. Obviously, the phosphorus incorporation was enhanced with higher dopant set poiint. In addition, higher doping concentration was achieved at lower temperature and lovver pressure.

4.3.3 C-V Measurements

The MOS capacitors built on SEGELO were measured using a probing station and an HP4275A multi-frequency LCR meter. A $1/C^2$ versus V plot was made based on the measured C-V data. A straight line in the depletion biasing region in this plot indicated uniform concentration in the depletion region. Then Equation 3.5 was used to calculate phosphorus concentration in the epitaxial layer from the slope of the $1/C^2$ vs. V plot. A simple computer analysis program written by Professor M. Lundstrom can also be used to calculate doping density from the measured C-V data. The program is in EC machine and the:command is "/a/ee557/CV/moscv".

Figure 4.11 presented a plot of phosphorus concentration determined by the C-V measurements versus dopant set point at 1020°C-150T, 970°C-40T, and 920°C-40T. Doping concentrations in the range 10^{16}-10^{18} phosphorus atoms/cm^3 were achieved in this experiment. The data points in Figure 4.10 were averaged values over at least 5 capacitors across the wafer. Again, significant increase in doping concentration was observed with larger dopant set point. Also, lower temperature and pressure were preferred for a higher phosphorus concentration.

Table 7 summarized the phosphorus concentrations determined by three different methods at various deposition conditions. Although there were differences among doping concentrations determined by different methods, similar dependences of dopant set point,

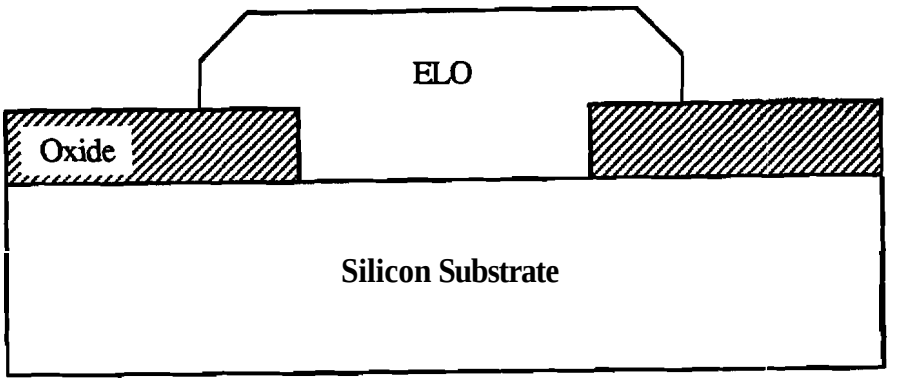


Figure 4.9 (a) Silicon epitaxial lateral overgrowth (ELO).

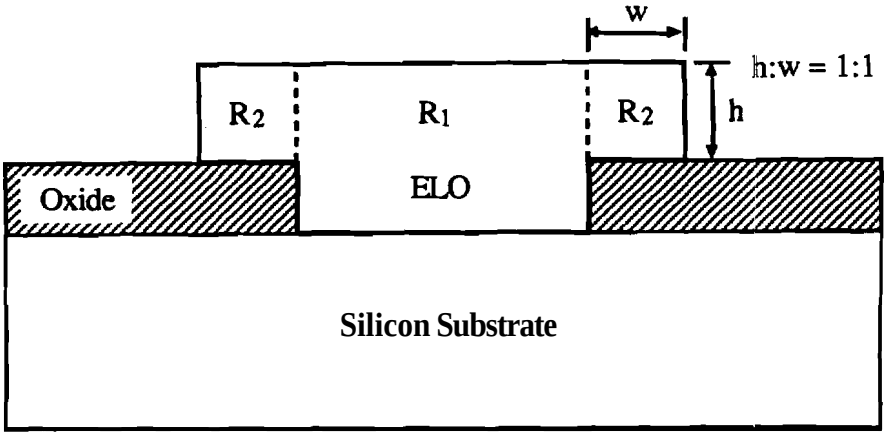


Figure 4.9 (b) A simple modification model of ELO for determining resistivity.

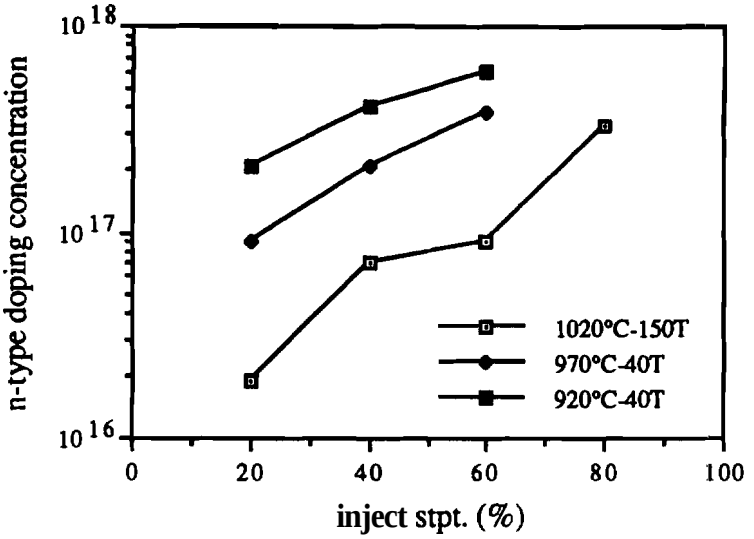


Figure 4.10 Phosphorus concentration determined by resistors vs. dopant set point at various growth conditions.

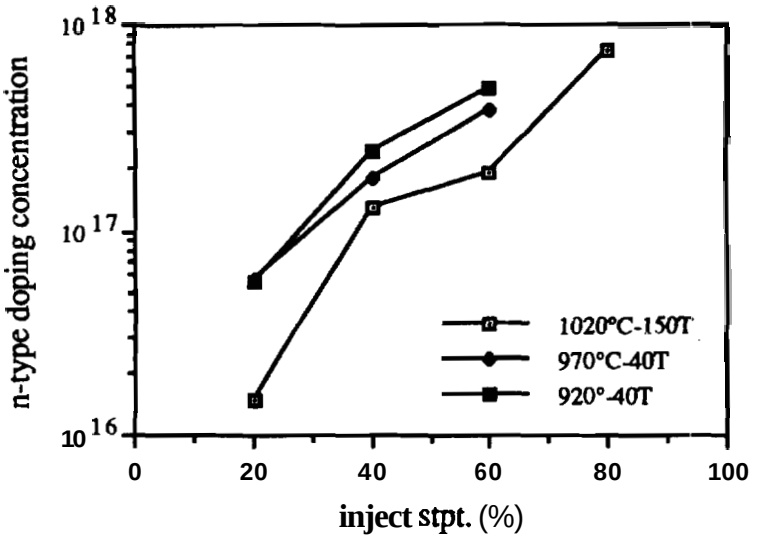


Figure 4.11 Phosphorus concentration determined by C-V measurements vs. dopant set point at various growth conditions.

Table 7

Summary of phosphorus concentration determined by different methods at various deposition conditions.

Run #	Temp (°C)	Press. (Torr)	HCl/DCS	Doping (%)	Doping Concentration		
					from 4-point probe	from resistors	from C-V
520	1020	150	6.4	20	1.2E+16	1.9E+16	1.5E+16
521	1020	150	6.4	40	4E+16	7E+16	1.3E+17
523	1020	150	6.4	60	6E+16	9E+16	1.9E+17
524	1020	150	6.4	80	2.5E+17	3.3E+17	7.4E+17
528	970	150	5.64	20	1.1E+16	-	-
529	970	150	5.64	40	5.3E+16	-	-
534	970	150	5.64	60	9E+16	-	-
535	970	150	5.64	80	3.3E+17	-	-
486	970	40	3	20	4E+16	9E+16	5.8E+16
467	970	40	3	40	9E+16	2.1E+17	1.8E+17
488	970	40	3	60	1.7E+17	3.8E+17	3.8E+17
490	970	40	3	80	4.5E+17	-	-
507	920	150	2.73	20	2.5E+16	-	-
509	920	150	2.73	40	5.5E+16	-	-
537	920	150	2.73	60	1.1E+17	-	-
538	920	150	2.73	80	4.3E+17	-	-
506	920	40	1.36	20	3E+16	2.1E+17	5.6E+16
508	920	40	1.36	40	1E+17	4E+17	2.4E+17
517	920	40	1.36	60	1.9E+17	6E+17	4.9E+17
518	920	40	1.36	80	7.5E+17	-	-

deposition temperature, and pressure were observed with each method. These data will be helpful in finding a close dopant set point for the desired in-situ doping concentration in SEG/ELO.

4.4 Electrical Measurements

Among semiconductor devices, the bipolar junction transistor is the most sensitive to material quality and processing defects. Therefore, comparative bipolar transistors, along with p-n junction diodes, were fabricated in SEG/ELO and in the identically processed n-type (100) silicon substrate, and their electrical characteristics were compared in order to characterize the SEG material quality. The fabrication process and the transistor structure were described in Section 3.3.2. After fabrication, devices were tested using an HP-4145A semiconductor parameter analyzer with a probing station. Dry nitrogen was passed over the wafer during the measurement. The initial electrical measurement results of the devices fabricated on undoped SEG/ELO, which was deposited at 40 Torr, are presented in this section. A photograph of a test bipolar junction transistor fabricated in SEG/ELO island is shown in Figure 4.12.

4.4.1 Diode Measurements

The diodes were tested first to ensure the transistor operation. It is important to test the performance of the diodes fabricated in SEG/ELO since p-n junctions are so widely used and the SEG/ELO material quality can be evaluated by these p-n junctions. Table 8 lists some important parameters that were extracted from the emitter-base and the collector-base diode characteristics. More than ten of each kind of diodes were examined for every wafer, and the numbers in Table 8 are the average values of functional devices. The p-n junction areas which were measured and compared are 3600 μm^2 and 10032 pm^2 for the emitter-base and the collector-base junctions, respectively.

A typical forward bias I-V curve for the SEG emitter-base diode, with collector open circuited, having 60μm x 60μm emitter is shown in Figure 4.13. The ideality factor, η, was calculated by taking the slope of the linear region in the forward bias I-V curve using Eq. (3.2). As listed in Table 8, the ideality factors were quite good for the diodes built in 970°C-40T SEG and in the substrate. At moderate forward bias voltages, ideality factors of emitter-base and collector-base junctions were between 1.00 and 1.01 for

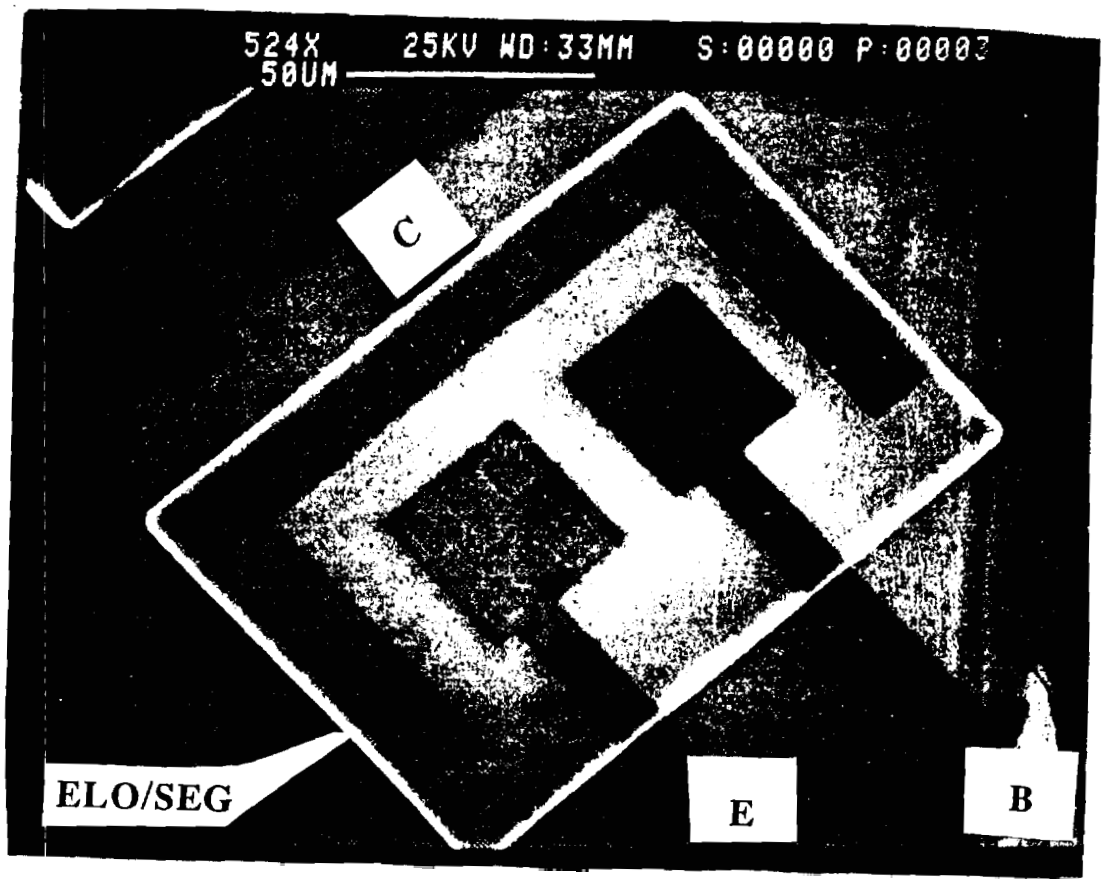


Figure 4.12 A SEM picture showing a test transistor fabricated in SEG/ELO.

Table 8

Summary of measured parameters from the emitter-base and collector-base diodes fabricated in bulk silicon substrate and 970°C-40T SEG.

Type	Substrate		970°C-40T SEG	
Junction	E-B	C-B	E-B	C-B
Ideality Factor (η)	1.01	1.01	1.00	1.01
Leakage Current Density (x 10^{-6} A/cm^2)	3.19	1.49	4.17	
Breakdown Voltage (V)	>40	>40	>40	

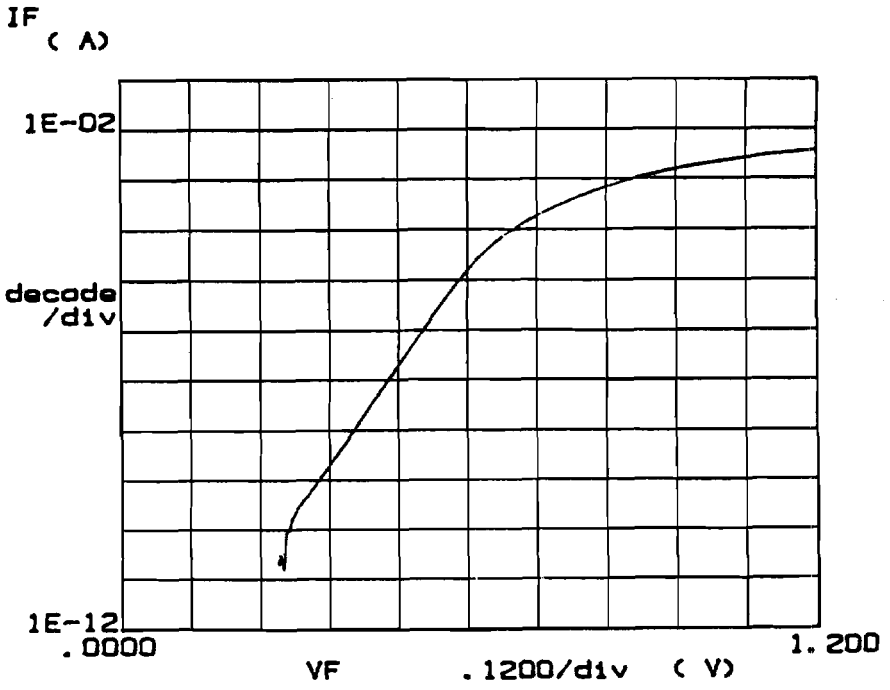


Figure 4.13 Forward bias I-V plot of a representative emitter-base SEG diode.

substrate diodes and for those fabricated in 970°C-40T SEG. The very low values of η indicated that the number of recombination centers, or defects, was low and the space charge layer recombination/generation currents are small. Hence the excellent quality of the 970°C-40T selective epitaxial film was demonstrated.

However, the ideality factors extracted from the diodes built in 920°C-40T SEG were high. For either emitter-base or collector-base diodes in 920°C-40T SEG, the average ideality factor was not less than 1.75, indicating significant recombination currents. It was suspected that more contaminant species, such as oxygen and carbon, were incorporated at lower temperatures, resulting in defects in the epitaxial layers.

The reverse leakage current densities of the emitter-base and the collector-base junctions, J_{ebo} and J_{cbo} respectively, were measured from the reverse bias I-V curves. The reverse bias leakage current was measured at -1.5V. As listed in Table 8, the reverse leakage current densities of E-B and C-B junctions for substrate devices and 970°C-40T SEG devices were in the same magnitude order, indicating that 970°C-40T SEG material quality was as good as silicon substrate quality. The reverse leakage current densities could be smaller if the devices were gettered to remove impurities and defects.

The breakdown voltages of the emitter-base and the collector-base junctions were also measured from the same curve. They were measured last since breakdown would affect device quality. The breakdown voltage was selected when the reverse bias exceeded 1mA. For all substrate and 970°C-40T SEG devices, the breakdown voltages of the E-R and C-B junctions were larger than 40V.

4.4.2 Transistor Measurements

Bipolar junction transistors fabricated in both 970°C-40T SEG and substrate with emitter dimension of 60μm x 60μm were measured and the device characteristics were then compared. The transistors were tested in the common emitter configuration. A set of I-V output curves for a representative SEG transistor were illustrated in Figure 4.14.

Figure 4.15 (a) and (b) present the Gummel plots, which are I_C and I_B versus V_{BE} curves, for two representative bipolar transistors built in 970°C-40T SEG and substrate, respectively. The shape of these two plots were very similar to each other. Fairly long and parallel ideal regions for I_C and I_B can be seen in these Gummel plots. The values at low current and voltage are sometimes erratic due to instrument error and bad contact between the probe and the metal pad. These values should not be considered meaningful. The forward DC current gain, β, was calculated from the vertical distance between I_C and I_B

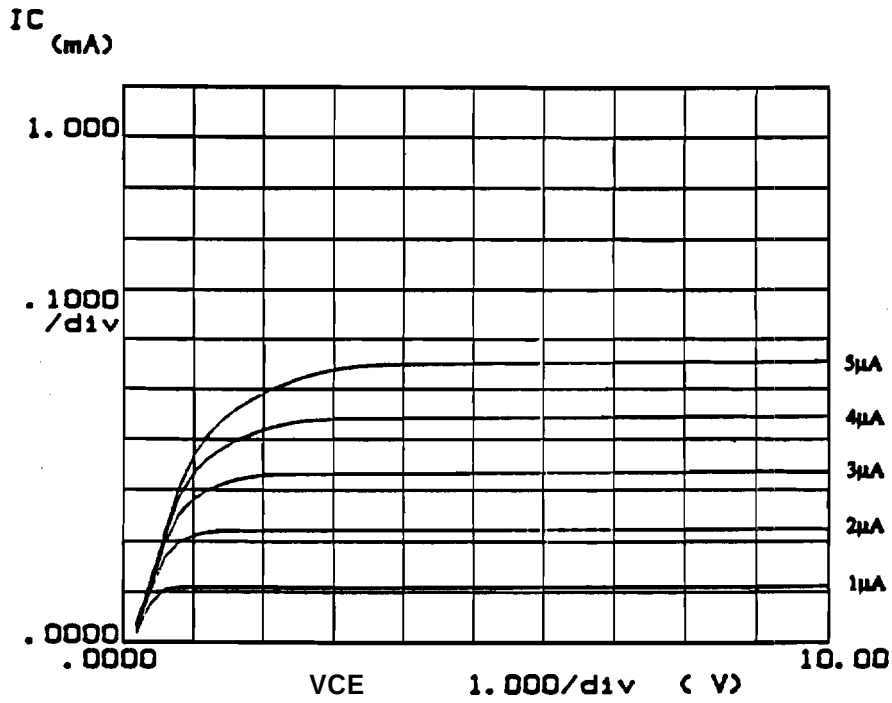


Figure 4.14 I_C versus V_{CE} characteristics for a representative bipolar transistor fabricated in 970°C-40T SEG.

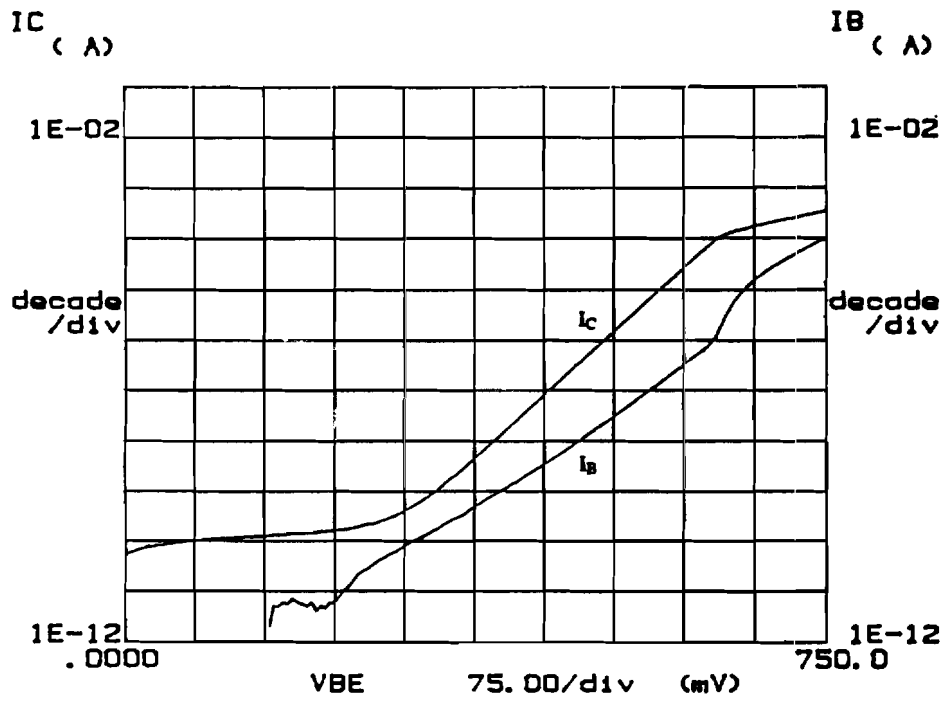


Figure 4.15 (a) Measured I_B and I_C versus V_{BE} characteristics for a representative bipolar transistor fabricated in 970°C-40T SEG.

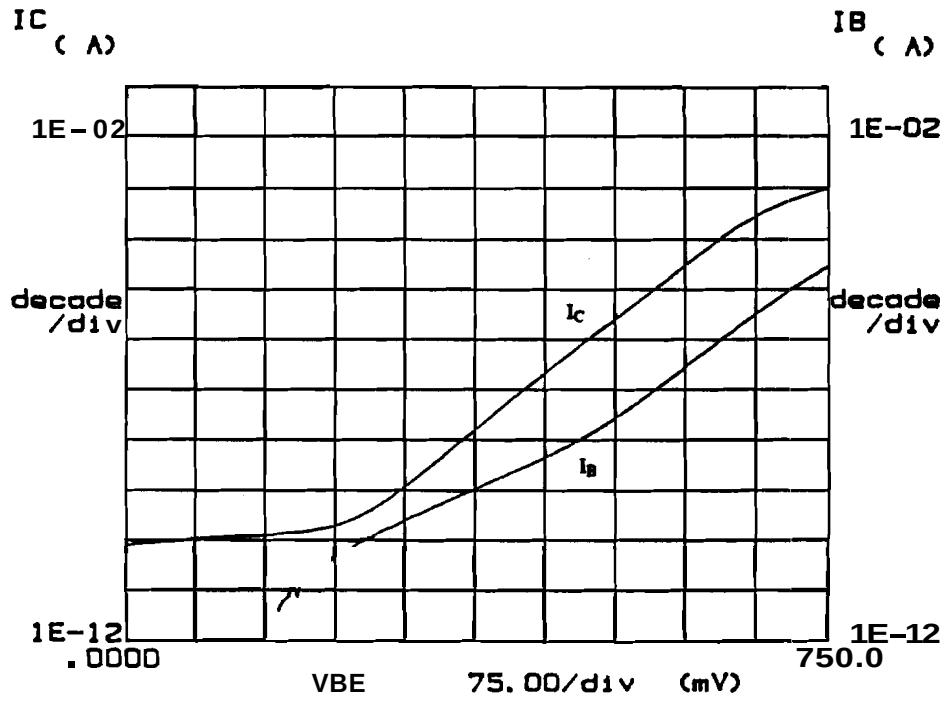


Figure 4.15 (b) Measured I_B and I_C versus V_{BE} characteristics for a representative bipolar transistor fabricated in silicon substrate.

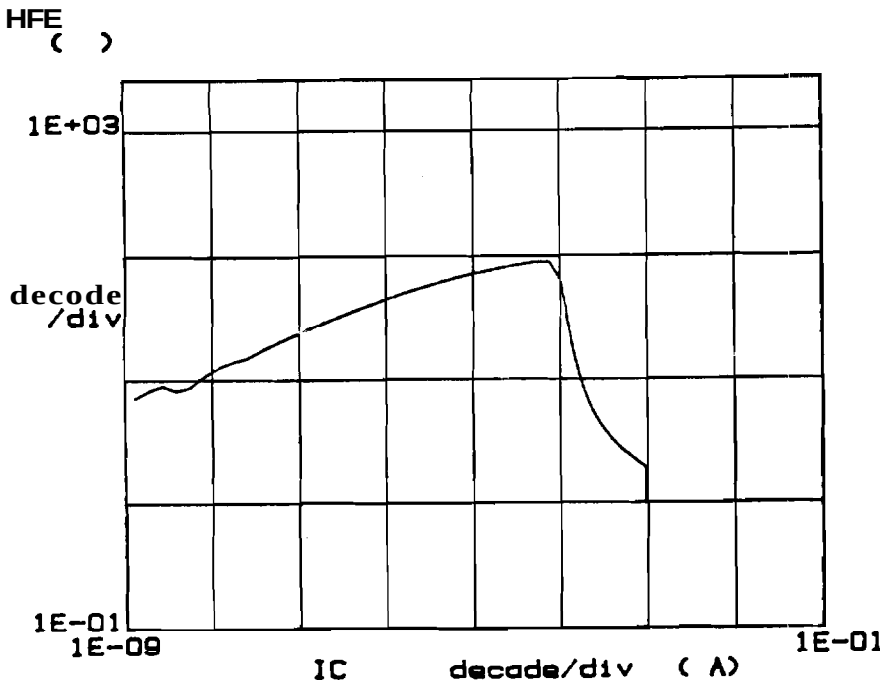


Figure 4.16 (a) Measured current gain (β) versus collector current (Ic) characteristics for a representative bipolar transistor fabricated in 970°C-40T SEG.

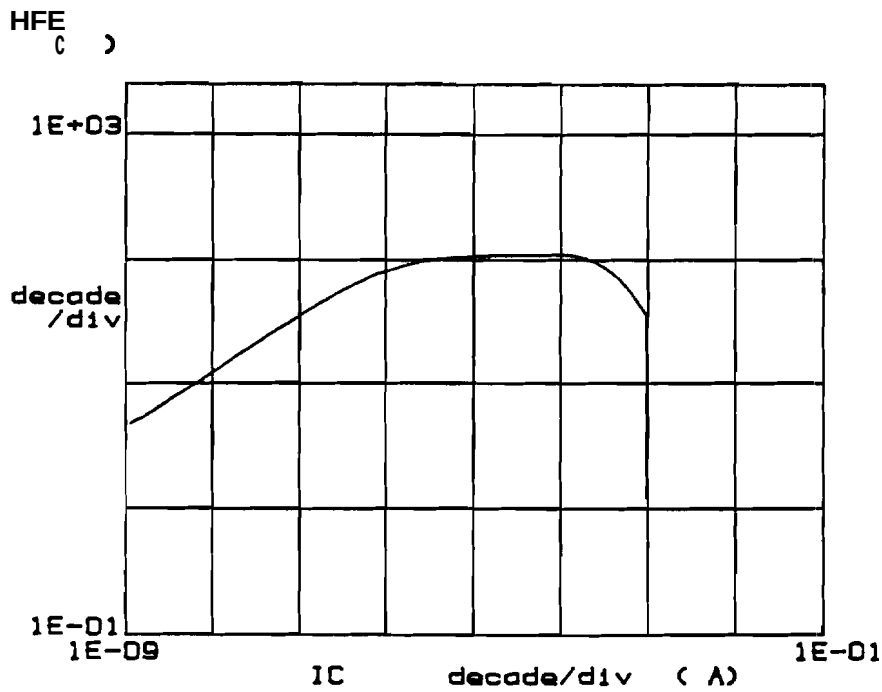


Figure 4.16(b) Measured current gain (β) versus collector current (Ic) characteristics for a representative bipolar transistor fabricated in silicon substrate.

curves at each tested V_{BE} value. Beta versus collector current plots for a representative SEG transistor and a substrate transistor are shown in Figure 4.16 (a) and (b), respectively, and the peak betas were obtained from these plots. Since there was no buried layer in both SEG and substrate transistors, which might result in large collect resistance, sharp β falloff with large collector current can be seen in these two plots. More than ten transistors were tested for each wafer and the maximum current gains were averaged over good devices. For the transistors fabricated in 970°C-40T SEG, the average maximum beta was 101. Compared to 112 for the substrate transistor, the material quality of the 970°C-40T SEG was again proved to be very similar to the substrate. Slight differences in average maximum betas, Gummel plots, and β vs I_C plots between these two kinds of transistors were most likely due to the differences in collector doping concentrations, and in the base width of the transistors as well.

CHAPTER 5: CONCLUSIONS

In this work, more than fifty epitaxy runs have been carried out using the Gemini-1 pancake reactor which is housed in the Purdue University Epitaxy Laboratory. Growth rate, uniformity, and doping characteristics of SEG deposited at temperatures between 820 and 1020°C and pressures between 40 and 150 Torr were investigated. In addition, test devices were fabri ated in SEG and measured to determine doping concentrations and to characterize SEG material quality.

The dependence of growth rate uniformities on growth temperatures and pressures was investigated. It was determined that better growth rate uniformity was achieved at lower deposition temperatures and/or pressures since epitaxial growth at lower temperatures and pressures was reaction-controlled. The ratios of standard deviation to mean growth rate across a wafer were normally less than ±3.3% for the all 40 Torr epitaxy runs. Wafer to wafer growth rate uniformities in the same epitaxy run were examined. Again, wafer to wafer uniformities were improved at lower pressures. For 40 Torr and 95 Torr runs, wafer to wafer uniformities always varied less than ±4.7%. Lower growth rates and better growth rate uniformities were observed for using the large inject tube in the reactor.

A number of n-type in-situ doped epitaxy runs at various temperatures and pressures, as well as at different dopant set points, were accomplished by introducing phosphine (PH_3) gas into the reactor during epitaxial deposition. Neither significant dependence of growth rates on doping with phosphine nor significant deterioration of growth rate uniformities in presence of phosphine were observed. Hence n-type in-situ doped SEG could be obtained with similar growth rates and uniformities as undoped SEG. Measurements of SEG doping concentration using three different methods revealed that the phosphorus concentrations of 10^{16}-10^{18} phosphorus atoms/cm^3 were achieved. It was shown that SEG doping concentration increased dramatically with increasing dopant set point. Also, lower deposition temperature and lower pressure was preferred for a higher phosphorus concentration. These results provided a basis for finding a close dopant set point for the desired in-situ doping concentration in SEG.

Previous work in SEG/ELO research has demonstrated the excellent quality of SEG material deposited at 970°C and 150 Ton [74]. In this work, diodes and bipolar transistors were fabricated in SEG films to evaluate the SEG material quality grown at 40 Torr. It was shown that the devices built in 970°C-40T SEG matched the performance of the device fabricated in bulk silicon. Junction ideality factors, reverse bias leakage currents, breakdown voltages, and maximum current gains extracted from the devices built in 970°C-40T SEG were as good as those parameters of substrate devices, indicating good quality of the SEG material grown at 970°C and 40 Torr. This implies that 970°C-40T SEG is sufficiently good to utilize it in development and fabrication of novel devices and other applications. It will provide better uniformity across the wafer than SEG grown at 970°C and 150 Ton without deteriorating the material quality. However, test results indicated that 920°C-40T SEG was of lower quality than 970°C-40T SEG. A possible reason for the degradation in 920°C-40T SEG may be that more contaminant species were incorporated at lower temperatures, resulting in higher defect density in the epitaxial layers.

The results obtained from this research work has laid the foundations for getting SEG with desired growth rate, uniformity, and doping characteristics in the Gemini-1 pancake reactor. It is hoped that these results will be helpful to utilize the SEG technology. However, device characterization of SEG material grown at lower temperatures will be further investigated. Future work will also include the study of the properties of in-situ doped SEG deposited by the Gemini-1 pancake reactor at low temperatures and reduced pressures.

LIST OF REFERENCES

LIST OF REFERENCES

[1] P. S. Burggraaf, "The Forces Behind Epitaxial-Silicon Trends," Semiconductor International, p. 45, Oct. 1983.

[2] K. E. Bean, W. R. Runyan and R. G. Massey, "Thin Film Technology for Advanced Semiconductors: Part 1-Silicon Epitaxy," *Semiconductor* International, p. 135, May 1985.

[3] G. R. Srinivasan, "Silicon Epitaxy for High Performance Integrated Circuits," Solid State Tech., pp. 101-110, Nov. 1981.

[4] Y. Hiroshima, S. Matsumoto, K. senda, T. Kuriyama, K. Horii, T. Kuroda, T. Kunii and H. Mizuno, "Elimination of Fixed Pattern Noise in Super-8 Format CCD Image Sensor By the Use of Epitaxial Wafers," IEDM-84 Tech. Dig. , pp. 32-35, 1984.

[5] A. Mohsen, "Vertical Charge-Coupled Devices," IEEE Intl. Solid State Circuit *Conf.* Dig. of Tech. Papers, pp. 152, Feb. 1979.

[6] G. Brosuk, F. Kub, N. Bluzer, D. Lampe, M. Evey and M.White, "High Speed Silicon CCDs Fabricated on High-Lifetime Epitaxial Material," IEEE Trans. Elec. Dev., vol. ED-26, no. 11, pp.1847, Nov. 1979.

[7] H. M. Liaw, J. Rose and P. L. Fejes, "Epitaxial Silicon for Bipolar Integrated Circuits," Solid State Tech., pp. 135-143, May 1984.

[8] D. S. Yaney and C. W. Pearce, "The Use of Thin Epitaxial Layers for MOS VLSI," *IEDM-81* Tech. Dig. , pp. 236-239, 1981.

[9] R. S. Payne, W. N. Grant and W. J. Bertram, "Elimination of Latchup in Bulk CMOS," IEDM-80 Tech. Dig. , pp. 248-251, 1980.

[10] T. Decan, "Silicon Epitaxy: An Overview," Microelectronics Manufacturing and Testing, Sept. 1984.

[11] S. M. Fisher, M. L. Hammond and N. P. Sandler, "Reduced Pressure Epitaxy in an Induction-Heated Vertical Reactor," Solid State Tech., pp. 107-112, Jan. 1986.

[12] R. B. Herring, "Advances in Reduced Pressure Silicon Epitaxy," Solid State Tech., pp. 75-80, Nov. 1979.

[13] B. S. Meyerson, "Low-Temperature Silicon Epitaxy by Ultrahigh Vacuum/ Chemical Vapor Deposition," Appl. Phys. *Lett.*, vol. 48, no. 12, pp. 797-799, Mar. 1986.

[14] T. J. Donahue and R, Reif, "Low Temperature Silicon Epitaxy Deposited by Very Low Pressure Chemical Vapor Deposition," J. Electrochem. *Soc.*, vol. 133, no. 8, pp. 1691-1705, Aug. 1986.

[15] W. Scot Ruska, Microelectronic Processing, McGraw-Hill, New York, p. 269, 1988.

[16] A. S. Grove, Physics and Technology of Semiconductor Devices, Wiley, New York, p. 10, 1967.

[17] F. C. Eversteyn, "Chemical-Reaction Engineering in the Semiconductor Industry," *Philips* Res. Rep., Vol. 29, p. 45, 1974.

[18] S. M. Sze, *Semiconductor* Devices: Physics and Technology,,Wiley, New York, 1985.

[19] S. Wolf and R. N. Tauber, Silicon Processing for the *VLSI* Era, vol. 1, Lattice Press, Sunset Beach, CA, 1986.

[20] H. C. Theuerer, "Epitaxial Silicon Films by the Hydrogen Reduction of $SiCl_4$," J. Electrochem. *Soc.*, vol. 108, p. 649, 1961.

[21] D. W. Hess, K. F. Jensen and T. J. Anderson, "Chemical 'Vapor Deposition," Reviews. in Chemical Eng., vol. 3, no. 2, p. 99, Apr. 1985.

[22] C. W. Manke and L. F. Donaghey, "Numerical Simulation of Transport Processes in Vertical Cylinder Epitaxy Reactor," Proc. of the Sixth *Intl.* Conf. on Chemical Vapor Deposition 1977, Electrochem. *Soc.*, p. 151, 1977.

[23] V. S. Ban, "Transport Phenomena Measurements in Epitaxial Reactors," J. Electrochem. *Soc.*, vol. 125, pp. 317-320, 1978.

[24] F. C. Eversteyn, P. J. W. Severin, C. H. J. van den Brekel and H. L. Peek, "A Stagnant Layer Model for the Epitaxial Growth of Silicon from Silane in a Horizontal Reactor," J. Electrochem. *Soc.*, vol. 117, pp. 925-931, 1970.

[25] E. Fujii, H. Nakamura, K. Haruna and Y. Koga, "A Quantitative Calculation of the Growth Rate of Epitaxial Silicon from $SiCl_4$ in a Barrel Reactor," J. *Electrochem. Soc.*, vol. 119, pp. 1106-1113, 1972.

[26] I. Oh, C. G. Takoudis and G. W. Neudeck, "Mathematical Modeling of Epitaxial Silicon Growth in Pancake Chemical Vapor Deposition Reactors," J. Electrochem. *Soc.*, vol. 138, no. 2, pp. 554-567, Feb. 1991.

[27] V. S. Ban, "Chemical Processes in Vapor Deposition of Silicon," J. Electrochem. *Soc.*, vol. 122, no. 10, pp. 1389-1391, Oct. 1975

[28] C. W. Menke and L. F. Donaghey, "Analysis of Transport Processes in Vertical Cylinder Epitaxy Reactors," J. *Electrochem. Soc.*, vol. 124, p. 561, 1977.

[29] H. A. Lord, "Convective Transport in Silicon Epitaxial Deposition in a Barrel Reactor," J. Electrochem. *Soc.*, vol. 134, no. 5, pp. 1227-1235, 1987.

[30] R. E. Logar and J. O. Borland, "Silicon Epitaxial Processing Techniques for Ultra-Low Defect Densities," Solid State Tech., p. 134, June 1985.

[31] B. S. Mayerson, E. Ganin, D. A. Smith, and T. N. Nguyen, "Low Temperature Silicon Epitaxy by Hot Wall Ultrahigh Vacuum/Low Pressure Chemical Vapor Deposition Techniques: Surface Optimization," J. *Electrochem. Soc.*, vol. 133, no. 6, pp. 1232-1235, 1986.

[32] K. V. Ravi, *Imperfections* and *Impurities* in Semiconductor Silicon, Wiley, New York, pp. 162-173, 1981.

[33] K. V. Ravi, "Crystallographic Defects in Epitaxial Silicon Films," Thin Solid Films, vol. 31, pp. 171-183, 1976.

[34] P. Rai-Choudhury, "Substrate Surface Preparation and Its Effect on Epitaxial Silicon," J. Electrochem. *Soc.*, vol. 118, p. 1183, 1971.

[35] P. Rai-Choudhury, A. J. Noreika, and M. L. Theodore, "Carbon in Epitaxial Silicon," J. Electrochem. *Soc.*, vol. 116, p. 97, 1969.

[36] H. R. Huff, R. C. Bracken, and S. N. Rea, "Influence of Silicon Slice Curvature on Thermally Induced Stresses," J. Electrochem. *Soc.*, vol. 118, p. 143, 1971.

[37] S. K. Ghandhi, *VLSI* Fabrication Principles, Wiley, New York,,1983.

[38] H. Voss and H. Kurten, "Device Isolation Technology by Selective Low-Pressure Silicon Epitaxy," IEDM-83 Tech. Dig. , pp. 35-38, 1983.

[39] N. Endo, K. Tanno, A. Ishitani, A. Kurogi and H. Tsuya, "Novel Device Isolation Technology with Selective Epitaxial Growth," IEEE Trans. Elec. Dev., vol. ED-31, no. 9, p. 1283, Sept. 1984.

[40] J. O. Borland and C. Drowley, "Advanced Dielectric Isolation Through Selective Epitaxial Growth Techniques," Solid State Tech., pp. 141-148, Aug. 1985.

[41] J. Freidrich and G. W. Neudeck, "Interface Characterization of Silicon Epitaxial Lateral Overgrowth over Existing SiO_2 for Three-Dimensional CMOS Structures," IEEE Elec. Dev. Lett., vol. EDL-10, no. 4 , pp. 144-146, Apr. 1989.

[42] G. W. Neudeck, "A New Epitaxial Lateral Overgrowth Silicon Bipolar Transistor," *IEEE* Elec. Dev. Lett., vol. EDL-8, no. 10, pp. 492-495, Oct. 1987.

[43] G. W. Neudeck, P. J. Schubert, J. L. Glenn, J. A. Friedrich, W. A. Klaasen, R. P. Zingg and J. P. Denton, "Three Dimensional Devices Fabricated by Silicon Epitaxial Lateral Overgrowth," J. Electronic Materials, vol. 19, no. 10, 1990.

[44] G. W. Neudeck, "Three-Dimensional CMOS Integration," Circuits and Devices, pp. 32-38, Sept. 1990.

[45] B. Joyce and J. Baldrey, "Selective Epitaxial Deposition of Silicon," *Nature*, vol. 195, no. 4840, p.485, Aug. 1962.

[46] R. Pagliaw, J. Corboy, L. Jastrzebski and R. Soydan, "Uniformly Thick Selective Epitaxial Silicon," J. Electrochem. *Soc.*, vol. 134, no. 5, p. 1235, May 1987.

[47] K. Tanno, N. Endo, H. Kitajima, Y. Kurogi and H. Tsuya, "Selective Silicon Epitaxy Using Reduced Pressure Technique," Jap. J. Appl. Phys., vol. 21, no. 9, pp. L564-566, Sept. 1982.

[48] P. Schubert and G. W. Neudeck, "Confined Lateral Selective Epitaxial Growth of Silicon for Device Fabrication," IEEE Elec. Dev. Lett., vol. 11, no. 5 , pp. 183-181, May 1990.

[49] G. Rubloff, R. Tromp, E. Van Loenen, P. Balk and F. LeGoues, "Summary Abstract: High Temperature Decomposition of SiO_2 at the Si/SiO_2 Interface," J. *Vac*. Sci. Tech., vol. 4, no. 3, p. 1024, May 1986.

[50] F. Smith and G. Ghidini, "Interaction of O_2 with Si (111) and (100)," J. Electrochem. *Soc.*, vol. 129, no. 10, p. 1326, Oct. 1982.

[51] G. Ghidini and F. Smith, "Interaction of H20 with Si (111) and (100)," J. Electrochem. *Soc.*, vol. 131, no. 12, p. 2924, Dec. 1984.

[52] H. Kitajima, A. Ishitani, N. Endo and K. Tanno, "Crystalline Defects in Selectively Epitaxial Silicon Layers," Jap. J. Appl. Phys., vol. 22, no. 12, p. L783, Dec. 1983.

[53] H. M. Liaw, D. Weston, B. Reuss, M. Birrittella and J. Rose, "Effect of Substrate Preparation and Growth Ambient on Silicon Selective Epitaxy," Proc. 9th Int. CVD *Conf.*, p. 463, 1984.

[54] H. Kurten, H. Voss, N, Kim and W. Engl, "Selective Low-Pressure Silicon Epitaxy for MOS and Bipolar Transistor Applications," IEEE Trans. Elec. Dev., vol. ED-30, no. 11, pp. 1511-1514, Nov. 1983.

[55] H. Regolini, D. Bensahel, E. Scheid and J. Mercier, "Selective Epitaxial Silicon Growth in the 650-1100°C Range in a Reduced Pressure Chemical Vapor Deposition Reactor Using Dichlorosilane," Appl. Phys. Lett., vol. 54, no. 7, pp. 658-659, Feb. 1989.

[56] L. Jastrzebski, "SOI by CVD: Epitaxial Lateral Overgrowth Review," J. Crystal Growth, vol. 63, p. 493, 1983.

[57] A. Ishitani, H. Kitajima, N. Endo and N. Kasai, "Facet Formation in Selective Silicon Epitaxial Growth," Jap. J. Appl. Phys., vol. 24, no. 10, pp. 1267-1269, Oct. 1985.

[58] A. Ishitani, H. Kitajima, N. Endo and N. Kasai, "Silicon Selective Epitaxial Growth and Electrical Properties of Epi/Sidewall Interfaces," Jap. J. Appl. Phys., vol. 28, no. 5, pp. 841-848, May 1989.

[59] C. Drowley, G. Reid and R. Hull, "Model for Facet and Sidewall Defect Formation during Selective Epitaxial Growth of (001) Silicon," Appl. Phys. Lett., vol. 55, no. 21, pp. 2205-2207, Feb. 1988.

[60] H. M. Liaw, R. H. Reuss, H. T. Nguyen and G. P. Woods, "Surface Morphology of Selective Epitaxial Silicon," Proc. 5th Int. Symp. on Silicon *Mat'ls* Science and Technology, p. 260, May 1986.

[61] J. Borland, R. Wise, Y. Oka, M. Gangani, S. Fong and Y. Matsumoto, "Silicon Epitaxial Growth for Advanced Device Structures," Solid State Tech., pp. 111-119, Jan. 1988.

[62] J. Pak, "A Process Technology for IC Compatible Micromechanical Sensors Using Epitaxial Lateral Overgrowth," Ph.D. Thesis Proposal, Purdue University, p.51, Mar. 1990.

[63] J. A. Friedrich, "Three-Dimensional MOS Process Development," Ph.D. Thesis, Purdue University, Feb. 1989.

[64] M. Kastelic, M.S.ChE. Thesis, Purdue University, Oct. 1988.

[65] A. Ishitani, N. Endo and H. Tsuya, "Local Loading Effect in Selective Silicon Epitaxy," Jap. J. Appl. Phys., vol. 23, pp. L391-394, 1984.

[66] C. I. Drowley, "Growth Rate Uniformity During Selective Epitaxy of Silicon," Proc. *10th* Int'l *CVD* Conf., Electrochem. Soc., pp. 418-427, Oct. 1987.

[67] J. A. Friedrich, M. Kastelic, G. W. Neudeck and C. G. Takoudis, "The Dependence of Silicon Selective Epitaxial Growth Rates on Masking Oxide Thickness," J. Appl. Phys., vol. 65, no. 4, pp. 1713-1716, Feb. 1989.

[68] J. H. Comfort and R. Reif, "Plasma-Enhanced Chemical Vapor Deposition of In Situ Doped Epitaxial Silicon at Low Temperatures. I. Arsenic Doping," J. Appl. Phys., vol. 65, no. 3, pp. 1053-1066, Feb. 1989.

[69] J. H. Comfort and R. Reif, "Plasma-Enhanced Chemical Vapor Deposition of In Situ Doped Epitaxial Silicon at Low Temperatures. II. Boron Doping," J. Appl. Phys., vol. 65, no. 3, pp. 1067-1073, Feb. 1989.

[70] M. L. Yu, D. J. Vitkavage and B. S. Meyerson, "Doping Reaction of PH_3 and B_2H_6 with Si (100)," J. Appl. Phys., vol. 59, no. 12, pp. 4032.-4037, June 1986.

[71] G. W. Neudeck, The PN Junction Diode, 2nd ed., Volume II in the Modular Series on Solid State Devices, Addison-Wesley, Reading, MA, 1989.

[72] R. F. Pierret, Advanced *Semiconductor* Fundamentals, Volume VI in the Modular Series on Solid State Devices, Addison-Wesley, Reading, MA, 1987.

[73] D. K. Schroder, Semiconductor Material and Device Characterization, Wiley, New York, 1990.

[74] J. W. Siekkinen, W. A. Klaasen, and G. W. Neudeck, "Selective Epitaxial Growth Silicon Bipolar Transistor for Material Characterization," *IEEE Trans*. Elec. Dev., vol. 35, no. 10, pp. 1640-1644, Oct. 1988.

APPENDICES

Appendix A: Fabrication Process Run Sheet for Test Devices

Date / time

1. Starting material _____
   - 2 inch p-type (boron)
   - orientation : (100)
   - resistivity : 6.29 - 8.51 Ω-cm

2. Piranha clean _____
   - $H_2O_2 : H_2SO_4 = 1:1$
   - BHF dip

3. Field Oxide
   - 20 min Hz burn oxidation @ 1050°C _____

4. Epi seed lithography (Mask#1,darkfield)
   Place wafer in hardbake oven _____
   10 min @ 120°C
   - Apply adhesive promoter HMDS _____
   - Apply AZ-1350 positive photoresist _____
   30 sec @ 4000 rpm
   - Place wafer in prebake oven _____
   20 min @ 90°C
   - Expose : 7.5 sec _____
   - Develop photoresist _____
   AZ developer : DI = 1 : 1, _____ sec
   - Place wafer in hardbake oven _____
   20 min @ 120°C
   Etch oxide in BHF _____
   Etch time : _____
   - Remove photoresist in ACE _____

5. Piranha clean _____
   - $H_2O_2 : H_2SO_4 = 1:2$
   - BHF dip

6. Selective epitaxy _____
   - Run# : _____
   - Bake Hz
     Time : _____ min
     Temperature : _____ °C
     Pressure : _____ torr
     H2 mass flow : _____ slm
   - Etch HCl
     Time : _____ min

Temperature : _____ °C
Pressure : _____ tom
HCl mass flow : _____ slm

- Deposit
  Time : _____ min
  Temperature : _____ °C
  Pressure : _____ tom
  DCS mass flow : _____ slm
  HCl mass flow : _____ slm
  N dopant setpt : _____ % (200 ppm PH_3 in H_2)
- Epi thickness (ave) : _____

7. Piranha clean (1:1) _____

*** For PMOS:**

8a. Gate oxide for **PMOS**
- 40 min dry oxidation @ 1100°C _____

8b. Deposit polysilicon
- 3000Å @ 580°C _____

8c. Poly gate lithography (Mask#4, lightfield)
Place wafer in hardbake oven _____
10 min @ 120°C
- Apply adhesive promoter HMDS _____
- Apply AZ-1350 positive photoresist _____
  30 sec @ 4000 rpm
- Place wafer in prebake oven _____
  20 min @ 90°C
- Expose : 7.5 sec _____
- Develop photoresist _____
  AZ developer : DI = 1 : 1, _____ sec
- Place wafer in hardbake oven _____
  20 min @ 120°C
- Etch poly (Wet etch) _____
- Remove photoresist in ACE _____

*** If no PMOS, then**

8. Epi oxide
- 20 min H_2 bum oxidation @ 1000°C _____

9. Piranha clean (1:1) _____

10. Base lithography (Mask#2, darkfield)
- Place wafer in hardbake oven _____
  10 min @ 120°C
- Apply adhesive promoter HMDS _____
- Apply AZ-1350 positive photoresist _____
  30 sec @ 3500 rpm
- Place wafer in prebake oven _____
  20 min @ 90°C
- Expose : 7.5 sec _____

- Develop photoresist
  AZ developer : DI = 1 : 1, _____ sec
- Place wafer in **hardbake** oven
  20 min @ **120°C**
- Etch oxide in BHF
  Etch time : _____

11. Base implant (P-implant)
- Implant Boron
  Dose : 5 x 10^{13}/cm^2
  Energy : 25 **KeV**
- Strip resist

12. Piranha clean (1:1)

13. Base oxide / drive-in
- 20 **min** wet oxidation @ **1000°C**
- 20 min @ **1000°C** in N_2

14. Piranha clean (1:1)

15. Emitter lithography **(Mask#3, darkfield)**
- Place wafer in **hardbake** oven
  10 min @ 120°C
- Apply adhesive promoter HMDS
- Apply AZ-1350 positive photoresist
  30 **sec** @ **3500** rpm
- Place wafer in **prebake oven**
  20 min @ 90°C
- **Expose** : 7.5 sec
- Develop photoresist
  AZ developer : DI = 1 : 1, _____ sec
- Place wafer in **hardbake** oven
  20 min @ **120°C**

Etch oxide in BHF
Etch time : _____

16. Emitter implant (N-implant)
- Implant Arsenic
  Dose : **1 x 10^{15}/cm^2**
  Energy : 25 **KeV**

Strip resist

17. Piranha clean (1:1)

18. Emitter oxide / drive-in
20 min wet oxidation @ **1000°C**

19. Contact lithography (Contact to epi, mask#6, **darkfield)**
- Place wafer in **hardbake oven**
  10 min @ 120°C
- Apply adhesive promoter HMDS

- Apply AZ-1350 positive photoresist
  30 sec @ 4000 rpm
- Place wafer in prebake oven
  20 min @ 90°C
- Expose : 7.5 sec
- Develop photuresist
  AZ developer : DI = 1 : 1, _____ sec
- Place wafer in hardbake oven
  20 min @ 120°C
- Etch oxide in BHF
  Etch time : _____
- Remove photoresist in ACE

20. Piranha clean (1:1)

21. Contact lithography (Contact to substrate, mask#5, darkfield)
- Place wafer in hardbake oven
  10 min @ 120°C
- Apply adhesive promoter HMDS
- Apply AZ-1350 positive photoresist
  30 sec @ 4000 rpm
- Place wafer in prebake oven
  20 min @ 90°C
  Expose : 7.5 sec
- Develop photoresist
  AZ developer : DI = 1 : 1, _____ sec
- Place wafer in hardbake oven
  20 min @ 120°C
- Etch oxide in BHF
  Etch time : _____
- Remove photoresist in ACE

22. Piranha clean (1:1)

23. Metal lithography (Lift-off, mask#7, darkfield)
- Place wafer in hardbake oven
  10 min @ 120°C
- Apply adhesive promoter HMDS
- Apply AZ-1350 positive photoresist
  30 sec @ 3500 rpm
- Place wafer in prebake oven
  25 min @ 90°C
- Expose : 7.5 sec
- Develop photoresist
  AZ developer : DI = 1 : 1, _____ sec
- Do not hardbake photoresist
- BHF dip
- Do not remove photoresist

24. Metal deposition
- sputter deposit Al-1%Si, 30 min

25. Metal lift off
    - Remove metal and photoresist in ACE

26. Metal anneal
    - 20 min N_2 @ 400°C

27. Electrical testing

Appendix B: Summary of Growth Rate Measurements for Epi Runs

Run#	Wafer ID#	Temp (°C)	Press. (Torr)	HCl/DCS	Doping (%)	Dep. Time	Ave. G. R. (μm/min)	Std. Dev. (μm/min)	Std. Dev./Ave. G. R. (%)	% Non-uniformity
480	480-1	1020	150	6.4	0	20	0.206	0.007	3.4	4.7
480	480-2	1020	150	6.4	0	20	0.222	0.0114	5.1	7.1
533	533-1	1020	150	6.4	0	20	0.202	0.0147	7.2	10.2
533	533-2	1020	150	6.4	0	20	0.196	0.0116	5.9	8.1
520	520-1	1020	150	6.4	20	20	0.185	0.0086	4.7	6.9
520	520-2	1020	150	6.4	20	20	0.187	0.0093	5	6.2
521	521-1	1020	150	6.4	40	20	0.183	0.0152	8.3	10.1
521	521-2	1020	150	6.4	40	20	0.197	0.0062	3.1	3.8
523	523-1	1020	150	6.4	60	20	0.217	0.0125	5.8	8.3
523	523-2	1020	150	6.4	60	20	0.193	0.0077	4	5.3
524	524-1	1020	150	6.4	80	20	0.232	0.008	3.4	4.8
524	524-2	1020	150	6.4	80	20	0.21	0.0093	4.4	5.3
431	w-1-4	970	150	5.64	0	40	0.134	0.0097	7.2	10.5
477	477-1	970	150	5.64	0	20	0.103	0.007	6.8	10.1
477	477-2	970	150	5.64	0	20	0.122	0.011	9	11.5
540	540-1	970	150	5.64	0	20	0.055	0.0018	3.3	4.6
540	540-2	970	150	5.64	0	20	0.059	0.0038	6.4	9.6
560	560-1	970	150	5.64	0	20	0.058	0.0018	3.1	3.4
484	484-1	970	95	4.32	0	20	0.138	0.0068	4.9	6.3
484	484-2	970	95	4.32	0	20	0.132	0.0036	2.7	3.8
511	511-1	970	95	4.32	0	20	0.113	0.0045	4	5.4
511	511-2	970	95	4.32	0	20	0.109	0.0041	3.8	5.1
561	561-1	970	95	4.32	0	20	0.094	0.0039	4.1	5.9
481	481-1	970	40	3	0	20	0.102	0.0008	0.8	1
481	481-2	970	40	3	0	20	0.097	0.0008	0.8	1
510	510-1	970	40	3	0	20	0.082	0.0021	2.6	3.7
510	510-2	970	40	3	0	20	0.079	0.0025	3.2	3.8
522	522-1	970	40	3	0	25	0.09	0.002	2.2	3.3
522	522-2	970	40	3	0	25	0.096	0.0011	1.2	1.6
528	528-2	970	150	5.64	20	20	0.101	0.066	6.5	7.9
529	529-1	970	150	5.64	40	20	0.102	0.0059	5.8	8.1
529	529-2	970	150	5.64	40	20	0.096	0.0036	3.7	5.2
534	534-1	970	150	5.64	60	20	0.095	0.0069	7.2	10.3
534	534-2	970	150	5.64	60	20	0.116	0.0062	5.4	6.6
535	535-1	970	150	5.64	80	20	0.094	0.0025	2.7	3.7
535	535-2	970	150	5.64	80	20	0.1	0.0094	9.5	13.1
486	486-1	970	40	3	20	20	0.11	0.0034	3.1	4.5
486	486-2	970	40	3	20	20	0.106	0.0013	1.3	1.8
487	487-1	970	40	3	40	20	0.11	0.0054	4.9	7.1
487	487-2	970	40	3	40	20	0.107	0.0037	3.5	4.6
488	488-1	970	40	3	60	20	0.114	0.0021	1.8	3.1
488	488-2	970	40	3	60	20	0.112	0.0034	3	4

Run #	Wafer ID#	Temp. (°C)	Press. (Torr)	HCl/DCS	Doping (%)	Dep. Time	Ave. G. R. (μm/min)	Std. Dev. (μm/min)	Std. Dev./Ave. G. R. (%)	% Non-uniformity
478	478-1	920	150	2.73	0	20	0.093	0.006	6.5	9.4
478	478-2	920	150	2.73	0	20	0.083	0.0042	5.1	6
541	541-1	920	150	1.36	0	30	0.042	0.0028	6.6	8.4
541	541-2	920	150	1.36	0	30	0.035	0.0021	6.1	8.6
548	548-1	920	150	2.73	0	30	0.052	0.0039	7.6	10.9
548	548-2	920	150	2.73	0	30	0.055	0.0028	5.1	6.4
485	485-1	920	95	2.05	0	20	0.084	0.0031	3.7	4.8
485	485-2	920	95	2.05	0	20	0.082	0.0069	8.4	10.7
512	512-1	920	95	2.05	0	30	0.063	0.0023	3.7	4.8
512	512-2	920	95	2.05	0	30	0.065	0.0045	6.9	8.5
547	547-1	920	95	2.05	0	30	0.049	0.0022	4.5	6.1
547	547-2	920	95	2.05	0	30	0.053	0.0023	4.3	5.7
481	482-1	920	40	1.36	0	20	0.056	0.0014	2.5	3.6
481	482-2	920	40	1.36	0	20	0.051	0.0017	3.3	5
500	500-1	920	40	1.36	0	30	0.128	0.0033	2.6	3.1
500	500-2	920	40	1.36	0	30	0.042	0.001	2.3	3.6
546	546-1	920	40	1.36	0	30	0.038	0.0009	2.4	2.6
546	546-2	920	40	1.36	0	30	0.04	0.001	2.5	2.5
564	564-1	920	40	0	0	30	0.118	0.005	4.2	6
507	507-1	920	150	2.73	20	30	0.058	0.0024	4.1	5.2
507	507-2	920	150	2.73	20	30	0.053	0.0047	8.8	11.5
509	509-1	920	150	2.73	40	30	0.06	0.0032	5.3	6.8
509	509-2	920	150	2.73	40	30	0.06	0.0023	3.9	5.1
537	537-1	920	150	2.73	60	30	0.076	0.0038	5	7.4
537	537-2	920	150	2.73	60	30	0.069	0.0031	4.5	5.9
543	543-1	920	150	2.73	80	30	0.042	0.0031	7.4	9.5
543	543-2	920	150	2.73	80	30	0.046	0.0021	4.5	6.7
506	506-1	920	40	1.36	20	30	0.04	0.0011	2.8	3.8
506	506-2	920	40	1.36	20	30	0.04	0.0009	2.2	2.5
508	508-1	920	40	1.36	40	30	0.041	0.0018	4.4	6.2
508	508-2	920	40	1.36	40	30	0.038	0.0008	2.1	2.6
517	517-1	920	40	1.36	60	30	0.051	0.0028	5.5	6.8
517	517-2	920	40	1.36	60	30	0.053	0.0005	1	1
518	518-1	920	40	1.36	80	30	0.045	0.0008	1.8	2.2
514	514-1	870	95	1.18	0	40	0.033	0.0015	4.5	6.3
514	514-2	870	95	1.18	0	40	0.035	0.0008	2.3	2.9
544	544-1	870	95	1.18	0	40	0.026	0.0016	6.2	8
544	544-2	870	95	1.18	0	40	0.024	0.0015	6.2	8.3
501	501-1	870	40	0.55	0	40	0.027	0.002	7.4	9.1
501	501-2	870	40	0.55	0	40	0.027	0.0009	3.3	3.7
513	513-1	870	40	0.55	0	40	0.027	0.0005	1.8	1.9
513	513-2	870	40	0.55	0	40	0.028	0.0005	1.9	1.8
545	545-1	840	40	0.4	0	40	0.012	0.0004	3.1	4.3
545	545-2	840	40	0.4	0	40	0.011	0	0	0
566	566-1	840	40	0	0	40	0.027	0.0009	3.3	3.7
573	573-1	820	40	0	0	60	0.014	0.0004	2.9	4.3