

# Analysis and Evaluation of MAC Operators for Fast Fourier Transformation

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<b>Article History</b>	<b>Abstract</b>
<p><b>Article Submission</b> 19 November 2017</p> <p><b>Revised Submission</b> 17 January 2018</p> <p><b>Article Accepted</b> 1 March 2018</p> <p><b>Article Published</b> 31<sup>st</sup> March 2018</p>	<p><i>Arithmetic tasks are broadly utilized in Digital Signal Processing (DSP) applications. In this paper, a streamlined plan of the melded Add-Multiply (FAM) administrators is being investigated for the expanding execution. The direct plan of an AM unit is executed by apportioning a snake and afterward driving its yield to the contribution of a multiplier, increments essentially both region and basic way postponement of the circuit. The immediate recoding of the entirety of two numbers in its MB structure prompts a progressively effective execution of the intertwined Add-Multiply unit contrasted with the regular one, earlier recoding plans depend on complex controls in bit-level, which are actualized by committed circuits in entryway level. This new recoding plan and Modified CSA Tree, diminishes the basic way delay and decreases power utilization. This paper focuses on the extra decrease of dormancy and force utilization of CSA tree multiplier. This is cultivated by the utilization of Modified stall ADD-Multiply administrator and 4:2 compressor adders. Three elective plans of the proposed S-MB approach utilizing regular and marked piece Full Adders (FAs) and Half Adders (HAs) are being investigated as building squares.</i></p> <p><b>Keywords:</b> <i>DSP, adders, compressors, CSA</i></p>

## I. Introduction

Recent time hardware utilizes Digital Signal Processing (DSP) giving custom quickening agents to the areas of interactive media, interchanges, and so on. The plan of number-crunching parts utilized for consolidating tasks, which share information, can prompt noteworthy execution upgrades. In light of the perception that an option can frequently be ensuing to an augmentation [10], the Multiply-Accumulator (MAC) and Multiply-Add (MAD) units were acquainted driving with progressively proficient executions of DSP calculations contrasted with the regular ones, which utilize just crude assets [3], [12]. A few structures have been proposed to advance the exhibition of the MAC activity regarding region occupation, basic way postponement, and force utilization [1-2].

The fundamental goal of the paper on the productive plan of Fused Add-Multiply administrators is focusing on the streamlining of the recoding plan for direct molding of the MB type of the aggregate of the two numbers (entirety to MB – S-MB). This paper is concentrating on another recoding procedure, which diminishes the basic way delay and lessens zone and force utilization. The proposed S-MB calculation is organized basic and can be effectively adjusted so as to be applied either in marked (in 2's supplement portrayal) or unsigned numbers, which involve odd or considerably number of bits. Three elective plans of the proposed S-MB approach utilizing traditional and marked piece Full Adders (FAs) and Half Adders (HAs) as building squares are being investigated. An organized and productive recoding method, this proposed structure, conveys upgrades in both territory occupation and force utilization.

## II. Existing techniques

Booth based Multipliers is an incredible calculation for marked number augmentation, which treats both positive and negative numbers consistently [9]. For the standard include move activity, every multiplier bit creates one numerous of the multiplicand to be added to the halfway item. In the event that the multiplier is exceptionally enormous, at that point countless multiplicands must be included [7], [13]. For this situation the postponement of multiplier is resolved for the most part by the quantity of increments to be performed. On the off chance that there is an approach to lessen the quantity of the augmentations, the exhibition will show signs of improvement.

TABLE I: RADIX-4 BOOTH ENCODING

$Y_{2j+1}$	$Y_{2j}$	$Y_{2j-1}$	$Y_j^{MB}$
0	0	0	0
0	0	1	+1
0	1	0	+1
0	1	1	+2
1	0	0	-2
1	0	1	-1
1	1	0	-1
1	1	1	0

Booth algorithm calculation is a technique that will diminish the quantity of multiplicand products. For a given scope of numbers to be spoken to, a higher portrayal radix prompts less digits [8]. Since a k-bit twofold number can be deciphered as K/2-digit radix-4 number, a K/3-digit radix-8 number, etc, it can manage more than the slightest bit of the multiplier in each cycle by utilizing high radix duplication.

An AM operator implies the Add-Multiply operator in which both the option and increase will be performed by a solitary execution cycle. A considerable lot of the DSP applications depend on this AM activity. The clear plan of the AM unit is by first dispensing a viper and afterward driving its yield to the contribution of a multiplier, increments both the zone and basic way deferral of the circuit. The combined AM operator is spoken to by the capacity  $Z = X \cdot (A + B)$ .

The square diagram of AM activity is appeared in fig. 1. It comprises of a viper, incomplete item generator, CSA snake tree, CLA viper, MB encoder and a Correction expression factor. It includes an AM operator which actualize the advancement of the activity as  $Z = X \cdot (A + B)$ . The traditional plan of the AM operator necessitates that its information sources An and B are first headed to a viper and afterward the info and the total  $Z = A + B$  are headed to a multiplier so as to get Y. The disadvantage of utilizing a viper is that it embeds a huge deferral in the basic way of the AM. As there are convey signs to be spread inside the snake, the basic way relies upon the bit-width of the information sources. So as to diminish this postponement, a Carry - Look-Ahead (CLA) viper can be utilized which, be that as it may, expands the zone occupation and force dispersal

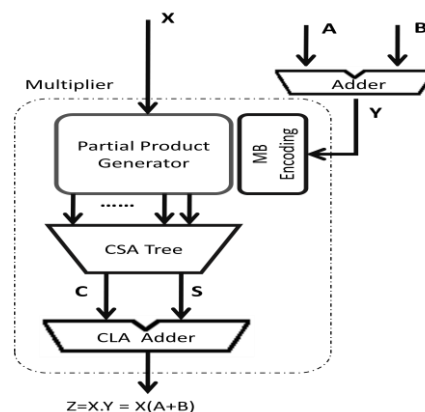


Fig 1 : Block Diagram of Add-Multiply operations

Diverse recoding in various entryway level executions and execution, the two options recoding plans is actualized [5]. The XOR entryway base execution gives least territory and defer numbers in many advances because of the little selector size and the even sign ways, while the mux-based usage can give best outcomes in some multiplexer based innovations [6].

### III. Proposed Methodology

An upgraded plan of the AM administrator depends on the combination of the snake and the MB encoding unit into a solitary information way hinder by direct recoding of the total to its MB portrayal. The melded Add-Multiply (FAM) just a single snake toward the end (last viper of the equal multiplier), therefore, huge region investment funds are watched and the basic way postponement of the recoding procedure is diminished and decoupled from the bit-width of its data sources.

Here we are given with the three inputs X, A and B. among which the A and B input bits will be converted to its two's complement form, and will be directly forwarded to its S-MB encoder in which all the consecutive bits are getting added and will be converted to the corresponding Modified Booth form simultaneously, so the delay and area will be got improved. Here we are using some specially designed half-adders and full-adders for its efficient implementation, depending on the sign of both the input and output bits.

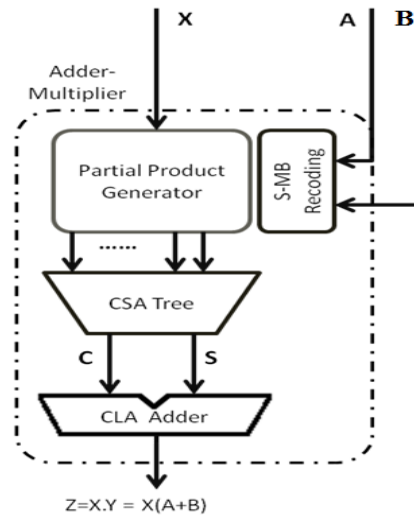


Fig 2: Basic structure of adder multiplier unit

Since the result say  $Y = A+B$  will be in used for the proposed Algorithm based multiplication with the reduced no of partial product stages. This implementation will suits for both the signed and unsigned numbers of any bit width. The results will be forwarded to the CSA adder tree on to which the Correction Term is also added, to nullify the errors present it, and for the final addition process we will use the Carry Look-ahead Adder. The detailed structural diagram of the projected structure is describes in fig. 2. The S-MB based FAM design used different schemes with the support of the specially designed components say, signed HA. These are all discussed below in detail along with the structure and truth tables of all the systems.

In these strategy, I have recode the total of two successive bits of the info  $A_n (a_{2j}, a_{2j+1})$  with two sequential bits of the information B ( $b_{2j}, b_{2j+1}$ ) into one MB digit  $y_{jMB}$ . As we see from Table I, three bits are remembered for framing a MB digit. The most critical of them is contrarily weighted while the two least noteworthy of them have positive weight. Thusly, so as to change the two previously mentioned sets of bits in MB structure we have to utilize marked piece number juggling. For this reason, we build up a lot of bit-level marked Half Adders (HA) and Full Adders (FA) believing their sources of info and yields to be agreed upon. Their reality tables and the Boolean articulations are as per the following block diagram.

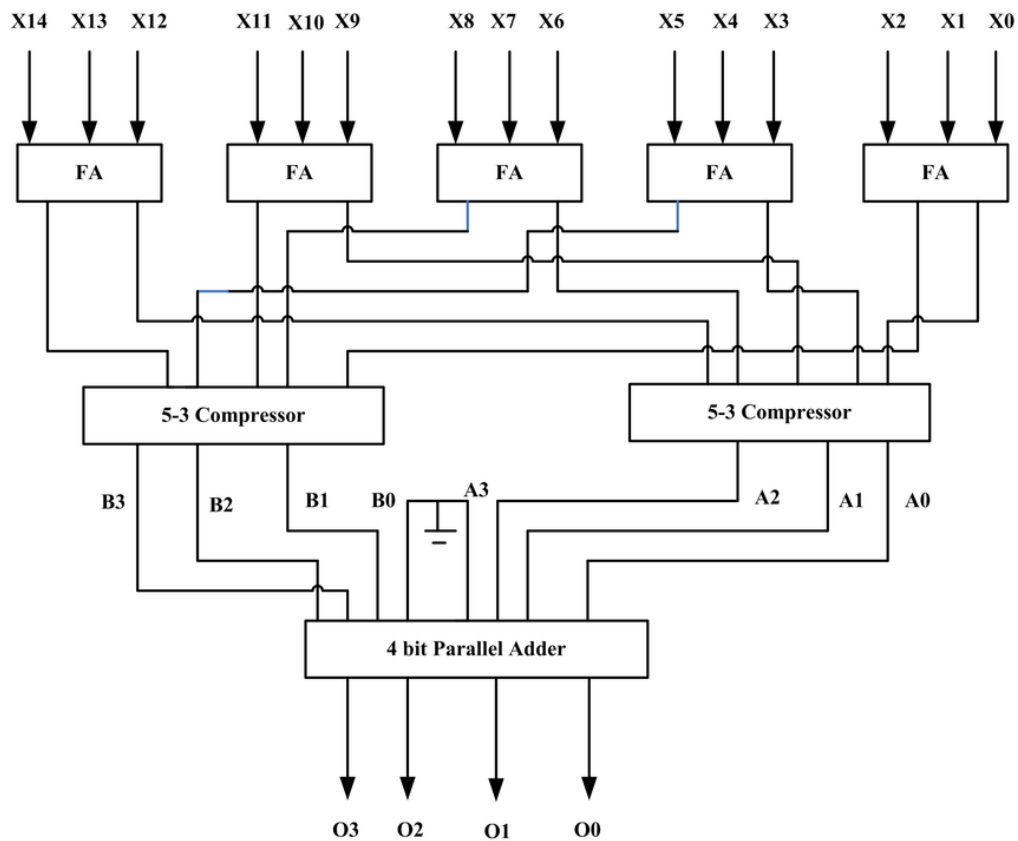


Fig 3: Proposed system

The inactivity in the CSA tree multiplier can be diminished by diminishing the quantity of adders in the fractional items decrease stage. In the proposed design, 4-2 blower is utilized for understanding the decrease in the quantity of fractional item expansion stages. The joined elements of low force, low transistor check and least defer make the 4:2 blowers, the suitable decision. In this blower, the yields created at each stage are proficiently utilized by supplanting the XOR hinders with multiplexer squares so the basic way delay is limited. The different snake structures in the ordinary design are supplanted by compressors.

The standard usage of the 4-2 blower is finished utilizing 2 full viper cells as appeared in fig 9. at the point when the individual full adders are broken into their constituent XOR squares, it tends to be seen that the general postponement is equivalent to 4 xor entryway delay. The square outline in Fig 10. shows the altered XOR entryway engineering for the execution of the 4-2 blower with a deferral of 3 xor door delay. Along these lines supplanting proposed xor door circuits brings about a critical improvement in delay.

#### IV. Simulation Results

Behavioral level simulation for various Booth MAC techniques was performed through ALTERA QUATRUS II simulator using verilog HDL to determine the adder multiplication result. The recoding schemes are developed based on modified Booth algorithm such as two stages MAC; carry save Booth MAC, PNQ Pre-coder and SMB techniques. By using these above mentioned recoding techniques, the add-multiply operation are developed from Proposed 4-2 compressor based modified CSA tree and prior CSA tree.

The performance of proposed CSA based add-multiply operations are compared with various prior techniques. The adder multiplications techniques are derived for various data length such as 8bits, 16bits and 32bits. These result obtained from various bit length are tabulated in Table II, Table III and Table IV respectively

TABLE II PERFORMANCE OBSERVED WHEN 8BIT LENGTH

Booth Multiplier	Time (ns)	Power (mw)	Area (LUT)	PDP ( $10^{-9}$ )
SMB1 Proposed	8.849	321.79	78	2.86071
SMB2 Proposed	8.827	321.72	86	2.83982
SMB3 Proposed	8.959	321.72	86	2.87939
SMB1 Existing	10.201	324.94	79	3.31471
SMB2 Existing	10.243	324.91	88	3.32805
SMB3 Existing	10.243	324.91	88	3.32805
Two stage decoder	12.314	390.77	96	4.81194
CA Booth recoder	12.337	384.81	90	4.70892
PNQ Precoder	12.822	382.64	96	4.52357
Ripple carry adder	13.300	372.68	99	4.95664

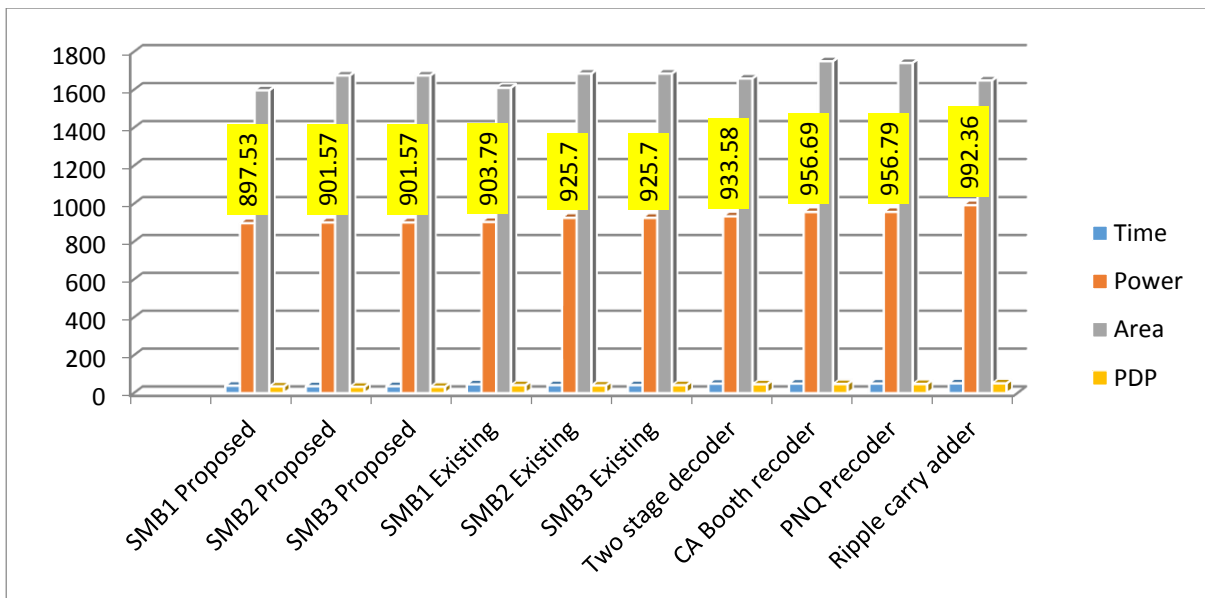


Fig 4: Comparison for 8bit length

TABLE III PERFORMANCE OBSERVED WHEN 16BIT LENGTH

Booth Multiplier	Time (ns)	Power (mw)	Area (LUT)	PDP ( $10^{-9}$ )
SMB1 Proposed	20.782	423.86	369	8.8086
SMB2 Proposed	20.028	421.41	402	8.4399
SMB3 Proposed	20.028	422.97	402	8.4712
SMB1 Existing	22.849	443.79	374	10.1402
SMB2 Existing	21.449	427.19	406	9.1627
SMB3 Existing	21.449	438.23	406	9.3995
Two stage decoder	23.289	513.77	414	11.9652
CA Booth recoder	23.339	513.98	438	11.9958
PNQ Precoder	23.094	509.69	442	11.2611
Ripple carry adder	24.113	549.86	412	13.2583

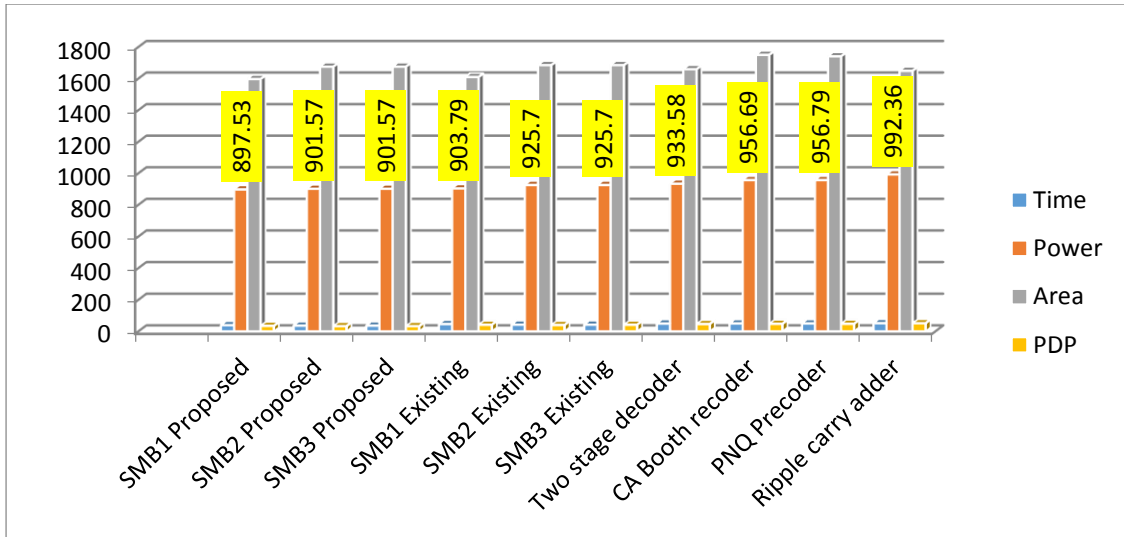


Fig 5: Comparison for 16 bit length

TABLE IV PERFORMANCE OBSERVED WHEN 32BIT LENGTH

Booth Multiplier	Time (ns)	Power (mw)	Area (LUT)	PDP (10 <sup>-9</sup> )
SMB1 Proposed	38.906	897.53	1597	34.9193
SMB2 Proposed	36.418	901.57	1675	32.8333
SMB3 Proposed	36.484	901.57	1675	32.8928
SMB1 Existing	46.069	903.79	1610	41.6367
SMB2 Existing	41.984	925.70	1685	40.1657
SMB3 Existing	41.984	925.70	1685	41.6632
Two stage decoder	49.464	933.58	1659	46.1786
CA Booth precoder	49.878	956.69	1750	47.7178
PNQ Precoder	49.997	956.79	1741	47.8366
Ripple carry adder	51.513	992.36	1649	51.1194

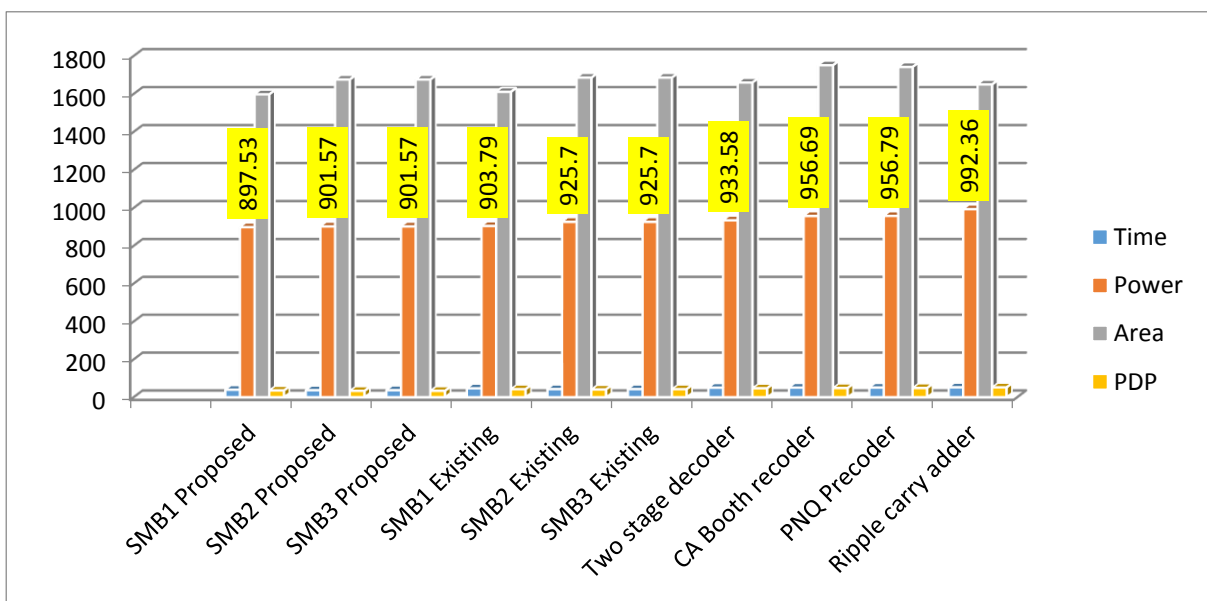


Fig 6: Comparison for 32 bit length

While comparing the add-multiplier design in multiple bit length, the proposed work provides considerable reduction in delay, power and also the power-delay product in proposed CSA based add-multiply techniques.

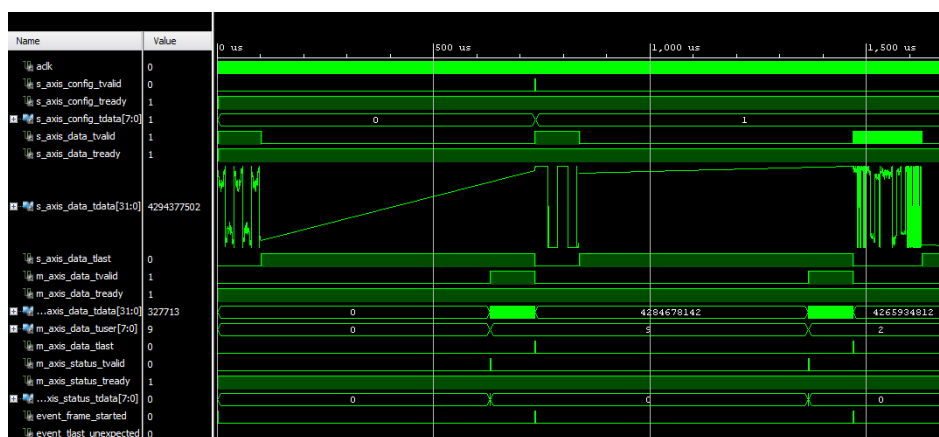


Fig : Output waveform of proposed system in FFT calculation

## V. Conclusion

The Fused-Add Multiply (FAM) operator is proposed to develop a high-speed, low-power Modified Booth adder multipliers design. This is an organized method for the immediate recoding of the total of two numbers to its MB structure. There are three elective plans of the proposed S-MB recoder and it has been contrasted and the earlier ones, for example, a two-phase recoder, convey spare corner recoder and PNQ Precoder. The proposed plans that are actualized by the utilization of Modified corner ADD-Multiply administrator and 4:2 blower adders are joined in FAM structures yield a superior presentation in power and basic way delay.

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