Design and Analysis of Low Power Hybrid Braun Multiplier using Ladner Fischer Adder

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Article History

Article Submission
22 April 2017
Revised Submission
21 June 2017
Article Accepted
16 August 2017
Article Published
30 September 2017

Abstract

Multiplier is important in many DSP systems and in many hardware blocks. Multiplier are used in various DSP application like digital filtering, digital communication. This needs parallel array multiplier to attain high speed for execution and better performance. A specific array multiplier is implemented known as Braun design. Braun multiplier is the one which is a kind of parallel multiplier. It contains different CSA count of AND gates. Braun multiplier employing Ripple Carry Adder is developed here having high speed PPA. It will reduce the delay and implemented using Tanner EDA tool.

Keywords: *Parallel prefix Adder, Ladner Fischer adder, PPA, CSA*

I. Introduction

The performance of the system is determined by performance of Multiplier. Multiplication is most important among all arithmetic operation. Implementation of VLSI system depends majorly on the multiplication and digital signal processing .In high performance system such as microprocessor multiplier plays a major role. Multipliers require more power to be employed in applications involving DSP. In the low power VLSI design low power multiplier design is necessary. Researchers are trying multiplier which offers high speed, low power consumption [1][2].

Multiplication of nxn bits is traditionally calculated by three stages. They are producing partial products, carry – free decrementing of partial products and propagation of carry addition. The partial product generation is usually a specific time of operation. The minimum delay in the PPR is of the order of log n. addition of partial products becomes fast by using fast adders [3][4].

Occurrence of the disturbance in the speeding up of addition is carry propagation. This gives more interest in the designing of arithmetic circuits. DSP Application depends not only on the computational capacity also on the power consumption. The area and performance are major consideration but power consumption has more preference than that. In VLSI, low power systems are necessary because of two reasons. In the first case, with operating frequency which is gradually becoming more and more and increase in chip processing capacity, more currents should be derived and heat should be eliminated by employing appropriate cooling approaches. In the second case, battery is limited in electronic devices which are portable and designs of low power results in large operating times [5][6].

II. Existing method

It is the one which is mostly employed for binary addition and best suitable for implementation of VLSI. Binary addition is a standard and repeatedly employed ALU operation. Also, the method discussed here is a balanced

ISSN: 2250-0839

one and is similar to CLA. Prefix adders are developed in many ways which will be dependent on their requirements. This might be used for generating the carriers. We employ tree structure to increment the speed of ALU functionality. PPAs are employed in better performed ALU architectures and are very fast adders [7]. Three steps addition by PPA is as follows.

In the first stage, we evaluate and transfer signals that are provided to produce input(A and B) for the carry in each adder. They are expressed by the following:

$$Si=Ax\ Bx. \quad (1)$$
$$Ti=Ax\ .Bx. \quad (2)$$

In the second stage, we evaluate carry that corresponds to each and every single bit. Simulation is performed in parallel manner. And after that, we divide them into tiny pieces [8][9]. Here, a Carry consists of OR gate (one), AND gates(two). Finally transfers signals from the intermediate stage that are expressed as follows. In the final stage, we evaluate the bits at the input are added and it is similar for all adders and is expressed by

$$Ui= Si\ Ci \quad (3)$$
$$Ci+1=(Si\ .C0) + Ti\ldots \quad (4)$$

Below figure 1 shows a 2-bit Kogge- Stone adder.

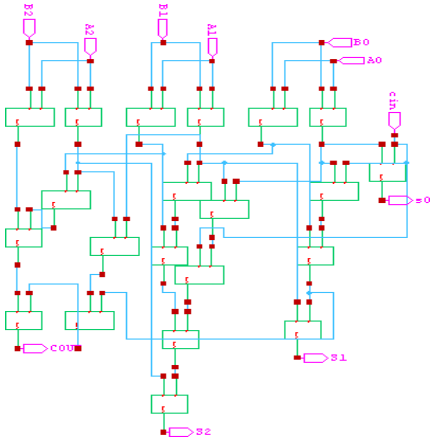

Fig 1 : Design of 3-bit Kogge-stone adder

Brent-Kung adder is also type of PPA that was developed by Brent and Kung in 1992. It is necessary to have less area and more logical depth [10]. Here, tree architecture was developed to compute each power of carry. Complexity is low in comparison with that of KS adder. It was developed by R. Ladner and M. Fischer in 1980. It has a benefit of minimum fan-out, low logical depth and is more spatial. Below figure 2 shows a 3-bit Ladner-Fischer adder

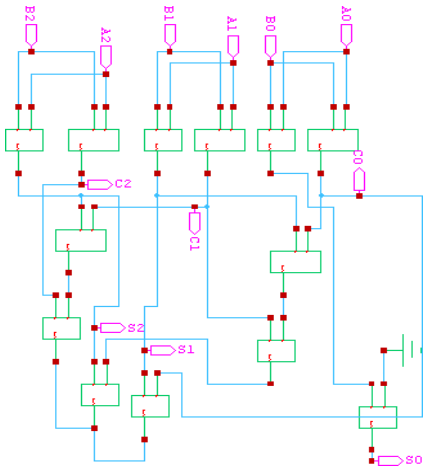

Fig 2 : Design of 3-bit Ladner Fischer adder

III. Proposed Work

This is also a parallel multiplier also known as carry save array multiplier. It cannot deal with signed bits and contains gates and adders. It is also known as non addictive multiplier. It has simple architecture when compared to other methods. Below figure shows the Braun's multiplier. In this multiplier, we employ PPA instead of ripple carry adder. This is shown in figure 3.

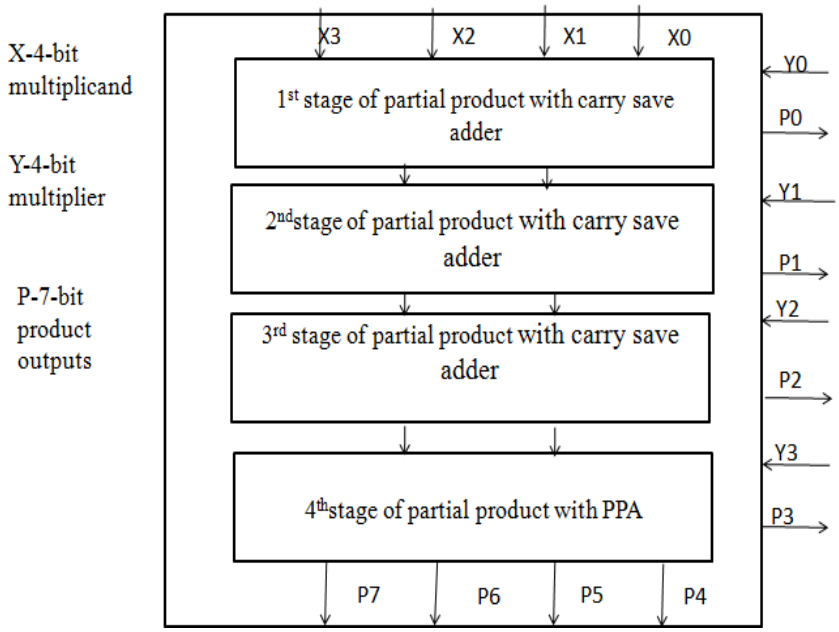

Fig 3 : Block Diagram of the Proposed Braun Multiplier

Products are generated based on each and every partial product that can be added in the next stage as a sum. It employs ripple carry adder which adds partial products in the final step. Here, we employ fast addition method. The circuit schematic is shown in figure 4.

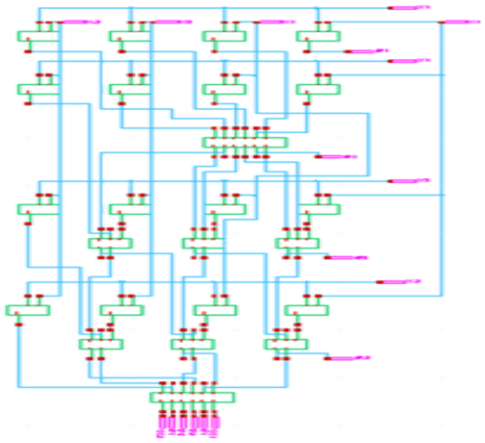

Fig 4 : Design of braun multiplier using Ladner Fischer adder

IV. Experimental Results

The simulations are performed using TANNER EDA tool at 130nm technology. Kogge-Stone adder is a type of PPA that develops CLA adder. It is design which generates is very fast adder. It is the key aspect in many VLSI Implementations. It is equipped with fewer inputs and is more spatial. It is employed to perform addition operation and produces less delay. Generated bits are XORed with starting inputs to get the sum bits. Count is evaluated by employing 2(n-1) -Log2n. LF adder is also type of PPA that forms a carry look ahead adder. It is represented as parallel prefix graph containd carry nodes. To produce carry signals, time needed is given by o(log n). It is mostly employed in adders which are of high performance. The braun multiplier is successfully implemented using kogge-stone adder. The output of Braun multiplier using kogge-stone adder is shown in figure 5.

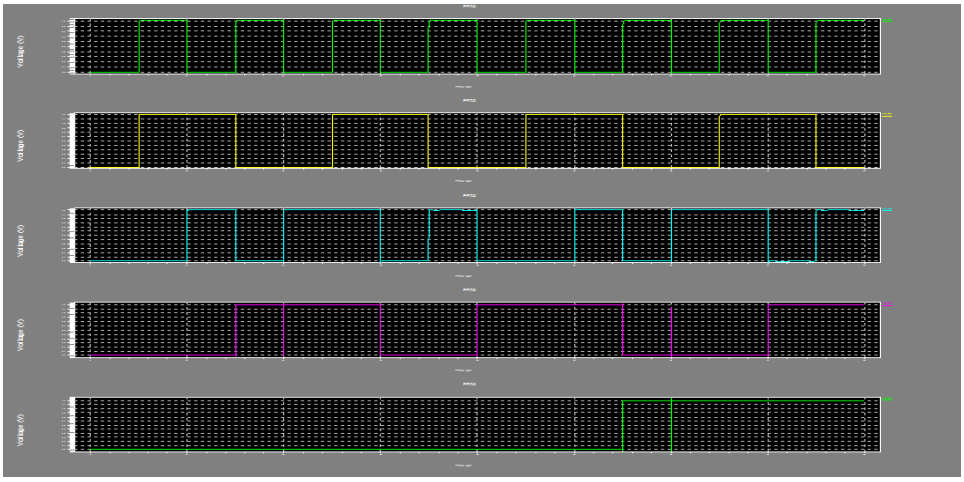

Fig 5: Output of Braun multiplier using kogge-stone adder

The output of Braun multiplier using Ladner Fischer adder is shown in figure 6.

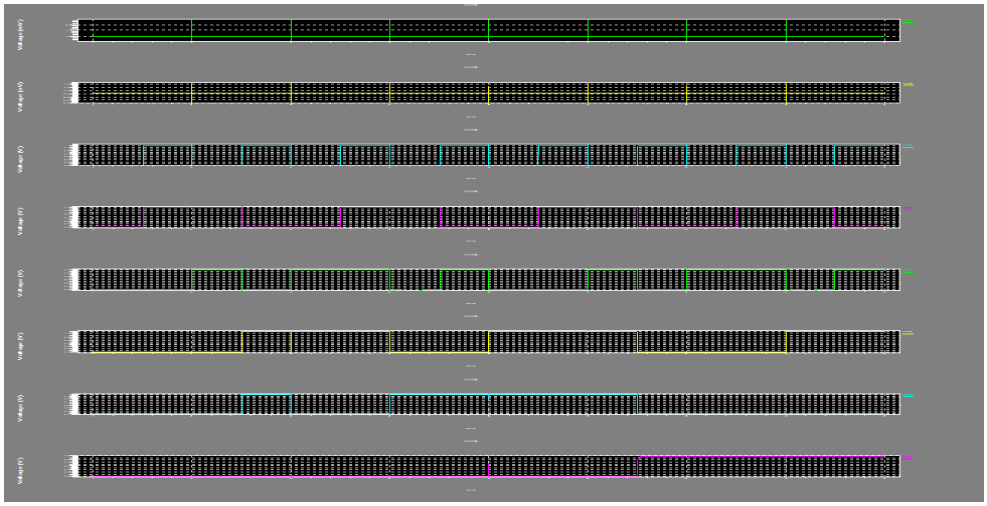

Fig 6: Output of Braun multiplier using Ladner Fischer adder

Table 1: Comparison of multiplier using various adders

Braun Multiplier	Power(mw)	Delay(µs)	PDP(nJ)
Using kogge stone adder	1.07	0.64	0.68
Using Brent kung adder	0.0020	0.52	0.001
Using Ladner Fischer adder	0.0017	0.62	0.002

The comparative chart showing the variations of proposed multiplier and conventional approach is shown in figure 7.

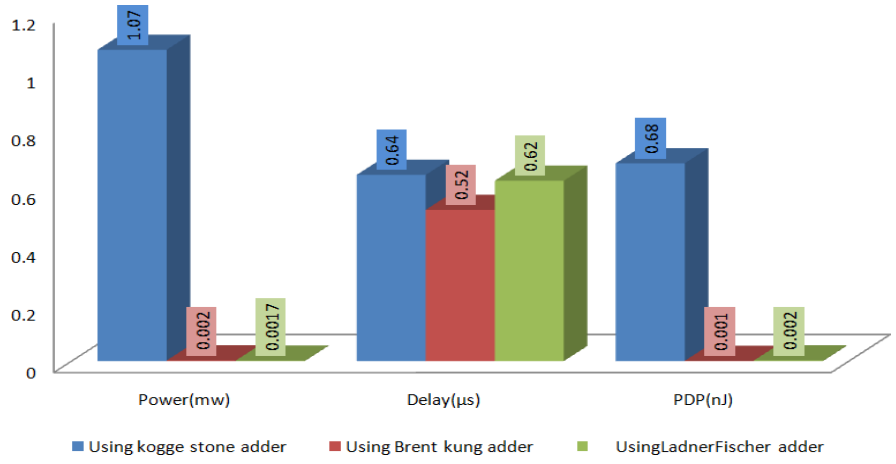

Fig 7: Comparison of Braun multiplier in different adders

V. Conclusion

From the analysis made above we can come to a conclusion that the Braun multiplier employing the parallel prefix adder have reduced the delay due the ripple carry adder and also among the above parallel prefix adders braun multiplier using the Ladner Fischer adder consume low power. All the simulations are performed using Tanner EDA at nominal operating conditions. The proposed method shows 60% improved results than conventional approaches.

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ISSN: 2250-0839