Design and Analysis of Low Power Dual Edge Triggered Mechanism Flip-Flop Employing Power Gating Methodology

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Abstract

The advancement of battery operated designs has abundantly increases the memory elements and registers to be operated in ultra-low power. That is the this paper we have proposed a design of CT_C DET flip-flop with power gating technique which is the most efficient power consuming reduction technique. The design of the power gating technique involves the pull-up transistor in the V_{dd} of the circuit and pull-down transistor in the ground terminal. This power gating technique reduces the power consumption by more than 40% than that of the existing design.
Keywords: *DET flip flop, low power consumption, power gating*

I. Introduction

The advancements in battery powered devices abundantly increasing these days. These increases in the small power consuming devises increase the importance of sub threshold operating devices are most needed to support the battery operated devices. Generally, chips having high performance will have frequency of the clock which is high [1][2]. Also, integration density will be more and more. So, these chips have a tendency to dominate in terms of consumption of power. Hence, these designs can perform better and low power is consumed. Dissipation of power are of three types in traditional CMOS circuit. First one is the switching power that refers to the dissipated power while signal transitions occur. Here, the energy is taken from the voltage source in charging the capacitances. Second one is the Short-circuit power [3].

Employing a pulse signal to double edge-triggered flip- flops needs many transistors to attain better performance. Among them, most of the transistors are linked to the clock signal that may increments a factor called as activity factor α. Also, increments the consumption of power. So, we employ dual data-path for further implementation. Transmission gates are employed to limit the unnecessary voltages which makes pass transistors to have low logic signals. Rather than employing two inverters and one transmission gate, when PMOS and NMOS are subsequently in the CMOS logic. MOSFETs are the one which has reverse leakage which is not zero & current which is sub- threshold effects leakage power consumption we use DET-FF as an inverter and PMOS which keeps the logic level [4][5].

An innovative flip flop known as high speed dual-edge triggered that is a flip-flop to increment the consumption of power by decrementing α. In this proposed work, we use C- element which is a flip-flop that is involved. This will help in limits the disadvantage of switching activity and attaining improvement in 12.5% data activity in comparison with the other designs. Moreover, speed, area is benefited about 5%, 12% subsequently. This paper is presented in four distinct sections where the existing work was discussed in Section II, and Section III deals with the proposed DET flip flop. The results and analysis of the existing and proposed designs are discussed in the Section IV. The Section V concludes the work and talks about the future work [6][7].

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II. Related Work

Below figure shows about conditional-toggle CT_C DET flip-flop design. CT_C flip-flop outline contains twenty transistors. These involve input transistor, output transistor and clock buffer transistors [8]. A flip-flop contains a C-element (output) and a latch which gives dynamic behavior of the design. The important aspect of CT_C flip-flop is that the latch's state does not alters which results in dissipation of energy during low switching. C-element is the output one that is preferably depends on weak-feedback that is implemented and observed in figure below. Circuit containing the latch component toggles the signal at X immediately next to transitions of the clock. Also, if D≠Q, Q is kept between clock transitions. Latch component contains two inverters attached end-to–end and output of a multiplier which is bi-directional is attached to X.

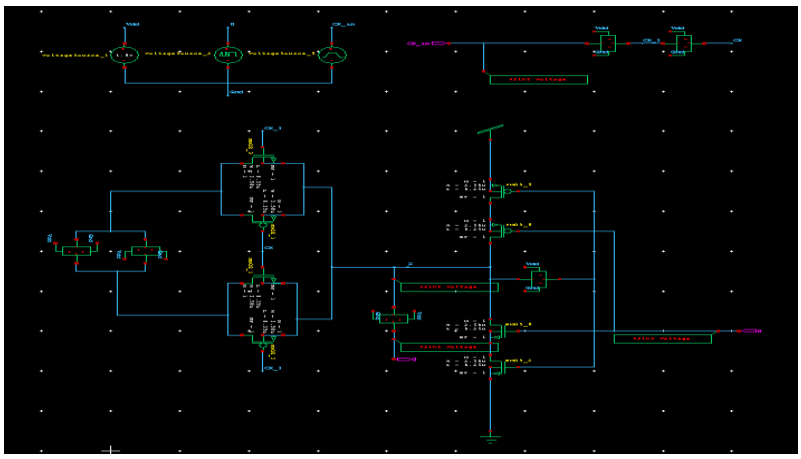

Fig 1: Conditional-toggle CT_CDET flip-flop.

CT_C flip-flop functioning is discussed by employing voltage signals that are simulated. Multiplexer is altered due to clock signal in between latch A and B next to each clock transition. Between these transitions of a clock, multiplexer switching is opposite to the latch that toggles X and Q if D≠Q prior to clock edge. If D= Q during clock edge, now the latch toggles the value that is stored and is not X due to C-element thrashes X to D.

Latch is the one here it toggles the value stored next to clock edge only when D=Q. CT_C flip-flop is the one moves across dissipation of power between high and low and delay in the circuit. Standard inverters in a latch switch the output speedily by having a small impact on the energy of switching. Moreover, high energy that takes to alter the state of the latch. CTF_C flip-flop is a modified CT_C flip-flop which does not alter the transitions is shown in below figure. CT_C flip-flop signals are strengthen at nodes A and B that depends on D. If D≠Q, Node D is strengthen by a multiplexer at node X using C- element. In the next transition, node X to low logic D is multiplexed very quickly with the cost of low energy [9][10].

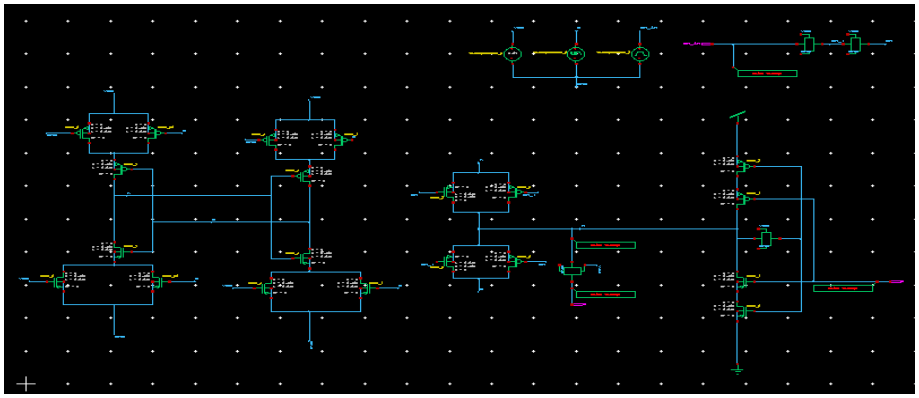

Fig 2: Conditional-toggle CDFF flip-flop.

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III. PROPOSED METHOD

The design is modified by using the efficient power reduction technique that is power gating. This technique is the one which is a noteworthy power reduction methodology that is involved in reduction of power in the digital ICs. Power gating is the one which is employed in an IC design for the reduction of consumption of power. This is done by closing the blocks of current in the circuit which are not used. Also to reduce leakage power, it has the advantage of Iddq test. It has more considerations for time concern during implementation. The below points are taken into consideration for this technique.

a) *Power gate size:* It is chosen to control the current during switching time. Also, the gate taken is larger so that no IR should be dropped in this one. Gate size according to thumb rule must be around thrice the switching capacitance. We also go for opting between PMOS (header) or CMOS (footer). Generally, CMOS occupies less area for the similar current during switching.

b) *Gate control slew rate:* Here, we determine the efficiency of power gating. If the slew rate is bigger, it uses more time to switch between ON and OFF. Thereby, efficiency of power gating is affected.

c) *Simultaneous switching capacitance:* It refers to circuit that is switched subsequently where no power network integrity is affected.

d) *Power gate leakage:* here, gates are made up of active transistors, so to maximize savings of power reducing the leakage is the main concern.

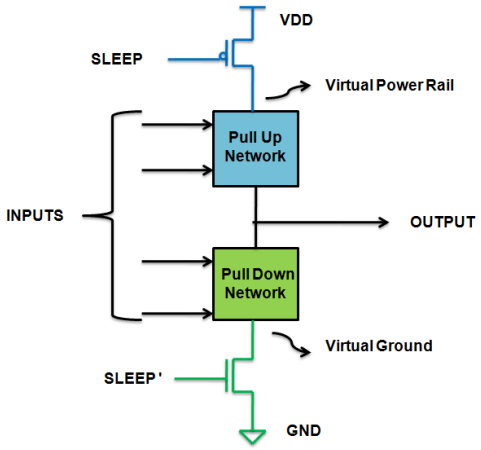

Fig 3: Schematic representation of Power gating technique

The important aspect of power gating is that it has two modes: an active mode, a low power mode. The idea is to switch between low power mode and active mode in preferable time slots and maximizing the savings of power. Here, we propose a flip-flop that involves a data path (up) which is responsible to the clock signal moving to the top and data path (low) which is responsible to the clock signal moving down.

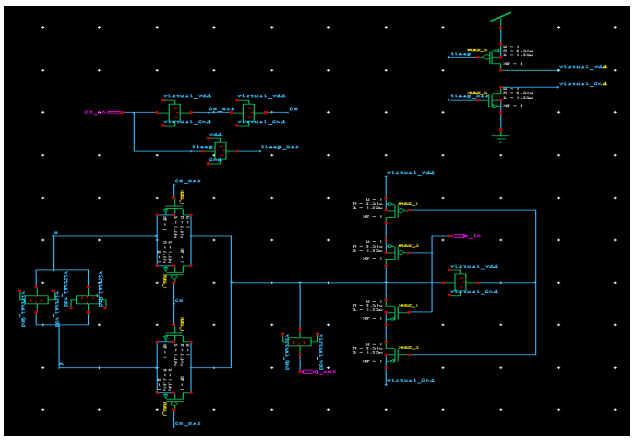

Fig 4: Proposed CT_CDET flip-flop with power gating technique

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Above figure 4 shows the proposed design. Coming to the operation, according to the clock signal the latch(up) transfers data to buffer output and according to the complementary clock signal latch(down) transfers data to buffer output. Clock input is present in the latch A that is inverted to activate the port in comparison with the latch B. D(two data) inputs given to the latches. These are given to 1 and 0 of a multiplexer that is attached to a clock. If Clk =0, latch A(up) identifies the input D whereas the latch B(low) has the present state. The multiplexer output chooses latch B output as a flip-flop output. If Clk =1, latch A has D input and the MUX chooses latch output as the next state. Similar operations are performed in a reverse manner that occurs falling edge.

IV. Analysis and Simulation Results

The design of various DET flip flops both the conditional-toggle CT_CDET flip-flop and proposed CT_CDET flip-flop with power gating technique are design in the TANNER Tools 13.0. The flip flops consisting of transistors design is designed using the s-edit tool and the simulated using the t- CT_C DET flip flop. Below figure shows the output of the CT_CD ET flip flop is forming the Flip flop and giving the operation. The design gives the functionality of a flip flop and the operation is explained in the previous chapter itself. Likewise the figure 6 shows the Existing CTF_C DET flip flop and the operation is explained in the previous section.

The proposed CT_CDET flip-flop output along with power gating method is observed in the figure above. Also, the functioning is discussed in the above chapter. From the below figure, it is straight that the result of CT_CDET flip-flop is most effective in terms of accuracy in comparison with that of existing methods.

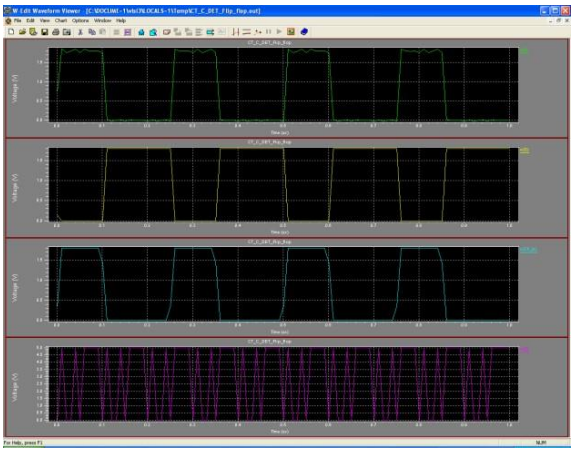

Fig 5: output of the Existing conditional-toggle

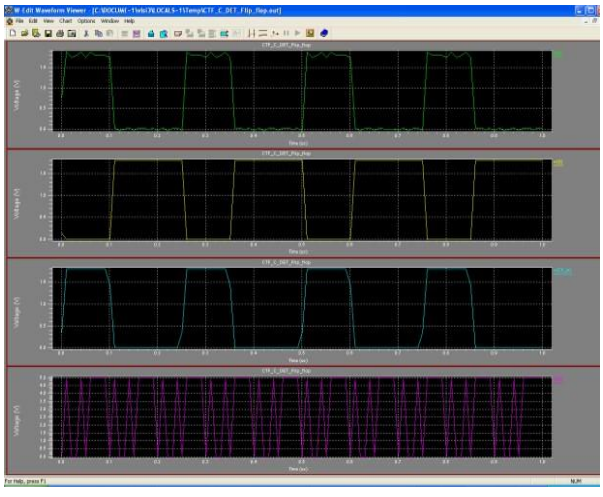

Fig 6: output of the Existing conditional-toggle CTF_C DET flip-flop

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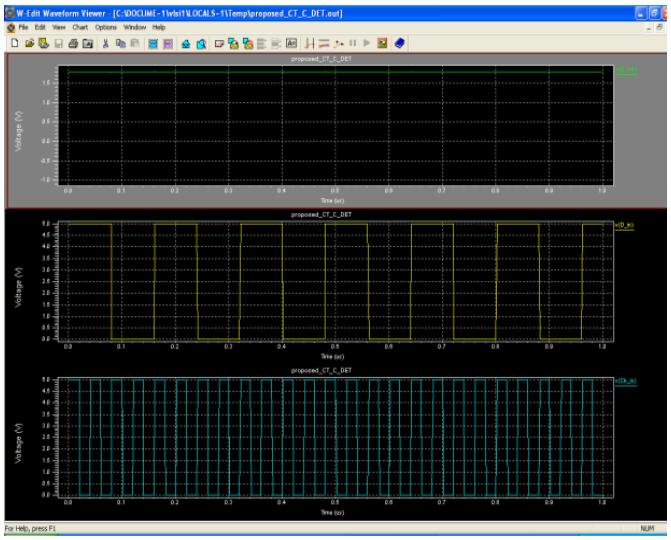

Fig 7: The output of the proposed CT_CDET

The power comparison of the existing and the design discussed is listed in the given table 1. Above tables makes clear about the designed flip-flop is very much less than that of the existing designs.

TABLE 1: Comparison of the existing and proposed design

Parameters	Existing CT_C DET Flip flop	Proposed CT_C DET Flip flop
MOSFETs	20	24
Total Nodes	13	17
Average Power Consumption	8.671685e-005 watts	1.841334e-007 watts

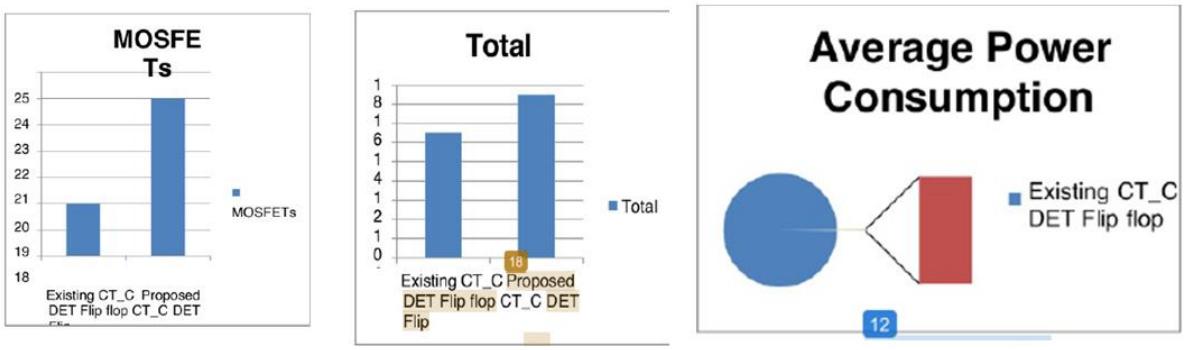

Fig 8: Comparison showing parameters of the existing and proposed design.

V. Conclusion

The design of CT_C DET flip-flop with power gating technique is the most efficient power consuming reduction technique which is discussed above. The design of the power gating technique involves the pull- up transistor in the Vdd of the circuit and pull-down transistor in the Gnd terminal. This power gating technique reduces the power consumption by more than 40% than that of the existing design. In future the flip- flop can be used in a memory design or some other flip- flop applications such as LFSR, counters, etc.

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