Design and Analysis of High Speed Low Power Hybrid Adder Using Transmission Gates

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Abstract

Addition is the vital arithmetic operation and it acts as a base for many arithmetic operations such as multipliers, dividers, etc. A full adder acts as a basic component in complex circuits. Full adder is the essential segment in many applications such as DSP, Microcontroller, Microprocessor, etc. There exists an inevitable swap between speed and power indulgence in VLSI design systems. A new modified hybrid 1-bit full adder using TG is presented. Here, the circuit is replaced with a simple XNOR gate, which increases the speed. Due to this, transistor count gets reduced results in better optimization of area. The analysis has been carried out also for 2, 4, 8 and 16 bit and it is compared with the various techniques. The result shows a significant improvement in speed, area, power dissipation and transistor counts.
Keywords: *Hybrid adder, Transmission gates, Xilinx*

I. Introduction

Portable electronics has become the part and parcel of our daily activities. Increase in usage of electronic devices such as laptops, mobile phones demands low power VLSI for the efficient design of circuits. Battery technology does not have much advantage as the electronic technology [1][2]. It demands the reduced power, less number of transistor count and delay, etc. As a density of transistor doubles every two years, its threshold voltage is also reduced correspondingly. All these technologies lead to higher power consumption and it directly affects the battery life. An adder is a basic element in digital circuits. Though adders can be designed using many representations but the most common representation is based on binary numbers. Generally, 2's complement and 1's complement are used to represent signed numbers but the signed number requires more complex adder. Full adder has a greater concern when designing the large circuits. Because, it influences the power, delay, switching activity of the transistor, noise immunity and also a driving capability. Several full adders have been designed such as C-CMOS, CPL, 14T, 10T, etc. Each full adder has one advantage over the other. A modified hybrid 1-bit full adder is proposed and it is shown that it is efficient over the hybrid adders. The following sections study the different types of full adders and its advantages and drawbacks have been discussed with the proposed design [3][4].

Full adder is a combinational circuit whose sum is obtained by using xor gates. By analysis, it is shown that xor gate is much time consuming when compared to other logics. The xor gate is replaced with various logics for the efficient operation of the circuit and various designs of full adders are available in the market for the required applications [5][6]. As full adder is basic essential component of many applications, the designers has a major concern on this in order to reduce the power consumption, delay, area and speed [7]. Conventional CMOS full adder has 28 transistors in a basic CMOS topology. It uses mirror technique complementary CMOS structure. In mirror technique, PMOS is exactly the mirror image of NMOS that leads to a fully symmetric topology and it has a ease of design. CMOS proves to be better when compared to CPL in-terms of speed (20% faster than CPL), area, power consumption and power-delay products [6]. PMOS transistor has high input capacitance which leads to a high dynamic power consumption [8][9]. The major advantage of these FAs is its reliability to operate even at low voltages. The layout of this full adder is also easy to implement.

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II. Related Work

TGA is based on a transmission gates and it consists of a 20 transistors. There is also a contrary called TFA (Transmission Function Adder) consists of 16 transistors. It also uses the same transmission gate logic and its output has the same delay for sum and carry.. It results in a decrease of power and area. Voltage drop problem is eliminated but it doubles the number of transistors used for the design. It consumes less power and it is good in designing XOR and XNOR gates. The power consumption and power delay product are reduced significantly when compared to other existing adders. It is shown that the speed is better when compared to Static CMOS, CPL and in addition it has less number of transistors. But, when it is used in complex circuits it gives deprived performance as it has large number of internal nodes which automatically increases the parasitic capacitances [6]. The major drawback of this adder is that it uses buffer at its output due to its week driving capability. The addition of buffers results in a high power consumption. Though, it has been reported as a fastest adder so far and its layout also is simpler than conventional 28T full adder.

In this adder, sum is executed using a pass transistor logic and carry is executed using a transmission gate logic. The inverter used in this circuit leads to dynamic power dissipation. It has low power consumption and high operating frequency and it also has a better cascading capability [10]. It uses hybrid logic style for its operation. It has less number of transistors and power dissipating nodes. Its driving capability and noise immunity is less. It uses pass transistor logic to improve the reduced power and leakage. In this adder, the transistor count increases by four per adder cell. Due to this, threshold loss is reduced that exists in SERF (Static Energy Recovery Full Adder). It is also considered as the fastest adder and it is simpler than the conventional adder. But, the power consumption is larger when compared to 28T adder even though it performs faster.

10T SERF focuses mainly on energy consumption [2]. This adder recycles the charge and therefore less power is consumed when compared to other non-energy recovering logic. Due to this faster operation of XOR and XNOR gates are possible and there is also a balance of delays between the outputs [7]. It has no direct path connected to the ground that reduces the static power dissipation. It reapplies the stored charge to the control gates together makes it an energy efficient design. But, the output nodes have a full swing and it fails to provide this for the internal nodes. The power consumption reduces the operation of the circuit. This 10T SERF cannot be cascaded at low voltages as it has multiple threshold problems.

GDI based full adder reduces the power consumption, delay and area of the circuits and it also reduces the complexity of the logic design. It has less number of transistors and it results in reduced power consumption. It is used to implement a wide variety of logic functions by using only two transistors. It has a less static power loss and hence it has a dynamic power loss. If the XOR gate is optimized, the overall performance of the 1-bit full adder is improved. GDI cell uses two pins which make it stretchier than CMOS design. The major disadvantage of this adder is that it uses twin well CMOS process and SOI process to realize, which more expensive [5] is. If it is realized with a standard p-well CMOS process, it lacks with a driving capability.

The usage of two new adders consumes less power even in high frequencies and it has high speed compared to 10T full adders and conventional 28T CMOS full adders [3]. It performs faster with same power consumption. 8T full adder consists of three transistor XOR gate and a multiplexer with a total of 8 transistors. The design is obtained by modifying the CMOS inverter and the PMOS pass transistor. The delay is improved significantly. The power delay product and the area (less silicon area) are also better when compared to 10T and 14T adders. The noise margin is increased by the proper sizing of transistors in 3T XOR [10]. The threshold voltage loss is neglected. The disadvantage is that it has high power consumption due to the short circuit current.

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III. Proposed Hybrid Full Adder Using Transmission Gates

Static CMOS logic styles aims at implementing the low power and high performance 1-bit full adder cell. Various types of full adders had been studied in the previous sections, where each full adder is limited with the driving capability, power consumption, threshold problems, short circuit currents, internal nodes, parasitic capacitances, etc. The structure of the proposed FA using TG is shown in figure 1.

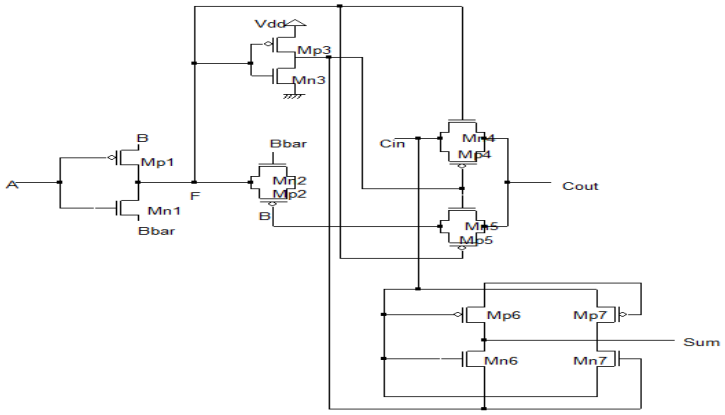

Fig 1: Hybrid Full Adder using transmission gates

In the proposed FA circuit, XNOR module is modified by 4 transistors instead of 6 transistors in the existing circuit. This module is considered to be most responsible for power consumption in an adder circuit. The XNOR module is designed to minimize the power and also to avoid the voltage dilapidation possibility. Fig 1, shows the modified hybrid 1-bit full adder. Various XOR/XNOR circuits have been reported so far. The XNOR uses only four transistors which results on a low logic swing. This is shown in figure 2.

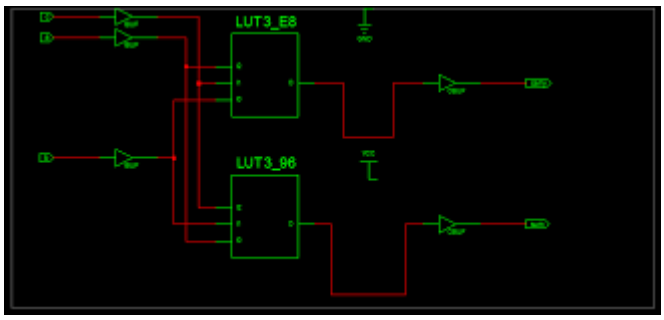

Fig 2: Schematic of Hybrid Full Adder using transmission gates

The carry is executed by the transistors Mp4, Mn4, Mp5 and Mn5 as in Fig 1. The C_{in} passes through a single transmission gate (Mp4 and Mn4), thereby reduces the proliferation path. In addition, the usage of strong TGs (Mp4, Mn4, Mp5 and Mn5) also reduces the overall propagation delay of the circuit. The proposed modified hybrid 1-bit full adder offers low power and high speed when compared with the existing techniques.

IV. Simulation Results

The devices that consume less power have more reliability than other strategy. The power utilization is an important factor in digital circuits. CMOS is well branded for its low power utilization. Each 1-bit FA is analyzed in-terms of propagation delay, power indulgence and PDP. The delay can be reduced by optimizing the transistor area of FAs without significantly improving the power consumption. The transistor counts are reduced as possible in all the adders and then it is simulated. The leakage power is also reduced using various techniques.

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The circuit is simulated using T-Spice based on various methodologies of full adder. The full adders using Complementary CMOS, mirror technique, transmission function adders, transmission gate adders, CPL, 14T and 10T are analyzed where each of the full adder is limited by the transistor count, area, delay, large output swing, power consumption, voltage drop, multiple threshold problems, etc. The simulation output is shown in figure 3.

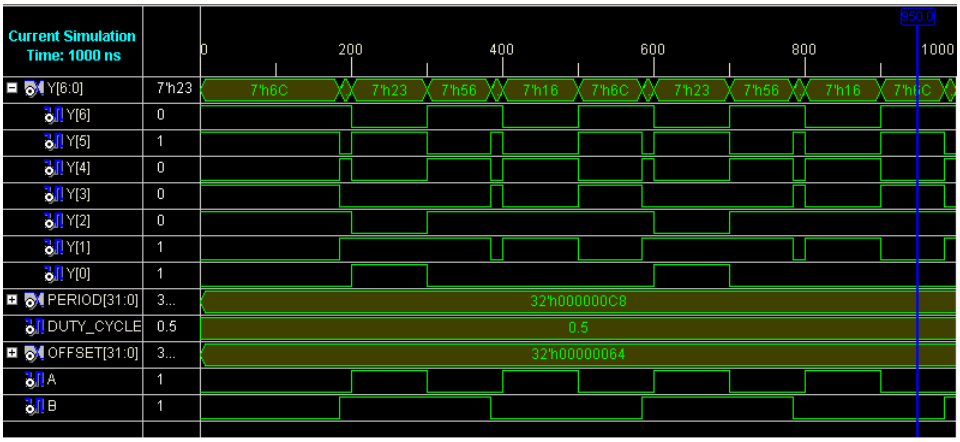

Fig 3: Simulation output of Hybrid Full Adder using transmission gates

The modified hybrid 1-bit FA has reduced power utilization, area, transistor count and delay as the XNOR module is modified. The layout of this FA is also simple when compared to the other FAs. The power, delay and power delay product and transistor counts are shown in Table 1, 2, 3 and 4.

TABLE 1: Comparison of Power for Various Techniques

Design	Power (µw)				
	1-bit	2-bit	4-bit	8-bit	16-bit
C-CMOS	6.219	6.226	6.237	6.226	6.228
Mirror	6.079	6.085	6.085	6.086	6.088
CPL	7.719	7.726	7.727	7.728	7.729
TFA	8.249	8.257	8.267	8.257	8.258
TGA	8.471	8.480	8.481	8.482	8.492
14T	12.727	12.739	12.740	12.741	12.752
10T	14.344	14.360	14.371	14.382	14.391
24-T	15.910	15.920	15.931	15.943	15.964
FA_Hybrid	5.978	5.983	5.991	5.994	5.999
FA_DPL	19.560	19.571	19.576	19.582	19.586
FA_CPL	20.780	20.791	20.792	20.793	20.802
Existing	4.156	4.160	4.175	4.179	4.186
Proposed	4.130	4.134	4.135	4.137	4.145

TABLE 2: Comparison of Propagation Delay of Various Techniques

Design	Delay(ns)				
	1-bit	2-bit	4-bit	8-bit	16-bit
C-CMOS	0.292	0.559	2.311	37.351	9568.23
Mirror	0.28	0.53	2.22	35.943	9207.78
CPL	0.183	0.341	1.439	23.399	5996.51
TFA	0.287	0.549	2.271	36.711	9404.39
TGA	0.293	0.561	2.271	36.711	9404.39
14T	0.381	0.737	3.023	48.743	12484.5
10T	0.132	0.239	1.031	16.871	4325.35
HPSC	0.273	0.521	2.159	34.919	8945.63
24-T	0.314	0.603	2.487	40.167	10289.1

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FA_Hybrid	0.252	0.479	1.991	32.231	8257.51
FA_DPL	0.226	0.427	1.783	28.903	7405.54
FA_CPL	0.220	0.415	1.735	28.135	7208.93
Existing	0.224	0.423	1.767	28.647	7340
Proposed	0.125	0.225	0.975	15.975	4095.97

The pace of the circuit is degraded by the number of transistors and the size of transistors. So, the no. of transistors should be reduced in order to make the circuit more efficient.

TABLE 3: Comparison of PDPs

Design	**Power Delay Product(J)**				
	1-bit	**2-bit**	**4-bit**	**8-bit**	**16-bit**
C-CMOS	1.815	3.480	14.413	232.54	59590.94
Mirror	1.702	3.225	13.508	218.74	56056.96
CPL	1.412	2.634	11.119	180.82	46347.03
TFA	2.367	4.533	18.774	303.12	77661.45
TGA	2.482	4.757	19.260	311.38	79862.08
14T	4.848	9.388	38.513	621.03	159202.3
10T	1.893	3.432	14.816	242.63	62246.11
HPSC	1.741	3.326	13.849	224.24	57770.88
24-T	4.995	9.599	39.620	640.38	164255.2
FA_Hybrid	1.506	2.865	11.928	193.19	49536.8
FA_DPL	4.420	8.356	34.904	565.97	145044.9
FA_CPL	4.571	8.628	36.074	585.01	149960.2
Existing	0.930	1.759	7.377	119.71	30725.24
Proposed	0.516	0.930	4.031	66.088	16977.8

V. Conclusion

In this paper, a modified hybrid 1-bit FA is proposed and it is also extended for 2, 4, 8 and 16 bit. The simulation is carried out using T-Spice and it is compared with other techniques such as C-CMOS, Mirror, CPL, 14T, 10T, TFA, TGA, 24T and also with the other designs. The result shows that the area is reduced due to the less no of transistor count and propagation delay is reduced as strong transmission gates are used. The power is consumed efficiently and it also results in a reduced power delay product.

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