Design and analysis of Low Power High Speed Pulse Triggered Flip Flop

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Abstract

The main important aspect is to outline a high speed and utilization of low power pulse triggered flip-flop and simulate the same. Also, we have to minimize leakage in the consumption of power in a flip-flop by employing pulse triggering technique that is adopted for clocks. Here, to solve the problem in the discharging path of the similar flip flop implementations, we employ signal feed through technique. The discharge time is reduced by the proposed method. This design out performs all the other similar pulse triggered flip flop implementation both in speed and power consumption. Now, it is implemented by employing Cadence Virtuoso Schematic Composer in 90nm GPDK. Simulation is done by a simulator known as Spectre.
Keywords: *High Speed, Low Power, Clocking.*

I. Introduction

Flip flops are the most important components in the memory, processor design and they are power hungry. They consume lot of power dissipation is more when the clock speed is more. A flip flop which is pulse- triggered contains a single-latch structure [1][2]. Flipflops employed in high-speed applications dependent conventional transmission gate and master–slave is less democratic than the above technique. Here, we assess the components like area, speed, power of above method in comparison with the orthodox type of P-FF outlines. Ep-DCO is an innovative method along with pulse generator is one of the semi dynamic flip-flops that are employed in very small critical paths with high speed. The main drawback of the design is to discharge energy in each internal node for a rising rim of the clock. Hence, it results in dissipation of power due to switching continuously. So, we are going for Conditional Discharge technique [3].

CDFF is the one that not only decreases switching activities inside, but produces the output with no glitches, also by managing the setup time which is going negative and small delay characteristics from D-to- Q. Ep-DCO is the one applicable for critical paths in terms of speed whereas CDFF is applicable for critical path speed and also no speed paths for utilization of energy in an effective way [4]. The above methods are also employed for the environment in low-voltage. Moreover, by employing threshold voltage escalating, the leakage power can be controlled which is very necessary. CDFF can also be implemented by employing MTCMOS with 1.0V, dual Vt methods in order to control the leakage power utilization [5].

Another technique is SCDFF which needs no pre-charging in the clock cycle every time. Also, in SCDFF data switching activity is based on switching activity that is very much less than that of switching activity of a clock [6]. Employing SCDFF is a better option for small area, high speed and low power functions. MHLFF is a Single Edge triggered Flipflop that reduces the dissipation of power. Consumption of power in clock tree is decremented by reducing half the frequency of the clock in MHLFF for a similar output [7]. Hence, MHLFF overcomes HLFF's activity of reducing power consumption by limiting node transitions which are unnecessary.

II. Conventional Pulse Triggered Flip Flop

Flip- flop operating principles of the above design is discussed here. If the arrival of the clock pulse and data transmission does not occur, then the passing of current through NM3 transistor that identifies the input level of the flip-flop from whatever driving attempt. Meanwhile, data at the input and feedback driven output takes

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opposite levels of the signal. Also, path of the pull-down transistor of Node x is OFF [8][9]. This is shown in figure 1.

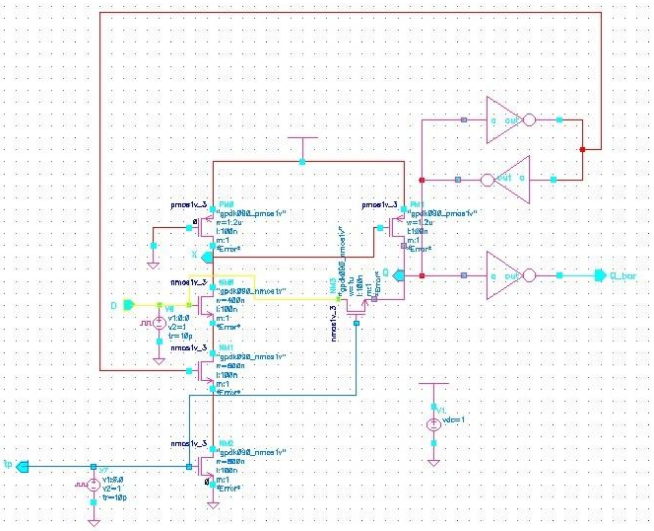

Fig 1: Existing P-FF Design

Therefore, switching of signals in any internal nodes does not occur. Otherwise, Node x discharges to ON the PM1 transistor during "0" to "1" transition of data and after Node Q is pulled to high. The effect loading is not important for the source at the input because NM3 is ON for a short period of time. Specifically, loss of energy is not due to delay in the critical path and reduces size of the transistor to increase the speed. Also, Node Q have a keeper logic that takes the duty of charging input source which is increased based on the keeper logic state that is inverted.

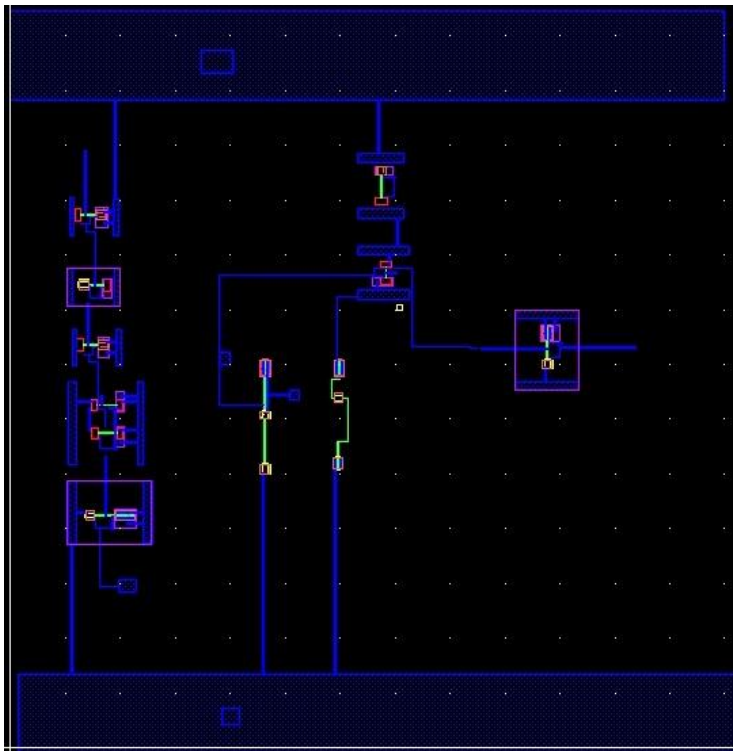

Fig 2: Existing P-FF Layout Design

III. Proposed P-FF Design

The figure 3 shows that the number of transistor is reduced compared to existing P-FF design. Q_feedback is removed so that the area and power are consumed. The width of the transistor is reduced. PM0 and PM1 are connected parallel; NM0 and NM1 are in series, through the pass transistor NM2 signal is feed through it. Continuously two 4 transistors in the form of inverters are designed. PM4 and NM5 output leads to Q_Bar, PM5 and NM6 output leads to Q.

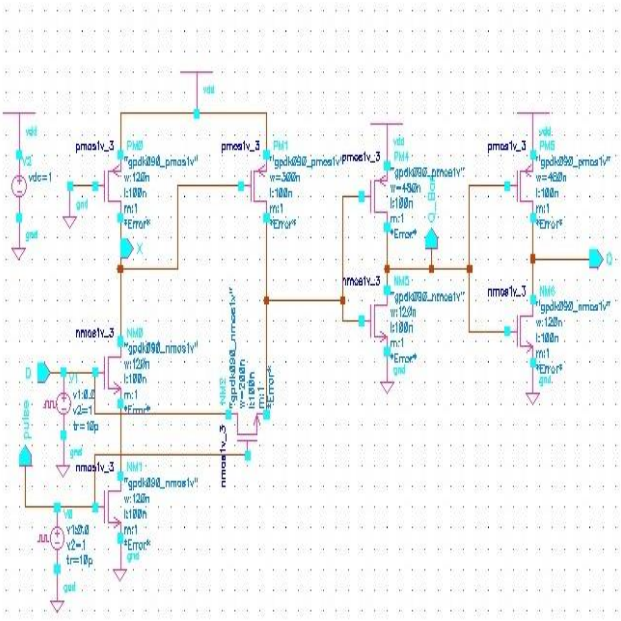

Fig 3: Proposed P-FF Design

The above figure shows the outline of P-FF design. Area of existing system is 86.14 Inches. The top and bottom rectangular box having yellow colour identifies VDD and GND. On the other hand outline of pulse generator is present. Yellow line indicates metal 1and wire is connected to the transistor and the blue wire indicates the poly i.e gate connected terminal. No DRC (design rule check) error found and LVS i.e (layout versus schematic) also verified. The layout is shown in figure 4.

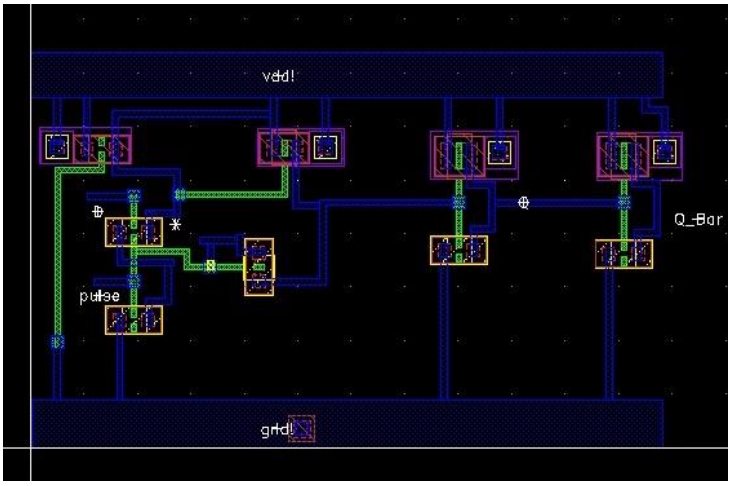

Fig 4: Proposed P-FF Design

Signal feed-through technique dependent low-power P-FF outline shows the disturbance in the delay connecting data zero and one. The outline directs to decrease the delay by employing the signal at the input straight to the

latch node to increase the speed of data transition. However, it is applied by employing a simple pass transistor that drives an extra signal. It decrements the number of transistors that are employed to design many logic gates by limiting the repeated use of transistors. Transistors are the one which are used as a switch to transfer logic 1 and 0 between the nodes. It decrements the count of devices which are active. Also, has the benefit of decreasing the levels of voltage i.e., 0 and 1 in each stage.

IV. Simulation Results

The proposed design is simulated by employing Cadence Virtuoso Schematic Composer in 90nm GPDK. Simulation is done by a simulator known as Spectre. Width of the pulse in a clock is 120ps, time period is 240ps whereas width of the clock pulse at the input is 400ps and time period is 800ps. The output waveforms are shown in figure 5 and figure 6 respectively.

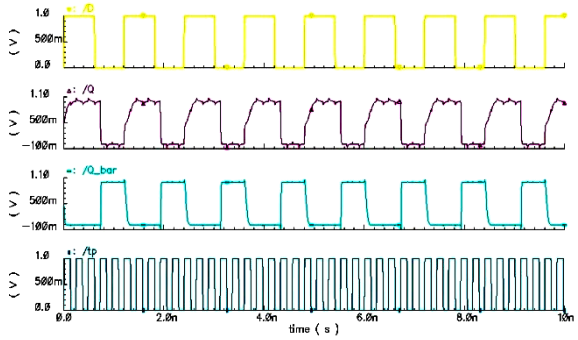

Fig 5: Existing P-FF Design output waveform

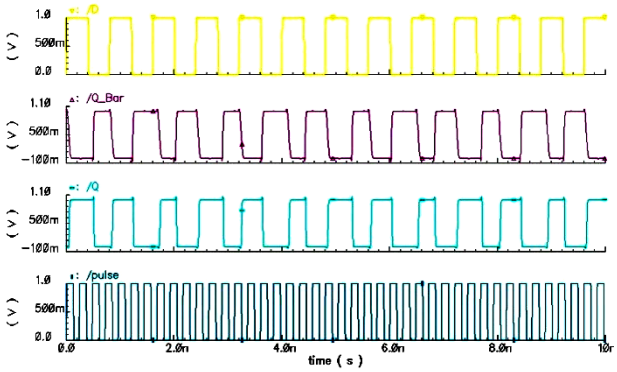

Fig 6: Proposed P-FF Design Output waveform

The below figure 7 shows the comparison of power leakage of conventional methods with the proposed P-FF outline. The proposed technique employing signal feed through technique gives better results in terms leakage of power in comparison with that of P-FF Design that already exists.

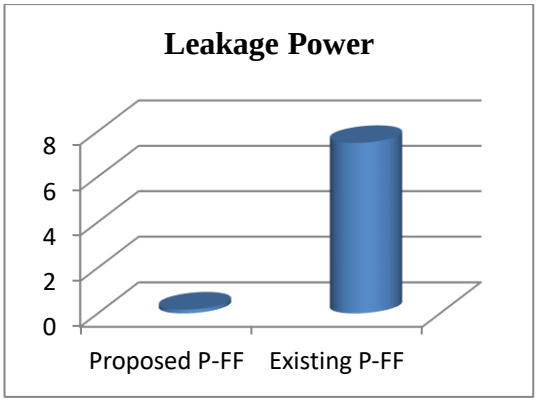

Fig 7: Schematic representation of Comparison of Proposed P-FF design Leakage Power with existing P-FF Design

Below figure 8 shows the comparison of the designed P-FF with P-FF design that already exists. The P-FF design employing signal feed through technique having average static power gives better results in comparison with that of P-FF Design that already exists.

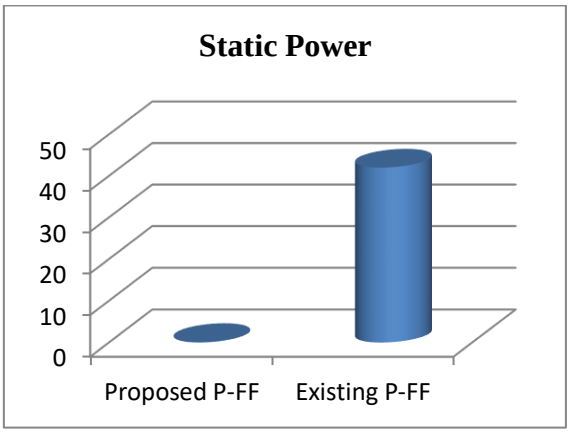

Fig 8: Schematic representation of Comparison of Proposed P-FF design Static Power with existing P-FF Design

Below figure 9 shows the comparison of the designed P-FF with P-FF design that already exists in terms of dynamic power. The P-FF design employing signal feed through technique having dynamic power gives better results in comparison with that of P-FF Design that already exists. The comparison of the designed P-FF with P-FF design that already exists in terms of delay. The P-FF design employing signal feed through technique having delay gives better results in comparison with that of P-FF Design that already exists.

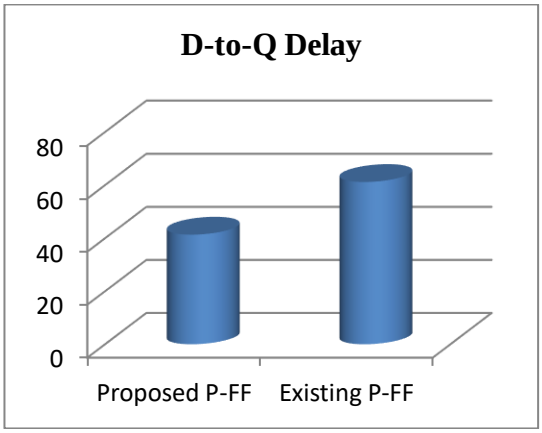

Fig 9: Schematic representation of Comparison of Proposed P-FF design Delay with existing P-FF Design

V. Conclusion

Employing signal feed through scheme in Pulse triggered flip flop have two aspects i.e., one is a pass transistor and the other one is a pseudo n-MOS logic. Source at the input has a signal feed through that transfers to the node inside a latch that has an extra driving signal to limit the time during transition, thereby gives low power and high speed. This is implemented by employing simple logic from pass transistor. Leakage power is decremented in this design which is proposed in comparison with conventional flip-flops. Also, dynamic and static powers are decreased in parallel. Therefore, we can say that the system designed in this paper is very much effective.

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