Design and Analysis of Optimized Fin-FETs

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Abstract

Semiconductor industry greatly depends on CMOS technology and now needs competent technology with handful benefits. This paper examines and analyzes the modern FINFET technology. This analysis is performed through 9 stages Ring Oscillator equipped with FINFET. Performance is analyzed by comparing the proposed structure with CMOS based 9 stage Ring Oscillator at the nano-scale level of abstraction.
Keywords: *Phase Locked Loop; Voltage Controlled Oscillator; CMOS Limitations ; FinFETs*

I. Introduction

In conventional CMOS transistor, electrically controlled gate separates source and drain. When Voltage is applied to gate, conductive channel is formed and electrons move from source to Drain, Similarly When the voltage is removed the current should completely cease ,however in CMOS transistor there will be substantial leakage when turned off and fortunately leakage current increases with every generation of transistor and also affects the growing proportion of power consumption [1][2].

Techniques such a High-k dielectrics reduces the leakage but it's not a complete solution. Material Innovation is increased, the performance by Stretching the silicon crystal structure increases current flow, and however they reached their limits. One Proposed solution is to radically reconstruct the transistor to improve gate's ability over the current; hence Fin-FET comes to the picture. Other Post technologies includes MESFET (metal–semiconductor field effect transistor), CNTFET (carbon nanotube field-effect transistor) however they are not completely credence for promising substitute [3][4].

The following points are the key features of Fin-FET type transistors (I) It has High Performance compared to CMOS (ii) Has Lower Leakage Current(iii) Reduced layout area (iv) Has Lower switching Voltage (v) Full gate controllability.

II. Related Work

constant miniaturization of MOSFET(Metal Oxide Semiconductor Field Effect transistors)corresponding to new generation of CMOS technology resulted in enhanced circuit performance and also ensured cost per function over the years, Though transistor scaling practically made up to 22nm regime due to fundamental process deadline. The main challenges in this tenure are : (a) minimization of Sub-threshold & gate leakage current (b) reduction in variability (device to device) to increase out turn. As discussed earlier Fin-FET are the promising alternative for current bulk CMOS technologies [5].

The Figure 1 shows the basic Fin-FET topology where it has a narrow silicon body where Tsi is the thickness .In Fin-FET current moves laterally with respect to the wafer, though the channel is formed at an angle of 90 degree to the plane of the wafer .Hence Fin-FET Devices are termed as quasi-planar [6].

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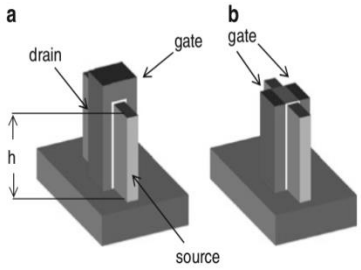

Fig 1: schematic representation of Fin-FET

Fin-FET has three types of terminal configuration namely Shorted gate type (Back gate and Front gate are tied together) and Independent gate(Independent signals made to drive back and front gate) and low power configuration(back gate is made reverse bias). The purpose of using Shorted gate type is to reduce the delay, similarly to drive high Id current independent Gate type is used and finally to reduce Leakage power and to maintain power consumption low power configuration is used. Among these three configuration Shorted Gate type can made as the direct alternative to CMOS, Since it's also a three terminal device [7] .

Phase locked loop or PLL are used in many areas in RF design .They are the main building blocks for RF Designers. They can be implemented in many ways, for example they can be used for FM demodulation, Signal re-constitution and Clock Recovery but widely used in frequency synthesizers. These Synthesizers allow Digital lines from circuits like Microprocessors to control the frequency, this gives the huge amount of Functionality and it also allows scanning digital frequencies. As the name coined, the operation of Phase Locked Loop is based on the Phase of the signals. To make it clear look at the basic sine wave which is illustrated below and look the different position on the waveform. A complete cycle can be viewed not only as a sine wave , but also a point rotating around the circle .Hence it can be said as Phase difference between them, and it can be measured in degree or in radiance [8].

The phase difference for two points on one waveform ,the phase difference can also measured between two waveform by taking the same point on each other waveforms and seeing the angle between them, this phase difference may change with time or it may remain the same . If it doesn't change means the two signals are moving around the phase of the circle exactly at the same rate. If they are moving at the same rate they must oscillate at exactly at a same frequency. The main point here is to note that the Phase difference is not changing, the frequencies are exactly the same .This is the concept behind the Phase locked loop. The fundamental blocks of PLL are Phase Detectors (PD), Voltage Controlled Oscillator (VCO) and loop filter . Another important element is Reference which is connected outside of the loop [9][10].

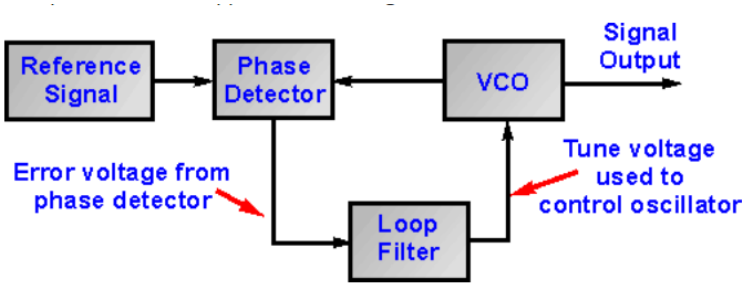

Fig 2: Schematic representation of phase locked loop

III. Analysis of Fin-FET technology

The main Function of Phase detectors is to take the signals from the reference and Voltage Controlled oscillator and produces a Voltage proportional to the phase difference between these two signals. There are several type of detectors, namely Phase only Sensitive and Phase frequency Sensitive. The next block is Voltage Controlled Oscillator; Where the Voltage is made to control the Frequency of the oscillator. As the output Frequency is proportional to the Voltage applied at the input on the controlled terminal, The main thing is it must always go up in in frequency for increasing voltage, If it bends or goes down which may happen in some circuits ,leads to instability to the loop. To overcome these types of causes RING OSCILLTORS are employed in Voltage Controlled Oscillators.

Finally Loop Filter, it's also one of the key element as it monitors so many loop characteristics, It is simply made up of one or more resistors and capacitors. The main Function is ,it attenuate the level of the reference frequency appearing at the output ,Its aim to provide a stable DC Control Voltage to VCO, it also controls the frequency transitions and finally governs the loop stability. Hence If we look the whole Phase lock loop ,there are three main blocks interconnected . As Phase Detectors takes the input from Reference Signal and VCO it produces the output proportional to the difference between them. This difference Voltage then Passes through Loop Filter to reduce the High Frequency Components and its further applied to Voltage Controlled Oscillator to control its frequency.

The Over Voltage from the phase detectors tries to reduce the phase difference between the VCO and Reference Signals. It draws the VCO frequency towards the response until there is a steady state of phase difference , If there is a fixed Phase Difference between the two signals means the frequency of the Reference and VCO are exactly same ,then the Loop will Lock, Also VCO requires the certain voltage to derive it to a right frequency and this indicates that there is always a phase difference between the reference and VCO. This type of operation can be used in many applications like FM Demodulators, Tuners etc.

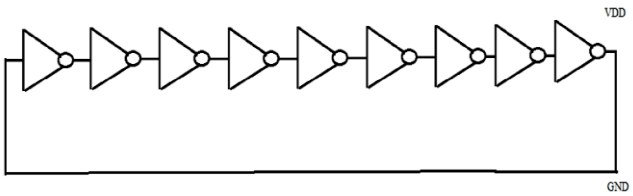

Fig 3: Schematic representation of the ring oscillator

IV. Simulation Results

To generate a waveform at a fixed frequency, Oscillators are introduced. There is much type of Oscillators Specifically Ring Oscillators can be made by connecting an Odd number of Inverters in a loop. In ideal case, The Loop of Inverters can change its state at constant frequencies. Here the period of oscillations is twice the sum of gate delays.

The main reason why it is used in VCO is (I) It can be designed with CMOS and BiCMOS Technology in a lucid manner. (ii) With Low power Dissipation it can generate high frequency oscillations.(iii)It can achieve its fixed frequency at low voltages also.(vi) Finally Due to its basic structure it generates Multiphase Outputs ,these Outputs can be functionally combined to analyze the Multiphase clock signals ,Which has many applications in Communication Systems. Figure 4 shows simulation of the 9-Stage Ring Oscillator.

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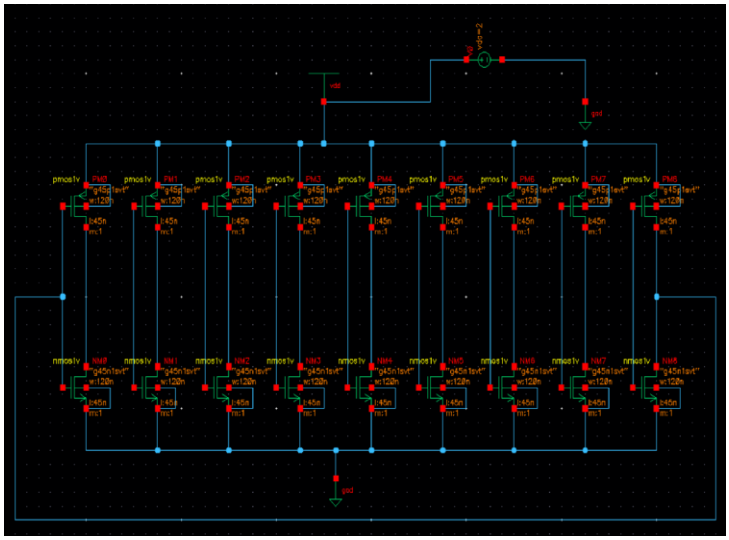

Fig 4: Simulation of 9-Stage Ring Oscillator with Fin-FET

Here the Systematic Representation of 9 stages Ring Oscillator is simulated using Cadence virtuoso and the Characteristics and device performance is analyzed. The waveforms are shown in figure 6.7 & 8 respectively.

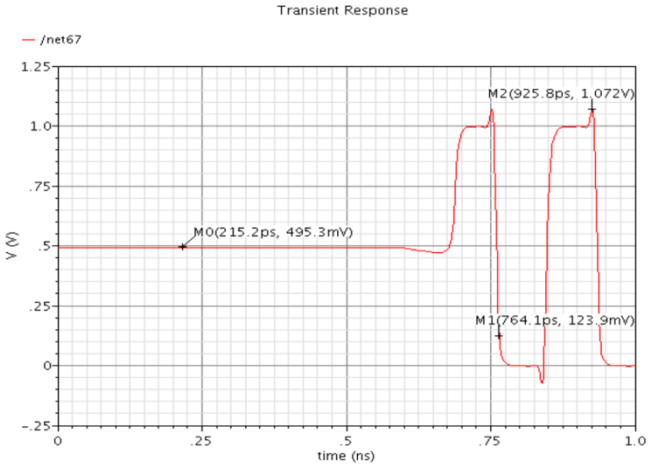

Fig 5: Waveform for Transient Analysis of 9 stages CMOS Ring Oscillator

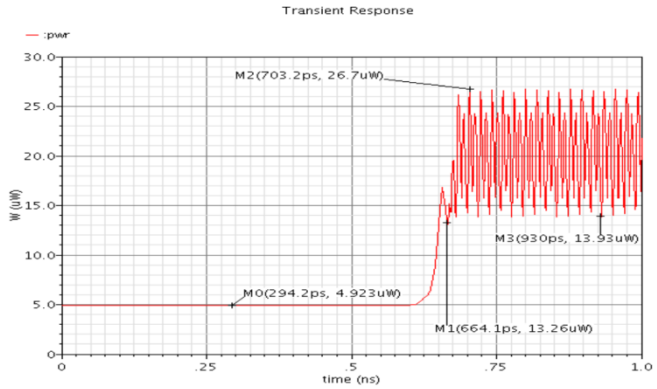

Fig 6: Waveform for Power consumption of 9 stages CMOS Ring Oscillator

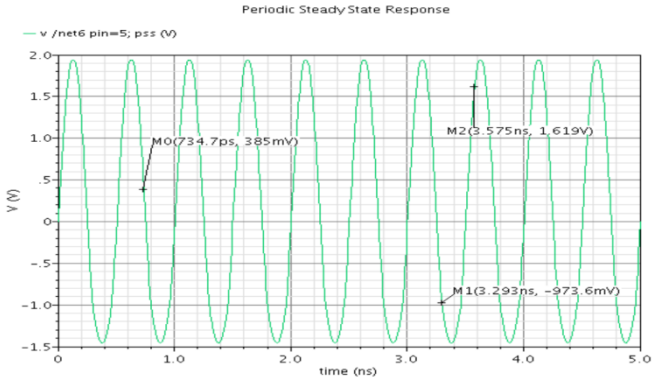

Fig 7: Waveform for Voltage of 9 stages CMOS Ring Oscillator

The Fin-FET model (45nm) is extracted from PTM which are based on BSIM-CMG models, the L-spice code is generated for 9 Stage Ring Oscillator and the waveform is plotted. This is shown in figure 8.

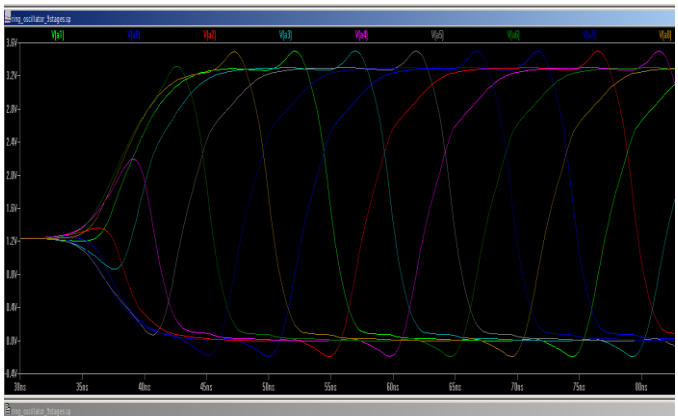

Fig 8: Overall Waveform for FinFET based Oscillator

V. Conclusion

Fin-FETs are the direct alternative for Bulk CMOS transistors. This Paper focused on the modeling of Fin-FET using the PTM Model files. Fin-FET model has been implemented by the advisable parameters .The sub-Circuit model of FIN Type transistors is successfully modeled and the performance of the device were studied. From the Result, It is clear that 45nm Fin-FET has lower power consumption and has better performance with optimum power consumption. Hence 45nm Fin-FET has better performance when compared to 45nm CMOS. The Characteristics of both 45nm Fin-FET and CMOS are successfully analyzed. In Fin type Transistors as the technology bond is decreasing, the size of the devices becomes smaller it occupy less space and has more efficiency.

References

[1] N. Weste and D. Harris, CMOS VLSI Design. Boston, MA: Pearson/Addison-Wesley, 2005.
[2] T.Weigandt, B. Kim, and P. Gray, "Analysis of timing jitter in CMOS ring oscillators," in Proc. IEEE Int. Symposium Circuits and Systems (ISCAS), 1994, pp. 27 30.
[3] Mak Kulkarni, Andrew Marshall, Weize Xiong, et, al. (2006, September), Ring Oscillator Performance and Parasitic Extraction Simulation in FINFET Technology, IEEE transaction on Solid State Device, pp. 176-182, September, 2006.

[4] R. Dreslinski, M. Wiekowski, D. Blaauw, D. Sylvester, and T. Mudge,"Near-threshold computing: reclaiming Moore's law through energy efficient integrated circuits," Proc. of IEEE, Vol. 98, pp 253-256, 2010.
[5] R. Moffat, P. Sen, R. Younker, and M. Bayoumi, "Digital phase locked. loop for induction motor speed control," IEEE Ind. Applicat., vol. IA-15, pp. 176182, 1979.
[6] A. W. Moore, "Phase-locked loops for motor-speed control," IEEE Spectrum, pp. 61-67, Apr. 1973.
[7] M. Mansuri and C. K. K. Yang, "A low-power adaptive bandwidth PLL and clock buffer with supply-noise compensation," IEEE J. Solid-State. Circuits, vol. 38, no. 11, pp. 1804–1812, Nov. 2003.
[8] T. Lee and W. Lee, "A spur suppression technique for phase-locked frequency synthesizers," in IEEE ISSCC 2006 Dig. Tech. Papers, Feb. 2006, pp. 592–593.
[9] D. Anandani, A. Kumar and V. S. K. Bhaaskaran, "Gating techniques for 6T SRAM cell using different modes of FinFET," 2015 International Conference on Advances in Computing, Communications and Informatics (ICACCI), Kochi, 2015, pp. 483-487, doi: 10.1109/ICACCI.2015.7275655.
[10] K. P. Pradhan, Priyanka, Mallikarjunarao, P. K. Sahu and S. K. Mohapatra, "Analysis of symmetric high-k spacer (SHS) trigate Wavy FinFET: A novel device," 2015 Annual IEEE India Conference (INDICON), New Delhi, 2015, pp. 1-3, doi: 10.1109/INDICON.2015.7443750.
[11] V. Moroz et al., "Modeling and optimization of group IV and III–V FinFETs and nano-wires," 2014 IEEE International Electron Devices Meeting, San Francisco, CA, 2014, pp. 7.4.1-7.4.4, doi: 10.1109/IEDM.2014.7047004.
[12] Y. Yang and N. K. Jha, "FinPrin: FinFET Logic Circuit Analysis and Optimization Under PVT Variations," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 12, pp. 2462-2475, Dec. 2014, doi: 10.1109/TVLSI.2013.2293886.
[13] R. Li, Y. Liu, K. Zhang, C. Zhao, H. Zhu and H. Yin, "Punch through stop layer optimization in bulk FinFETs," 2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Guilin, 2014, pp. 1-3, doi: 10.1109/ICSICT.2014.7021523.

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