Ancient Vedic Multiplication Based Optimized High Speed Arithmetic Logic

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Abstract

*Here, we deal with most effective Vedic multiplication method dependent 4*4 bit arithmetic logic unit having high speed. In this paper, we will perform ALU operations. ALU is a development of research work that has been done for years so we have chosen this topic. Normally ALU is a heart of digital processor, central processing unit, microprocessor and micro controller. Every digital domain based technology has to depend on the performance of ALU. Hence, there is a necessity of ALU which generates high speeds which depends on the speed of multiplier. Therefore, we go for designing a 4-bit multiplier. To generate high speeds, multiplier is employed which is one of the important blocks of the hardware unit and also an important initiation of delay in the path. We have studied many algorithms for multiplication technique but research says that Vedic multiplication is most effective of all in terms of speed. The algorithm contains 16 sutra, out of which we are employing URDHVA TIRYAKBHYAM and the code is written in Very High Speed Integrated Circuit Hardware Description. Our supporting synthesizing and simulating tools are Xilinx ISE9.2i and model sim-altra6.3g-pi (Quartus II) respectively. At last, we will compare 4-bit ALU with 4-bit Array ALU.*

Keywords: *urdhva triyakbhyam multiplication Algorithm, Vedic arithmetic and logic unit, Vedic mathematics, VHDL.*

I. Introduction

Already, we have studied that ALU is a mathematical unit and executes arithmetic & logical operations. Hence, ALU is the heart of µprocessor, µcontroller and DSP. Here, not only executes arithmetic functions but also carryout logical functions. It can execute three arithmetic and five logical functions. In recent days, high speed processors are becoming more and more. ALU speed is the main important feature of digital domain based system. The ALU is used to perform partially or whole in all the technologies and the ALU speed mostly depend upon multiplier speed. Therefore, we go for developing a 4-bit Vedic multiplier having more speeds. This multiplier is very fast and less hardware components are required and shown in fig 1.

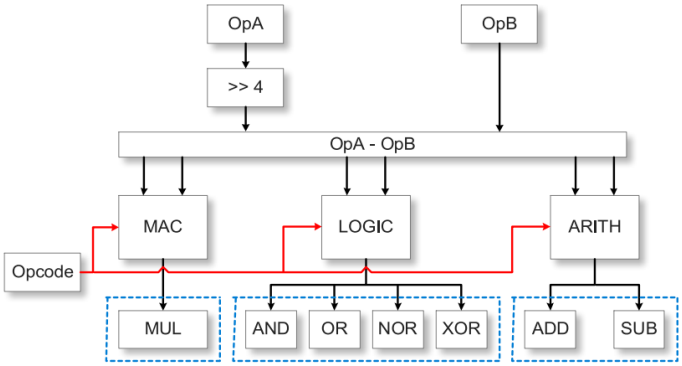

Fig 1: Basic Blocks in ALU Architecture

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II. Related Work

The ancient Vedic mathematic is a gift given to Indian sages. Hinder cleric wrote Vedic mathematics. It contains mental calculation techniques related to Vedas. This is described in Vedic work. The Vedic mathematics uses a large number of calculations are done within a short time. The Vedic mathematics is based on the normal human mind working principle. The Vedic mathematic perform high speed calculations used in the engineering field for performing effective algorithm. Multiplier dependent 4-bit Vedic ALU is discussed here. We are going to employ an algorithm called as urdhva tiryakbhyam procedure. It is employed in decimal system to product two numbers. Here, proposed method develops the same in binary system. Hence, it is generalized for all multiplication purposes which is adopted for digital hardware units. Multiplier adopts the sutra called as partial protect where the sums are evaluated in parallel. Advantages of the above discussed method are increment in bits, area and decrement in speed.

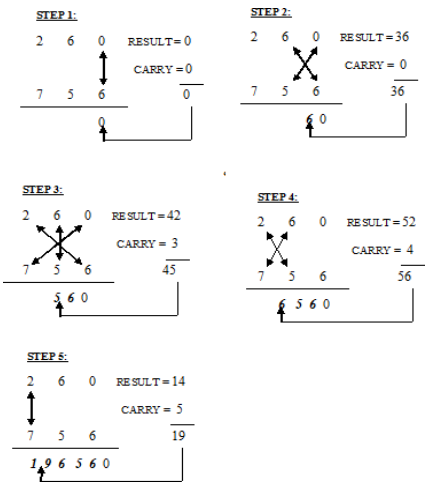

Fig 2: schematic representation of multiplication of two decimal numbers

We will now adopt this algorithm for binary number system. The binary multiplication technique multiplies two bits which is just an AND operation. Let us consider, two 4-bit binary numbers such as A=1011 and B=1101.It produces 8-bit binary number by using vertically and crosswise method. The example of 4-bit binary multiplication technique in urdhva thriyakbhyam method is given below in figure 3.

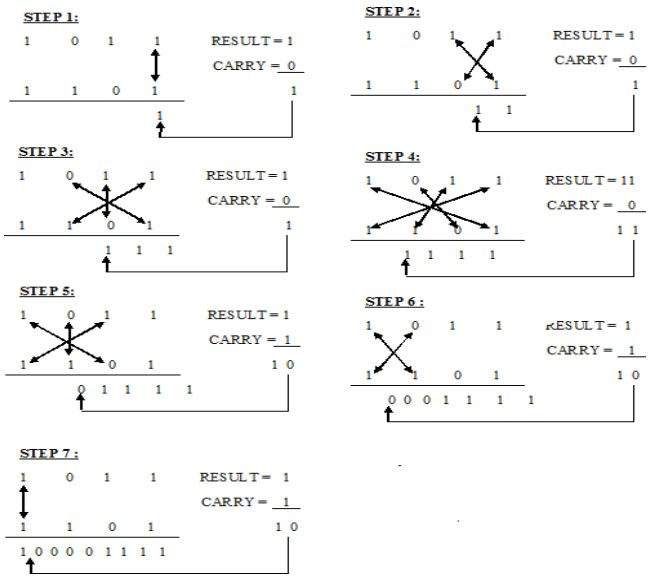

Fig 3: Schematic representation of multiplication of two 4-bit binary numbers

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III. Proposed Data path Designs

Here, we discuss in detail about two 2x2 bit, 4x4 bit are observed. We also employ urdhva tiryakbhyam in multiplying two numbers. The benefit of this method is the result of partial products and done addition in parallel. In this section explained multiplied two 2- bit numbers in urdhva tiryakbhyam method. This is already explain above section and now let us consider two 2-bit number X=x1x2 and Y=y1y2.The implementation equation of 2x2 Vedic multiplier are

$$S0 = x0y0 = A \quad (1)$$
$$C1\ S1 = x0y1+y0x1 = B \quad (2)$$
$$C2\ S2 = C1+x1y1 = C \quad (3)$$

The final result is DCBA. The D is specified by carry bit. Here the implemented 2-half adder modules as given below in figure 4. The two half adders used here generate their own path delays and shown in fig 4..

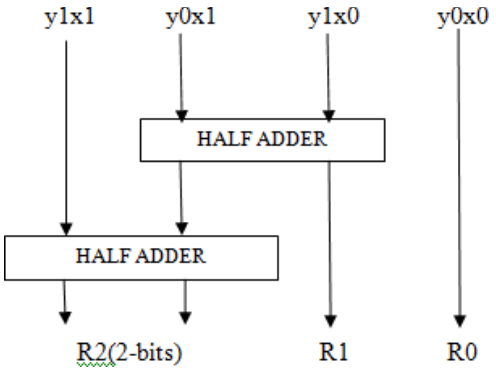

Fig 4: Schematic representation of 2X2 multiplier module

A 4-bit Vedic multiplier is designed by employing AND gate, adder in this paper. It contains full adders eight in number, half adder three in number, AND gates sixteen in number. The main purpose is to decrement speed. Below figure shows the architecture. We take into consideration 4x4 multiplication X=x3x2x1x0 and Y=y3y2y1y0. An eight bit plus carry bit is the output generated. The result is given by P=p7p6p5p4p3p2p1p0 and is shown in fig 5.

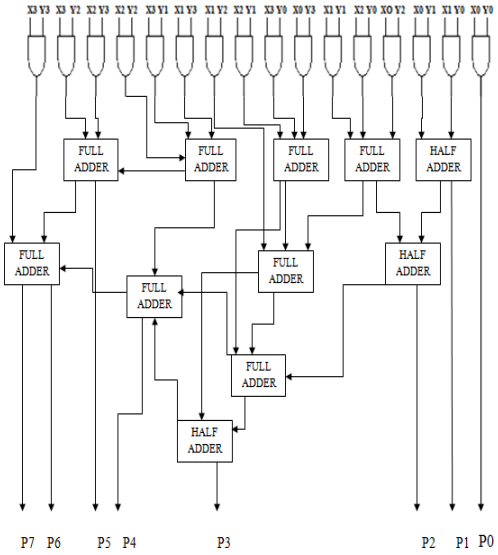

Fig 5: block diagram of 4x4 multiplier module

Figure 6 shows a Vedic 4-bit architecture which is proposed here. Dependent on selection lines inputs A and B executes ALU functions. We here employ 8:1 and two 2:1 multiplexer. Input B, 2's complement are received by 2:1 multiplexer. If all the selection lines are zero, A is added with B directly, or else, A and input of 2's complement together added to produce output subtraction. All the arithmetic functions at the output are received by 8:1, employing selection lines logical functions are produced at the output. Logical functions output may be excess 4-bit that is of two state. Logical operations attained will observed in output of LSB. Arithmetic functions output may be also excess 4-bit and is observed in MSB.

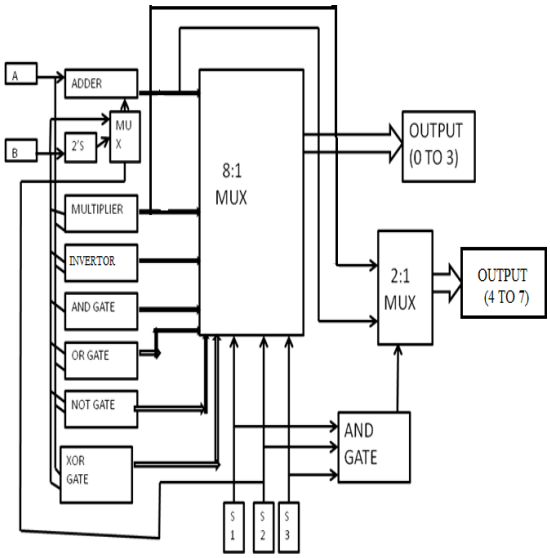

Fig 6: Schematic representation of the 4-bit vedic ALU architecture

IV. Simulation Results

In this paper, 4x4 bit Vedic multiplier and ALU are coded by employing VHDL. Xilinx ISE12.1i project navigator to simulate VHDL code. The four bits given below are tested by employing 4-bit multiplier simulator. Inputs of 4-bit multiplier are A=1111 , B=1111 and benefited output is C=11100001 and is shown in figure 7 and figure 8 respectively.

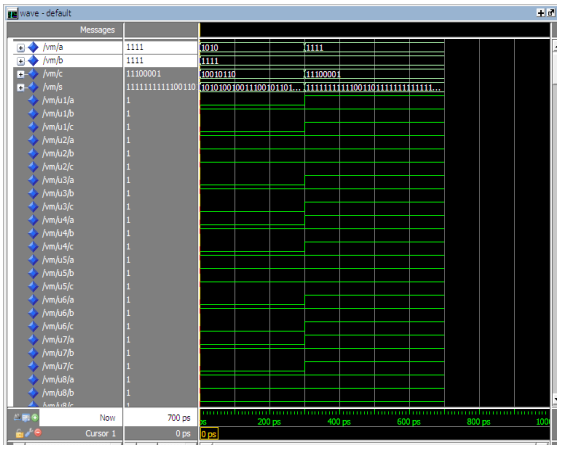

Fig 7: Simulation of 4-bit vedic multiplier

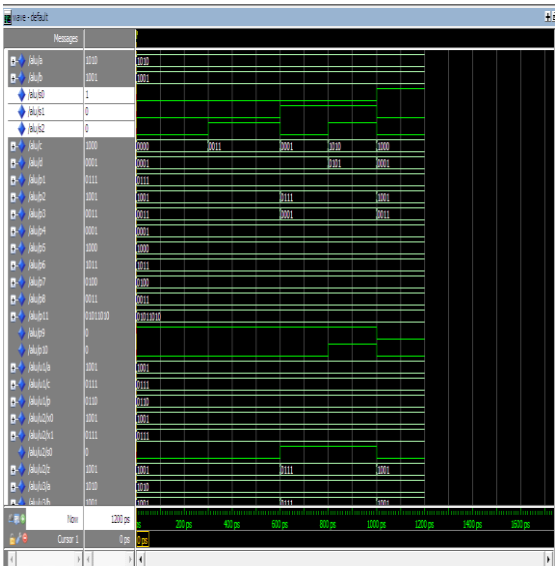

Fig 8: Simulation of 4-bit ALU

The inputs of selection lines are considered to be zero. After that addition function is chosen. Considered inputs are A=0011, B=1001 and the output generated is C=0011 , D=0001.The inputs of selection lines are considered to be zero except S3=1. After that subtraction function is chosen. Considered inputs are A=1010, B=1001 and the output generated is C=0001, D=0001. From the table below , we verify that the Vedic multiplier has the better speed in comparison with multipliers. We have also designed all of this multiplier. Then this delay time is compared to our Vedic multiplier, which produces better time delays. The results are tabulated in table 1.

TABLE 1: Comparison of Delay in Multiplier

Multipliers	**Number of bit slices**	**Number of IOs**	**Number of LUTs**	**Delay (ns)**
Array Multiplier	40	20	45	20.11
Vedic Multiplier	18	16	31	17.47

Below table 2 shows the differentiate between 4-bit Vedic ALU and array ALU in terms of their speeds. Simulation results show that array ALU less path delay in comparison with Vedic ALU. This 4-bit array ALU and it delay time will compared.

TABLE 2: Comparison of Delay in Multiplier

Multipliers	**Number of bit slices**	**Number of IOs**	**Number of LUTs**	**Delay (ns)**
Array Multiplier	29	19	51	17.58
Vedic Multiplier	49	23	65	20.22

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V. Conclusion

Multiplier design discussed above is an effective one dependent on urdhva tiryakbhyam sutra. In simulation process, this technique decreases the path delay. So, it has the capability of simulating the calculations with higher speeds in comparison with various methods adopted. A 4x4 multiplier produces a speed of 15.27ns in this paper. Speed of 4-bit ALU is 17.583 that far less in comparison with Array ALU path delay. So, it is much better than array ALU. Simulation results show 23% improvement in delay parameter and can be implemented in higher architectures.

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