Leakage Power Minimization Using Gating Technique In FPGA Controlled Device

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Article History

Article Submission
27 September 2013
Revised Submission
27 October 2013
Article Accepted
25 November 2013
Article Published
31 December 2013

Abstract

FPGA based controlled devices are widely used in integrated chip sector provided the power consumed by such devices should be low. Leakage power takes vital part in contributing towards the total power consumption. This research work concentrates in proposing a power gating technique based on look up table approach. The novelty of this approach is that common look up tables are employed for asynchronous architectures for each leaf node. Due to this the leakage power and the total area overhead can be minimized. The proposed architecture is simulated through M-Power analysis and simulator tool for leaf nodes and efficiently utilizes H-tree methodology to minimize area. The reduction in number of look up tables leads to 45% to 50% reduction in leakage power of FPGA device.
Keywords: *Leakage power, Fine grain gating, Look up table, Leaf node gating*

I. Introduction

The VLSI and ULSI technologies are widely used for many applications like computer, digital camera, cell-phones and etc. VLSI applications find eminence in the certain areas of research and development. These areas are system specification, design and partitioning, wafer level integration and neural frame architectures [1][2]. Due to this wide application of VLSI components, power consumption of these devices is an important criterion to be considered. Power consumption is broadly classified as static and dynamic power consumption due to the charging and discharging process occurring in the load capacitances. Leakage current is contributed by threshold and junction current which forms the major percentage of leakage current. This leakage current widely increases with increase in the scaling dimension of the transistors [3].

Historically, most CMOS designs are executed with V_{dd} much more than V_{th}. If V_{dd}=5V, then the threshold voltage must be greater than 700mV [4]. The leakage power also comprises of active leakage current and stand-by leakage current. The leakage power optimization shall also be concentrated on active and sleep mode leakage power. During standby mode, the unwanted power consumption did by circuit blocks that are inactive on temporary basis is to be eradicated by sleep states [5].

The sleep transistor strategy is commonly used Application Specific Integrated Circuits (ASIC) domain. The dynamic threshold voltage adjustment is also preferred to reduce leakage power [6]. Multi-threshold approaches also find its importance in reduction of leakage power in FPGA. Another dedicated approach is the use of stacked transistors in series instead of individual transistors may also reduce leakage power. Such sleep transistor is shown in figure 1.

ISSN: 2250-0839

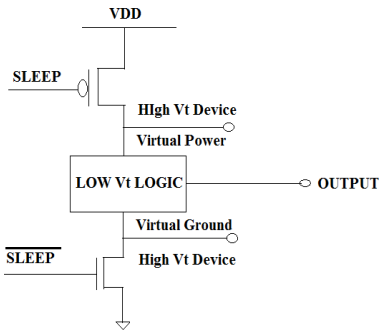

Fig.1: Sleep transistor circuit

The sleep transistor reduces the sub-threshold leakage current in peripheral circuits through sleep mode. Various sleep modes are in practice in case of non-volatile FPGA's. The sleep transistor is actually connected between actual ground and circuital ground [7].

II. Existing Methods

Two existing approaches such as zig zag power gating and individual LUT based logic blocks are discussed in this section.

A. Zig-Zag Power Gating

CMOS circuits like inverter and logic gates needs straight forward implementation of zig zag power gating. Implementation of such power gating circuits in transmission gate interfaces leads to sneak oriented leakage and area overhead problems [8]. The zig zag power gating method is shown in figure 2.

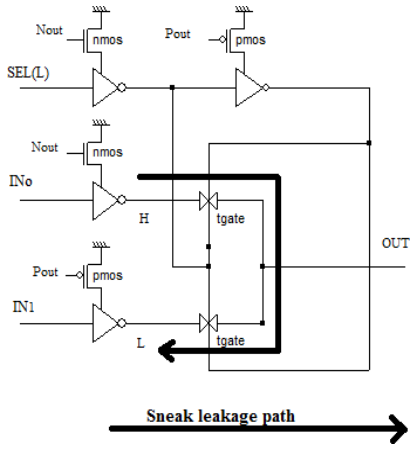

Fig.2: Sneak leakage problem path

B. Individual LUT Based Logic Blocks

According to this method for every logic blocks a look up table is set. The logic block for the given expression is activated only by decision made by the look up table is set. If thousand logic blocks is present means thousand LUT table is needed [9]. It consumes particular amount of power and circuit complexity and area overhead also increased. To reduce the large number of LUT, fine grain based logic blocks introduces common LUT for k number of logic blocks. In this method number of LUT is reduced. So power and circuit complexity also minimized. In our method 65nm CMOS processor is utilized [10].

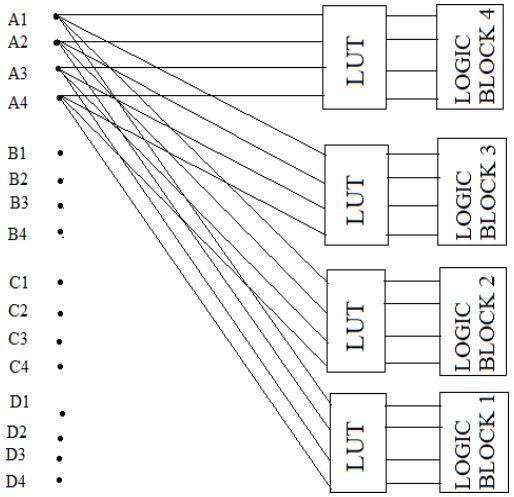

Fig.3: Block Diagram of Individual LUT base logic blocks

III. Proposed Method

Our proposed method implements a novel LUT based fine grain power gating which will reduce the number of LUT by using a single LUT as common. A single LUT has to manage more number of logic blocks. The number of logic blocks per LUT will depend upon the number of I/P combination. An FPGA k-LUT is comprised of k- input signals which select single output from single input bit. For example 3 I/P signal and 1 enable signal means we can connect 16 logic blocks for that LUT. The proposed block is shown in fig.4.

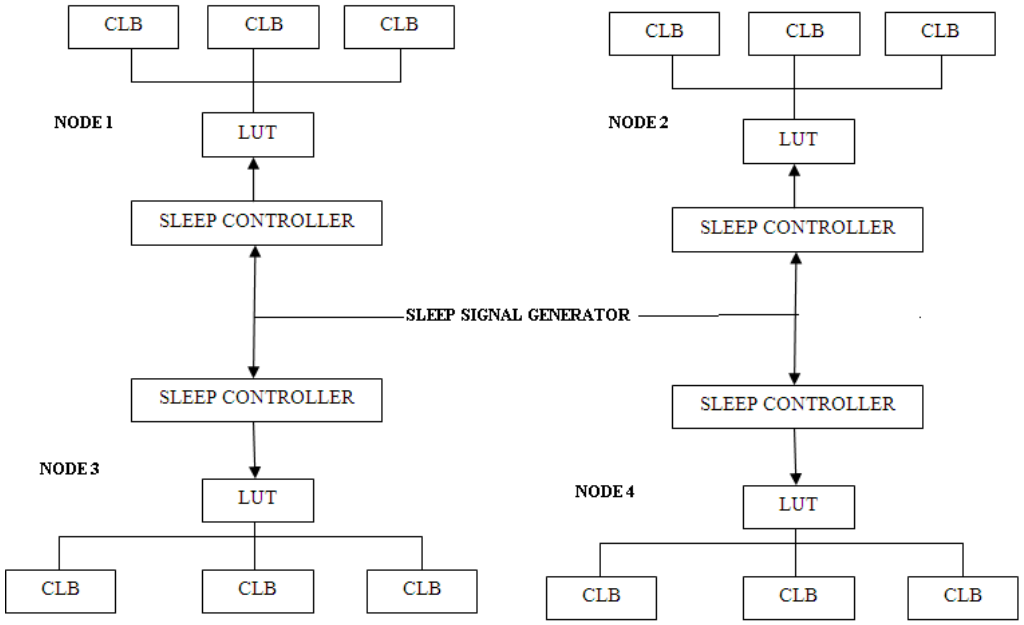

Fig.4: Block diagram for proposed method

To activate the logic blocks a sleep signal acts as an enable signal. The sleep signal is distributed through H tree. Control signal is distributed to each leaf nodes which should activate the logic blocks. The structure of H-tree is shown in figure 5.

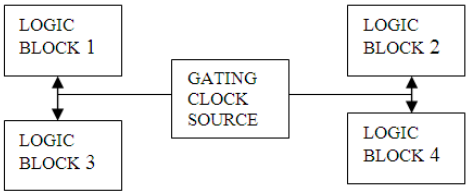

Fig.5: Block Diagram of H Tree

The sleep transistor is used to reduce the leakage power in FPGA circuits. It is an effective way to reduce the leakage of a transistor. It is identified that the sleep transistor itself consume a large leakage power and it is avoided by utilizing a single sleep controller for each leaf node logic blocks. Sleep control signal is selected and distributed through LUT. Look Up Tables (LUT) are the used in FPGAs to select the action of logic blocks. The function of LUT for three inputs is shown in table.1

Table.1.Truth table for 3 input LUT

A	B	C	X = AB + BC
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

IV. Simulation Results, Comparison and Optimization

A four node logic block circuit leakage of power was analyzed references and obtains the power consumption for a 5V input using microwind for conventional LUT and LUT based circuits. The table.2 shows the power consumption for their corresponding vdd's for conventional power gating. Similarly table.3 shows the power consumption for fine grain based logic blocks. The figure.6 represents power consumption variations for both the techniques. By simulating our proposed system the power consumption is reduced by 32% to conventional power gating system. Power dissipation for individual LUT/ conventional LUT/ LUT base fine grain method comparison of different methods is shown in figure 6.

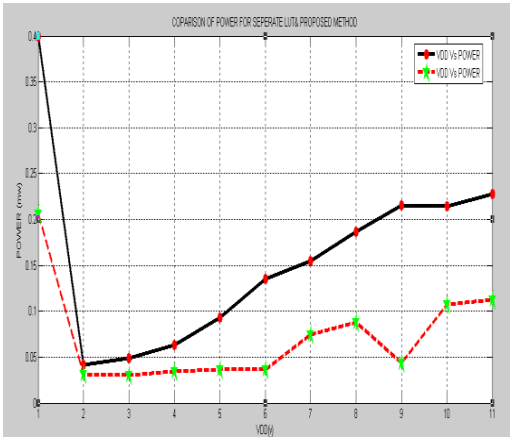

Fig.6: Power dissipation for individual LUT/ conventional LUT/ LUT base fine grain method comparison of different methods.

The figure.6 represents power consumption variations for both the techniques. By simulating our proposed system the power consumption is reduced by 53.9% to separate LUT system. The power comparison of the LUT and conventional power gating are tabulated and the comparison is shown in the graph. In the graph Blue color line indicates the power consumption of non-LUT based logic blocks and red line indicates individual LUT based logic blocks and black line indicates fine grain LUT based logic blocks. The simulation is carried out for 65µm CMOS processor and the results are compared with previous methods. The whole simulation is carried out in M Power simulation and results are shown in table 2. The Idd for their corresponding vdd's for conventional power gating. Similarly table.6 shows the power consumption for fine grain based logic blocks. The figure.10 represents power consumption variations for both the techniques. By simulating our proposed system the power consumption is reduced by 33% to separate LUT system and is shown in figure 7

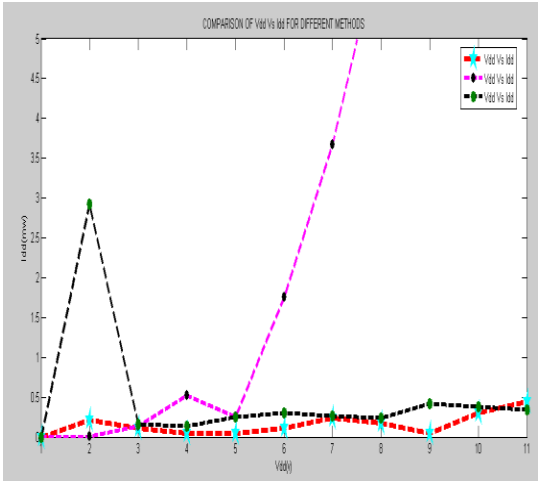

Fig.7: Idd comparison of individual LUT

Table.2. power dissipation of different methods

METHODS	POWER CONSUMPTION OF NODES		
	2 NODE	3 NODE	4 NODE
Leaf Nodes For Conventional Power Gating	17.31mW	24.4mW	34.62mW
Leaf Nodes For Individual LUT Based Logic Blocks	0.16mW	0.27mW	0.39mW
Leaf Nodes For Fine Grain Based Logic Blocks	0.076mW	0.122mW	0.167mW

The Idd comparison of the LUT and conventional power gating are tabulated and the comparison is shown in the graph. In the graph pink color line indicates the Idd consumption of conventional power gating based logic blocks and black line indicates individual LUT based logic blocks and red line indicates fine grain LUT based logic blocks.

V. Conclusion

This research article examined the relations that exist between configurable logic blocks and LUT reconfiguration of FPGA. The number of LUT reduction in each node leads to reduction in leakage power to considerable amount. This paper also made analysis in area reduction for logical blocks by the usage of minimum controller. In addition to fine grained gating network Idd current also reduced to considerable amount in logic blocks. Our proposed method simulation shows that the total leakage power is reduced to about 40%-50% with little area overhead.

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