Vedic Multiplier Implementation for High Speed Factorial Computation

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Abstract

Vedic Mathematics arise from the prehistoric classification of Indian mathematics that was recreated by Tirthaji. Ancient mathematical operations are depending on sixteen methods. In this article, a new VLSI architecture to compute factorial of the given number with Vedic based multiplier is proposed. Simulations are performed using Xilinx ISE 14.2. Effective comparative analysis is made with existing multipliers to prove the momentous development in competence and high speed operation. This efficient multiplier is implemented in the proposed factorial architecture which significantly reduces the path delay and provides better optimization.
Keywords: *VLSI Architecture, Multiplication, Vedic Mathematics, Factorial Calculations.*

I. Introduction

Multipliers acts as heart of Microprocessors, Digital Signal Processors and high end communication oriented processors with sophisticated operational units. Adders plays a vital role in construction of high speed multipliers which are used to compute partial products. The necessity of high speed multipliers is directly proportional to the demand of real time processors for modern day operations. Dealing with reduced delay and power parameters are essential for domestic and industrial applications. Machine based multiplication is combination of addition and shifting operations [1].
Urdhava Tiryakbhyam Sutra is a method through which partial products are calculated in parallel which reduces the computation time there by enhancing its efficiency [4]. Conventional factorial results are compared with our proposed factorial architecture which has the efficient multiplier as one of its module which provides optimization in terms of speed and efficiency. When dealing with combinations and permutations (when dealing with probabilities), the importance of factorial is more [5].

II. Vedic Multiplication

U. Tiryakbhyam Sutra from vedic mathematics is used to perform multiplication in a faster way which means 'vertical as well as crosswise'. The steps concerned in the Urdhava Tiryakbhyam Sutra are as follows:

STEP1: It has n-bit Vedic multiplication unit.
STEP2: It has Partial products and carry.
STEP3: It has adders and the results of multiplication.

Consider a pair of two bit numbers such as a0a1 and b0b1. Multiplication process is as follows. The process of multiplication is shown in figure 1 and steps is shown in figure 2.
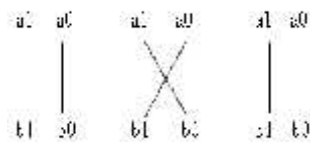
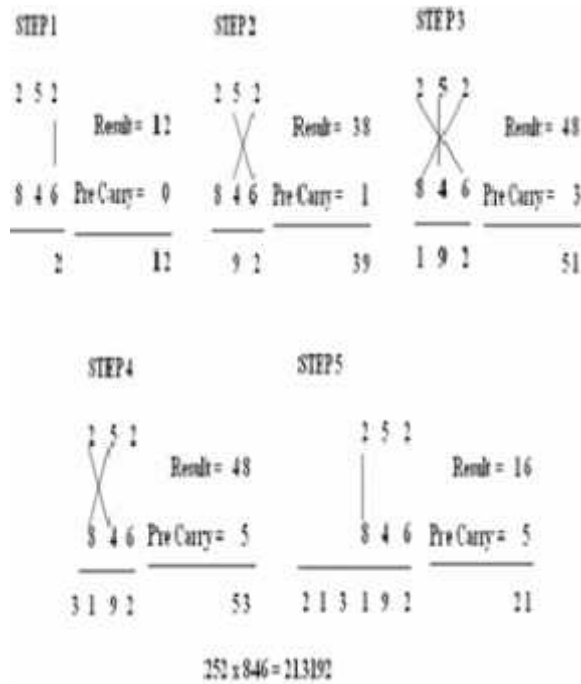*Fig.1   Multiplication of 252x846 (decimal)*

Fig.2 Steps in Multiplication of 252x846 (decimals)

III. Proposed Model of UT Multiplier to Calculate Factorial

The architecture [2]-[3] shown in fig.1 is similar to conventional multiplier. Let's consider 2 bit numbers such as A = a1a0 and next B = b1b0. The 2X2 VM module is premeditated using 4 AND gates and two half-adders. Architecture is as follows:
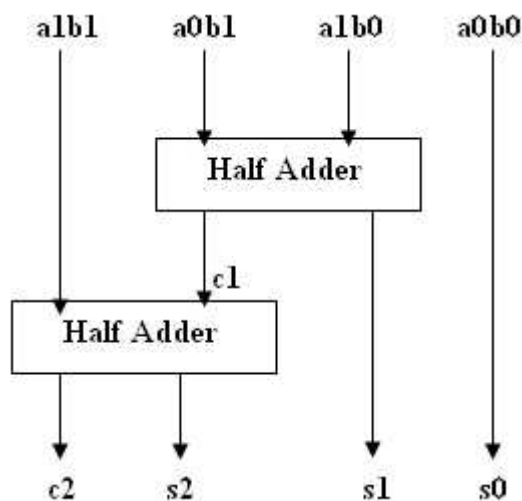

Fig.3. Architecture of 2x2 Vedic Multiplier

With the four 2x2 bit VM modules, 4X4 VM is deployed in fig. 4. Let's consider a pair of 4-bit as A and B, say A=a3a2a1a0 & B= b3b2 b1 b0. The resultant product is 8-bit– s7s6s5s4s3s2s1s0 .Architecture of 4X4 VM is shown in figure 4.
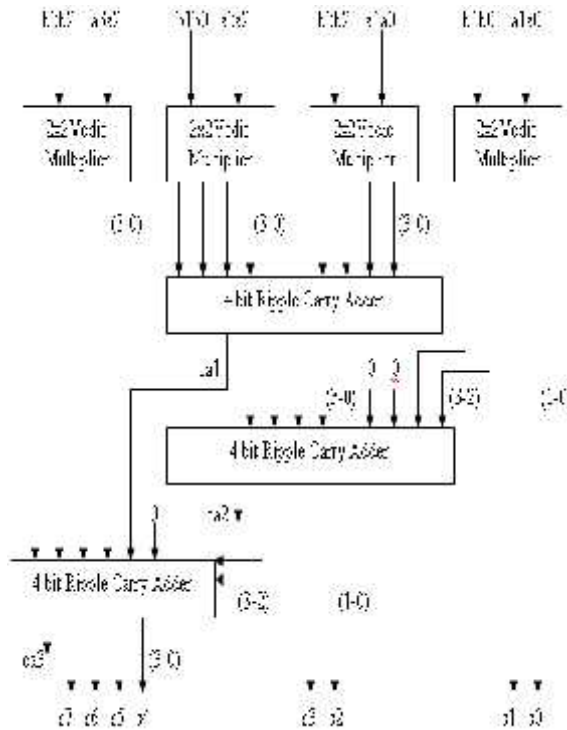

Fig.4. Block of 4x4 Vedic Multiplier

With the four 4x4 bit VM modules, 8X8 VM is deployed in fig. 5. Let's consider a pair of 8-bit as A and B. The resultant product is 16-bit–s15 to s0 .Architecture of 8X8 Vedic multiplier is exposed in figure 5.
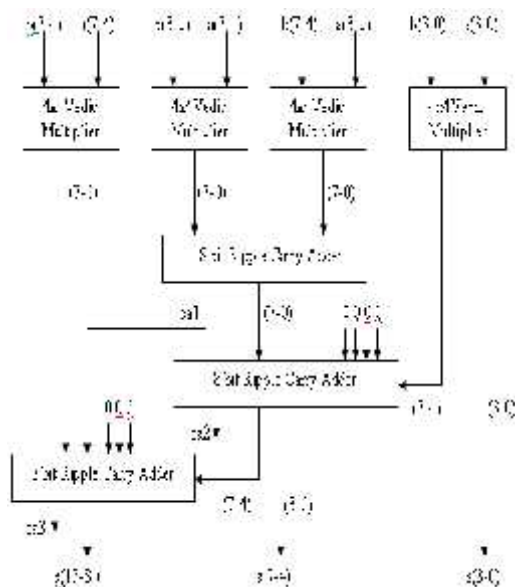

Fig.5. obstruct of 8x8 Vedic Multiplier

With the four 8x8 bit VM modules, 16X16 VM is deployed in fig. 6. Let's consider a pair of 16-bit as A & B. The resultant product is 32-bit–s31 to s0 .Architecture of 16X16 VM is shown in figure 6.
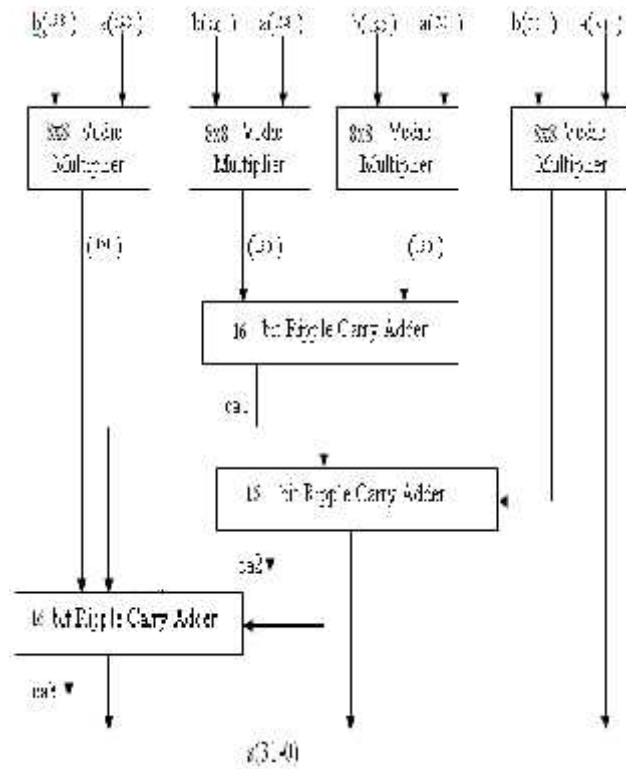

Fig.6. structural design of 16x16 Vedic multiplier

IV. Proposed Architecture of Factorial Computation

Factorial is the product of integers from 1 to n inclusive. The formula used to calculate the factorial is as follows:

Factorial of a number = (n)(n-1)(n-2)

Example: 4! Can be computed as follows:

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4!      = (4)x(4-1)x(4-2)x(4-3)
        = 4x3x2x1
4!      = 24
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We have used the efficient multiplier as one of the module to calculate the factorial of a number. The VM 16 bit multiplier is used to compute the factorial value. The architecture is explained as follows: First the number whose factorial to be computed is given as input 'n'. The value of 'n' is stored in a memory. Up counter performs counting operation until its value reaches n. The output of up counter and temporary variable is repeatedly multiply up to n times. The architecture is shown in figure 7.
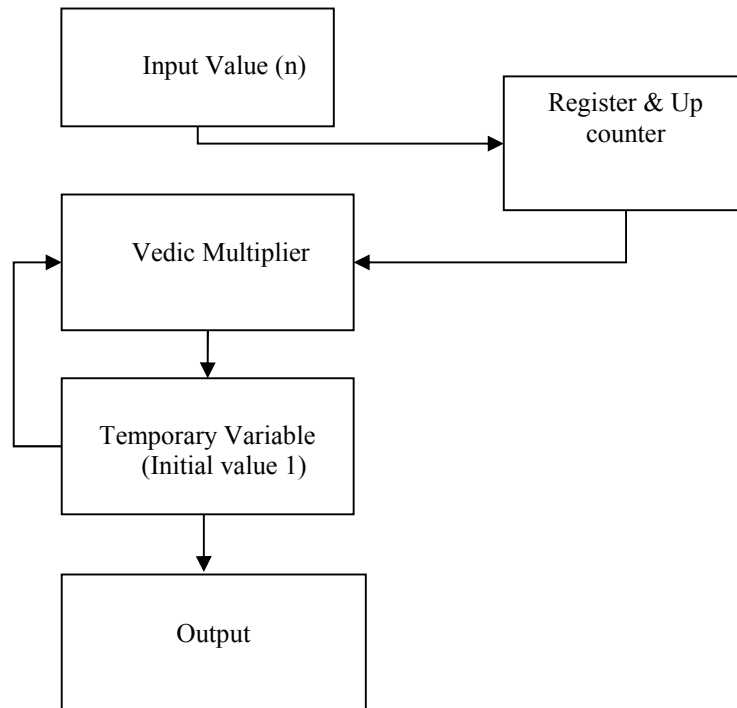
Fig.7. Block Diagram of Vedic Multiplier based Factorial Calculation

Simulations of the proposed design were conducted in the Xilinx ISE 14.2 design environment. The fig 8 & 9 demonstrate the simulation results of 8 bit and 16 bit Vedic multiplier. Figure 10 shows the experimental results of factorial calculation using Vedic Multiplier.
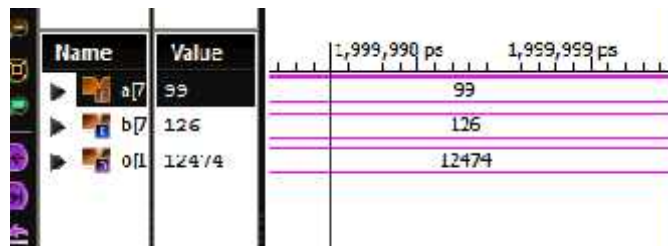

Fig. 8. Results-8x8 Vedic multiplier
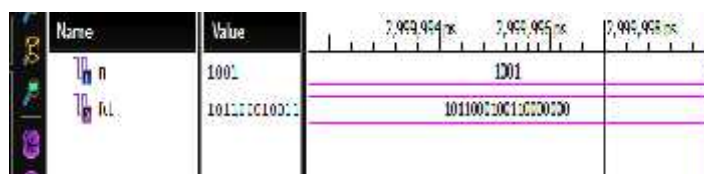

Fig.9. results-16x16 Vedic multiplier

Fig. 10. Results-Factorial Calculation

Table 1 depicts the comparative analysis of Vedic multiplier with conventional array multiplier for 8 and 16 bit, the synthesized results shows that VM outperforms in terms of delay compared to conventional multiplier.

Table I: Performance Analysis between Conventional and Vedic Multiplier

Multipliers	Number of LUT's	Delay (ns)
Conventional Multiplier 8x8	114	30.059
Conventional Multiplier 16x16	506	59.156
8x8 Vedic Multiplier	115	28.629
16X16 Vedic Multiplier	510	55.037

V. Conclusion

The 2X2 VM module is designed using 4 number logic AND gates and 2 circuit based half adders. With the four number of 2x2 bit Vedic multiplier modules, 4X4 VM is deployed. With the four 8x8 bit Vedic multiplier modules, 16X16 VM is deployed. We have used the efficient multiplier as one of the module to calculate the factorial of a number. The VM 16 bit multiplier is used to compute the factorial value. The synthesized results shows that VM outperforms in delay compared to conventional multiplier. Using Vedic multiplication to calculate factorial is the better way to obtain optimized path delay and efficiency.

References

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