Analysis of Analog to Digital Converter for Biomedical Applications

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Abstract

This paper presents an ADC which can be used for biomedical application like pacemaker. For the low-power operation, monotonic switching scheme and operating voltage reduction have been implemented in the design. The 10bit 1.8V rail-to-rail (SAR) ADC is realized using UMC 0.18µm CMOS process. Simulations are performed by spectre simulation. From static performance, offset error and full scale error are noticed. This performance issue can be corrected by reducing discharge in capacitor by implementing sampling switch as bootstrapped switch and proper selection of common-mode voltage where 20fF is used as unit capacitance.
Keywords- *ADC, Low power,SAR*

I. Introduction

Analog-to-digital converters (ADCs) are used in all electronic systems to convert analog signals to digital signal data. [3, 4]. In SAR ADCs, the principal sources of power dissipation and consumption are comparator, controllable logic circuit and reference capacitive DAC circuit. Except preamplifier, no component will consume static power. As mentioned before, all the components except preamplifier can be subjected to technology scaling which leads to considerable power reduction. On the other hand, scaling on sizing of capacitor and comparator is restricted by noise and mismatch. Recent days, several switching methods and architectures of DAC are proposed.

The capacitor split method [7] eliminates switching energy by 37 percent and the novel capacitive DAC switching scheme [8] reduces 60% switching energy and 68% area of conventional SAR ADC. Different switching scheme reduces switching power, but in other hand, it increases the complexity of control logic circuit. This paper combines the different energy-efficient techniques and implements the 10 bit 1.8V rail-to-rail SAR ADC. The implemented ADC contains the following techniques to trim down the power utilization: (i) monotonic switching scheme which reduces 81% switching energy and 50% area while comparing to conventional one. (ii) Two stage dynamic voltage comparator which is reliable for supply voltage reduction. (iii) 20fF unit capacitance and reliable switches. The performance is analyzed by spectre simulation and discussed how to improve the performance by several techniques.

II. ADC Architecture and Design Concept

To achieve 10bit accuracy, fully differential configuration of SAR ADC is used. Figure 1 represents the 10 bit fully differential SAR ADC. The fundamental building blocks comprises of sample-and-hold (S/H) circuit, the comparator, DAC and controllable logic circuit. For improving energy efficiency, different switching scheme are proposed, among that, monotonic switching scheme can be used because of adaptability on fully differential configuration and massive reduction in power consumption as well as area in higher resolution ADC design.

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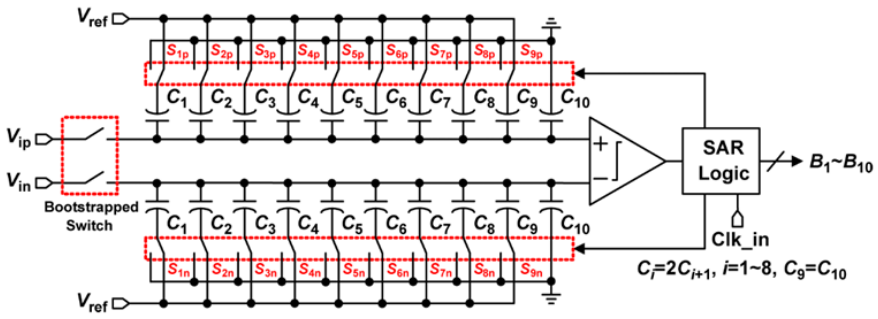

Fig 1. 10-bit SAR ADC

Figure 2 shows the SAR ADC which implemented by monotonic switching scheme. The monotonic switching can be upward and downward depending upon reference settling whereas downward switching is preferred for most ADC design. It samples the input signal by sampling switches and boot-strapped switch can be used as sampling switches for increasing bandwidth and settling speed.

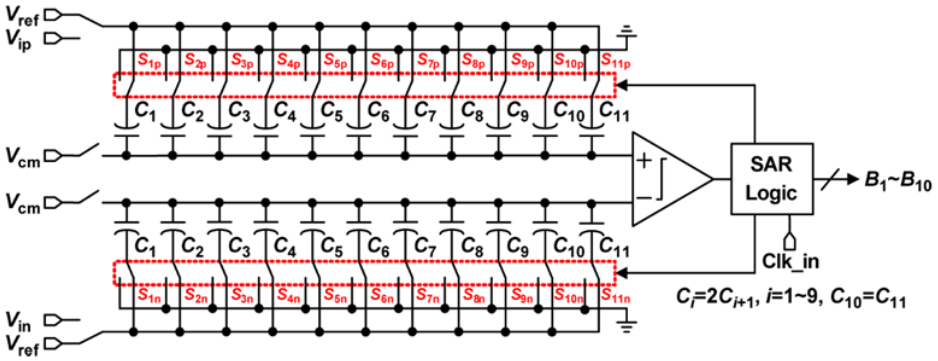

Fig 2. Switching Architecture 10-bit SAR ADC

During sampling phase, foot plate of all capacitors is reorganized to V_{ref} because of downward switching. Next, after switching off the upper plate switch, the comparator directly performs the first comparative analysis for MSB and no need for any switching. If comparator output is 1, the largest capacitor C_1 side remains same. Figure 3 shows flow diagram for switching scheme i.e., successive approximation procedure.

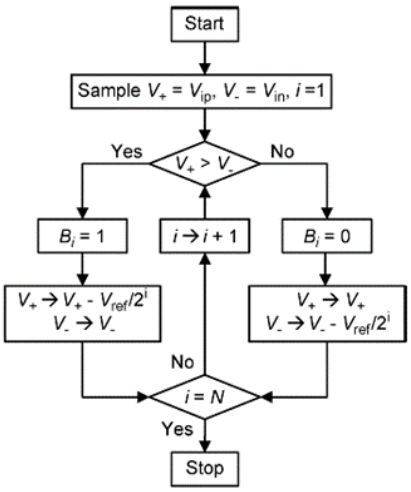

Figure 3. Flow diagram of the Monotonic Switching ADC

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One of the major differences between conventional and monotonic switching scheme is common-mode voltage of gradually decreasing from half Vref to ground as given in Figure 4. Downward changeover increases settling time. In addition to that, first comparison is done without any switching because of sampling on top plate of capacitor. It reduces the total capacitance size to half, while comparing with conventional architecture.

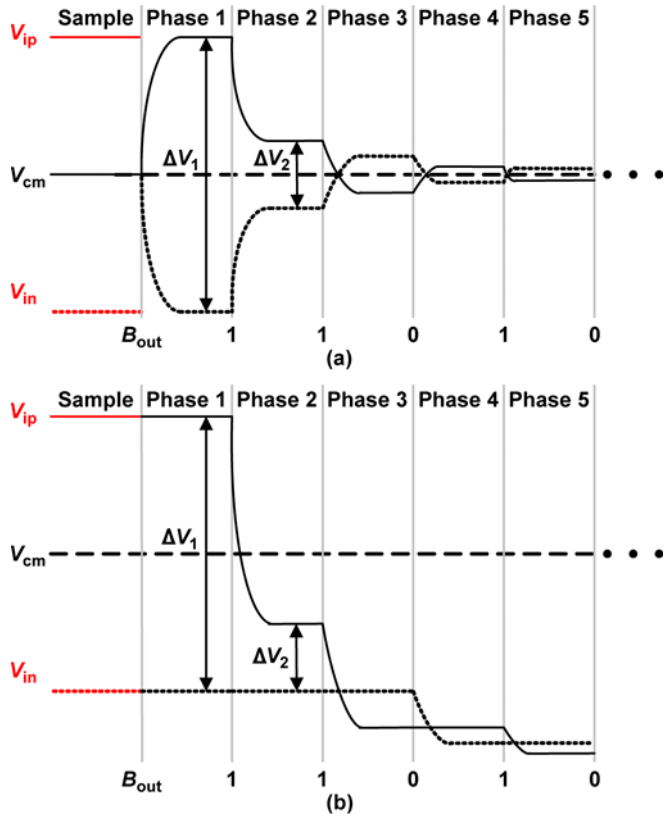

Figure 4. Waveform of conventional and monotonic switching procedure

III. Proposed Methodology

The fundamental building blocks of the ADC comprises of a dynamic comparator, SAR controllable logic and series capacitor network. The design details of the proposed building blocks are described below in the subsection.

a. Dynamic Comparator

Figure 5 shows the dynamic comparator with preamplifier and regenerative latch [8]. The parasitic capacitance present at V_a and V_b are discharged to zero at different rate ratio based upon the input voltage at transistors M1 and M2 transistors. By inverters, the rate of changing at node V_c and V_d is increased and isolated by transition phase on inverter characteristics. When V_c and V_d is increased more than the threshold voltage of n-type transistors, transistors M25 and M26 is turned on. Due to the strong regenerative force on inverter, 1 output node pulls high whereas another node pulls low.

Generally in fully differential configuration, impedance should be balanced and kick-back noise is cancelled out between each terminal. But different switching in input terminals in this architecture create kick-back noise at

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the inputs. The purpose of adding transistors is to preserve the same potential at the drain of differential-pair in both sample and regenerative phase. The input-referred offset is another performance metrics which leads to erroneous comparator output. This offset is signal dependent and also several possible approaches to improve this. One of the possible is to upsize the n-type M1 and M2 transistors, but it leads to large power consumption [5].

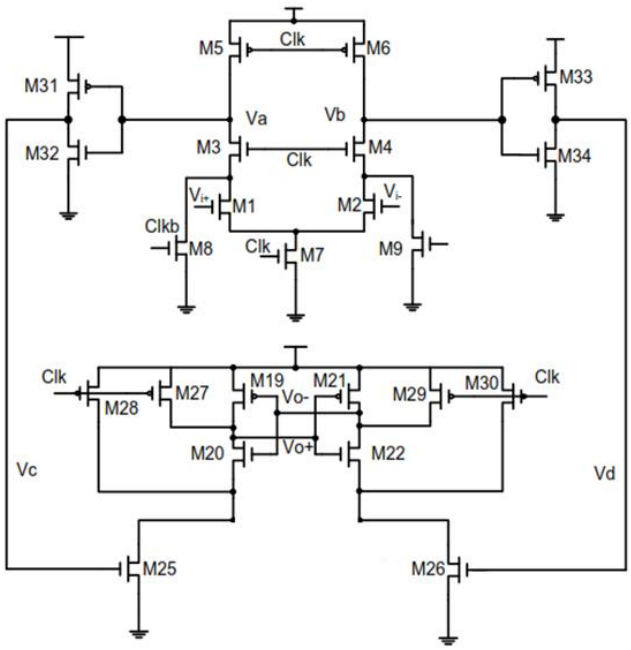

Figure 5. Schematic sketch of the dynamic comparator

b. Successive Approximation Register (SAR)

The SAR act as the control unit that takes the input from comparator and controls the switches in the DAC capacitor network. Figure 6 shows the SAR that encompasses a data register and a ring counter. If reset is activated in ring counter, all the data reset to zero as the initial step of each conversion. Ring counter activates each data register for every clock cycle and comparator output will be stored in the particular register which is activated. The cycle of activation in data register starts from MSB to LSB. For 10-bit SAR, in each end of 12 clock cycles, one sample is converted to digital. The major advantage of this SAR is the less power dissipation on high frequency and low supply voltage.

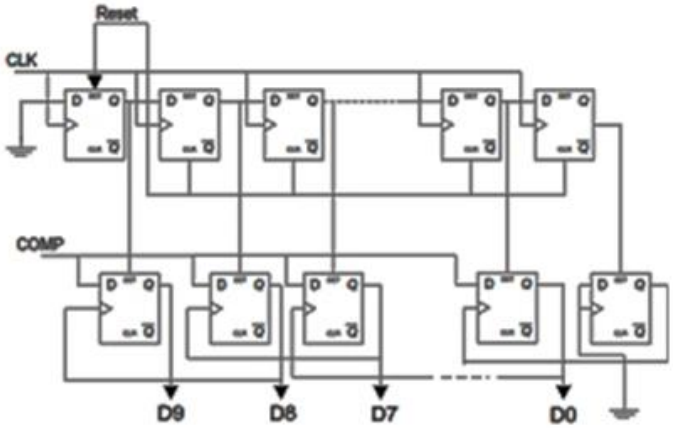

Figure 6. Schematic diagram of the SAR

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Data register is the one of the major component in SAR. By selection of low power design in register, total power consumption can be reduced. For low power design, C^2MOS logic and transmission gate logic can be used. While considering the insensitivity to clock slope, C^2MOS logic is preferred. Figure 7 shows the circuit diagram of set-reset data register which is implemented by master-slave configuration.

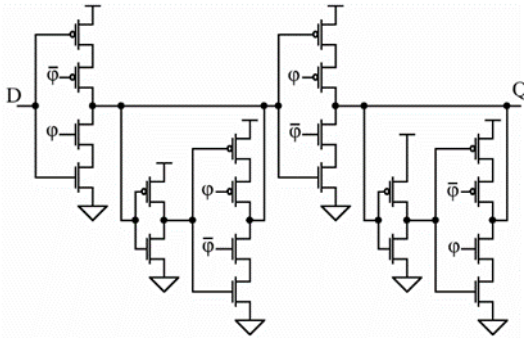

Fig 7. Schematic diagram of the C2MOS logic data register

c. Capacitive DAC network

The linearity and power consumption of ADC is directly related with DAC capacitor array formation and selection of unit capacitance. There are different types of capacitor array formation like binary capacitor array, split capacitor array, C&C capacitor array, etc. Binary weighted capacitor array formation is preferred for achieving good linearity and it consists of capacitors and switches. Other capacitor array formations are impaired by tolerance of capacitance and layout of capacitor array.

For saving power in ADC, unit capacitance should be taken very minimal value. But kT/C noise parameter, parasitic capacitor identical and the design policy are limiting the selection of minimum capacitances. By using of MIM capacitors and a careful layout routing, the top-plate parasitic capacitance is limited to 3% of unit capacitance. The result improves the linearity of ADC. The design uses 20fF MIM capacitors as unit capacitors and total capacitance is 20.48pF. For better layout of the capacitor array, a technique named common oriented centroid technique is used in design as shown in figure 8.

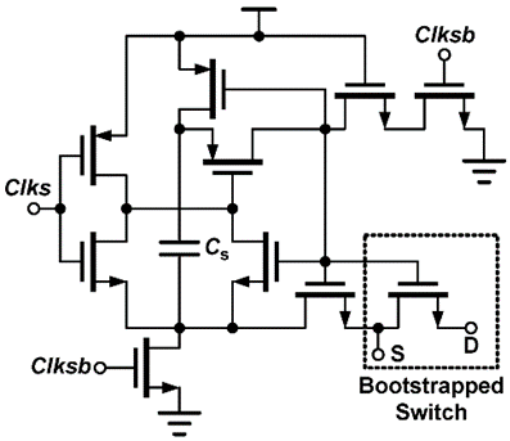

Fig 8. Schematic diagram of bootstrap switch

The bootstrapped switch is used for performing S/H function improving the switch linearity. When the bootstrap switch is turned off, dynamic offset is created due to coupling effect of drain-source capacitance at high frequency. It can be avoided by implementing cross-coupled capacitor (around 5fF). To further

neutralizing this effect, dummy switches and dummy routing can be used. Figure 8 shows the schematic diagram of bootstrap switch where Cs is sampling capacitor [4]. Bottom-plate capacitor switching is done by using dummy switches in design.

IV. Simulation Results & Discussions

The proposed ADC for biomedical application is implemented in UMC simulation tool with 0.18µm file mixed signal RF/CMOS process with MIM capacitors. The performance metrics are analyzed and corrections on issues are discussed with multiple solution. In static performance, offset error is neutralized by choosing common-mode voltage and results are shown in table 1.

Table 1. Offset Error Correction

Common Mode Voltage (V_{CM})	**Sizing of top plate switch**	**Digital output for 0V input**
0.8	720 – 600 nm	11010_01011
0.9	720 – 600 nm	10000_10000
0.9	480 – 400 nm	10000_00010
1.0	1000 – 900 nm	01101_00111
1.0	720 – 600 nm	10000_01111
1.0	480 – 400 nm	01110_00010

Full scale error is noticed on simulation. While analyzing from the figure 9, erronous output is noticed after ±0.5V. This error can be nullified by proper sampling switches and reduction on offset from comparator. Dynamic performance need to be analyzed and corrected for good signal-to-noise ratio (SNR).

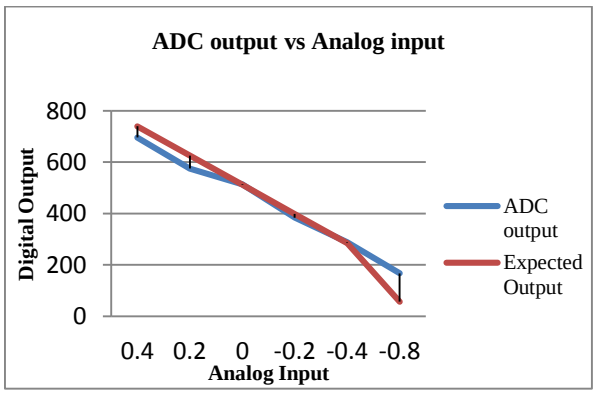

Fig 9. Analysis on Full-scale Error

V. Conclusion and Future Work

The ten bit fully differential SAR based ADC is designed to focus on reducing the power dissipation for biomedical application. The simulation is done using UMC 0.18µm with Cadence-Virtuso tool. From the simulation result, offset error of 2LSB for V_{REF} = 1.8V and full-scale offset error is observed. The dynamic range is limited to ±0.5V due to full-scale offset error. Limitation of input signal range can be overcome by implementing bootstrapped switches and reduction in offset at comparator. For improving input signal range and linearity of ADC, the following corrective action need to be taken based on analyzing following parameters:

- Selection of Common Mode voltage
- Discharge possibilities in bottom plate switch
- Input referred offset voltage on comparator
- Implementation of Bootstrapped Switch

The power consumption further be reduced by implementing operating supply voltage reduction, introducing adder in input signal to avoid input charging loss and unit capacitance reduction. Low power solution should be implemented in satisfying other limitation on performance metrics.

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