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Silicon Germanium BiCMOS Integrated Circuits for Scalable Cryogenic Sensing Applications

Mohsen Hosseini
University of Massachusetts Amherst

SILICON GERMANIUM BICMOS INTEGRATED CIRCUITS FOR SCALABLE CRYOGENIC SENSING APPLICATIONS

A Dissertation Presented

by

MOHSEN HOSSEINI

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Approved as to style and content by:

Joseph C. Bardin, Chair

Robert W. Jackson, Member

S. Raman, Member

Grant W. Wilson, Member

Christopher V. Hollot, Department Chair
Electrical and Computer Engineering

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ABSTRACT

SILICON GERMANIUM BICMOS INTEGRATED CIRCUITS FOR SCALABLE CRYOGENIC SENSING APPLICATIONS

FEBRUARY 2022

MOHSEN HOSSEINI

B.Sc., SHARIF UNIVERSITY OF TECHNOLOGY

M.Sc., SHARIF UNIVERSITY OF TECHNOLOGY

Ph.D., UNIVERSITY OF MASSACHUSETTS AMHERST

Directed by: Professor Joseph C. Bardin

This dissertation is focused on an investigation of BiCMOS cryogenic low noise amplifiers (LNAs based on Silicon-germanium (SiGe heterojunction bipolar transistors (HBTs for simultaneous low noise and low power design and also taking advantage of CMOS circuitry for adding flexibility to the LNA design. Cryogenic LNAs' scalability challenges are discussed and addressed in the dissertation. To achieve that, first, HBTs of three state-of-the-art technologies are characterized and modeled at cryogenic temperature. It is shown that SiGe HBT provides a promising compromise of noise temperature, power consumption, and bandwidth. Moreover, a scalable on-chip approach is proposed and verified for biasing of SiGe HBTs based LNAs. Finally, the first cryogenic re-configurable LNA is designed, implemented, and measured.

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CHAPTER 1

BACKGROUND MATERIAL AND MOTIVATION

Cryogenic low noise amplifiers are regularly used in a wide range of applications, including radio astronomy [62], quantum computing [11, 13], and fundamental physics research [41]. For many years, InP high-electron-mobility transistors (HEMT) were the only choice for the implementation of these amplifiers [19, 91]. In the last decade, it is shown that SiGe HBT is a promising choice for these applications [93, 14] particularly for low power purposes [63] and lower than 10 GHz frequency range. However, state-of-the-art readout systems in different applications require larger arrays, and consequently, higher scalability and better noise performance for cryogenic LNAs are desired. For example, currently, 54 qubits quantum processor is the state of the art [7], and scaling quantum computers to million qubits is required for practical quantum computers [12], and consequently, it demands implementation of a massive amount of microwave electronics blocks, including scalable, high-performance cryogenic LNAs.

Here in this chapter application of the cryogenic LNAs are described as a motivation for the dissertation. Particularly, it is focused on the applications of the LNAs which are designed in the next chapters of the dissertation.

1.1 Need for Highly Scalable Integrated Cryogenic LNAs

1.1.1 Terahertz Detection

The terahertz part of the spectrum (0.1–10 THz) is described as the final unexplored area of the spectrum. Even though human beings have relied on sun radiation (including terahertz band) since a long time ago, the development of terahertz

technologies started in the 1940s, and it was mostly about laboratory applications. Terahertz radiation is resistant to the well-known approaches used for infrared and microwave radiation detection, making it challenging. Despite the fact that the significant use of terahertz spectroscopy is for astronomers and chemists, detection of terahertz is an engineer's challenge [78].

Terahertz remote sensing is challenging because ambient moisture of Earth's atmosphere causes strong absorption at this frequency range. Moreover, unlike visible light and infrared detectors, terahertz detectors have not yet reached fundamental quantum limit characteristics. Therefore, there is still an opportunity for research in this field [84].

Signal to noise ratio of the detected signal is that of the signal current to the shot noise, namely [28]:

$$\mathrm{SNR} = \frac{i_{\mathrm{sig}}}{i_{\mathrm{n,shot}}} = \frac{\Phi_{\mathrm{p,sig}}\eta q}{\sqrt{2q\bar{i}\Delta f}} = \frac{\Phi_{\mathrm{p,sig}}\eta q}{\sqrt{2q(\Phi_{\mathrm{p,sig}}\eta q + \phi_{\mathrm{p,bkg}}\eta q)\Delta f}}, \tag{1.1}$$

In which,$\Phi_{\mathrm{p,sig}}$ and $\Phi_{\mathrm{p,bkg}}$ are desired signal and background noise flux and η is quantum efficiency (electrons per photon). Depends on the type of the telescope (ground-based or space-based) the dominant noise contribution can be the shot noise generated by the signal-power envelope or background noise. With a weak signal source detected against a large background which is the most common situation, the dominant shot noise contribution is the shot noise of the background ($\Phi_{\mathrm{bkg}} \gg \Phi_{\mathrm{sig}}$). The background-limited infrared photo-detector (BLIP) can be calculated from the below equation:

$$\mathrm{SNR}_{\mathrm{BLIP}} \simeq \frac{\Phi_{\mathrm{p,sig}}\eta}{\sqrt{2\Phi_{\mathrm{p,bkg}}\eta\Delta f}} = \Phi_{\mathrm{p,sig}}\sqrt{\frac{\eta\tau}{\Phi_{\mathrm{p,bkg}}}}, \tag{1.2}$$

It shows the $\mathrm{SNR}_{\mathrm{BLIP}}$ is inversely proportional to the square root of the background flux; so, reducing the background photon flux increases the SNR. The ultimate performance of the detectors is reached when the readout (including both detector and

LNA) input-referred noise temperature is low (more than a factor of 3–5) compared to the photon noise.

The performance of BLIP detectors can be improved by reducing the background photon flux ($\Phi_{\mathrm{p,bkg}}$). This can happen by two approaches. First, a cryogenic or reflective spectral filter for limiting the spectral band. Second, a cooled shield to limit the angular field of view of the detector. The first approach will eliminate background radiation from out-of-spectrum regions. In conclusion, the best detectors yield background-limited directives in a narrow field of view [56].

All radiation detection of terahertz can be divide into two main groups: 1. incoherent Detection and 2. Coherent Detection. Here I briefly describe these two approaches and the pros and cons of each.

1.1.1.1 Incoherent Detection

Incoherent detection is done by direct sensors, which allow just amplitude of the signal, and typically, it has wide instantaneous bandwidth. Incoherent detection provides more effortless scalability than a coherent approach but with lower spectral resolution, and it is also commonly used for ultraviolet, infrared, and visible directions. The schematic of a typical incoherent detection is shown in Fig. 1.1, in which W_S is the desire signal power and W_B is background radiation power. Usually, an optic filter is located before detectors to remove background radiation at frequencies other than the desired one. Most sensitive direct detectors are cooled to $T \approx$0.1–0.3 K reaching noise equivalent power (NEP) limited by cosmic background radiation fluctuation.

The threshold power detected by direct detectors is higher than heterodyne because of the LNA's added thermal noise, which is why the noise performance of LNA is critical for this type of detector. On the other hand, the main advantage of direct detection is simplicity and the possibility to design a large array, which requires

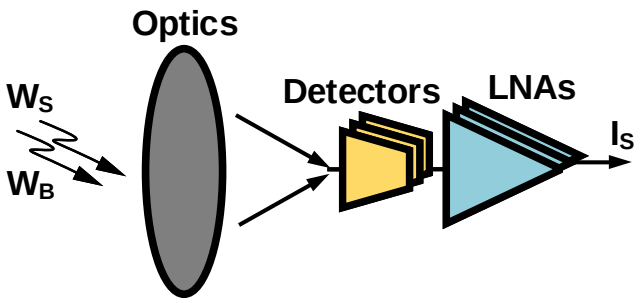


Figure 1.1. Schematic of direct detection. W_S is the signal power and W_B is the background radiation power.

an array of LNAs and consequent power consumption considerations [35]. Power consumption of the LNA is also important for scalable coherent detection method.

Here in this dissertation, I am focusing on a specific type of incoherent detection technology: MKID. In Fig. 1.2 you can see 1800 pixels as an MKIDs array which will be implemented inside, and a millimeter-wavelength camera. Three different arrays are implemented inside the camera to cover 2, 1.4, and 1.1 mm wavelengths. The total number of detectors is 7718, and 13 LNAs are required to read out detectors. The design and implementation of the LNAs for this particular example are described in the dissertation.

For this type of detection, typically, thousands of detectors are coupled to a single transmission line, and an array of LNAs should amplify the detected signal at once. That is why intermodulation of the detected signals is also important for the LNA, and consequently, linearity specifications of the LNA should be characterized.

1.1.1.2 Coherent Detection

Coherent detection is done by a heterodyne structure in which the terahertz signal is down-converted to an intermediate frequency (IF) by a mixer. It can preserve both phase and amplitude information. This method usually provides high spectral resolution compared to the previous method because $\nu_{\mathrm{IF}} \ll \nu$. A schematic of typical

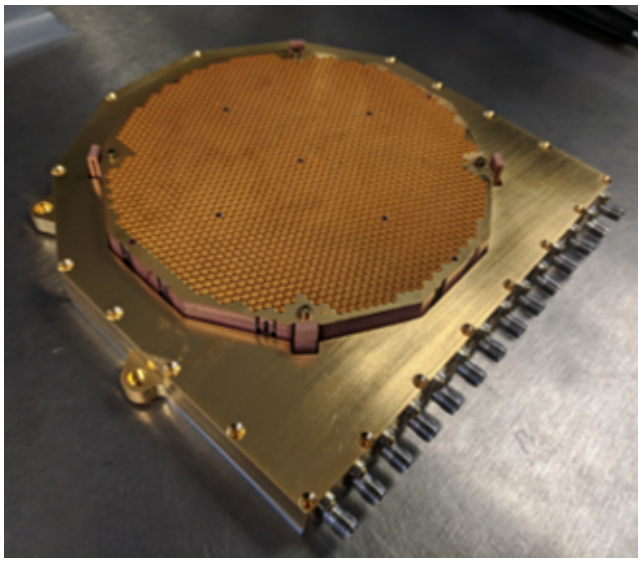


Figure 1.2. TolTEC 1.1 mm MKID Array 1800 pixels, 3600 detectors [10].

heterodyne structure is shown in Fig. 1.3. As shown, a mixer and local oscillator are required to down-covert the detected terahertz frequency to IF.

Typically the mixer contributes the most noises to the heterodyne receiver [27]. Basically, any nonlinear electronic device can be used as a mixer. However, the choice of mixer is essential for receiver sensitivity. The most used technologies (at THz frequencies) for the mixer are superconductor-insulator- (SIS) tunnel junctions, semiconductor and superconducting hot-electron bolometers (HEBs), Schottky diodes. SIS provides the best sensitivity for lower than 1.3 THz frequency range and usually requires >4 GHz IF. At larger frequencies (higher than 1.3 GHz), intrinsic noise of SIS mixer is increasing because high-frequency losses increase. HEB is typically used for 1.3–5 THz frequency range and ν_{IF} <4 GHz [83].

Scalability is even more challenging for coherent detectors. The biggest challenge is the requirement of an IF channel for each element. Another challenge is the limitation of solid-state LO power, which is on the range of milliwatt or microwatt in the terahertz range. Moreover, semiconductor lasers that are used in IR and optical

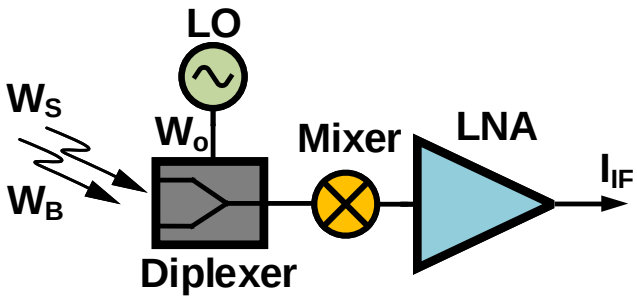


Figure 1.3. Schematic of heterodyne detection. W_S is the signal power and W_B is the background radiation power. W_o is LO radiation power.

bands are not available in most of the terahertz bands. The Fig. 1.4 is showing the terahertz gap with respect to source technology.

A scalable 64 pixels heterodyne array that integrates mixers and amplifiers into a single array is implemented [38]. In this case, IF LNA power consumption is limiting the scalability of coherent detectors. Cryocoolers efficiency drops significantly ($\sim$1 % of Carnot efficiency at 4 K [72]) with temperature, and it limits the capacity to remove the heat generated inside a cooler. That is why sub-milliwatt cryogenic LNAs are required for practical thousands pixels array.

An integrated wideband low-power LNA is proposed in the dissertation for the heterodyne structure based on an HEB mixer. Usually, the noise performance of the HEB mixer is poor at higher than 4 GHz IF bandwidth. Therefore, having wideband cryogenic LNA working at the lowest possible frequency is desirable for this particular application.

1.1.2 Quantum Computing Scalable Readout

Quantum computing technology is grown quickly in the past decade. It heavily relies on microwave technologies for readout and control parts. As an example, currently, for a 50-qubit Google quantum processor, four racks of microwave electronics, including 250 base-band arbitrary wave generators (AWGs), 50 single side-band

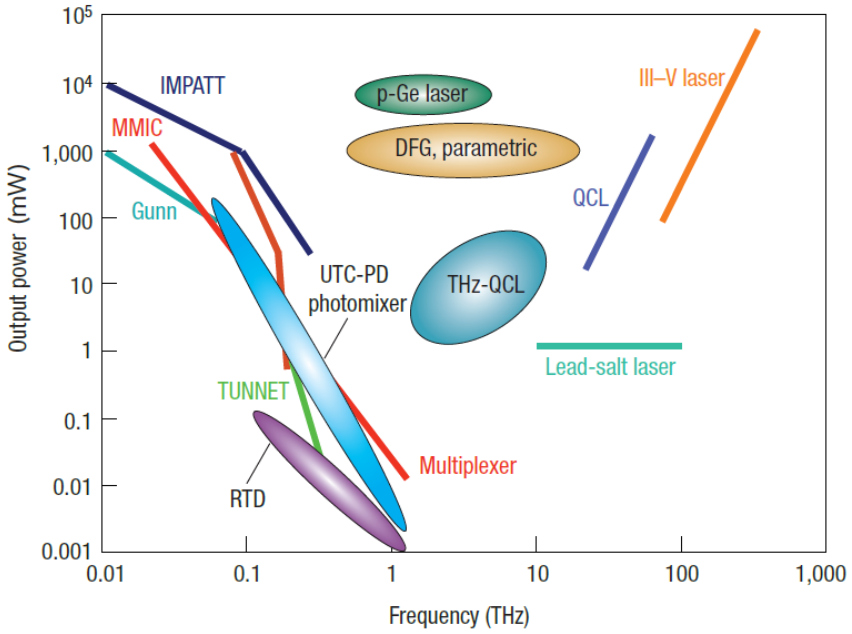


Figure 1.4. Terahertz emission power regard to frequency which shows the gap with respect to source technology [88].

(SSB) modulators, 10 SSB demodulators, 8 frequency synthesizers, and 10 digitizers, are used [11]. State-of-the-art error rates for control and readout depend on the type qubit, that are in the range of 10^{-4} to 10^{-2}, which is much higher than typical classical computers. That is mainly because of the noise toleration difference between classical and quantum computers. That is why there are some error correction techniques for large-scale computations in the quantum computing field [77]. Integrated circuits will be the ultimate solution because thousands/millions of qubits are required for reliable error counted quantum processors.

Recently, in the literature, an integrated approach is investigated for the control part of these processors [12] as shown in Fig. 1.6. However, here, I am focusing on just the readout part of quantum computing.

For practical quantum algorithms, 1% error rate is required. Since a qubit's state energy level is much lower than the sensitivity of detectors (for example, for trans-

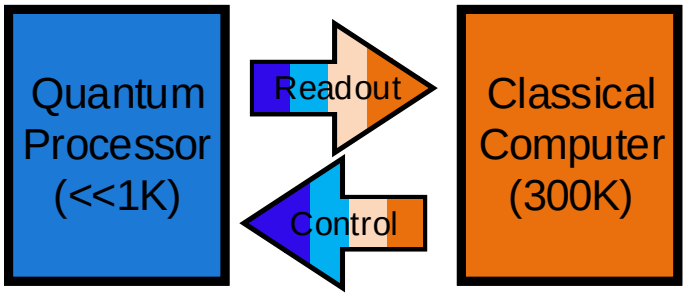


Figure 1.5. Fault-tolerant quantum computer with feedback loop of classical computer.

mon qubit, a single 5 GHz microwave photon carrying the energy of about 20 μeV), reflection coefficient difference is measured rather than the absolute value of energy level by radio frequency reflectometry [13]. This approach is also used for spin qubit readout because of the higher charge sensitivity of this approach. In the rest of this section, the quantum processor readout approach and LNA requirements are briefly described for two types of qubits (spin and transmon).

1.1.2.1 Spin Qubit Readout

A single spin qubit device can be built as a double-gate nanowire FET implemented in a fully-depleted silicon-on-insulator (SOI) process. Since the gate impedance of an FET is high, an impedance matching network is required for conversion of the high impedance to 50 Ω. A simplified electrical model of a single spin qubit including an LC matching network is shown in Fig. 1.7. Depends on the state of a qubit, the capacitor value at the gate can be different (ΔC), and this information via phase difference of the LC matching network response can be detected [70]:

$$tg(\Delta\varphi) \simeq (\frac{1-\Gamma_0}{1+\Gamma_0})Q_{\mathrm{M}}(\frac{2\Delta C}{C_{\mathrm{p}}+C_{\mathrm{M}}}), \tag{1.3}$$

where C_{M} and Q_{M} are matching network capacitor and quality factor, C_{p} is parasitic gate capacitor, and Γ_0 is the return loss of state zero. Typically, ΔC is lower than

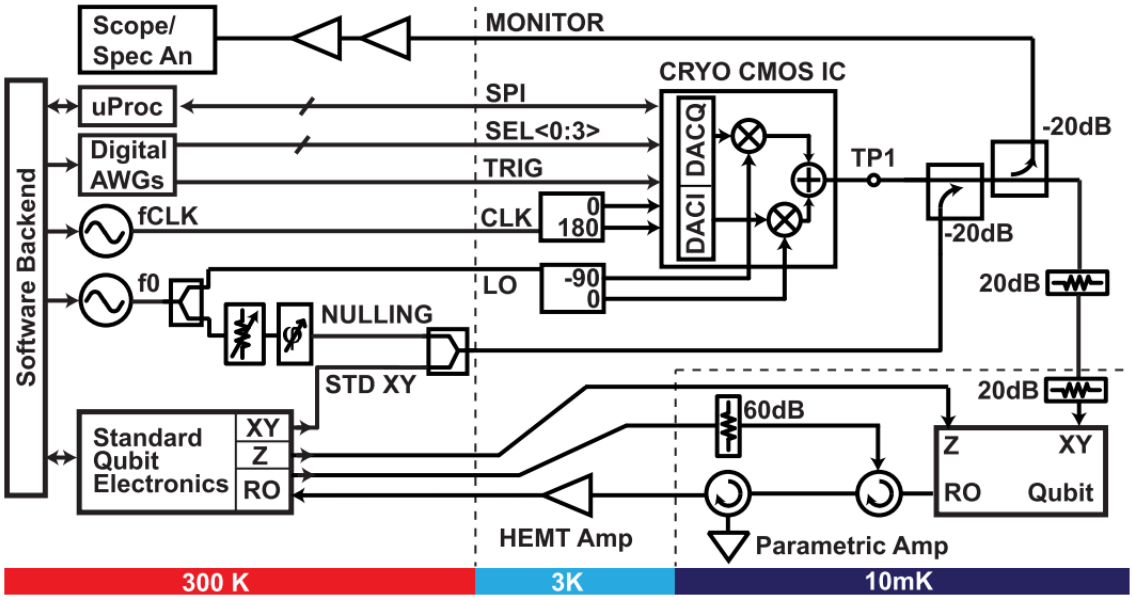


Figure 1.6. Integrated quantum control approach described in [12].

1 fF [4], and the minimum value of $\Delta\varphi$ determines type of modulation. As shown in Fig.1.8, for demodulation of a signal with a lower than 0.01% bit error rate (BER), around 8, 12, 16, and 22 dB SNR for 4, 8, 16, and 32-PSK modulation are required, respectively. SNR of the readout is mainly determined by the LNA and insertion loss of the circulator, and the noise performance of the LNA can be calculated based on the calculated SNR (from Fig. 1.8), qubit probe signal power, and bandwidth of the readout. A simplified block diagram of spin qubit readout is shown in Fig. 1.7.

1.1.2.2 Transmon Qubit Readout

The idea of reflection coefficient measurement for a single transmon qubit is shown in Fig. 1.9. The nonlinear behavior of the qubit resonator pulls readout resonator frequency into different states. This frequency difference between two states of the qubit is called "dispersive shift." If the dispersive shift is selected to be equal to the resonator linewidth, a phase-contrast as high as 180 degrees between 0 and 1 can be measured. A sample of a phase difference measurement is shown in Fig. 1.10.

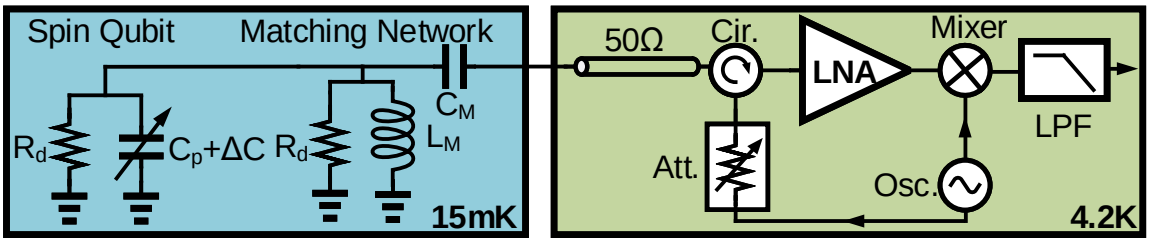


Figure 1.7. Simplified model of a spin qubit and readout front end block diagram. Figure is reproduced from [70].

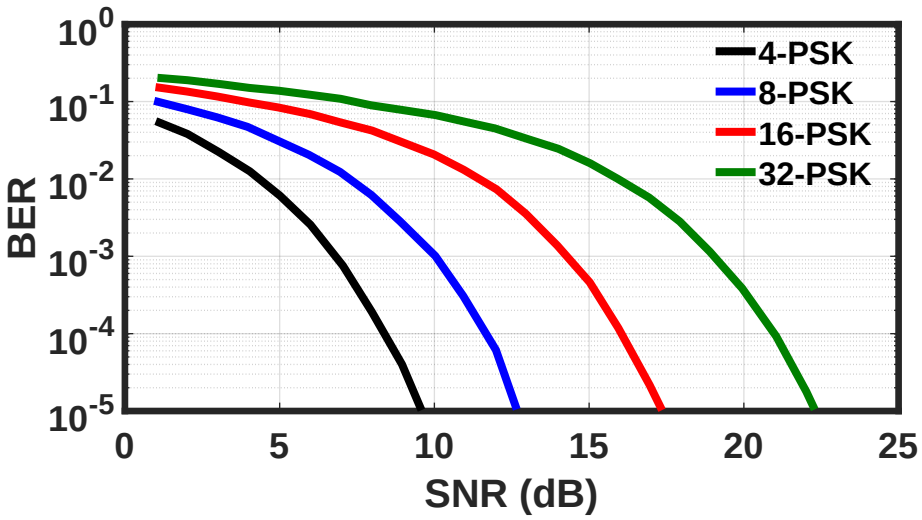


Figure 1.8. BER of MPSK via SNR for a given fixed phase error ($\theta = 0$). Figure is reproduced from [49].

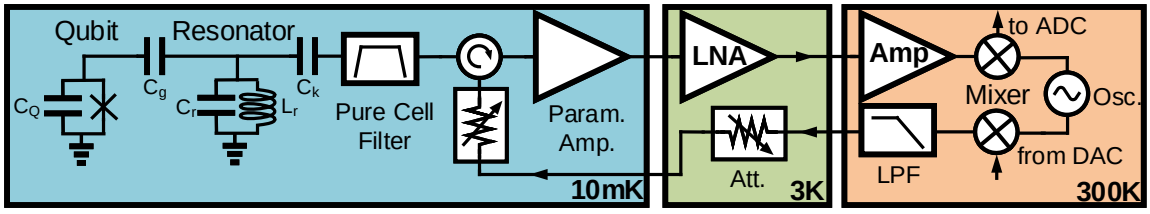


Figure 1.9. Simplified model of transmon qubit and readout block diagram. Figure is reproduced from [13, 54].

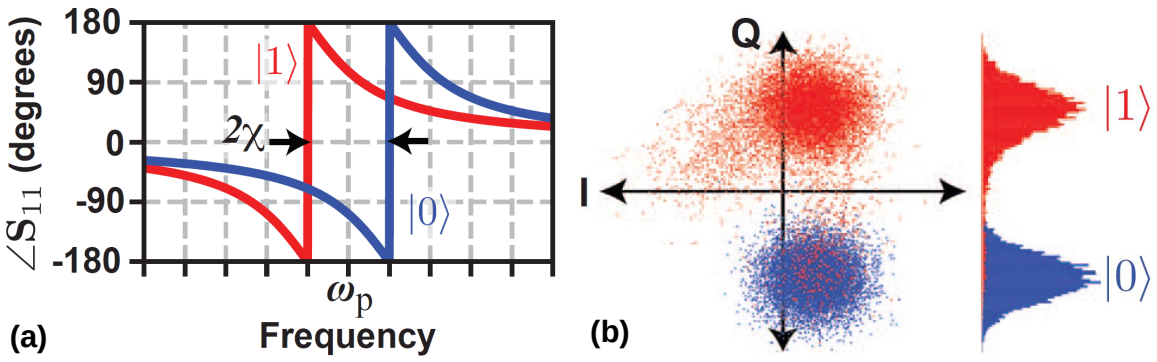


Figure 1.10. (a) State-dependent dispersive frequency shift which can be detect as a phase shift in reflection phase. (b) Typical baseband constellation measurement. Blue and red colors correspond to 0 state and 1, respectively[11].

To characterize readout accuracy measurement, error probability function of 180 degree phase shift measurement should be minimized ($P_{\text{error}} = \frac{1}{2}\text{erfc}(\sqrt{\text{SNR}})$). After adding system parameters to the error probability function [74] :

$$P_{\text{error}} = \frac{1}{2}\text{erfc}\left(\sqrt{\frac{\epsilon n \kappa \tau}{1 + T_{\text{RX}}/T_{\text{Q}}}}\right), \tag{1.4}$$

Where ϵ is loss factor (because of limited quantum efficiency which is less than 1), n is the average number of photons, κ is ring-up rate, τ is an integration time, T_{RX} is input-referred noise temperature of measurement readout, and T_{Q} is quantum limit for noise ($T_{\text{Q}} = \hbar f/2k$) added by a phase-preserving amplifier. To improve error rate, the obvious way is to increase the number of photons. However, there is a fundamental limitation because of the non-linear nature of the qubit resonator, which causes frequency variation for a high number of photons. Typically, $n \leq 25$ for transmon qubits [80]. Another factor in improving the error rate in quantum computer readout related to this dissertation is T_{RX}. It can be shown that for reaching an error rate lower than 1%, a cryogenic LNA near the quantum limit noise is required. Currently, the best state-of-the-art semiconductor-based cryogenic low noise amplifiers based on InP HEMT are eight times higher than the quantum limit of noise [1].

Moreover, even if the quantum noise limit was achievable, it would be impractical to put a semiconductor cryogenic amplifier due to the required nanowatt level power consumption. This is because of the heatsink considerations of the 10-mK stage of the dilution refrigerator. Currently, the only approach is using Josephson parametric amplifier before the semiconductor LNA [20, 3].

Integrated circuit readouts will be the most promising approach because thousands of qubits are required for reliable quantum processors. Consequently, the integrated readout is an open problem for quantum processors. In this dissertation, I tried to address those issues which are related the LNA scalability. Notably, in [95], it is shown that the proposed SiGe HBT based LNA is a promising replacement for InP HEMT LNA (which is currently the first choice for readout of the specific type of qubit quantum computer readout) in the readout.

1.2 Need for Programmable Integrated Cryogenic LNAs

An LNA with tunable specifications is studied due to demands for versatile radio transceivers for multiple standards such as ISM, WiFi, Bluetooth, and WiMAX. Particularly, for the applications which are vulnerable to undesired interferes, and when power consumption is critical, having an LNA with tunable frequency response is more desirable rather than a wideband LNA. As an example for the mentioned application, Fig. 1.11 shows a room temperature CMOS LNA with programmable frequency response is designed and implemented for 2.1–6 GHz frequency band based on transistor scaling approach.

Moreover, for multi-standard wireless sensor applications, having an LNA with tunable frequency response to avoid wideband LNA and reduce power consumption is desirable. In [59], authors designed and implemented a band-tunable CMOS LNA based on 45 nm CMOS SOI technology for the mentioned application. An LC switch tank approach is used to achieve the tunable frequency response as shown in Fig. 1.12.

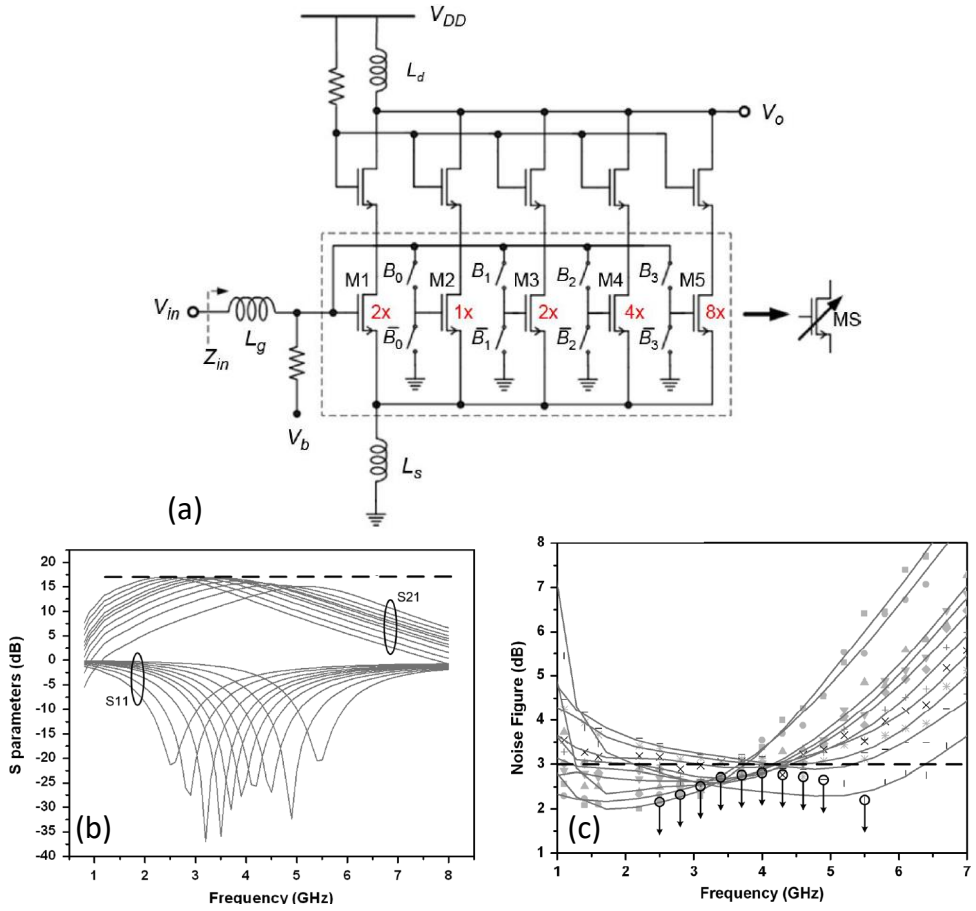


Figure 1.11. Tunable frequency response LNA with transistor size scaling approach for versatile radio transceiver applications [92]. (a) LNA schematic, (b) Measured S parameters, and (c) Measured noise figure.

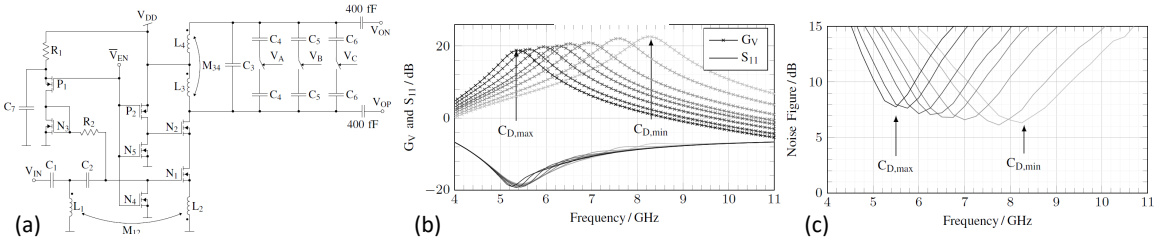


Figure 1.12. Tunable frequency response LNA with LC-switch approach for wireless sensor applications [59]. (a) LNA simplified schematic, (b) Measured S_{11} and voltage gain, and (c) Measured noise figure.

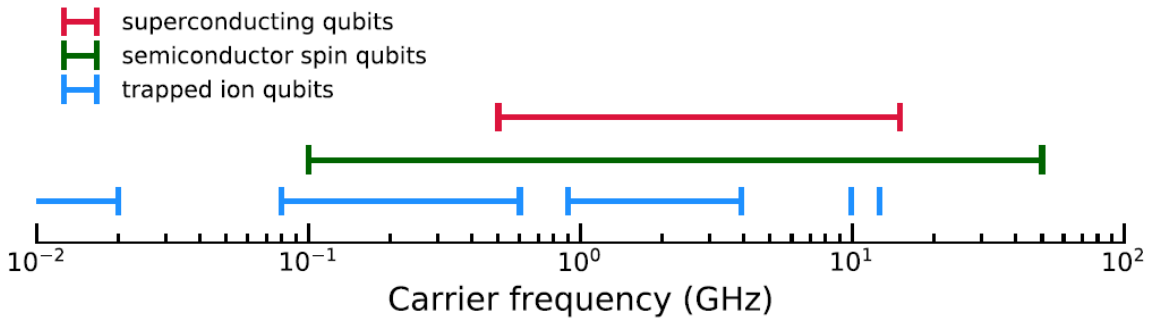


Figure 1.13. Different frequency ranges requiered for different type of qubits control and readout. For example, the carrier frequency for trapped ions can be in the a few MHz range. The narrow trapped ion carrier frequency bands at ∼10 GHz and ∼12.6 GHz. The figure is reported in [13].

The ability to tune characteristics of LNA is also desirable for cryogenic applications because the warming up and cooling down process of the LNA is time-consuming, and typically there is uncertainty in the exact LNA requirement for a particular application. For example, for the readout of quantum processors, which I discussed in the last section, different frequency ranges are required depending on the type of qubit, as shown in Fig. 1.13. In the dissertation, I have taken advantage of full CMOS stacks of the BiCMOS process to design and implement a programmable cryogenic LNA with tunable gain, power consumption, and frequency response.

CHAPTER 2

OPEN PROBLEMS OF CRYOGENIC LNAS SCALABILITY

Here in this chapter, some specific open issues of cryogenic LNAs are summarized. These open problems are addressed in the dissertation.

2.1 Open Issues

1. In general, sensitive THz heterodyne receivers require ultra-low-noise and sub-milliwatt cryogenic LNAs. Particularly, scalability of Hot-Electron Bolometer (HEB) mixer-based receiver requires ultra-low noise and low power cryogenic LNA, which covers a wide very-low-frequency band because of the limited IF bandwidth of this type of technology. It was shown before that SiGe HBTs provide an excellent compromise between noise temperature and power consumption, ideal for SIS mixer-based heterodyne receivers. However, based on the author's knowledge, no cryogenic LNA is reported, which satisfies the bandwidth, noise temperature, and power consumption required for LNAs of HEB mixer-based receivers.

2. Cryogenic compression characteristic of the LNA is essential for scalable incoherent detection, using multiplexed detectors. However, there is no significant research about linearity performance and characterizations of SiGe HBT cryogenic LNAs for this specific type of application. Here I tried to characterize compression point and inter-modulation of a cryogenic LNA as a part of MKID readout.

3. Scaling up the number of cryogenic LNAs to thousands (which is the requirement of future quantum processor detectors and focal plane array) requires a robust biasing circuitry that allows all LNAs to be biased simultaneously. This biasing approach should be extremely low noise and low power, not to cause degradation of the LNA noise and power performance. Preferably, the on-chip method is more desired because of easier scalability with other readout components. The biasing requirement is even more extreme for SiGe HBT because of these devices' exponential I-V curve function. Typically, a sub-mV resolution is required to bias up these transistors.

4. Noise reproducibility of cryogenic LNAs must be understood and optimized to implement a large-scale array of LNAs. Therefore, automatic adjustment of the amplifier parameters is essential for this purpose. Moreover, different applications require LNAs for different frequency bands. For example, each type of qubit works in a specific frequency range. Having a cryogenic LNA with tunable frequency response while maintaining noise and power performance can satisfy all of these applications. Furthermore, as thermal cycling of a cryogenic system is time-consuming, there is often considerable uncertainty in the exact LNA requirements (e.g., frequency and bandwidth) for a particular application. BiCMOS process potentially can be used for this cryogenic tunable LNA, which has not been done yet based on the author's knowledge. Also, there are some considerations for the design of this LNA, such as accurate passive components cryogenic modeling, low noise digital part, and characterization approaches.

2.2 Dissertation Contributions

The contributions of the dissertation for the open scalability issues of cryogenic LNA are listed as follow:

1. **Device Cryogenic Performance Characterization**: In this chapter, the SiGe HBT cryogenic performance of three different state-of-the-art BiCMOS technologies are investigated. This chapter is focusing on noise performance comparison and evaluation of these technologies for cryogenic LNAs. Notably, a specific process is optimized for SiGe HBT noise performance. Therefore, cryogenic performance comparison is done between standard and optimized transistors of the process. It is shown how fabrication optimization improves the cryogenic performance of SiGe HBT. After that, based on the on-wafer cryogenic measurement, a cryogenic standard noise and small-signal model of the transistors are created for amplifier simulations. Finally, some passive component characterizations across the temperature are done as a part of BiCMOS LNA design process. The optimized noise process cryogenic performance and modeling are published in the 2020 IEEE/MTT-S International Microwave Symposium (IMS) [95].

2. **State-of-the-Art SiGe HBT Cryogenic LNAs**: Three state-of-the-art SiGe HBT cryogenic LNAs are designed and implemented for radio astronomy applications based on the created models of the previous chapter. The first amplifier is characterized for readout of a millimeter-wavelength camera detection, and both room temperature and cryogenic performance are measured. The second amplifier is characterized as a part of the HEB mixer-based receiver. The third amplifier is a wideband design for heterodyne mixer-based applications. The design process and measurement results of two of these LNAs are published in IMS 2019 and 2021 [46, 47].

3. **Biasing Integration of BiCMOS Cryogenic LNA**: Different approaches of biasing of SiGe HBT cryogenic LNAs are described and investigated. An on-chip and low power method is used for integration of bias of cryogenic LNA,

and the first bias integrated cryogenic LNA is designed and implemented to verify the. Moreover, the first on-chip low-power cryogenic digital to analog converter (DAC) is designed and used as a part of the LNA biasing circuit.

4. **Programmable Cryogenic LNA**: The ability to tune the performance characteristics of a cryogenic LNA is described as an advantage for the BiCMOS stack. Furthermore, the first programmable cryogenic LNA is designed and implemented for quantum computing readout application. As experimental results, critical LNA specifications such as ripple, noise temperature, bandwidth, center frequency, absolute value of gain, and bias currents are programmed digitally. The amplifier is measured in different tuning states at cryogenic temperature, and the mentioned biasing approach is used for the LNA. Moreover, a programmable RLC resonator which is the core of the designed is characterized and verified at cryogenic temperature. The programmable LNA is a collaborative project with Zhenjie Zou. Some portions of this chapter are published in IMS 2021 [100].

CHAPTER 3

FUNDAMENTAL REVIEW OF SIGE HBTS AND EXPECTED CRYOGENIC PERFORMANCE

In this chapter, the fundamental physics and operation principles of SiGe HBTs are described. Then, the expected cryogenic performance of SiGe HBTs is reviewed. Moreover, standard small-signal and noise models of the devices are briefly explained. These models will be used in the next section for the cryogenic model creation of the SiGe HBTs, consequently, for design and simulations of cryogenic LNAs in the dissertation.

The evaluation and expected cryogenic performance of SiGe HBTs is explored deeply in the literature [18, 26, 25, 64, 42]. In [18], it is shown that the SiGe HBT is a promising choice for cryogenic LNA design because of a large increase in DC current gain (β_{DC}) and moderate gain in f_{t} and f_{max} with cryogenic cooling. Moreover, author proposed a small-signal and noise model for a HBT at cryogenic temperature. This model was verified experimentally through cryogenic LNA measurements. In [64], the authors proposed a modified small-signal model for cryogenic SiGe HBTs and showed these devices can keep their performance at V_{CE} near knee voltage which proves SiGe HBTs are also ideal choices for low-power cryogenic LNA design. The linearity of these devices is investigated in [42], and a non-linear model of cryogenic HBT is proposed and verified [96]. Cryogenic performance of SiGe HBT based LNAs are verified for a wide frequency range from near DC to 120 GHz [90, 73, 58, 86, 15].

3.1 Device Physics of SiGe HBTs

In order to better understand SiGe HBT physics, this chapter is began by reviewing the physics of a standard bipolar junction transistor (BJT), and its main noise performance limitation are discussed.

3.1.1 BJT Energy Band Diagram

The energy band diagram of a BJT device in the active region is shown in Fig. 3.1. The DC current gain (β_{DC}) of the BJT, which it will be shown as an important parameter for noise performance of the device, can be calculated as [26]:

$$\beta_{\mathrm{DC,BJT}} \approx \frac{\mu_{nb} L_{\mathrm{PE}} N_{\mathrm{DE}}^{+}}{\mu_{pe} W_{\mathrm{B}} N_{\mathrm{AB}}^{-}}, \tag{3.1}$$

where μ_{nb} and μ_{pe} are carrier mobilities in the base and emitter, respectively. L_{PE} and W_{B} are emitter diffusion length and base width, N_{DE}^{+} is ionized donor concentration in emitter, and N_{AB}^{-} is ionized acceptor concentration in base.

The ratio of doping in the emitter to the base can be increased, or the base width can be decreased to improve current gain of a BJT. However, both of these approaches cause higher base sheet resistance which can degrade the noise performance of the device. Explicitly, the base sheet resistance can be calculated as [6]:

$$R_{\mathrm{B}} = \frac{1}{q \mu_{pb} W_{\mathrm{B}} N_{\mathrm{AB}}^{-}} (\Omega/\mathrm{square}), \tag{3.2}$$

where μ_{pb} is the mobility of holes in the base. A solution to the trade-off between DC current gain and base sheet resistance was proposed by Kroemer in 1957 [55], and will be discussed below.

3.1.2 Band Engineering in SiGe HBT

The idea of the energy band diagram of SiGe HBT is shown in Fig. 3.2. As shown, by adding Germanium (which has a significantly lower energy bandgap compared to

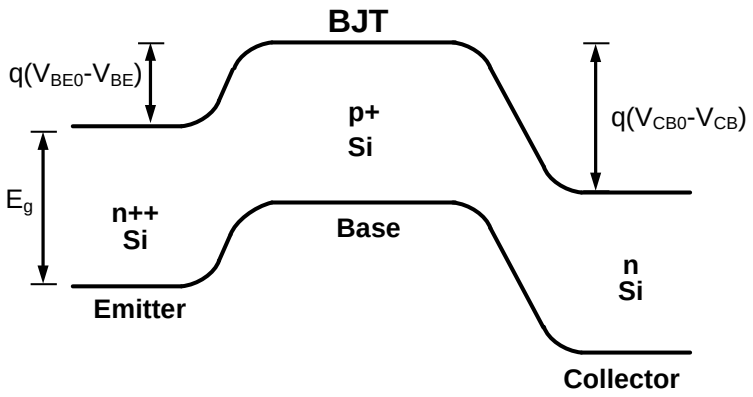


Figure 3.1. Energy band diagram of simple BJT device under active forward operation.

Silicon) in the base, the non-uniform energy band diagram can be achieved. Since the emitter material has a wider bandgap than the base material, the minority carrier from the emitter to the base will face a smaller barrier than carriers back from the base to the emitter. As a result of this heterojunction, the DC current gain of the transistor is enhanced exponentially [55]. Typical doping and Ge profile are appear in Fig. 3.3 [85]. As shown, Ge concentration is increased gradually from emitter to base.

The improvement in DC current gain achieved due to the Ge content in a SiGe HBT with respect to that of an otherwise identical Si BJT can be quantified as [26]:

$$\frac{\beta_{\mathrm{SiGe}}}{\beta_{\mathrm{Si}}} \approx \chi \frac{\mu_{nb,\mathrm{SiGe}}}{\mu_{nb,\mathrm{Si}}} \times \Delta E_{\mathrm{g,Ge(grade)}}/kT_a \times \frac{e^{\Delta \mathrm{E}_{\mathrm{g,Ge(0)}}/KT_a}}{1 - e^{-\Delta \mathrm{E}_{g,\mathrm{Ge(grade)}}/KT_a}}, \tag{3.3}$$

where χ is effective density-of-states ratio (typically <1), μ_{nb} is mobility of carrier in base, $\Delta E_{\mathrm{g,Ge(0)}}$ is difference of energy bandgap at emitter, and $\Delta E_{\mathrm{g,Ge(grade)}}$ is difference of energy bandgap at collector. The last two parameters are the function of Ge doping profile, which is the key factor in improving the DC current gain in SiGe HBTs.

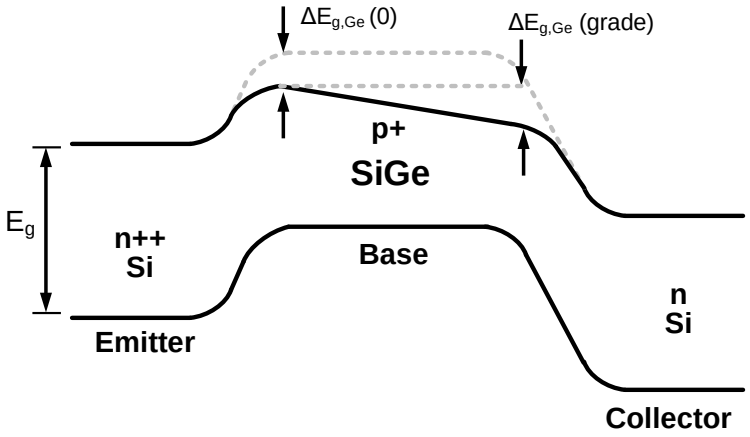


Figure 3.2. Energy band diagram of simple SiGe HBT device under active forward operation.

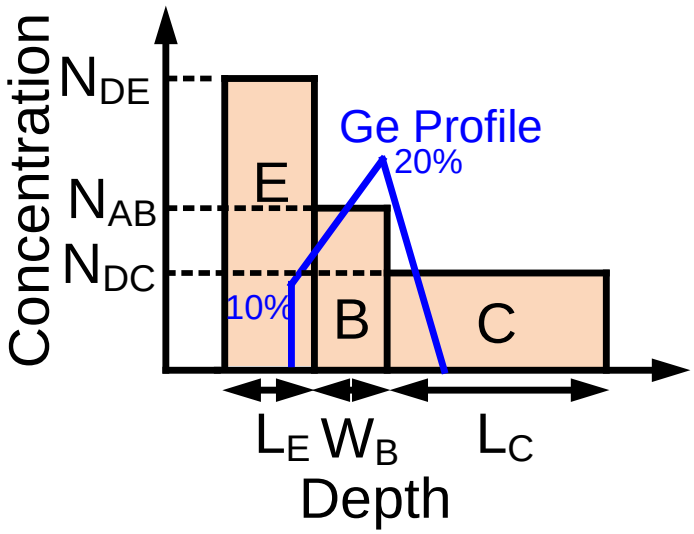


Figure 3.3. Schematic of doping and Ge profile for a typical SiGe HBT. Figure reproduced from [85].

3.1.3 SiGe HBT Fabrication Process

Since the full BiCMOS stack is used to implement cryogenic LNAs, understanding the fabrication process, including CMOS integration, will be helpful. The CMOS integration approaches and processing steps associated with each technology platform technology can be different. However, there are some common fabrication process steps for a typical SiGe HBT device. Here these steps are summarized [26]:

1. Adding n^+ sub-collector on a p^- substrate to allow CMOS integration.
2. High temperature lightly doped n-type collector.
3. Polysilicon trenches to isolate sub-collector of devices.
4. Thin oxide trenches to isolate devices from each other.
5. Implementation of collector sinker to the sub-collector.
6. SiGe epitaxy layer including Si buffer, the active layer, and a-Si cap.
7. Emitter-base self alignment which is similar to Si BJT technology.
8. Collector implantation to improve high current density performance.
9. Polysilicon extrinsic as base contacts and silicided extrinsic base.
10. Heavy-doped or implanted polysilicon as the emitter.
11. Back-end-of-line (BEOL) metalization (Al or Cu).

A typical cross-section of a fabricated SiGe HBT device is shown in Fig. 3.4. This picture is drawn through first metal.

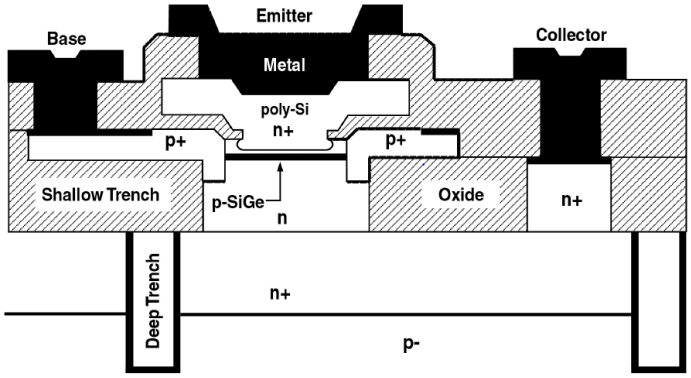


Figure 3.4. Cross section of a typical SiGe HBT device [26].

3.1.4 CMOS Integration with SiGe HBT

One of the most important advantages of SiGe technologies compare to III-V technologies is that they are generally integrated within CMOS processes. This advantages allows digital circuits to be co-integrated in a high performance circuit; this capability is leveraged in this dissertation. A brief overview of the BiCMOS fabrication process is described in this section.

There are two approaches for integration of SiGe HBTs with CMOS. The first is "base-during-gate" (BDG) and second is "base-after-gate" (BAG) [44, 43]. Each one has it's own pros and cons. BDG has less complex structures, however, the SiGe HBT epitaxial base sees all CMOS thermal cycles which causes broadening of the base profile. Modern technologies are using BAG which first CMOS process is completed then SiGe epitaxial base is deposited. CMOS fabrication process in BAG is very similar to pure CMOS process. In BAG the SiGe HBT can be optimized for RF performance. The flowchart of both BDG and BAG process including SiGe HBT fabrication steps is shown in Fig. 3.5.

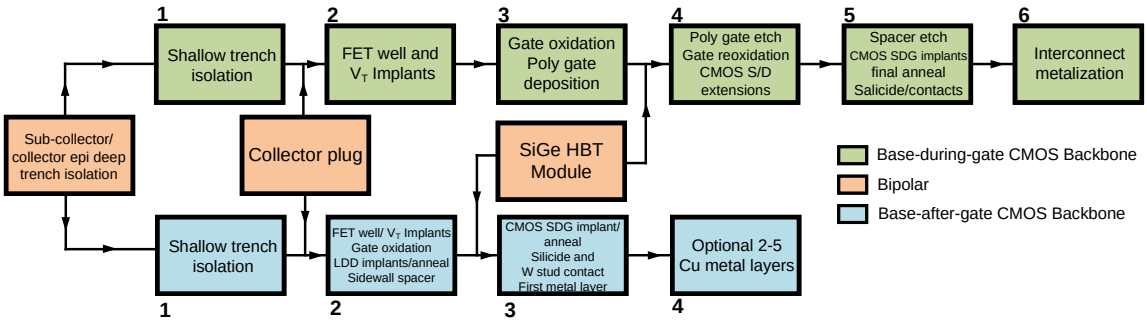


Figure 3.5. BiCMOS fabrication process flowchart for BDG and BAG approaches. Figure is reproduced with some changes from [26].

3.2 SiGe HBT Equivalent Circuit Model

3.2.1 Ebers-Moll Equivalent Model

The first equivalent circuit proposed for a bipolar transistor is the Ebers-Moll model [26]. The model of an NPN device is shown in Fig. 3.6. It consists of two back-to-back diodes, which I_{F} and I_{R} are the emitter currents at forward and inverse operations, respectively. Also, α_{F} and α_{R} are common-base (CB) current gains at forward and inverse operations. I_{F} and I_R are a function of V_{BE} and V_{BC} as:

$$I_{\mathrm{F}} = I_{\mathrm{F0}}(e^{qV_{\mathrm{BE}}/kT} - 1), \tag{3.4}$$

$$I_{\mathrm{R}} = I_{\mathrm{R0}}(e^{qV_{\mathrm{BC}}/kT} - 1), \tag{3.5}$$

Where I_{F0} and I_{R0} are the saturation currents of forward and inverse emitter currents.

3.2.2 Small-signal Equivalent Model

The large-signal model described can be linearized as a small-signal model for a specific dc operation point. The schematic of this model is shown in Fig. 3.7(a). $g_m = I_{\mathrm{C}}/V_{\mathrm{T}}$ and $r_{be} = \beta/g_m$. By adding parasitic resistors and capacitors and substrate nodes, a high-frequency small-signal model of SiGe HBT can be achieved,

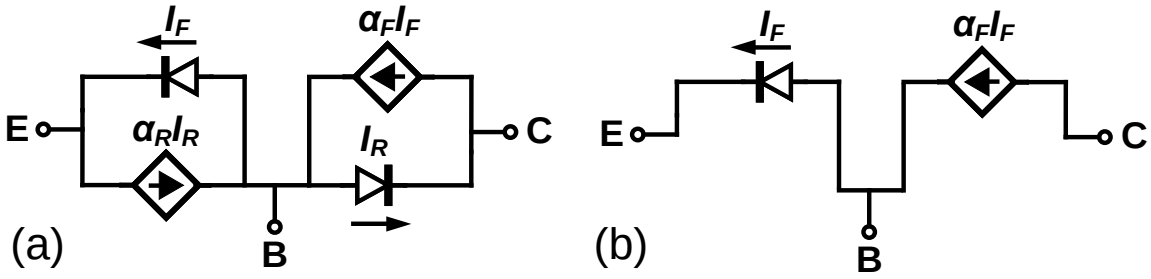


Figure 3.6. (a) Simple Ebers-Moll model of NPN device (b) Ebers-Moll model of NPN at active region.

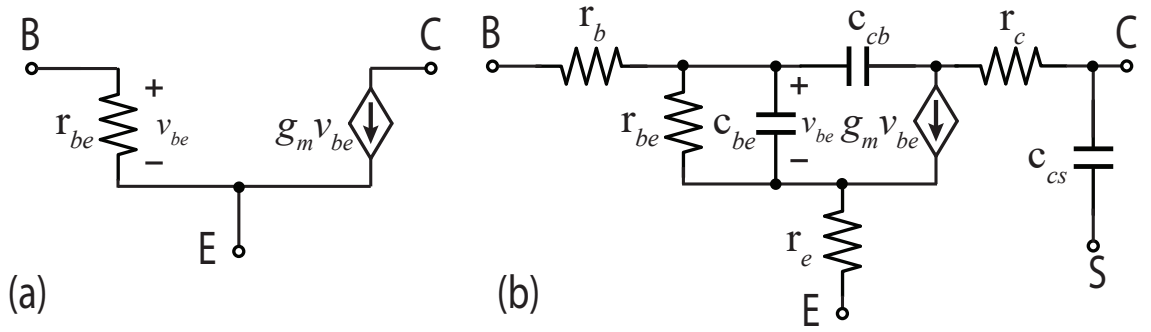


Figure 3.7. (a) Simple linearized small-signal model of BJT device (b) High frequency small signal model of SiGe HBT.

which is shown in Fig. 3.7(b). f_t and $f_{\max}$ which are two critical factors of SiGe HBT describing RF performance of the device, can be calculated from this model as:

$$f_t \approx \frac{g_m}{2\pi(C_{be} + C_{cb})}, \tag{3.6}$$

$$f_{max} \approx \sqrt{\frac{f_t}{8\pi r_b C_{cb}}}, \tag{3.7}$$

3.3 Noise Sources in SiGe HBT

An understanding of the source of noise in a SiGe HBT permits the design of cryogenic low noise amplifiers. Here the primary noise sources of SiGe HBTs are listed.

3.3.1 Shot Noise

Shot noise is generated when a carrier passes a barrier in a junction. Shot noise exists in every forward biased diode structure. It can be assumed the shot noise is frequency independent because the phase delay in the junction is negligible in typical target frequency bands of cryogenic LNAs [71]. The spectral density of shot noise current can be written as $\overline{|i|^2} = 2qI$, where I is the dc current of the junction and q is the electron charge.

As discussed, there are two junctions in the SiGe HBT device. The first one is between base and emitter. Therefore, the total shot noise at the base-emitter junction can be obtained from this formula:

$$\overline{|i_{n,e}|^2} = 2q(I_{\mathrm{En}} + I_{\mathrm{Ep}}), \tag{3.8}$$

where $I_{\mathrm{E,n}}$ and $I_{\mathrm{E,p}}$ are electrons injected from the emitter to the base and holes back injected from base to emitter, respectively [32].

Another junction is between base and collector. The current magnitude going through this junction is the same as the emitter junction, but there is a delay. It can be formulated as:

$$\overline{|i_{\mathrm{n,c}}|^2} = \overline{|i_{\mathrm{n,e}} e^{-j\omega\tau_n}|^2}, \tag{3.9}$$

where τ_n is the transit time. As mentioned, these two shot noise sources are correlated to each other [67].

Since the common-emitter topology is mostly used for cryogenic LNA design, it can be rewritten and represent the noise sources for common-emitter structure as:

$$\overline{|i_{\mathrm{n,c}}|^2} = 2qI_{\mathrm{C}}, \tag{3.10}$$

$$\overline{|i_{\mathrm{n,b}}|^2} = \overline{|i_{\mathrm{n,c}}|^2} + \overline{|i_{\mathrm{n,e}}|^2} - 2\mathbb{R}\{\overline{i^*_{\mathrm{n,e}} i_{\mathrm{n,c}}}\}, \tag{3.11}$$

where $i_{\mathrm{n,c}}$, $i_{\mathrm{n,e}}$, and $i_{\mathrm{n,b}}$ are total noise current power spectral densities of collector, emitter, and base, respectively. The base and collector shot noises are correlated as [67]:

$$\overline{|i^*_{\mathrm{n,b}} i_{\mathrm{n,c}}|} = \overline{|i^*_{\mathrm{n,e}} i_{\mathrm{n,c}}|} - \overline{|i_{\mathrm{n,c}}|^2}, \tag{3.12}$$

it can be shown that the shot noise correlation factor between base and collector in the CE topology can be calculated as:

$$\overline{|i^*_{\mathrm{n,b}} i_{\mathrm{n,c}}|} = 2qI_{\mathrm{C}}(e^{-j\omega\tau_n} - 1), \tag{3.13}$$

$\omega\tau_n$ is negligible in the target frequencies of this dissertation (<10 GHz). So the noise correlation factor between emitter and collector can be neglected in our HBT noise models.

3.3.2 Thermal Noise

Thermal noise exists wherever carrier charge is excited thermally. The available thermal noise power can be calculated as [50, 68]:

$$P = \frac{hf}{e^{hf/kT_{\mathrm{a}}} - 1}\Delta f, \tag{3.14}$$

Where f is the frequency range, Δf is the bandwidth, T_{a} is the ambient temperature, k is the Boltzman's constant, and h is the Plank's constant. If $hf \ll kT_{\mathrm{a}}$ which is a

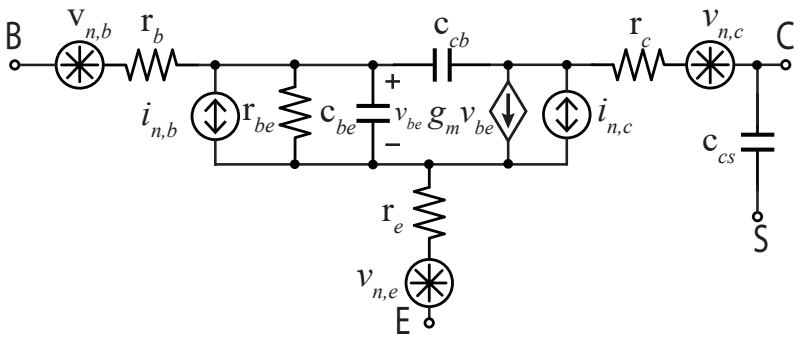


Figure 3.8. SiGe HBT small signal model including noise sources.

reasonable assumption at our target frequency range and ambient temperature, the above equation can be simplified as:

$$P \approx kT_{\mathrm{a}}\Delta f, \tag{3.15}$$

In SiGe HBTs, the main sources of thermal noise are coming from parasitic resistors. The power spectral density (PSD) of each resistor can be written as:

$$S_{\mathrm{V}} = 4kT_aR\ (V^2/Hz), \tag{3.16}$$

where R is the parasitic resistor value. For cryogenic applications of SiGe HBTs, which is the target of this dissertation, thermal noise has less effect on noise performance compared to shot noise. The small-signal model of SiGe HBT, including both shot noise and thermal noise sources, is shown in Fig. 3.8. This model is used for simulations at cryogenic temperatures. In the next chapter, the parameters extraction process of this model is described.

3.4 Expected Cryogenic Performance of SiGe HBTs

Cryogenic expected performance of SiGe HBT are studied deeply in the literature [18]. Here, a summary of the expected performance of SiGe HBT at cryogenic tem-

perature is described. The focus is on important parameters that directly affect the noise performance of the device.

3.4.1 Base Current Density

The base current density (J_{B}) can be written as:

$$J_{\mathrm{B}}(T) \approx \frac{kT\mu_{\mathrm{pe}}(T)n_{io}^2(T)}{L_{\mathrm{PE}}(T)N_{\mathrm{DE}}^{+}(T)}e^{qV_{\mathrm{BE}}/kT}, \tag{3.17}$$

where T is the ambient temperature, k is the Boltzmann's constant, μ_{pe} is the mobility of holes in the emitter, L_{PE} is emitter diffusion length, and N_{DE}^{+} is the concentration of acceptors in the emitter.

μ_{pe} dependence on temperature is a function of dopant concentration, and it is weak because of high dopant concentration (typically $> 10^{19}\mathrm{cm}^{-3}$) in the emitter. N_{DE}^{+} is almost independent of the ambient temperature. L_{PE} can be written as $L_{\mathrm{PE}} = \sqrt{\mu_p \tau_p kT/q}$ [2]. Where μ_p is the mobility of holes, and τ_p is the hole minority carrier lifetime. All of these parameters are nearly temperature-independent [34]. So, L_{PE} is a function of the square root of ambient temperature. The ratio of base current density at cryogenic to room temperature after some approximations can be written as [18]:

$$\frac{J_{\mathrm{B0}}(T)}{J_{\mathrm{B0}}(300)} \approx 7.83 \times 10^{18}(\frac{T}{300})^{3.5}e^{-E_g(T)/kT}, \tag{3.18}$$

where E_{g} is the energy bandgap of Silicon which increases from 1.12 eV at room to 1.17 eV at 4 K [21]. From this analysis, it can be said that J_{B} will decrease significantly at cryogenic temperatures, which improves dc current gain of SiGe HBT and, consequently, the noise performance of the device.

3.4.2 Collector Current Density

A similar process can be applied for the collector current density (J_{C}). However, since the Germanium profile is different among processes, it is difficult to predict

how much the collector current density increases at cryogenic temperature. Nevertheless, the ratio of collector current between cryogenic and room temperatures can be obtained from the below equation [18]:

$$\frac{J_{C0}(T)}{J_{C0}(300)} \approx 7.83 \times 10^{18} (\frac{T}{300})^3 e^{-E_g(T)/kT} \frac{e^{(\Delta E_{g,app}+\Delta E_{g,Ge(0)})/kT}}{e^{(\Delta E_{g,app}+\Delta E_{g,Ge(0)})/k300}}, \tag{3.19}$$

where $\Delta E_{g,app}$ and $\Delta E_{g,Ge}(0)$ are difference of energy bandgaps after adding Germanium to the SiGe HBT.

3.4.3 DC Current Gain

DC current gain (β) is a critical factor that shows the noise performance of SiGe HBT, especially at the low-frequency range (few GHz). The ratio of β between room and cold based on the last two equations can be written as:

$$\frac{\beta(T)}{\beta(300)} \approx \sqrt{\frac{300}{T}} \frac{e^{(\Delta E_{g,app}+\Delta E_{g,Ge(0)})/kT}}{e^{(\Delta E_{g,app}+\Delta E_{g,Ge(0)})/k300}}, \tag{3.20}$$

This shows an exponential improvement on β at cryogenic temperatures. Also, since $\Delta E_{g,app}$ and $\Delta E_{g,Ge}(0)$ are different among fabrication processes, the amount improvement in β depends on the type of technology.

Please note this is an optimistic ideal analysis for the expected improvement of β at cryogenic temperature, and it is valid only to the onset of cryogenic temperature ($\sim$150 K). In [75], it is experimentally shown that tunneling of electrons through the base dominates the collector current density of SiGe HBT at lower cryogenic temperatures. Collector current density is found experimentally to be weakly dependent on temperature below 40 K.

3.5 Conclusion

As shown, the noise performance of SiGe HBT is improved significantly with cryogenic cooling. However, the amount of improvement depends on the Germa-

nium profile and is different among technologies. Therefore, experimental cryogenic performance evaluation is required for each technology. In the next chapter, three state-of-the-art technologies are reported that show excellent improvement of β among other technologies with cryogenic cooling.

CHAPTER 4

SIGE HBT CRYOGENIC CHARACTERIZATION AND TRANSISTOR MODELING

This chapter describes cryogenic characterization and modeling of SiGe HBT from three BiCMOS technologies from Tower Semiconductor, IHP Microelectronics, and Global Foundries, and the potential cryogenic performance of each process for the design of cryogenic LNA is discussed and compared. In addition, HBTs of one of these processes (IHP Microelectronics SG13G2) are optimized particularly for cryogenic noise performance.

The SiGe HBT cryogenic models described in chapter are used and published in [95, 47, 100].

4.1 Tower Semiconductor-SBC18H5/SBC18S5

The SBC18H5 BiCMOS process has six layers of aluminum metal, including a top thick metal layer, suitable for the implementation of RF inductors and transmission lines. It includes two 1.8 V and 3.3 V CMOS transistors. The minimum gate length for the 1.8 V MOS is 180 nm and for the 3.3 V PMOS and NMOS is 300 nm and 360 nm, respectively. The technology also includes high and low-value unsilicided resistors, suitable for cryogenic applications because of the low-temperature coefficient. Hyper-abrupt junction varactor are also available, and, as described below, these devices are characterized at cryogenic temperature. Metal-Isolator-Metal (MIM) capacitors with 2, 2.8, 4, and 5.6 fF/μm^2 are also available. Importantly, this technology contains three HBT variants. High-speed NPN, standard NPN, and high voltage NPN. Based

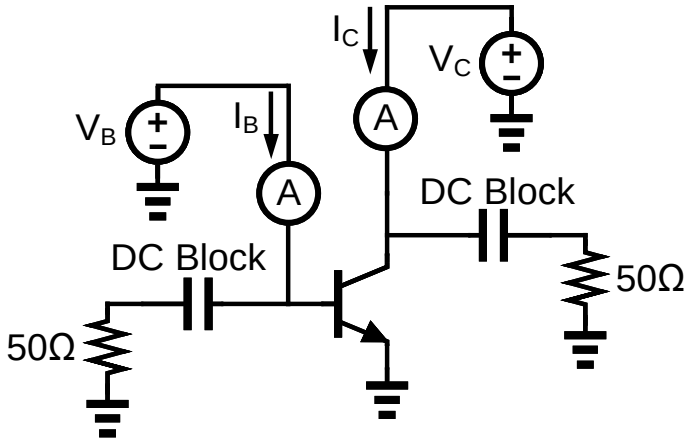


Figure 4.1. DC Gummel measurement setup. Collector and base DC currents are measured regards to V_{BE} while V_{CB} =0. Bias tee is used in the measurements.

on the foundry information, f_t for the high-speed one is higher than the other two SiGe HBTs (>300 GHz). Of these, the high speed variant is most appropriate for cryogenic operation and is characterized and used in this work.

4.1.1 Gummel Measurement of SiGe HBT

Gummel measurements can be used to evaluate g_m and β, and hence provide initial indications as to the noise performance of a given technology. This measurement is done for this technology at physical temperature of 7 K and 300 K. Through this measurement, β_{DC}, extrinsic transconductnace (G_{M}), as well as r_{e} are evaluated.

The Gummel measurement setup is shown in Fig. 4.1. Two DC voltage sources are used to sweep the base and collector voltages while V_{CB} is constant. Example Gummel curves for a $0.09\times20\times1\,\mu\mathrm{m}^2$ SBC18H5 transistor biased at both 7 and 300 K appear in Fig. 4.2. For these curves, V_{CB} was set to 0 V.

As shown, the base current density dropped by more than a factor of 100 with cryogenic cooling. Also, in Fig. 4.2(b), DC current gain (β_{DC}) plotted as a function of collector current density (J_{C}). The β_{DC} improvement between 300 K and 7 K is more than a factor of 10 and maximum β_{DC} can reach to 50,000.

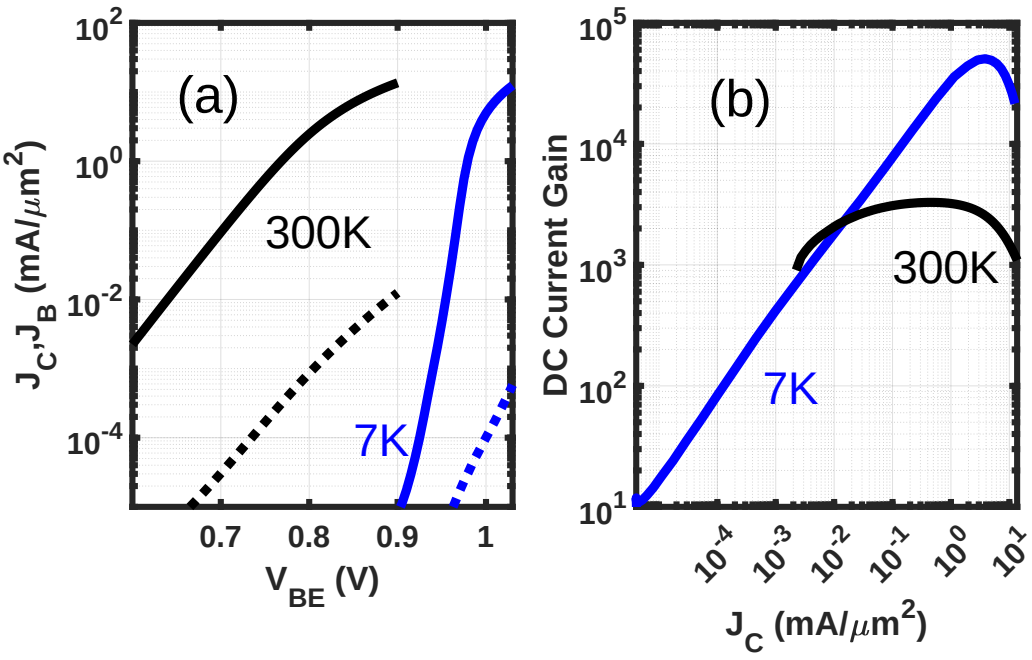


Figure 4.2. DC Gummel measurement results of SiGe HBT of SBC18H5 process. (a) Collector (solid lines) and base (dotted lines) current densities regards to V_{BE} for room (black lines) and cryogenic (blue lines) temperatures. (b) DC current gain (β_{DC}) of SiGe HBT for room (black line) and cryogenic (blue line) temperatures.

4.1.2 RF Measurement and $f_t/f_{\max}$ Plots

Other important parameters to evaluate cryogenic RF and noise performance of SiGe HBTs for LNA design are f_t and $f_{\max}$.

After measuring scattering parameters for a wide range of collector current densities, to obtain the $f_t/f_{\max}$ plots, first, de-embedding of the test structure wiring and pads (described in Appendix A) is required. Then f_t can be obtained by extrapolating the ac current gain from the below equation:

$$h_{21} = \frac{Y_{21}}{Y_{11}} = 1, \tag{4.1}$$

h_{21} rolls off with 20 dB per decade and that f_t can be extrapolated at a given frequency as $h_{21} \times f$.

Also, $f_{\max}$ can be found by extrapolating unilateral gain, defined as [60]:

$$U = \frac{|Y_{21} - Y_{12}|^2}{4(\mathbb{R}\{Y_{11}\}\mathbb{R}\{Y_{22}\} - \mathbb{R}\{Y_{12}\}\mathbb{R}\{Y_{21}\})}, \tag{4.2}$$

where Y_{ij} are Y-parameters converted from measured scattering parameters after de-embedding.

Measured cryogenic f_t and $f_{\max}$ of the SiGe HBT of SBC18H5 are shown in Fig. 4.3. The maximum of f_t and $f_{\max}$ are 360 and 340 GHz at 7 K ambient temperature while $J_C \approx$12–15 mA/μm^2.

4.1.3 Cryogenic Model Parameter Extraction

To simulate the cryogenic LNA and noise performance of the HBT, cryogenic small-signal model including the noise sources, described in the previous chapter (Fig. 3.8), are created. Then, each model parameter can be extracted from specific cryogenic DC and/or RF measurements. This model is done for a wide range of current densities (typically wider than 0.1–10 mA/μm^2). In this section, the parameter

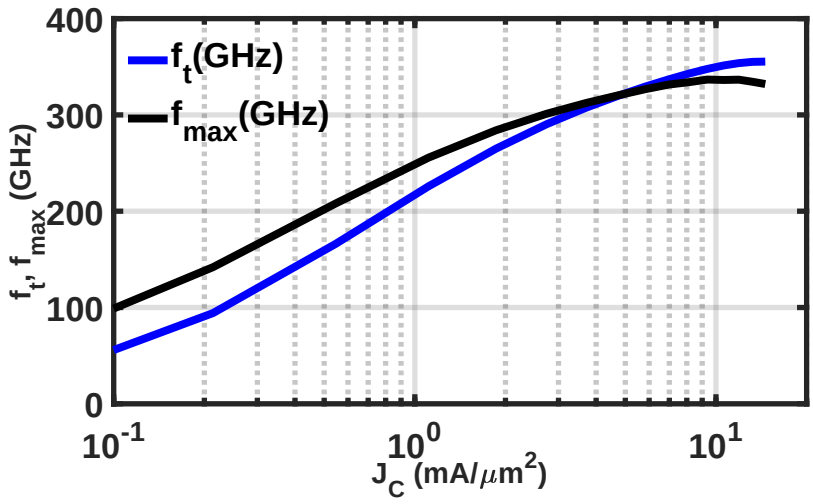


Figure 4.3. f_t (blue) and $f_{\max}$ (black) measurement results of SiGe HBT of SBC18H5 process at 7 K ambient temperature regards to collector current density. The measured transistor size is $0.09\times20\times1\,\mu\text{m}^2$. V_{CE} =0.7 V while V_{CE} is swept.

extraction procedure and the related test setup are briefly described are described briefly.

4.1.3.1 r_e and r_c Extraction

There are different methods to extract r_e and r_c parameters [18]. In this work, the open-collector method are used for the extraction. The measurement setup is shown in Fig. 4.4. Two DC current sources are used to provide base and collector biases. The base current source is swept from a low current until $\sim$20 mA/μm^2 while the collector current is held constant and the collector voltage is measured. A sample of these measurement results is shown in Fig. 4.5. It can be shown that r_e can be estimated as [18]:

$$\left.\frac{dV_{\text{C}}}{dI_{\text{B}}}\right|_{I_{\text{C}}=0} \approx r_e + \frac{V_{\text{T}}}{I_{\text{B}}}(n_c - n_{br}), \tag{4.3}$$

Therefore, by taking derivative of the curve in Fig. 4.5 ($I_{\text{C}} = 0$), it can be obtained the emitter resistance. It is obtained r_e =2.9 $\Omega.\mu$m^2 at 7 K ambient temperature. It is assumed this resistor is bias independent. Also, for this measurement, DC cable

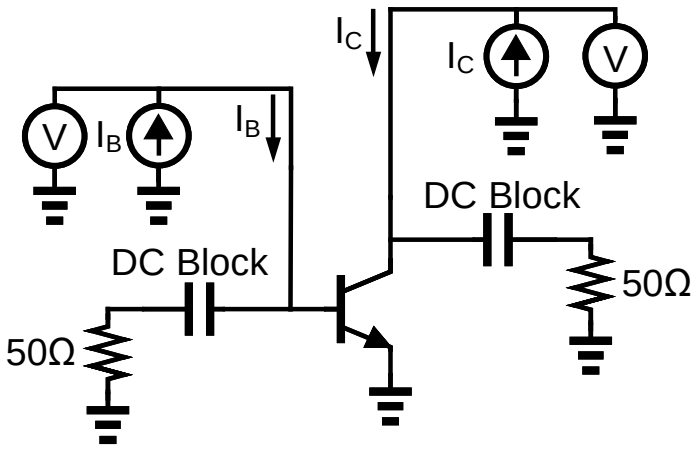


Figure 4.4. Open-collector measurement setup for r_e and r_c parameters extraction. I_{B} is swept in wide range for different values of I_{B}.

resistances should be de-embedded. The details of the de-embedding are described in the Appendix B.

The open-collector measurement was also used to obtain the collector parasitic resistor (r_c). The resistor can be approximated as [18]:

$$\frac{dV_{\mathrm{C}}}{dI_{\mathrm{C}}} \approx r_c + r_e + \frac{n_c V_{\mathrm{T}}}{I_{\mathrm{B}} + I_{\mathrm{C}}}, \tag{4.4}$$

For this process, r_c =5.4 $\Omega.\mu\mathrm{m}^2$ at 7 K ambient temperature, and it is also assumed to be bias independent.

4.1.3.2 C_{CB} and C_{CS} extraction

Cold bias measurements were used to determine C_{CB} and C_{CS}. The base voltage is kept at zero for this measurement, and collector voltage is swept in the range of 0.3–0.7 V. Then scattering parameters of the SiGe HBT are measured with a commercial probestation and Vector Network Analyzer (VNA). The small-signal model of SiGe HBT at the off-bias region is shown in Fig. 4.6. It can be shown that C_{CB} and C_{CS} can be calculated as [18]:

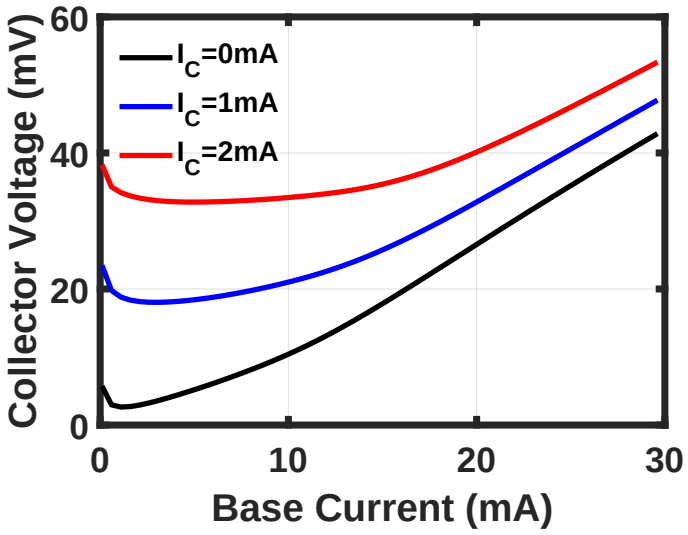


Figure 4.5. Open-collector sample cryogenic measurement results. Collector voltage is swept regards to base current for different collector currents.

$$C_{\mathrm{CB}} = -\lim_{\omega \to 0} \frac{Im\{Y_{12,\mathrm{off}}\}}{\omega}, \tag{4.5}$$

$$C_{\mathrm{CS}} = \lim_{\omega \to 0} \frac{Im\{Y_{12,\mathrm{off}} + Y_{22,\mathrm{off}}\}}{\omega}, \tag{4.6}$$

where Y_{ij} are the converted Y-parameters of the measured transistor. The extracted C_{CB} and C_{CS} versus to V_{CE} is plotted for this process in Fig. 4.7. The average of cryogenic parasitic capacitor density for C_{CB} and C_{CS} are 26.3 and 6 $fF/\mu\mathrm{m}^2$, respectively. It is important to be noted that these capacitors are junction capacitors. So, for cryogenic model creation, those plots should be fitted on $C_{\mathrm{CB,S}} = \frac{C_{\mathrm{CB_0,S_0}}}{(1+V_{\mathrm{CB,S}}/V_{\mathrm{CB_0,S_0}})^m_{cb,s}}$ equation. This has done this by curve fitting functions of Matlab software.The parameters of the equation cannot be obtained for C_{CB} because of the collector-base bias range in the off-bias measurement. Therefore, active bias measurement is used to extract the capacitor in the practical bias voltage range. However, off-bias measurement is used to verify the extracted collector-base capacitor from active bias measurement is not out of the range.

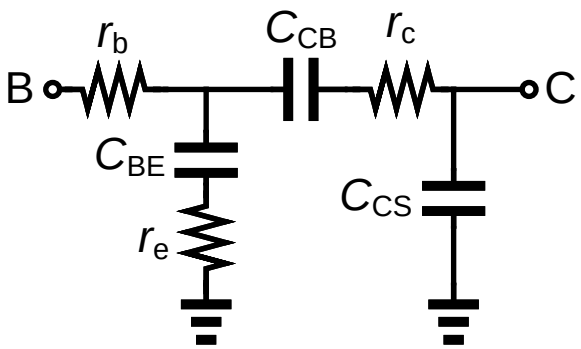


Figure 4.6. Small-signal model of SiGe HBT at off-bias state. This model is used to extract C_{CB} and C_{CS} parameters.

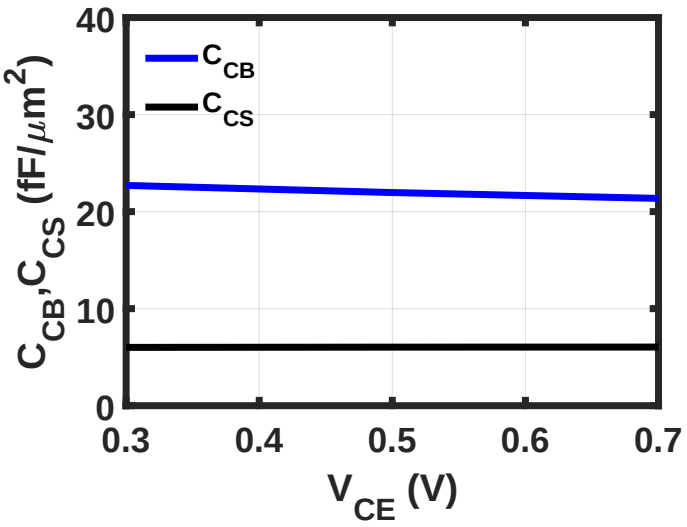


Figure 4.7. Extracted cryogenic (7 K) C_{CB} and C_{CS} regards to collector-emitter voltage while V_{BE}=0 obtained from off-bias measurement. The measured device size is $0.09\times20\times1\,\mu\mathrm{m}^2$.

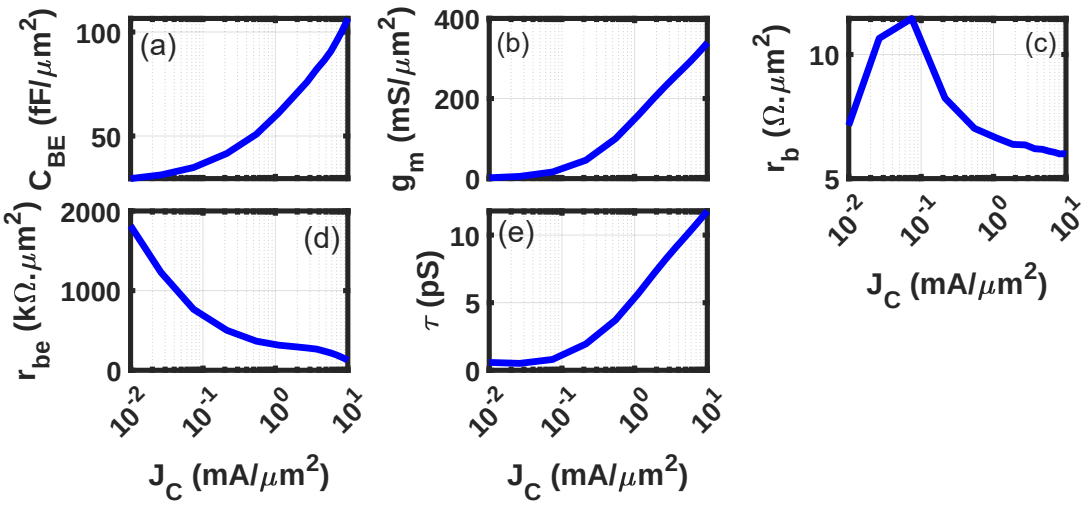


Figure 4.8. Cryogenic (T_a=7 K) small-signal model parameters extraction from active sweep measurement. (a) C_{BE}, (b) g_m, (c) r_b, (d) r_{be}, and (e) τ regards to collector current density while V_{CE}=0.7 V. The measured device size is 0.09×20×1 μm^2. Extracted τ is greater than be anticipated for this process ($\tau \approx C_{be}/g_m$). It might be due to a measurement error.

4.1.3.3 g_m, r_b, C_{BE}, r_{be}, and τ extraction

After de embedding the small-signal model with the extracted parameters which were obtained from previous sections, the rest of the parameters can be extracted by the method described in [97]. For the active sweep measurement, the base voltage of SiGe HBT is swept while it is in the active forward region. Thus, the extraction is done for a wide range of current densities (0.01–10 mA/μm^2). Also, this measurement is done for three different V_{CE} voltages (0.3, 0.5, and 0.7 V). After extracting all small-signal model parameters, each parameter with a polynomial function are fitted in Matlab and imported the acquired functions into AWR software for cryogenic simulations. The inputs of the polynomial functions are collector current density and device emitter area, and the outputs are small-signal model parameters. Finally, shot noise sources of collector and base (without correlation factor) are added to the model. In the next section, a summary of cryogenic simulation results of the modeled SiGe HBT will be presented.

4.1.4 Cryogenic Simulation Results of the SiGe HBT

Since the modeled SiGe HBT was going to be used for the cryogenic LNA, essential noise specifications are summarized and simulated based on the created cryogenic model to evaluate noise performance.

The most important parameter is the minimum noise temperature ($T_{\min}$) of the device. It can be shown that $T_{\min}$ of the SiGe HBT can be approximated as [18]:

$$T_{\min} \approx T_a n_c \sqrt{\frac{1}{\beta_{\mathrm{DC}}}(1+2\frac{g_m(r_b+r_e)}{n_c}) + 2\frac{g_m(r_b+r_e)}{n_c}(\frac{f}{f_t})^2}, \tag{4.7}$$

where $n_c = I_{\mathrm{C}}/g_m V_{\mathrm{T}}$ is the collector current ideality factor and V_{T} is the thermal voltage. The simulated cryogenic $T_{\min}$ of the SBC18H5 SiGe HBT at 16 K temperature is plotted in Fig. 4.9. As shown, the optimum current density for this device is around $\sim$1 mA/μm^2, and the minimum achievable noise temperature at 1, 4, and 7 GHz is 0.5, 1, and 1.7 K, respectively. The reason $T_{\min}$ is simulated for 16 K temperature. This is the minimum available temperature of cryostat was available the lab and it was calibrated for noise measurement.

Another parameter that is critical for noise performance evaluation is the optimum noise impedance (Z_{opt}). This parameter directly affects the complexity of the input matching network of the LNA and its power consumption. Another parameter, noise resistance (R_n), shows how sensitive the device is to the source impedance. In other words, if the input matching network is not ideal, how much it affects the noise performance of the LNA. These parameters can be written as [18]:

$$R_{\mathrm{opt}} \approx \frac{\beta_{\mathrm{DC}}}{g_m(1+\beta_{\mathrm{DC}}(f/f_t)^2)} \sqrt{\frac{1}{\beta_{\mathrm{DC}}}(1+2\frac{g_b(r_b+r_e)}{n_c}) + 2\frac{g_b(r_b+r_e)}{n_c}(\frac{f}{f_t})^2}, \tag{4.8}$$

$$X_{\mathrm{opt}} \approx \frac{\beta_{\mathrm{DC}}}{g_m}\frac{f/f_t}{1+\beta_{\mathrm{DC}}(f/f_t)^2}, \tag{4.9}$$

$$R_n \approx \frac{n_c}{2g_m}\frac{T_{\mathrm{a}}}{T_0}(1+2\frac{g_m(r_b+r_e)}{n_c}), \tag{4.10}$$

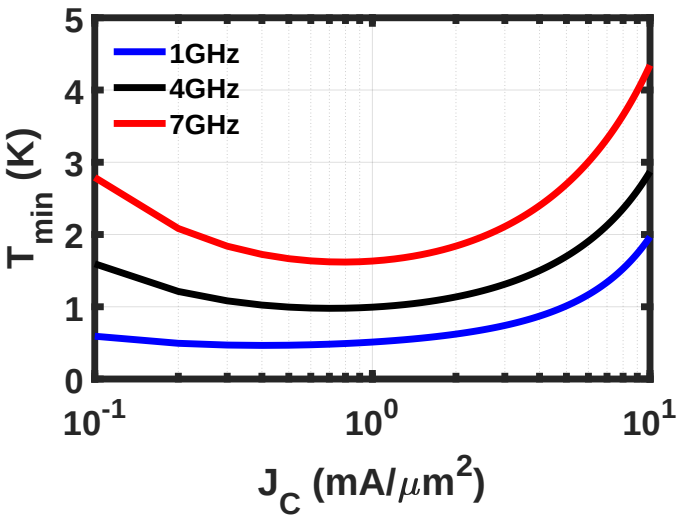


Figure 4.9. Simulated cryogenic (16 K) $T_{\min}$ of SBC18H5 SiGe HBT regards to current density when V_{CE}=0.7 V.

The simulated cryogenic R_{opt}, X_{opt}, and R_n are plotted versus frequency while V_{CE}=0.7 V, J_{C}=1 mA/μm^2, and the transistor size is 1×20×0.09 μm^2. As shown, the optimum noise impedance is higher than 50 Ω, particularly for low frequencies. That is common in cryogenic temperature and it is because of the high β_{DC} of the SiGe HBT at cryogenic temperatures. Larger transistors should be used to decrease R_{opt}, which causes higher power consumption and higher X_{opt}. This trade-off is discussed in the subsequent chapters of the dissertation.

4.2 IHP Microelectronics-SG13G2

4.2.1 Technology Description

As part of a collaboration with IHP, a set of devices from the IHP SG13G2 130-nm BiCMOS technology platform are characterized. Two flavors of devices were provided to us. First, devices from the standard SG13G2 technology platform. Second, devices that were optimized for low-noise cryogenic operation. At room temperature, these

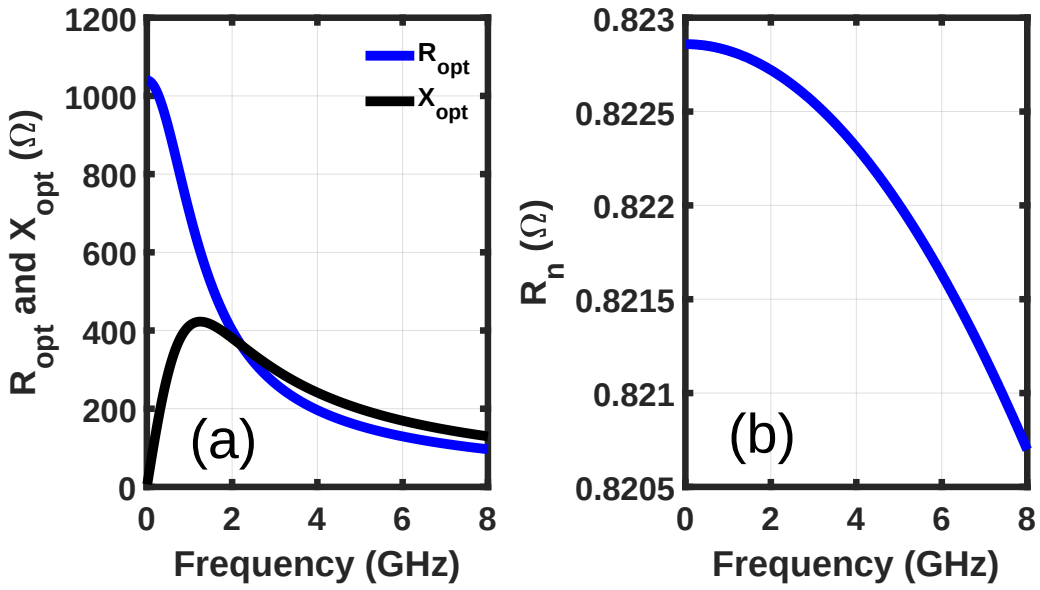


Figure 4.10. Simulated cryogenic (16 K) (a) R_{opt} (blue line) and X_{opt} (black line) and (b) R_n of SiGe HBT regards to frequency when V_{CE}=0.7 V and J_{C}=1 mA/μm^2. Transistor size is 1×20×0.09 μm^2.

devices demonstrate peak f_{t} and f_{max} vaules of 350 GHz and 450 GHz at a current density of 20 mA/μm^2 for the standard HBT.

In comparison with the devices fabricated in the standard SG13G2 process, the optimized transistors featured modified the doping profile of the base and emitter and Ge profile of the SiGe layer. An schematic of the modification is shown in Fig. 4.11(b). This optimization targets improved cryogenic β_{DC}, with the goal of improving the low frequency limit of T_{min}:

$$T_{\text{min,LF}} \approx \frac{qI_{\text{C}}}{kg_m}\frac{1}{\sqrt{\beta_{\text{DC}}}}, \tag{4.11}$$

This approximation of T_{min} is more valid at cryogenic because the added thermal noise from r_e and r_b is less significant.

A higher Ge profile at the base provides a larger collector current by reducing the potential barrier height for electron tunneling, as shown in Fig. 4.11(a). Moreover,

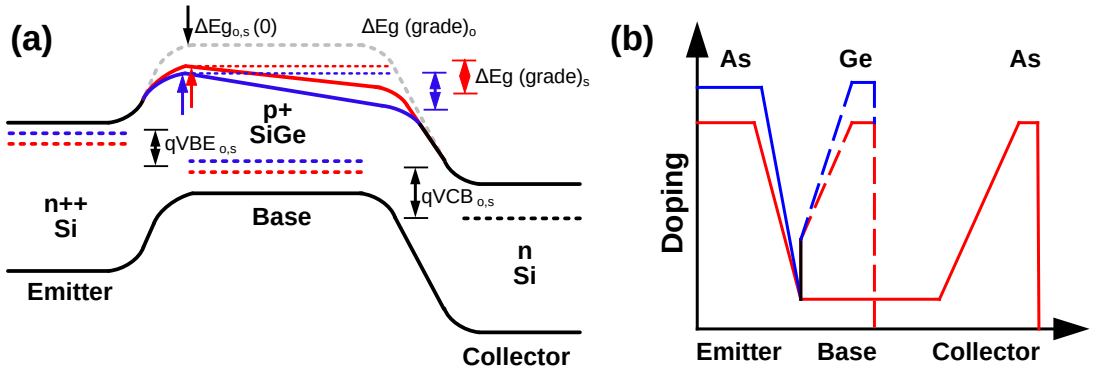


Figure 4.11. (a) Energy band diagram (blue: optimized HBT and red: standard HBT) and (b) Doping structure of standard and optimized HBT devices.

increasing As in the emitter results in reducing the emitter parasitic resistance, which improves HBT extrinsic transconductance (G_{M}) at high current densities.

4.2.2 Cryogenic Characterization and Comparison

The DC and RF performance of standard and optimized SiGe HBT are measured and compared at 7 K. The measurement is carried-out for three different transistors for each type of HBT to make sure chip-to-chip variation is negligible. The de-embedding process, including test structure and DC resistors of the measurement setup, is explained in the Appendix A and B.

The Gummel measurement results for both standard and optimized HBTs at room and cryogenic temperatures are plotted in Fig. 4.12. As shown, the cryogenic DC current gain of the optimized device improved by more than a factor of 10 in comparison to the standard device (Fig. 4.12(b) and (e)). The maximum cryogenic β for standard and optimized devices is 2000 and 20000, respectively. Also, f_t and $f_{\max}$ plots are shown in Fig. 4.12(c) and (f). The peak of cryogenic f_t and $f_{\max}$ are 480 and 620 GHz, respectively. The high cryogenic AC and DC current gain is indicative of excellent cryogenic noise performance. Moreover, the chip-to-chip variation looks small along three measured HBTs.

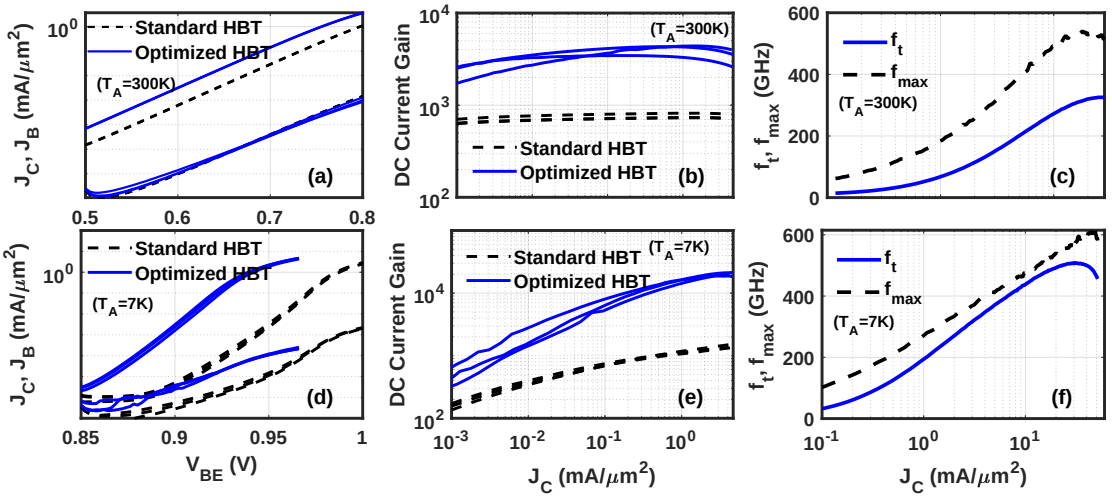


Figure 4.12. (a) and (d) Room (T_a =300 K) and cryogenic (T_a =7 K) collector and base current densities regards to base-emitter voltage of standard (dashed black lines) and optimized (solid blue lines) of SiGe HBT coming from Gummel measurement. (b) and (e) Room (T_a =300 K) and cryogenic (T_a =7 K) DC current gain of standard (dashed black lines) and optimized (solid blue lines) of SiGe HBT coming from Gummel measurement. f_t (solid blue) and f_{max} (dashed black) of (c) standard HBT and (f) optimized HBT at Room (T_a =300 K) and cryogenic (T_a =7 K) temperatures regard to collector current density coming from active sweep measurement while V_{CE} =0.7 V. Three different samples are measured for each type of transistor.

Cryogenic approximated $T_{min,LF}$ regards to current density is plotted for both HBTs based on the approximated equation mentioned above. The results are shown in Fig. 4.13. The minimum of $T_{min,LF}$ for standard and optimized transistors is 2.2 and 0.9 K, respectively. Also, the current density, which minimum of $T_{min,LF}$ occurs, is around 0.3 mA/μm^2, which is ideal for low-power design.

4.2.3 Small-signal Model Parameters Extraction and Comparison

Small-signal noise models were extracted using the procedure described in previous section. Based on the parameters and mentioned curve fitting, the cryogenic models are created for AWR simulations in a wide range of current density (0.01–20 mA/μm^2) and frequency (0.01–10 GHz for noise simulations and 0.01–40 GHz for s-parameters simulations). All data were acquired using a commercial cryogenic probe station,

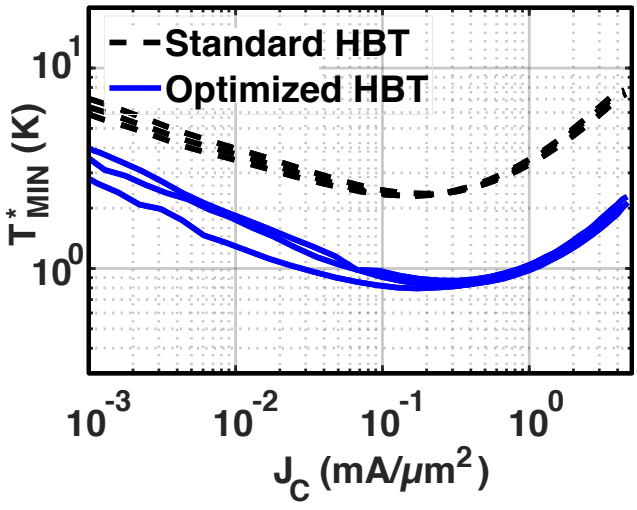


Figure 4.13. Room and cryogenic (7 K) minimum noise temperature regards to current density for both standard (dashed black lines) and optimized (solid blue lines) HBTs. Three different samples are measured for each type of transistor.

Table 4.1. Model Parameters at 7 K. Units: Current denisty–mA/μm^2, Area–μm^2, Res.–$\Omega \cdot \mu$m^2, Cap.–fF/μm^2, Transcond.–mS/μm^2, Delay–ps

Process	J_C	Emitter Area	R_B	R_E	R_C	C_{CB}	C_{CS}	C_{BE}	g_m	τ	β	r_{be}
IHP (SG13G2, Optimized)	0.51	4.56	2.3	2.8	5.2	14.9	4.4	37.1	71.2	0.3	1.7e4	24e4
IHP (SG13G2, Standard)	0.51	4.56	5.9	3.9	4.8	14.1	2.2	46.8	76.7	0.3	1.5e3	20e3

which permitted on-wafer measurements at a physical temperature of 7 K. As the transport properties of SiGe HBTs change little below 20 K, these models should be sufficient to predict the noise performance at temperatures below 20 K.

The small-signal parameters of HBTs are summarized in Table 4.1. While transconductance (g_m) and collector current density (J_C) are similar for both of the process variants, the DC current gain (β) of the optimized device is improved by a bit more than a factor of 10. The parasitic base and emitter resistances (r_b and r_e) decreased, improving noise performance, particularly in high current density design (because of drop voltage decreases on emitter).

The cryogenic models of SiGe HBT are created based on the extracted parameters, and simulation results are shown for T_{min} at 5 GHz at Fig. 4.14. The minimum of T_{min}

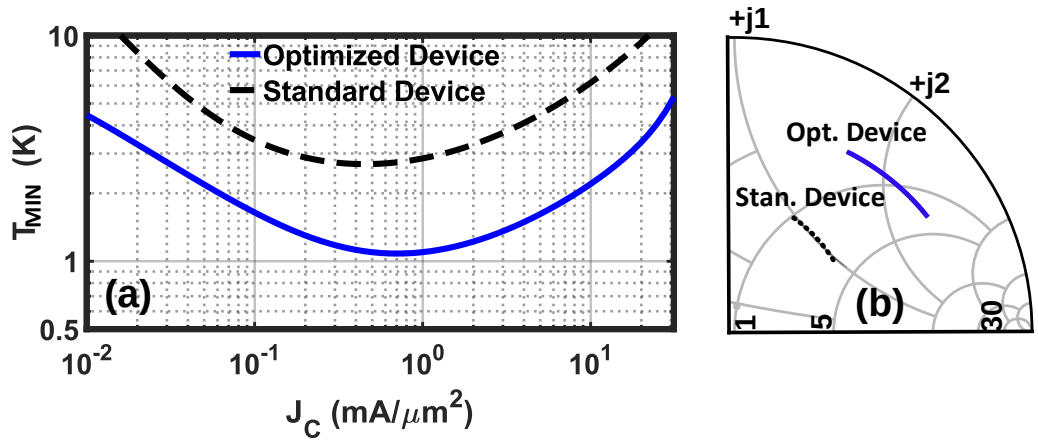


Figure 4.14. Modeled noise parameters of the optimized (blue) and standard (dashed black) HBTs at 5 GHz: (a) $T_{\min}$ and (b) Γ_{opt} (4–8 GHz).

is 1.2 and 2.7 K for the optimized and standard HBTs, respectively. For both devices, the optimum collector current density is around 0.5-1 mA/μm^2. Please note that these simulation results are different from Fig. 4.13 and involve all model parameters, including frequency. However, the plots are consistent with the $T_{\min}$ plot coming from the approximated equation. The optimum reflection coefficient (Γ_{opt}) of both types of HBTs is plotted in Fig. 4.14(b). The frequency range of the simulation is 4-8 GHz and optimum current densities are selected for each device. The optimum noise impedance of the standard HBT is nearer to 50 Ω because of the lower β. Moreover, the real and imaginary parts of optimum noise impedance are plotted at 5 GHz as a function of current density in Fig. 4.15; these results are consistent with expectation. In summary, the optimized device noise performance is improved significantly, and it requires scaling of transistor size. All in all, the optimized HBT of SG13G2 looks promising for low-noise and low-power cryogenic LNA design.

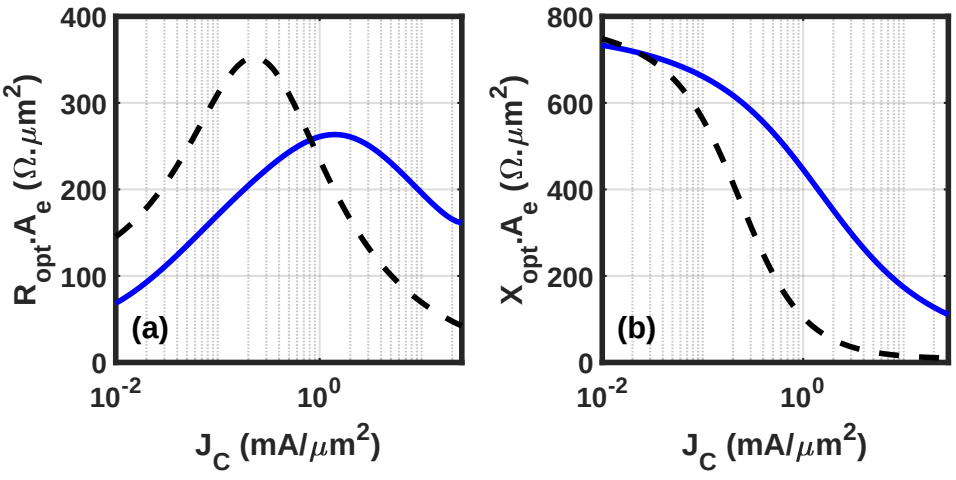


Figure 4.15. Modeled noise parameters of the optimized (blue) and standard (dashed black) HBTs at 5 GHz and regards to collector current density: (a) $R_{\text{opt}} \times A_{\text{E}}$ and (b) $X_{\text{opt}} \times A_{\text{E}}$.

4.3 Global Foundries-SG03

The last technology characterized at cryogenic temperatures in this thesis is an experimental variant of the SG03 Global Foundries SG03 BiCMOS process technology which was tuned for high dc current gain. The results presented here were enabled through a collaboration in which Global Foundries provided an 8 inch wafer from this experimental process variant. The peak of f_t and f_{max} of these HBTs at room temperature is 300 and 380 GHz, respectively. Based on the information provided by Global Foundries, the normal HBT (0.12×2×1 HP CBEBC) from this technology platform has a peak dc current gain of 560; the peak room temperature dc current gain of the samples provided by the foundry was 6300.

The RF and DC characteristics of the HBT from the high-β wafer at 300 and 7 K temperatures are measured using the same experimental setups described above. The results of the Gummel measurement are shown in Fig. 4.16. The peak DC current gain is 5000 and 30000 for room and cryogenic temperatures, respectively. Such high dc

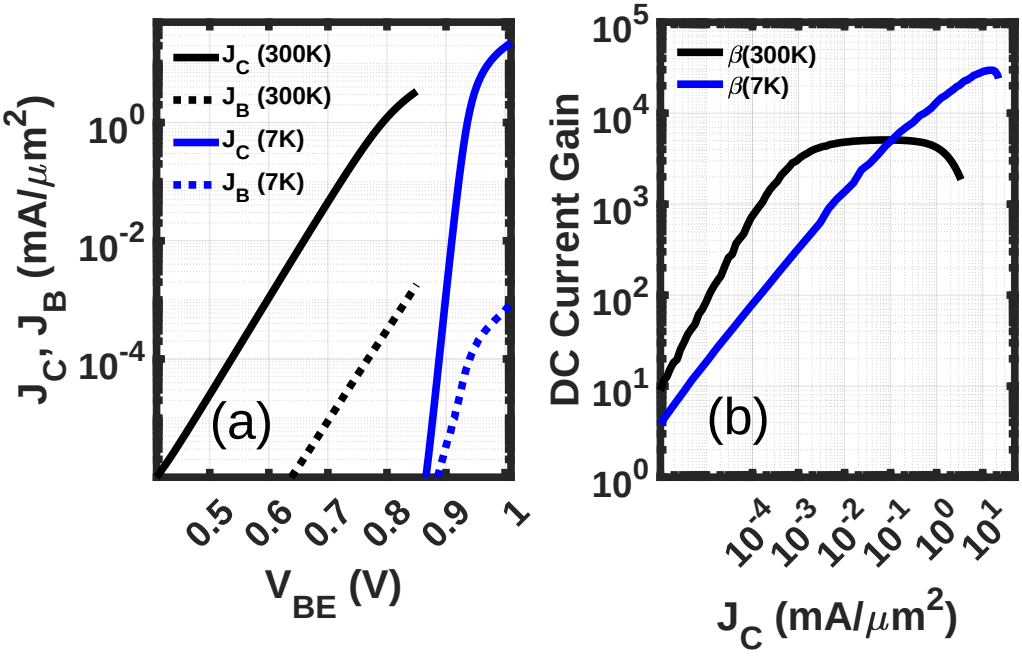


Figure 4.16. Room (300 K, black lines) and cryogenic (7 K, blue lines) Gummel measurement of optimized HBT from SG03 BiCMOS technology. (a) Base (dashed lines) and collector (solid lines) current densities regards to base-emitter voltage and (b) DC current gain (β) regards to collector current density. The sample HBT size is $0.12\times12\times1\,\mu\text{m}^2$ with CBEBC layout structure.

current gain is promising for the implementation of low-noise cryogenic LNAs in this technology. However, the maximum DC current occurs at $J_\text{C} \approx 15\,\text{mA}/\mu\text{m}^2$, which is well into the high-injection regime and is not an ideal bias for cryogenic LNAs both due to the high power consumption and increased noise compared to the more typical bias of $<1\,\text{mA}/\mu\text{m}^2$. Nevertheless, β_DC remains high over a wide range of current densities, which motivated us to measure the RF performance of these devices at cryogenic temperatures.

To verify the HBT cryogenic performance and study chip-to-chip variation, the Gummel measurement for different HBT sizes and from different locations across the 8 inch wafer are repeated. The DC current gain of these devices is plotted in Fig. 4.17.

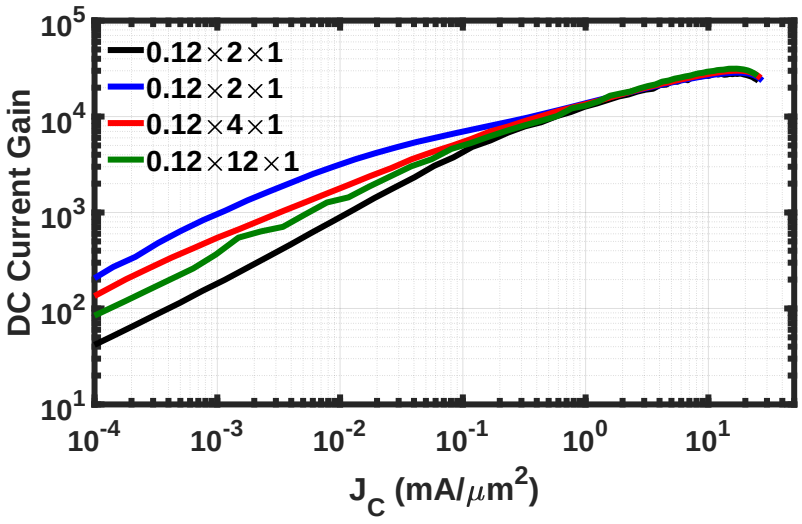


Figure 4.17. cryogenic (7 K) DC current gain regards to collector current density for different HBT sizes in different locations of the wafer. The plots are based on Gummel measurement setup.

As shown, the maximum β is in the range of 26000–32000 and remains above 4,000 for current densities above 0.1 mA/μm^2.

Next, the cryogenic RF performance of this technology are characterized. The intrinsic values of f_t and $f_{\max}$ as a function of collector current density while V_{CE} =0.7 V are plotted in Fig. 4.18. The maximum values of f_t and $f_{\max}$ are 410 and 580 GHz, respectively.

Finally, to evaluate the cryogenic noise performance, extraction of small-signal and noise model parameters, with the approach described above, is done for J_{C} in the range of 0.1–20 mA/μm^2. Cryogenic (7 K) $T_{\min}$ simulation results are shown in Fig. 4.19. $T_{\min}$ is plotted as a function of frequency for three practical current densities in Fig. 4.19(a). Based on these simulations, $T_{\min}$ can reach 0.8 K at low frequencies. Also, to find the optimum collector current density of the HBT, the simulated values of $T_{\min}$ have plotted as a function of J_{C} at 4 and 10 GHz in Fig. 4.19(b). The optimum collector current density is in the range of 0.5–1 mA/μm^2.

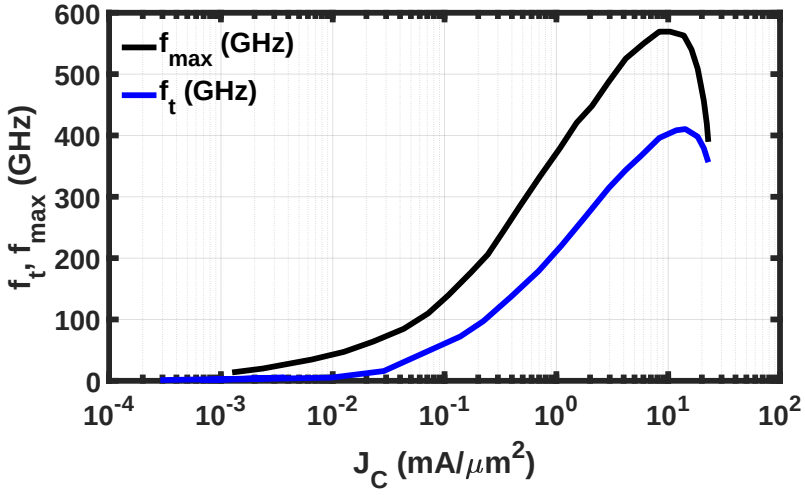


Figure 4.18. cryogenic (7 K) measured f_t and $f_{\max}$ of the HBT regards to current density. The sample HBT size is $0.12\times12\times1\,\mu\text{m}^2$ with CBEBC layout structure. The plot is created based on active-sweep measurement while V_{CE} =0.7 V.

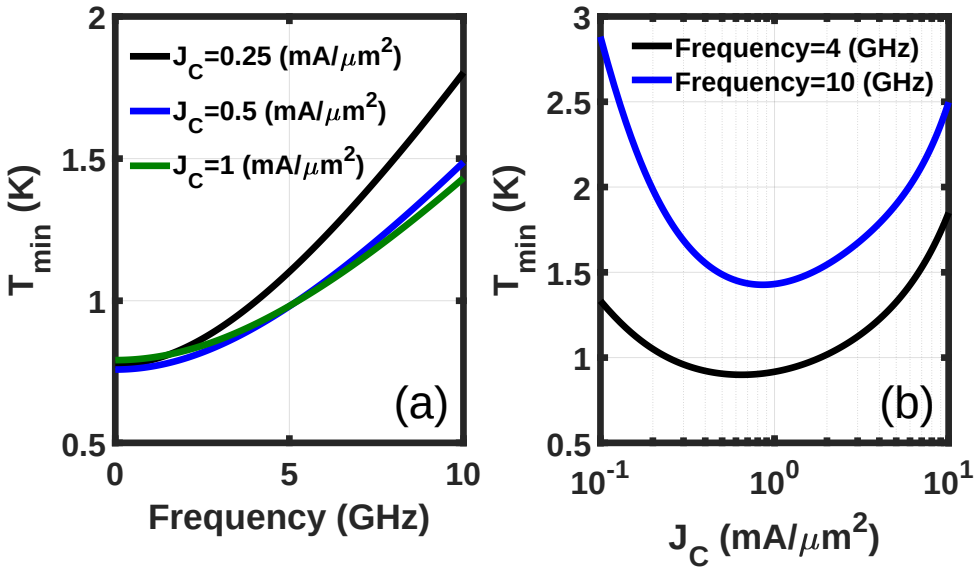


Figure 4.19. cryogenic (7 K) $T_{\min}$ simulations based on created standard small signal model regards to (a) frequency and (b) collector current density. The sample HBT size is $0.12\times12\times1\,\mu\text{m}^2$.

Table 4.2. Summary and comparison of some important cryogenic specifications of HBT in different technologies for LNA design. The ambient temperature is 7 K and frequency of simulated $T_{\min}$ is 4 GHz.

Technology	Fabrication Company	$f_{\mathrm{t,peak}}$ GHz	$f_{\mathrm{max,peak}}$ GHz	$\beta_{\mathrm{DC,peak}}$ -	$J_{\mathrm{C}}\vert_{\beta_{\mathrm{DC,peak}}}$ mA/μm^2	$T_{\min}\vert_{J_{\mathrm{C}}=J_{\mathrm{C,opt}}}$ K
SBC18H5	Tower Semiconductor	360	340	50,000	4	0.8
SG13G2	IHP Microelectronics	480	610	20,000	5	1
SG03	Global Foundries	420	580	30,000	15	0.8

4.4 Summary and Conclusion

HBTs from three state-of-the-art BiCMOS technologies are characterized cryogenically, and small-signal models are created based on the RF and DC measurements. HBT of SG13G2 is particularly optimized for cryogenic noise performance by the foundries. A summary of the measured or modeled results appears in Table 4.2. In general, all three technologies are promising for cryogenic LNA design. However, SBC18H5 provides the highest value of DC current gain while the f_t and $f_{\max}$ are lower than two other processes. On the other hand, the optimum current density of SG03 is higher than the two other processes, which is not ideal for low power design. In the following chapters of the dissertation, several cryogenic LNAs are designed based on the SBC18H5 and SG13G2 processes.

CHAPTER 5

SIGE HBT CRYOGENIC LNAS FOR MKID READOUT

The design and characterization of a low noise amplifier optimized for the readout of microwave kinetic inductance detectors (MKIDs) is described here. These results were previously published in the Transactions of the 2019 International Microwave Symposium [46].

This chapter is first motivated through a description of microwave kinetic inductance detectors and a discussion of the requirements for the low-noise amplifiers employed for the readout of these devices. Then, the design of a two-stage SiGe cryogenic integrated circuit low noise amplifier is presented.

The small-signal and large-signal characteristics of the fabricated amplifier are then measured and explained. It is shown that at a physical temperature of 16 K, the amplifier achieves a gain of greater than 30 dB and an average noise temperature of 3.3 K over the 0.4–1.2 GHz frequency band while dissipating less than 7 mW. Moreover, the wideband compression characteristics are measured. It is found that the amplifier's linearity is sufficient to support frequency domain multiplexed readout of more than 500 detectors.

Moreover, for biasing an array of the LNAs in the system, a servo bias board is designed and implemented. By using this bias board, a single unregulated power supply is sufficient to bias up to 16 LNAs. Finally, system implementation wiring of the LNA array is discussed in the last section of this chapter.

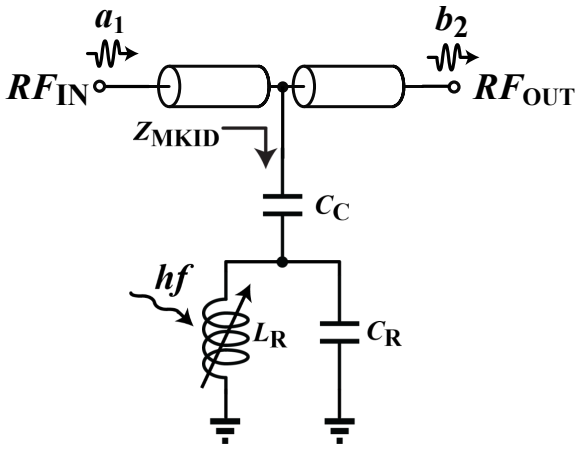


Figure 5.1. Equivalent model of a single MKID, including readout line. The kinetic inductance (L_K) is modulated by photon flux, resulting in a shift in the series resonant frequency of the coupled MKID, as observed from the transmission line.

5.1 Microwave Kinetic Inductance Detector (MKID)

Microwave kinetic inductance detectors (MKIDs) have become popular for use in terahertz direct detection systems due to their low noise effective power (NEP) and favorable scalability [29, 37, 30]. An MKID is a planar device that consists of a superconducting resonator, weakly capacitively coupled to a transmission line, as shown schematically in Fig. 5.1. The resonator is typically realized using thin-film superconducting materials and may be implemented with distributed [29] or lumped-element structures [33]. In either case, an MKID is designed to leverage the dependence of a superconductor's kinetic inductance on the density of Cooper pairs in the material; that is, when the superconducting film absorbs photons with sufficient energy, they break Cooper pairs, thereby modulating the kinetic inductance and leading to a detectable shift in the series resonant frequency of the coupled MKID. The inductance of the MKID (L_{R}) is dominated by kinetic inductance and can be approximated as:

$$L_{\mathrm{R}} \approx L_{\mathrm{K}} = \frac{1}{n_{\mathrm{C}}} \frac{m}{q^2} \frac{l}{A}, \tag{5.1}$$

where n_C is Cooper pair density, m is electron effective mass, q is electron charge, and l and A are the length and cross sectional area of the superconducting film. The resonant frequency of the MKID can be written as:

$$f_0 \approx \frac{1}{2\pi\sqrt{L_K(C_C + C_R)}}, \tag{5.2}$$

where C_C and C_R are the resonator coupling capacitor and parasitic capacitor of the resonator, respectively.

The minimum frequency of a photon that can be detected using this technique is determined by the gap energy of the superconducting film (Δ) and is approximated as:

$$f_{min} \approx \frac{2\Delta}{h} \approx T_C(73.5 \text{ GHz/K}), \tag{5.3}$$

where h is Planck's constant and T_C is the critical temperature of the superconducting film. As such, THz MKIDs typically employ superconducting materials such as Al and TiN, which have critical temperatures in the range of 1–3 K, and the devices are usually cooled to the 100 mK range.

Measured quality factors for MKIDs capacitively coupled to a transmission line are on the order of 15,000 [61], meaning that the fractional frequency range over which any single MKID interacts with the transmission line is well below 0.1%. As the relative value of f_0 can be engineered by varying the relative size of C_C and/or C_R, it is feasible to couple hundreds or even thousands of MKIDs, each with a unique value of $C_C + C_R$, to a single microwave line (see Fig. 5.2). The ability to multiplex hundreds of detectors on a single line makes MKIDs appropriate for use in large focal plane array systems.

As shown in Fig. 5.2, multiple resonators with different resonance frequencies can be capacitively coupled to a single transmission line. Since quality factors of MKID resonators are high (can be reached up to 10,000), thousands of these resonators can be coupled in a reasonable frequency range.

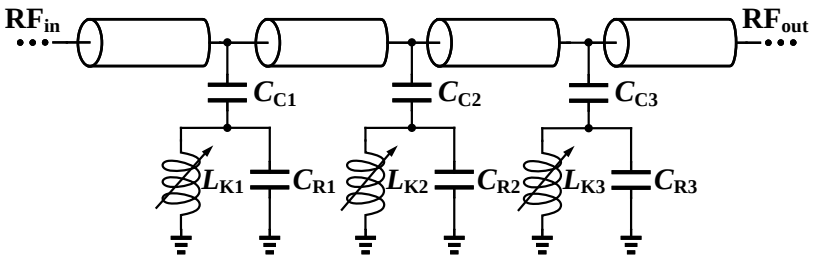


Figure 5.2. Frequency domain multiplexing of MKIDs

Here, LNAs are developed for frequency domain multiplexed readout of the ToLTEC camera, which leverages MKID arrays developed at NIST [9]. There are three independent detector arrays with more than 7718 pixels in the TolTEC camera. The three detector arrays cover bands of 125–170 GHz, 195–245 GHz, and 245–310 GHz respectively.

5.2 MKID Readout System

An overview of the MKID readout system is shown in Fig. 5.3, where a simplified block diagram of one of the 13 readout channels is shown. The readout line is excited by a comb of probe tones generated by an I-Q modulator, with each of the probe tones tuned to the average resonant frequency of one resonator of the MKIDs. As the signals pass through the readout line, the readout tones will be modulated due to power-dependent frequency shifts in the resonant frequency of the associated MKID. After significant amplification by the LNA and a room temperature post amplifier, the amplitude and phase information corresponding to the power absorbed by each MKID is recovered through homodyne detection. Since the information in such a system is carried in the modulation applied to probe tones, SNR is maximized when one uses the strongest possible tones (limited by the power level at which the microwave excitation breaks Cooper pairs [31]).

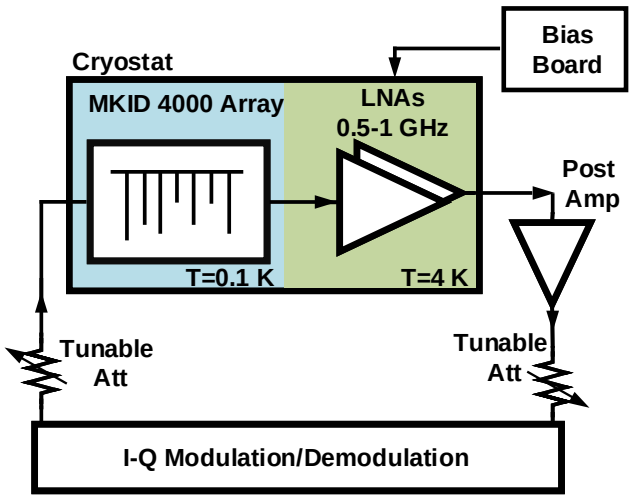


Figure 5.3. Simplified system block diagram of the MKID readout.

Typical readout tones are in the 1 pW range at the detector coupling capacitor and, while the phase of each tone can be randomized, the peak to average ratio of the aggregate waveform used to readout a large MKID array can be well above 10 dB. The cryogenic low noise amplifier (LNA) used for readout must be able to handle such excursions.

Here the requirement of two parts of the ToLTEC readout system is described briefly: Cryogenic LNAs and LNAs array biasing board. The design, implementation, and measurement results of the TolTEC LNA are described in detail in the following sections of this chapter.

5.3 Cryogenic LNA Design Overview and Specifications

The primary considerations that must be taken into account in specifying a cryogenic LNA for MKID readout are (1) the required probe signal power and frequency band,(2) the impact of LNA noise on overall sensitivity, (3) the available power budget, and (4) the system complexity associated with biasing the cryogenic LNAs. In the case of the camera currently under development, the 6,000 pixels will be inter-

faced to using a total of 13 readout lines, each operating in the 0.5–1 GHz frequency range. As such, thirteen amplifiers are required, and a frequency band of 0.4–1.2 GHz is targeted to provide a margin. The number of detectors coupled to each readout line varies from 450 to 601, so the larger number is considered in setting the linearity requirement. Since the detectors are fabricated out of TiN, the power of each probe tone is assumed to be −90 dBm [48], corresponding to a worst case average power of about −62 dBm. Thus, the amplifiers should remain linear with input powers in this range. The 0.1 dB compression point is considered for the linearity specification to ensure LNA linearity does not affect the readout.

Another consideration is noise performance. Assuming the amplifier has high gain (i.e., > 30 dB), its noise contribution will dominate the noise of the overall receiver. It can be shown that the microwave receiver chain contributes a fractional frequency noise of approximately $\sqrt{kT_e/P_{\text{probe}}}/Q_{\text{C}}$ where T_{e} is the LNA input-referred noise temperature, P_{probe} is the microwave probe tone power, and Q_{C} is the coupling quality factor [61]. While the relative impact of this noise depends strongly on the responsivity of the MKID, it is aimed to minimize this effect by realizing an amplifier with a noise temperature below 4 K. Such noise performance has previously been demonstrated using SiGe BiCMOS technologies [23].

The power consumption of each amplifier is less constrained, as the heat-lift of a typical commercial closed-cycle refrigerator operating at 4 K is on the order of 1 W. Nonetheless, in anticipation of larger-scale arrays, A power consumption of less than 7 mW is targeted to keep the aggregate DC power consumption of the 13 amplifiers required to read out the TolTEC detector arrays around 90 mW.

Finally, it is considered the complexity associated with biasing of the amplifier array. The most straightforward approach is to employ self-biasing, which has the advantage that it makes single-supply operation feasible. However, there is a significant mismatch between the voltage required at the base (≈1.05 V at 16 K) and that

required at the collector (≈300 mV at 16 K) of an HBT operated at cryogenic temperatures [63]. As such, this approach is avoided and opted for independent control of each base voltage. To ease the challenge of generating and distributing a large number of bias voltages to the 13 amplifiers, a servo-bias system is designed to maintain constant collector current while operating from a low collector supply voltage. The bias circuitry and implementation are described later in this chapter.

5.4 LNA Design and Implementation

A two-stage SiGe HBT cryogenic LNA was targeted for this application. The LNA is based on ST BiCMOS9MW process. In [14], it is shown that this process is promising for cryogenic noise performance and LNA design. 30 dB gain, lower than 4 K noise temperature, lower than 10 mW power consumption, and higher than 10 dB input/output return loss are targeted for this LNA. Cryogenic simulations are carried out in Microwave office (AWR) design environment. Additionally, room temperature simulations and circuit layout layout is carried-out in Cadence Virtuoso leveraging foundry PDK models and technology information.

The amplifier schematic design is shown in Fig. 5.4. The amplifier is a two-stage common emitter design with inductive emitter degeneration; this topology is selected to minimize the noise temperature. The first stage device size and current density are selected for minimum noise temperature and 50 Ω optimum noise impedance (R_{opt} =50 Ω), and the second stage provides the rest of the required gain. An off-chip second-order LC ladder input matching network is chosen to tune the noise performance of the LNA after fabrication. A 60 Ω resistor is used for the collector of the first stage, which helps the stability of the LNA with power consumption cost. Also, 1 nF wire-bondable off-chip silicon bypass capacitors is placed right beside the chip for stability and low-frequency noise reduction.

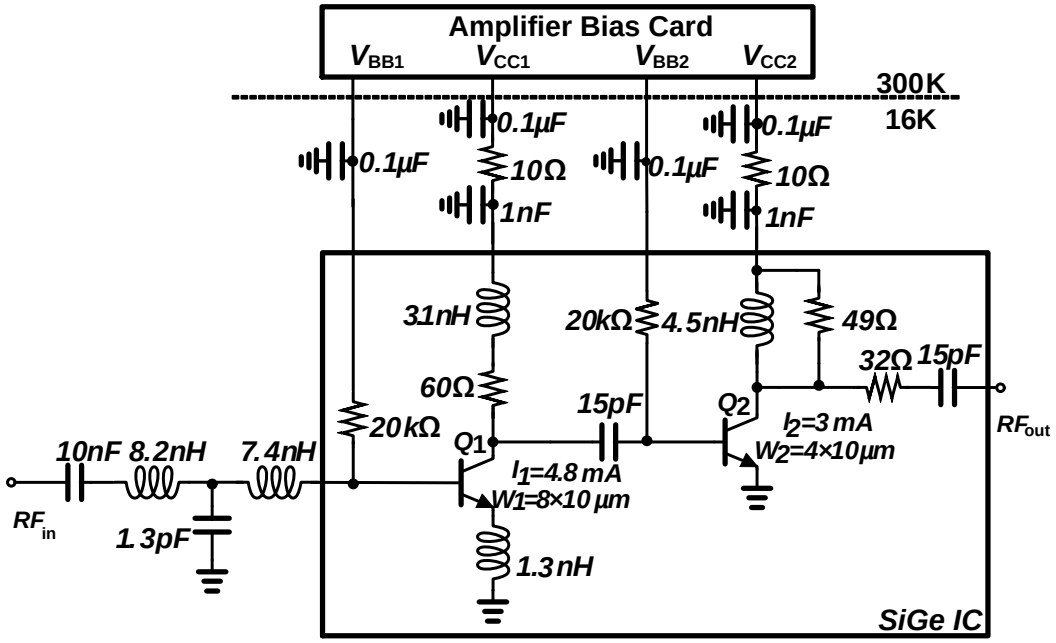


Figure 5.4. Schematic design of cryogenic LNA for MKID array readout including off-chip bypassing components and input matching network. Bias points are related for 16 K measurements.

Table 5.1. Model parameters extracted at a physical temperature of 18 K. W_{E}=0.13 μm, $J_{\mathrm{C1,2}}$=0.46, 0.58 $mA/\mu\mathrm{m}^2$. A standard hybrid-π model topology is used [14].

L_{E}	R_{B}	R_{E}	R_{C}	C_{CB}	C_{CS}	C_{BE}	g_{m}	τ	β
μm	Ω	Ω	Ω	fF	fF	fF	S	pS	-
80	0.75	0.12	0.65	190	60	436	0.4	0.45	4.6e4
40	1.5	0.24	1.3	95	30	232	0.25	0.47	3.9e4

The extracted transistor parameters for both stages at 18 K temperature are shown in Table 5.1. The DC current gain (β) of this process is promising even at low current densities. The chip is integrated inside a custom-designed module for cryogenic noise characterizations, as shown in Fig. 5.5. The chip (Fig. 5.5(a)) dimensions are 1.1×1.2 mm^2 including bondpads. As shown in Fig. 5.5(b), a nano-D 9-pin DC connector is used to supply dc bias to the module. However, DC bondpads are on both the north and south sides of the chip (RF input/output is on the west/east side of the chip). To route the DC bias to one side of the module, a four layer output PCB is used

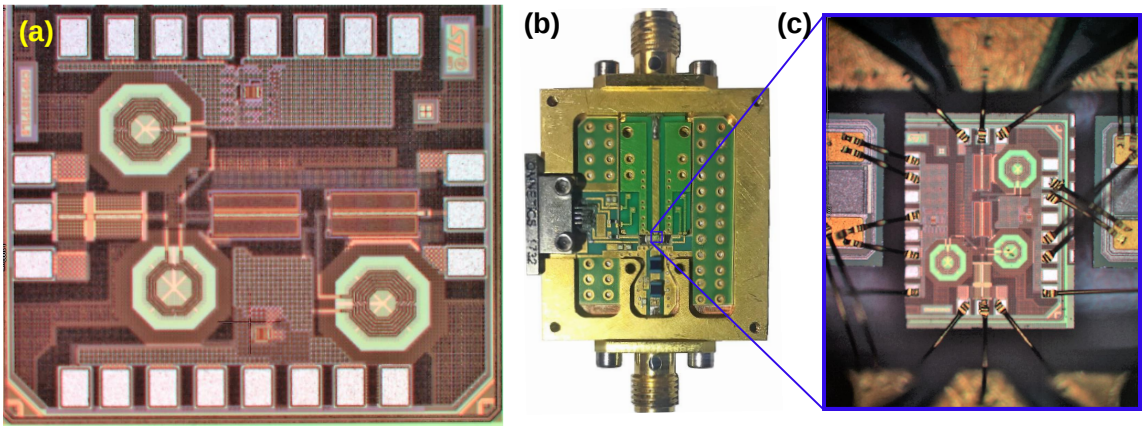


Figure 5.5. (a) Chip photograph, (b) Assembled module, and (c) Wire-bonded chip of cryogenic LNA for MKID array.

and routed the DC bias underneath the output transmission line ground plane. Two off-chip SMD aire-core inductors are selected for the input matching network.

A vertically wire-bondable silicon capacitor is used to complete the LC ladder network. The module is designed in Inventor Professional software, and it is fabricated using oxygen-free high thermal conductivity (OFHC) copper, which is gold plated (type-3, 0.1 mil nickel, 0.03–0.05 mil gold). A standard female SMA connector is used. EM simulations are carried-out to design the transition between the chip and PCB transmission lines (CPW to microstrip transition type). The wire-bonded chip is shown in Fig. 5.5(c). The distance between chip to bypass capacitors and PCBs is minimized to prevent stability.

5.5 Servo Bias Board Design and Implementation

5.5.1 Servo Bias Board Design

SiGe HBT biasing is challenging due to the inherent exponential function of I_C-V_{BE} curve. The sharpness of this curve is increased significantly at cryogenic temperatures (Fig. 4.2), and consequently, sub-mV base bias voltage control is required. High-resolution voltage sources can provide precise control for the base voltage. For this

LNA, 4 voltage sources are required for each LNA (and 52 sources are required for the 13 amplifier array). Moreover, wiring outside of the camera is more complicated with using these sources. To minimize the biasing wiring (outside of the cryostat) of 13 LNAs in the system and prevent requiring so many high-resolution power supplies (typically four supplies are required for a two stages SiGe HBT cryogenic LNA), a servo bias board is designed and populated, capable of biasing up to 8 amplifiers. Two of these servo-bias cards can thus bias the full 13-amplifier array.

The simplified design of the servo bias board for one stage bias is shown in Fig. 5.6. A feedback loop is used to stabilize the collector current. The loop operates as follows. Collector current (I_{C}) is measured and converted to a voltage by R_{sense}=10 Ω. This voltage is then amplified by a variable-gain instrumentation amplifier (IA_1). The amplified voltage (V_{sense}) is then compared with a reference voltage ($V_{\mathrm{ref_B}}$). The difference voltage of V_{sense} and $V_{\mathrm{ref_B}}$ is amplified by another instrumentational amplifier (IA_2), integrated, and applied to the base voltage. The collector current can be written as:

$$I_{\mathrm{C}} = \frac{V_{\mathrm{ref_B}}}{A_{v_1} R_{\mathrm{sense}}} \times \frac{1}{1 + R_{\mathrm{int}} C_{\mathrm{int}} S / A_{v_1} A_{v_2} g_m R_{\mathrm{sense}}}, \tag{5.4}$$

where A_{v_i} are voltage gains of the amplifiers, R_{int}, and C_{int} are integrator resistor and capacitor, respectively, and g_m is the HBT cryogenic transconductance. At steady-state, it can be shown that the DC collector current can be approximated as:

$$I_{\mathrm{C}} \approx \frac{V_{\mathrm{ref_B}}}{A_{v_1} R_{\mathrm{sense}}}, \tag{5.5}$$

As shown above, in the equation, collector current can be precisely controlled by $V_{\mathrm{ref_B}}$.

Please note that the first-order system approximation is valid for DC current analysis and does not capture the stability issue. Since the instrumentational amplifiers have unity-gain bandwidth, there is a trade-off between maximum loop speed and stability for implementing the servo bias loop idea. By increasing the gain of

the instrumentational amplifiers, the loop speed increases, and resolution control of DC current improves. However, it potentially causes higher loop gain and low-frequency instability because of the limited gain-bandwidth of the instrumentational amplifiers. Please note there are three poles in the open-loop transfer function. One low-frequency pole is coming from the integrator and contributes -90∘ phase, and the other two poles (30 kHz for gain of 10) are coming from instrumentational amplifiers. Therefore, the phase margin is zero at 30 kHz, and the magnitude of the open-loop gain should be lower than one before 30 kHz.

Since a high-speed biasing was not required (even below 100 Hz range would be enough for our target), this trade-off did not limit the bias board design. More details of the trade-off is shown in Appendix C.

Added noise of the servo bias to the LNA is another challenge and should be minimized during the design. The main noise contributors are the instrumentational amplifiers and the sensing resistor. There is a $10\,\mu\text{F}\|10\,\text{nF}$ capacitor in each supply node of the bias board. Also 127 nH ferrite bead is used in series with the supplies bypass capacitors. A $1\,\mu$F bypass capacitor is also placed on the DC PCB of the LNA to minimize the added noise of the servo bias. This capacitor causes a lower loop speed (and it helps to stability). However, as mentioned before, minimizing the added noise was a more important factor than loop speed for the servo bias board.

5.5.2 Servo Bias Board Implementation

The detailed circuit design of the servo bias for one stage LNA is shown in Fig. 5.7. Two low-noise and low-power tunable voltage regulators (LT3056) are used to minimize the main power supply's ripple. One of these regulators provides supply voltage for amplifiers and op-amps inside the bias board. The second regulator provides collector voltage for the LNAs.

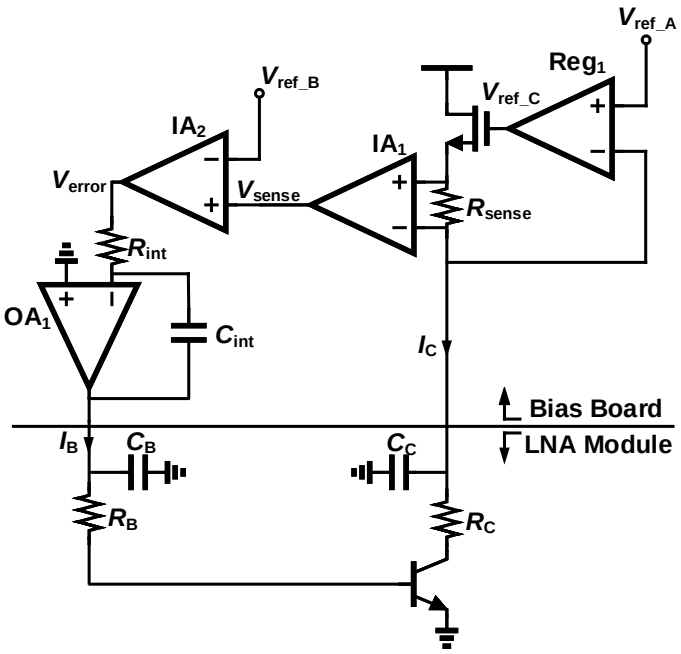


Figure 5.6. Design idea of the servo bias of the one stage LNA. Collector current can be precisely controlled by the reference voltage in the servo loop.

Two gain-programmable, low-power, low-noise instrumentational amplifiers (LT1789-1) are employed to control the collector current precisely with minimum added noise. The reference voltage ($V_{\mathrm{ref_B}}$), supply voltages of the instrumentational amplifiers/op-amp (V_{DD}), and the collector voltage are tunable via three potentiometers. A low-pass filter structure including two parallel capacitors (10 n and 10 μF) and a series ferrite bead (127 nH) are placed on the output of the regulators and supply voltages of the amplifiers and the op-amp to minimize added noise of servo bias to the LNA.

The circuit discussed above is assembled on a four-layer standard FR4 printed circuit board to bias 8 LNAs. Layer 2 and three is used as the ground plane.

The populated board image is shown in Fig. 5.8. As shown, the bias board channel is repeated 16 times to provide biasing for eight LNAs. Two of these boards are enclosed in RF tight packages on two sides of the cryostat. A Micro-D 100-pin connector is used for connecting between the LNAs and the bias boards.

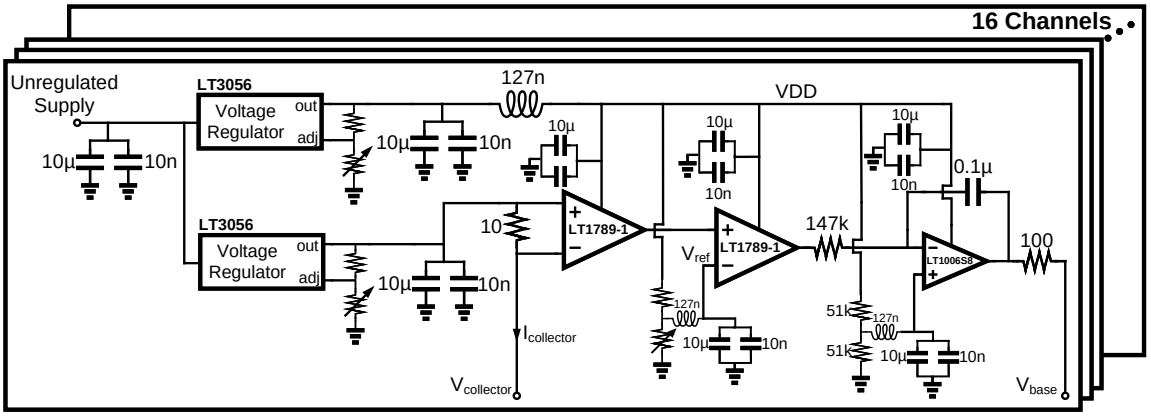


Figure 5.7. Servo bias circuit implementation for biasing one stage of cryogenic LNA. The circuit is copied 16 times to bias up 8 LNAs.

To minimize ground loop issues, an independent ground wire is allocated for each LNA base and collector bias. A 25-pin D-sub connector is used to monitor voltages of some bases an collectors; the 7 V power supply for the bias board is also supplied via this connector.

5.6 Experimental Results and Comparison to Simulations

In this section, cryogenic characterization of the LNA is reported. Since the linearity of the LNA is essential for our specific application, both the small-signal/noise and linearity performance of the circuit are characterized.

5.6.1 Small-signal Measurement Results

After assembly, the amplifier was mounted in a closed-cycle cryostat for characterization at a physical temperature of 16 K. These measurements were carried out in a two-channel cryostat, with one channel used for scattering parameters measurements and the second used for cold attenuator [36] based noise measurements. The amplifier was biased at V_{C1}=0.85 V, I_{C1}=4.8 mA, V_{C2}=0.85 V, and I_{C2}=3 mA ($P_{DC} \approx 6.6$ mW).

Cryogenic noise temperature and scattering parameters of the LNA are characterized at a physical temperature of 16K, and the results are shown in Fig. 5.9. The

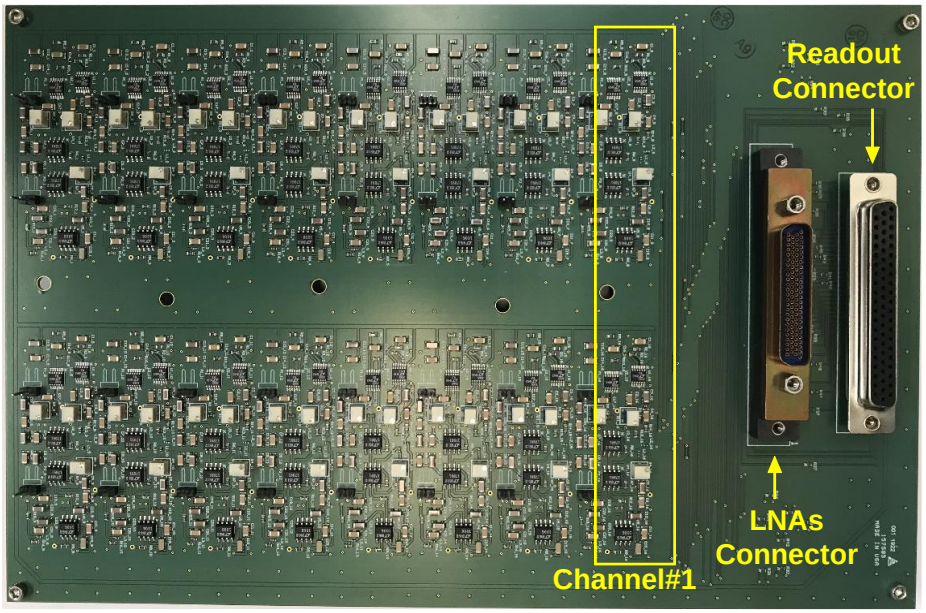


Figure 5.8. Eight channels assembled bias board. Standard 4 layers FR4 board is used. A 100-pins Miro-D connector is selected as cryogenic compatible connector. A 25-pins D-sub connector is selected to monitor base and collector voltages and is providing heater signals of the cryostat.

amplifier achieved 3.3 K average noise temperature, 30 dB average gain, and higher than 7 and 20 dB input and output return loss. Moreover, the excellent agreement observed between model and measurement confirm the accuracy of the cryogenic design models. The measured input and output return losses differ some from simulation, which may be explained by the difference in the reference plane, as the measurement included long coaxial cables within the cryostat. Nonetheless, the measured input and output return losses are believed to be sufficient for this application.

5.6.2 Linearity Performance

The TolTEC camera is comprised of more than 7718 pixels spread between the 125–170 GHz, 195–245 GHz, and 245–310 GHz bands. Since there are 13 readout lines, each operating in the 0.5–1 GHz frequency range is used in the camera, the number of detectors coupled to each readout line varies from 450 to 601, so the

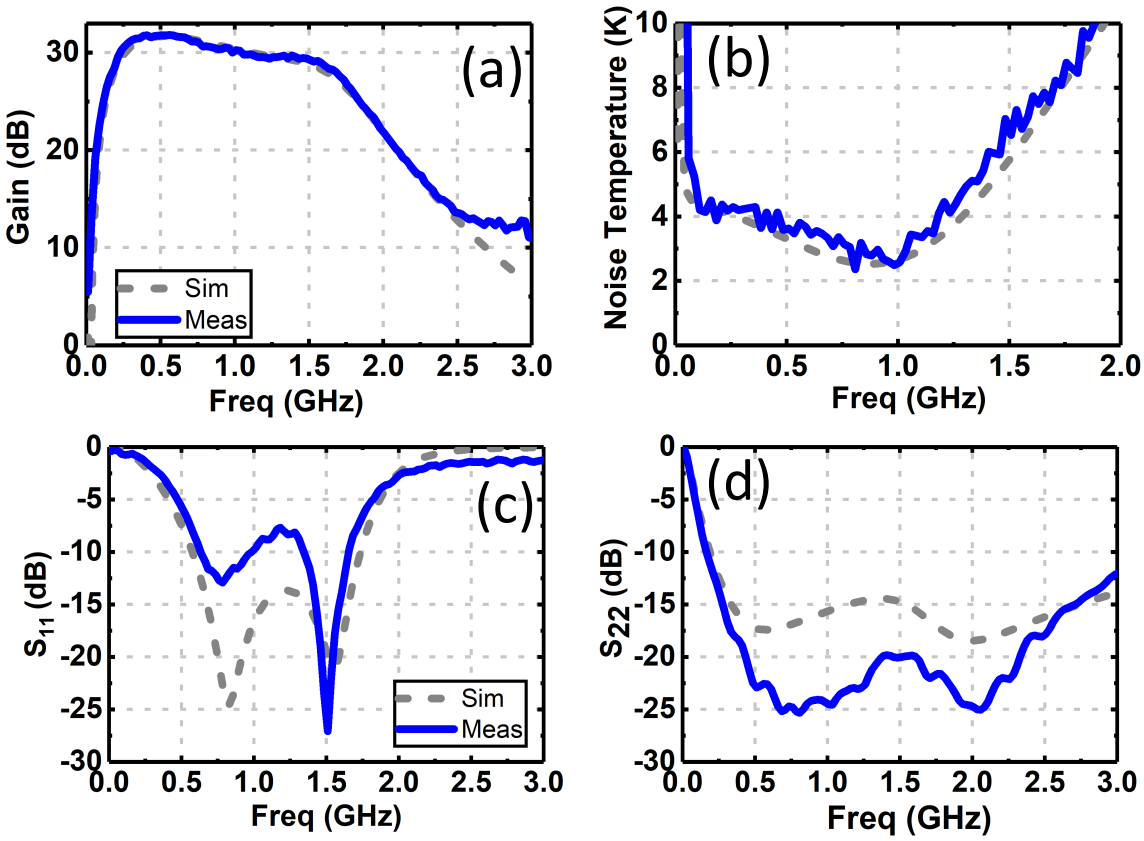


Figure 5.9. LNA cryogenic measurement results (solid blue lines) and comparison with simulations (dashed black lines) while the amplifier is consuming 6.6 mW dc power ((a) Gain (b) Noise temperature (c) S_{11} (d) S_{22}). The amplifier was biased at V_{C1}=0.85 V, I_{C1}=4.8 mA, V_{C2}=0.85 V, and I_{C2}=3 mA. The amplifier and the attenuator temperatures were 16 and 15 K, respectively.

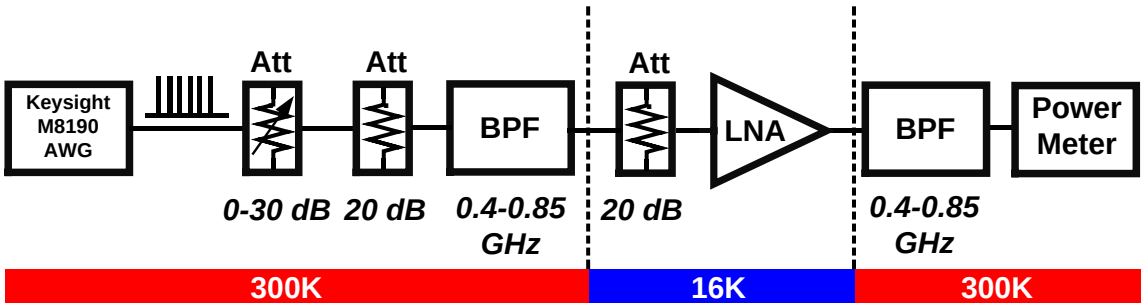


Figure 5.10. Test setup used to characterize compression characteristics of the LNA. For CW measurements, the arbitrary waveform generator was replaced by a CW generator.

worst case is considered in setting the linearity requirements. Assuming -90 dBm power of each tone (referenced to the plane of the detector coupling capacitor), this corresponds to about -62 dBm average power at the input of the LNA. It is also assumed a randomized phase for input tones to minimize peak to average power ratio. Compression measurements were carried out using the test setup shown in Fig. 5.10, with both CW and multi-tone stimuli. For the multi-tone measurement, a frequency comb consisting of 560 random phase sinusoidal tones spanning the frequency range of 0.4–0.85 GHz is employed, as shown in Fig. 5.11. This frequency range was chosen to align with the filters shown in Fig. 5.10. Results of the CW compression measurements are compared to those of the multi-tone measurement in Fig. 5.12 for a bias point of V_{CC1} =0.7 V, I_{CC1} =4.8 mA, V_{CC2} =0.5 V, and I_{CC2} =3 mA (P_{DC} =4.9 mW). In all cases, the input-referred 1 dB compression point was found to be greater than -53 dBm. Based on these results, it appears that the amplifier should be able to amplify the required spectrum without introducing significant distortion.

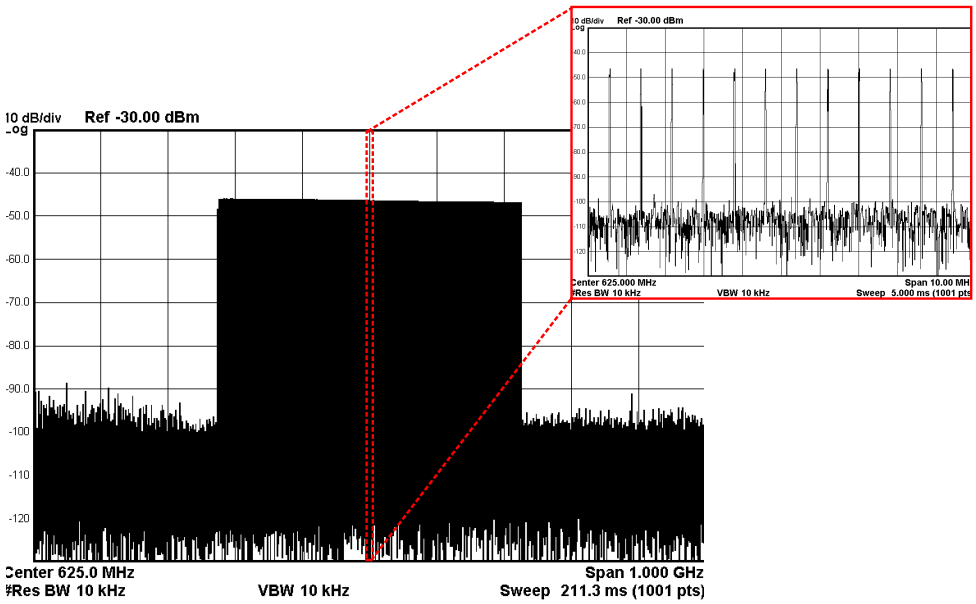
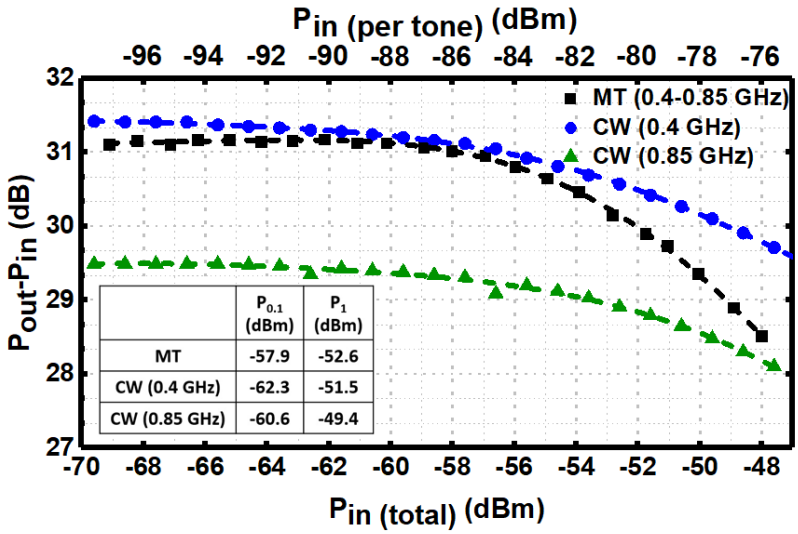


Figure 5.11. Spectrum of multi-tone stimulus. The signal consists of 560 evenly spaced tones spanning the frequency range of 0.4–0.85 GHz.



	$P_{0.1}$ (dBm)	P_1 (dBm)
MT	-57.9	-52.6
CW (0.4 GHz)	-62.3	-51.5
CW (0.85 GHz)	-60.6	-49.4

Figure 5.12. Measured compression characteristics for CW (Blue=0.4 GHz and green=0.85 GHz) and multi-tone stimuli (Black). The upper x-axis scale corresponds to the input power per-tone for the multi-tone (560 tones) stimulus, which is expected to be -90 dBm in the TolTEC system.

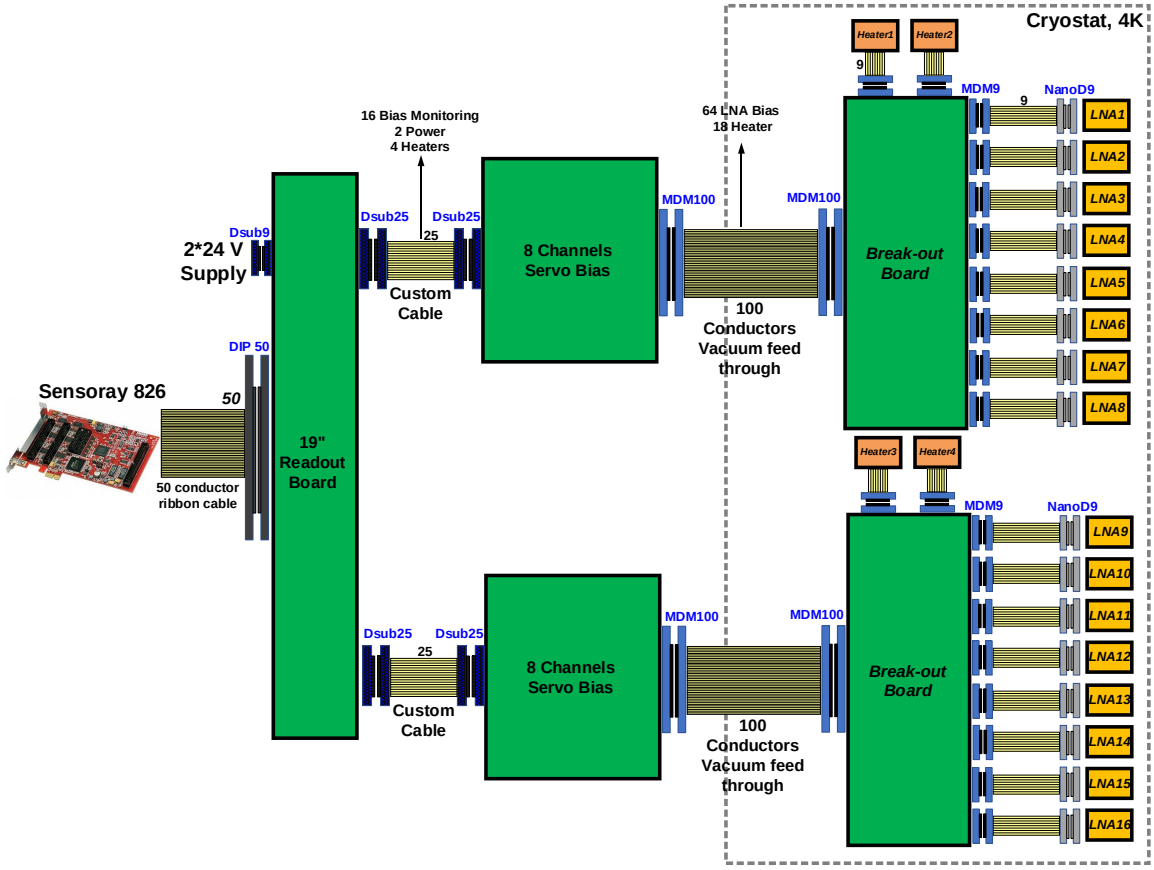


Figure 5.13. Simplified diagram of the bias board and wiring towards LNAs array and sensory board. Two breakout boards are used to divide each LNA biasing signals.

5.7 LNAs Array Implementation in the MKID Readout System

As mentioned, two designed servo bias boards are mounted in two custom-built RF tight packages and placed on two sides of the cryostat. A simplified diagram of bias board wiring to the LNA array is shown in Fig. 5.13. Two custom-built standard two-layers FR4 boards, called "breakout boards," are used within the cryostat to route the bias lines from a single 100 pin micro-D connector to up to eight amplifiers via a 9-pin nano-D interface. This breakout board is also used to distribute the signals associated with four heaters. A versatile analog and digital I/O system on a PCI Express board, is used to receive the readout signals from the readout board.

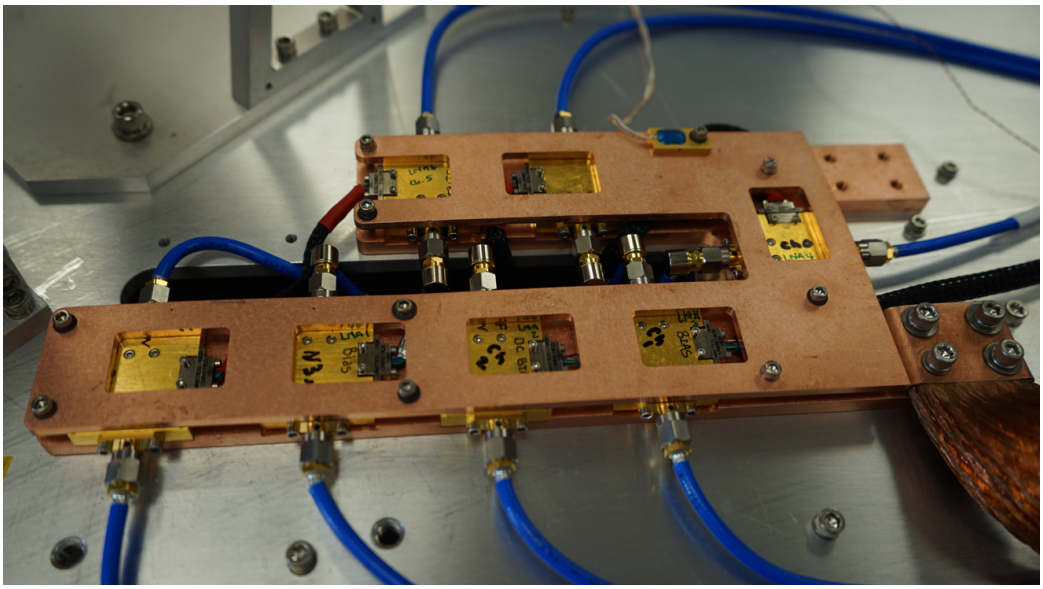


Figure 5.14. First LNA array, including 7 LNAs, implemented in the camera.

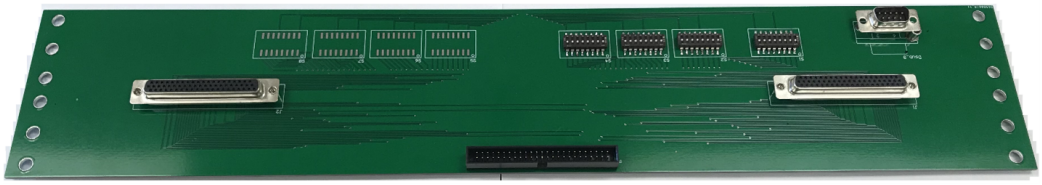


Figure 5.15. Readout board for monitoring base and collector voltages of the LNAs.

Thirteen LNAs are used in the camera system. It is divided into two assemblies, which include 7 and 6 LNAs, respectively. An image of the 7-LNA array is shown in Fig. 5.14. A picture of the readout board is shown in Fig. 1.6. Two 25-pin D-sub connectors are included to monitor the base and collector voltages of to a 64 element switch matrix is included at room temperature to route these monitor points to the digitizer system.

CHAPTER 6

WIDEBAND SIGE HBT CRYOGENIC LNAS AS MIXER-BASED SYSTEMS

Heterodyne detection is another application for cryogenic LNAs, which is the target of this chapter. Two wideband cryogenic LNAs (as IF amplifiers) are designed and implemented for HEB and SIS mixers. Wideband and low power LNA design challenges and trade-offs, which are required for these readouts, are discussed in the design section, and finally, experimental results and comparison with other state-of-the-art cryogenic LNAs are reported. Some portions of this chapter is reported in International Microwave Symposium [47].

6.1 SiGe HBT LNA Direct Integration with HEB Mixers

The scalability of THz heterodyne focal plane arrays (FPAs) for radio astronomy is fundamentally limited by the power dissipation of the IF low-noise amplifiers (LNAs), which must be tightly coupled to superconducting mixers and heatsunk to the 4 K stage of a closed-cycle refrigeration system. Therefore, any reduction in the power consumption of these cryogenically cooled amplifiers can be translated into more pixels or a reduced heat load for the cryogenic cooler, which corresponds to a reduced system power consumption.

While SIS mixers can operate with relatively high IF frequencies—allowing for the use of octave bandwidth IF LNAs—these devices only work below the gap frequency of the superconductor (proportional to critical temperature), which is typically about 1 THz. As such, heterodyne focal plane arrays operating well above 1 THz typically

employ hot electron bolometer (HEB) mixers. Since the IF bandwidth of an HEB mixer is limited to 3–5 GHz by electrothermal feedback [53, 76], an IF LNA with frequency response extending as close as possible to dc is desired for this application. This imposes additional challenges when trying to design for low power consumption while also achieving a noise temperature below 5 K, as needed for maximizing sensitivity. Here, the design and implementation of a wideband cryogenic SiGe LNA optimized for integration into an HEB-based FPA is described.

6.1.1 LNA Design and Implementation

A two-stage amplifier is designed based on the Tower Semiconductor SBC18H5 technology, and cryogenic noise and small-signal models are created for simulations with the procedure described in Chapter 3. To match the specifications associated with an HEB IF amplifier, it is targeted a gain, bandwidth, and noise temperature of 30 dB, 0.1–3 GHz, and 5 K, respectively, all while maintaining a power consumption of no more than 1 mW. The final circuit design appears in Fig. 6.1. Capacitively coupled resistive feedback was employed to provide a broadband input match (35 MHz lower cutoff frequency) while enabling separate biases for the base and collector of the first stage. In comparison to a traditional self-biasing approach, capacitive coupling enables a power reduction of up to six times (at cryogenic temperatures, typical values of V_{BE} are about 1 V, but V_{CE} can be below 200 mV). The first-stage transistor sizing was selected to give $R_{\mathrm{OPT}} \approx 50\,\Omega$ near the upper frequency when the HBT was biased at a collector current of 2 mA ($J_{\mathrm{C}} = 0.41\,\mathrm{mA}/\mu\mathrm{m}^2$). Resistive loading with inductive peaking was employed due to the broadband nature of the design. The second stage features a similar design, but was optimized as a trade-off between gain flatness and output match. The design requires off-chip capacitors for input and bypass, which can be realized using off-the-shelf wire-bondable silicon capacitors. Since the lower band cut off of the amplifier was specified to be 100 MHz, a >47 pF ac coupling capacitor

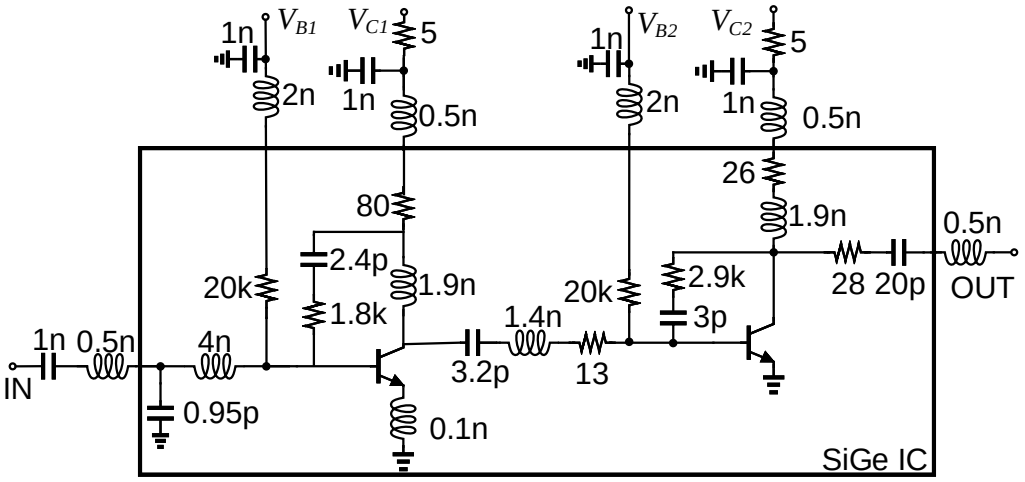


Figure 6.1. Schematic design of wideband cryogenic LNA for HEB mixer readout. Transistors total emitter areas for the first and second stages are 5.4 and 7.2 μm^2, respectively.

Table 6.1. Model Parameters at a Physical Temperature of 7 K

Stage	J_C $mA/\mu m^2$	Device Size μm^2	R_B $\Omega \cdot \mu m^2$	R_E $\Omega \cdot \mu m^2$	R_C $\Omega.\mu m^2$	C_{CB} $fF/\mu m^2$	C_{CS} $fF/\mu m^2$	C_{BE} $fF/\mu m^2$	g_m $mS/\mu m^2$	τ ps	β -	r_{be} $\Omega \cdot \mu m^2$
First	0.41	5.4	7	2.9	5.4	26.3	6	61	54.7	6.1	1.7e4	35e4
Second	0.13	7.2	5.9	2.9	5.4	26.3	6	50	25.3	3.2	9.1e3	47e4

was required; on-chip implementation of such a large capacitance is impractical due to area constraints. Instead, a 1 nF off-chip input AC coupled capacitor is used. Also, the input wire-bond is considered as a degree of freedom for noise optimization. Cryogenic small-signal model parameters for the first and second stage transistor are shown in Table 6.1.

A disadvantage of using resistive feedback for broadband impedance match is the thermal noise contribution of the resistor. For the first stage, added noise is $T_a R_{\rm gen}/R_f$, where $T_{\rm a}$ is the ambient temperature, $R_{\rm f}$ is the feedback resistor, and $R_{\rm gen}$ is the impedance seen looking back towards the generator from the node where the feedback resistor connects to the input. With assuming 15 K ambient temperature, the added noise will be 0.4 K. Second, the ac coupling capacitor limits the

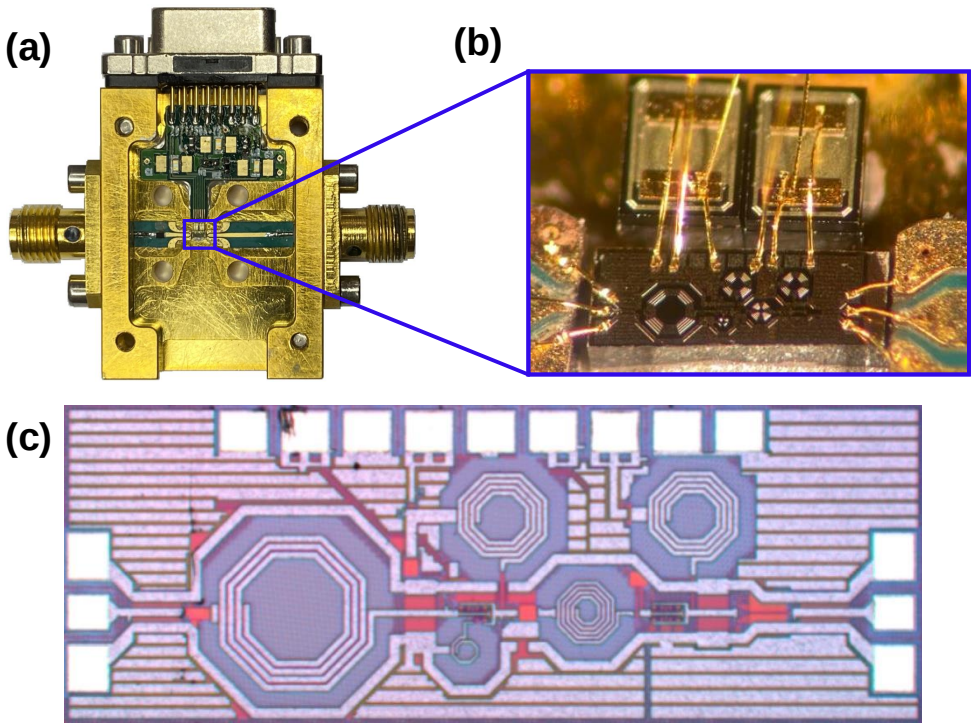


Figure 6.2. (a) Assembled module, (b) Wire-bonded chip, and (c) Chip photograph.

low-frequency cutoff of the input-match, so a 2.4pF coupling capacitor was selected to push this cut-off to well below the required 100 MHz.

The integrated circuit was fabricated in the Tower Semiconductor SBC18H5 process. The small-signal and noise models and the SiGe HBT cryogenic performance of the process were discussed in Section 1 of Chapter 3. The fabricated chip photograph is shown in Fig. 6.2(c). The chip dimensions are 0.45 mm×1.4 mm and standard 100 μm-patch GSG pads are used for RF I/Os. The amplifier was measured both on-wafer (s-parameters) and in a coaxial fixture (gain and noise). The amplifier is assembled inside a coaxial module (Fig. 6.2(b)). Two 8- mil Rogers 4003C RF PCBs are designed to permit RF transitions into and out of the chip and also to accommodate the off-chip bypass capacitor, a standard FR4 PCB is used. The wire-bonded chip chip, along with two 10 nF bondable bypass capacitors, is shown in Fig. 6.2(b).

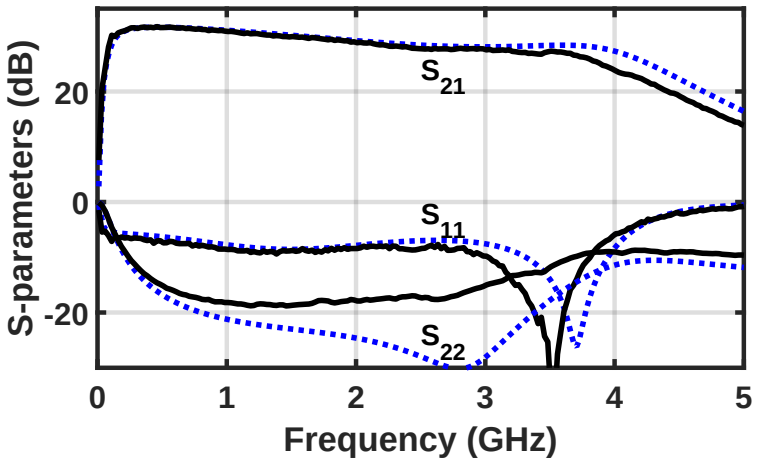


Figure 6.3. On-wafer room temperature measurement of chip and comparison with simulations ($P_{\mathrm{DC}} = 8\,\mathrm{mW}$).

6.1.2 Experimental Results

To verify the chip performance and Cadence models, on-wafer s-parameters measurement were carried out at 300 K using a room temperature probe station. The measurement results and comparison with Cadence simulations are shown in Fig. 6.3. For these measurements, the amplifier was biased at a DC power consumption of 8 mW. As shown, there is an excellent agreement between measurement and simulation.

After verifying room temperature operation, the amplifier was mounted within a module for cryogenic characterization. The module was then installed in a cryostat equipped for the cryogenic noise and gain measurements using the cold attenuator method. This system is calibrated, and it is believed the accuracy is better than ± 1 K. Measurement results acquired at a physical temperature of 15 K and power consumption of 0.96 mW are compared to simulation in Fig. 6.4. The measured noise temperature agrees quite well with simulation for frequencies below 2 GHz and then begins to rise. Based on the simulations, it is believed this discrepancy is due to an overestimation of the input bond wire inductance in the simulation and that the noise

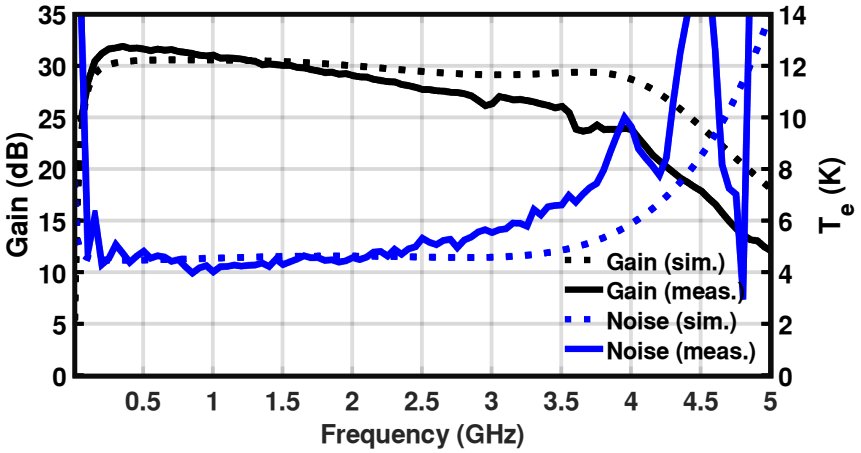


Figure 6.4. Measured and simulated gain and noise temperature at a physical temperature of 15 K. These data were taken for a dc power consumption of 0.96 mW (I_{C1} =2 mA, I_{C2} =0.8 mA, V_{C1} =0.4 V, and V_{C2} =0.2 V).

could be improved in the upper-frequency range by tweaking the length of this bond wire.

On the other hand, the gain response demonstrated significantly more roll-off in comparison to simulation in Cadence Microwave Office. As the same behavior was seen when the module was measured at room temperature but saw better agreement between the gain when measured on-wafer, it is believed that the discrepancy may be due to incomplete modeling of the passive components for the cryogenic simulations or related to packaging. Nonetheless, the performance is sufficient for the HEB IF amplifier application because, in the simulations, the bandwidth was over-designed. The required specifications for the bandwidth was 0.1-3 GHz; however, in the cryogenic simulations, 0.1-4 GHz was considered for that.

To ensure that the performance was not sensitive to V_{C1}, the dependence of the amplifier on the collector-side supply voltage is studied when biased for a constant collector current. The results (Fig. 6.5) confirm that the noise performance of the amplifier is insensitive to V_{C1} for collector-emitter voltages as low as 100 mV.

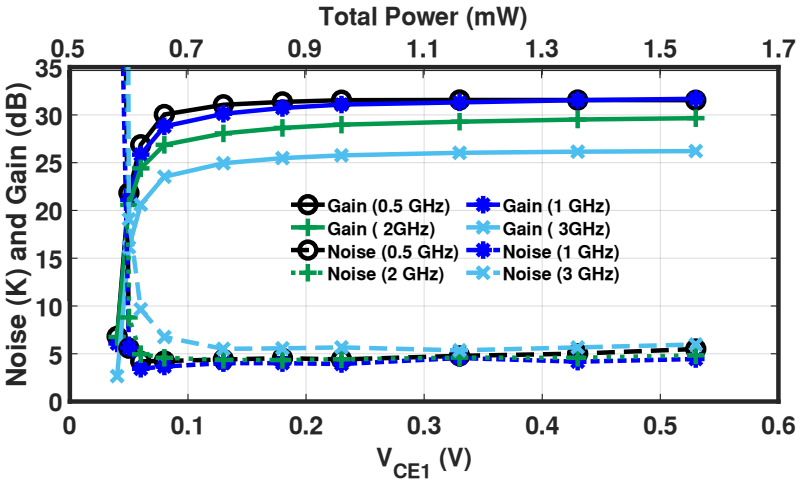


Figure 6.5. Cryogenic amplifier performance as a function of first stage power dissipation. As there is 85 Ω of series resistance, V_{C1} is 170 mV higher than the collector–emitter voltage.

6.1.3 Comparison and Conclusion

The noise temperature, power consumption, and bandwidth of the cryogenic LNAs reported in the literature that can potentially be used for this application are shown along with the results achieved by this amplifier in Fig. 6.6. As shown, InP HEMT based LNAs (red plots) provide the lowest noise temperature, but dissipate relatively high power. Moreover, InP LNAs are not very practical at lower than 1 GHz frequency because of the inherent features (very high input impedance) of HEMT devices. Furthermore, existing SiGe HBT LNAs (blue plots), which can be used at lower than 1 GHz frequency, consume more than 7 mW dc power while lower than 1 mW power consumption for the target application is required. The black line is the measured performance of the designed LNA. As shown, we achieved lower power and a wider fractional bandwidth in comparison with other works.

6.2 General Purpose Wideband Cryogenic LNA

In this section design of a general purpose SiGe HBT cryogenic LNA is targeted. The goal of the design was a fully integrated amplifier that is compatible with both

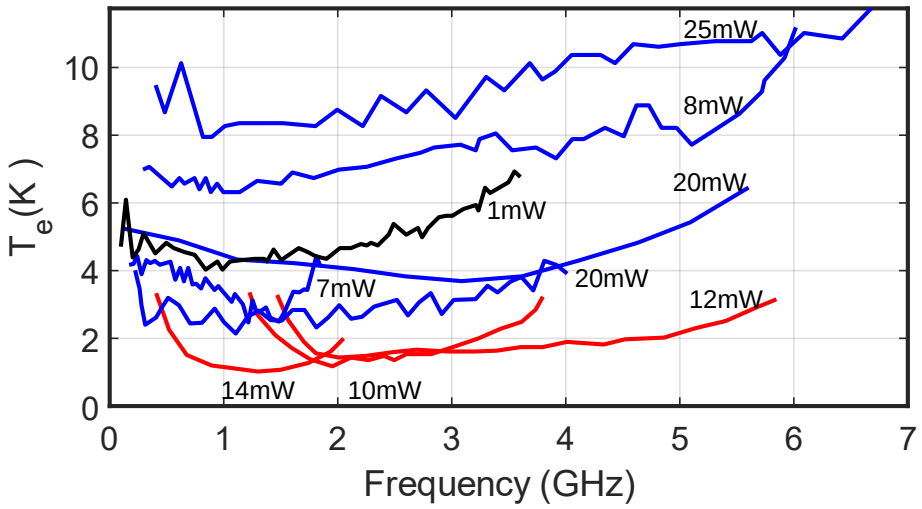


Figure 6.6. Cryogenic LNAs specifications which potentially can be used for IF LNA of HEB mixer (Black: This work, Red : InP HEMT, and Blue: SiGe HBT) [15, 79, 81, 82, 23, 46].

HEB and Superconductor-Insulator-Superconductor (SIS) mixers based heterodyne receivers [52, 40]. Therefore, the bandwidth specification for this LNA is 0.5-8 GHz. Since using of a simple input matching network was desired (second-order), there is a compromise between noise performance and bandwidth which will be discussed in the design section below. Power consumption of the LNA should be as low as possible to enable scalability of these receivers, as described in the previous section. A power consumption lower than 2 mW was targeted in our cryogenic simulations. Typically, 27-30 dB gain is enough for both HEB and SIS mixer based receivers [62, 66, 39]. A higher than 10 dB input and output return loss was aimed for this LNA.

6.2.1 Cryogenic LNA Design and Implementation

A SiGe-based cryogenic LNA IC was designed, implemented, and characterized. 28 dB gain, lower than 2 mW DC power consumption, and lower than 6 K noise temperature was targeted for this LNA while the ambient temperature is 4 K. The schematic of the LNA is shown in Fig. 6.7. A two-stage common-emitter with re-

sistive load and without inductive degeneration provides wideband response for this LNA.

A series of 80 Ω resistor with 0.5 nH inductor in the collector of the first stage HBT provides wideband gain. However, the voltage drop on the resistor causes higher power consumption. To prevent that, a relatively small transistor size is used for the first stage (A_e=3.6 μm^2), which helps to have lower dc current (and lower drop voltage on the resistor) while current density is still at the optimum place for the noise performance. The smaller size of the transistor causes higher optimum noise impedance. This may not be ideal when the LNA is matched with 50 Ω source impedance. However, it provides lower sensitivity of the noise performance with the source impedance. Please note the amplifier was designed for 100 Ω noise optimum impedance. That's why noise performance is less sensitive to source impedance (50 Ω was inside a noise circle). Since the target of this LNA was general purpose applications, lower sensitivity to the source impedance is a desirable characteristic.

A second-order ladder input matching network is selected to achieve simultaneous noise and power matches, while the first stage current density is chosen to minimize added noise of the transistor. An off-chip DC-block capacitor and length of input wirebond are used as the degree of freedom for noise performance tweaking after fabrication. The same biasing circuit as HEB mixer LNA is selected for this LNA.

The chip is fabricated based on the Tower Semiconductor SBC18H5 process (is the same as the previous LNA). The assembled chip inside the coaxial module is shown in Fig. 6.8. Assembly components are the same as the HEB mixer LNA. However, the input ac coupled capacitor is part of the matching network for this LNA.

6.2.2 Experimental Results

First, the on-wafer room temperature performance of the chip is verified by on-wafer s-parameter measurements. The measurement results and comparison with

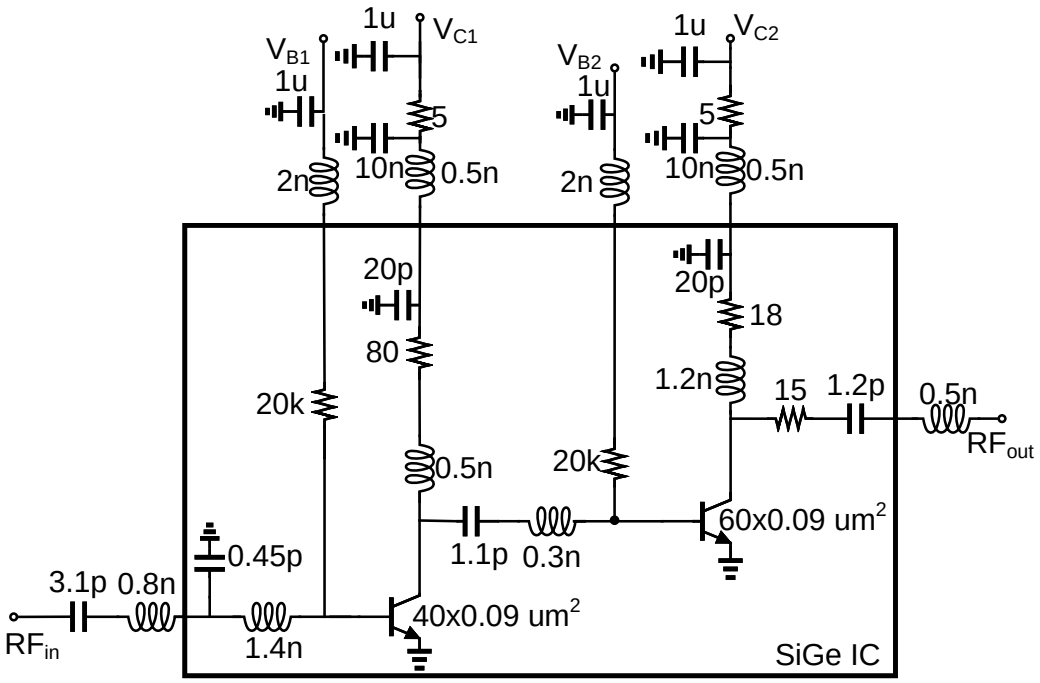


Figure 6.7. Schematic design of wideband cryogenic LNA for SIS mixer readout.

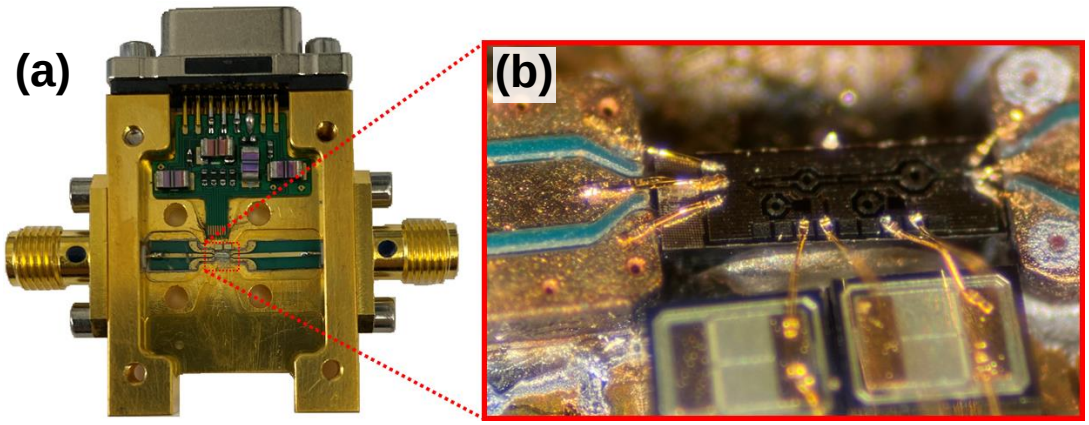


Figure 6.8. (a) Assembled module, (b) Wire-bonded chip and bypass capacitors.

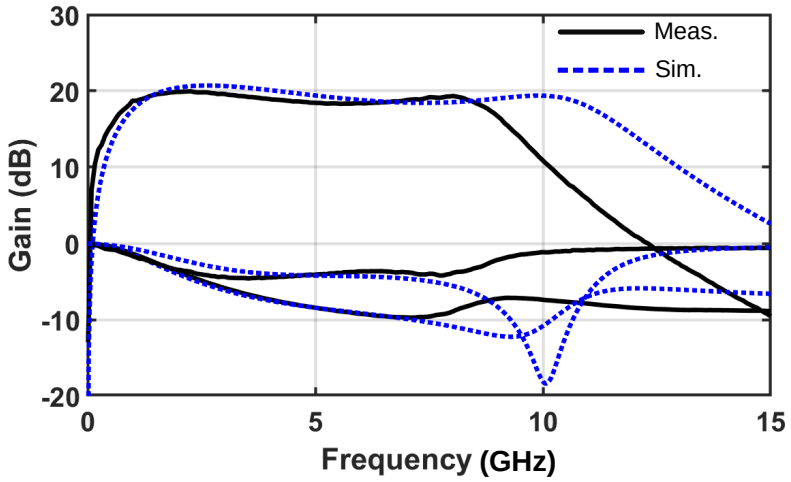


Figure 6.9. On-wafer room temperature measurement of chip and comparison with simulations ($P_{\mathrm{DC}} = 17\,\mathrm{mW}$).

Cadence simulations are shown in Fig. 6.9. The observed mismatch in gain and return loss above 7 GHz may be due to the fact that we did not run parasitic extraction or may be related to incomplete electromagnetic modeling. Since off-chip input ac-coupled capacitor is part of input matching network, measured on-wafer input return loss is low.

The assembled amplifier was next characterized inside the custom-built cryostat. The measured input-referred noise temperature and gain are shown in Fig. 6.10. Noise and gain are measured based on the cold-attenuator method with ±1 K noise measurement accuracy. 28 dB average gain, and 6.5 K average noise temperature is measured for 1–7 GHz frequency band while the cryostat temperature is 16 K and dc power consumption is 1.5 mW.

6.3 Conclusion and Future Work

Two wideband cryogenic IC LNA are designed and measured based on BiCMOS SBC18H5 technology. The first LNA was characterized as IF LNA for HEB mixer heterodyne receivers. A feedback resistor topology with dc block capacitor provided

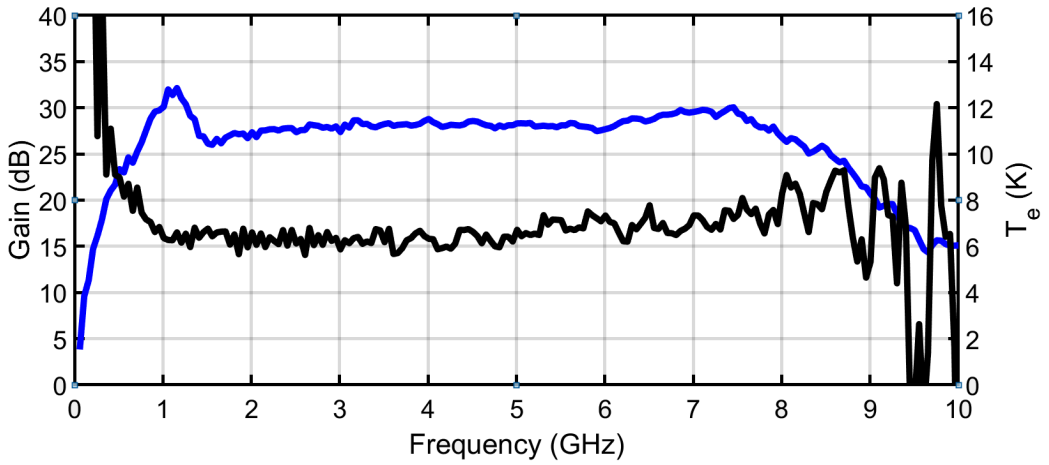


Figure 6.10. Measured gain and noise temperature at a physical temperature of 16 K. These data were taken for a dc power consumption of 1.5 mW.

simultaneous wideband (0.1-3 GHz) and low-power (<1 mW) specifications which are ideal for scalable heterodyne receivers. As a next step, an array of these LNAs should be integrated with a HEB mixer and characterized inside the receiver system.

The second amplifier was targeted for general purpose mixer-based heterodyne receivers. Smaller transistor size with resistive load provides wideband (0.5-8 GHz) and low power (<1.5 mW) specifications are achieved with a compromise of noise temperature performance (<8 K). Based on cryogenic simulations, it is believed noise temperature results will be better with larger source impedance.

CHAPTER 7

LOW POWER AND HIGH RESOLUTION CRYOGENIC DAC DESIGN

Biasing of cryogenic HBT LNAs is challenging due to the inherent exponential relation between collector current and the base voltage and the requirement of precise control of DC current for most cryogenic applications. Moreover, most conventional biasing methods, such as collector feedback resistor and resistor divider, consume power that is not suitable for scalable applications. Added noise of biasing circuitry is another essential factor that should be considered.

In this chapter, an integrated approach for biasing of SiGe HBT LNAs is proposed, which improves their scalability. The approach is implemented in a bias-integrated LNA, and also it is used for a programmable LNA, which will be described in the next chapter.

First, a quick literature review is presented on the current methods of cryogenic LNA biasing before proposing our approach. Then, the design of an on-chip digital to analog converter (the core of the biasing method) and cryogenic considerations are described. Finally, to verify the approach, it is implemented inside a tunable bias integrated cryogenic LNA.

7.1 Cryogenic LNAs Biasing Approaches

At cryogenic temperatures, the sharpness of the I_C versus V_{BE} curve of a SiGe HBT increases drastically, and the entire valid operating range ($\ll 0.1\mathrm{mA}/\mu\mathrm{m}^2$ to $> 10\mathrm{mA}/\mu\mathrm{m}^2$) compresses to a V_{BE} swing of less than 100 mV. As such, when biasing

the base of a cryogenically-cooled SiGe HBT using a voltage source, which is the most common approach to bias a cryogenic LNA, the supply resolution must be $\leq 500\,\mu$V. Previous experiments have employed external sourcemeters [65, 62]. This approach is not scalable, even for a small array of LNAs. As mentioned in the MKID chapter, a servo bias board was designed and implemented to bias up an eight LNAs array [46]. Using the bias board method, the requirement of 32 high-resolution external source meters for 8 LNAs is removed, and just one unregulated power supply is sufficient. However, for a more extensive LNA array (e.g., thousands) which might be required for the next generation of quantum computers readout, the bias board approach wiring complexity will be increased, and it is not a feasible approach. So, an on-chip approach is more reliable for a larger LNA array.

The most common on-chip approach that is used in the literature is self-biasing [23]. Two typical circuit implementations are shown in Fig. 7.1. Both of these approaches have two common problems. First, since V_{CC}>V_{B}, the minimum value of the collector supply voltage is determined by the voltage required to bias the base terminal. Since $V_{\mathrm{BE}} \approx 1\,\mathrm{V}$ at cryogenic temperatures, V_{CC} must be in the 1 V range as well. This problem causes higher power consumption because of collector DC current.

It turns out that, one of the main advantages of SiGe HBT cryogenic LNA to its counterpart, InP LNA, is low power consumption because of the capability of operating with V_{CC} at near the knee voltage. By using the self-bias approaches, taking advantage of this feature is not possible.

In the next section, a low-power approach will be proposed that does not need a high-resolution power supply by taking advantage of the CMOS integration of the BiCMOS process.

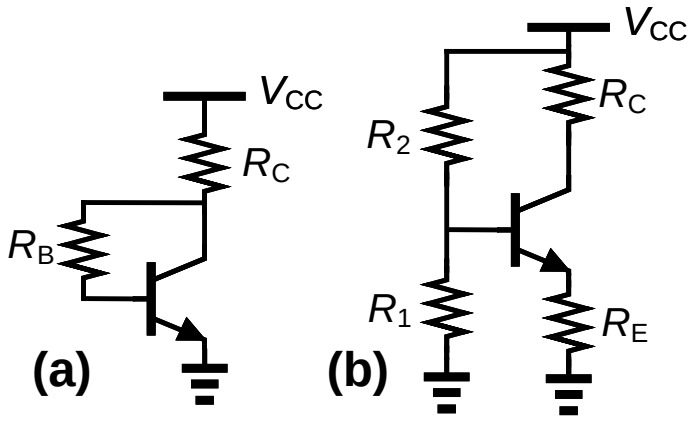


Figure 7.1. Self bias approaches of SiGe HBT cryogenic LNAs.

7.2 Programmable Base Voltage Biasing

The proposed approach for biasing of the SiGe BiCMOS LNA is shown in Fig. 7.2. It is a tunable resistor divider followed by a low-pass filter (LPF) to minimize the noise and increase the impedance seen from the resistor divider (Z_{in}). Base DC current of the transistor must not affect the resistor divider current. In other words, real part of impedance seen from divider should be much higher than R_1 in all programming states ($\Re(Z_{\text{in}}) \gg R_1$). The current through the divider should be 10-100 X larger than the base current. This does not make any problem at cryogenic temperature, since β is significantly larger than room temperature. So, selection of a low value for R_1, which caused power consumption in the resistor divider, is not required.

The supply sensitivity should be considered for the proposed approach, the g_m sensitivity to the supply voltage (V_{DD}) can be written as:

$$\frac{\partial g_m}{\partial V_{\text{DD}}} \approx \frac{I_C}{n^2 V_{\text{T}}^2} \times \frac{R_1}{R_1 + R_2} e^{\frac{R_1}{R_1+R_2}\frac{V_{\text{DD}}}{nV_{\text{T}}} - \frac{V_{\text{BE}}}{nV_{\text{T}}}}, \tag{7.1}$$

$$\Delta V_{\text{DD}} \approx \frac{\Delta g_m}{g_m} \tag{7.2}$$

where, R_1 and R_2 are resistor divider resistors. For typical numbers of a cryogenic HBT, it can be shown that $40\,\mu$V RMS supply fluctuation leads to 1% RMS fluc-

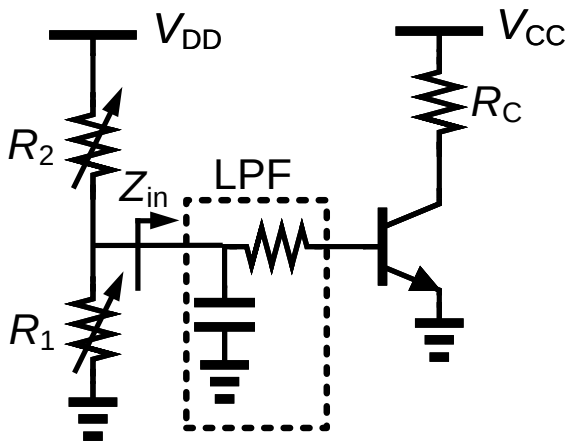


Figure 7.2. Idea of programmable base voltage biasing for SiGe BiCMOS LNA.

tuation in g_m and these numbers can be achieved using an LDO with appropriate filtering. Moreover, the added noise of the resistive feedback should be taken into account because it potentially causes supply fluctuation. RMS noise equivalent voltage of 1 MΩ resistor at 20 K temperature is $33\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. A 20 kΩ series resistor and 20 pF parallel capacitor are used as an LPF structure (Fig.7.2) to eliminate added noise of the resistive DAC.

To enable testing, the states of the resistive divider should cover the base voltage biasing range for both cryogenic and room temperature operation. For a typical HBT, this range is inside 0.8–1.1 V. Moreover, as mentioned in the previous section, the resolution should be lower than ∼0.5 mV. A 0.6-1.2 V with 250 mV steps are targeted in our design.

The circuit implementation of our approach is shown in Fig. 7.3. To cover 0.6 V tuning range with 0.25 mV steps, 4 bits of coarse tuning range and 8 bits of fine-tuning are used. The fine-tuning bits are implemented using an digital to analog converter, described in the following section. The coarse tuning is realized using unit cells, each consisting of three nMOS switches and a resistor as shown in the Fig. 7.3. The total absolute value of the resistors (R_t) in the coarse tuning circuit dominates the power

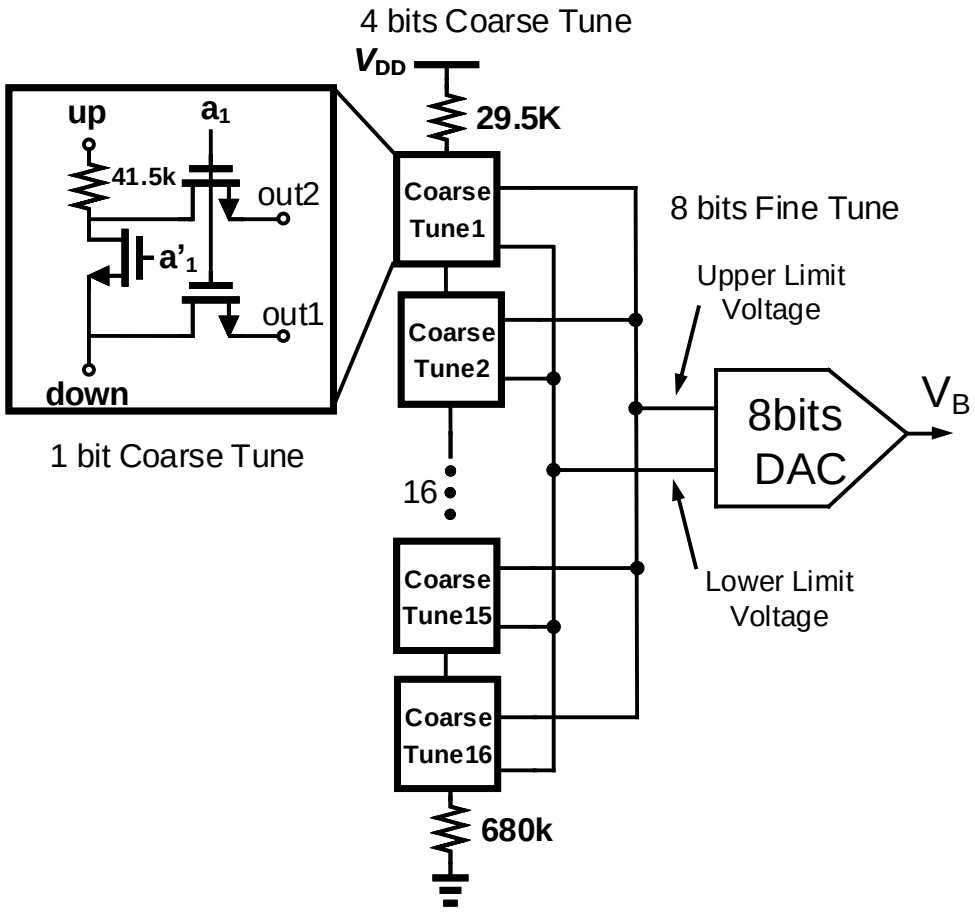


Figure 7.3. Circuit implementation of base voltage divider for the LNA. Four/eight bits coarse/fine tuning bits are used for 0.6 V voltage covering range and 0.25 mV voltage resolution.

consumption of the whole biasing circuit. However, as mentioned before, there is a trade-off between power consumption and linearity of the proposed circuit because the R_t should be lower than impedance seen from the base of the HBT device. A 41 kΩ as the resistor value for each coarse tuning bit is selected. The total resistor of the divider, including 16 coarse tuning cells and 700 kΩ tail resistor, is 1.3 MΩ. Therefor, the power consumption of the total biasing circuit ($P_{DC} = (V_{DD})^2/R_t$) is around 1.4 μW which is negligible compare with the power consumption of a typical cryogenic LNA.

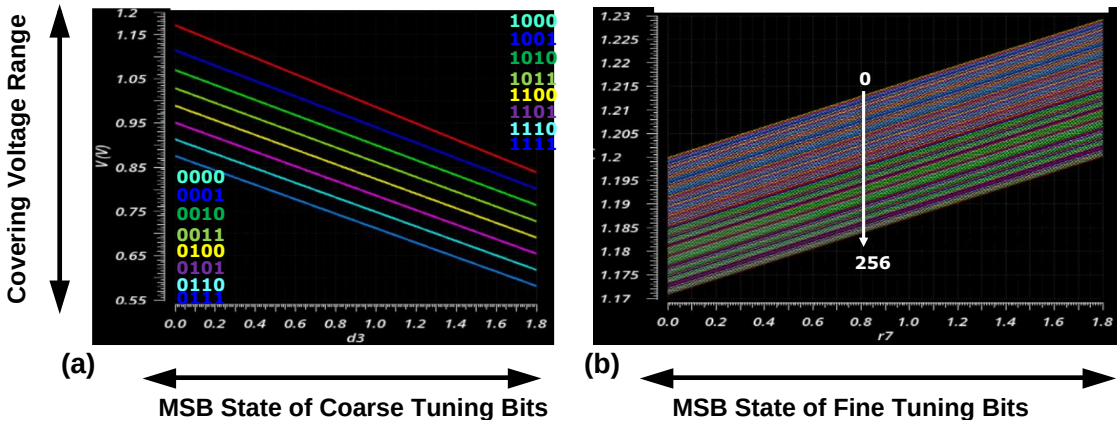


Figure 7.4. Cadence simulation results of base voltage tuning range. (a) Output voltage range for 16 states of coarse tuning bits and (b) Output voltage range for 256 states of fine tuning bits while coarse bits state is '1000'.

The room temperature simulation results of the programmable voltage divider are shown in Fig. 7.4. In Fig. 7.4(a), the output voltage of the divider (base voltage of transistor) is simulated while coarse tuning bits have swept. Four coarse tuning bits provide 15 states for the output voltage, as shown in the figure. There is a significant overlap voltage between each state as a margin to ensure the voltage divider covers all the 0.6–1.2 V range. Also, the output voltage of different states of fine-tuning bits (256 states of 8-bits DAC) are shown while coarse bit state is fixed to '1000', and the results are shown in Fig. 7.4(b). The DAC loading for this simulation is an HBT (with a 20 kΩ resistor in the base) at 300 K temperature.

7.3 Digital to Analog Converter Design

To implement the fine-tuning bits of the programmable voltage divider, an 8-bit DAC is designed. The simplified schematic of the design is shown in Fig. 7.5. This DAC also is used in the next chapter for programmable cryogenic LNA design. Unsalicided polysilicon resistors are selected for use in the DAC (also is used for the whole voltage divider) because of the low thermal coefficient of these resistors

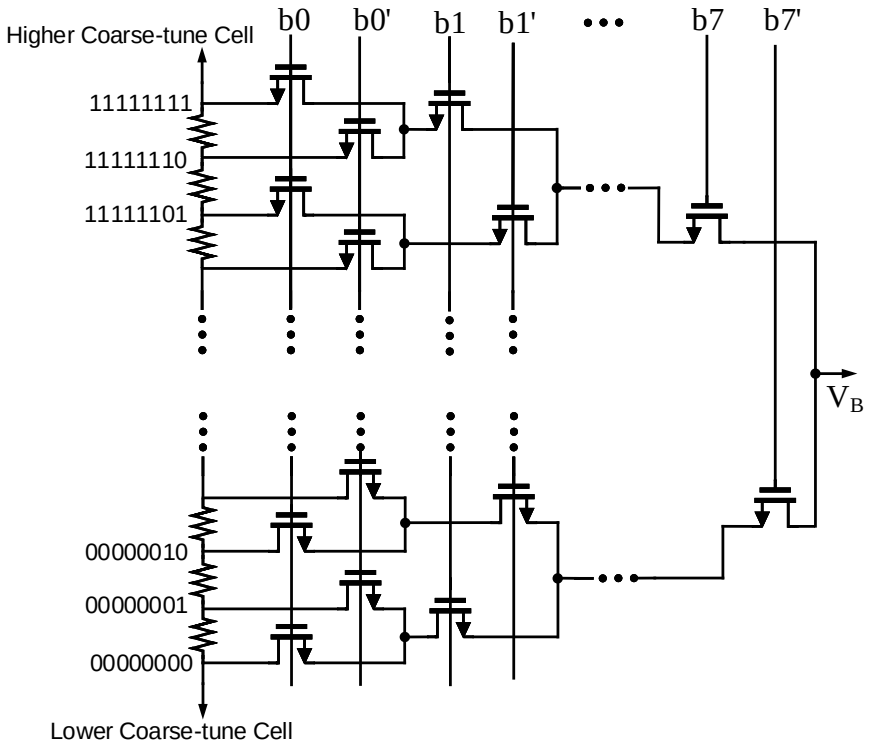


Figure 7.5. Eight bits low-power digital to analog converter.

compared other available resistors. However, this costs a bit larger area in the DAC because of relatively low sheet resistance of these resistors. The final layout of the whole programmable base voltage divider, including required digital programming circuits (standard shift register and decoder), is shown in Fig. 7.6.

7.4 Biasing Integrated Cryogenic LNA

7.4.1 Biasing Integrated Cryogenic LNA Design and Implementation

Using the described biasing approach, a SiGe BiCMOS cryogenic LNA is designed and implemented to verify the method. The LNA schematic design is shown in Fig. 7.7. A three-stage common-emitter topology was selected to provide 40 dB gain from 4-8 GHz. As shown, three base voltage dividers with RC LPF are used to bias up the stages. Also, an on-chip serial programming interface is used to program the

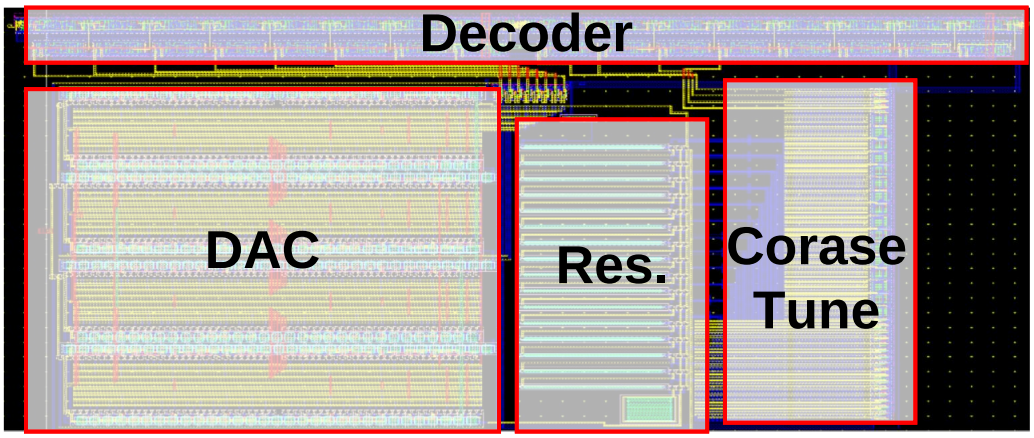


Figure 7.6. Programmable base voltage divider layout. The dimensions are $230 \times 140\,\mu m^2$. The layout includes 8-bits DAC, 4 bits coarse tuning switch-resistors, and a standard decoder.

DACs. The clock frequency of the programming bits can be reached up to 10 MHz. A simple first-order matching network is designed for the first stage to provide power matching while the first stage current density is selected to provide minimum noise temperature at 8 GHz frequency.

Three resistors with almost the same values are placed in the collectors. Since DC bias currents for all stages are 2 mA, the same collector voltage could be used for all stages. Therefore, using an on-chip programmable voltage divider approach, two unregulated power supplies are required for biasing the three stages of LNA. Please note that this LNA has not been optimized for minimum power consumption and optimum noise temperature, and it is just tried to verify the biasing approach and the digital interface with that. The gain of the LNA can be controlled by programming of DC bias currents.

The amplifier is fabricated based on the Tower Semiconductor SBC18H5 BiCMOS process. The chip photograph and assembled LNA are shown in Fig. 7.8. The assembly components are similar to what had been used for HEB and SIS mixers readout LNA. The only significant difference is using two-sided 15-pin MDM connector be-

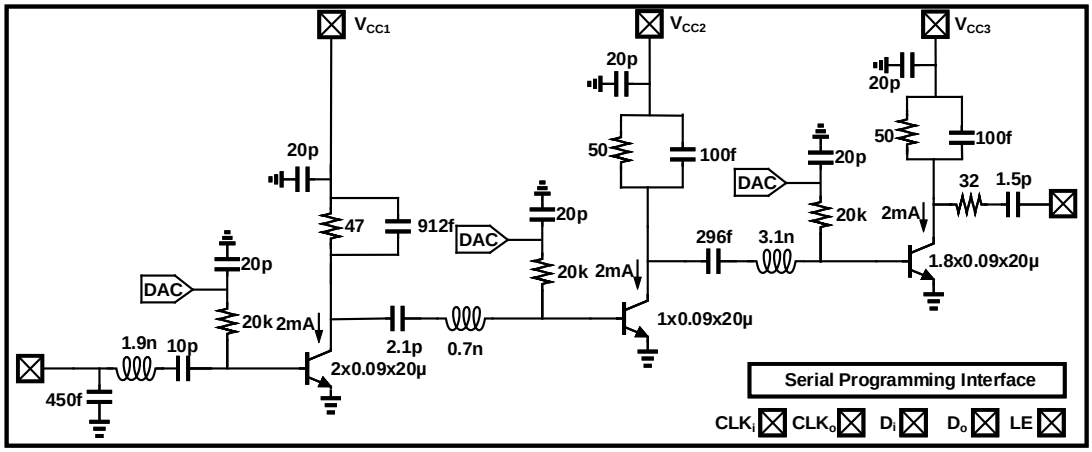


Figure 7.7. The schematic design of SiGe BiCMOS LNA to verify the bias integration approach. A three-stage LNA with common emitter topology without inductor degeneration. The chip includes a standard digital programming interface.

cause DC pads including digital interfaces and collector biases are on both sides of the chip. A 10 nF silicon wire bondable capacitor (near the chip), 5 Ω SMD series resistor, and 10 μF (thick near the DC connector) film SMD capacitor are used for collector DC bypassing.

7.4.2 Biasing Integrated Cryogenic LNA Experimental Setup and Measurement Results

The amplifier noise temperature and gain are characterized inside the custom-built cryostat with the cold attenuator method, while the amplifier and attenuator temperatures are 16.5 K and 19 K, respectively. The experimental setup is shown in Fig. 7.9. A Raspberry pi board is used to program the chip. Since the minimum available output voltage of the board was 3 V, a custom-built level shifter, PCB is designed to convert the voltage to 1.8 V. A constant 1.8 V supply voltage was sufficient to bias up three base stages. Two KE2401 supplies are used for the chip V_{DD} and collector bias voltages. Low-pass filters, including ferrite beads and bypass capacitors, are placed on the DC PCB (inside the module) for every biasing signal.

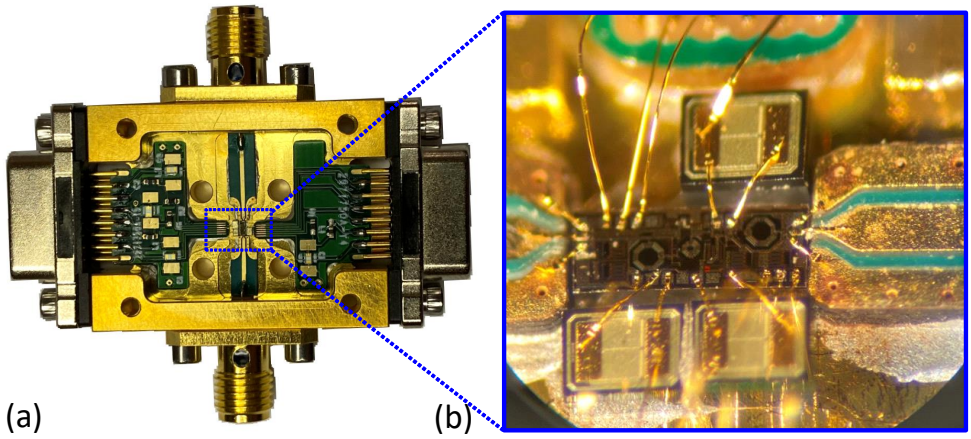


Figure 7.8. (a) Assembled chip inside a coaxial module. (b) wirebondeded chip photograph and collector bypass capacitors.

During the measurement, it is found that a stable supply for the DACs provides lower gain fluctuation of the LNA. As mentioned in the design part, g_m is sensitive to the supply changes, and this can be considered as a disadvantage of the resistive DAC. It was possible to decrease the gain fluctuation by adding a Low-pass filter structure on the module dc bias board (an RC structure, 100 kΩ and 50 nF). The author believes this effect could also be alleviated by using an LDO.

The standard cold attenuator method and a spectrum analyzer are used to characterize the LNA, as shown in the setup picture. 100 kHz clock frequency is used to program the chip. The programming efficacy was validated via clock-out and data-out signals.

Some samples of gain and noise temperature cryogenic measurement results are shown in Fig. 7.10. Even though biasing currents of all stages could be programmed, the first stage bias was kept constant to observe the LNA noise performance at the optimum noise biasing current. Then, DC bias currents of the second and third stages are programmed to verify the on-chip programmable biasing approach. First stage DC current is 5 mA for all cases while the second/third stages DC currents are 2.3 mA,

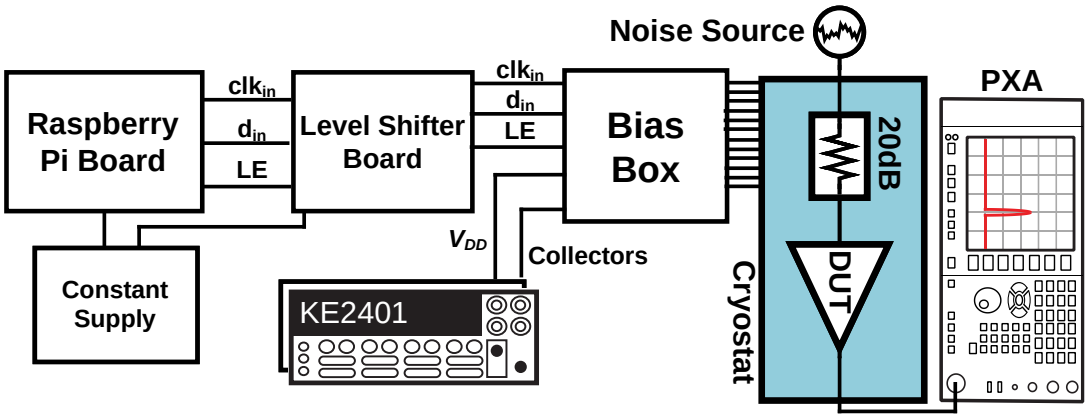


Figure 7.9. Cryogenic measurement setup for bias integrated cryogenic LNA.

2.5 mA, and 2.7 mA to achieve 33 dB, 35 dB, and 37 dB average gain, respectively (in 1.5-7.5 GHz). The noise temperature of the LNA remains constant (to 5 GHz) while bias currents are changing, which verifies that different states in biasing programming are not affecting the noise performance of the LNA.

The same biasing approach, DAC, and digital programming is used in the next chapter to implement programmable cryogenic LNA biasing. Moreover, the described DAC is used to provide required voltages in different parts of that LNA.

7.5 Conclusion

An on-chip scalable approach was proposed and verified to bias up a SiGe HBT cryogenic LNA. The approach was based on a programmable resistor divider and provided 0.6-1.2 V biasing range with 0.25 mV step for the base voltage. The number of high resolution supply voltage requirement is alleviated by using this approach, however, there are a couple of issues which should be considered.

First, an independent voltage supply for the collector is still required (even though a high-resolution supply is not needed for collector biasing). Second, the proposed approach is potentially sensitive to device parameter drift during the time. So, it is

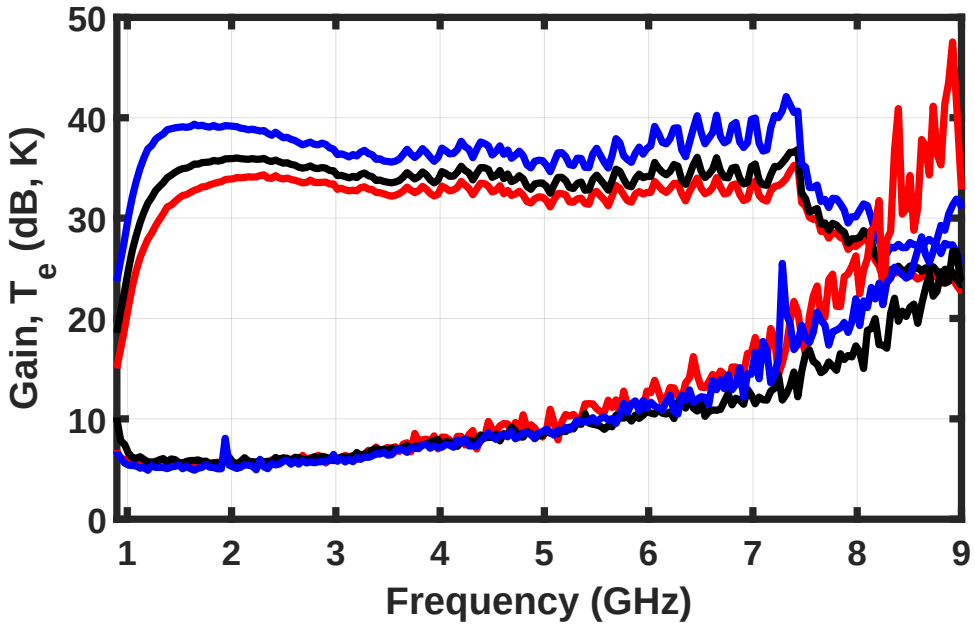


Figure 7.10. Cryogenic measurement results of the bias integrated LNA. Second and third stages DC bias currents are swept to achieve different average gains.

required that the HBT be programmed precisely for each device and during the time. A solution for this issue can be using digital feedback. It can be done by using an Analog to Digital Converter (ADC) and sampling from collector current, comparing with a reference voltage, and applying the difference to the base voltage via a digital integrator and the DAC.

CHAPTER 8

PROGRAMMABLE CRYOGENIC BICMOS LNA DESIGN AND IMPLEMENTATION

In this chapter, by taking advantage of the CMOS digital circuitry, including the previous chapter biasing approach, the first programmable cryogenic LNA is designed and measured. The LNA design and part of the measurements is a collaboration project with Zhenjie Zou.

8.1 Introduction

As mentioned in the motivation chapter, for a fault-tolerant quantum computer, an order of 1M qubits and 100,000 LNAs are required in readout channels. Reproducibility of the noise performance should be understood and optimized for this large-scale array of LNAs because it is not practical to package and measure each amplifier at cryogenic temperature. Having a cryogenic amplifier with the ability of performance tuning can be considered a step to achieving the goal.

Furthermore, the cryogenic LNA should satisfy these readouts' noise performance and power consumption requirements. For example, for a Transmon qubit readout, the required noise temperature for a 5 GHz signal is around 0.12 K [17]. This amount of noise temperature can be achieved by a Josephson parametric amplifier. However, the output saturation level of these types of amplifiers is limited (typically lower than 90 dBm). Since the signal levels are on the order of -120 dBm and 5–10 tones are typically multiplexed on a single readout line, the gain of such a parametric amplifier is limited to 15–20 dB [8]. So, the readout still needs another cryogenic LNA to provide

the rest of the required gain, and the noise performance of this LNA is critical due to the low amount of gain of the parametric amplifier. Typically a cryogenic LNA with <2 K noise temperature and >30 dB gain is required at a physical temperature of 4 K [16, 24]. Moreover, to scale up the number of qubits, the power consumption of these LNAs should be as low as possible.

For the mentioned quantum computing applications, the first re-configurable cryogenic SiGe HBT based LNA by taking advantage of CMOS integration of BiCMOS process is designed, implemented, and measured in different configurations. The target frequency band in wideband mode is 3-6 GHz. 4.3 K average noise temperature, and 35 dB average gain are achieved at 15 K ambient temperature while the LNA consumed 1.8 mW power. A digitally programmable RLC resonator-based can control the LNA bandwidth and center frequency as a second-order filter response. Moreover, the gain and biasing currents of the amplifier can be tuned and programmed by an on-chip digital to analog converter precisely. The noise performance is maintained with the appropriate choice of settings, and the power consumption is lower than 2.9 mW in all programming states.

Room temperature reconfigurable LNAs have previously been studied. For example, an amplifier whose gain profile was controlled via a tunable transformer was reported in [5]. Another frequency tunable LNA where the response was controlled via transistor sizing was reported in [92]. Moreover, for multi-standard wireless sensor applications to have an LNA with tunable frequency response to avoid wideband LNA and reduce power consumption. Therefore, in [59], authors designed and implemented a band-tunable CMOS LNA based on 45 nm CMOS SOI technology for multi-standard wireless sensor applications. A programmable LC switch tank approach is used to achieve the tunable frequency response. Gain and bandwidth of a distributed CMOS LNA are tuned in [98] by tuning the cascode transistor gate biasing voltage. Also, a field programmable LNA using a tunable N-path notch filter

is described in [99]. In this work, gain, noise figure, linearity, and power consumption can be tuned by using a tunable N-path notch filter and biasing control of TIA.

8.2 Design Approach

Two second-order bandpass filter responses are cascaded to achieve a tunable frequency response for the LNA. The bandwidth, center frequency, ripple, and absolute value of the response can be tuned by independent control of the quality factors (Q_1 and Q_2) and resonance frequencies (ω_1 and ω_2) of the filters. In principle, any second-order bandpass Butterworth and Chebyshev responses can be realized by independently tuning these filters' quality factor and resonance frequency. However, in practice, the achievable range of Q and ω_0 will limit the tunability.

The conceptual design of the proposed amplifier with a parallel RLC resonators is shown in Fig. 8.1 (block diagram) and Fig. 8.2(a). It is a five-stage amplifier with two tunable RLC resonators for frequency response control at stages two and four. The first stage provides wideband gain, and is optimized for noise performance without tunability to avoid any noise penalty because of the following stages' tunability. Buffer stages are incorporated after the tunable second-order-systems to minimize loading effects. Considering only the dynamics of the tunable stages, the gain of the amplifier is approximated:

$$A_v \approx g_{m1}R_1 \frac{g_{m2}R_2}{\sqrt{1+Q_2^2(\frac{\omega}{\omega_2}-\frac{\omega_2}{\omega})^2}} \frac{g_{m3}R_3}{\sqrt{1+Q_3^2(\frac{\omega}{\omega_3}-\frac{\omega_3}{\omega})^2}}, \tag{8.1}$$

where g_{mi} is the transconductance of the stages, R_i is the load resistor of each stage, and Q_i/ω_i are the resonator quality factor and resonance frequency, respectively. It is assumed that g_{mi} of each stage can be tuned via programmable bias. Also, Q_i and ω_i of the second and third stages can be tuned via programmable RLC resonators.

Please note that neglecting of the buffer stages gain in the above equation is just for simplification. A sample plotted voltage gain magnitude of each stage resonator and total gain of the LNA is shown in Fig. 8.2(b) and (c). By tuning the resonator's resistor and capacitor values, each stage quality factor and resonance frequency can be controlled, and, consequentially, the frequency response of the LNA [94]. Fig 8.3 shows example curves demonstrating example responses that can be obtained by varying ω_0 and Q of each stage. These plots are based on the equation mentioned above, and both frequency and magnitude axis is normalized for simplicity.

While on the surface this approach seems straightforward, there are some particular challenges that must be considered for our cryogenic application. First, the noise performance of the cryogenic LNA is sensitive to the interstage matching network between the first and second stages, which, in combination with the available gain of the first stage determines the second stage noise contribution. Since the optimum noise impedance will change as the bias and tuning of the second stage are adjusted, it is essential that the first stage have sufficient available gain to minimize the effect of second stage noise. Second, to realize a narrowband response for the LNA, a high resonator quality factor is require for the resonator. While the inductor quality factor does increase by about 3X with cryogenic cooling [69], it is not enough; therefore, a negative resistor cell to the resonator is added. The noise and impact on linearity of the negative resistor should be considered and simulated for the noise and IP3 performance. Third, since a very high absolute value of gain is required for a cryogenic LNA (30–40 dB), the stability of the LNA should be considered during the design and measurement. Particularly, the negative resistor structure can potentially cause oscillation.

The frequency response tuning idea is implemented for the LNA by designing a programmable RLC resonator, which will be described in the following sections.

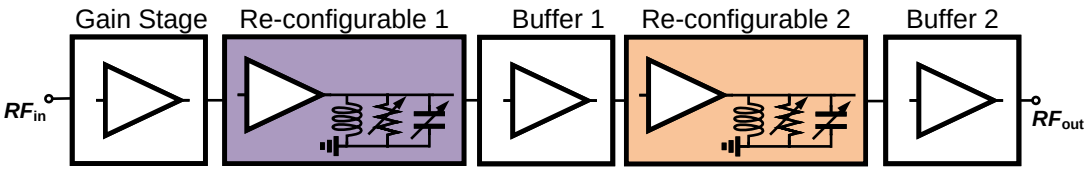


Figure 8.1. Block diagram of the proposed reconfigurable LNA.

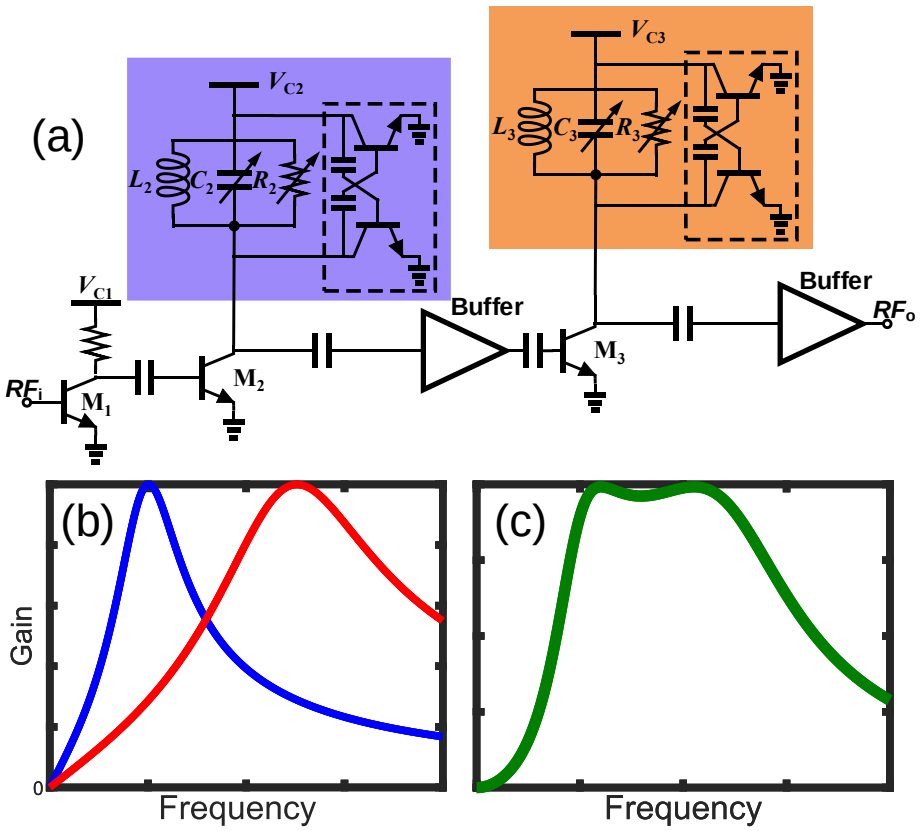


Figure 8.2. (a) Simplified schematic of three stages tunable frequency response LNA, (b) Magnitude of the voltage for second and third stages, and (c) Total frequency response of the LNA.

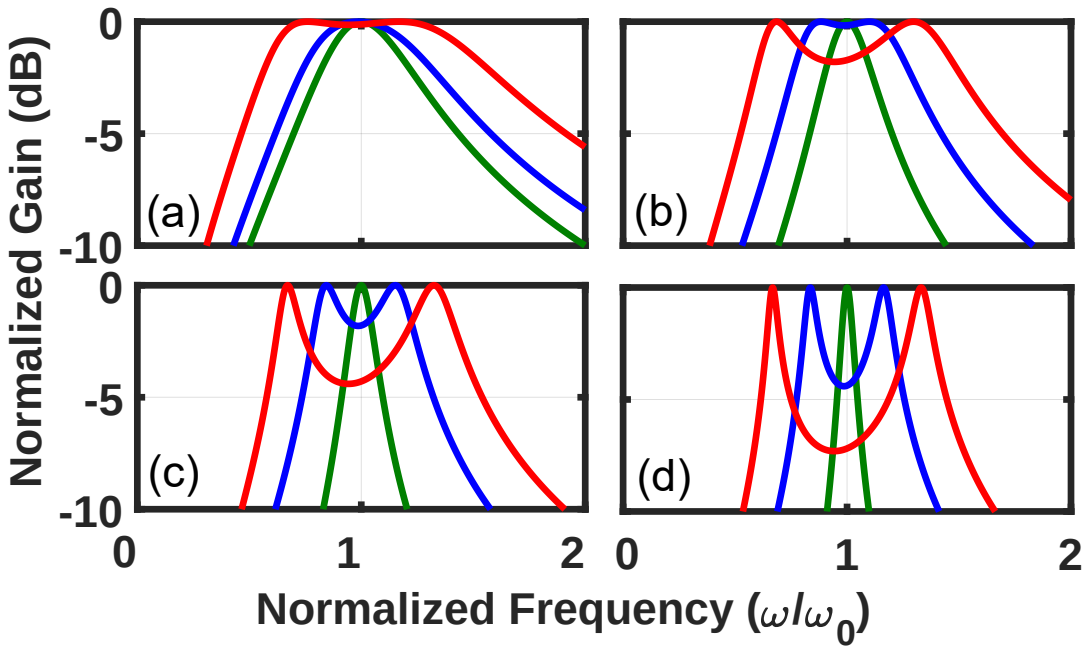


Figure 8.3. Normalized voltage gain of the two stages amplifier with tunable RLC load. (a) Q_1=Q_2=2, (b) Q_1=Q_2=4, (c) Q_1=Q_2=8, and (d) Q_1=Q_2=16 (Red: ω_1=0.66ω_0 and ω_2=1.33ω_0 , blue: ω_1=0.83ω_0 and ω_2=1.16ω_0, and green: ω_1=ω_2=ω_0).

8.3 Programmable RLC Resonator Design

To implement the idea of tunable frequency response, a tunable RLC tank with the ability to program center frequency and quality factor is required. Moreover, the mentioned resonator should be able to perform at cryogenic temperature. The schematic of the proposed resonator is shown in Fig. 8.4. The selected inductor value is 1 nH and a five-bit capacitor bank is used coarse tuning of the resonator center frequency. A six-bit resistor bank (MOSFETs in triode region) is used to achieve wideband (low-Q) response and gain tuning. The values of the resistors and capacitors are binarily weighted, with unit cells of 48 fF and 650 Ω, respectively. A DAC-biased varactors is included to permit fine tuning of the center frequency. The minimum and maximum values of the varactor (at room temperature) are 118 and 316 fF, respectively.

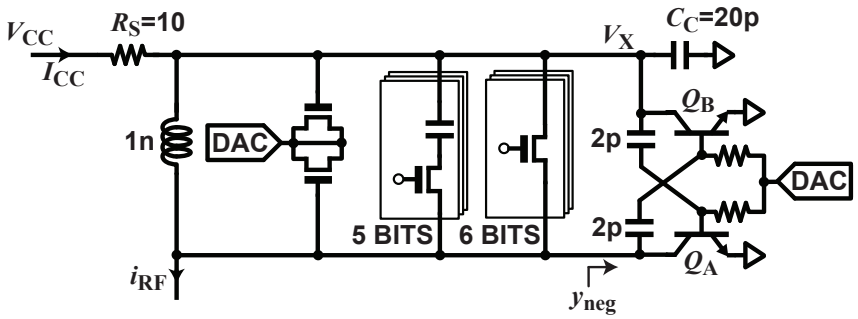


Figure 8.4. Tunable LC tank. The MOS varactor and negative conductance biases are provided by on-chip DACs. The capacitor and resistor banks are binary weighted with LSB values of 48 fF and 650 Ω, respectively.

A negative admittance cell is included to boost the resonator quality factor beyond the limit set by the passive components. The same biasing circuit described in the previous chapter is used to bias the varactor and negative resistor cells. The details and limitations of the design of each part is described in the following subsections.

8.3.1 Tuning Resistor and Capacitor Banks

Five MIM capacitors in series with MOSFET switches are used to provide coarse tuning of resonator center frequency as shown in Fig. 8.5(a). There is a trade-off between quality factor and tuning range ($C_{\max}/C_{\min}$), which should be considered for transistor size selection. A larger switch provides lower ON resistance (higher quality factor) with the cost of limited tuning range. Capacitor values are binarily weighted, and minimum and maximum values of the capacitors are 48 and 771 fF, respectively. Also, the minimum and maximum gate lengths of switches in series with capacitors are 4 and 64 μm, respectively.

The variable resistor is shown in Fig. 8.5(b) and consists of 6 binary-weighted MOSFETs which are operated in the cutoff or triode regions, depending on the programming state. The minimum and maximum size of the transistors are 1 and 32 μm, respectively.

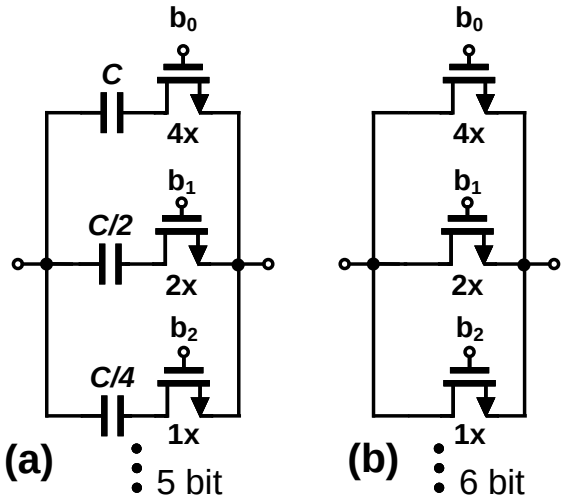


Figure 8.5. (a) 5-bits switch-capacitor tuning circuit. (b) 6-bits resistor bank tuning circuit. Minimum transistor gate width for capacitor and resistor banks are 4 and 1 μm, respectively. Lowest capacitor value is 48 fF.

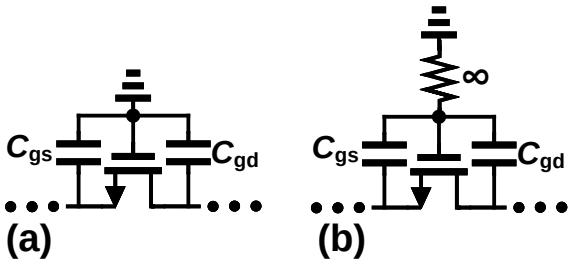


Figure 8.6. Adding series resistor in gate to decrease parasitic capacitors of MOS switch. (a) Gate is directly connected to control voltage. (b) Gate is connected to control voltage via a 20 kΩ series resistor.

A 20 kΩ series resistor is used in the gate of MOS switches to minimize gate-drain and gate-source total parasitic capacitors in the ON-state. Without using the resistor the total parasitic capacitor is $\sim c_{gs}+c_{gd}$ when the switch is ON (Fig. 8.6(a)). However, with adding large enough resistor, the parasitic capacitor will be series and the total is $\sim c_{gs}c_{gd}/(c_{gs}+c_{gd})$ (Fig. 8.6(b)).

8.3.2 Varactors at Cryogenic Temperatures

A programmable MOSFET accumulation varactor is used for fine-tuning of the amplifier's center frequency. The on-wafer performance of the varactor test structure is characterized at cryogenic temperature using a cryogenic probe station. The measured capacitance of the varactor as a function of the control voltage is plotted in Fig. 8.7 for three different temperatures. The minimum achievable capacitance decreases significantly with cryogenic cooling, and consequently $C_{\max}/C_{\min}$ increases. The decrease in $C_{\min}$ with cooling may be related to substrate freezeout and, consequentially, the associated reduction in the substrate contribution to the aggregate capacitance of the varactor. Also, the voltage range over which the varactor is sensitive is decreased and shifted to a higher value, which can be compensated by adjusting the control voltage range.

The circuit implementation of the varactor in the resonator is shown in Fig. 8.8. The same approach of resistive DAC used for base biasing is used to program the control voltage. Also, a 200 kΩ resistor isolates the varactor from the programming circuit and reduces added noise of the digital circuit. A 10 pF capacitor is used to bypass the varactor control voltage.

8.3.3 Negative Resistor

A programmable negative resistor cell is used to provide a higher quality factor for the narrowband response of the LNA. A cross-coupled structure is selected for this purpose. While the topology is similar to a standard differential cross-coupled negative resistance, it is operated in a single ended configuration because of the bypass circuit and thus has a modified operational principle.

The effect of the bypass circuit on the Q-enhance cell is investigated. As shown in Fig. 8.9(a), the admittance of the RLC resonator is a function of the tunable RLC resonator admittance (y_1), Q-enhance cell input transconductance, and bypass

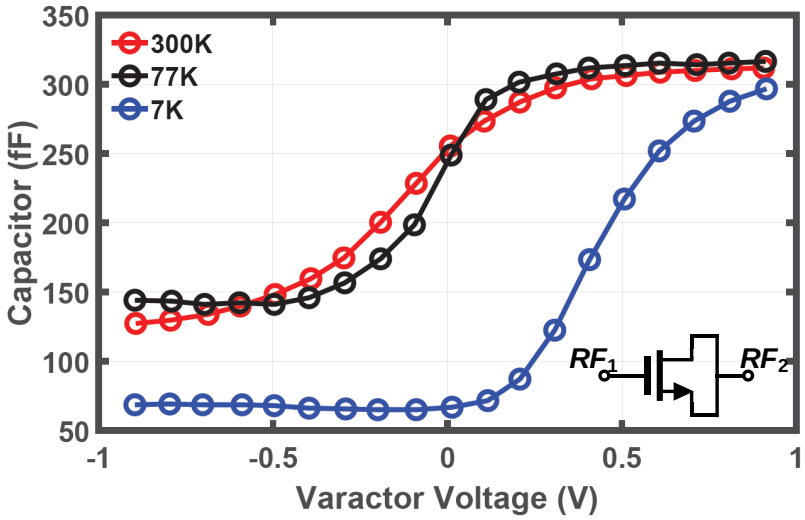


Figure 8.7. On-wafer measured total capacitor of MOS varactor test structure regards to control voltage for different temperatures. The DAC is not included for this measurement.

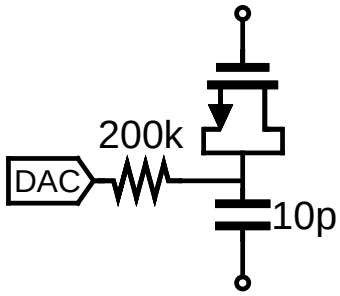


Figure 8.8. Circuit implementation of the programmable varactor used in the tunable RLC resonator.

circuit admittance (y_2). In Fig. 8.9(b), the circuit implementation is shown. The load admittance can be calculated as:

$$y_{\text{load}} = y_1 - \frac{y_1^2}{y_1 + y_2}(1 - g_m z_1)^2, \tag{8.2}$$

in which y_1 is the RLC load admittance, y_2 is the admittance of the bypass capacitor, and g_m is the transconductance of the transistor of the Q-enhance cell. With the assumption of $y_2 \gg y_1$ and $g_m z_1 \gg 1$:

$$y_{\text{load}} \approx y_1 - g_m^2 z_2, \tag{8.3}$$

This can be thought of as a negative inductance in parallel with a negative resistance. The equation implies that the operational mechanism gives both a reactive and a resistive component and the reactive part leads to a frequency shift of the resonance as a function of the negative resistor value. Based on the equation, the magnitude of the resonator impedance regarding the g_m is plotted based on some nominal values of the resonator and bypass circuit in Fig. 8.10. As mentioned, the plot shows that the negative resistor improves the resonator's quality factor while the center frequency shifts lower in frequency.

Given that we are introducing a negative resistance into the circuit, it is important to consider the effect on stability. For the narrow-band response, the parallel negative resistor of the structure can be approximated as:

$$R_p \approx -\frac{(\omega C_s)^2 R_s}{g_m^2}. \tag{8.4}$$

For stability, the value of the parallel resistor should be higher than the real part of the load impedance. This limit defines the maximum g_m of the Q-enhance cell and consequently the narrowest bandwidth of the LNA. In other words, the Q goes

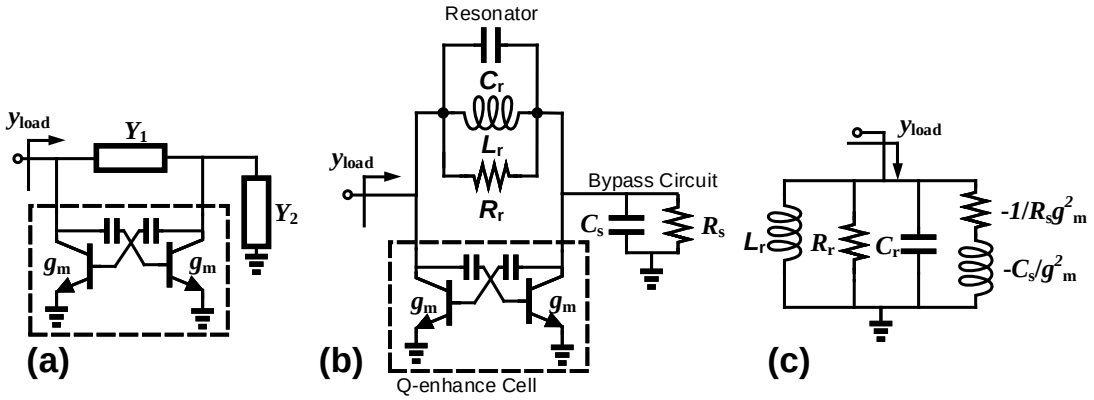


Figure 8.9. (a) Simplified model of RLC tank including negative resistor. (b) Load impedance calculation of RLC tank including negative resistor and bypass circuit. (c) Equivalent load impedance.

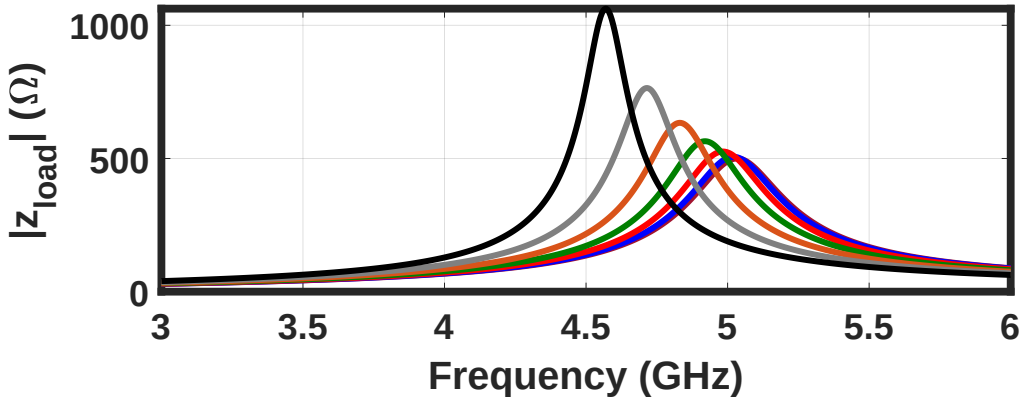


Figure 8.10. Effect negative resistor g_m on magnitude of RLC resonator. (R_r=500 Ω, C_r=1 pF, L_r=1 nH, R_s=10 Ω, C_s=20 pF, and g_m=0–60 mS)

through infinity at the onset of instability. So in principle, one could operate with near infinite Q. However, there are gain fluctuations which start up oscillation. The stability was investigated by looking at k-Δ factors during the experimental results.

8.3.4 Experimental Results of Programmable Resonator

As a backup plan to debug the programmable LNA, four programmable RLC resonators are fabricated based on the mentioned design to verify the resonator's performance at cryogenic temperature. The chip photograph and the corresponding

schematic of one version is shown in Fig. 8.11. The inductor value is 1 nH in all samples, and the varactor minimum and maximum capacitor values are 118 and 316 pF, respectively. The only difference between the samples is the value of the coupling capacitors, which are 0, 13, 88, and 162 fF. In these test structures, the Q-enhance cell could not be used because one side of the circuit is grounded; however, the Q-enhance structure is still there to make sure the parasitic effect of that cell is included in the measurement.

To verify the operation of the programmable resonator, one sample of the resonators is characterized at both room and cryogenic temperatures by a cryogenic probe station. Here the measurement results of the version without coupling capacitor are reported. Some sample measurement results are shown in Fig. 8.12. The input impedance of the resonator is measured while states of the resistors and capacitors are swept. As shown in Fig. 8.12, the quality factor of the RLC resonator has increased with cryogenic cooling. Based on the measured states of the plot, the highest Q for the resistor states at room and cryogenic temperatures are 1.8 and 4.1, respectively. Also, the highest Q of the capacitor states are 2 and 3.1 for room and cryogenic temperatures. Moreover, it is verified that the digital programming circuit is working as expected, and the center frequency and bandwidth of the resonator could be tuned by changing parallel capacitor and resistor values, respectively.

8.4 Amplifier Design, Implementation, and Experimental Setup

Based on the programmable RLC resonator and the biasing approach, A programmable BiCMOS integrated cryogenic LNA is designed and implemented with the capability to tune its specifications digitally. The design and implementation of the LNA, including some cryogenic simulation results, are described below.

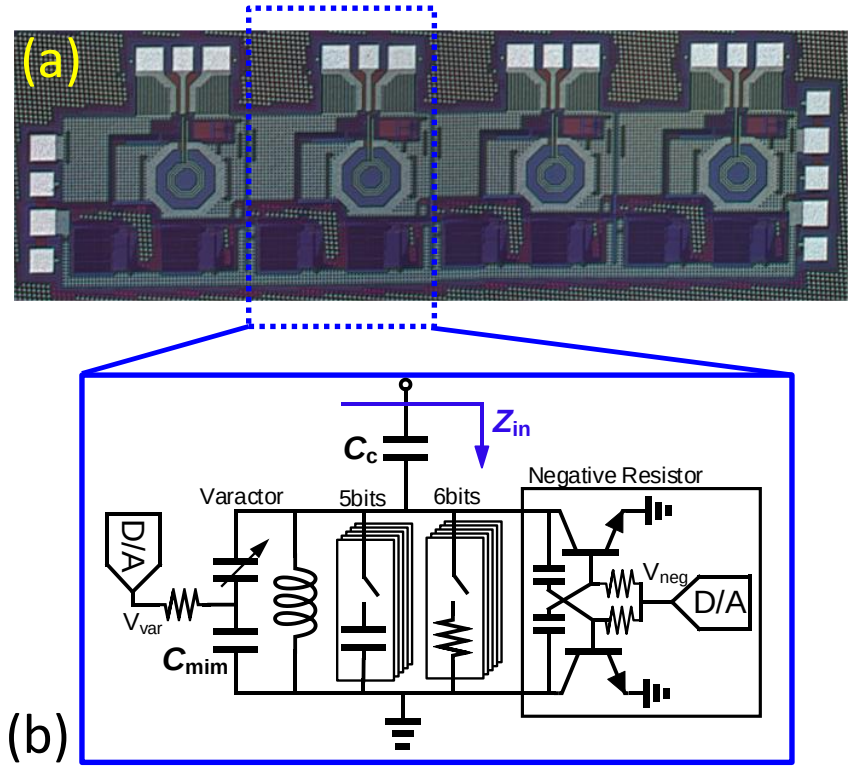


Figure 8.11. (a) Programmable RLC resonators test structure. (b) Correspond schematic design.

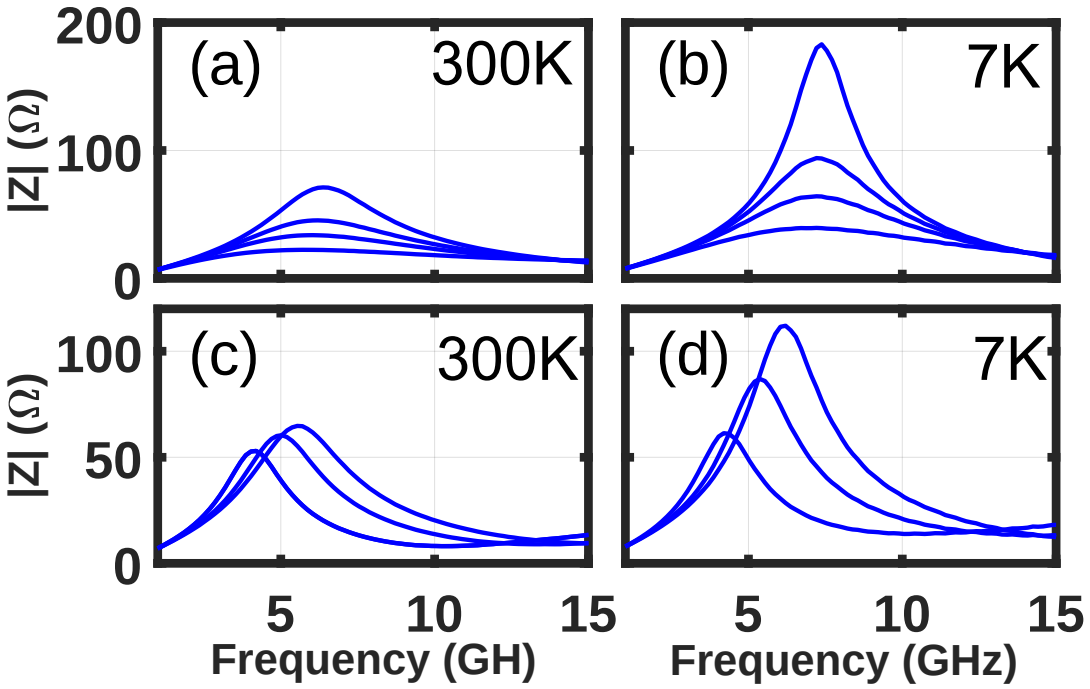


Figure 8.12. Sample on-wafer measurement results of input impedance magnitude of the programmable RLC resonator (the version without coupling capacitor). (a) Different states for the parallel resistor at room temperature. (b) Different states for the parallel resistor at 7 K temperature. (c) Different states for the parallel capacitor at room temperature. (d) Different states for the parallel capacitor at 7 K temperature.

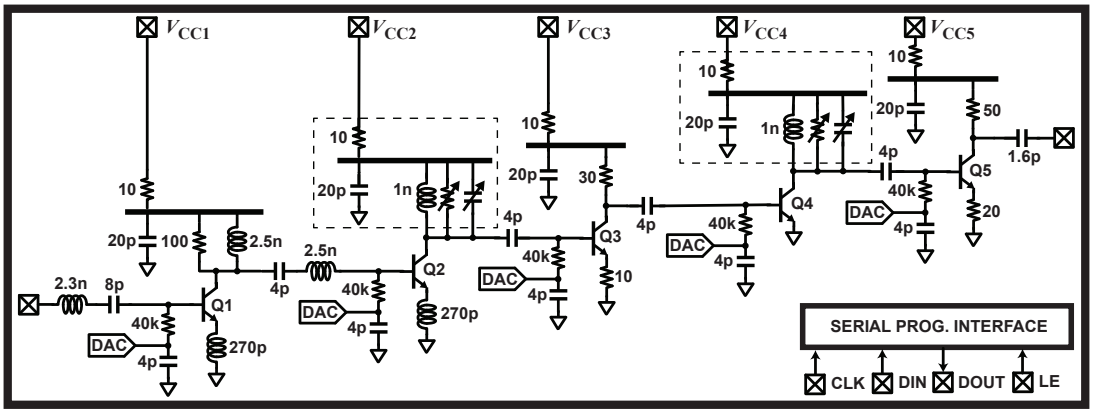


Figure 8.13. LNA schematic. The circuitry in the dashed boxes is further described in Fig. 8.11. Transistor dimensions: $Q_1 : 3\times0.09\,\mu\text{m}\times10\,\mu\text{m}$, $Q_2 : 1\times0.09\,\mu\text{m}\times10\,\mu\text{m}$, $Q_3 : 1\times0.09\,\mu\text{m}\times10\,\mu\text{m}$, $Q_4 : 1\times0.09\,\mu\text{m}\times10\,\mu\text{m}$, $Q_5 : 2\times0.09\,\mu\text{m}\times10\,\mu\text{m}$.

8.4.1 LNA Design

The LNA employs the five-stage architecture shown in Fig. 8.13 to enable the simultaneous realization of low noise and a high degree of tunability over the 3–6 GHz band. The first stage of the LNA (Q_1) is a broadband circuit that was designed to set the noise, the second and fourth stages (Q_2 and Q_4) are reconfigurable second-order systems (SOSs), which can be used to program the frequency response, and the third and fifth stages (Q_3 and Q_5) are broadband buffer amplifiers, used to isolate the two programmable SOSs.

On-chip digital to analog converters (DACs) are used to generate the necessary base-bias voltages. The Tower Semiconductor SBC18S5 process is targeted for this design. Systematic design of the overall circuit was enabled using experimentally extracted small-signal HBT noise models; this process was described previously in Chapter 3. These models also are used in [45]. The cryogenic model parameters of each stage HBT are summarized in Table8.1.

The input stage (Q_1) is a broadband common-emitter design that is tuned to balance gain, noise, and input return loss. When biased at 2 mA ($J_C = 0.74\,\text{mA}/\mu\text{m}^2$), the simulated available gain of this stage is > 13 dB over the entire operating fre-

Table 8.1. Model Parameters at a Physical Temperature of 16 K. Bias current densities are related to the wideband state of the LNA.

Stage	J_C $mA/\mu m^2$	Device Size μm^2	R_B $\Omega \cdot \mu m^2$	R_E $\Omega \cdot \mu m^2$	R_C $\Omega.\mu m^2$	C_{CB} $fF/\mu m^2$	C_{CS} $fF/\mu m^2$	C_{BE} $fF/\mu m^2$	g_m $mS/\mu m^2$	τ ps	β -	r_{be} $\Omega \cdot \mu m^2$
First	0.74	2.7	7.1	2.9	5.4	26.3	6	59.2	104	5.7	3.3e4	37e4
Second	0.55	0.9	8.5	2.9	5.4	26.1	6	43.6	117	1.8	5.3e4	59e4
Third	0.77	0.9	8.1	2.9	5.4	26.1	6	46.5	155	2.4	6.2e4	53e4
Fourth	0.55	0.9	8.5	2.9	5.4	26.1	6	43.6	117	1.8	5.3e4	59e4
Fifth	0.72	1.8	7.5	2.9	5.4	26.2	6	53.2	121	4	4.1e4	43e4

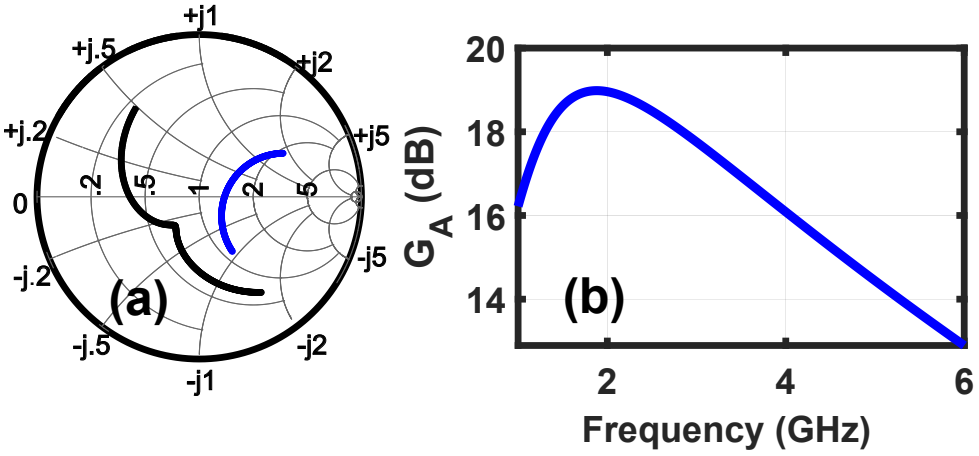


Figure 8.14. (a) Cryogenic simulation noise optimum impedance (blue) and conjugate of the input impedance (black) for 3-6 GHz frequency range. (b) LNA First stage cryogenic available power gain of the LNA. Both of these simulations are when LNA is in wideband state.

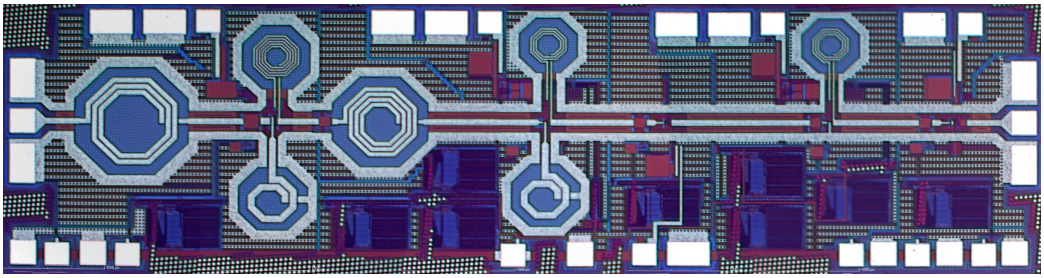


Figure 8.15. Chip micrograph. The chip dimensions are 0.75 mm×2.8 mm.

quency range (see Fig. 8.14(b)), significantly reducing the impact of subsequent stages on the overall noise. Furthermore, this stage does not have tuning capability to avoid any potential effect of the programmable circuit on the LNA noise performance. The cryogenic simulated optimum impedance for the power and noise at 3-6 GHz frequency band is shown in Fig. 8.14(a).

The buffer stages, Q_3 and Q_5, were designed to present well-defined load impedances to the SOSs. Emitter degenerated common-emitter stages were used for this purpose.

8.4.2 LNA Implementation and Experimental Setup

The chip is fabricated based on the Tower Semiconductor SBC18S5 BiCMOS process. This process has seven layers metal stack and minimum 90 nm emitter width for the HBT and 180 nm gate length for CMOS devices. The chip photograph is shown in Fig. 8.15. Standard ground-signal-ground (GSG) bondpads are used for on-wafer measurement and collector biasing pads are on the top side of the chip, and the digital programming required bondpads are on the bottom side of the chip.

The amplifier is assembled inside a coaxial module for cryogenic noise performance characterization. An image of the assembled module and the wire-bonded chip is shown in Fig. 8.16(a) and (b), respectively. Two separated 10 mil thickness RO4003C RF boards are used to transition between chip to SMA connectors, and a standard FR4 board is used as a digital and biasing board. As shown, in Fig. 8.16(b), 10 nF silicon wire bondable capacitors is placed in close proximity to the chip for stability.

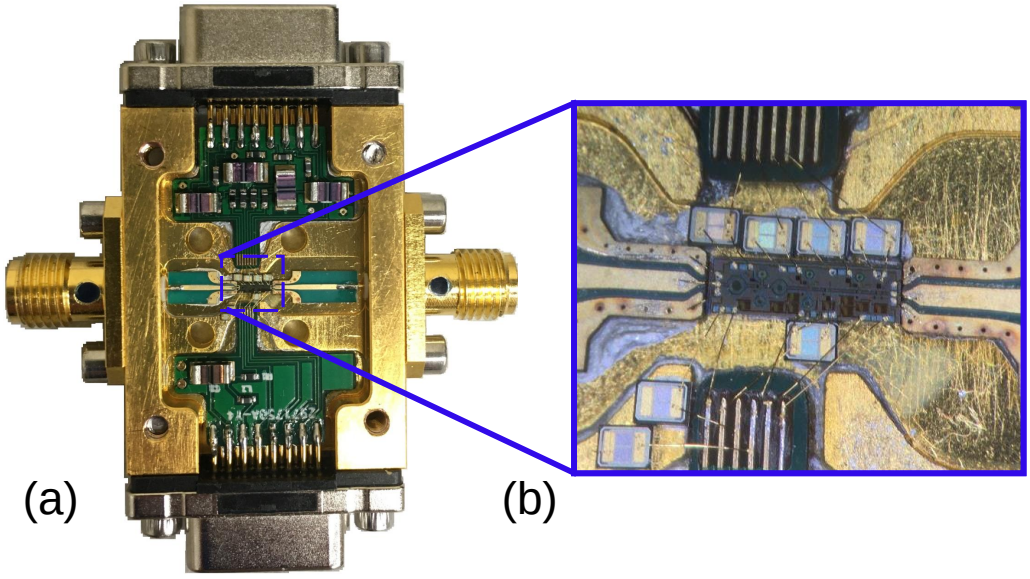


Figure 8.16. (a) The amplifier was packaged within a module for characterization at cryogenic temperatures. (b) Photograph showing the packaged IC. The RF signal enters on the left and leaves on the right. 10 nF silicon capacitors are incorporated in close proximity of the IC to optimize the grounding of the collector biases.

The measurement setup for cryogenic scattering parameters and noise characterizations of the amplifier is shown in Fig. 8.17. The LNA are mounted inside a two-channel custom-built 15 K cryostat. A Raspberry Pi and a level-shifter board are implemented for chip programming and provide a 1.8 V voltage level, respectively. Collector voltages and chip digital V_{DD} are coming from high-resolution power supplies.

The assembled module was characterized using a custom-built cryostat capable of achieving a base temperature of 15 K. This system has a pair of channels configured to measure LNA noise temperature and scatter parameters, respectively. The noise measurement channel is calibrated to an accuracy that is believed to be better than ± 1 K.

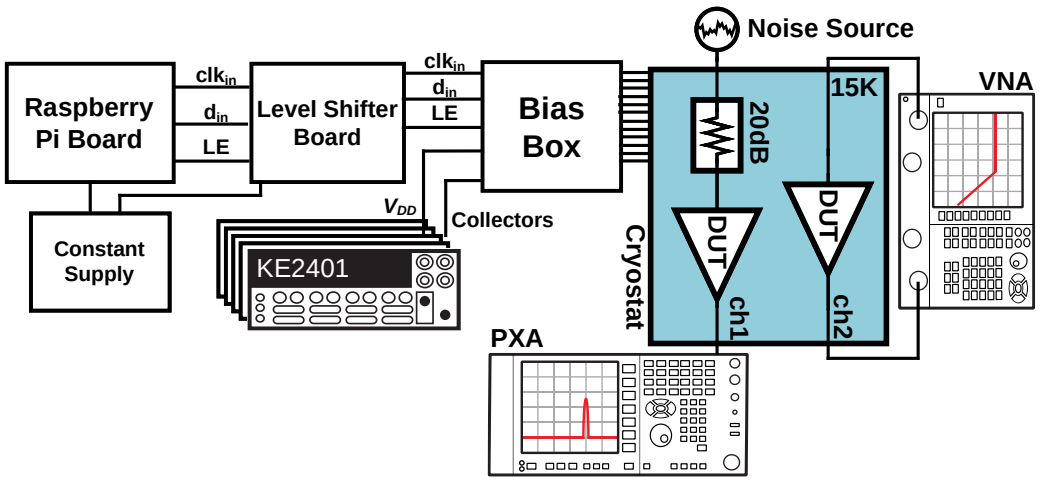


Figure 8.17. The cryogenic measurement setup is used for noise characterization and scattering parameters. Five KE2401 are used in the measurement setup because of DC current sensing requirements of the measurement. However, one supply should be enough because 0.3 V is the common voltage for the collectors.

8.5 Measurement Results

The LNA was first measured in a broadband configuration. The cryogenic noise temperature and gain measurement and comparison with simulation appear in Fig. 8.18. An average gain and noise temperature of 36.1 dB and 4.3 K were observed from 3–6 GHz while the chip dissipated 1.8 mW from 0.3 V collector supply voltage. Moreover, an excellent agreement between cryogenic simulations and measurement is achieved.

Cryogenic input and output matching in wideband mode are shown in Fig. 8.19. Greater than 5 dB input and output return losses were measured over 3-6 GHz frequency band, and the average input and output return losses were better than 10.9 and 11.4 dB, respectively.

Next, the bandwidth control features of the IC is characterized by programming the resistor bank and negative resistor values. Example results are shown in Fig. 8.20(a) and (b). Is is found that it was feasible to reduce the bandwidth from 2.6 GHz to 0.3 GHz with little impact on the mid-band gain or noise and at a modest cost in power consumption, which increased from 1.9 mW in the broadband mode of

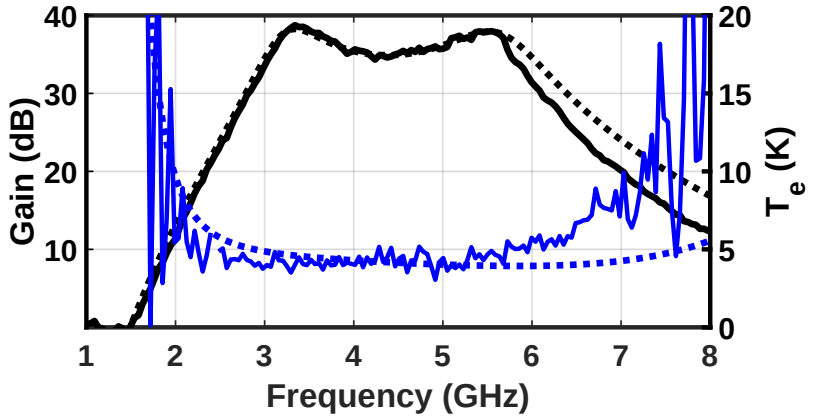


Figure 8.18. Measured (solid lines) and simulated (dotted lines) Gain and noise temperature of the LNA at a physical temperature of 16 K when tuned for wideband operation. In this configuration, the LNA drew 1.8 mW from a 0.3 V supply.

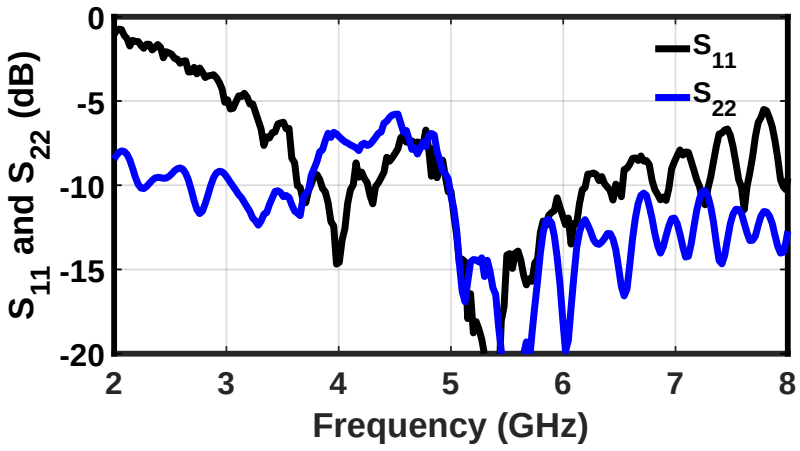


Figure 8.19. Cryogenic measurement of input and output matching in wideband mode.

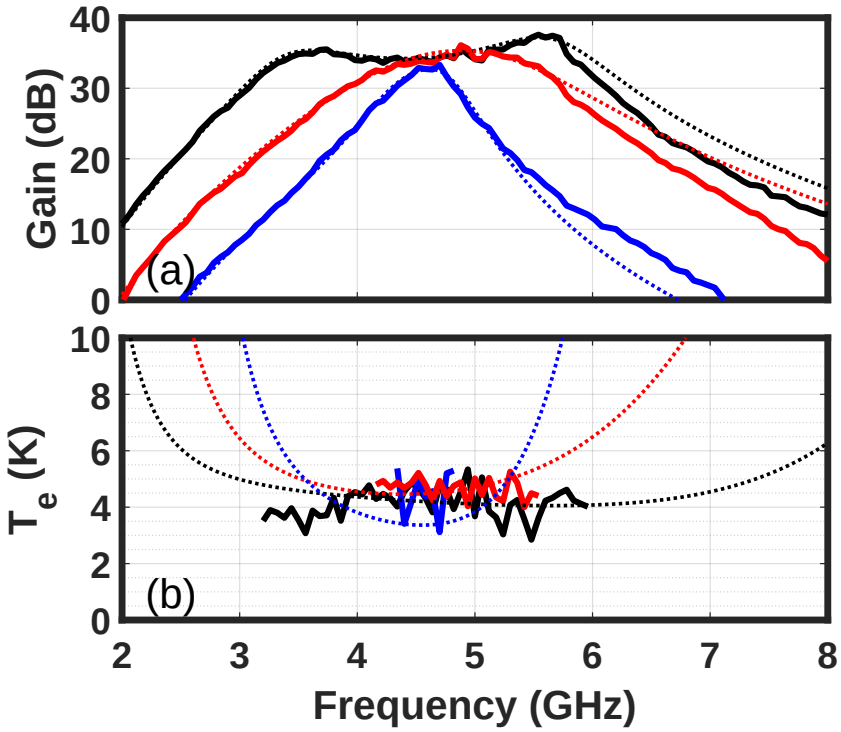


Figure 8.20. (a) Gain and (b) noise simulation (dotted lines) and measurement (solid lines) for the LNA at a physical temperature of 16 K when tuned for different bandwidths. The center frequency for these measurements was set to 4.4 GHz. The power consumed from the 0.3 V supply for the wide-bandwidth, medium-bandwidth, and narrow-bandwidth settings was 1.9, 2.9, and 2.7 mW, respectively.

operation to 2.7 mW in the narrowband operating mode, with the additional power associated with the activation of the negative conductances. In each case, the input and output return losses averaged across the passband were found to be better than 11 and 11.8 dB, respectively. Also, the cryogenic simulations for each measured state are shown in Fig. 8.20.

The center frequency control features of the integrated circuit is also evaluated by programming the capacitor bank and varactors setting, and example simulation and measurement results appear in Fig. 8.21(a) and (b). It is found that tuning the center frequency from 4 GHz to 5.5 GHz had little impact on the noise or power consumption of the IC.

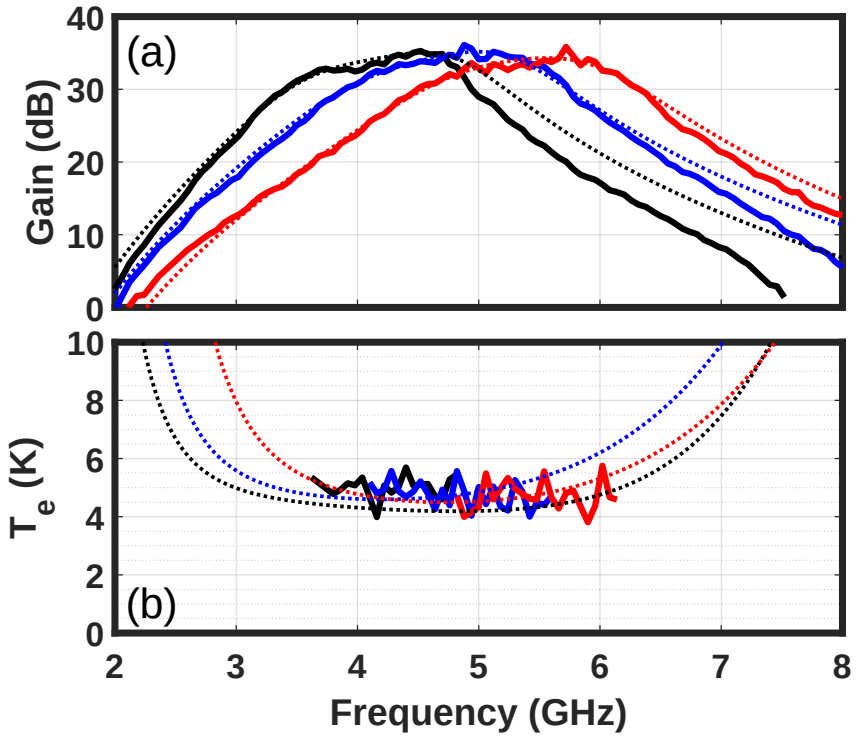


Figure 8.21. (a) and (b) Gain and noise simulation (dotted lines) and measurement (solid lines) of the LNA at a physical temperature of 16 K when configured for different center frequencies. When configured for center frequencies of 4, 4.8, and 5.5 GHz, the chip drew 2.0, 2.2, and 1.7 mW from the 0.3 V supply, respectively.

A similar center frequency control measurement is done while the bandwidth of the LNA fixed to about 250 MHz, and the gain and noise results are shown in Fig. 8.22 (a) and (b). It is found that the entire desired bandwidth could be covered with 250 MHz center frequency steps without affecting the noise performance. Also, input and output return loss and stability factors (k-Δ) are measured for each narrowband state to make sure the LNA is unconditionally stable. Also, the output spectrum of the LNA is checked by a spectrum analyzer to ensure the LNA was not oscillating in different settings.

Next, the average gain of the LNA is characterized with 3 dB steps. Some samples of the measurement results and the corresponding simulations are shown in Fig. 8.23(a) and (b). The average gain for these measurements is 28, 31, and 34 dB without significant effect on the noise performance.

Ripple control of the frequency response is tested to verify of quality factor control of the resonators without affecting the center frequency, and the measurement results are shown in Fig. 8.24. The measured ripple for these plots are 0, 0.1, 1, 2, and 3 dB.

The return losses were found to be configuration-dependent. For the settings corresponding to Figs. 8.20 and 8.21 the worst-case input and output return losses across each passband were in the range of 4.3–8.1 dB and 4.1–6.1 dB, respectively. Also, all reported configurations, the measured input, and output return losses averaged across each passband were better than 10.9 and 11.4 dB, respectively. The cryogenic measurement results of the input and output matching are shown in Fig. 8.25.

The stability of the LNA was also characterized for each of the configurations described above. In each case, it is found that the LNA was unconditionally stable. It should be pointed out that it is found that the LNA could be made to oscillate for large enough values of the negative conductance and avoided those values in experiments.

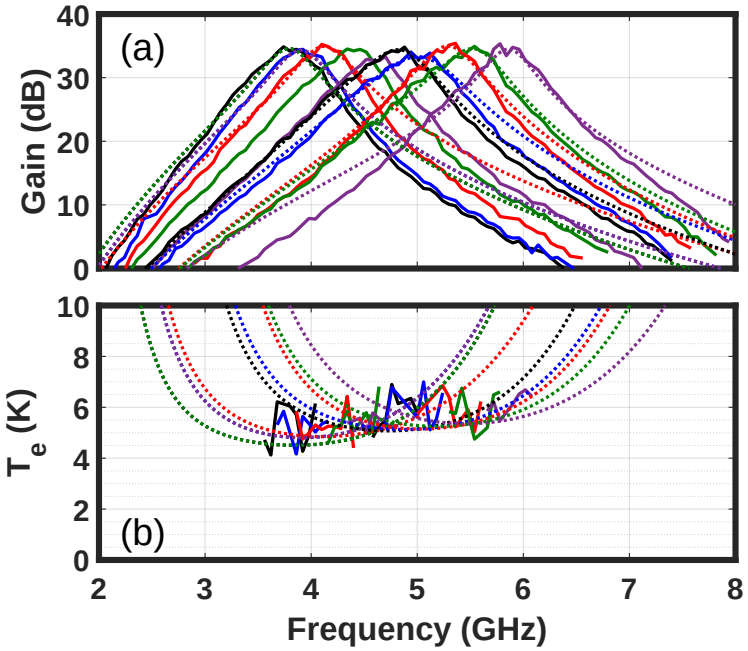


Figure 8.22. (a) and (b) Gain and noise measurements of the LNA at a physical temperature of 16 K when configured for different center frequencies with around 250 MHz bandwidth.

As described in the previous chapter, g_m of the HBT is sensitive to supply changes. During the measurement, it is found that a stable supply for the DACs provides lower gain fluctuation of the LNA. That is a disadvantage of the resistive DAC is that it is very sensitive to noise on the bias line. It was possible to decrease the gain fluctuation by adding a Low-pass filter structure (a series 100 kΩ resistor and a parallel 50 nF capacitor) on the module dc bias board. The author believes this could also be solved by using an LDO.

Finally, the compression characteristics of the IC as a function of frequency under the various modes of operation is characterized. In all cases, it is found that the output referred 1 dB compression point was greater than −30 dBm. This is sufficient for use in quantum computing applications, where input signals are expected to be in the range of −100 dBm.

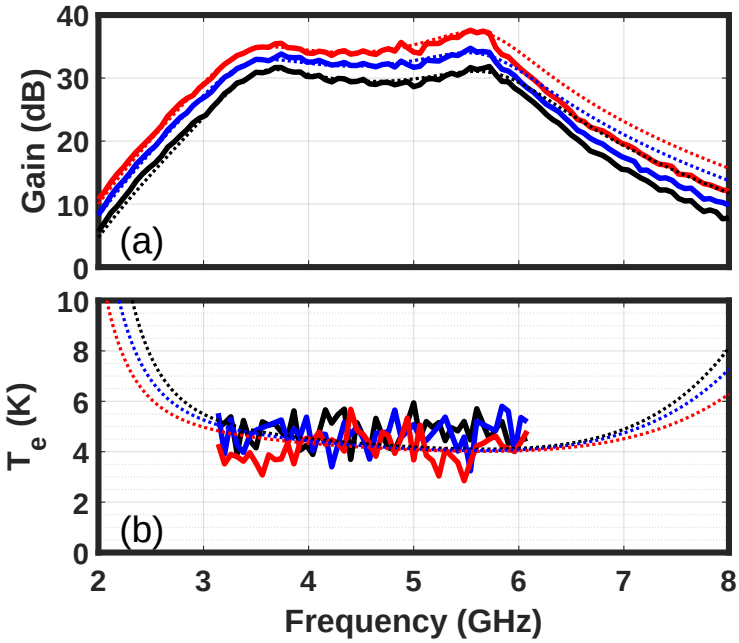


Figure 8.23. (a) and (b) Gain and noise simulation (dotted lines) and measurement (solid lines) of the LNA at a physical temperature of 16 K when configured for different absolute gain values.

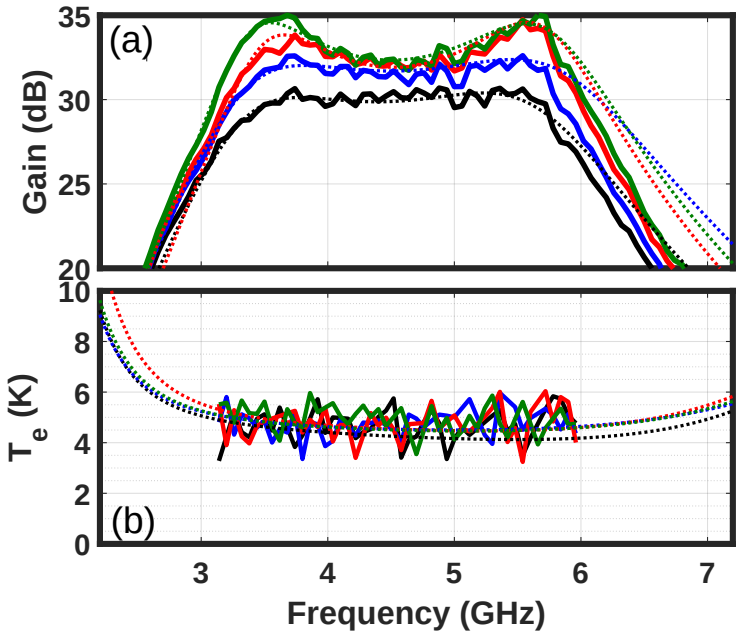


Figure 8.24. (a) and (b) Gain and noise measurements of the LNA at a physical temperature of 16 K when configured for different ripples of 0, 0.1, 1, 2, and 3 dB.

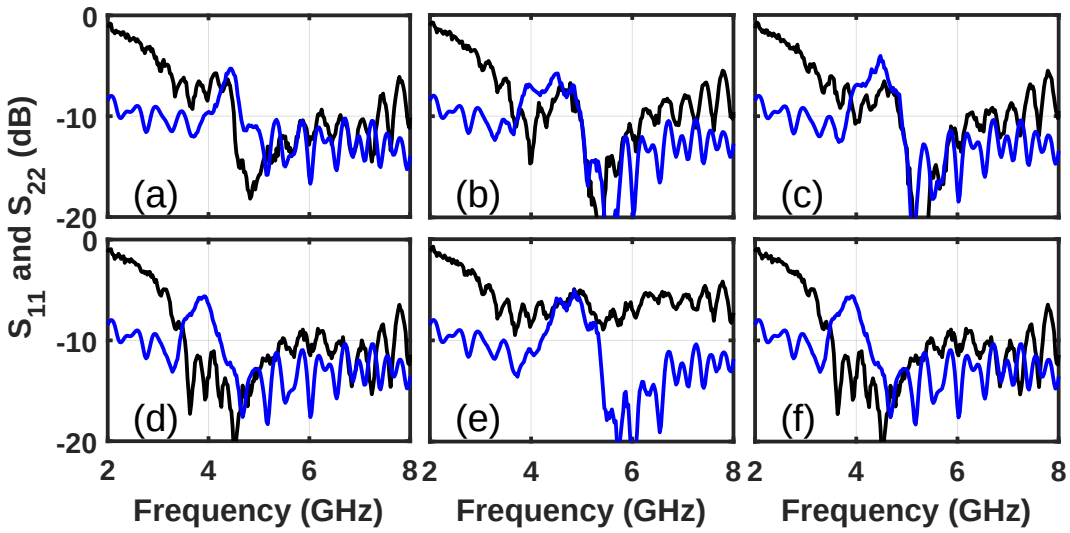


Figure 8.25. Measured S_{11} (black) and S_{22} (blue) at a physical temperature of 16 K when tuned for different bandwidths and center frequencies. Top row: The center frequency for these measurements was set to 4.4 GHz. The power consumed from the 0.3 V supply for the (a) narrow-bandwidth, (b) medium-bandwidth, and (c) wide-bandwidth settings was 1.9, 2.9, and 2.7 mW, respectively. Bottom row: center frequencies of (d) 4, (e) 4.8, and (f) 5.5 GHz, the chip drew 2.0, 2.2, and 1.7 mW from the 0.3 V supply, respectively.

Table 8.2. Comparison with state-of-the-art cryogenic LNAs.

Ref.	Technology	Frequency (GHz)	Gain (dB)	Noise (K)	P_{DC} (mW)	Tunability
[1]	InP-HEMT	4-8	39	2.3	7.7	NO
[95]	SiGe-HBT	4-8	28	3.2	1	NO
[65]	SiGe-HBT	4-8	26	8	0.6	NO
[22]	InP-HEMT	4-8	23	3.2	0.3	NO
This	SiGe-HBT	3-6	36	4.3	1.8	YES

The circuit is compared to state of the art in Table 8.2 for the case of wideband operation (Fig. 8.18). It is competitive with the other results while offering digital programmability.

8.6 Conclusion

The design, implementation, and characterization of a highly tunable cryogenic LNA is presented. In addition, a programmable RLC resonator is proposed to realize a frequency tunable cryogenic LNA. While the results shown here are pretty promising, there are several areas in which further work is warranted. First, the noise performance achieved and power consumed by this design is still higher than the state-of-the-art for SiGe cryogenic LNAs, so the demonstration of reconfigurable cryogenic LNAs which approach or exceed the state-of-the-art in these metrics is an important goal. Secondly, the demonstrated circuit required a stable external supply for the DACs, and a future design should include on-chip regulation for this task.

CHAPTER 9

CONCLUSION AND SUGGESTIONS FOR FUTURE WORK

9.1 Conclusion and Summary

SiGe HBT based cryogenic LNAs provide an excellent trade-off between power consumption and noise performance, which is used to satisfy readout requirements for different applications such as terahertz detection and quantum computing. To verify that, in this dissertation, three state-of-the-art SiGe technologies are characterized and modeled cryogenically, and several integrated circuit LNAs are designed and measured.

The first LNA satisfies the readout requirement of MKID arrays as an incoherent detector-based mm-wave length camera. Moreover, an array of 16 LNAs, including a servo bias system, is implemented and deployed within the camera. Additionally, two wideband and low-power integrated circuit LNAs are designed and measured, targeting coherent detector applications. By achieving a promising compromise between power consumption, bandwidth, and noise temperature, it is verified that SiGe HBT based LNA is also promising in wideband design, particularly for the $<10\,\mathrm{GHz}$ frequency range.

Biasing integration of cryogenic LNA is highly desired to improve the scalability of these LNAs. By taking advantage of the CMOS integration capability of the SiGe process, an on-chip base voltage biasing approach using a cryogenic DAC is described and verified. All base voltages can be biased-up with an unregulated power supply while a high-resolution power supply had been required before for each stage base biasing of the LNA.

Finally, the first re-configurable BiCMOS LNA, which it can be programmed digitally for different specifications, is designed, implemented, and measured. The LNA frequency response factors, including absolute value of gain, bandwidth, center frequency, and ripple, can be tuned by digital CMOS circuitry. Also, the DC collector current and base voltage bias of this LNA can be tuned and programmed at cryogenic temperature with the mentioned approach. The amplifier can be programmed to achieve the lowest noise temperature published for silicon-based integrated circuits. The LNA tunability is based on a programmable RLC resonator which is cryogenically characterized as an independent test structure.

9.2 Suggested Future Work

An on-wafer cryogenic noise measurement approach can be a great future work to minimize the parasitic packaging effect on cryogenic noise characterization. Currently, the cold-attenuator method is the conventional approach for cryogenic noise characterizations. On-wafer noise measurement requires a chip attenuator with a precise cryogenic model. Heat loading of probes can be a challenge to find the exact temperature of the attenuator to create the model. An on-chip temperature sensor could be a possible solution that needs to be studied. Moreover, the attenuator and LNA should be on the same wafer with minimum distance to minimize the wirebond and pad parasitic effects.

Quantum computing readout requires a few photon limited noise performance for the cryogenic LNA while the LNA consumes sub-milliwatt DC power. One future work might be to develop an ultra-low-noise and low-power cryogenic LNA, which is near to quantum limit noise performance. A noise-optimized SiGe process with Germanium doping can be a potential solution to achieve the goal.

Scaling up the number of array elements in qubits and THz detector readout requires thousands of LNAs that must be biased simultaneously. To achieve the

minimum power consumption for each LNA, the collector voltage of different stages needs to be biased up independently. Having an on-chip low-power circuitry approach to bias up base and collector simultaneously is essential to optimize the power consumption. Using an on-chip servo bias loop can be a suggested method. However, low-frequency stability and added noise of the loop at cryogenic temperature need to be studied to use this approach.

The shot noise correlation factor between base and collector shot noise sources is neglected for the SiGe HBT small-signal model used in this dissertation. This approximation can be valid for the frequencies below 10 GHz. However, this approximation should be considered during modeling to have accurate cryogenic noise models for the simulations, especially for above 10 GHz applications.

The nonlinear cryogenic model of SiGe HBT has not been studied intensely in situ based on the author's knowledge. However, these models are studied for MOS devices at cryogenic temperature [42]. Furthermore, cryogenic linearity simulations are helpful for specific applications like MKID readout when the intermodulation of input probe tones can limit the readout performance, as mentioned in chapter 4 of the dissertation.

The cryogenic characterization of the varactor is done, and it is found that both effective voltage range and $C_{\max}/C_{\min}$ are changed with cryo cooling. Study of the varactor cryogenic behavior and model creation will be helpful for the next reconfigurable LNAs.

APPENDIX A

DE EMBEDDING TEST STRUCTURE PARASITIC

Different approaches are reported for de-embedding in the literature [57, 87, 51]. A method is selected by using Open, Short, and Pad-open test structures [89]. The model which was used for test structures is shown in Fig.A.1. Y_i and Y_o are pads parasitic capacitors (in parallel with a resistor at room temperature). Y_f is a pad-to-pad parasitic capacitor that can be negligible. Z_1 and Z_2 are mainly because of transmission lines parasitic inductors (in series with a resistor in room temperature). Y_3 is a parasitic capacitor of HBT layout wiring. Z_3 is because of ground loop back parasitic. Finally, Y_1 and Y_2 is substrate parasitic capacitor because of layout wiring of HBT. Please note that lumped component fitting was not used for the parasitic elements, and each element is de-embedded as a 2-ports matrix.

Pad-open, short, and open are required to obtain the Y-matrix of the device under test (DUT), as shown in Fig.A.2. Thus, it can be shown that Y_{DUT} can be calculated as:

$$Y_{\mathrm{DUT}} = [(Y_{\mathrm{meas}} - Y_{\mathrm{pad}})^{-1} - (Y_{\mathrm{short}} - Y_{\mathrm{pad}})^{-1}]^{-1} - [(Y_{\mathrm{open}} - Y_{\mathrm{pad}})^{-1} - (Y_{\mathrm{short}} - Y_{\mathrm{pad}})^{-1}]^{-1}, \tag{A.1}$$

where Y_{meas} is Y-matrix of the measured sample and Y_{DUT} is de-embedded Y-matrix of the sample. The above formula modeling de-embedding was used.

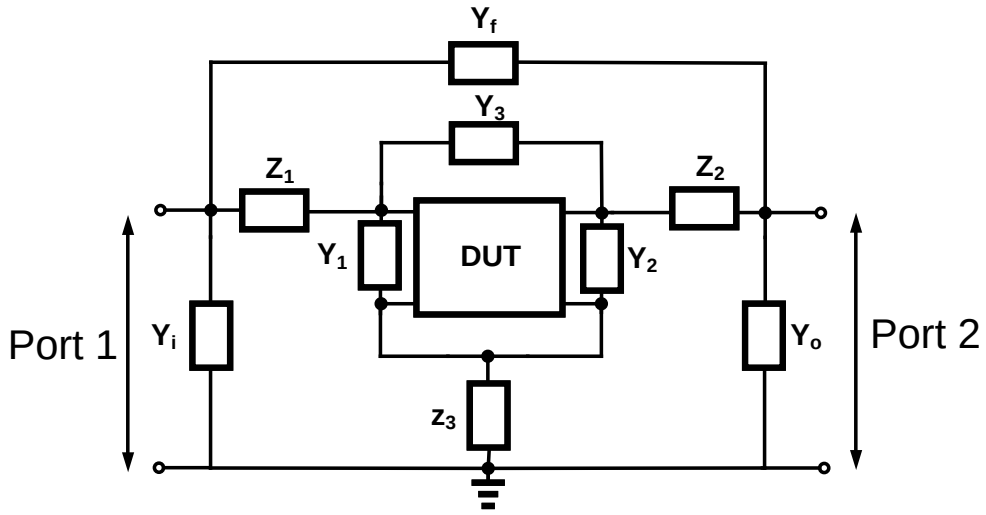


Figure A.1. Sample DUT model including parasitic components of test structure.

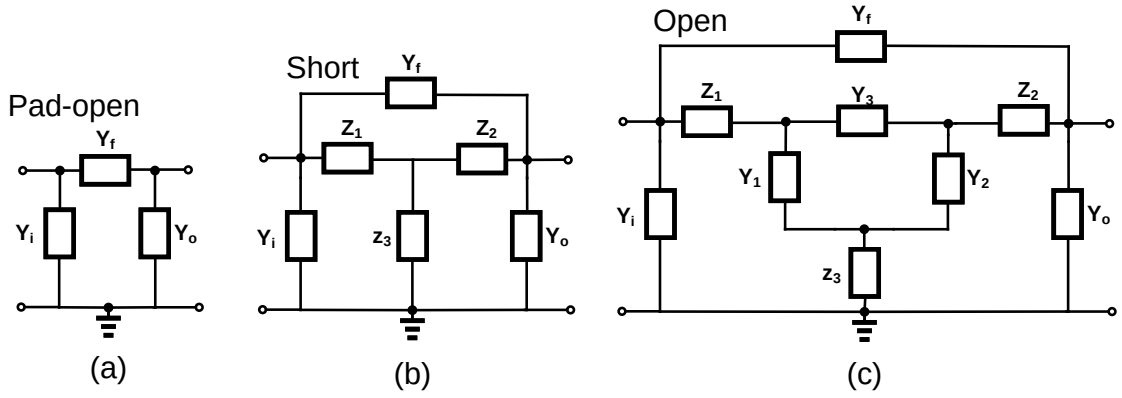


Figure A.2. De embedding test structures model. (a) Pad-open (b) Short (c) Open.

APPENDIX B

DE EMBEDDING OF DC RESISTANCE

As discussed in the modeling chapter, two small-signal model parameters of SiGe HBT, r_e, r_c, are obtained from open-collector measurement, a DC measurement. Having precise values for these extractions is essential. Particularly, dropping the voltage on r_e is affecting on g_{m}, and consequently causes a gain mismatch in LNA's gain simulation. This is even more effective in high current density design. Moreover, in common-emitter topology, the thermal noise of r_e can be referred to the input without any division factor. That is why DC resistors of the measurement setup, including RF cables, probes, and test structures were de-embedded .

These resistors can be measured and extracted through Z-matrix measurement of the short test structure. DC model of short test structure is shown in Fig. B.1(a). Z_A, Z_B, and Z_C can be written as:

$$Z_{11} = Z_A + Z_C = \frac{dV_1}{dI_1}|_{I_2=0}, \tag{B.1}$$

$$Z_{22} = Z_B + Z_C = \frac{dV_2}{dI_2}|_{I_1=0}, \tag{B.2}$$

$$Z_{21} \approx Z_{12} = Z_C = \frac{dV_2}{dI_1}|_{I_2=0}, \tag{B.3}$$

when the Z-matrix of the short test structure is calculated, Z_{ij} parameters can be obtained from the above equations, and DC resistance can be de-embedded based on Fig. B.1(b).

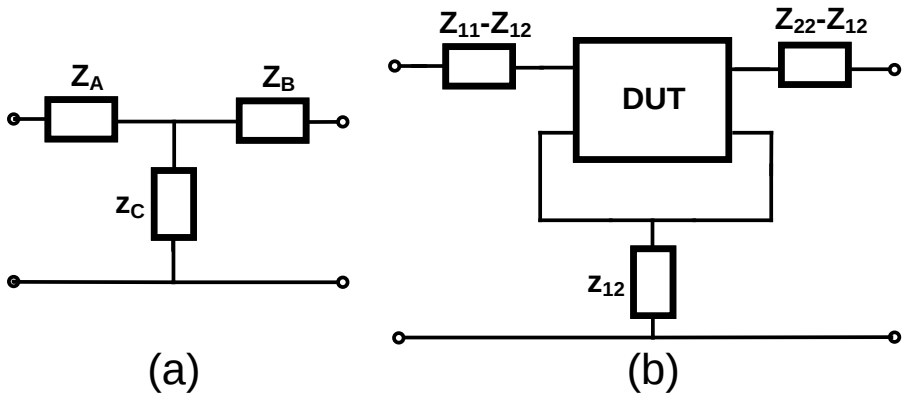


Figure B.1. De embedding of measurement setup DC resistance . (a) DC model of short test structure (b) Resistance de embedding based on short test structure.

APPENDIX C

SERVO BIAS BOARD STABILITY ANALYSIS AND SIMULATIONS

The Equation 5.4 can be used to calculate collector current as a function of $V_{\mathrm{ref_B}}$, and it shows by increasing the instrumentational amplifier gain, resolution control and loop-speed can be increased simultaneously. However, since instrumentational amplifiers have limited gain-bandwidth (it can be modeled as a single-pole amplifier), the amplifiers' limitations should be considered a design part. For example, for the amplifier used as an instrumentational amplifier, the bandwidth for voltage gain of 10, 100, and 1000 are 30, 3, and 0.2 kHz, respectively. This limited gain-bandwidth of the amplifiers affects on stability.

The gain of both instrumentational amplifiers is 10 in our servo loop. So, there are two 30 kHz poles in our circuit which decreases the phase margin and potentially causes oscillation. Please note the second pole of the integrator happens in a significantly higher frequency than 30 kHz. So, the effect of that pole on the phase margin can be neglected.

Starting phase of open-loop gain is -90° because of the integrator pole. Two poles at 30 kHz (two instrumentational amplifiers with the gain of 10) cause another -90° phase at this frequency. Therefore, the total phase of the open-loop gain is -180°, and during the design, the magnitude of the open-loop gain should be lower than one in 30 kHz. This frequency is a limit for the loop-speed of the servo bias. In the design, the loop gain is one at 2 kHz which tells the designed bias loop is stable with enough margin.

The open-loop phase margin formula in the loop can be approximated as:

$$\text{P.M.} \approx 90^\circ - 2\arctan\frac{\omega_n}{\omega_p}, \tag{C.1}$$

where ω_n is the gain-bandwidth of the loop, and ω_p is pole locations of the instrumentational amplifiers. The equation shows the trade-off of phase margin, loop speed, pole locations of the instrumentational amplifiers.

We have used transient single-pulse simulations for examining the stability of the servo bias loop. The results are shown in Fig. C.1. Collector current is plotted as a function of time for different values of SiGe HBT g_m. g_m =0.4 S is chosen for the simulations, which is the same value as the first stage of the LNA for cryogenic simulations. This simulation is carried out by LTspice, and an ideal voltage-dependent current source is used as the HBT model. Voltage gain of both instrumentational amplifiers are 10 and R_{sense}=10 Ω. As shown, the bias board is stable even with 3.3 times cryogenic g_m.

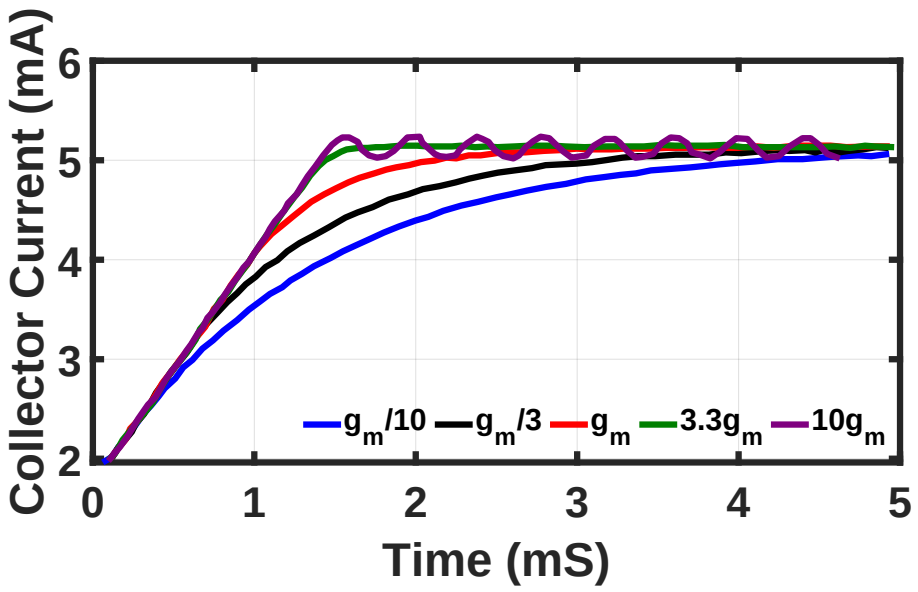


Figure C.1. Time-doamin collector current as a pulse response of $V_{\mathrm{ref_B}}$ for different values of cryogenic g_m. R_{sense}=10 Ω, g_m=0.4, and instrumentational amplifiers voltage gains are 10.

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