Front-End Electronics of the ALICE dimuon trigger

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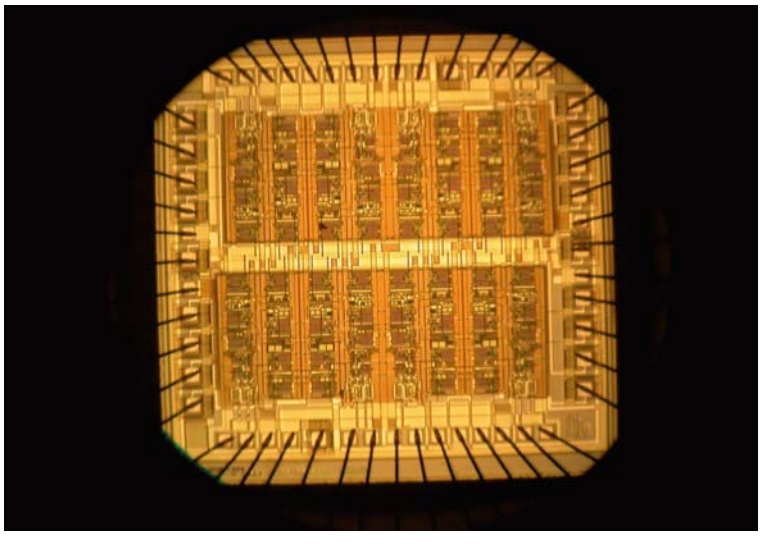
Abstract

This document presents the design and performance of the Front-End Electronics (FEE) developed for the ALICE dimuon trigger operating with Resistive Plate Chambers (RPCs) in streamer mode. This electronics, yet ready for production, is based on a dedicated ASIC designed at LPC Clermont-Fd.



Picture of the front-end ASIC

Contents

1 Introduction

ALICE [1] (A Large Ion Collider Experiment) [1] is the only one detector dedicated to nucleus-nucleus collisions at LHC (the Large Hadron Collider) which is foreseen to start running in year 2007.

The forward part of ALICE consists of a dimuon spectrometer [2] which is aimed to study the charmonium and bottomium decay in the $\mu^+\mu^-$ channel. Indeed, their yield in heavy ion collision should provide a clear signal for the QGP (Quark-Gluon Plasma) formation which is expected to occur according to lattice QCD (Quantum Chromo-Dynamic) calculations.

The general setup of the dimuon arm is displayed in figure 1.

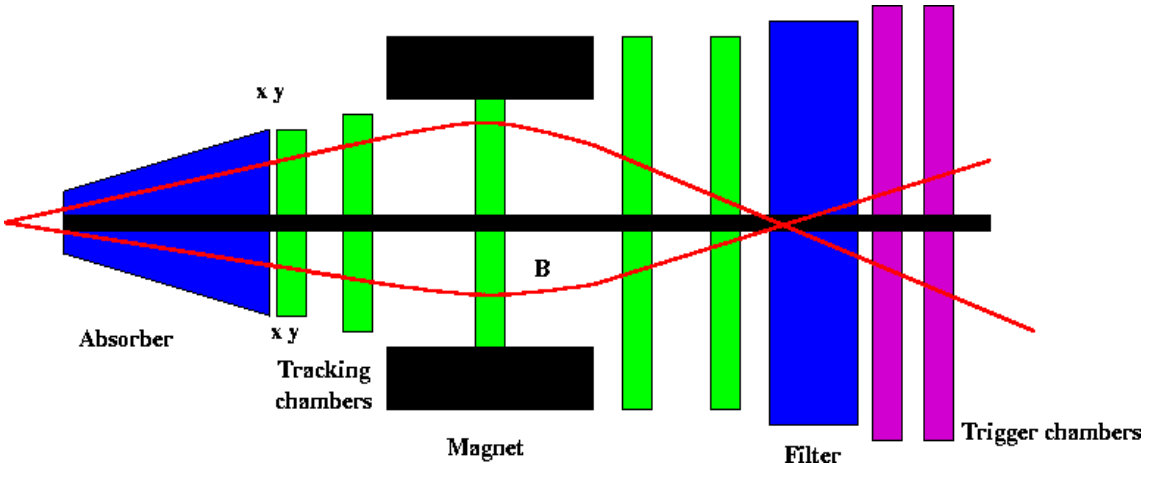


Figure 1: Layout of the forward dimuon spectrometer of the ALICE experiment.

Its angular acceptance is $2^\circ < \theta < 9^\circ$ corresponding thus to the pseudo-rapidity range $2.4 < \eta < 4$. It consists of a front and small angle absorber, a large dipole magnet, ten high granularity tracking chambers, a muon filter and a trigger system.

The dimuon trigger is included in the level 0 ALICE trigger (L0). It enables to select events containing muons in the forward direction. An online cut on transverse momentum ($p_\perp$) is applied on the charged particles reaching the trigger chambers.

A dedicated trigger electronics based on a geometrical algorithm is developed for this goal.

The trigger system consists of two $\approx (6 \times 6)\,\mathrm{m}^2$ area stations, called MT1 and MT2, located approximatively 16 m and 17 m from the interaction point. Each station is made of two RPC planes (Resistive Plate Chambers[3]) which are readout in X and Y directions with a Front-End Electronics (FEE) amounting to 20992 electronics channels.

The role of the FEE is to transmit a logical signal to the trigger electronics when a valid analog pulse has been read on the corresponding channel, as illustrated in figure 2.

The goal of the present document, prepared for the Production Readiness Review (PRR) of the FEE, is to give a detailed status report of the FEE in view of its production for the experiment.

[1] The main acronym used are reported in a Glossary at the end of the document.

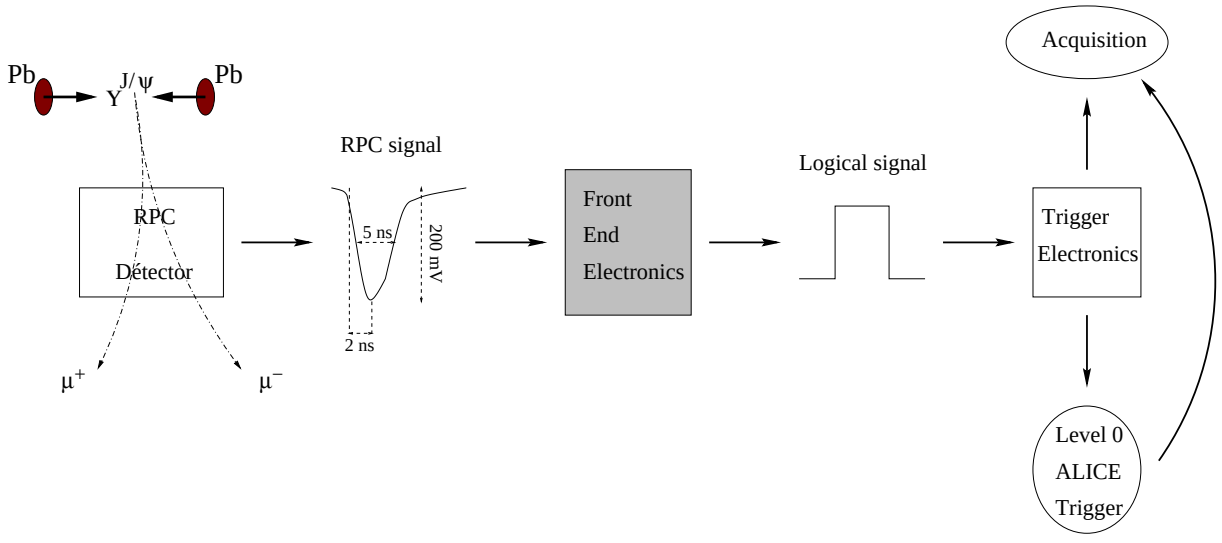


Figure 2: Role of the Front-End Electronics (FEE) of the ALICE dimuon trigger.

This PRR begins with an overview that the FEE must fulfill. The electronics is then described in two steps: the ASIC especially designed for this application and its implementation on boards. Next, general considerations about grounding, power supply and Detector Control System (DCS) are discussed. A summary of all the tests performed both in laboratory and using beams at CERN is given. Finally, the test bench designed to check the characteristics of the whole production is described.

2 General presentation and environment

2.1 RPC pulses

The single 2 mm gas gap RPCs [4] (fig. 3) operate in streamer mode. The choice of the bakelite electrode resistivity (around $10^9\,\Omega$.cm) and the gas mixture (49% Ar + 7% $i C_4H_{10}$ + 40% $C_2H_2F_4$ + 4% SF_6) have been optimized in beam tests. At present, the fraction of SF_6 has been decreased to 1 % to improve the aging of the RPCs.

These characteristics allow to reach a good efficiency (about 98 %) up to a rate of 500 Hz/cm^2, well above the expected maximum flux of particles in nucleus-nucleus collision at the LHC, which is about 40 Hz/cm^2 [2]. The best tuning for efficiency is achieved with a high voltage (HV) at 400 V above the "knee", that is typically about 8 kV (with 1% SF_6), fixing thus the normal operating conditions for these RPCs.

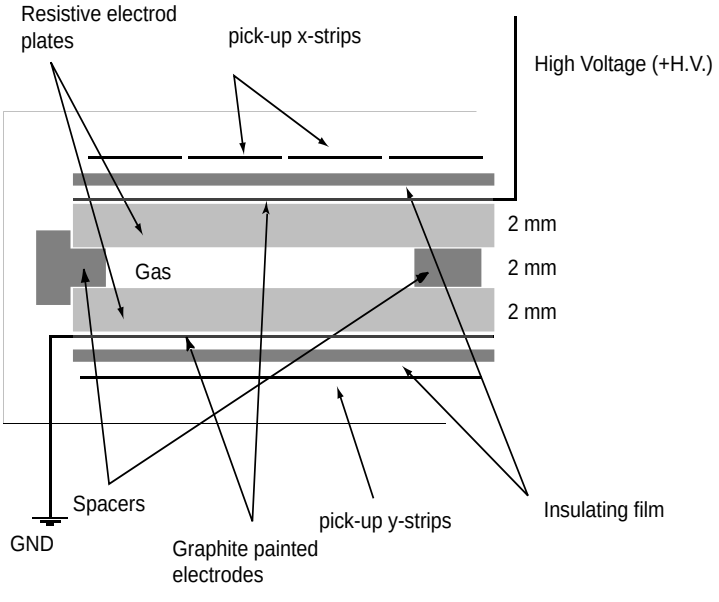


Figure 3: Cross-section of a Resistive Plate Chamber (RPC) used in the ALICE dimuon trigger system.

Examples of pulses developed with this type of RPC are displayed in figure 4. It appears that the pulse shape in streamer mode has the following features (see ref. [7] for more details).

- A first peak, called precursor in the following, is fixed in time relatively to the passing time of the particle through the chamber:
  - 2 ns rise time (typ [2]),
  - 5 ns width (typ),
  - (20 – 50) mV amplitude (typ).
- A second peak, called streamer in the following, which may be delayed from the precursor by several nano-seconds (delay denoted by Δt_{p-s}):

[2] typ: typical value.

– 2 ns rise time (typ),

– 5 ns width (typ),

– $(100 - 200)$ mV amplitude (typ), some pulses may reach several volts.

The mean value of the delay between the precursor peak and the streamer peak depends on the high voltage applied to the RPC. In normal operating conditions of the RPC, the fraction of events with a streamer delayed by more than 15 ns is quite small (about one percent).

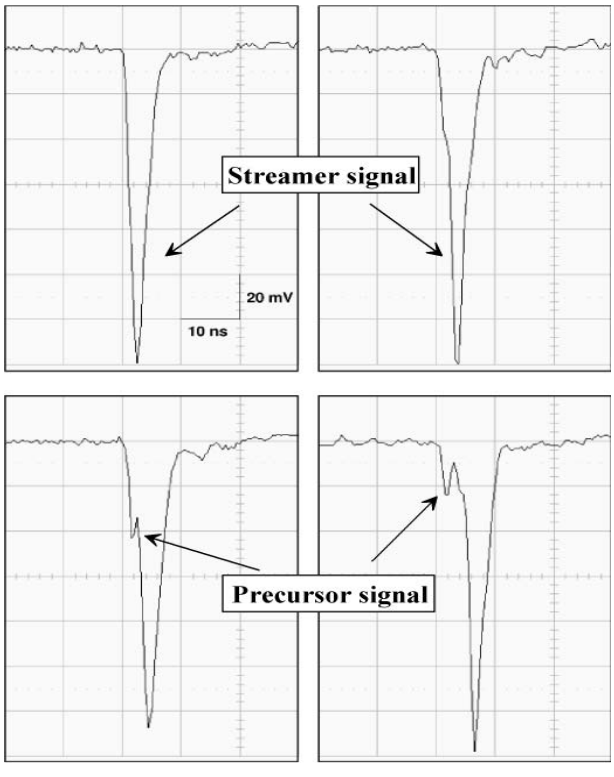


Figure 4: Typical pulses picked-up on a single gas gap RPCs operating in streamer mode, with a digital oscilloscope (1 GHz bandwidth) via a short BNC cable (50 Ω impedance).

2.2 Mechanical layout

The two trigger stations, called MT1 and MT2, are composed of two chamber planes. Each half chamber plane is made of 9 independent RPC modules, namely 72 modules at total, equipped of X and Y strips on each side as displayed on figures 51 and 52 (see appendices A).

Figures 51 and 52 display also the layout of different types of strips whose characteristics are given in table 1. The number of strips amounts to 20992 for the whole trigger system.

The distance between the two stations is of 1 m, while the distance between the two planes inside a station is 17 cm. Thus there is about 6 cm free space between two chamber planes of the same station.

Table 1: Total number of strips as a function of their pitch and their orientation X or Y, the numbers being the same for the two stations MT1 and MT2. The length of the strips varies from 170 to 720 mm.

		Strip X (horizontal)			Strip Y (vertical)	
Strip pitch (mm):	MT1	10.625	21.25	42.5	21.25	42.5
	MT2	11.3	22.6	45.2	22.6	45.2
Number of strips		3840	8448	2688	3584	2432
Total		14976			6016	

2.3 Trigger electronics considerations

The trigger electronics is divided into three parts: local (234 boards), regional (16 boards) and global (1 board).

The main function of the local trigger is to do a backup of all signals coming from the RPC strips (sequence called bit-pattern) in a pipeline memory, and to identify single tracks with $p_\perp$ above pre-defined cuts by using a dedicated trigger algorithm.

The regional and next global electronics collect the information from the local boards in order to select dimuon or single muon events. This final decision has to be delivered to the general ALICE L0 trigger < 700 ns after the collision, and the L0 response must be delivered to the ALICE sub-detectors within 1.2 μs.

Due to the 40 MHz LHC clock (beams collide every 25 ns) the bit-pattern must be received by the local trigger boards within a window of less than 25 ns.

The rack housing the trigger electronics will be placed on the edge above the detector [6], such that the maximum cable length from the RPC to the trigger electronics is 20 m.

Therefore the dedicated Front-End Electronics (FEE) will be placed directly on the trigger detector to pick-up the RPC signals and to deliver a logical signal to the trigger electronics, as described in figure 5.

When taking all the timing constraints into account, the response time of the FEE should be as fast as possible, typically less than 50 ns.

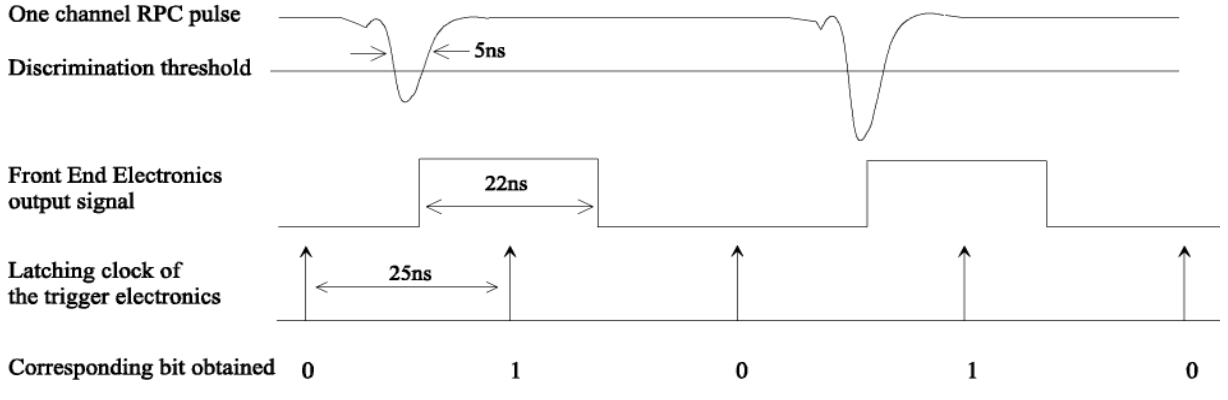


Figure 5: Electronics timing for one channel of the ALICE dimuon trigger.

2.4 Requirements for the FEE

In summary, the requirements for the Front-End Electronics is given in table 2.

Table 2: Summary of the requirements for the Front-End Electronics (FEE).

Number of channels	20992
Input signal (RPC streamer mode)	precursor ($\approx 50\,\mathrm{mV}$) + streamer ($\approx 200\,\mathrm{mV}$) with { rise time $= 2\,\mathrm{ns}$; width $= 5\,\mathrm{ns}$ }
Δt_{p-s}	(0 to 15) ns
Output LVDS signal width	$20\,\mathrm{ns} < w_{out} < 25\,\mathrm{ns}$
Maximum response time dispersion between channels	$\pm 2\,\mathrm{ns}$
Maximum response time	50 ns
Maximum consumption / channel	100 mW
Radiation hardness	$10^{10}\,\mathrm{n/cm^2}$, $1\,\mathrm{Gy}$ } over 10 years
Chip spares Board spares	30 % 10 %
Maximum price / channel	5 FCH
Number of channel / chip	8

- The FEE must be able to handle very fast signals delivered by RPCs and send an output logical signal to the trigger electronics.
- Because all 20992 FEE signals must be received by the trigger electronics within a window of less than 25 ns, a very careful timing is needed.
- To avoid using a special cooling system for the trigger detector, the power consumption per electronics channel must be lower than 100 mW. Therefore the maximum total power consumption of the front-end electronics will be of 2.1 kW directly dissipated in the cavern.
- The dimuon trigger detector is located over 16 m from the interaction point. Furthermore the absorber, the beam shielding and the filter protect the chambers against radiation damage. The maximum rates expected at the trigger station level, integrated over 10 years of LHC working, are [8]: $10^{10}\,\mathrm{n/cm^2}$ for the neutron fluence and 1 Gy (100 rad) for the absorbed dose.
- Mainly for cost and consumption reasons, it has been decided to develop this dedicated electronics in micro-electronics technology. Furthermore, the strip segmentation of the detector and trigger electronics imply the grouping of 8 channels per chip (or ASIC).

Basically the required FEE consists of a discriminator stage followed by a shaper. No amplification of the input signal is needed with RPC operating in streamer mode.

3 Front-end chip design

3.1 ADULT discrimination technique

As described in reference [7], a standard single threshold discrimination technique to pick-up the streamer signal of the RPC in the operating conditions gives a time resolution of about 3 ns. Furthermore, a double structure appears in the time distribution. This originates in the time fluctuation Δt_{p-s} of the streamer peak for the pulses developed in a RPC (fig. 4).

In order to improve the time resolution, a new discrimination technique has been developed at LPC Clermont-Fd. This technique takes advantage of the precursor time stability with respect to particle crossing through the RPC, by using two discriminators. The first one with a low threshold (typically $U_{LT} = 10\,\mathrm{mV}$) detects the precursor, and the second one with a high threshold (typically $U_{HT} = 80\,\mathrm{mV}$) validates the streamer one. This new discrimination technique is called ADULT (A DUaL Threshold).

The precursor detection (low threshold U_{LT}) provides a good time reference. But due to its small amplitude, and to keep all advantages of the streamer mode (large signal/noise ratio and small cluster size), the validation of the RPC pulse is done by the streamer detection (high threshold U_{HT}).

3.2 Principle of one channel

This dedicated discrimination technique has been implanted in the Front-End Chip (FEC) developed at LPC Clermont-Fd. The AMS BiCMOS 0.8 μm chosen technology is well adapted to the design of fast comparators with low input offset voltage.

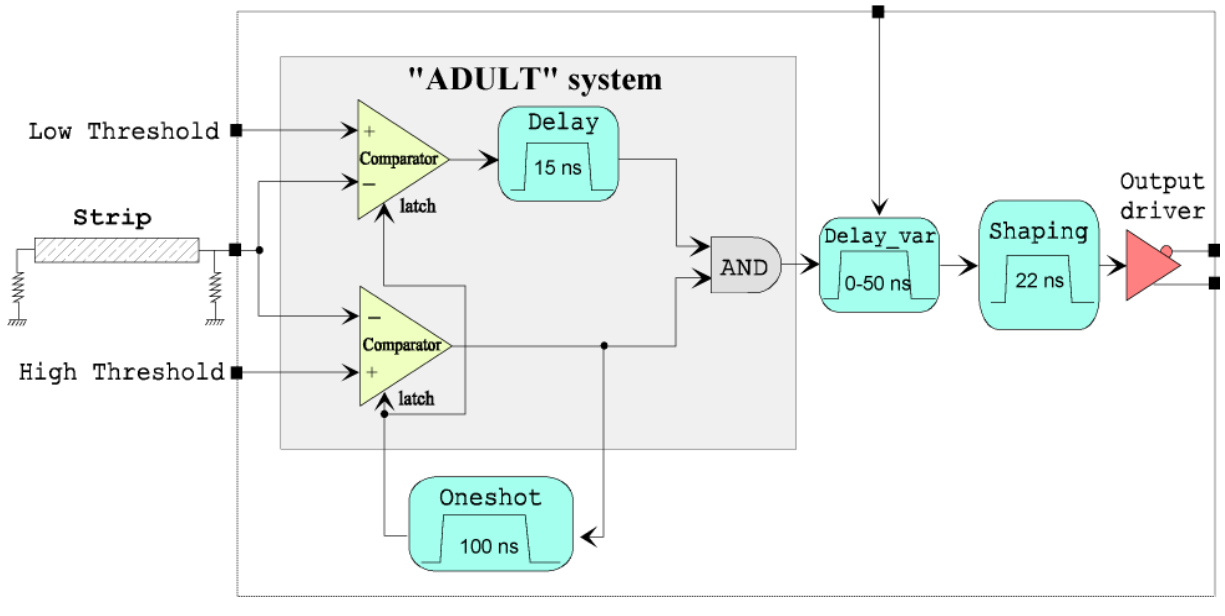


Figure 6: Block diagram principle of one single electronics channel.

The principle of this electronics is presented in figure 6. The main parts are the following:

- The ADULT discriminator stage is made of two fast comparators and a delay followed by an AND gate. The output signal of the low threshold comparator is delayed by about 15 ns, and then a coincidence with the output signal of the high threshold comparator is done. This delay value, optimized during cosmic ray and beam tests [7], is chosen according to the fact that the precursor peak comes earlier than 15 ns relatively to the streamer peak. Thus the coincidence output is in time with the latest of the two input signals, namely the low threshold comparator one, as long as the delay between the precursor and the streamer peaks is shorter than 15 ns, as illustrated in figure 7.

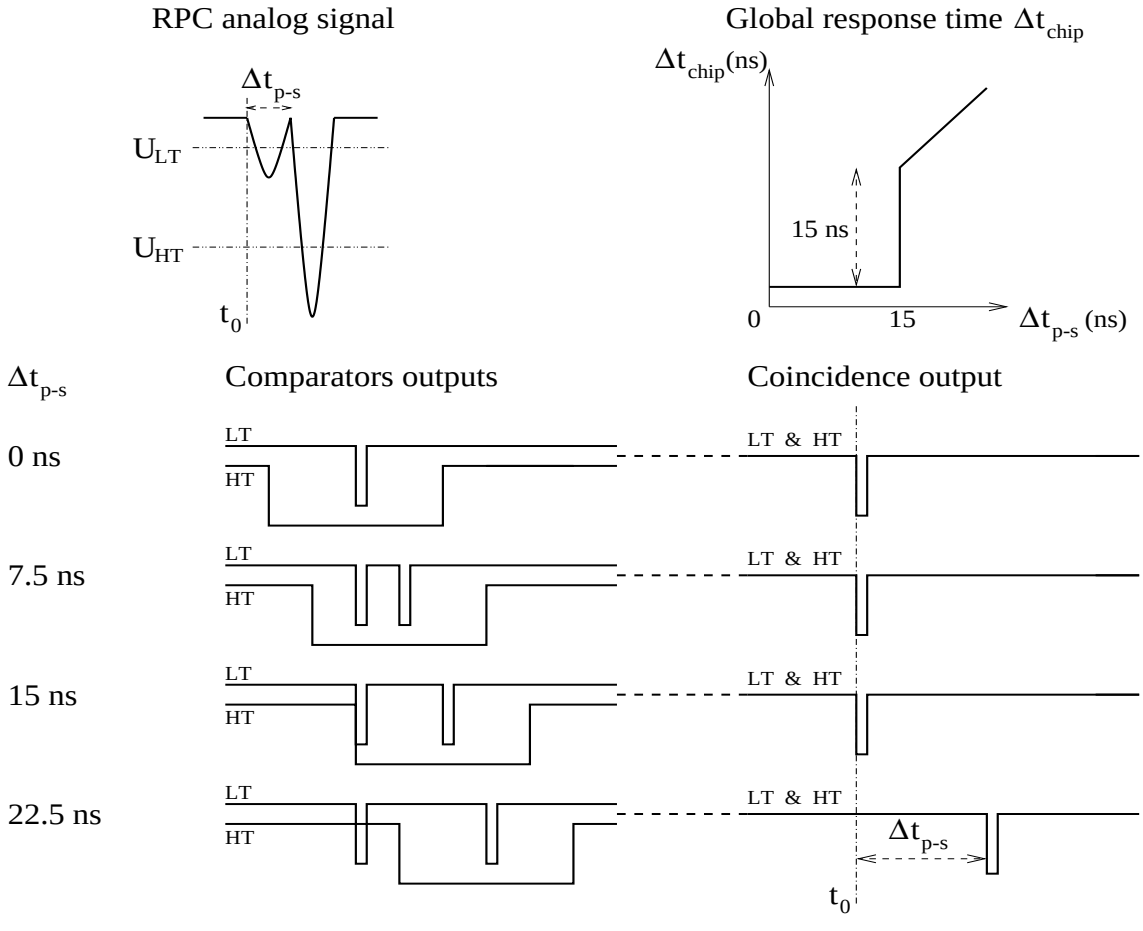


Figure 7: Timing of the output signal with the ADULT technique. The output of the low threshold comparator delayed by 15 ns is noted LT, and the one of the high threshold comparator is labeled HT. The output of the AND gate is noted LT & HT. The curve on top right illustrates the expected global response time (Δt_{chip}) versus the streamer peak delay (Δt_{p-s}) for a chip delaying by 15 ns the output of the low threshold comparator.

- An "oneshot" system prevents any channel from re-triggering during 100 ns. When the high threshold comparator detects a streamer, its output activates a monostable. The monostable output changes immediately and the new level is held during about 100 ns. The two comparators are disabled during this time.

- A remote control delay, up to 50 ns, and common for a whole chip (namely for the 8 channels of a chip) is tuned by a DC voltage. It allows to adjust the timing of

the output signal, if needed.

- The signal is converted into a 22 ns logical LVDS signal in order to drive a 20 m twisted pair cable. The LVDS standard is well adapted to transmit fast signals with weak consumption.

3.3 Schematic of one channel

The schematic of one front-end electronics channel is composed of several blocks as displayed in figure 8. The input stage is made of 2 comparators called "discri", the upper one being used to discriminate the precursor pulse (low threshold), and the lower for the streamer pulse (high threshold). Each of them is followed by the "2_XOR" block which can invert the polarity of the output comparator pulses, depending of the RPC pulse polarity. The polarity is selected by an external pin called "pol". The latching blocks "latch_lt2" and "latch_ht" deliver a logic pulse of fixed width independent of the comparator output signal duration. The "latch_ht" block is also required to freeze the discrimination system during the "oneshot" period of 100 ns. The output of the low threshold latching block "latch_lt2" is delayed by about 15 ns, as described above, and set into coincidence with the high threshold latched signal. This is done with the "coincdiscri" block to validate the precursor signal by the detection of a streamer pulse. Thus the coincidence output is in time with the latest of its two inputs signals which is the low threshold one, as long as the delay between the precursor and the streamer is shorter than 15 ns (fig. 7). This signal can be delayed in a range of 50 ns by an external DC voltage applied on the "delay" pin. The final 22 ns LVDS signal is obtained through the two last stages called "shaper" and "driver".

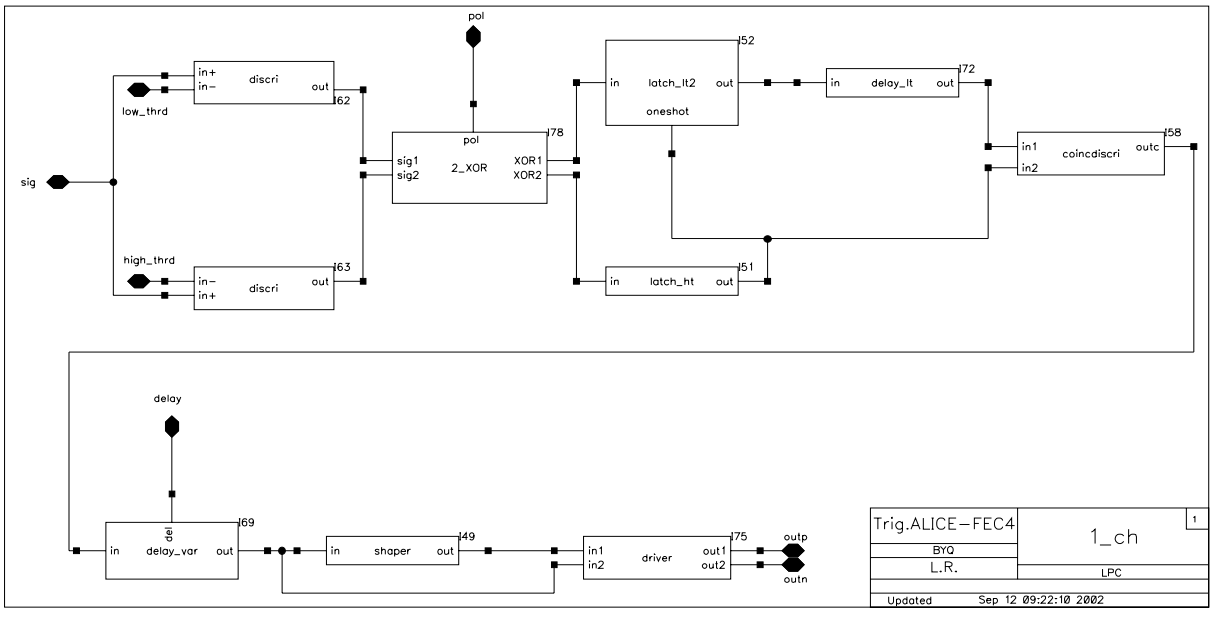


Figure 8: Block diagram of one single front-end electronics channel.

The design and performance of each of these blocks has been described in details in previous papers [9] [10].

Main and new (or updated) considerations are reported below.

3.3.1 Comparator

The schematic of the comparator is displayed in figure 53 (appendices B). It is composed of two differential amplifiers followed by an emitter follower transistor Q26. The total gain is greater than 200 up to 100 MHz. The input noise voltage is dominated by thermal noise of the bipolar input transistors Q0 and Q1, but does not exceed 100 μV RMS for the total frequency bandwidth. Bipolar transistors are preferred to MOS transistors, in order to minimize the input offset.

Two transistors used as diodes are inserted between the two collectors of Q0 and Q1 in order to prevent a slow response time for large RPC pulses due to saturation of the input stage.

3.3.2 Polarity inversion

The two comparators deliver negative (up to down) or positive (down to up) signals according to the polarity of the RPC pulses which is positive for vertical Y strips and negative for horizontal X strips. Thus it is necessary to invert the signal in one of these two situations in order to always input the latching block with the same type of signal. The choice was made to invert for positive RPC pulses. This inversion is carried out with an XOR logic gate, whose the scheme is shown in figure 54 (appendices B). When the "pol" pin is plugged to the upper voltage V_{cc}, the outputs XOR1 and XOR2 are the inverted signals of respectively "sig1" and "sig2". When "pol" is grounded, the inputs are directly copied to the respective outputs.

3.3.3 Latching

Two latching blocks have been designed. The "latch_ht" block outputs a 100 ns logic signal when a streamer pulse is detected (high threshold). The "latch_lt2" block delivers a 15 ns logic signal when the low threshold is crossed. The duration of this pulse is fixed and independent of the input pulse duration. A second input called "oneshot", directly connected to the "latch_ht" block output, is required to prevent from new latching during 100 ns. The schematics of the two latching blocks are displayed in figure 55 (appendices B). In a first stage, a three (or only two for the "latch_ht" block) inputs NAND gate is built with PMOS and NMOS transistors: the output state is low only when the three inputs are high. Typical simulated signals of the "latch_lt2" block are drawn in figure 9. As the input "in" (after the CMOS gate) goes up to 3.5 V when the low threshold is overshot, the output of the NAND gate goes down. Few nanoseconds later, the state of the out pin (after the CMOS gate) goes down, producing thus the coming back of the NAND output to the high state. This pulse controls the PMOS gate of the monostable stage which delivers a 15 ns logic pulse to the next block "delay_lt" (see the description of the monostable below).

The function of the "latch_ht" is similar. It delivers a 100 ns logic pulse to the "oneshot" input of the "latch_lt2" block and to the "coincdiscri" block.

3.3.4 Low threshold delay and monostable function

As previously discussed for the ADULT system, it is required to delay the low threshold discriminated signal by a fixed value, in order to guarantee that the reference time will be given by the precursor pulse. This function is carried out by a monostable structure as represented in figure 10. A constant current source I_0 loads a capacitor C when the PMOS transistor Q, operating like a switch, is open. Then the base voltage of T1

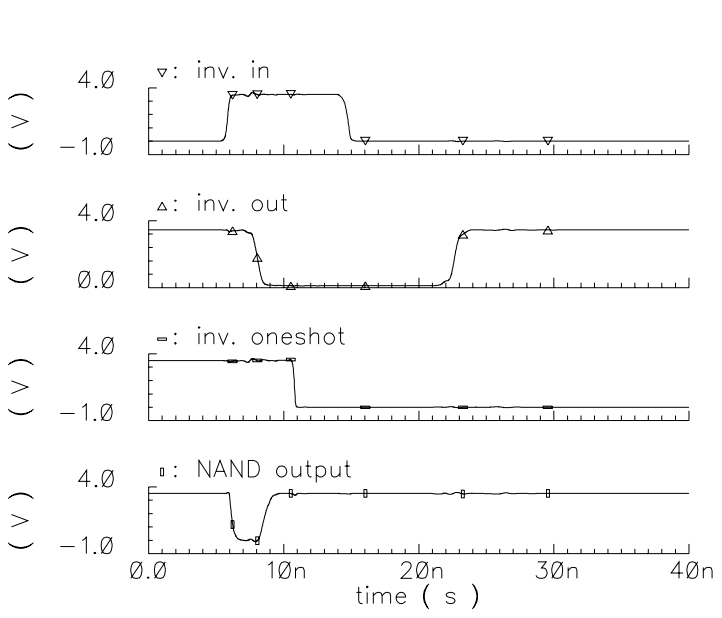


Figure 9: Simulated signals for the low threshold latching block "latch_lt2".

decreases with a constant slope proportional to I_0/C. This signal is compared to a constant potential ΔV by a differential amplifier whose outputs "out" and "$\overline{\text{out}}$" swing after a time $t_w = f(C, \Delta V, I_0)$. This structure is used in the "delay_lt" block, and also in the "latch_ht", "latch_lt2", "delay_var" and "shaper" blocks, with values of C, I_0 and ΔV adjusted to the required delay.

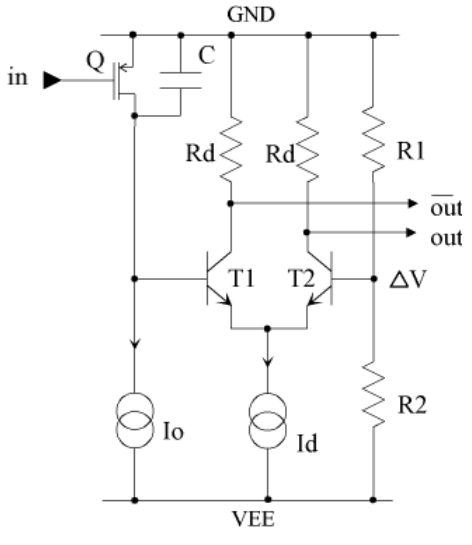


Figure 10: Typical monostable structure.

The schematic of the "delay_lt" block is given in figure 56 (appendices B). The $C = 1\,\text{pF}$ capacitor, the $I_0 = 80\,\mu\text{A}$ current and the $\Delta V = +2.10\,\text{V}$ reference voltage have been optimized in order to obtain a delay of about 15 ns between the input and output signals.

3.3.5 Coincidence

Figure 57 (appendice B) displays the schematic diagram of the "coincdiscri" block, using a classic NAND gate structure. The time of the output pulse as plotted in figure 11 is given by the precursor discrimination, but this signal is only present when a streamer pulse has been discriminated.

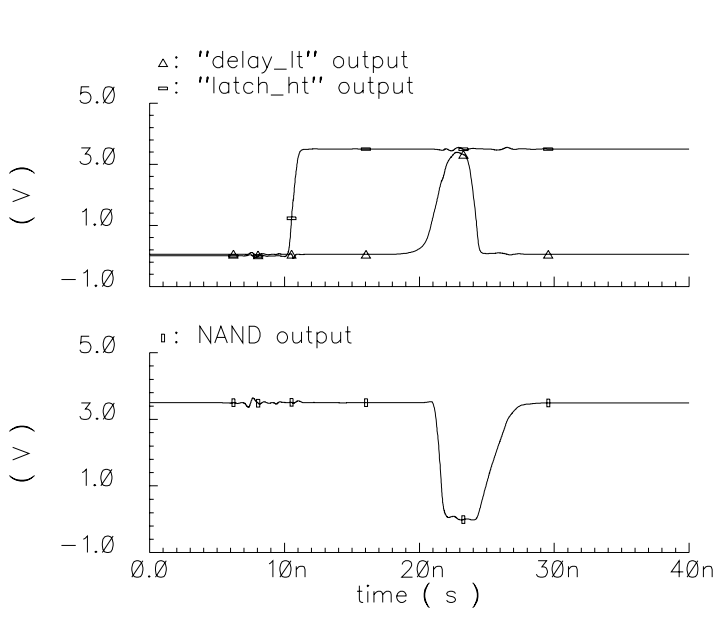


Figure 11: Input and output signals of the coincidence obtained by simulation.

3.3.6 Variable delay

Figure 58 (appendice B) of the "delay_var" block exhibits a classical monostable structure. The delay is tuned via the external DC voltage applied on the "del" pin to control the ΔV threshold. The others monostable parameters are: $I_0 = 125\,\mu$A and $C = 5\,$pF.

3.3.7 Shaping

The width of the LVDS output signal is obtained by combining two signals as represented in figure 12. When the output of the "delay_var" block goes up, the capacitor of the monostable of the "shaper" block (fig. 59 in appendice B) is short-circuited by the PMOS transistor. Then the monostable output goes down quickly (transition 1 in figure 12). When the delay signal comes back to the low state (transition 2), the PMOS transistor of the "shaper" block presents a high impedance and the capacitor is loaded until the voltage reaches the threshold potential (see 3.3.4). Therefore the "shaper" output comes back to the high state (transition 3). This signal and the delay block output are inputted to a NOR gate implanted in the "driver" block. The resulting signal is a pulse with a fixed width according to the monostable parameters of the "shaper" block ($C = 2\,$pF, $I_0 = 125\,\mu$A, $\Delta V = 1.4\,$V) and delayed by the "delay_var" block according to the external voltage applied to the 'delay' pin.

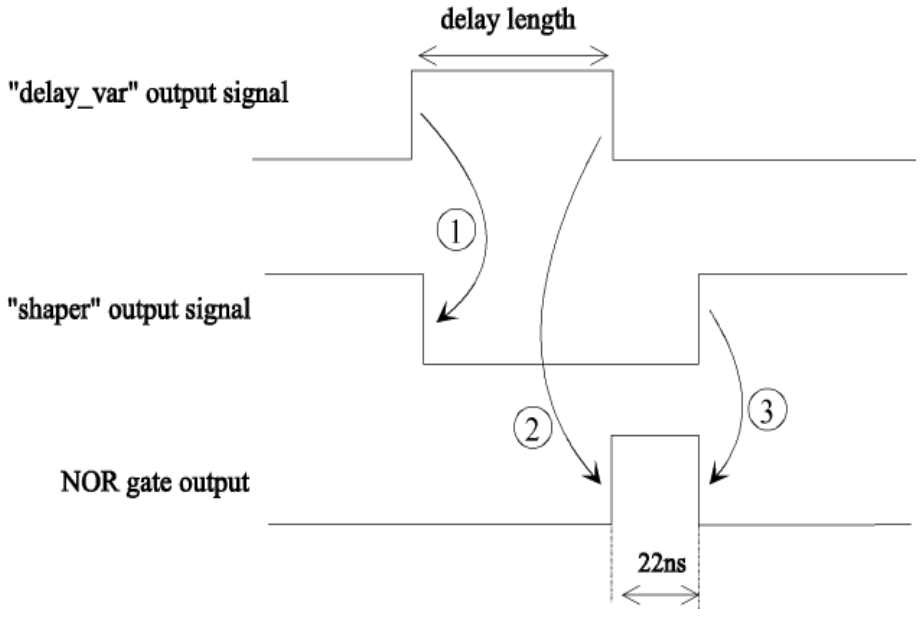


Figure 12: Principle to obtain the delay and the width of the output LVDS signal.

3.3.8 LVDS driver

The previously introduced NOR gate is simply made of two parallel bipolar transistors of an emitter-coupled pair circuit, noted Q3, Q7 or Q2, Q10 in figure 60 (appendice B) of the "driver" block. It is worth noticing that two emitter-coupled pair circuits are drawn in parallel. The upper one is used to switch the NMOS transistors M0 and M3, and the lower stage to adjust the DC voltage of the two complementary LVDS outputs "out1" and "out2". The common mode voltage imposed by the LVDS standard is about +1.2 V. Thus the common mode voltage on the bases of the bipolar transistors Q0 and Q1 must be set to about +2.0 V. The resistors R7, R20 and R23 produce the required 1.5 V voltage drop, according to the DC current across the corresponding emitter-coupled pair circuit (about 520 μA).

The output stage is composed of two bipolar transistors, two NMOS transistors and a DC current source (about 3.8 mA) supplied by Q8. When the driver switches, it changes the current direction across the cable termination resistor, thereby creating a valid 'one' or 'zero' logic state to the LVDS receiver. For example, when the output of the NOR gate rises, the NMOS transistor M3 is switched on and M0 is off. The current is out-putted across the "out2" pin, and comes back through "out1" pin.

3.4 Global schematic and layout

3.4.1 Global schematic

The global schematic of the ASIC is displayed in figure 13, and the pins allocation given in figure 63 (appendices B). Eight previously described one-channel blocks are used. The eight inputs are connected to analog AMS Pcells PADs (see figure 61 in appendices B) to protect them against ESD (ElectroStatic Discharge) and over voltage input pulses. These PADs are also used for the other analog inputs (delay, threshold...).

Four different power supplies are used. The "vcc" +3.5 V power supply, referenced to ground "gndl", supplies all the dynamic stages, except the "driver block". When a +3.5 V DC voltage is required for the current source mirrors or for the threshold values,

a dedicated power supply distribution is used, named "vccd", also referenced to ground "gndl". The −2.0 V negative voltage is supplied by "vee" and used only in the block "discri" in order to discriminate negative RPC pulses. Finally, a distinct power voltage distribution ("vcca" and "gnda") is dedicated to the "driver" block supply, in order to prevent from high current variation on the previous power supplied stages when the outputs switch.

Moreover, three 30 pF decoupling capacitors are directly inserted between the power supply pins "vcc", "vccd", "gndl" and the lowest potential represented by "vee", as displayed in figure 13.

3.4.2 Global layout

The global layout picture is given in appendices B (Fig. 64).

The power distribution of one-channel cell is displayed in figure 14. Horizontal metal2 layers are drawn to distribute the different power supplies to the respective blocks. Two 10 μm metal2 layers are used to output the LVDS signals on pins "out1" and "out2". The different widths of the power supplies layers and the values of the respective maximum DC current transported are reported on table 3.

Table 3: Maximum DC current for each power supply layers.

Layer	Width (μm)	Max. DC current (mA)
vcc	30	6
vccd	21	8
vee	29	5
gndl	30	6
vcca	48	5
gnda	30	9
out	10	4

Figure 15 displays the global power supply distribution on the 8 one-channel cells. The vertical metal2 layers distribute the different LV power supplies to the horizontal power layers of each one-channel cell. Each of them is connected to several PADS in such a way that the current density across metal is limited. The VCCA and GNDA layers are drawn near the output stages of each channel in order to prevent from voltage drops due to long power paths. In the same way, the VCC and GND metal2 layers are drawn in the center of the chips, close to the input stages, and the VEE and VCCD layers form a ring all around the chip. Table 4 gives the width, the maximum DC current, and the numbers of PADs for each vertical power supply layer.

Table 4: Maximum DC current for each vertical power supply layers.

Layers	Width (μm)	Max. DC current (mA)	Numbers of PADs
vcc	50	25	4
vccd	70	33	4
vee	55	19	2
gndl	50	26	4
vcca	60	10	4
gnda	60	17	4

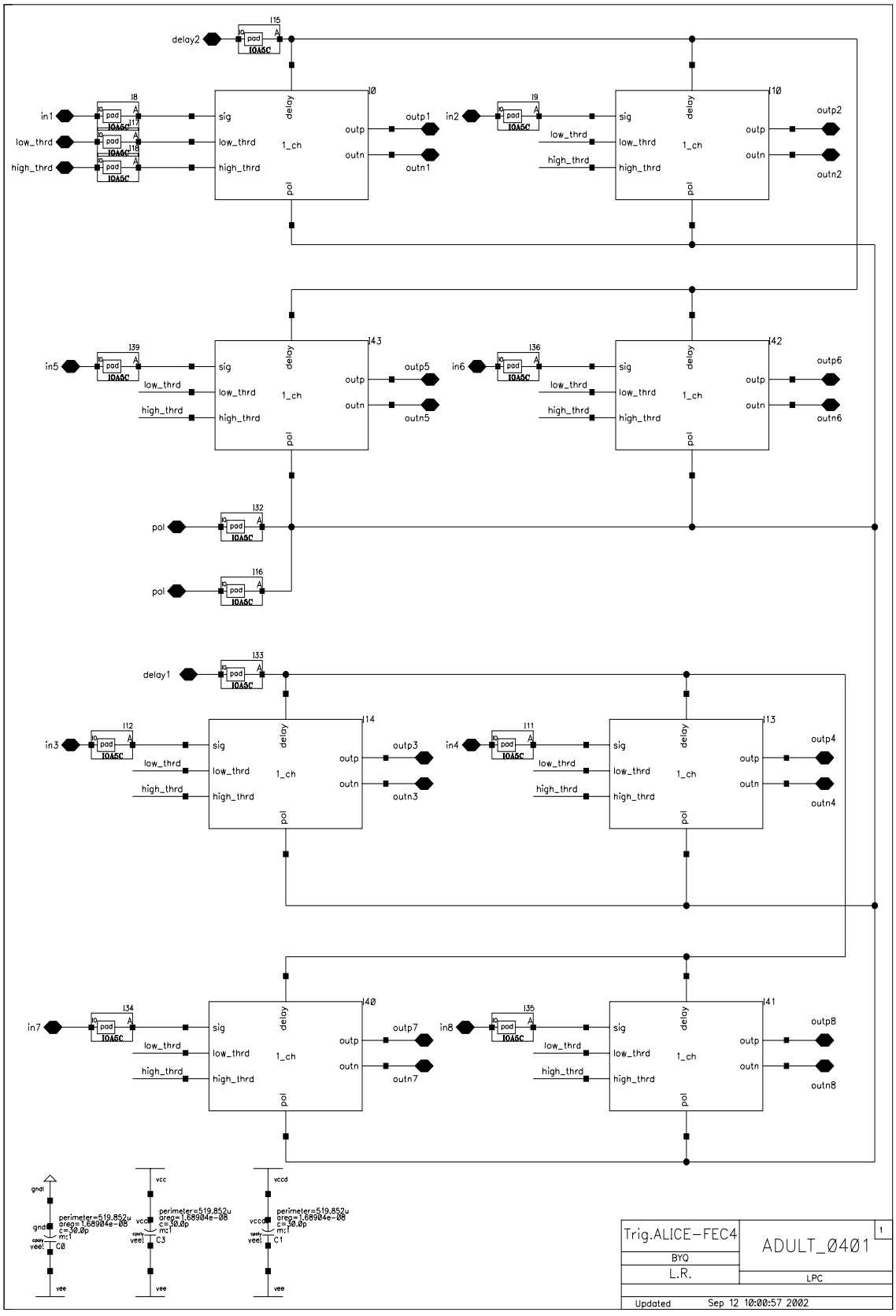


Figure 13: Global electronics scheme of the chip.

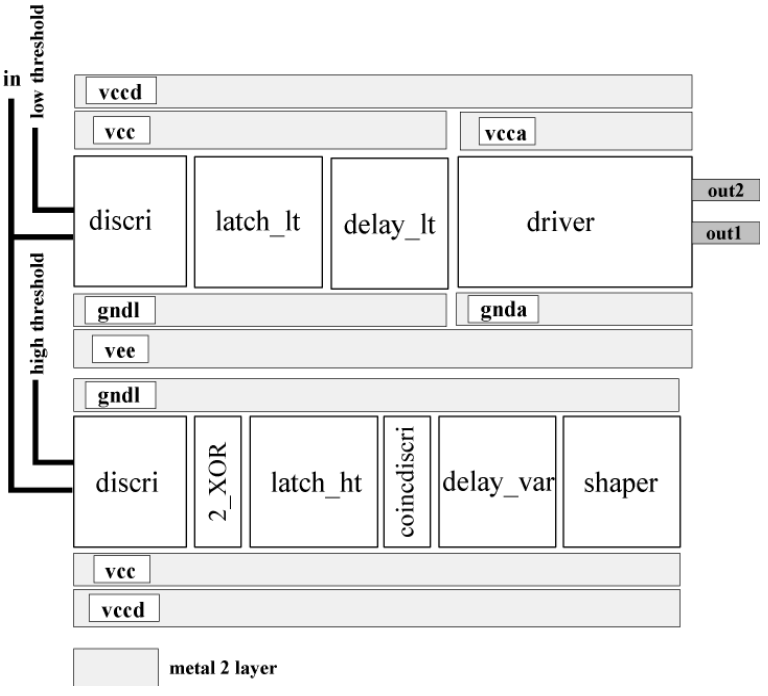


Figure 14: Power distribution on one-channel cell.

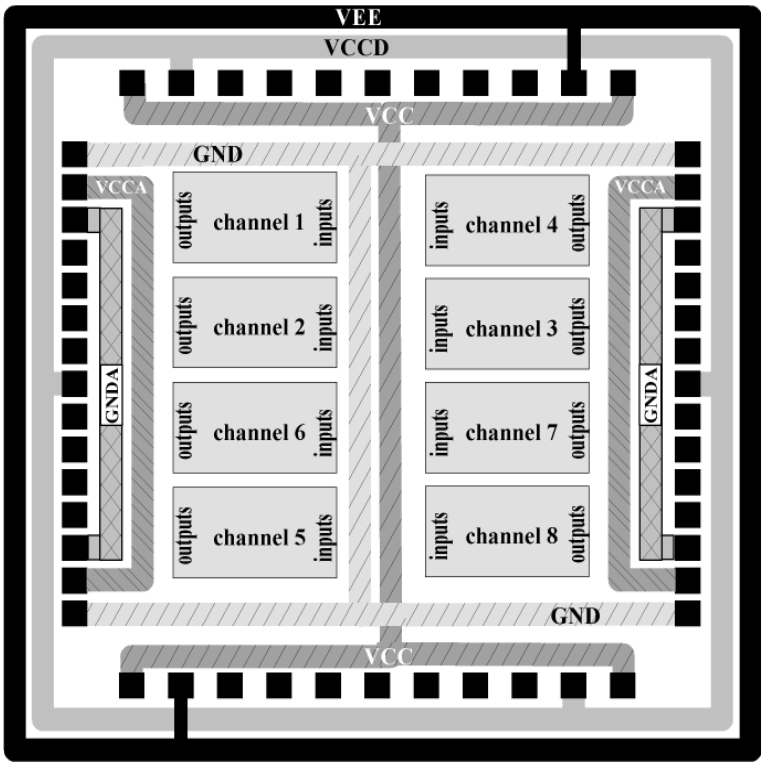


Figure 15: Global power distribution on the chip.

To conclude, it can be noticed that the 1.5 mA/μm maximum current density (metal2) advised by AMS is greatly respected in the layout.

3.5 Results of simulations

Numerous simulations have been carried out to validate the design, but only the main results are reported here. They were obtained with the model of the "analog_extrated view" of one channel included in the schematic displayed in appendices B (fig. 62). RPC like pulses are generated as inputs to the FEE channel, and the corresponding LVDS output signals are computed.

3.5.1 Comparators

The sensitivity of the low and high threshold comparators has been simulated, with positive and negative polarities, and the result is plotted in figure 16, The value of the low and high thresholds are fixed respectively to ±10 mV and ±80 mV, but the precursor or streamer amplitudes are variable.

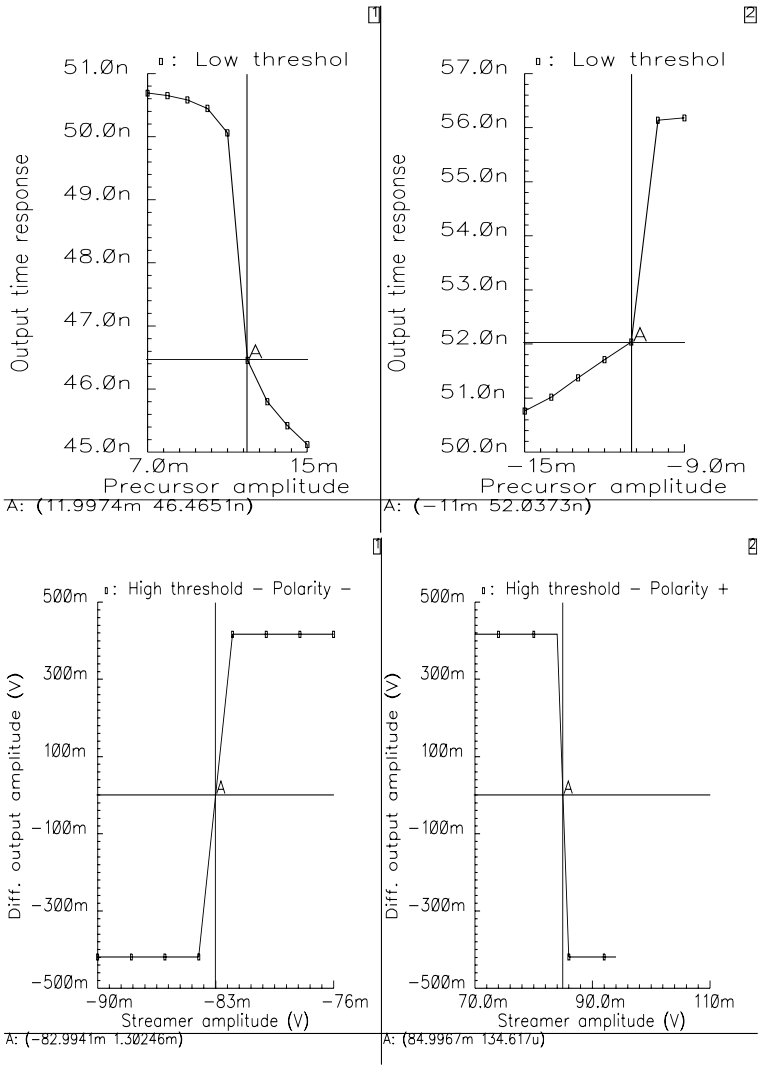


Figure 16: Sensitivity of the comparators for each polarity: upper plot for low threshold (±10 mV) and lower plot for high threshold (±80 mV).

- The sensitivity of the low threshold comparator is defined as the minimum amplitude of the precursor signal above the threshold which is required to change abruptly the response time of LVDS output signal. Then, the reference time is given by the precursor signal instead of the streamer pulse. The sensitivity obtained is about 1 mV for the low threshold comparator for each polarity.

- The sensitivity of the high threshold comparator is defined as the minimum amplitude of the streamer signal above the threshold which is required to swing the differential amplitude of the LVDS output signal. The simulated sensitivity is 5 mV for positive and 3 mV for negative polarity, which is acceptable according to the experimental requirements.

3.5.2 ADULT system

The test consists in increasing progressively the delay between the precursor and the streamer signals while measuring the response time of the FEE channel. The corresponding curve is plotted in figure 17. It is worth noticing that the response time is almost steady for a delay up to 18 ns, with a maximum time variation of ± 1 ns. For a delay longer than 18 ns, the time reference is not any more given by the precursor signal but by the streamer one (fig. 7). Then, a jump of about 20 ns appears in the response time. According to this plot, the operation requirements of the ADULT system are fulfilled.

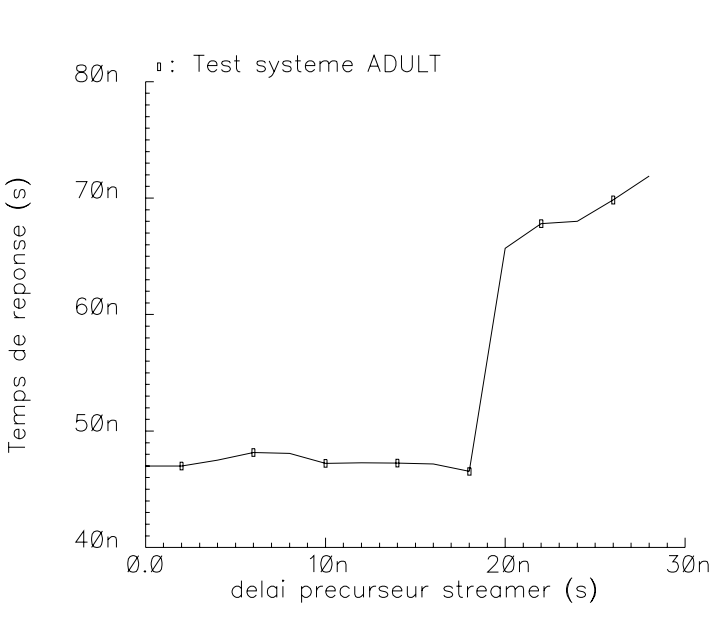


Figure 17: Response time (arbitrary absolute value) of a front-end channel as a function of the delay between the precursor and the streamer peaks.

3.5.3 Statistical simulations

In order to evaluate the consequences of process parameters variations in AMS BiCMOS 0.8 μm technology on the chip performances, Monte-Carlo simulations have been processed using the Affirma Analog Statistical Analysis tool of Cadence and the models of AMS. Several parameters have been controlled, like those presented in figure 18.

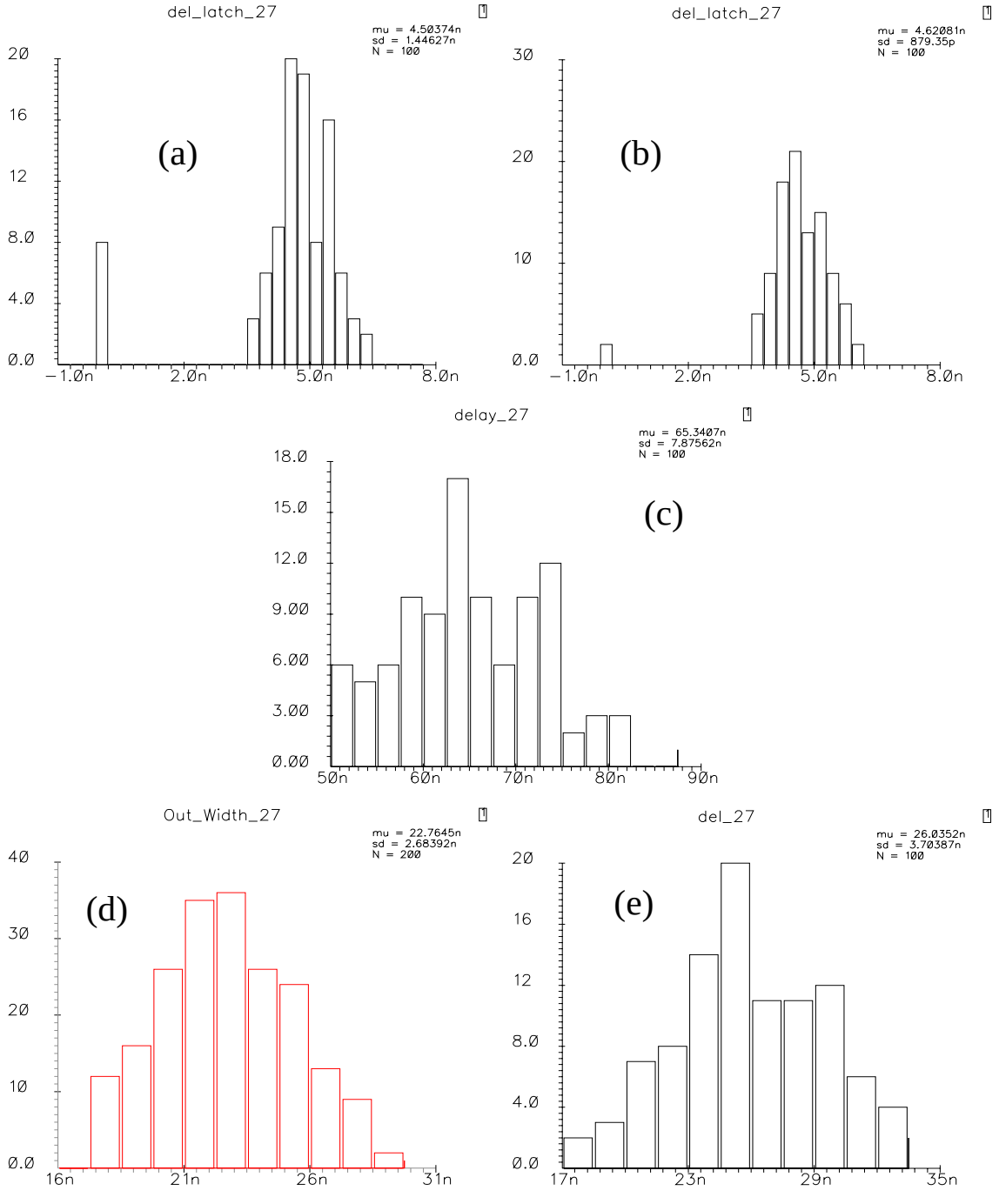


Figure 18: Statistical simulations to estimate several parameters value from one foundry Run to another: (a) and (b) discriminators sensitivity, (c) variable delay range, (d) output signal width, (e) global response time.

- Discriminators sensitivity (a) and (b)
  The sensitivity decrease of the low threshold discriminator is not significant (about 2 mV instead of 1 mV). The sensitivity loss is higher for the high threshold discriminator. The number of missing discrimination is 8 % (a) with an input signal amplitude 10 mV over the threshold, and drops to only 2 % (b) with an amplitude of 15 mV above the threshold. This sensitivity loss can be corrected by increasing the high voltage power supply of the RPCs. Moreover, the delay applied to the low threshold discrimination signal varies from 9 ns to 17 ns (instead of 15 ns typ.), which are still acceptable values from the physical viewpoint.

- Variable delay range (c)
  The minimum variable delay range is 50 ns which matches the required value, so no external adjustment of this parameter is needed.

- Global response time of one channel (e)
  The response time dispersion among the chips must be lower than ±1 ns. As all the ASICs will be produced during the same run, we can assume that the response time variation will be limited. However, this parameter will be adjusted on test bench in order to compensate for any mismatching between chips, using a potentiometer on the front-end board described below.

- Output signal width (d)
  Last but not least, the output signal width variation with process, from 16 ns to 30 ns, is not acceptable as compared to the required value between 20 ns and 25 ns. As described before, the LVDS signal width is controlled by the components values (C, I_0, ΔV) of a monostable stage. The variation of the slope of the capacitor loading curve, due to capacitor and resistor values fluctuations, may be corrected by the adjustment of the DC current I_0, through the "Vccd" power supply voltage. Increasing or decreasing "Vccd", compared to the typical value of +3.5 V, the output signal width is respectively decreased or increased. This correction is also beneficial for all the others DC current sources implemented in the chip, because they are in the same time taken back to their typical values. The benefits of "Vccd" adjustment have been evaluated by the simulation of the two worst cases, it means with the minimum and the maximum 'rpoly2' and 'cpoly' parameters values. The results are plotted on figure 19. The typical LVDS signal width is represented by the horizontal line between 22 ns and 23 ns. With the minimum values of 'rpoly2' and 'cpoly' (lower plot), the typical value of the signal width is recovered with a "Vccd" value of about +3.2 V. For the maximum values of 'rpoly2' and 'cpoly' (upper plot), the typical curve is crossed with "Vccd" equal to 3.9 V. It is also important to notice that, during simulations, when the "Vccd" power supply is increased, the negative "Vee" power supply is decreased in the same ratio in order to not exceed the breakdown voltage of 5.5 V advised by AMS.

Finally it has been checked that the temperature fluctuations have no major effect on the chip response time. This has been simulated over a large range of temperature, from 27^0C to 80^0C. The results as plotted in figure 20 show a good stability with respect to temperature fluctuations, with a sensitivity coefficient of about:

$$\left(\frac{\partial \Delta t_{chip}}{\partial \theta}\right) \approx 37\,\mathrm{ps}/^{\circ}\mathrm{C}\,.$$

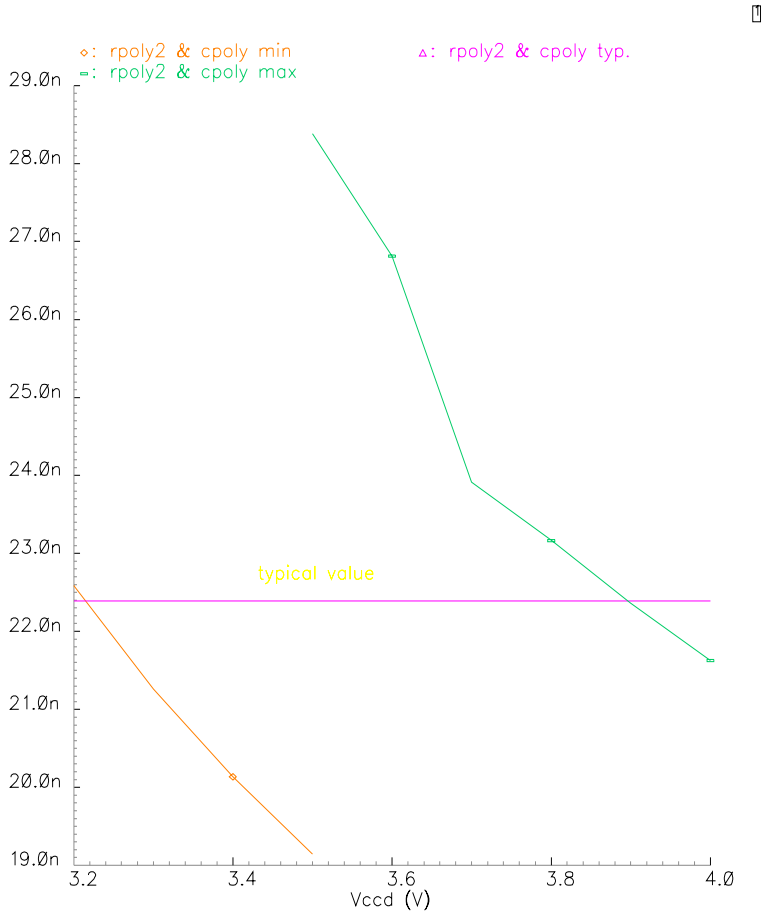


Figure 19: Output width variation as a function of "Vccd" for the extreme value of 'rpoly2' and 'cpoly'.

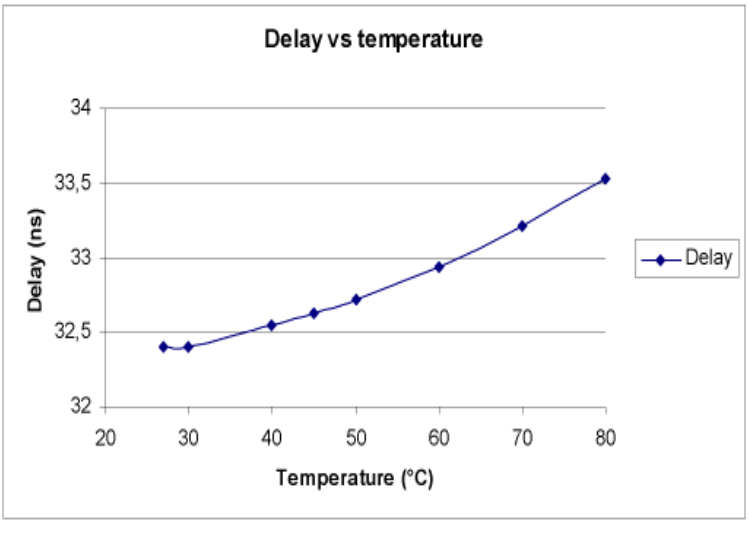


Figure 20: Response time of the output LVDS signal as a function of temperature.

4 Front-end boards design

The length of the RPC detectors is about 2.7 m. The granularity in the deviation planes (X horizontal strips) implies to pick-up the signals on the surface of the RPCs (fig. 21), while this is usually done at their edges. Thus, the front-end boards (FEB) are directly plugged on dedicated connectors placed at the end of the strips.

Each FEB is equipped with one or two ASICs and with all the components which are required to configure, supply and test the FECs.

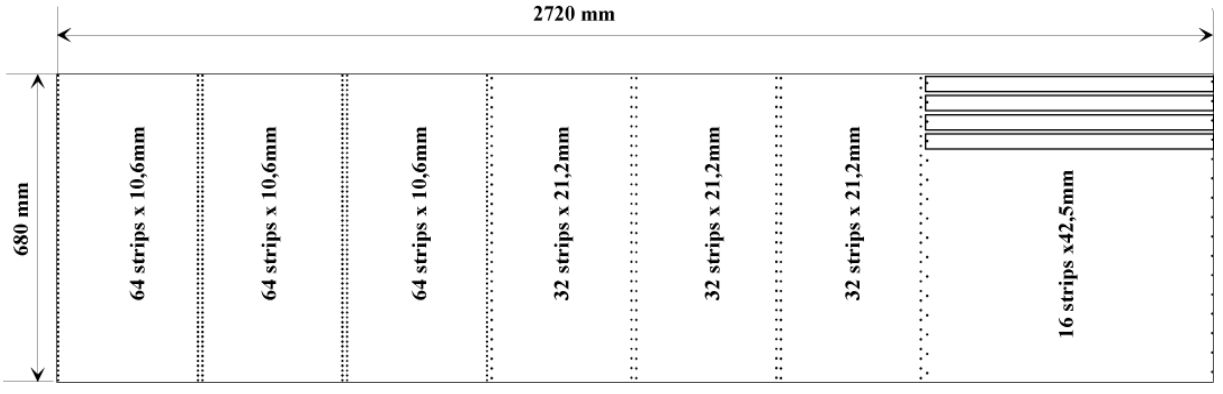


Figure 21: Scheme displaying the points where the signals of X strips (horizontal) are picked-up on an entire RPC, with the three types of strip pitch.

4.1 Chip integration

The electronics schematic viewes of the front-end board are shown in appendice C for the most complicated: a FEB11X (fig. 65 to 70). Front-end ASIC are directly soldered on the PCB because of the bad ageing of the socket to chip contacts.

4.1.1 Thresholds

The two threshold values (± 10 mV and ± 80 mV) are fixed on board and simply built with resistive dividers referenced to the $+3.5$ V supply for positive thresholds, and to the -2 V supply for the negative ones. The polarity is chosen at the manufacturing stage, and consists in soldering the required resistors on the board. As trigger dimuon collaboration asked to foresee an external tuning of the thresholds with a external voltage reference, two dedicated connectors are implanted on the board for threshold adjustments, through a resistive $\frac{1}{100}$ ratio divider. Two jumpers on boar allow to choose the fixe thresholds (10/80 mV) or the external ones.

4.1.2 Delay

The LVDS output signals can be delayed by five 7.5 ns steps in order to compensate different cable lengths. The required delay is configured with jumpers, according to the cable length attached to the front-end board. The values of the resistive dividers corresponding to the five delay steps are given in table 5. In addition, a potentiometer is tuned up during test on bench to put in time all the boards (in a window of 4 ns).

As the two trigger stations are 1 meter apart, the signals delivered by the MT1 station front-end electronics must be delayed by about 3 ns relatively to those of the MT2 station to compensate for the time of flight difference. Therefore different resistive dividers are used for stations MT1 and MT2.

Table 5: Different delay values for the boards of the two stations MT1 and MT2. $R_{2\,th}$ and $V_{d\,th}$ are the calculated values, while $R_{2\,real}$ and $V_{d\,real}$ the real values.

		MT1				MT2			
Delay (ns)	R_1 (Ω)	$V_{d\,th}$ (V)	$R_{2\,th}$ (Ω)	$R_{2\,real}$ (Ω)	$V_{d\,real}$ (V)	$V_{d\,th}$ (V)	$R_{2\,th}$ (Ω)	$R_{2\,real}$ (Ω)	$V_{d\,real}$ (V)
0	1000	2.61	2933	2940	2.61	2.53	2608	2610	2.53
7.5	1000	2.41	2211	2210	2.41	2.33	1991	2000	2.33
15	1000	2.21	1713	1690	2.20	2.13	1555	1540	2.12
22.5	1000	2.01	1349	1330	2.00	1.93	1229	1210	1.92
30	1000	1.81	1071	1070	1.81	1.73	977	976	1.73
37.5	1000	1.61	852	845	1.60	1.53	777	768	1.53

4.1.3 Polarity

The polarity, depending on which of the X or Y strips the FEB are connected, is configured by a strapping 0 Ω resistor soldered to ground or to the +3.5 V power supply, respectively for the negative and positive polarity.

4.1.4 Signal and output connectors

The connection of the front-end board on the RPC strips is done by dedicated female Burndy pin (in brass) plugged into specific strip connectors (fig. 22). Each input is connected to a 50 Ω strip adaptation resistor and to a 100 nF decoupling capacitor.

The mechanical resistance and resistivity reliability of these connectors, both on strips (for the male part) and on PCB (for the female part), has been tested by a succession of connections and disconnections (about 100). No damage has been observed. Furthermore, several connectors have been tested after suffering for nine months in a corrosive environment (humidity and temperature variations). No increase of the contact resistance has been observed. In addition, during all the tests performed with RPC prototypes (at the LPC Clermont-Fd and at CERN) no connection problem occured.

To improve the ground connection (see section 6 illustrating the effect on cross-talk), a connection to the ground of the strip plane is obtained in the same operation with dedicated connectors (fig. 22), when the FEB is plugged in the strip connectors.

An output connector (16 pins HE10 type) is used on the FEB, with the corresponding female part on the cable (see section 4.4), for each 8 output differential signals of one chip.

4.2 Low voltage power supplies

As described before, the FEC needs three different power supplies: $V_{ee} = -2$ V for the analog input stage, V_{ccd} adjustable between 3.2 V and 4 V for the DC current sources, and $V_{cc} = +3.5$ V for the others parts of the chip. Low voltage digital circuits implanted on the FEB are supplied with V_{cc}.

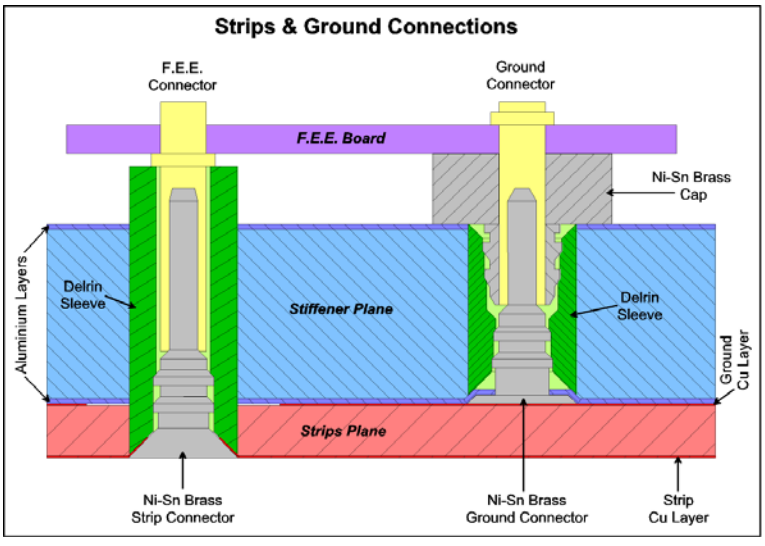


Figure 22: Connection between a FEB and a strip plane, with a strip connector (left) and a ground connector (right).

4.2.1 Low voltage connectors

The low voltages which are used to supply the chips are brought along a specific power distribution system (see section 5.2) in such a way that several boards are connected in chain. Then two low voltage connectors are necessary on each FEB in order to transmit the power supply from a board to the following. Furthermore, the choosen connector are obliques, as displayed in figure 28, to avoid large cable loop between two boards.

4.2.2 Regulation

The two positive voltages required to supply the chip are obtained through two MAX1818 regulators from Maxim company. The voltage V_{cc} is fixed to +3.5 V, while V_{ccd} will be adjusted depending of the performances of some numerous FEC samples picked up in the amount of manufactered chips. The voltage is determinated by a resistive divider made of R_1 and R_2, which obey to the following equation:

$$R_1 = R_2 \left[\frac{3.5}{1.25} - 1 \right] ,$$

where $R_2 = 10\,\mathrm{k}\Omega$ and $R_1 = 18\,\mathrm{k}\Omega$ (the last value is obtained using two serial resistors of $17.8\,\mathrm{k}\Omega$ and $200\,\Omega$) to obtain a voltage of 3.50 V.

4.2.3 Over current protections

The current of the negative −2 V power supply is limited with the use of one Very Fast-Acting fuse. The ampere rating is 125 mA for a nominal supply current of about 80 mA (16 channels boards). Concerning the positive +3.5 V power supply, the use of fuse is prohibited due to the voltage drop induced by the serial resistance. However, the DC/DC regulators Max1818 include an thermal overload protection and an output current limit. Combined with the current limit provided by the Wiener power supplies through the DCS, these protections are suitable with the safety CERN policy.

4.2.4 Decoupling

The input positive and negative are each filtered with one serial ferrite inductor and one 10 μF ceramic capacitor connected to the ground. The DC/DC regulators outputs are also filtered as recommanded in the datasheets (see Fig. 66).

4.3 Front-End Test (FET) system

A global test of the front end and trigger electronics is required before and during physics runs. It will allow to check:

- the good running of every front-end electronics channel,
- the quality of the transmission of the LVDS signals on every twisted pairs cable,
- the good running of the trigger electronics with any algorithm implemented.

The principle of the system chosen is to generated a RPC like pulse to each front end electronics input, at the same time, when a procedure of test is requested. In other words, the whole 21000 FEE channels must be lighted in the same 25 ns window. Considering the different time jitter sources (between twisted pairs, chips, ...), the jitter time of the test system must be then limited to 5 ns. The frequency of this test will not exceed 1 kHz.

The test system is composed of several devices, as represented in figure 23.

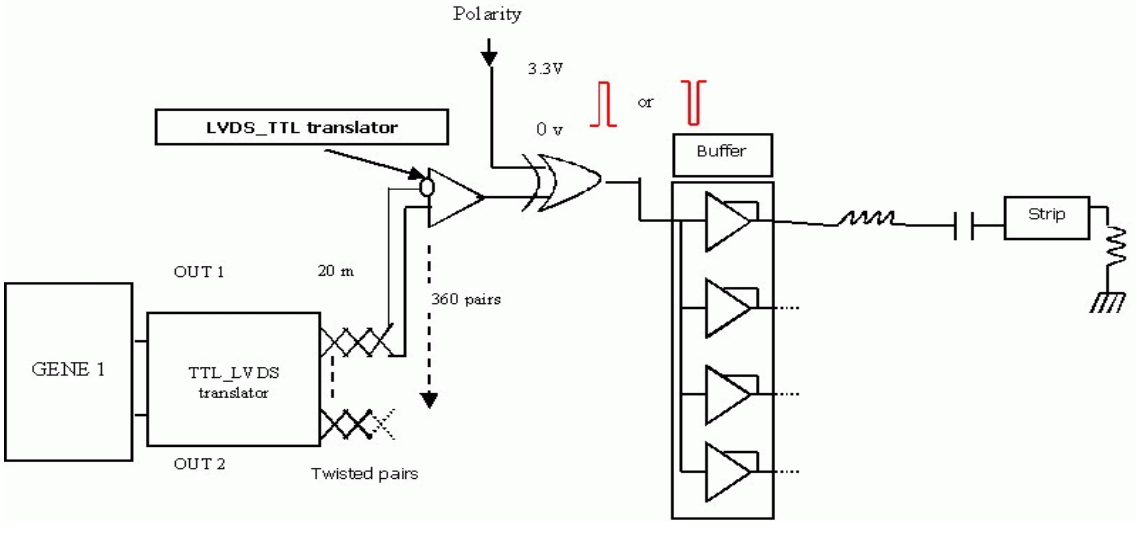


Figure 23: Whole FET principle for one channel.

- A pulse generator delivers a trigger signal to the Local Trigger Unit (LTU) to inform the DAQ that a test is in progress. At the same time, it generates a logical pulse to TTL-to-LVDS translator modules.
- The TTL-to-LVDS translator modules distribute the logical pulse to every front-end board plugged on the 72 RPCs, through dedicated twisted pairs cables.

- On each FEB, the LVDS pulse is translated into a TTL pulse, through a LVDS-to-TTL translator. This signal is inverted or not with a XOR gate, according to the required pulse polarity (X or Y plan), and inputted to an octal low voltage buffer. Each buffered output is then sent to every front-end ASIC input through a 300 Ω resistor to reduce the pulse amplitude, and through a 1 nF capacitor to filter the DC voltage. The positive pulse obtained is plotted in figure 24.

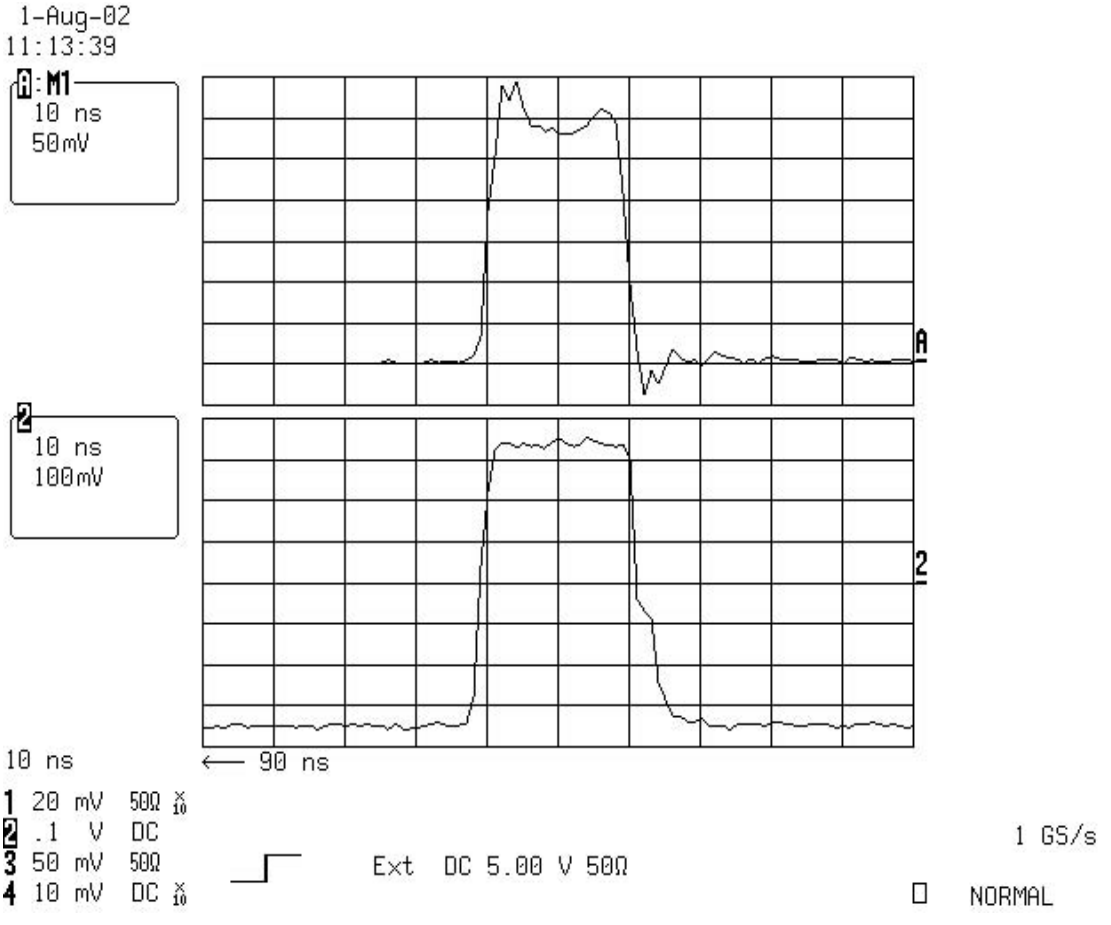


Figure 24: Result of the FET system: pulse test generated at the FEC input (upper plot) and LVDS pulse test received on the FEB (lower plot).

The time jitter measured between the 8 channels of the same FEB20 is lower than 1.5 ns. Moreover, the distribution of the LVDS signals on every FEB will be optimized in order to limit the global time jitter to 5 ns as required.

4.4 Output signal cables

The output signal cables must transmit a fast LVDS pulse from the front-end electronics to the trigger electronics. The different cable lengths required with the corresponding quantity are given in the table 6 (amounting to about 24 km).

A twisted pairs cable with global shielding has been chosen, in order to minimize transmission losses and sensitivity to electromagnetic interferences. A 21 round twisted pairs cable, available at CERN store, has been tested. Figure 25 displays a LVDS signal measured at the beginning and at the end of a 20 meters long cable. The loss of differential amplitude is about 25 % with no alteration of the pulse edges. When

Table 6: Cable lengths and quantities.

Length (m)	20	18.5	17	15.5	14
Number	120	324	358	360	270

this output signal is put into a LVDS receiver, the logic signal is recovered without information loss.

The technical specifications of the required cable are based on the tested cable. A pre-production of 200 m cable has been done to validate the manufacturing. Tests show that the cables are in accordance with the specifications: $\Delta t_{max} < 3$ ns between pair on 20 m long cable.

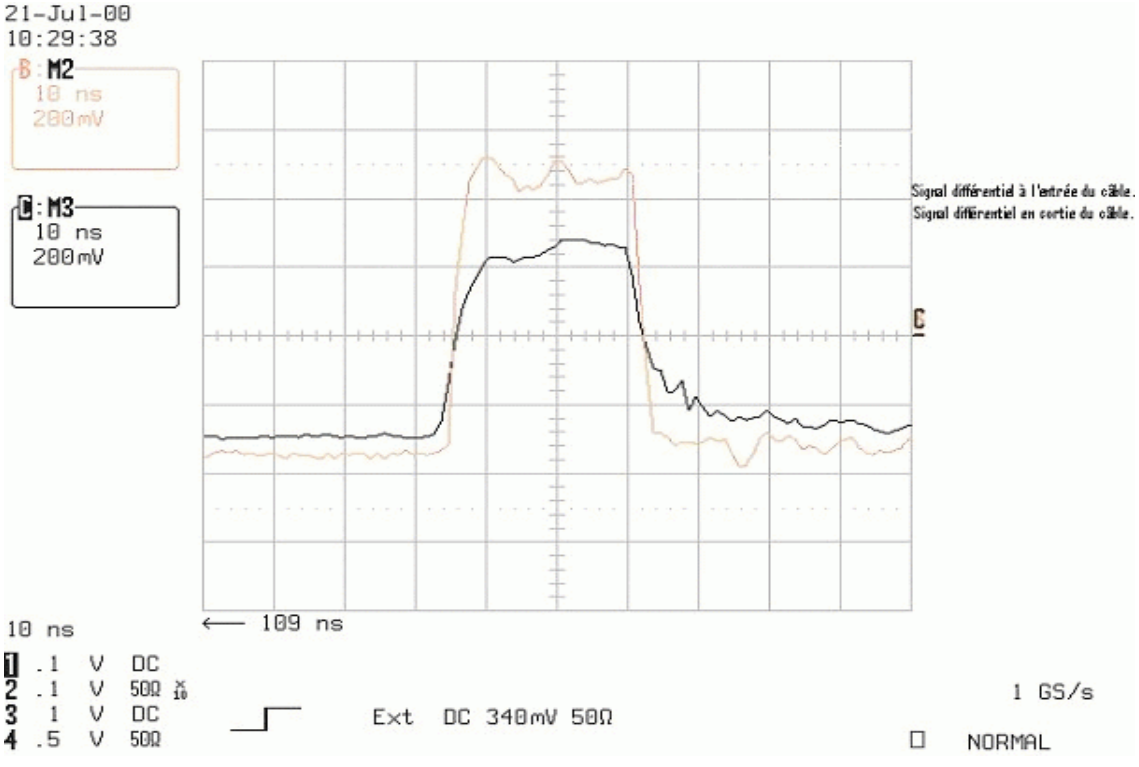


Figure 25: Output LVDS signal at the beginning (channel B) and at the end (channel C) of the 20 m differential cable.

4.5 Adaptation boards

The RPCs strip must be adapted on both ends in order to avoid signal reflections.

The characteristic impedance Z_c has been measured for each of the three types of strip widths corresponding to station MT1. The results displayed in table 7 (first line) represent the mean value of ten measurements, and the associated error calculated as their root mean square (rms).

Amplitude measurements have been carried out with the same RPC (in cosmic rays) using successively the three types of strip width, with 50 Ω at each end. The results are reported in table 7 (second line). Moreover, figure 26 displays the efficiency of the RPC (at CERN-GIF) as a function of its high voltage for the three type of strips. In all the cases, the efficiency plateau is reached for a high voltage of about 8 kV.

According to these measurements, it has been decided to take the same impedance termination $Z_0 = 50\,\Omega$ for the three types of strip width.

Table 7: Characteristic impedance Z_c of the strips (station MT1), and mean value of the signal amplitude picked-up on the strips equipped with $50\,\Omega$ impedances at both ends.

Strip width	1 cm	2 cm	4 cm
Z_c	$(49 \pm 2)\,\Omega$	$(40 \pm 3)\,\Omega$	$(28 \pm 3)\,\Omega$
Signal amplitude	400 mV	450 mV	450 mV

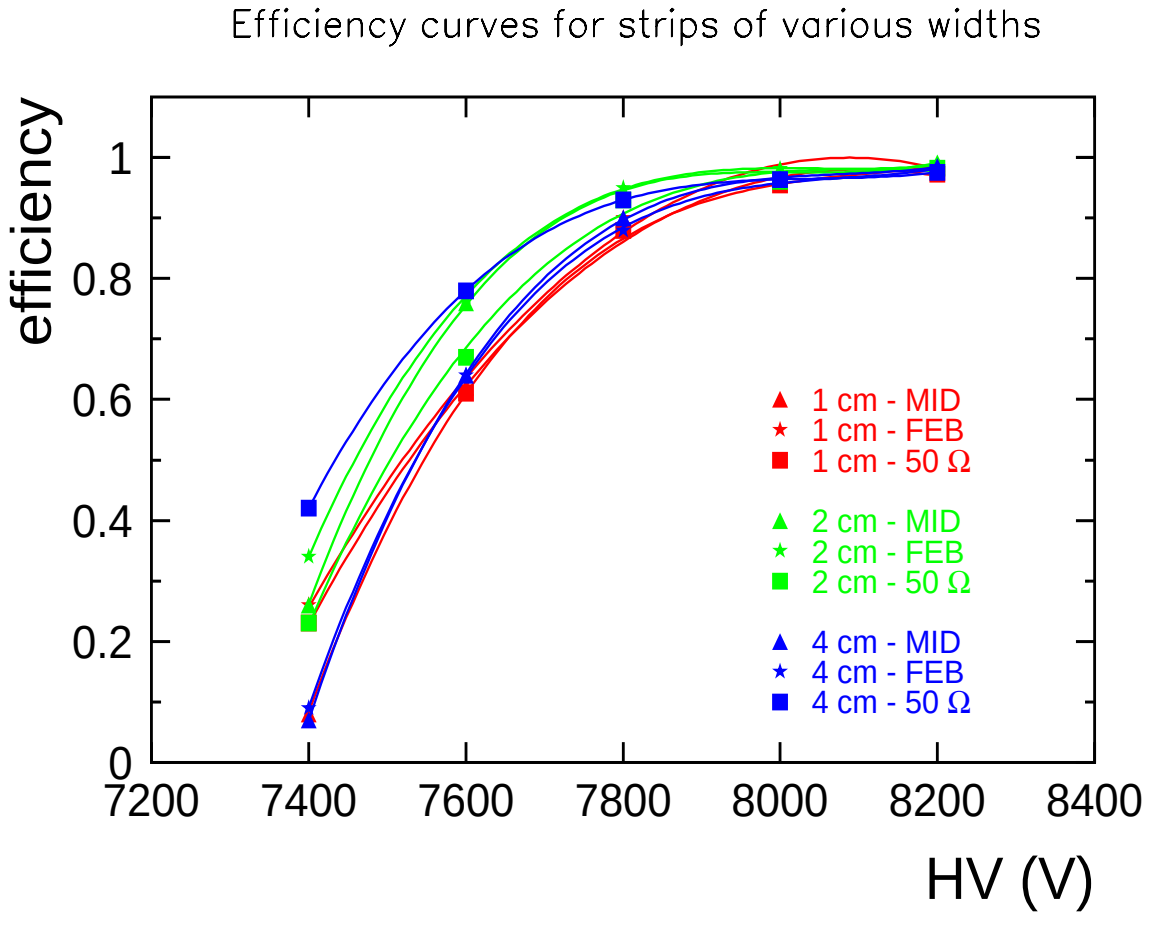


Figure 26: Efficiency curves as a function of the RPC high voltage for strips of various widths (50 cm long) for particles crossing the strip: on the middle (MID), near the front-end board (FEB) and near the adaptation board ($50\,\Omega$).

An equivalent resistor is inserted on each input of the FEB. Moreover, dedicated adaptation boards are plugged on the other end of the strips, which also contain $50\,\Omega$ resistors connected to ground. The layout and the plug system of these boards are identical to the FEB ones (see Fig. 27).

4.6 Summary

To make the connection and disconnection of the FEB easier as well as their manufacturing, it has been decided to limit the length of the boards according to 8 strips of

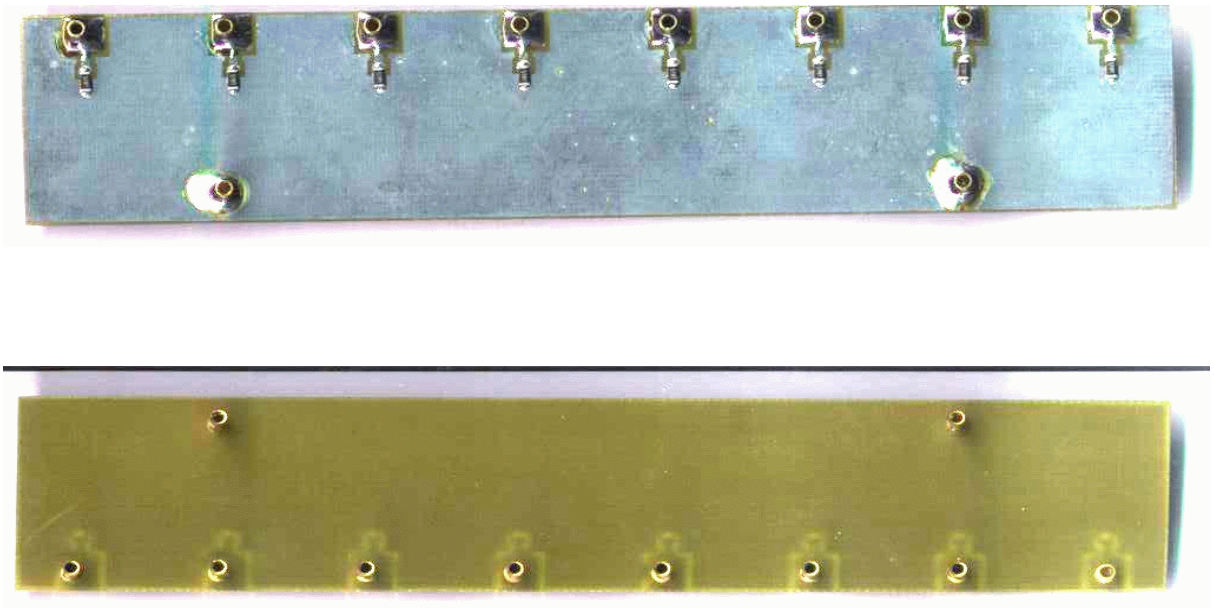


Figure 27: Adaptation board (50 Ω resistor) with 8 strip connectors (2 cm pitch) and 2 ground connectors: top view (upper picture) and bottom view (lower picture).

45.2 mm width, namely to about 36 cm. So the final solution consists of three types of FEB:

- FEB10 with 2 chips for a strip pitch of about 1 cm (16 channels),
- FEB20 with 1 chip for a strip pitch of about 2 cm (8 channels),
- FEB40 with 1 chip for a strip pitch of about 4 cm (8 channels).

A summary of the front-end boards features is given in table 8, while figures 28 and 29 illustrate a FEB with all its connectors. Due to services (power supply and output cable "goulottes" roads estimated on a mock-up), the connectors are not placed on the edge of the boards in order to make the cable connections or disconnections easier.

Finally, the whole list of electronics components for the front-end board types FEB11X is given in appendice D, and the number of different FEBs is listed in table 9.

Table 8: Mechanical data for the three types of front-end boards: FEB10 (1 cm pitch), FEB20 (2 cm pitch) and FEB40 (4 cm pitch).

Board type	FEB10	FEB20	FEB40
Number of chips	2	1	1
Number of strip connectors	16	8	8
Number of ground connectors	2	2	4
Number of output connectors	2	1	1
Number of low voltages connectors	2	2	2
Number of test system connectors	2	2	2
Length (mm) for MT1 / MT2	167 / 175	167 / 167	304 / 326
Width (mm) for MT1 / MT2	50 / 50	50 / 50	50 / 50

Table 9: Number of front-end boards FEBijk for the different types required (without spares), with i giving the pitch (1 cm, 2 cm or 4 cm), j the station number (1 for MT1 and 2 for MT2), and k the strips direction (X for the horizontal strips and Y for the vertical strips). The designations FEB10, FEB20 and FEB40 gather together all the FEBs of a given pitch (for instance FEB20 = FEB21X + FEB21Y + FEB22X + FEB22Y).

FEB10			
240			
FEB11		FEB12	
120		120	
FEB11X	FEB11Y	FEB12X	FEB12Y
120	0	120	0

FEB20			
1504			
FEB21		FEB22	
752		752	
FEB21X	FEB21Y	FEB22X	FEB22Y
528	224	528	224

FEB40			
640			
FEB41		FEB42	
320		320	
FEB41X	FEB41Y	FEB42X	FEB42Y
168	152	168	152

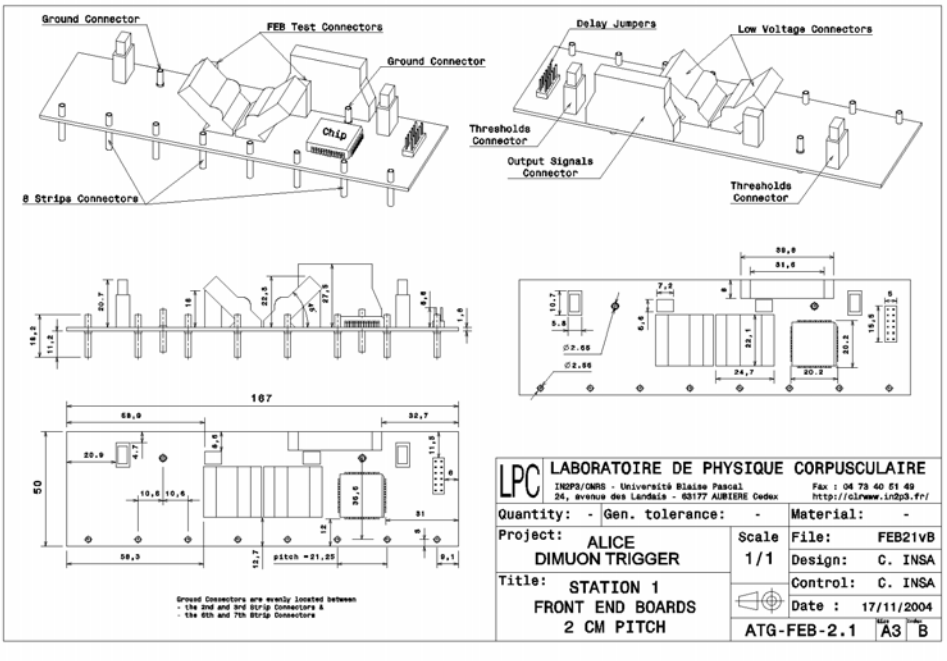
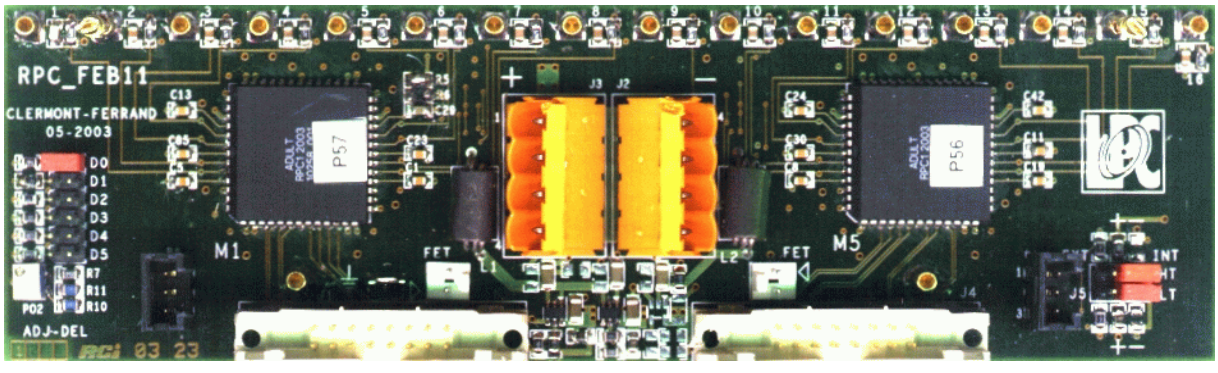


Figure 28: Connectors used on a FEB20 or FEB40. For a FEB10 (with 2 chips), 16 strip connectors and 2 output connectors are used.

Upper side view of a FEB11



Underside view of a FEB11

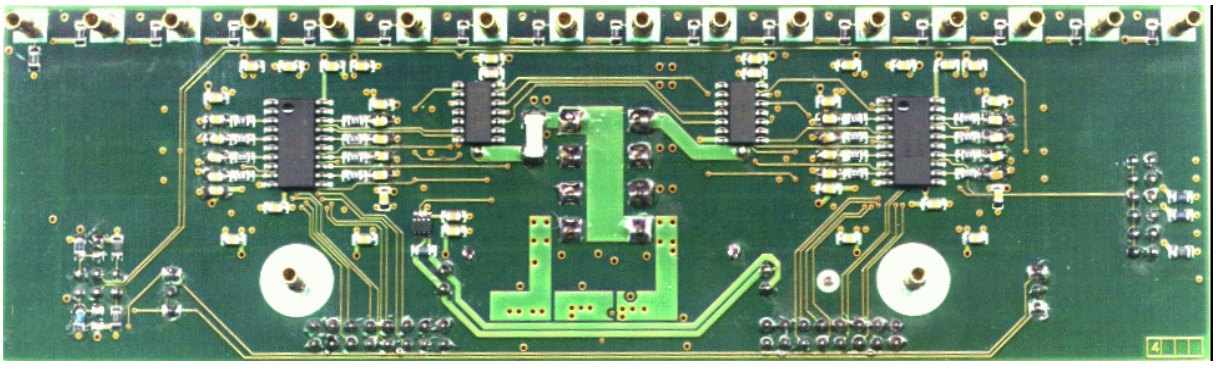


Figure 29: Pre-serie version of FEB11.

5 Power supply considerations

5.1 Grounding and shielding overview

An overview of the global grounding and shielding proposal of the Dimuon trigger setup is shown on figure 30. It is mainly based on general considerations of the ALICE grounding plan [11].

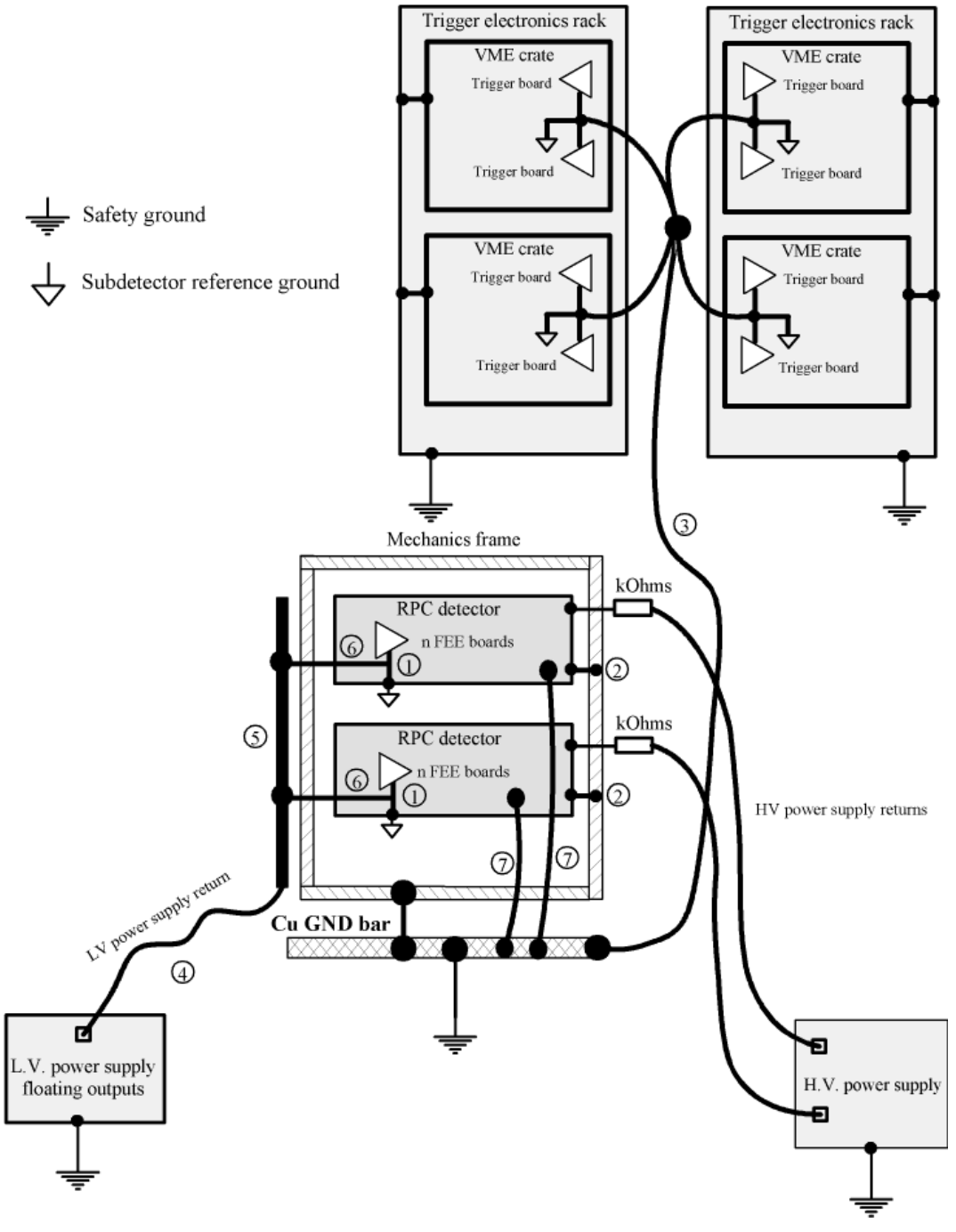


Figure 30: Global FEE grounding scheme.

5.1.1 Constraints

The reference ground of each front-end board is connected to the metallic body of the RPC on which the board is plugged (connection 1 on Fig. 30). The RPCs are held up by a steel frame which is in contact with the RPC body. So, the whole frame of the trigger chambers setup is connected indirectly to the FEE reference ground (connection 2 in Fig. 30). Moreover, as the FEE transmits LVDS signals to the Trigger electronics, the shifting of their respective reference ground must not exceed $\pm 1\,\mathrm{V}$. It is why the FEE and Trigger electronics reference grounds must be connected (connection 3 in Fig. 30).

5.1.2 Proposal

1. Low Voltage Power Supply (LVPS)
   The LVPS of the FEE has floating outputs. Each LVPS return (connection 4 in Fig. 30) is connected to a vertical copper bus-bar distribution, where the ground reference of each FEB is connected (connection 6 in Fig. 30).

2. High Voltage Power Supply (HVPS)
   Each HVPS with floating outputs supplies one RPC. The HVPS return is isolated from the sub-detector reference ground by a resistor, typically of order $1\,\mathrm{k}\Omega$.
   For personnel safety reason, the whole mechanical frame of the trigger setup must be connected to earth. However it is recommended to separated the signal ground to the safety ground. The description of the setup has shown that, by construction, these 2 potentials are connected together. We propose to build an equipotential central point with copper bars located below each half trigger plan. This single point connection is a center of a star network (connections 7 in Fig. 30), which provides the reference and safety potential and avoids shield currents flowing into the system.

3. LVDS signal cables
   The 1500 cables which transmit data from each FEB to the trigger boards are shielded. In order to prevent ground loops, the cable shield is connected to the sub-detector reference ground on the FEB and via a capacitor to the local ground on the trigger boards.

5.2 Power supply distribution

The aim of such a device is to supply the front-end boards, by taking into account different consumptions according to the voltage:

- $10\,\mathrm{mW}$/channel for the $-2\,\mathrm{V}$,
- $90\,\mathrm{mW}$/channel for the $+3.5\,\mathrm{V}$.

The trigger detector is divided into 8 half planes, as displayed in figure 31. Each part has the same number of front-end channels and can be supplied in the same way.

Two low voltage power units, corresponding to $+3.5\,\mathrm{V}$ and to $-2\,\mathrm{V}$, will supply all the FEB plugged in each half plane. The 16 power supply units which are required for the whole detector are manufactured by the Wiener company. They are modular floating power supplies and are designed to provide external load channels with high power consumption over long distances.

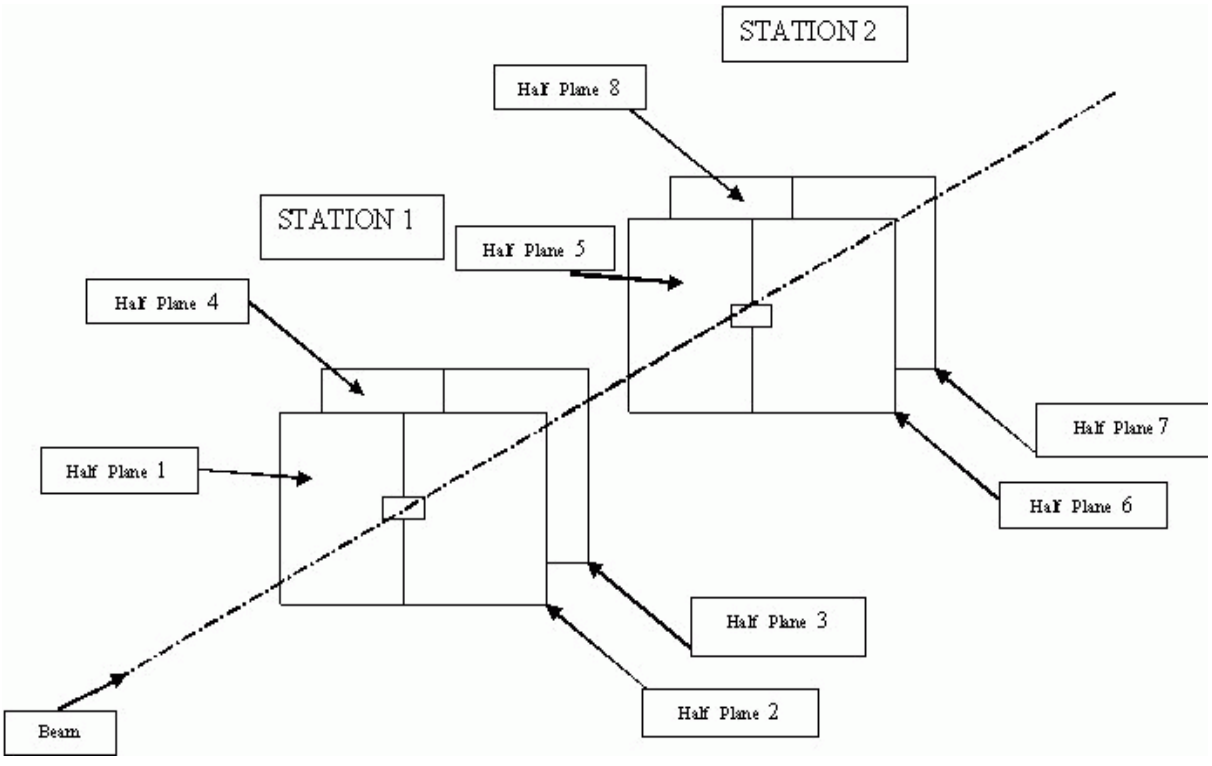


Figure 31: Segmentation of the low voltages for the whole dimuon trigger detector.

The power supply modules are housed into two 6U crates. Each crate admits 10 modules, but only 8 are required in our case (4 positive and 4 negative). The first crate will supply the four left half planes and the second one the four right half planes. The cable length between the power supplies and the detector will be 20 meters approximately. The voltage drops along these cables are compensated by a remote-sense regulator.

As displayed in figure 32, four vertical copper rods transport the low voltage currents from the cable ends to the edge of the 9 RPCs of one single half plane. The voltages are then distributed along each RPC using a distribution cable device. There will be as many such cables as RPC.

The results show that voltage regulators are required for the positive voltage. Concerning the negative voltages, regulators are not essential. Nevertheless, in order to avoid losses due to the connections along the distribution, a particular care must be taken during the manufacture of these connections (tinning and use of resin). Under these conditions, simulations show that the differences of the power supply voltages on each FEB are less than $\pm 100\,\mathrm{mV}$.

5.3 Detector Control System

As previously explained, the low voltage power supply system will be made of sixteen modules (eight for the positive voltages and eight for the negative ones). These modules will be arranged by eight into two crates: four positive and four negative modules in each of them.

Figure 33 displays the structure of the DCS (Detector Control System), in which the low voltages system is inserted.

It is expected to control about thirty parameters concerning each low voltage channel [12] (both for positive and negative voltage):

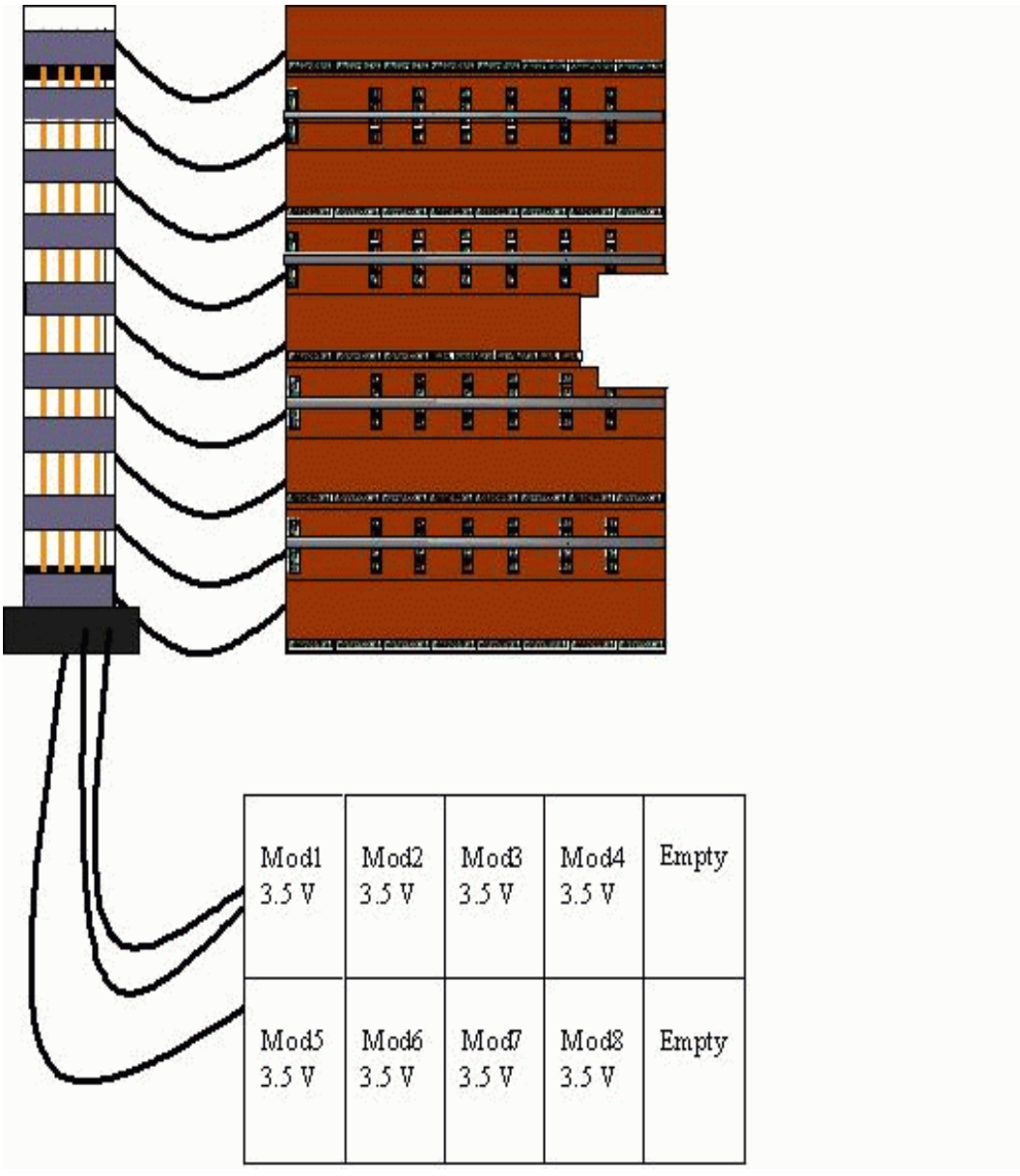


Figure 32: Global view of the low voltages distribution system.

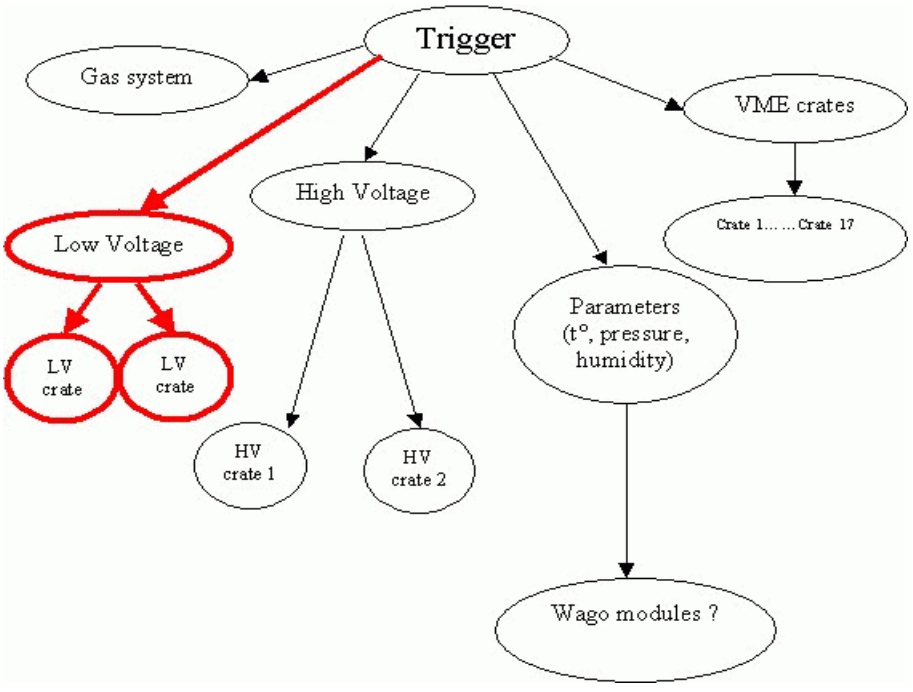


Figure 33: Structure of the dimuon trigger DCS.

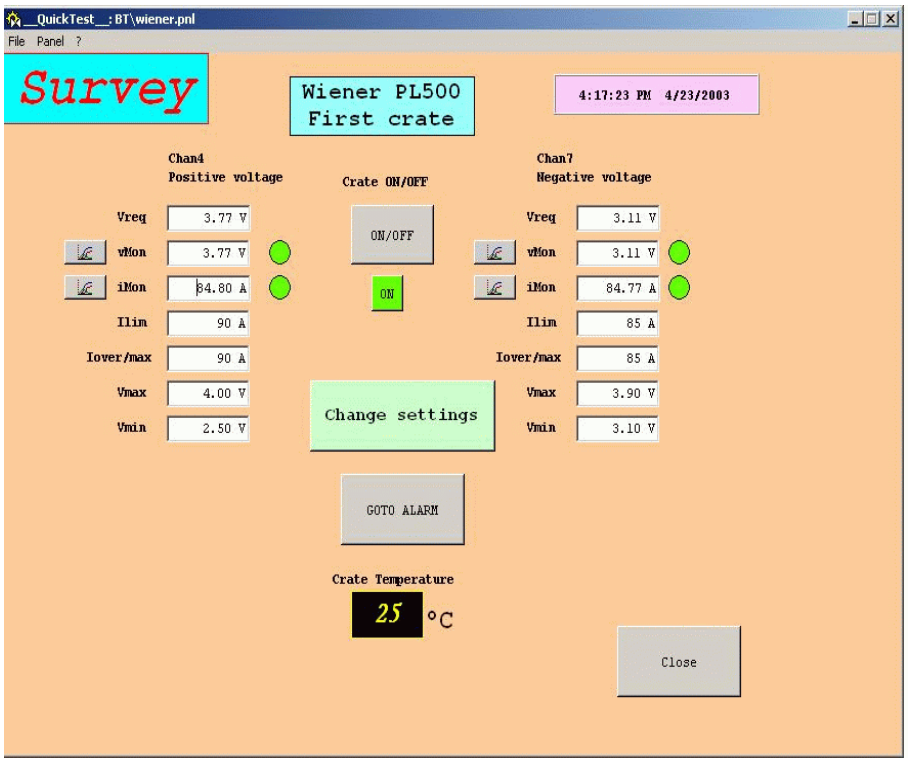


Figure 34: Structure of the dimuon trigger DCS.

- Parameters of low voltage modules (8)
  - status setting and reading (on / off),
  - input voltage setting,
  - output current limit setting,
  - output ramp up setting,
  - output ramp down setting,
  - output voltage reading,
  - input current limit reading,
  - input ramp up reading,
  - input ramp down reading;
- Parameters of low voltage crates (2)
  - status setting and reading (on / off),
  - input voltage reading,
  - input current reading,
  - input temperature reading,
  - output speed fan setting,
  - input speed fan reading.

With this scheme, there will be no control of the low voltage directly on the front-end boards. The working of each FEB can be checked only with the help of the FET system.

According to the CERN standard, the DCS of the Low Voltage powe supply is built up within the PVSS software. The actual working version, uses the CERN custom SLiC OPC server, which is to be replaced by the genuine Wiener OPC server as soon as the later will be available. The main drawback of the present solution is its limitation to the Wiener PL500 LV device while the Wiener OPC server should allow to manage Wiener crates.

The graphical user interface is made of a main panel which summarizes the LV status for each half plane of the trigger. Clicking into the representation of a half plane gives access successively to two panels, dedicated respectively to the survey and the setting of its LV power supply. The survey panel (see Fig. 34) displays the status of each channel with the corresponding date and time, and a button to set ON/OFF the crate. A green/red light shows the ON/OFF status. The settings are shown for information, and the monitored current and voltage are displayed, together with a green/red light. For each of them, a button allows to display the trending curve. Alarms are displayed by the way of pop-up windows to acknowledge. A button gives access to the alarm log file. The second important panel is accessed via a dedicated button. It allows to change the settings. Note that access control facilities will be attached to this button.

6 Characterization results

6.1 Chip evolution

The electronics presented in this document has been developed over four years. In other words, the final version of the ASIC described in section 3 and its associated boards is the fruit of several improvements. Table 10 summarizes the evolution of the main characteristics of this chip.

Table 10: Different versions of the ASIC developed at LPC Clermont-Fd.

Chip version	FEC1	FEC2	FEC3	FEC4 final version
Run foundry date	Jan. 2000	Jun. 2000	Nov. 2000	Apr. 2001
Delivery date	15/05/2000	22/09/2000	16/05/2001	18/09/2001
Number of channels	1	1	8	8
Low voltages values (V)	+3.5 / -3.5	+3.5 / -2.0	+3.5 / -2.0	+3.5 / -2.0
ADULT system	no	yes	yes	yes
Output signal standard	ECL	LVDS	LVDS	LVDS
Polarity implementation	outside	outside	outside	inside
Consumption per channel (mW)	140	100	75	86
Silicium area (mm^2)	3	9	7.8	8
Packaging	JLCC28	JLCC28	JLCC68	JLCC52

6.2 Test in laboratory

The performances of the final ASIC prototype have been evaluated with a dedicated test bench at LPC Clermont-Fd. The set-up is composed of a fast pulse generator able to output RPC like pulses, with an adjustable precursor to streamer delay. The signals are observed through a 1 GHz bandwidth oscilloscope. The chip is plugged in a FEB20.

6.2.1 Comparators

The low and high threshold voltages are set on the corresponding chip inputs, with the respective values of 10 mV and 80 mV. The sensitivities of the low and high thresholds comparators are tested with the method described for simulation, using the fast pulse generator. The tests are performed for the positive and negative polarity. The amplitude of the input pulses required to swing the output state of the comparators are given in table 11.

The sensitivity of the high threshold discriminator is quite smaller than the value obtained by simulation (+93 mV instead of +85 mV in positive polarity). However, this limitation can be easily compensated by increasing slightly the high voltage power supply

Table 11: Comparators sensitivity measurements.

Polarity	Threshold values	Precursor amplitude	Streamer amplitude
positive	$+10\,\mathrm{mV}/+80\,\mathrm{mV}$	$+12\,\mathrm{mV}$	$+93\,\mathrm{mV}$
negative	$-10\,\mathrm{mV}/-80\,\mathrm{mV}$	$-12\,\mathrm{mV}$	$-91\,\mathrm{mV}$

of the RPC in order to guarantee a good efficiency. The results obtained during beam tests which are reported below confirm that the sensitivity is adequate to the required detector performance.

6.2.2 ADULT system

Figure 35 displays the result of the test of the dual threshold discrimination technique carried out on one chip. The curves obtained with other chips are very similar. It is worth noticing that the precursor pulse gives the time reference until the streamer signal delay exceeds 18 ns, as it has been already observed in simulations.

Furthermore, the response time of the electronics is lower than the required value of 50 ns, in normal conditions ($\Delta_{p-s} < 15\,\mathrm{ns}$).

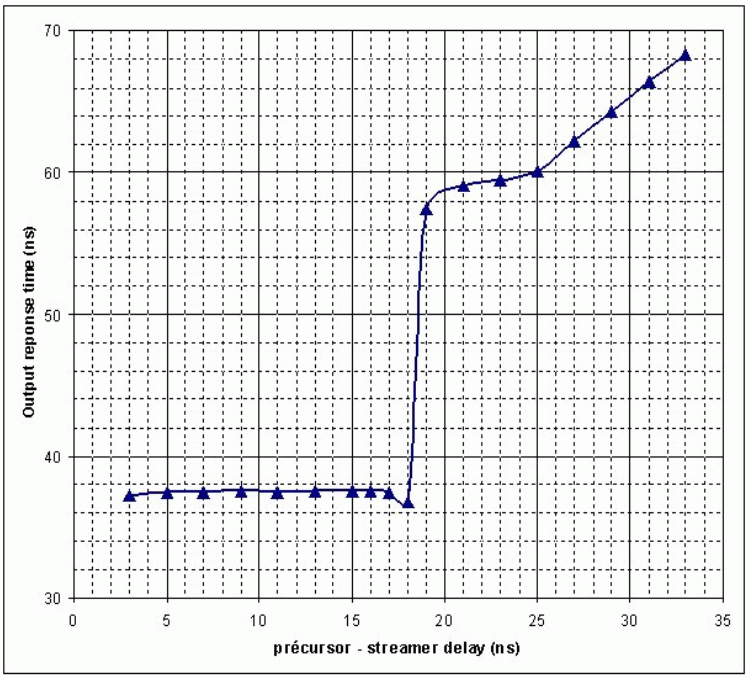


Figure 35: Test of ADULT system: absolute value for the response time.

6.2.3 One shot system

The one shot time measured value is 98 ns, which is very close to the 100 ns expected value.

6.2.4 Variable delay

Five different cable lengths are used to transmit the LVDS signals from the front-end electronics to the trigger electronics on the whole trigger set-up. The corresponding propagation time variation is compensated with the "variable delay" function implemented on the ADULT chip. This delay can be increased up to 37.5 ns using five 7.5 ns pitches. This function has been tested and the results for one chip channel are plotted in figure 36. Thus a very good linearity is observed, but the measured delay values are slightly lower than the expected ones (up to −0.7 ns). The required delay will be adjusted with a potentiometer on the test bench during front-end electronics checking.

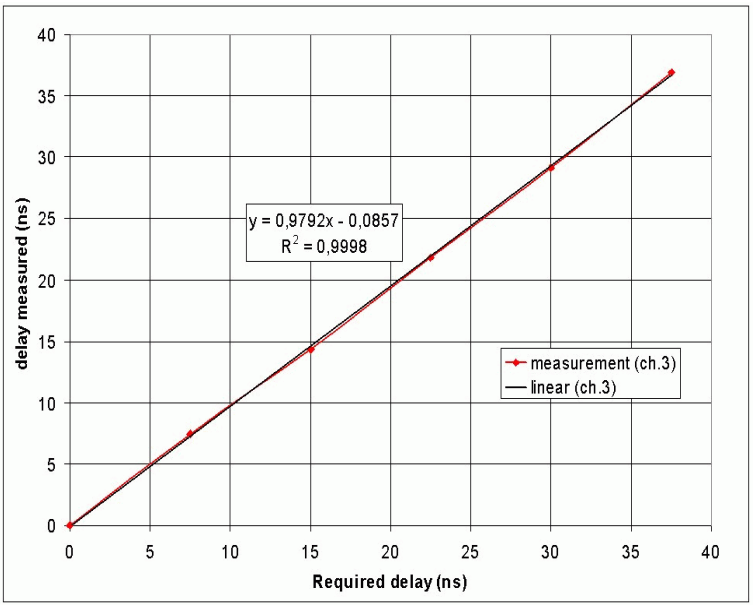


Figure 36: Test of the variable delay.

6.2.5 LVDS output signal

The measured LVDS output signals have the following features:

- width = 21 ns,
- differential amplitude = +380 mV/ − 430 mV,
- common mode = +1.3 V,
- transition time = 2.6 ns/3.4 ns.

These signals meet the LVDS specifications.

6.2.6 Temperature sensitivity

The global time response of the chip (Δt_{chip}) is a function of the room temperature (θ), as displayed on figure 37. The sensitivity coefficient measured with FEC4 is:

$$\left(\frac{\partial \Delta t_{chip}}{\partial \theta}\right) = (60 \pm 20)\,\mathrm{ps}/^{\circ}\mathrm{C}\,.$$

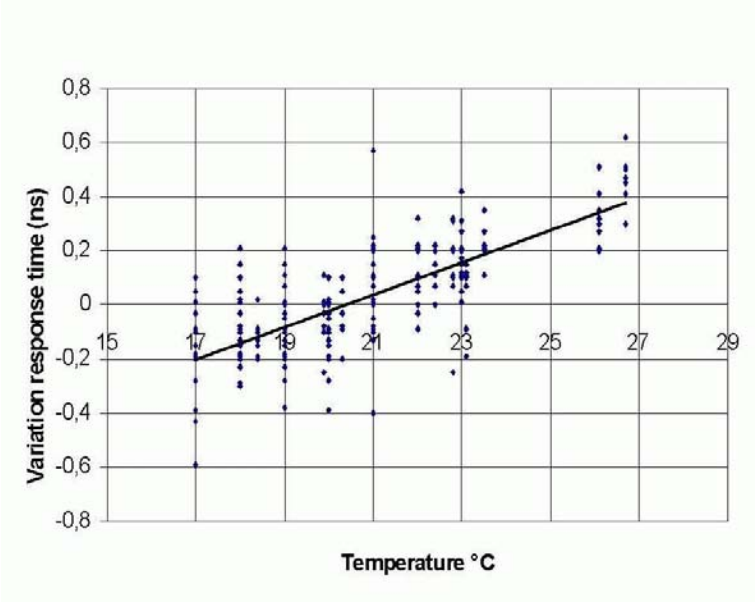


Figure 37: Global time response variation as a function of temperature (FEC4).

This experimental result is compatible with the simulated one ($\approx 37\,\mathrm{ps}/^{\circ}\mathrm{C}$).

Concerning the expected temperature in ALICE, no simulation has been done for the dimuon trigger detector. On the one hand, the global temperature in the ALICE pit (about 50 m underground) is not expected to vary in a large range over the seasons. On the other hand, especially between the two plans of a single station, the temperature will not be the same at top and bottom. Even if this temperature difference would be of 10°C, the variation of the chip response time would be of 0.6 ns only in the worst case.

6.2.7 Response time dispersion (between channels and between chips)

The time dispersion between the eight channels of a single chip is an important parameter to check. Figure 38 displays an example of response time fluctuations measured on one single chip, for five delay values. The observed time fluctuation of a group of eight channels never exceeds ± 1 ns, which is an acceptable value according to the timing requirements. Moreover, as already explained, the response time fluctuations between ASICs are compensated during the adjustment procedure on test bench.

6.2.8 Cross-talk

Precautions against cross-talk effects have been taken, when drawing the printed circuit board. It is composed of four layers, one of them being fully dedicated to the ground plane. Concerning the chip layout, input and output PADs are separated, and each one-channel block is isolated from its neighbours with contact connected to the bulk layer. As a result, no cross-talk has been observed on the front-end electronics, with amplitude input signals up to 3.5 V. This means that only one LVDS output swings when the corresponding input channel is fired.

6.2.9 External thresholds uniformity

The possibility to bring external thresholds on the front-end boards has been tested on a full size RPC equipped with 32 FEBs. The procedure is similar to the one used to send

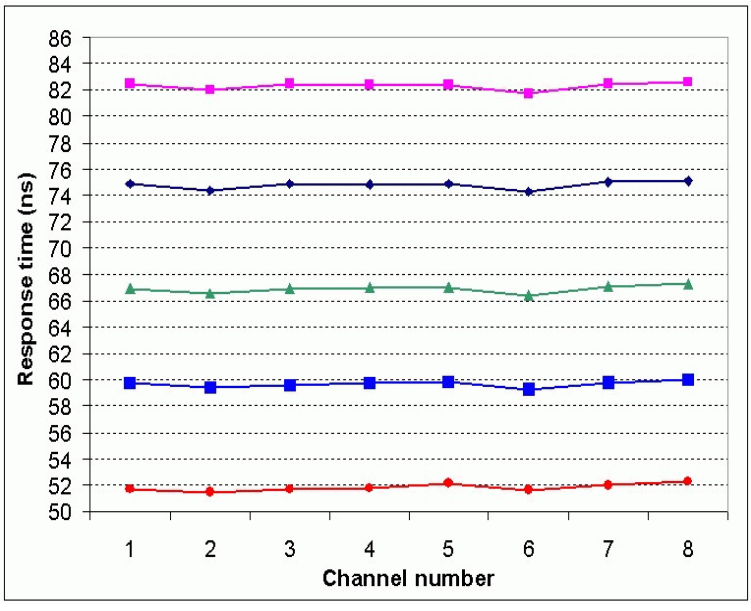


Figure 38: Response time dispersion (arbitrary absolute value) between the eight channels of the same chip (for five delay values).

the LVDS signal for the FET system, namely with 9 cables per RPC. Furthermore, as for the FET system, the cable used is the same than the output signal cable.

For a required value of 1 V on the boards (corresponding to 10 mV for the FECs), the maximum variation of the thresholds is: $\Delta U_{TH} = XX$ mV. This result corresponds to a non uniformity of YY %.

6.3 Beam tests at CERN

To validate in real conditions the working of the front-end electronics, several tests have been done at CERN with beams (π^- of 3 or 7 GeV at PS, and μ^- of about 100 GeV at SPS):

- FEC1 (8 chips 1 channel) at PS during June 2000 (for 15 days),
- FEC2 (8 chips 1 channel) at GIF during January 2001 (for 15 days),
- FEC3 (1 chip 8 channels) at GIF+SPS during June and October 2001 (for 7 + 15 days),
- FEC4 (20 chips 8 channels) at GIF+SPS during June 2002 (for 10 days).

Note that GIF [3] was used to provide background radiation environment, much greater than the one expected in ALICE.

The set-up of these tests was made of RPC prototypes $(50 \times 50)\,\mathrm{cm}^2$, with a trigger provided by means of scintillators.

Figure 39 displays examples of time distributions obtained with version FEC3 using the $(\pm 10, \pm 80)$ mV set of thresholds. In working conditions (8400 V), the time resolution in the peak distribution is: $\sigma_t^{peak} < 1$ ns. At lower high voltage (7800 V), a second structure is visible which corresponds to events triggering the FEE with the streamer peak, instead of the precursor peak (as described in Ref. [7]).

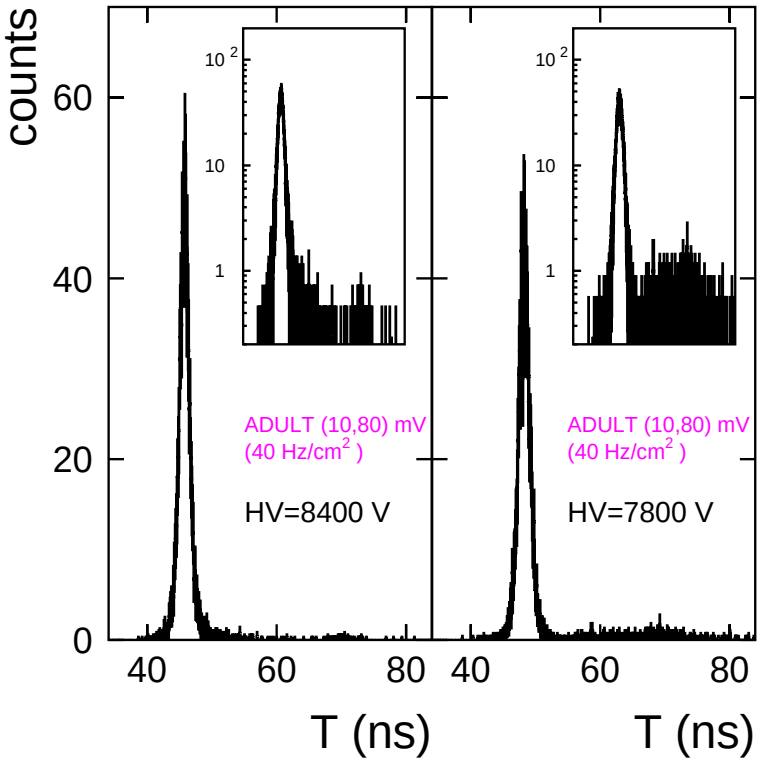


Figure 39: Time distribution of FEC3 chip at two different high voltages.

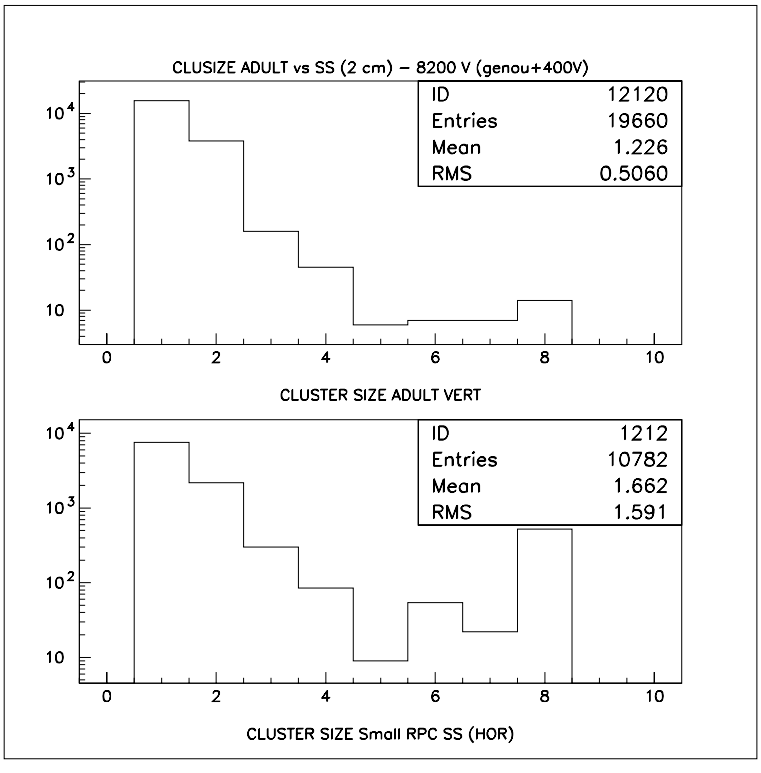


Figure 40: Cluster size distribution for 2 cm width strips for FEC3 with ground connectors on board (top), and for standard electronics (using single threshold) without special ground connectors (bottom).

Figure 40 illustrates typical cluster size distributions (number of adjacent strips fired) at 8200 V for a RPC using 8 strips of 2 cm width. Top figure displays the cluster size distribution for strips equipped with a front-end board (FEC3) and an adaptation board having two ground connectors; while bottom figure displays the same distribution for strips equipped with standard electronics (single threshold) and an adaptation board without special ground connection. Then, it is clear that the number of events with a lot of strips fired (very small probability as explained in Ref. [13]) is decreased when the grounding of the electronics board is carefully done. That means less cross-talk at the board level.

The main source of cross-talk comes from the capacitive coupling between strips.

The last beam test performed in June 2002 (GIF+SPS) was used to check the working of the dimuon trigger system in ALICE like conditions, namely with two stations of two RPC prototype planes in radiative environment. These RPCs were equipped with 16 strips of 2 cm width on each side. Thus, a total of 16 front-end boards (with FEC4) was used. Furthermore, the final output cables (25 m length) and a prototype version of the trigger electronics was also used. Then, the possibility to put correctly in time all the electronics channels ($20 \times 8 = 160$) in a window smaller than 1 ns has been demonstrated (for more informations, see Ref. [14]).

To conclude all the tests done with beams at CERN, a total of about 240 days of 1 channel chip (FEC1 and FEC2) and 220 days of 8 channels chip (FEC3 and FEC4) have shown a very good working of the front-end electronics. Moreover, cumulated over 20 chips, 700 days of 8 channels chip (FEC4) in cosmic rays at LPC Clermont-Fd have been performed without any problem.

6.4 Pre-serie production

6.4.1 Tests on bench

A pre-serie of 119 ASICs (50 ceramic packaging and 69 plastic packaging) and 40 front-end boards of station 1 (12 FEB11, 32 FEB21, 6 FEB41) has been produced beginning of 2003.

Seven of the 119 ASICs failed in the preleminary tests:

- 5 ceramic chips do not work (short circuit on power supplies, incorrect output signal for at least one channel) giving a production yield of 90 % for this type of packaging,
- 2 plastic chips have a bad working (twice the normal consumption for the negative LV, no low threshold discrimination on one channel) giving a production yield of 97 %.

Then, the performances of all the chips were measured on the same FEB to evaluate the dispersion of their characteristics. The same results are observed for the two types of packaging and then the retained solution is the cheapest, namely the plastic one. Figure 41 and table 12 show for the chips: the width and the amplitude of the output signal, the response time (delay), the high and the low thresholds sensitivities. From the results, we can see that the most critical parameter, the response time fluctuation window, respects the requirement of ± 2 ns before tuning on test bench (a smaller dispersion will be obtained after tuning). Others performances and dispersion are suitable with the readout electronics requirements.

[3] GIF (Gamma Irradiation Facility): Cs source delivering 662 keV γ rays.

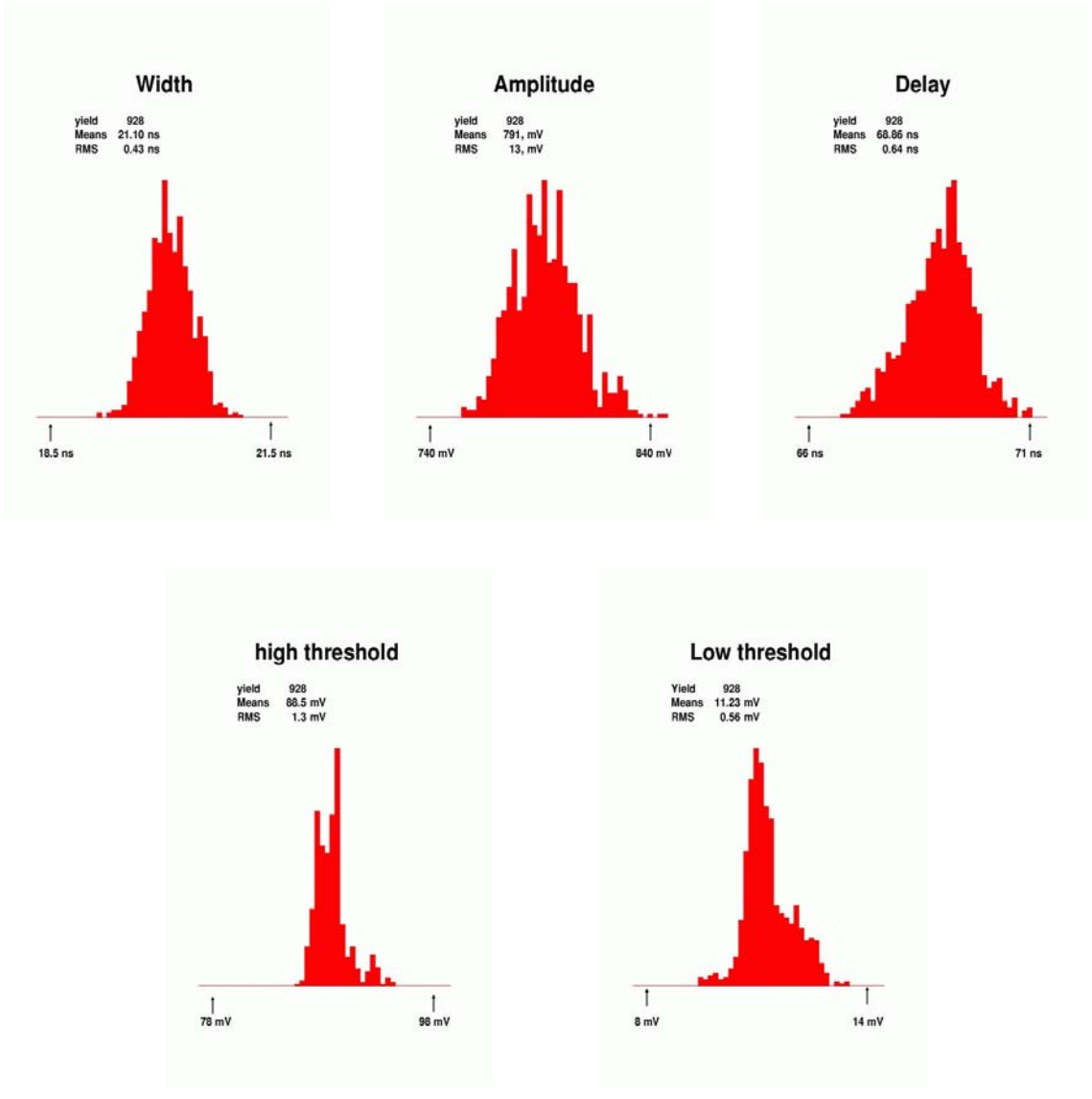


Figure 41: Pre-serie production results for: the width and the amplitude of the output signal, the response time (delay), the high (80 mV) and the low (10 mV) thresholds sensitivities.

Table 12: Results of the pre-serie test of the ASICs on bench (the error given corresponds to the RMS of the distribution).

Parameter	Measured values	Acceptable range
output signal width	(21.10 ± 0.43) ns	$19 - 23$ ns
output signal amplitude	(791 ± 13) mV	$700 - 900$ mV
response time (delay)	(68.86 ± 0.64) ns	$67 - 71$ ns
high threshold	(88.5 ± 1.3) mV	$85 - 95$ mV
low threshold	(11.23 ± 0.56) mV	$9 - 13$ mV

The cabling of the boards was done by a manufacturer to evaluate the production rate. No problem has been noticed for the 40 FEBs tested on bench.

6.4.2 Tests on RPC

A part of this electronics (32 FEBs using 40 FECs) has been installed in April 2003 at Torino on a final full scale prototype (called RPC1), as displayed in figure 42. The goal of this experiment is to test the characteristics of an ALICE like RPC, particularly in term of uniformity. A preliminary test was performed in cosmics at Torino, next the RPC was exposed under SPS beam with background environment at GIF in August-September 2003.

The timing peformances of the whole readout electronics chain was estimated by using the RPC1 setup. In this setup, the Front-End Test system, triggered by a pulsed generator, light up all the 320 electronics channels throught a dedicated 25 m twisted pairs cable. The on board FET system generates streamer like pulse to chip inputs. Then, each readout cable transmites LVDS signal to the acquisition system.

Through the whole chain, all the 320 electronics channels are in a window of 12 ns. This result is in agreement with the requirement: a FET signal jitter of 6 ns + a FEB dispersion of 4 ns + an output signal cable dispersion of 3 ns.

The consumption was measured when the FET system is on. No increase is observed up to a frequency of 1 MHz for the FET pulse (consumption of 1.6 A for the negative voltage and 8.2 A for the negative voltage). At 5 MHz, the consumption increase by about 6 %. The maximum expected rate in ALICE is about 40 Hz/cm^2 near the beam pipe. For longest strips of 22.6 mm width (720 mm length), the maximum rate will be of about 6.5 kHz. Furthermore, it is expected to use the FET system with a frequency of about 1 kHz. So only the static consumption can be considered for the power supply distribution study.

During the beam test at CERN (SPS + GIF) in August-September 2003, first evaluation of electromagnetic compatibility have been performed by F. Szoncso from the CERN Technical Inspection and Safety (TIS) division. All the measurements were done with the readout electronics under power, but with the high voltage of the RPC off. The first operation was to measure the noise (common mode current) at the end of the 25 meters output signals used. A peak at 250 kHz, attributed to low voltage switched power supplies in near racks, was noticed; and a serie of peaks at several MHz. After that, a common mode current of 30 μA (1 V) has been generated around signal cable, up to 1 GHz. Then no change of the output logical state was observed at the end of the signal cables. The same things was done at the level of the low voltage cable, and no significant signal were observed on the output cables. The conclusion is that the filtering on the FEBs and the shielding of the output cables are efficients.

Moreover the voltage noise on the strips was measured with a scope. The result is about $\pm$2 mV, which is much lower than the low threshold of 10 mV.

With the chamber off, and the threshold of the two comparators of the ADULT system put to the same value, it has been observed that the electronics is triggered when the threshold reach down a value of 3 mV for the positive boards and 7 mV for the negative boards. This difference is due to the sensitivity difference already observed between the two polarities at the level of the simulation of the ASIC.

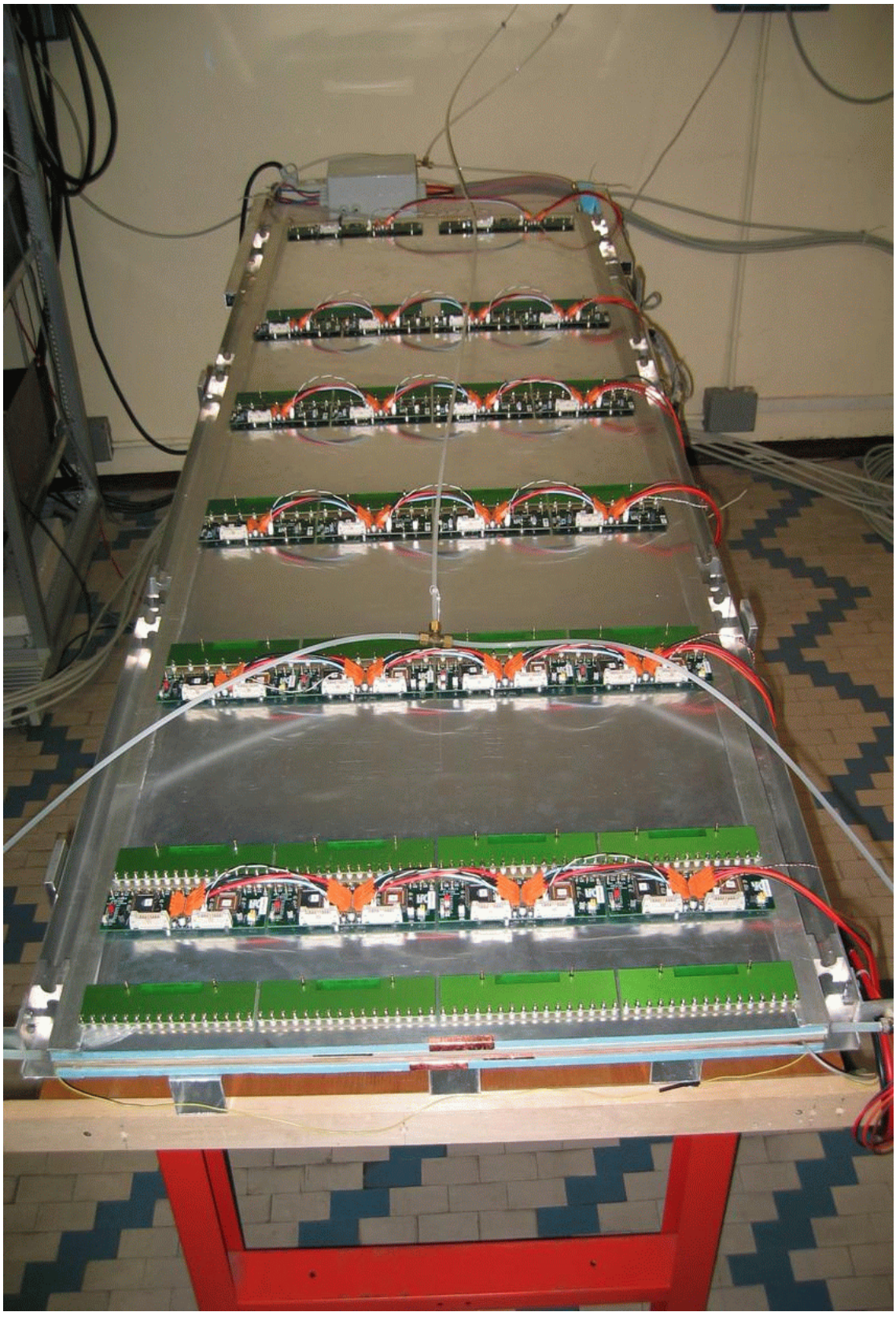


Figure 42: Pictures of the full scale RPC1 prototype equipped with final front-end electronics.

6.5 Radiation hardness

Concerning the radiation aspects, three campaigns of test have been performed [15]. The goal of these tests is to evaluate the radiation hardness of the front-end electronics with respect to different possible effects in the ALICE working environment:

- The cumulative effects due to low and medium energetic neutrons and to ionising particles (such as photons) which detoriate progressively the electronics components.

- The Single Event Effects (SEE) due to energetic hadrons ($> 30\,\mathrm{MeV}$) which involve a bad working of the components or destroied it. In this case, severals effects can be distinguished:

  - the Single Event Upset (SEU) creating bit inversions in memories,
  - the Single Event Latch-up (SEL) creating a short-circuit in the component,
  - the Single Event Transient (SET) causing false electronics signals.

For each irradiation, a FEB11 was chosen in order to have two ASICs tested in the same time, and different boards was used for each campaign. During the irradiation, RPC like pulses were send on the input board to check the working of the ASICs and regularly the FET system was started up to check its working. Furthermore, the consumption was continuously measured for the two voltages.

6.5.1 Neutron test

A first irradiation to neutrons of 14.1 MeV was done with the neutron generator of our laboratory in April 2003. The main characteristics of this generator and the irradiation conditions was the following:

- neutron intensity $= (1.4 \pm 0.4) \times 10^8\,\mathrm{n/s}$ in a solid angle of 4π,

- distance between the source and the board = 6.6 to 11.2 cm from the center to the edges of the board,

- maximum flux $= 2.6 \times 10^5\,\mathrm{n/cm^2 s}$ near the middle of the board,

- irradiation time = 42.5 h in 5 days of about 8.5 hours.

Fig. 43 gives the total fluence received by the board on its two sides. For the components on the board, the total fluence varies between $2.5 \times 10^{10}\,\mathrm{n/cm^2}$ for the ASICs and $3.8 \times 10^{10}\,\mathrm{n/cm^2}$ for the LV regulators.

Five PIN diodes [4] to meausure the dose received by the components were placed at several positions on the board. The result is a dose between 1.5 Gy and 2.5 Gy for the main components (ASICs, LV regulators and integrated circuit of FET).

[4] The PIN diodes are from the society FIMEL. The principle consists to measure the indirect current of the diode before and after irradiation, next this difference is converted in absorbed dose.

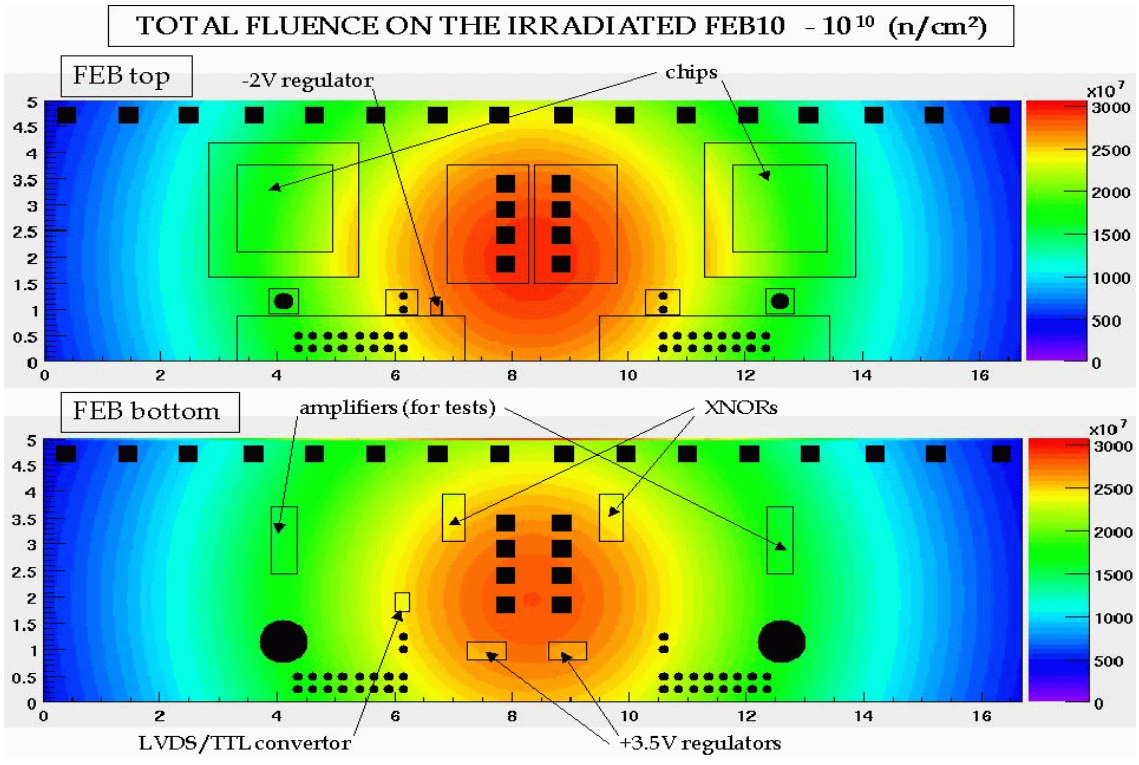


Figure 43: Total neutron fluence received by a FEB11: top map for the upper side of the board and bottom map for the lower side.

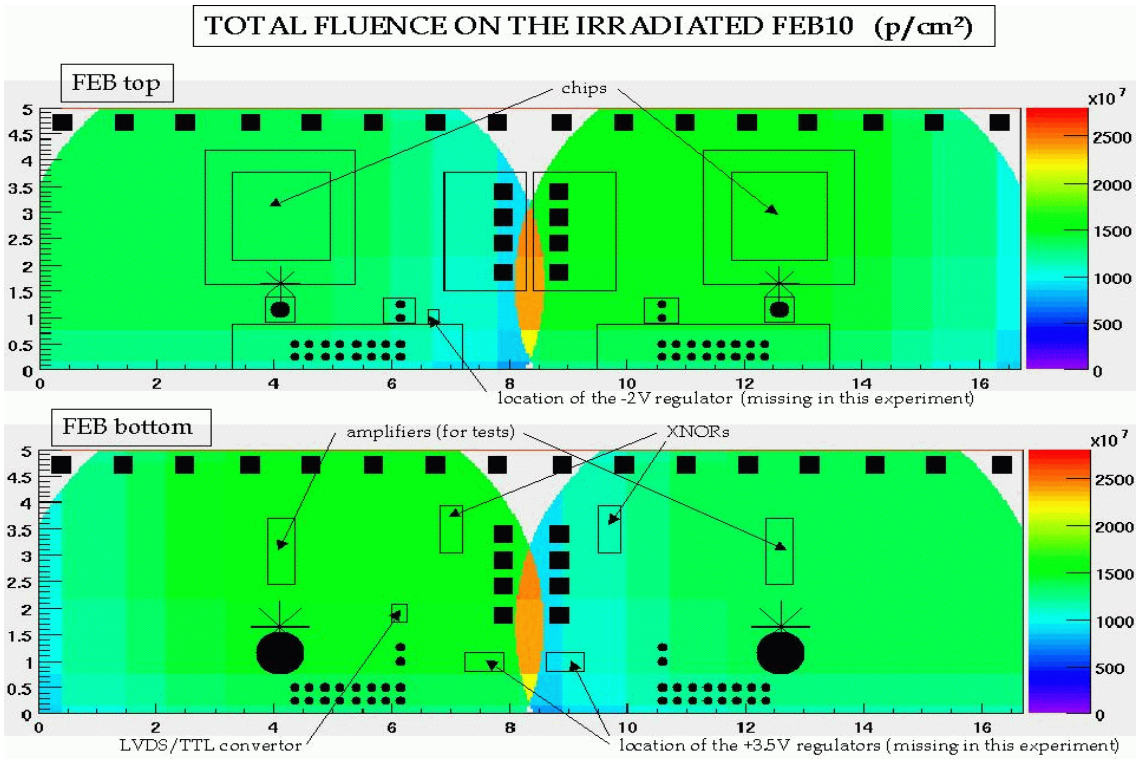


Figure 44: Total proton fluence received by a FEB11 for the test 1 and 2 combined: top map for the upper side of the board and bottom map for the lower side.

6.5.2 Proton test

A test to energetic protons (E_p = 60 MeV) was performed. This test was the only required by the referees during the PRR review to evaluate the possible SEE (particularly SEL) for the electronics. The test was done at the Paul Scherrer Institut (PSI) of Zürich in May 2003.

Table 13 summarizes the irradiation conditions and the total exposure and Fig. 44 shows the total proton fluence received by the board used for the two first tests.

Table 13: FEE irradiations to energetic proton of 60 MeV at PSI-Zürich with a beam diameter of about 9 cm.

Test number	1	2	3	4
proton flux	10^7 p/cm^{2}s	10^7 p/cm^{2}s	0.8×10^8 p/cm^{2}s	1.4×10^8 p/cm^{2}s
exposure time	26 mn	21 mn	42 mn	25 mn
maximum total fluence	1.32×10^{10} p/cm^2	1.43×10^{10} p/cm^2	1.08×10^{11} p/cm^2	2.38×10^{11} p/cm^2
electronics components exposed to beam	1 ASIC (FEC)	1 FEC + FET	LV regulators	all components

6.5.3 Photon test

As mentionned in section 6.3, several boards have equipped chambers during ageing test at GIF. The Gamma Irradiation Facility (GIF) is a Cs source of 0.7 GBq delivering γ of 662 keV. This means that the electronics has been put under γ radiations during several months with a rate of about 10 Hz/cm^2.

Furthermore, a specific test with one board was carried out. The board was positionned at 30 cm from the source, then exposed to a flux of 6.2×10^4 γ/cm^{2}s, during 10 hours. The total fluence on the board was 2.22×10^9 γ/cm^2, and the dose received was 0.25 Gy.

6.5.4 Conclusion

No effect have been observed during the three irradiation campaigns excepted a small drift of the low voltage delivered by the regulators under energetic protons irradiation (test 3), as displayed in figure 45. Nevertheless, the working of the others electronics components is not affected. Figure 46 shows the response time of the most irradiated board (test 4) before and after irradiation with proton beam. The behaviour is very similar between the two curves, indicating that the timing performances of the ASIC are not affected.

Table 14 gives a comparison between the performed tests and the expected radiation level in ALICE for 10 LHC years. From this results a minimum life time for the front-end electronics with respect to the radiation hardness can be given:

$$\tau_{FEE} > 15 \quad \text{LHC years}\,.$$

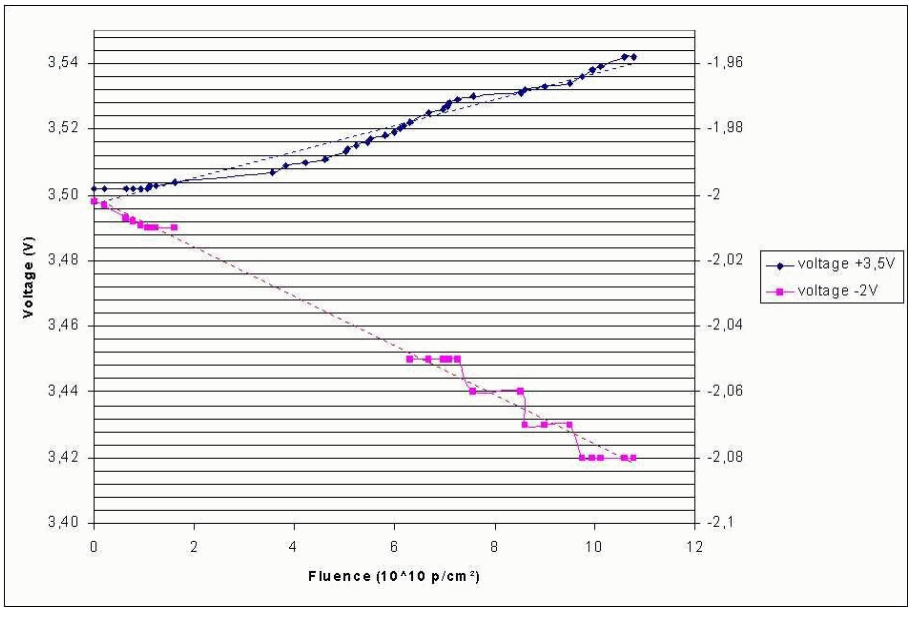


Figure 45: Evolution of the low voltage delivered by two regulators during the proton irradiation: MAX1818 for +3.5 V and LT1964 for −2.0 V.

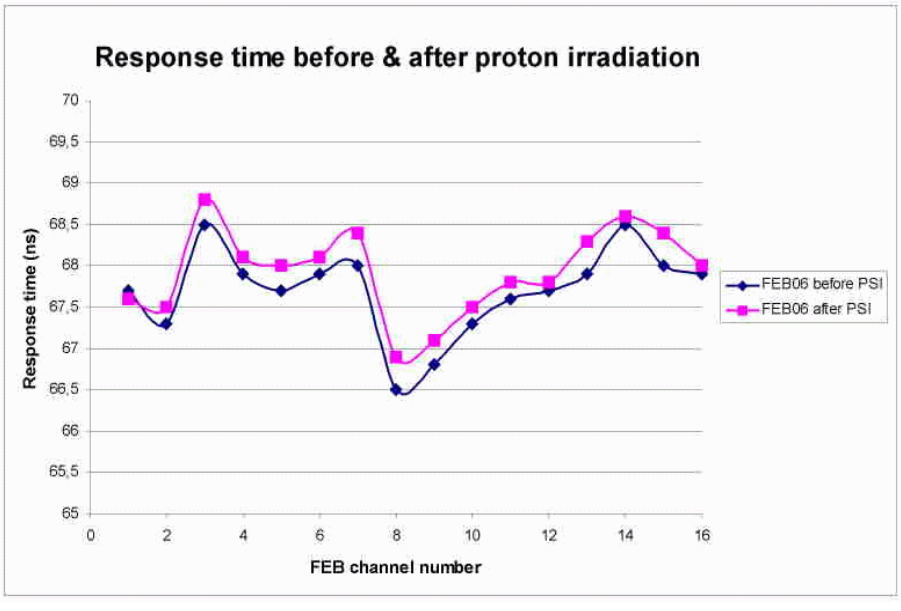


Figure 46: Response time for the 16 channels of a FEB11 (test 4 at PSI) before and after irradiation with proton beam. The fluence was: 2.38×10^{11} p/cm^2.

Table 14: Confidence level of the FEE radiation hardness by comparison between the expected rate and the performed tests.

Radiation type	Expected level in ALICE (10 yr)	FEE radiation test	Life time in LHC years
neutrons	1.4×10^9 n/cm^2	2.5×10^9 n/cm^2	17.9
neutrons (absorbed dose)	1 Gy	1.5 Gy	15
energetic nucleons	$< 1.4 \times 10^9$ p/cm^2	2.4×10^{11} p/cm^2	1714
photons	1 Gy	0.25 Gy	2.5

7 Test bench and maintenance

7.1 Test bench design

The test bench is aimed to characterize all the channels of all the FEE (chip on its board) after production. The characterization is done by measuring the main parameters of the chips, see table 15, and by checking their values in a given range. The tolerance range is set according to the electronics performance requirements.

Table 15: List of parameters checked on test bench (L.T. means low threshold and H.T. means high threshold). Note that the response time is initially tuned with the potentiometer (on the board).

Parameter under test	Expected value	Tolerance
LVDS signal differential amplitude	800 mV	±100 mV
LVDS signal width	22 ns	±2 ns
Response time (medium delay: 22.5 ns)	60 ns	±2 ns
L.T. discrimination sensitivity	(10 + 1) mV	±2 mV
H.T. discrimination sensitivity	(80 + 10) mV	±5 mV
Oneshot	100 ns	±10 ns
Precursor-streamer maximum delay $\Delta t_{p-s\,max}$	15 ns	±2 ns
Response time for $0 < \Delta t_{p-s} < \Delta t_{p-s\,max}$	60 ns	±1 ns
Response time jump for $\Delta t_{p-s} = \Delta t_{p-s\,max} + 2\,\text{ns}$	20 ns	±3 ns
FET	OK	

In order to test over 2600 electronics boards, it has been necessary to develop a special test bench. The principle of the test bench, displayed in figure 47, is to do, as far as possible, an automatic characterization. In this scope, the test bench uses: a pulse generator to simulate RPC like analog signals (with a 2 ns rise time), a low voltage power supply for the board, a digital oscilloscope to analyze the input and output signals (500 MHz bandwidth), and a multimeter to control the consumption of each board. A system of input and output relaies allows to test individually each of the 8 channels of up to two chips. The whole test bench is operated by a computer system running the LabView software. It monitors the apparatus via a GPIB Bus and the relaies via a DIO card.

The number of boards to test will be, half for the MT1 station and half for the MT2 station (namely 6 different board types):

- 240 FEB10 with two ASICs each,
- 1504 FEB20 with one ASIC each,
- 640 FEB40 with one ASIC each.

The spares are not included.

The chosen solution is a test bench made of a relay board able to test either: one FEB10, or one FEB20, or one FEB40. Furthermore, for each type of board (FEB10,

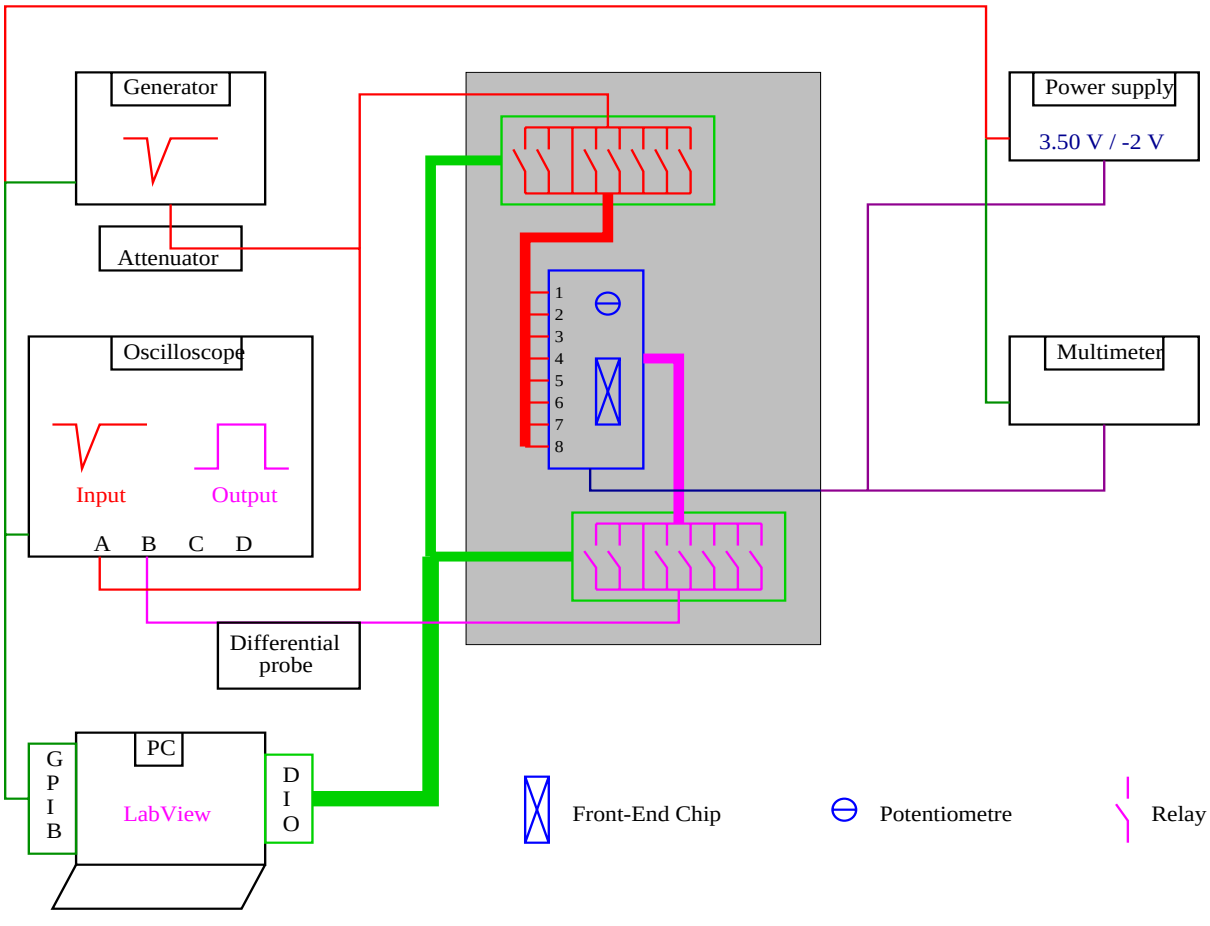


Figure 47: Architecture of the FEE test bench.

FEB20 and FEB40), it is possible to test either a board of station MT1 or a board of station MT2.

Figure 48 displays the actual prototype of the relay board. The input signal is sent to the lower central connector (the left one), while the right one allows to have a control of the input signal (on an oscilloscope) send to the FEB. A set of 16 relaies allows to select the input channel of the FEB. The output signal is picked-up with the differential probe, the 16 output relaies allowing to select the corresponding channel. The two DIO buses (on the right) command the input and output relaies, and also those used to measure the power supply voltage of the board, its current consumption and the room temperature. The three connectors on left bring the low voltages for the FEBs and for the 38 relaies.

To ease the maintenance of the FEE, each board will be identified (for instance with a magnetic bar code) and its characterization parameters will be stored in a file (fig. 49).

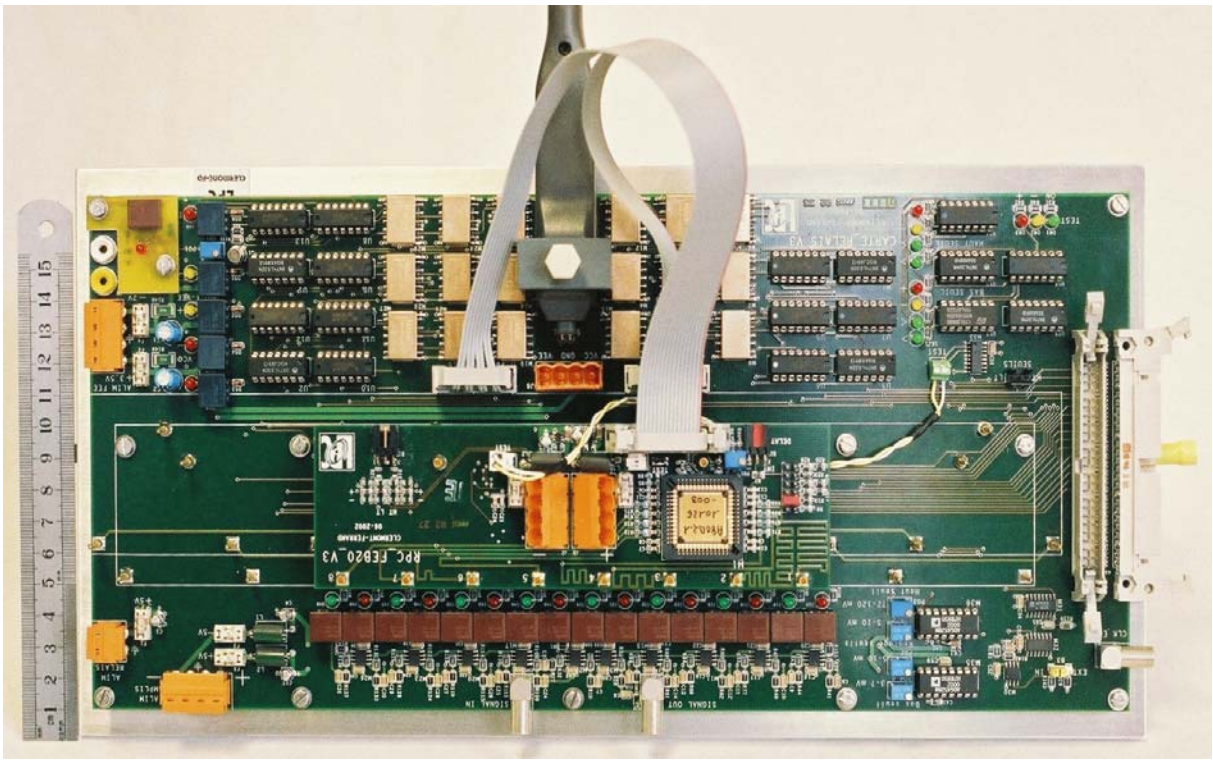


Figure 48: Prototype relaies board designed to test the FEE (a FEB20 is plugged in).

7.2 Single point failures and maintenance

Technical daily stop every 24 hours to allow rapid access to underground equipment is foreseen during the LHC operation [17]. Presently it seems that one hour will be enough to change the less accessible boards, thus a burn-in of the FEB is not necessary.

The test bench will be maintained over the whole ALICE lifetime for controls and repairs of the front-end electronics.

The effect of single point failures of the FEE system has been estimated, see table 16 for FEB20 (FEB40) and table 17 for FEB10. The worst case happens when a regulator is in short circuit. In this case the FEE is out for a whole half plane. Note that the same situation is reached when a LV unit is off.

Début du test	09/09/02	16:59	3s								
Polarisation	Négative										
Codes Barres	0										
Mes. tension	CH1	-1.99E+00	CH2	3.59E+00							
Mes. intensit	CH1	4.63E-02	CH2	1.66E-01							
Température	7.9										
Validité voie	Voie	Largeur	Amplitude	Retard2	One Shot	Seuil Haut	Seuil Bas	Retard1max	Val saut Ret2	Var max Ret2	Test de var al
		ns	mV	ns	ns	mV	mV	ns	ns	ns	
Bonne	1	21.3	790	66.4	100	78.8	15	13	22	2.5	0
Bonne	2	20.8	800	66	100	83.4	16.9	13	21.4	3.1	0
Bonne	3	17.8	790	66.6	95	83.4	13.1	13	21.2	2.7	0
Bonne	4	17.8	772	65.9	100	85.3	14.1	12	20.5	2.8	0
Bonne	5	21.2	773	66.5	100	85.3	15	13	21.7	2.9	0
Mauvaise	6	20.9	791	66.4	100	85.3	17.8	13	21.5	2.7	0
Mauvaise	7	17.1	769	66.7	100	82.5	16.9	13	21.5	3.2	1
Bonne	8	19.4	766	67.3	100	83.4	14.1	13	21.2	2.4	0
Fin du test	09/09/02	17:15	56s								

Figure 49: Example of Excel file sheet (for one chip) to store the characterization results of the test bench.

Table 16: Single point failures for FEB20 and FEB40.

Components	Reference	Short circuit	Open circuit
ASIC ADULT	M1	No read out signals of 8 strips	No read out signals of 8 strips
MAX1818	M6,M9	LV tripped, no read out signals of the whole half plane	No read out signals of 8 strips
Fuse	F1		No read out signals of 8 strips
Input capacitors of LV regulators	C43,C47	LV tripped, no read out signals of the whole half plane	No AC power supply filtering
Strip resistor (51 Ω)	R68-R75	No read out signal on one strip	Higher strip signal amplitude
LVTH244	M5	No signal test on one ADULT chip inputs (8 channels)	No signal test on one ADULT chip inputs (8 channels)
MAX9111	M4	No signal test on the FEBs group (64 channels max)	No signal test on the 2 ADULT chips inputs (8 channels)
CD74HC7266	M8	Bad polarity of the FET signals (8 channels)	No signal test on one ADULT chip inputs (8 channels)

Table 17: Single point failures for FEB10.

Components	Reference	Short circuit	Open circuit
ASIC ADULT	M1	No read out signals of 8 strips	No read out signals of 8 strips
MAX1818	M6,M9	LV tripped, no read out signals of the whole half plane	No read out signals of 16 strips
Fuse	F1		No read out signals of 16 strips
Input capacitors of LV regulators	C43,C47	LV tripped, no read out signals of the whole half plane	No AC power supply filtering
Strip resistor (51 Ω)	R35,R39, R43,R47, R53,R61, R65,R68, R71,R74, R77,R80, R83,R86, R89,R92	No read out signal on one strip	Higher strip signal amplitude
LVTH244	M5	No signal test on one ADULT chip inputs (8 channels)	No signal test on one ADULT chip inputs (8 channels)
MAX9111	M4	No signal test on the FEBs group (64 channels max)	No signal test on the 2 ADULT chips inputs (16 channels)
CD74HC7266	M8	Bad polarity of the FET signals (8 channels)	No signal test on one ADULT chip inputs (8 channels)

8 Milestones and conclusions

Table 18 and figure 50 summarize respectively the milestones for LHCC and the general planning of the FEE (chips, boards, test bench, low voltages, signal cables). The remaining tasks are planned from the beginning of 2002 up to installation in the ALICE pit (UX25) at CERN and commissioning of the whole dimuon trigger system.

Table 18: Milestones of the front-end electronics for LHCC.

Task	Date
Production Readiness Review	28/11/2002
End of production	30/12/2003
End of test - Ready to install	30/03/2004

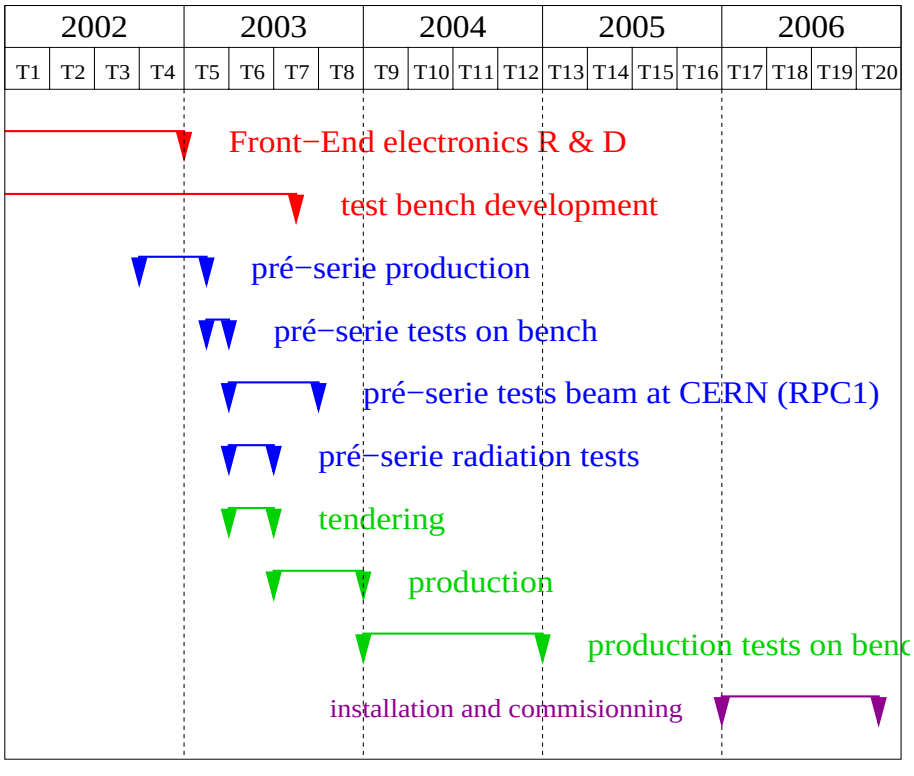


Figure 50: General planning for the front-end electronics.

To conclude, this document has presented a technical design report of the front-end electronics of the dimuon trigger system in its final version before production. This electronics is the fruit of several years of work (five years of R&D), without taking into account the four coming years before its implementation in the experimental area. During this R&D period, the requirements have been reached, and the various tests in laboratory and with beams at CERN have demonstrated the good performances and reliability of the front-end electronics system.

A Strips segmentation

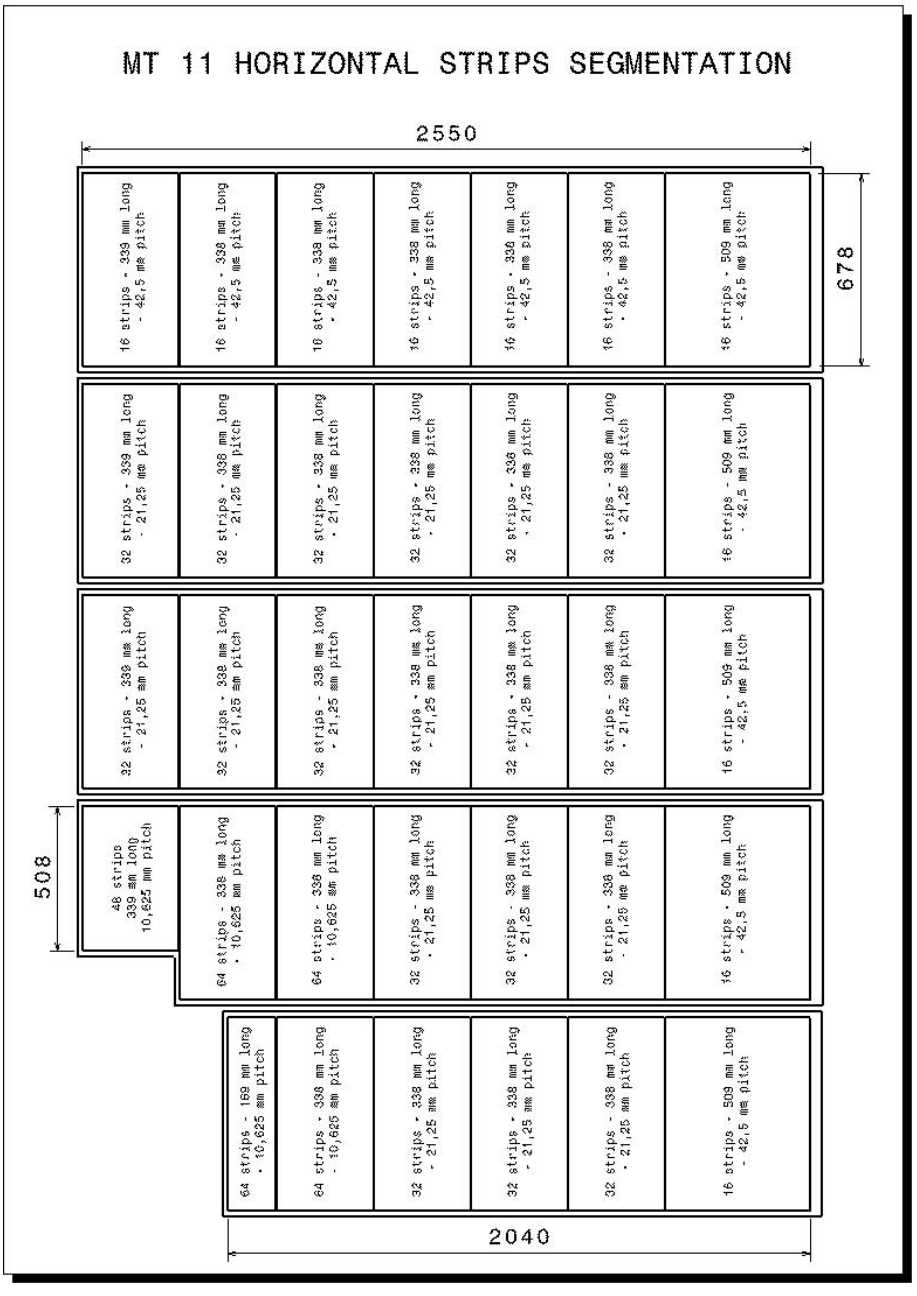


Figure 51: Quarter plan layout for horizontal strips (X).

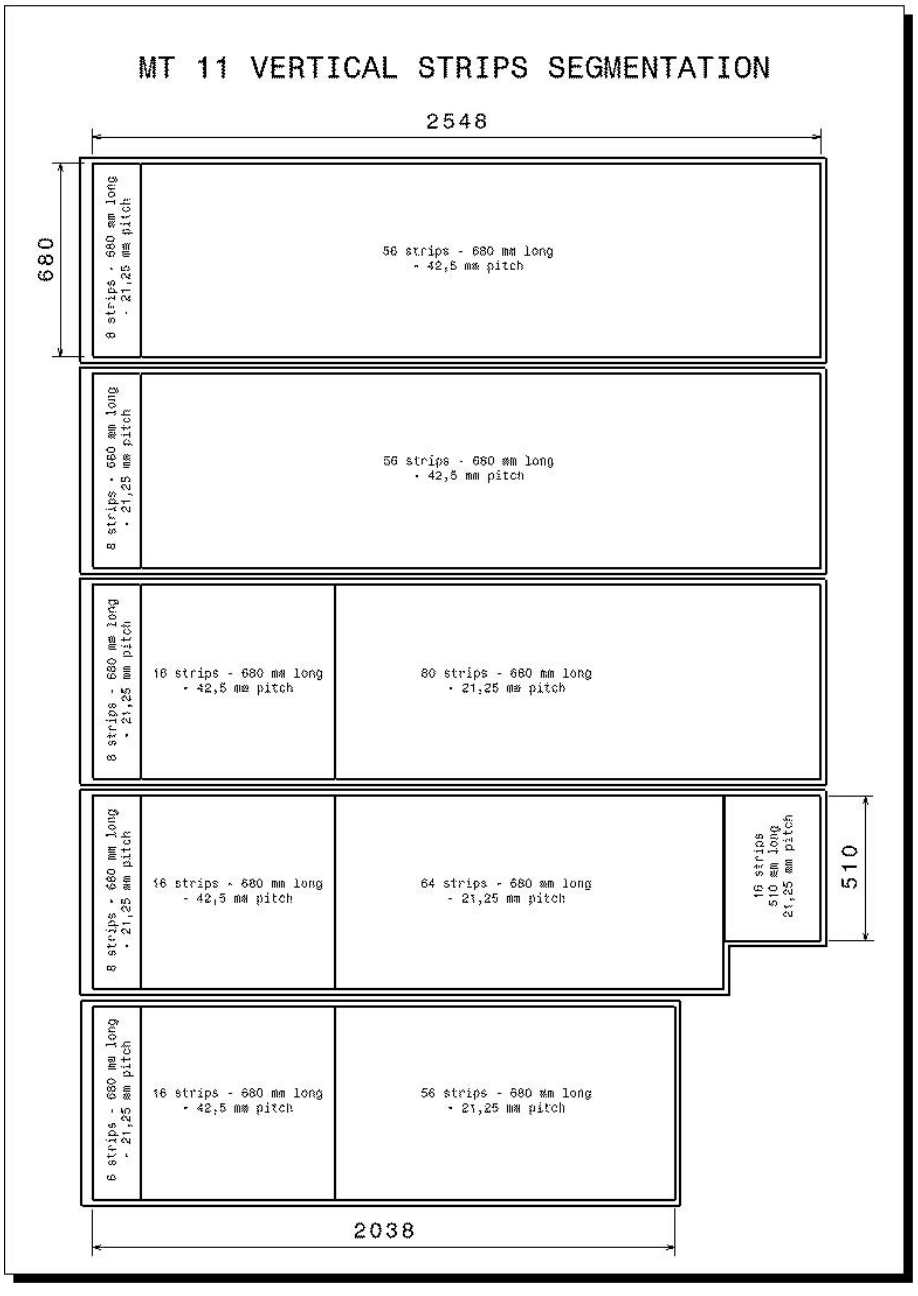


Figure 52: Quarter plan layout for vertical strips (Y).

B Front-end chip electronics schemes

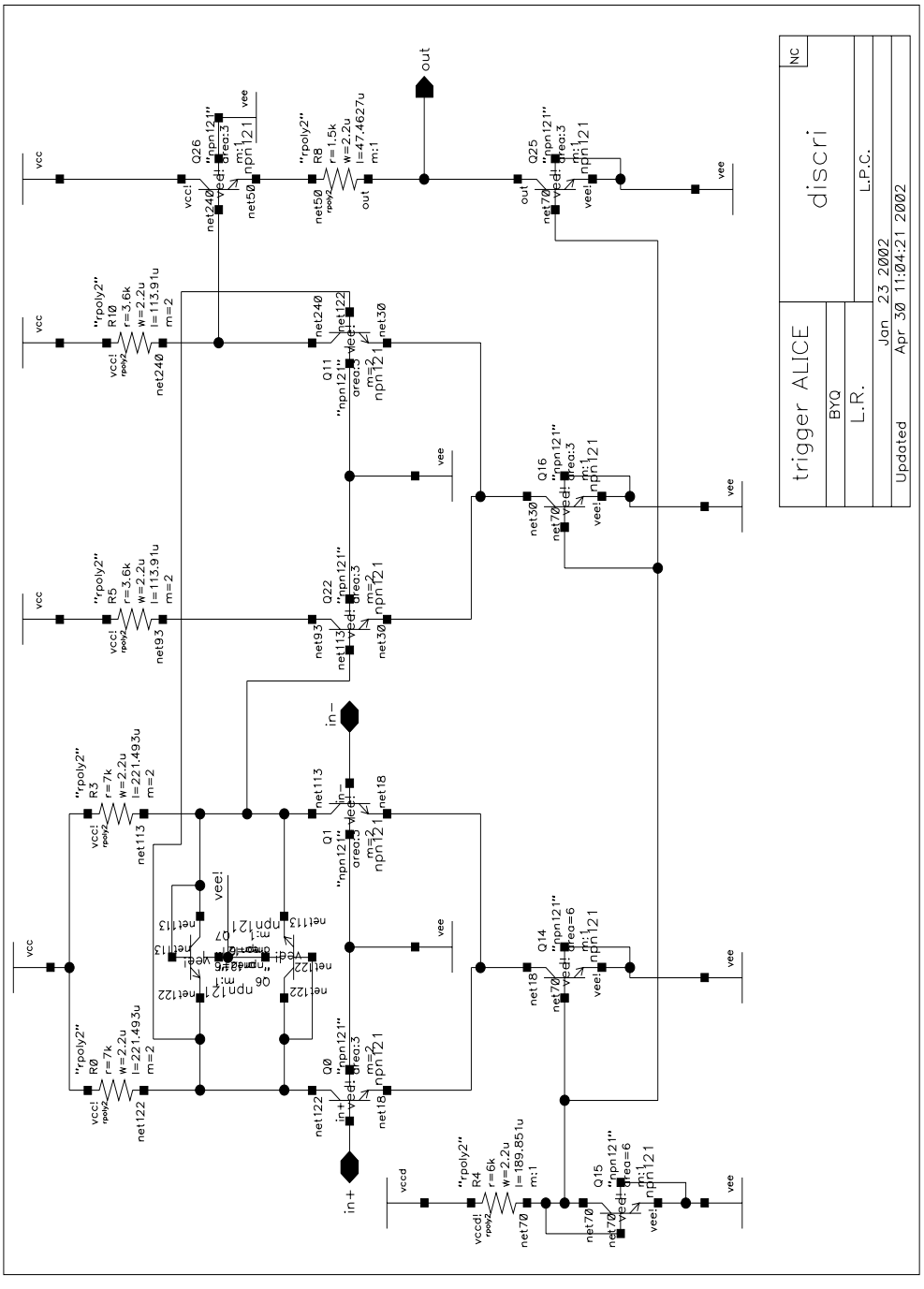


Figure 53: Comparator electronics schematic view.

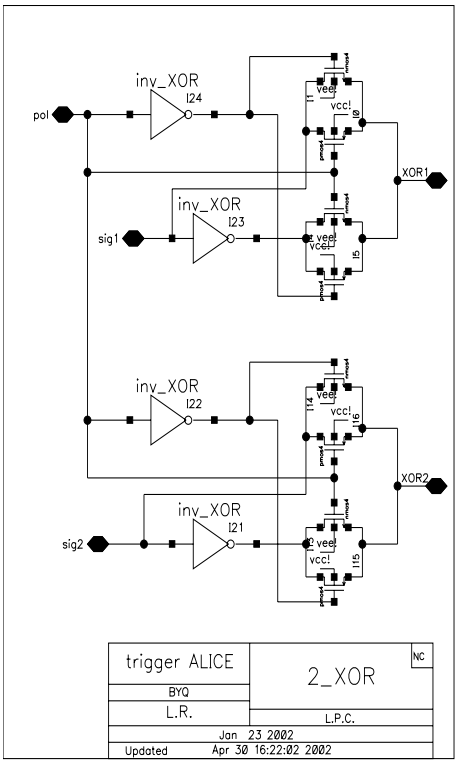


Figure 54: Electronics scheme for the polarity inversion.

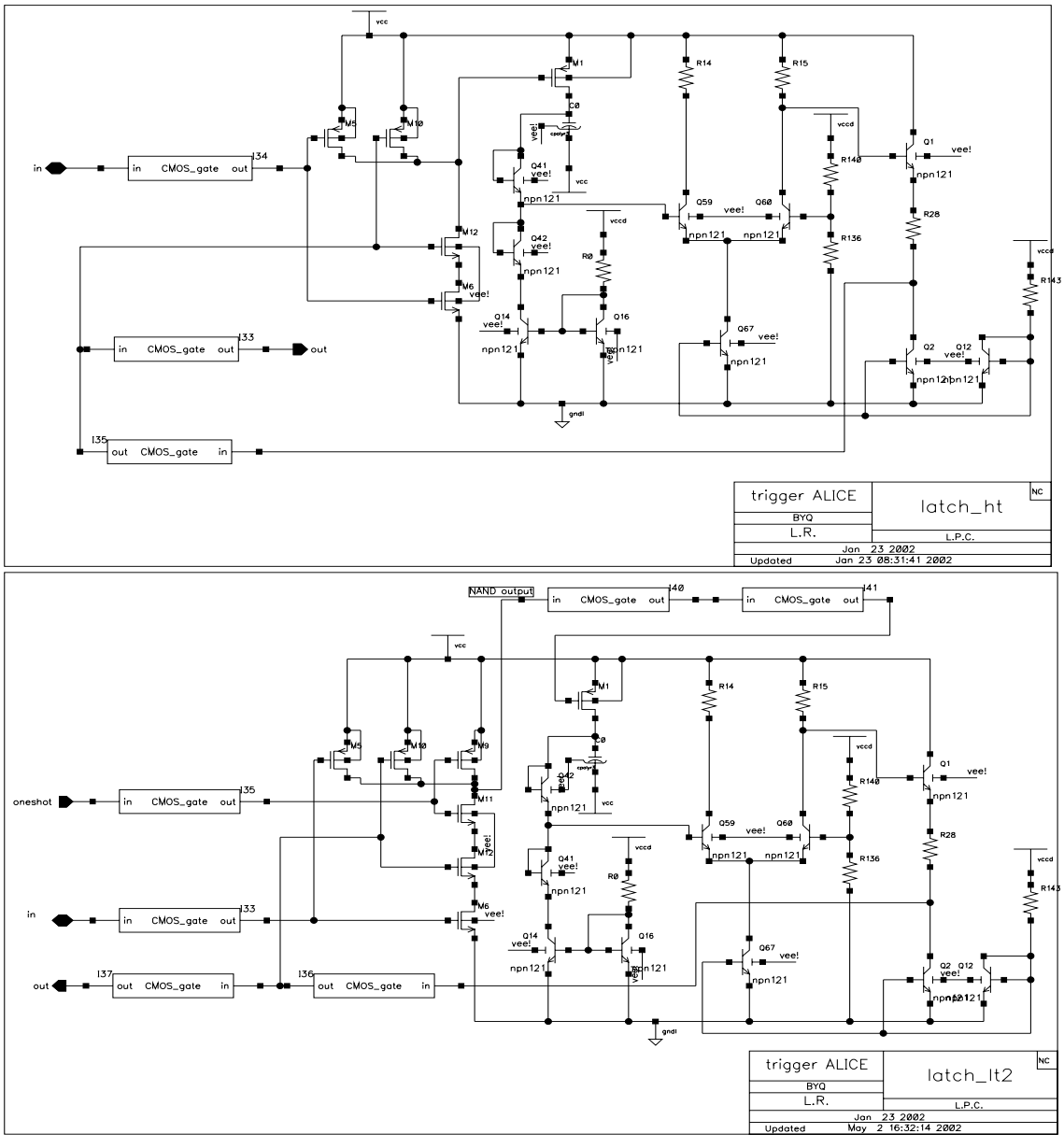


Figure 55: Latching blocks electronics schemes: upper for the high threshold (latch_ht) and lower for the low threshold (latch_lt2).

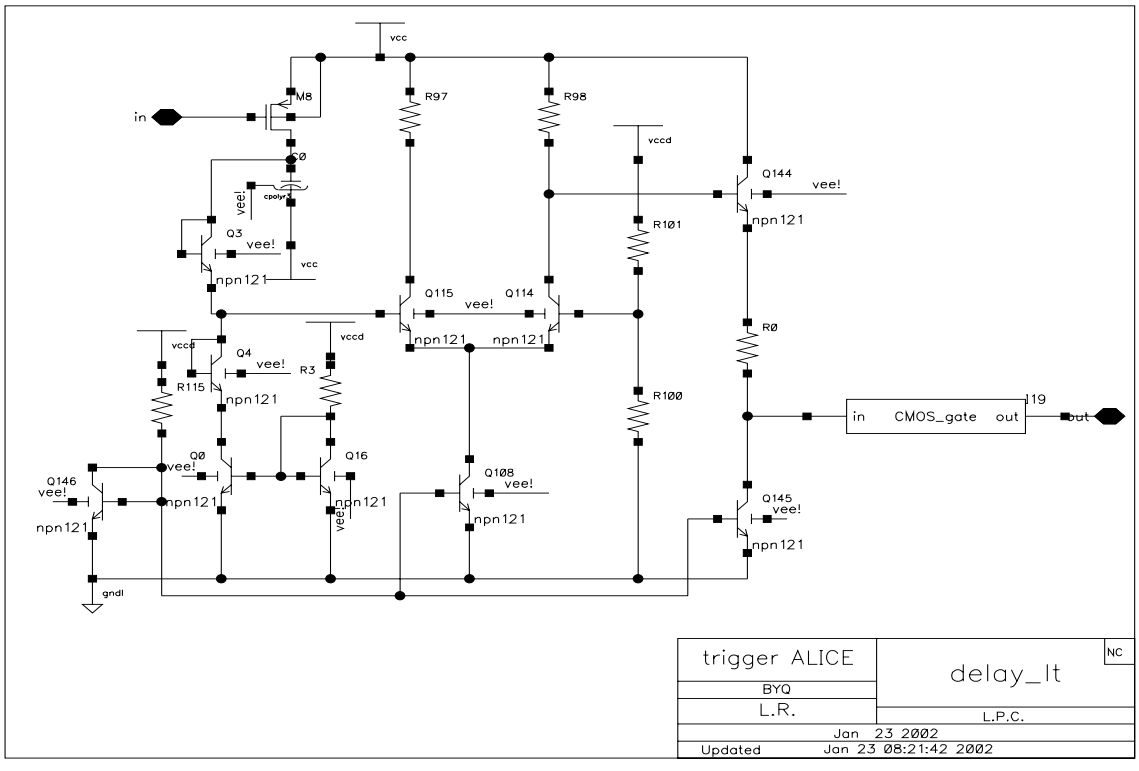


Figure 56: Electronics scheme of "delay_lt" block.

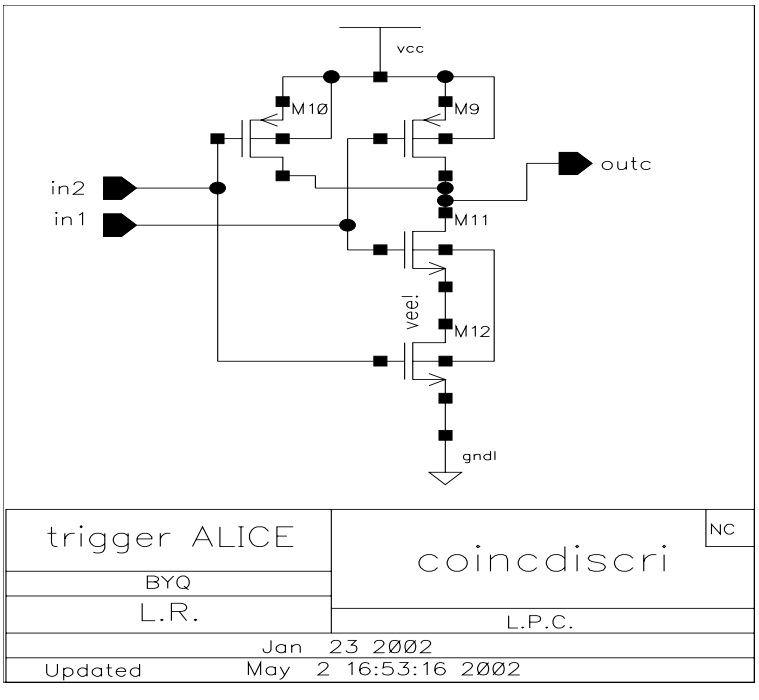


Figure 57: Electronics scheme for the coincidence of discriminator signals.

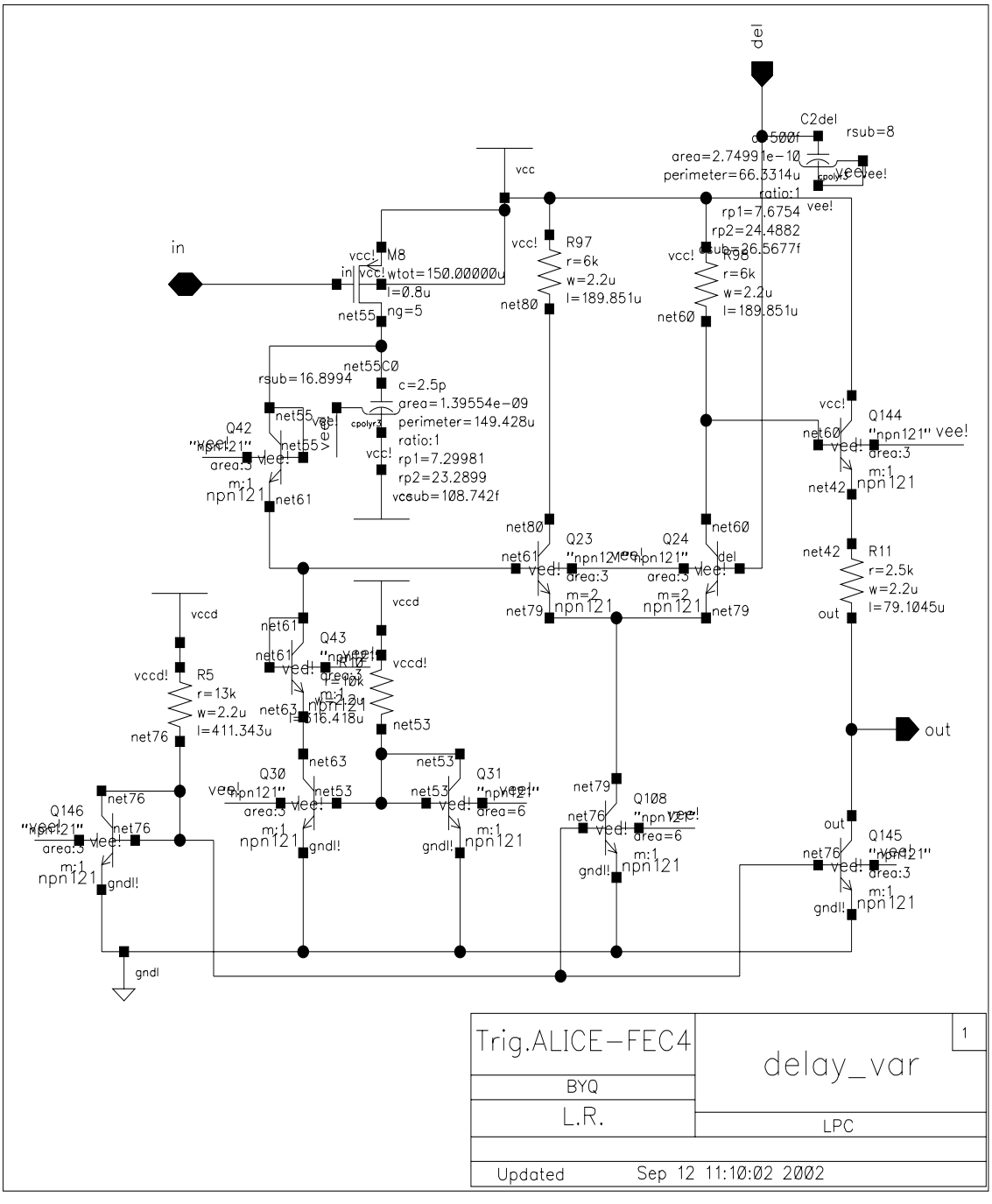


Figure 58: Electronic scheme of the variable delay ("delay_var" block).

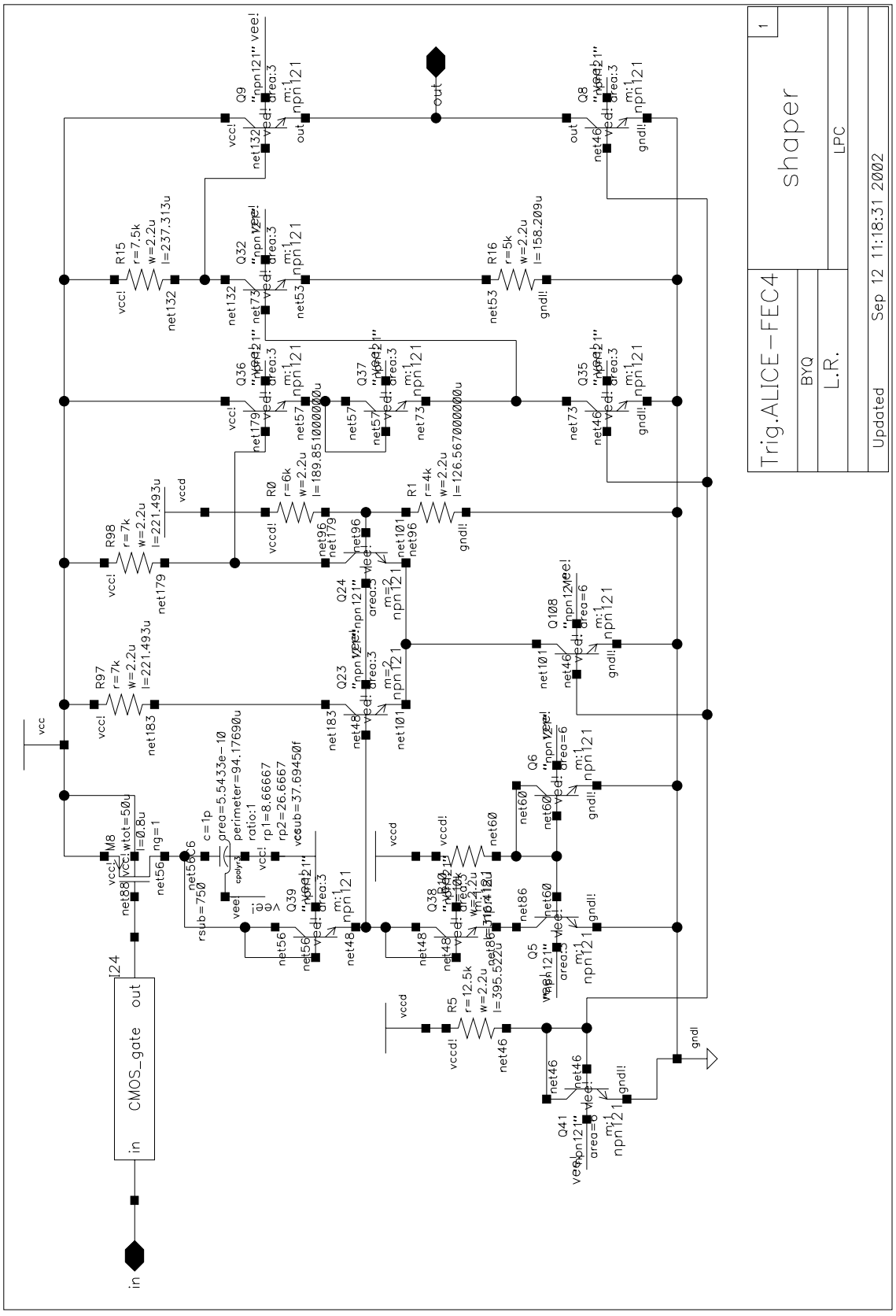


Figure 59: Electronics scheme of the "shaper" block.

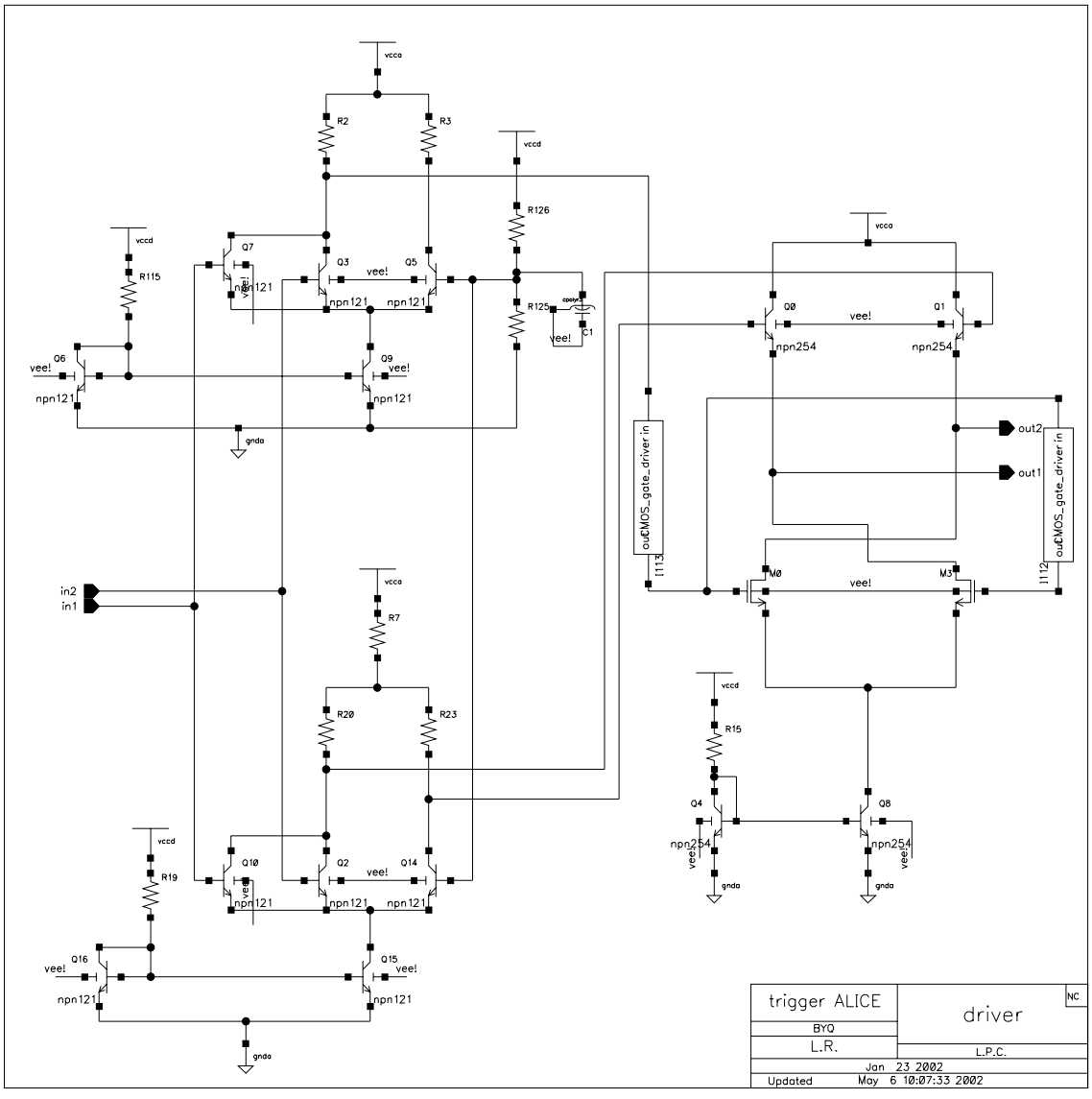


Figure 60: Electronics scheme of the "driver" block.

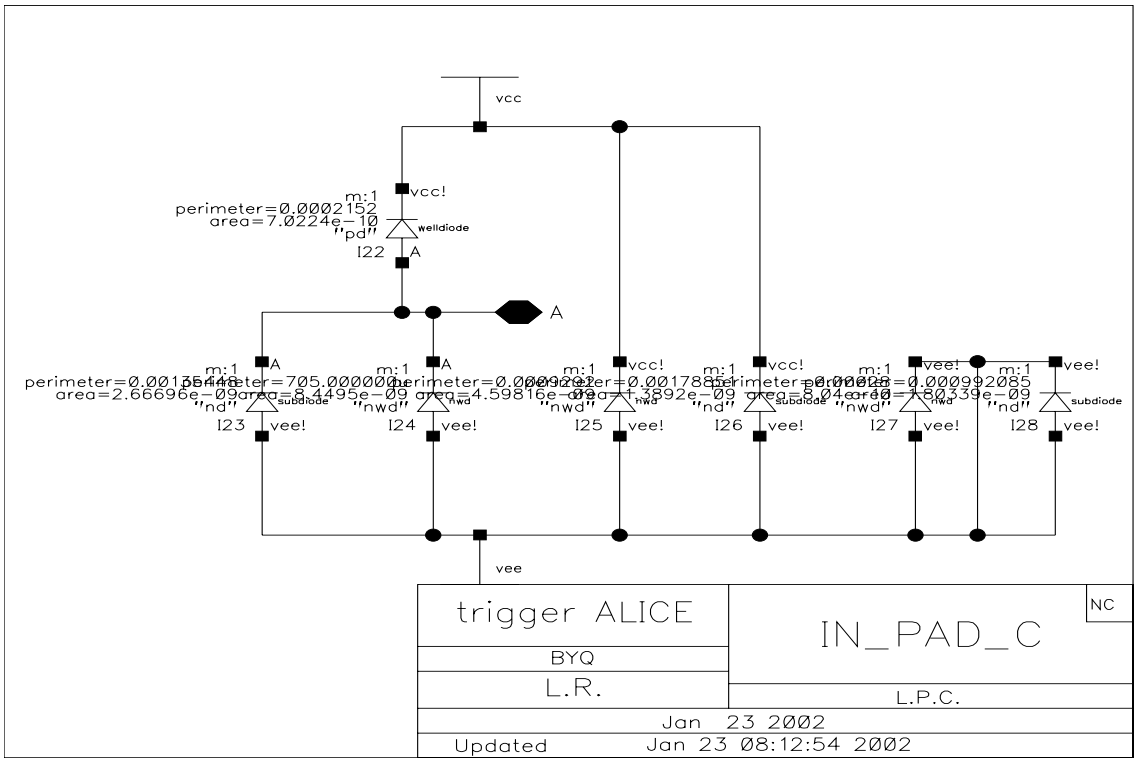


Figure 61: Electronics scheme of one standard Pcells PADs.

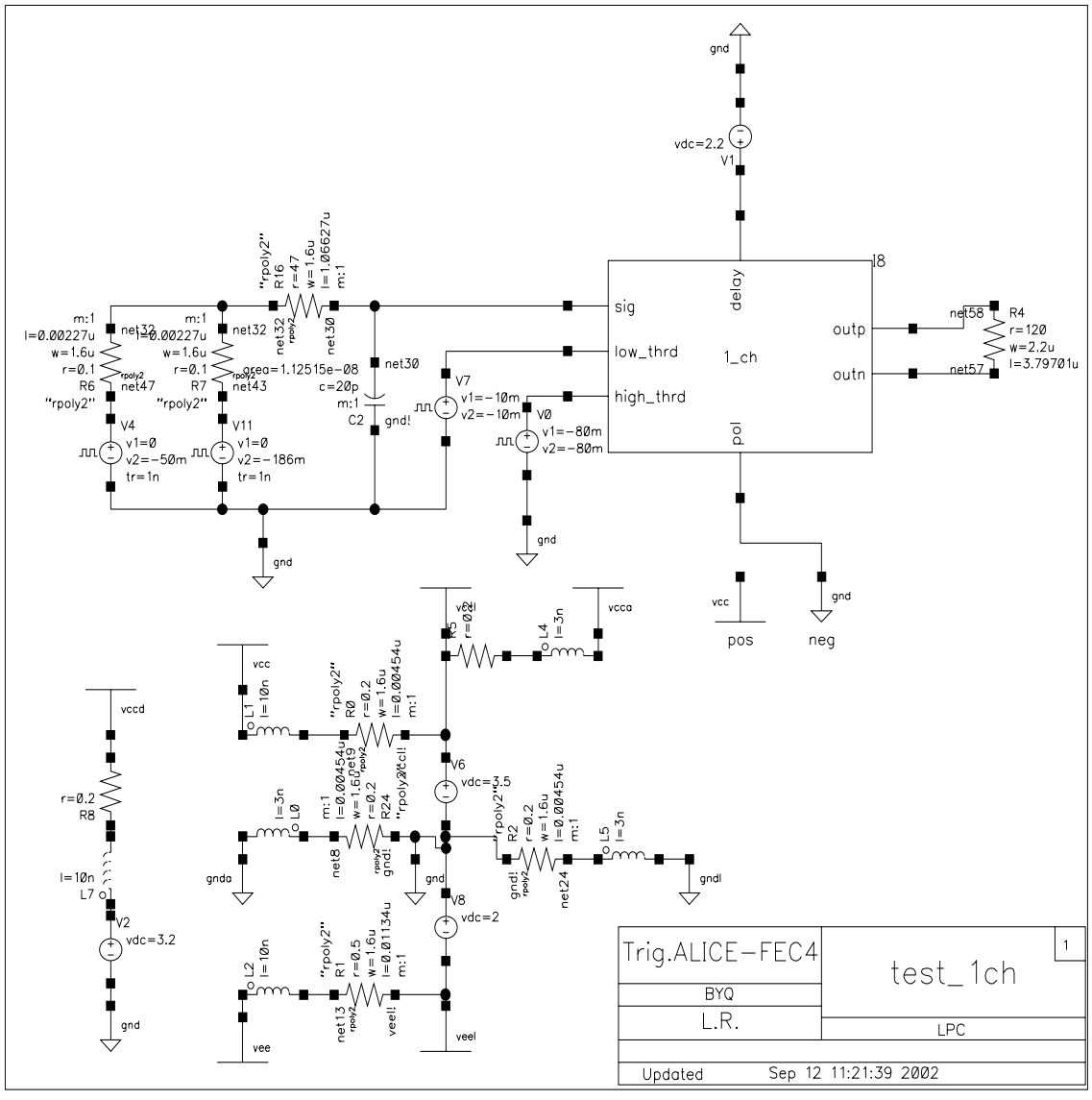


Figure 62: Schematic used to simulate one single analog_extrated channel.

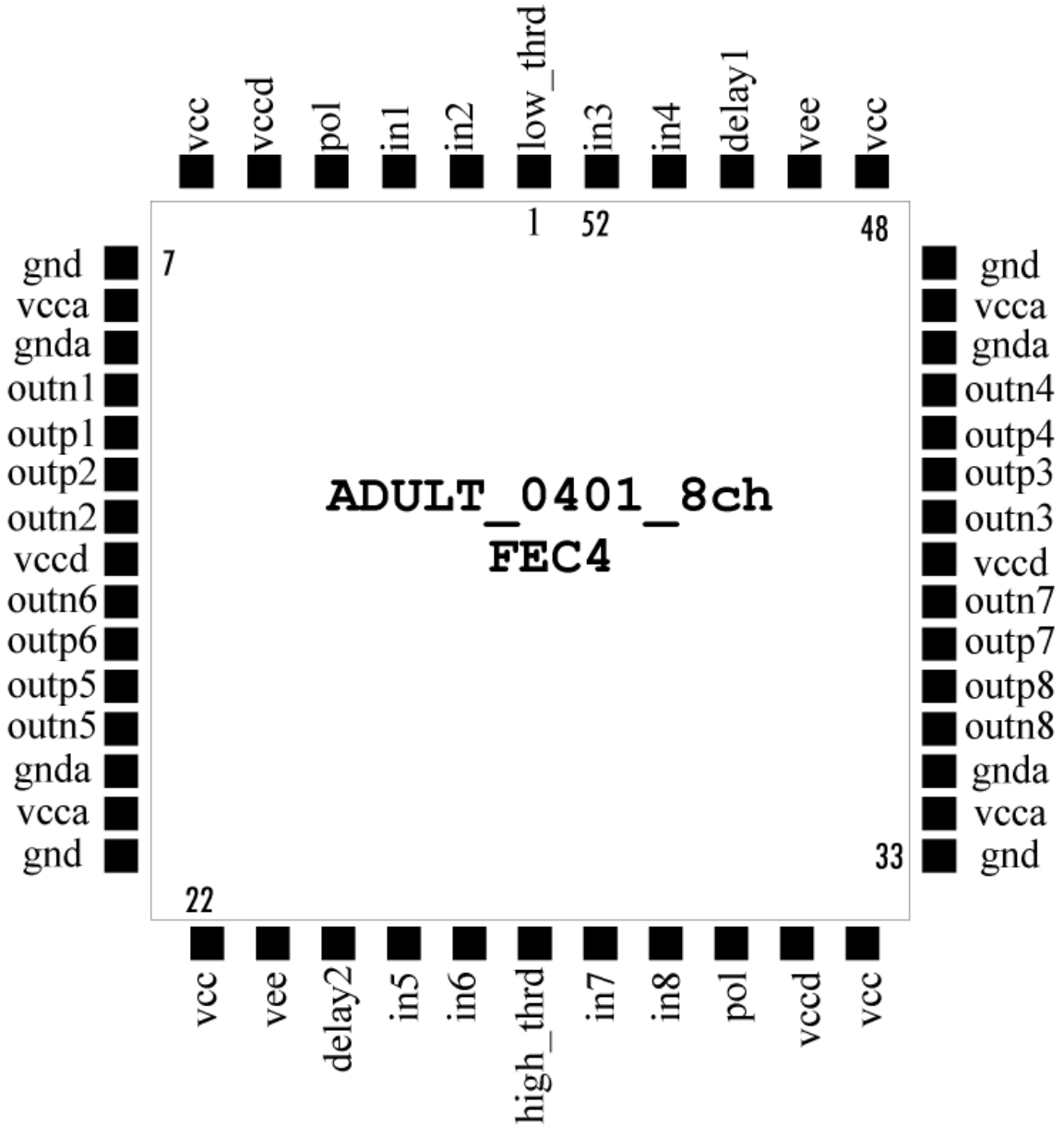


Figure 63: Pin-out of the ASIC.

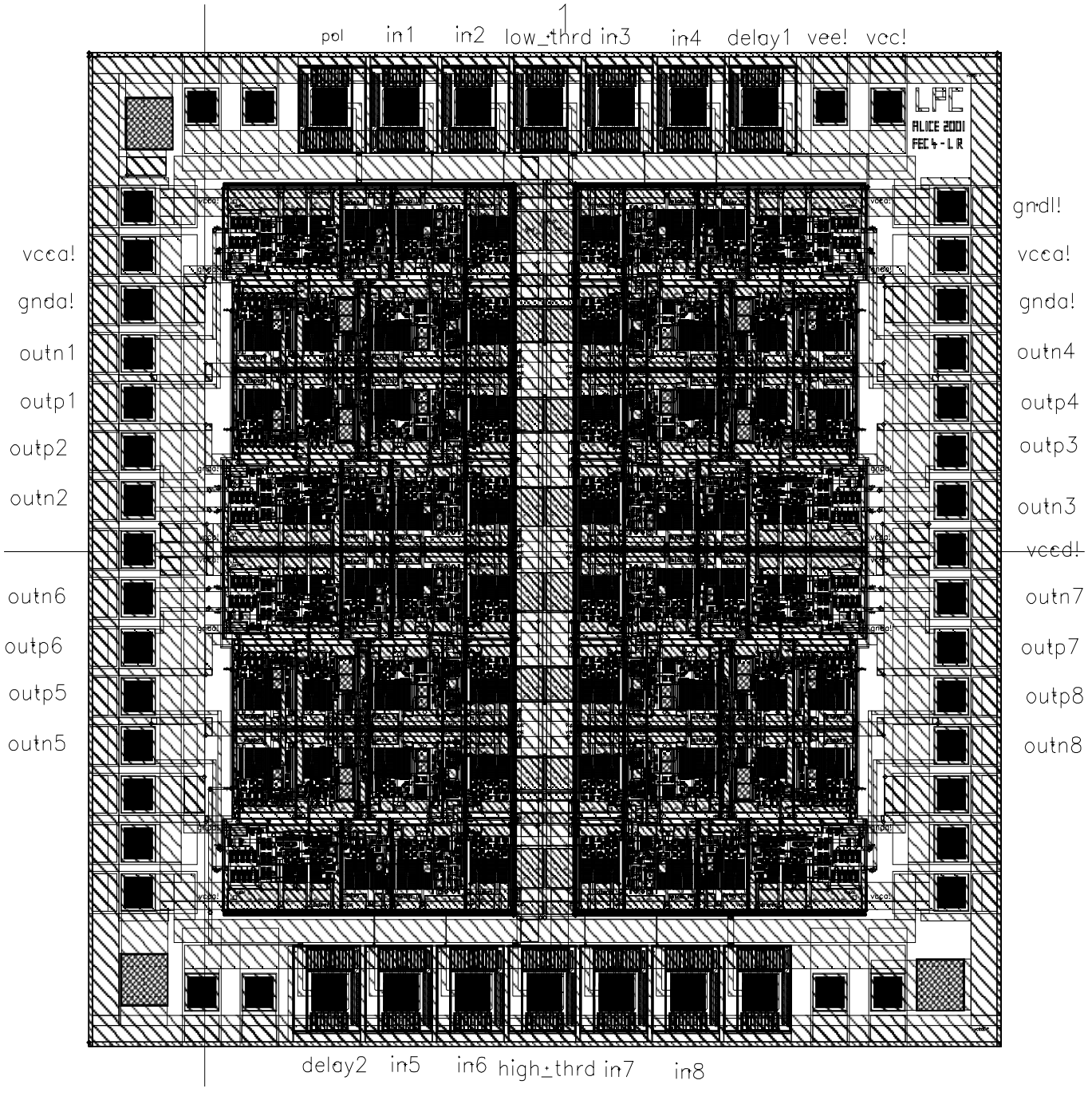


Figure 64: Global layout picture of the chip.

C Front-end boards electronics schemes for FEB11X

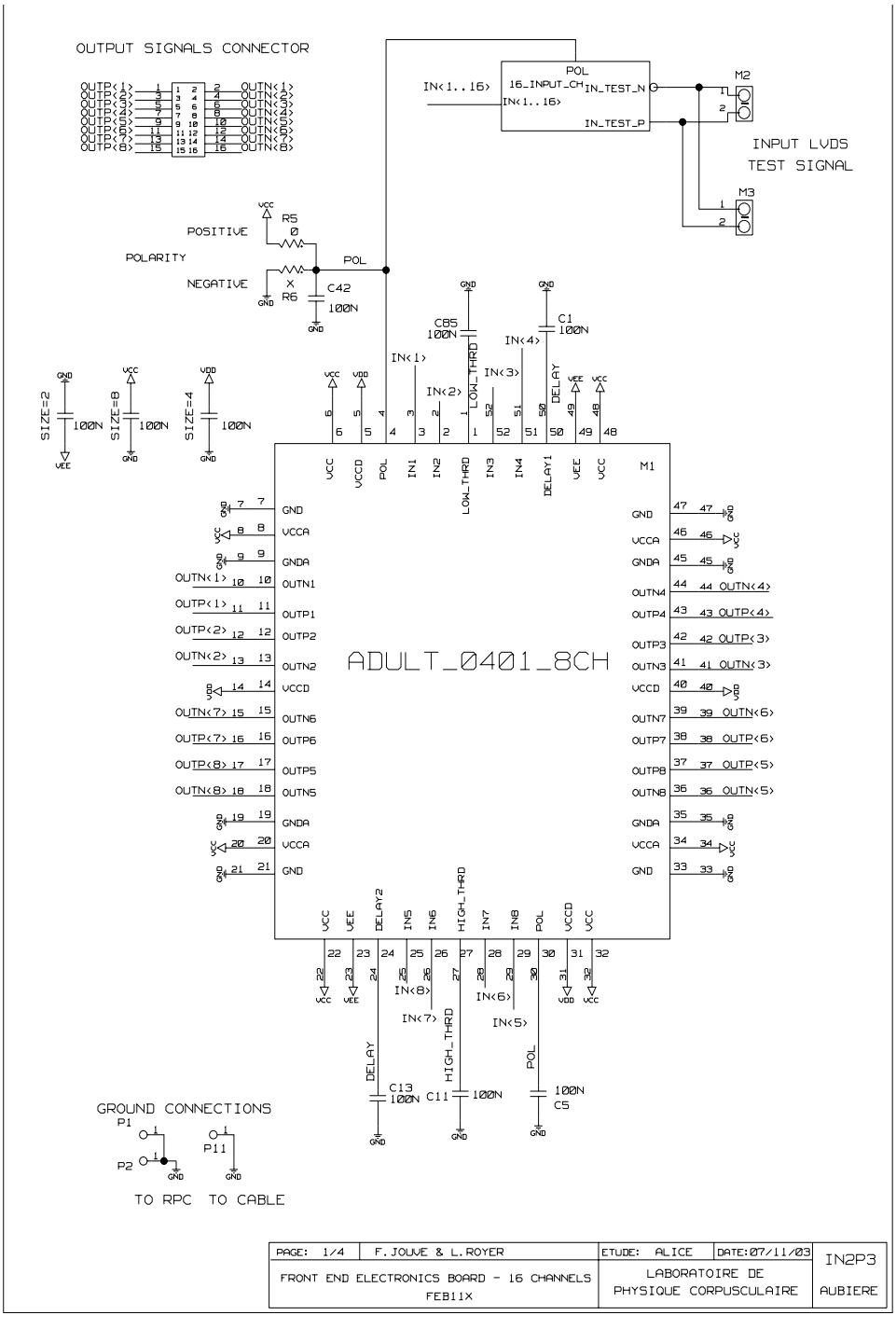


Figure 65: FEB11X schematic view: ASIC 1 implementation.

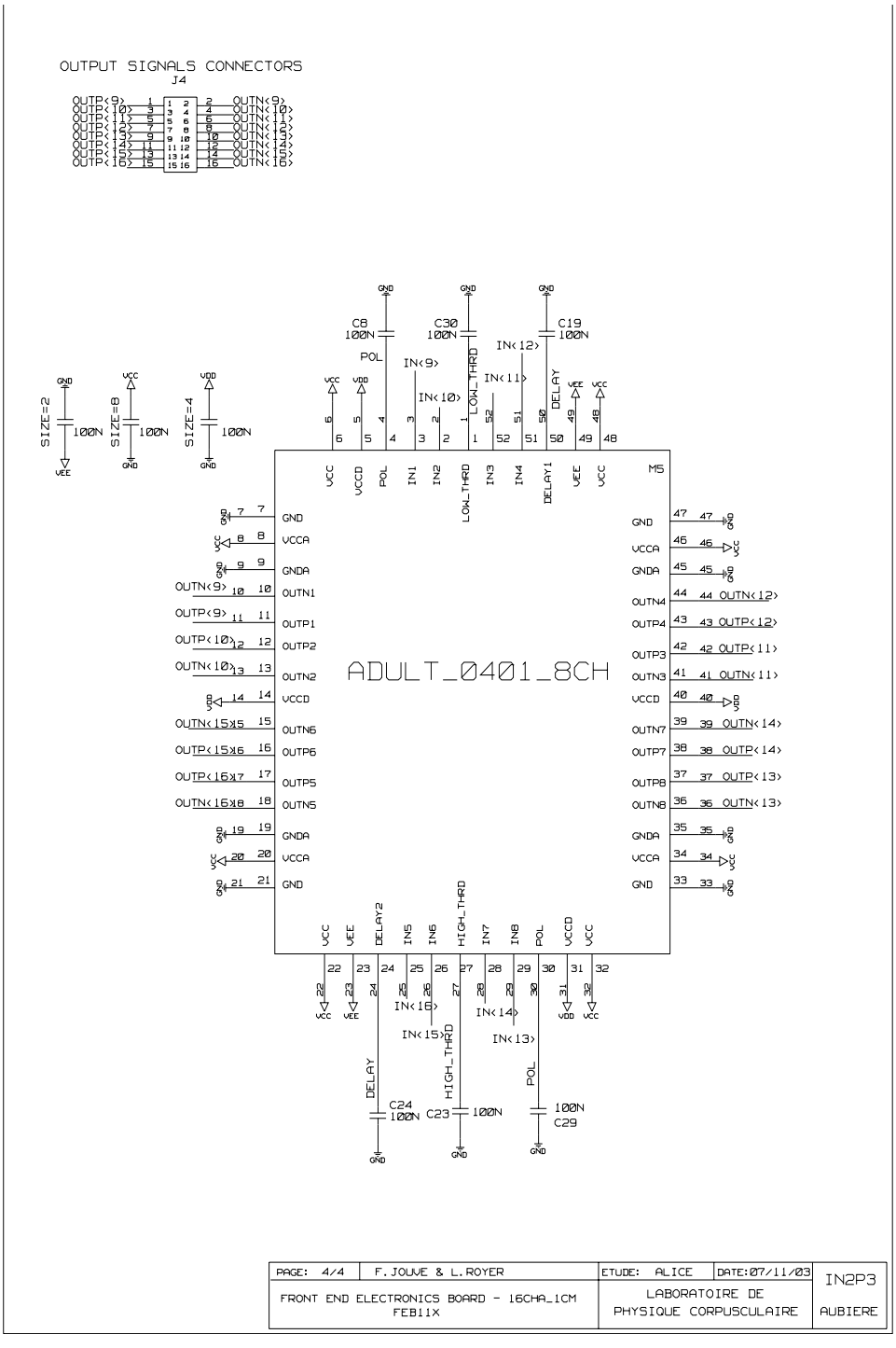


Figure 66: FEB11X schematic view: ASIC 2 implementation.

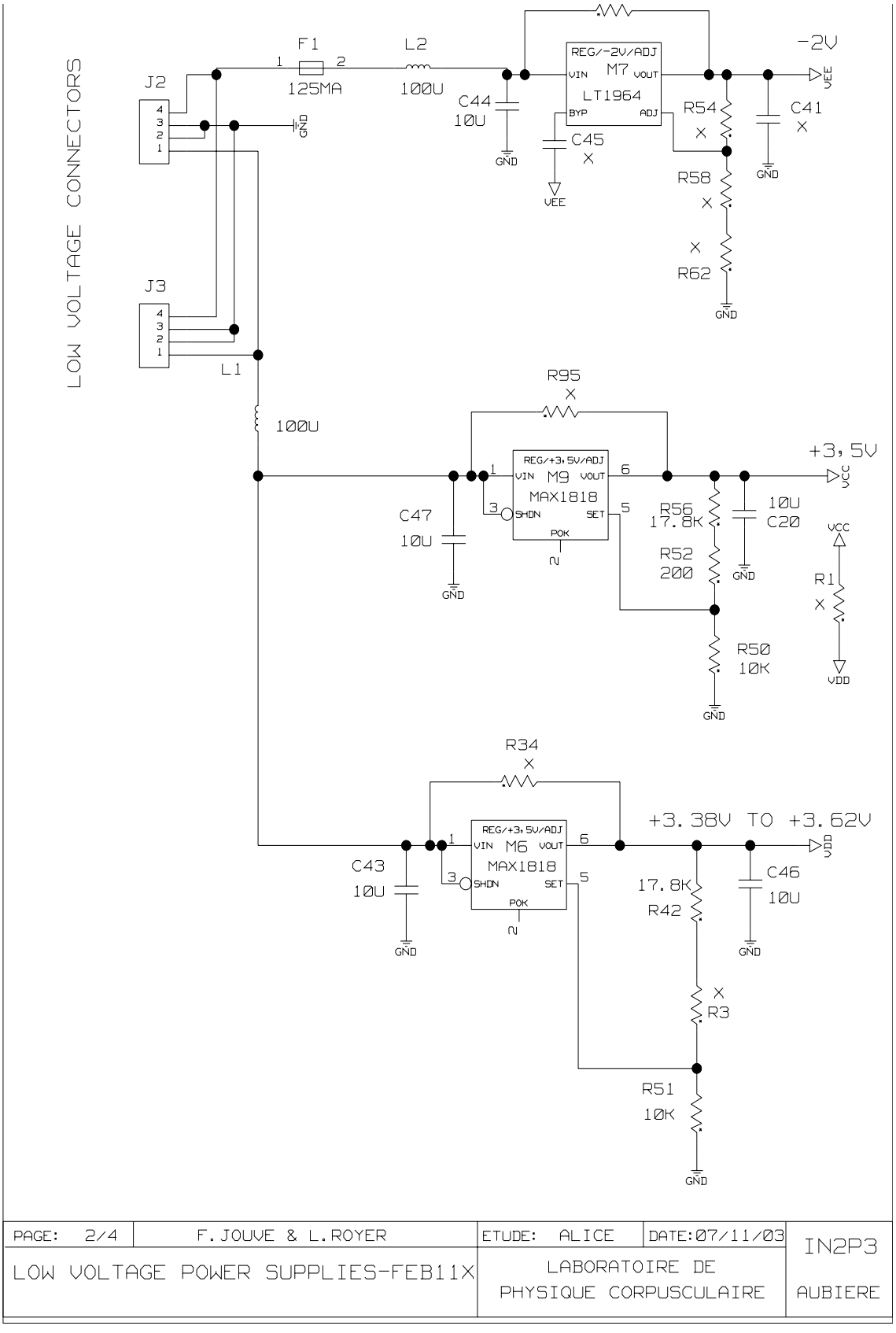


Figure 67: FEB11X schematic view: low voltage power supplies.

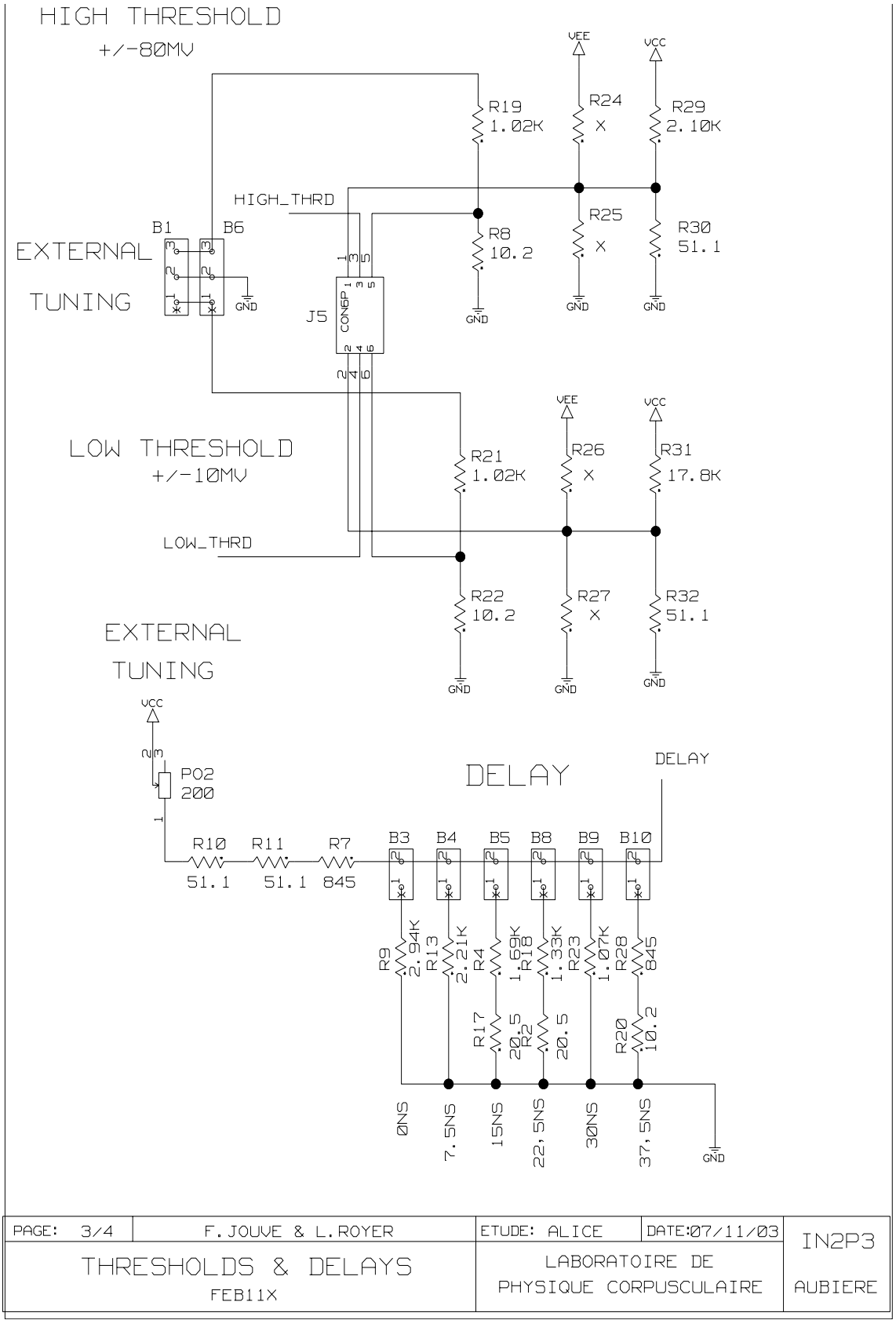


Figure 68: FEB11X schematic view: threshold and delay configuration.

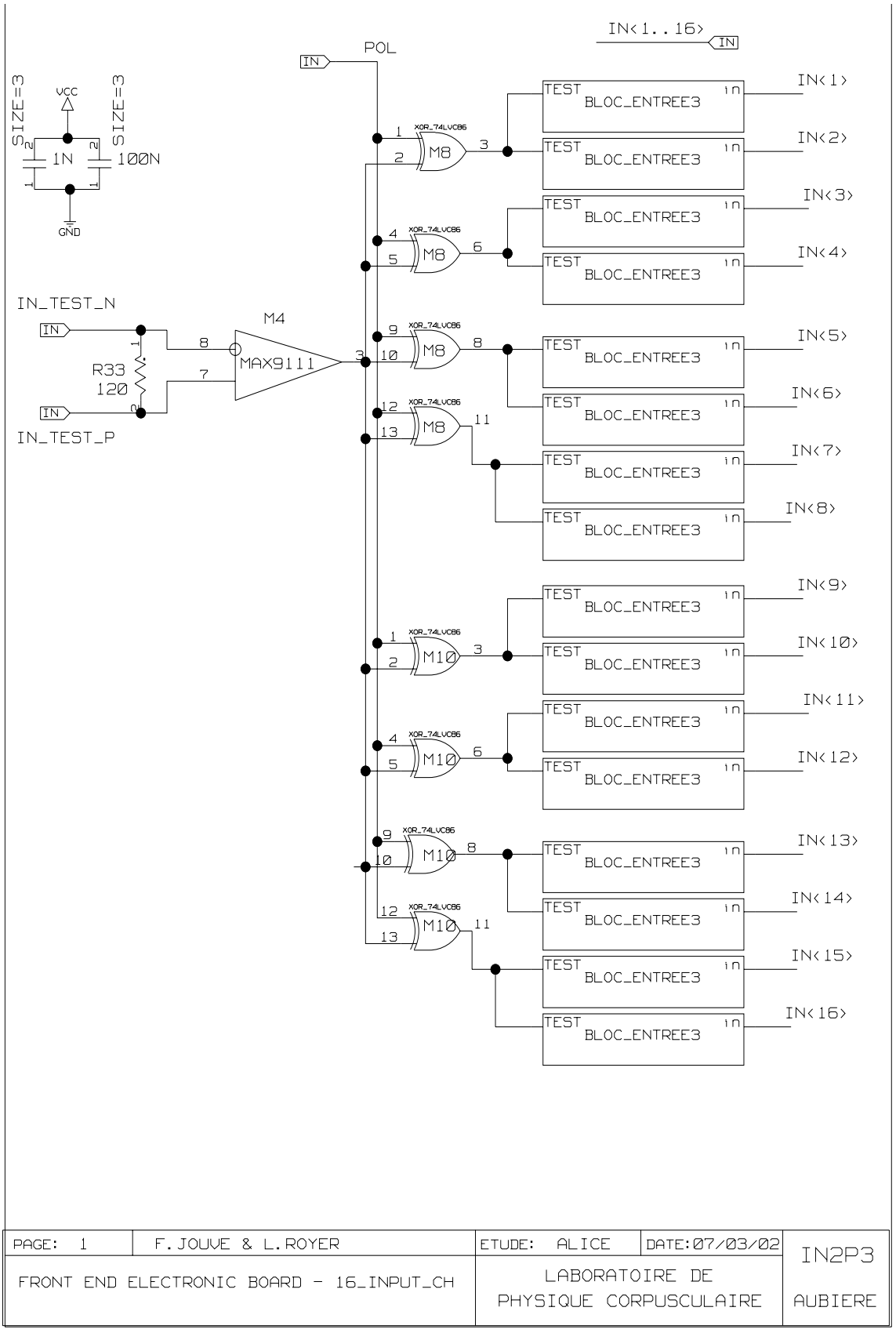


Figure 69: FEB11X schematic view: LVDS test signal input.

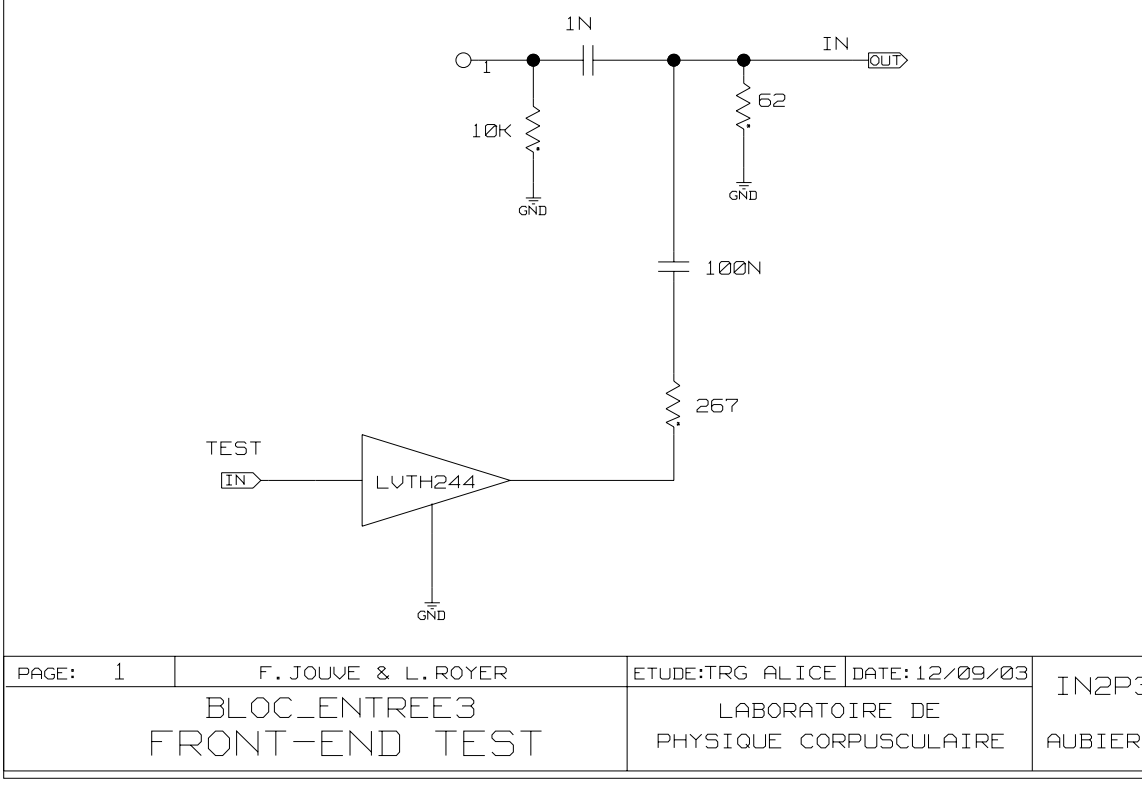


Figure 70: FEB11X schematic view: one channel test system.

D Electronics components for FEB11X

ADULT_0401_8CH_PLCC	M1,M5	2		AMS/CMP
BORNIER2B-1CAVALIER	B3-B5,B8-B10	6	?	?
CON6P-SUPP 3CAVALIERS	J5	1		
FUSIBLE-125mA	F1	1	Nanofuse R451.125	Littlefuse
INDUCTANCE -100U FERRITE	L1,L2	2	SCEM 08.11.76.400.2	CERN
CON16P-VROUD	J1,J4	2	3408-6202	3M
CON3P-BARCONC3	B1,B6	2	78208-103	Berg
CON4P-SL508C4/45	J2,J3	2	160555	Weidmuller
MPT2540-DIP_254	M2,M3	2	2227.2021	Molex
Female pin BURNDY	P1-P10,P12-P19	18	RC16M23K	Burndy
COSSE POIGNARD	P11	1		
CAPA-10U,CS10V10%	C20,C43,C44,C46,C47	5	CMS1206	NCC
CAPA-100N,C805S25V20%	C1-C19,C22-C24,	59	CMS 0805	?
	C27-C40,C42,C48-C53			
	C55,C57,C59,C61,C63,			
	C65,C67,C69,C71,C73,			
	C75,C77,C79,C81,C83,			
	C85			
CAPA-1N,C805S25V10%	C21,C25,C26,C54,C56,	19	CMS 0805	?
	C58,C60,C62,C64,C66,			
	C68,C70,C72,C74,C76,			
	C78,C80,C82,C84			
LVTH244_SOIC-SOZ_1270BIS	M11,M12	2	FSC74LVTH244SJ	Fairchild Semic.
MAX9111-SOT23_0650	M4	1	MAX9111EKA	Maxim
XOR-74LV86	M8,M10	2	SN74LVC86AD	Texas Semic.
MAX1818	M6,M9	2	MAX1818EUT50	Maxim
POT-200,1/4W11T	PO2	1	3224W101	Bourns
RGEN-0, S23X15_0805	R5, R38	2	CMS 0805	?
RGEN-1.07K, S125MW1%	R23	1	CMS 0805	?
RGEN-1.33K, S125MW1%	R18	1	CMS 0805	?
RGEN-1.69K, S125MW1%	R4	1	CMS 0805	?
RGEN-10.2, S125MW1%	R8,R20,R22	3	CMS 0805	?
RGEN-10K, S125MW5%	R35,R39,R43,R47,R50,	18	CMS 0805	?
	R51,R53,R61,R65,R68,			
	R71,R74,R77,R80,R83,			
	R86,R89,R92			
RGEN-120, S125MW5%	R33	1	CMS 0805	?
RGEN-17.8K, S125MW1%	R31,R42,R52	3	CMS 0805	?
RGEN-1.02K, S125MW1%	R19,R21	2	CMS 0805	?
RGEN-2.10K, S125MW1%	R29	1	CMS 0805	?
RGEN-2.21K, S125MW1%	R13	1	CMS 0805	?
RGEN-2.94K, S125MW1%	R9	1	CMS 0805	?
RGEN-20.5, S125MW1%	R2,R17	2	CMS 0805	?
RGEN-200, S125MW1%	R56	1	CMS 0805	?
RGEN-267, S125MW1%	R36,R40,R44,R48,R57,	16	CMS 0805	?
	R63,R66,R69,R72,R75,			
	R78,R81,R84,R87,R90			
	R93			
RGEN-51.1, S125MW1%	R10,R11,R30,R32	4	CMS 0805	?
RGEN-62, S125MW5%	R37,R41,R45,R49,R60,	16	CMS 0805	?
	R64,R67,R70,R73,R76,			
	R79,R82,R85,R88,R91			
	R94			
RGEN-845, S125MW1%	R7,R28	2	CMS 0805	?
NOT USED	R1,R3,R6,R24-R27	15		
	R34,R54,R58,R62,R95			
	C41,C45			
	M7			
TOTAL		221		

E Production Readiness Review recommendations

The Production Readiness Review (PRR) for this electronics was held the 28 of November 2002, and the report written by the referees dates from the 30 January of 2003.

Except the three autors of this note, the present persons were: A. Baldit, C. Fabjan, Y. Le Bornec, F. Staley, G. Stefanini, H. Taureg and A. Tournaire.

The referees were: E. Delagnes (expert in micro-electronics) , C. de la Taille (expert in micro-electronics) and P. Edelbruck (expert in electronics).

The summary of the recommendations (reported here in italic) and the replies (reported in normal characters) was:

- *Radiation tests: The referees insist that one tests for all components their sensitivity to radiation. The radiation level for ALICE are lower than for CMS or ATLAS and the main problem will be SEU and latch-up. One should as well stay in contact with the other experiments to profit from their test. F. Faccio can give advice on the tests.*

  As described in section 6.5, the electronics has been tested under radiations up to 15 LHC years compare to the expected rate in ALICE. For the SEE, the test with energetic protons correspond to more than 1000 LHC years of working.

- *Time dispersion: The referees asked about the way one can detect channels, which fall outside the specified time windows and what margin of adjustment exists. Cables should be tested for their time dispersion after installation.*

  The timing of the front-end boards will be adjusted with a specific test bench after production. Boards with one or more channels outside the required time window will be rejected. The results obtained with the pre-serie, see section 6.4, show a time window less than 4 ns, as required. Concerning the cable, a dedicated test bench is under design at LPC Clermont-Fd. The time response of each pair (16 pairs per output cable) will be measured, and the cable with a time dispersion outside the required window (3 ns) will be rejected. It will not be possible to test the time dispersion of the cables after installation in the cavern. However, with the help of the local trigger electronics, it will be possible to detect the channels outside the time window of about 22 ns.

- *Chips: The referees suggests asking for a single batch production. They asked about the lifetime of the process. The envisaged quantity of spares seems adequate. Should one use sockets for ASIC? Should one go to a ceramic housing?*

  A single batch for the ASICs production is in principle not a problem. Due to the risk of contact oxydization, the socket has been replaced by a direct welding on the board. The results of the pre-serie production (50 ceramic and 69 plastic packagings) show no performances difference between ceramic and plastic packagings, then the plastic solution has been retained.

- *Protection: One should test the limits of the input protection of the ASIC.*

A good working of the ASIC is observed with input pulse up to 5 V. The input is destroyed when a DC low voltage greather than 5.2 V is applied in input. When the output is connected to the ground, the ASIC is not destroyed; and a good working is observed after recovery.

- *Grounding: The grounding scheme should be completed and documented.*

  The scheme principle was elaborated in consultation with F. Szoncso, from the CERN Technical Inspection and Safety (TIS) division, and tests of electromagnetic compatibility performed by him during RPC1 experiment at GIF (see section6.4) indicate that the grounding is efficient.

- *Contact to chamber body: The referees expressed their worries about a long-lasting, good contact to the aluminium of the chamber body. Should one increase the number of ground pins?*

  In the final design of strip readout planes, the pround plane and strips are now in copper (instead of aluminium during R&D period).

- *FEE cards variety: The referees insisted on elaborating a system for managing the spare cards; identifying, marking and bookkeeping of the different FEE cards. What are the means to check and the time needed to modify the cards? The amount of spares (*10 %*) seems reasonable.*

  During the test bench step of the production, each front-end board will be tagged with an optical code bar to identify the station, the polarity, the delay (corresponding to a cable length), the pitch and a serial number. Furthermore, for each board, besides the general parameters such as currents consumption, the parameters characterizing each channel will be stored in a database.

- *FEE cards: The referees asked if a 'burn-in' is planned. This seems only feasible by operating the trigger chamber system in situ. One should monitor the temperature of the FEEcards. There are plans in this direction.*

  The burn-in will be done after installation during the commissioning stage. The monitoring of the temperature is under the responsibility of the Torino group which builts the chambers.

- *Power supplies: One should check the behavior as function of the number of channels firing.*

  For one RPC equipped with 40 ASICs, the consumption start to increase when the frequency of the test signal is greather than 1 MHz (see section 6.4), a frequency which is much higher than the expected rate in ALICE.

- *Test input: The referees suggested to consider segmentation of the test pulse distribution and a capacitor at the test input.*

  The segmentation of the test pulse distribution has been increased to 15 zones (instead of 10) on each RPC, with a maximum of 4 FEBs per zone in order to reduce time dispersion. The capacitor of the input test signal has been changed from 100 nF to 1 nF, to avoid a too long discharge of the input signal.

The general conclusion of the Production Readiness Review was:

The referees acknowledged the thorough work done and the detailed documentation for the review. They suggested checking and following up on a number of points, which are given above, and updating the documentation with the results from pre-serie tests. They regarded the system well enough understood and tested to proceed to the production phase.

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Glossary

- ADULT: A DUaL Threshold.
- ALICE: A Large Ion Collider Experiment.
- AMS: Austri MicroSystems.
- ASIC: Application Specific Integrated Circuit.
- DC: Direct Current.
- DCS: Detector Control System.
- ESD: ElectroStatic Discharge.
- FEB: Front-End Board including
  - FEB10 for a strip pitch of about 1 cm,
  - FEB20 for a strip pitch of about 2 cm,
  - FEB40 for a strip pitch of about 4 cm.
- FEC: Front-End Chip (dedicated ASIC).
- FEE: Front-End Electronics (including FEB, FEC, FET).
- FET: Front-End Test system.
- HV: High Voltage.
- HVPS: High Voltage Power Supply.
- L0: Level 0 trigger.
- L1: Level 1 trigger.
- LHC: Large Hadron Collider.
- LHCC: Large Hadron Collider Committee.
- LPC: Laboratoire de Physique Corpusculaire.
- LV: Low Voltage.
- LVDS: Low Voltage Differential Signal.
- LVPS: Low Voltage Power Supply.
- MT1: Muon Trigger station number 1 (located at 16 m from the interaction point).
- MT2: Muon Trigger station number 2 (located at 17 m from the interaction point).
- PPR: Production Readiness Review.
- QCD: Quantum Chromo-Dynamic.
- QGP: Quark-Gluon Plasma.
- RPC: Resistive Plate Chamber.