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# ASIC para Estimulação Elétrica da Espinal Medula

# An ASIC for Electrical Stimulation of adECM/GBM Scaffolds

Universidade de Aveiro
2021

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Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia de Eletrónica e Telecomunicações, realizada sob a orientação científica do Doutor (Luis Filipe Mesquita Nero Moreira Alves), Professor Auxiliar do Departamento de Eletrónica, Telecomunicações e Informática da Universidade de Aveiro, e do Doutor (José Luís Vieira Cura), Professor Auxiliar do Departamento de Eletrónica, Telecomunicações e Informática da Universidade de Aveiro.

Dedico este trabalho aos meus pais, Arménio e Leonor, e ao meu irmão, Arménio.

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**agradecimentos / acknowledgements**

Agradeço, em primeiro lugar, ao meu orientador, Prof. Luis Nero Alves, por me ter dado a oportunidade de participar num projeto tão multidisciplinar, pelo apoio dado durante a implementação e conceção do trabalho apresentado nesta dissertação e pela revisão e crítica da mesma. Agradeço, ao meu co-orientador, Prof. José Luís Cura, por apoiar toda a fase de implementação da dissertação, por todos os momentos de esclarecimento de dúvidas e pela revisão da mesma.

Agradeço aos meus pais e ao meu irmão por todo o apoio e por me providenciarem, ao longo destes anos, com tudo o que precisei facilitando todo o meu percurso.

A todos os meus amigos, um obrigado, por todas as aventuras, companheirismo, momentos de convívio e longas jornadas épicas que me proporcionaram.

Agradeço ainda a todos do laboratório de circuitos e sistemas integrados do Instituto de Telecomunicações, pelo companheirismo ao longo da dissertação e por terem tornado esta jornada mais animada.

Por fim, agradeço ao Instituto de Telecomunicações e à Universidade de Aveiro por me terem disponibilizado com o necessário para o desenvolvimento da dissertação.

**Palavras Chave**

circuitos integrados, CMOS, dispositivo implantável, estimulação elétrica, medula espinal, neurorregeneração

**Resumo**

Lesões na Medula Espinhal são causadas sobretudo devido acidentes rodoviários, quedas e lesões na prática de desportos. Estas têm graves consequências no estado de saúde dos pacientes, uma vez que saõ responsáveis por diagnósticos como tetraplegia e paraplegia. Até hoje, terapias eficazes para este tipo de lesões ainda não foram conseguidas, o que torna esta temática num foco de estudo. Atualmente, uma das orientações deste foco de estudo está direcionado em dispositivos elétricos implantáveis capazes de estimular a espinal medula in-vivo, promovendo a regeneração da mesma. Adicionalmente, o uso de materiais (scaffolds) que permitem manter o alinhemento no crescimento das fibras, em conjunto com estimulação elétrica é vista como a solução consensual para terapias relacionadas com Lesões na Medula Espinhal. Assim, o projeto NeuroStimSpinal, na qual este trabalho se insere, foi proposto. Este tem como objetivo propor uma terapia para esta problemática usando estimulação elétrica em conjunto com scaffolds impressas em 3D. O trabalho apresentado nesta dissertação é baseado num circuito integrado de aplicação específica (CIAE) para estimulação em corrente da espinal medula, com o intuito de promover a regeneração da mesma. Os desafios na implementação deste tipo de circuitos estão relacionados com a necessidade destes terem de ser pequenos em tamanho e consumir uma potência reduzida, mantendo as características necessárias para a estimulação, uma vez que é necessário que o mesmo faça parte de um dispositivo implantável. O circuito de estimulação proposto consiste: numa interface de comunicação com a unidade de controlo (microcontrolador) usando o protocolo Serial Peripheral Communication (SPI); um conversor digital para analógico de 10 bits, o qual se baseia numa arquitetura de escalonamento binário por carga; um conversor tensão para corrente rail-to-rail e uma ponte H que direciona a corrente pela scaffold, cuja implementação se baseia no uso de portas de transmissão como comutadores. Resultados ao trabalho desenvolvido mostram que o circuito é capaz de estimular a scaffold com correntes entre 0 to 200$\mu$A com um erro na corrente de estimulação inferior a 0.75$\mu$A. O circuito é capaz ainda de fornecer uma corrente linear, na gama mencionada, a cargas com impedancias até 15k$\Omega$. Para cargas superiores o circuito é capaz de fornecer uma corrente linear, embora em gamas de correntes menores. O circuito implementado usa como tensão de alimentação 5V, tem um consumo médio de potência de 19.5mW e ocupa uma área de 0.19$mm^2$. No decurso do trabalho desenvolvido foi utilizada uma tecnlogoia CMOS de 0.35$u$m. A implementação e resultados foram obtidos com recurso ao software Cadence.

**Keywords** ASIC, CMOS, electrical stimulation, implantable device, scaffold, SCI.

**Abstract**

Spinal Cord Injuries (SCI) have severe consequences such as tetraplegia and paraplegia, which dramatically affect the healthcare of the patients. Successful therapies for such injuries are yet to be attainable. Currently, there is a focus on the study and implementation of small implantable devices that are capable of providing in-vivo electrical stimulation to the spinal cord. Since the impedance of the neural tissue experiences constant changes, the focus is on using current stimulation instead of voltage, to compensate the impedance variations. Furthermore, the usage of scaffolds to provide alignment on the regrown fibers, combined with electrical stimulation is viewed as possible solution for SCI therapy. The NeuroStim-Spinal project, in which this work is inserted, aims to propose a SCI therapy based on in-vivo electrical stimulation combined with 3D printed scaffolds that have in its composition based materials (GBM) and adipose derived decellularized tissue (adECM). The work presented is an application-specific integrated circuit design (ASIC) that provides current-mode stimulation for neuronal regeneration, with the objective of providing in-vivo electrical stimulation for SCI therapy. The main challenges on the design of such devices is in obtaining low circuit area and power consumption, while maintaining the specifications needed. These characteristics are important, since it is intended to be an implantable device. The stimulation circuit consists of, a communication interface with a microcontroller using the Serial Peripheral Communication (SPI) protocol, a 10-bit DAC (Digital-to-Analog Converter) based on a binary charge scaling architecture, a voltage-to-current converter with a feed-forward voltage attenuator (FFVA) architecture, and a H-bridge circuit composed of CMOS switches to drive the scaffold. Results demonstrate that the system developed is capable of driving current from 0 to 200$\mu$A with an absolute error bellow 0.75$\mu$A. In addition, the developed circuit can provide these range of currents with high linearity to a 15k$\Omega$ load impedance. The system can still provide linear stimulation for higher load impedance's, but in smaller current ranges. Furthermore, the circuit uses a supply voltage of 5V and has an average power dissipation of 19.5mW. The ASIC was developed using a 0.35$\mu$m CMOS technology, has dimensions of 270$\mu$m per 700$\mu$m, which corresponds to a total area of 0.19$mm^2$. The work was developed using the Cadence software.

# Contents

# List of Figures

# List of Tables

# Glossary

| | |
|---|---|
| **adECM** | adipose derived decellularized tissue |
| **ADC** | Analog-to-Digital Converter |
| **AMS** | AustriaMicroSystems |
| **ASIC** | Application Specific Integrated Circuit |
| **BiCMOS** | Bipolar CMOS |
| **CS** | Chip Select |
| **CMOS** | Complementary Metal Oxide Semiconductor |
| **CMRR** | Common Mode Rejection Ratio |
| **DAC** | Digital-to-Analog Converter |
| **DC** | Direct Current |
| **DNL** | Differential Non-Linearities |
| **DRC** | Design Rule Check |
| **FBVA** | Feedback Voltage Attenuation |
| **FFCA** | Feedforward Current Attenuation |
| **FFVA** | Feedforward Voltage Attenuation |
| **GBM** | Graphene Based Materials |
| **IC** | Integrated Circuit |
| **ICMR** | Input Common Mode Range |
| **IMD** | Implantable Medical Devices |
| **INL** | Integral Non-Linearities |
| **ISCAS22** | IEEE International Symposium on Circuits and Systems 2022 |
| **LSB** | Least Significant Bit |
| **LVS** | Layout Versus Schematic |
| **MSB** | Most Significant Bit |
| **MISO** | Master Input Slave Output |
| **MOSI** | Master Output Slave Input |
| **MOSFET** | Metal Oxide Semiconductor Field Effect Transistor |
| **MUX** | Multiplexer |
| **NMOS** | N-Channel Metal Oxide Semiconductor |
| **NSS** | NeuroStimSpinal |
| **OTA** | Operational Transconductance Amplifier |
| **PMOS** | P-Channel Metal Oxide Semiconductor |
| **PWM** | Pulse Width Modulation |
| **QFN** | Quad-Flat No-leads |
| **SAR** | Successive Approximation Register |
| **SCI** | Spinal Cord Injuries |
| **SPI** | Serial Peripheral Communication |
| **SS** | Slave Select |
| **V-I** | Voltage-to-Current |

CHAPTER 1

# Introduction

## 1.1 Motivation

Spinal Cord Injuries (SCI) are catastrophic injuries on the nervous system that have severe consequences, being responsible for diagnostics such as tetraplegia and paraplegia. Therefore, SCI therapy is considered to be a global health priority [1]. Studies performed indicate that around 50% of the SCI cases occur in the age group of 16 to 30 years, mainly due to traffic accidents, acts of violence, falls and injuries in sports, which greatly affect the health and quality of life of the patients. Furthermore, health care expenses due to spinal cord injuries, are brutal and directly proportional to the injury severity [2].

A successful therapy to fully recover patients from spinal cord injuries remains to be achieved. The main challenge on SCI treatment is the fact that the spinal cord is constantly suffering changes, which interfere with the neuronal regeneration. Therefore, current therapies rely on preventing complications on the diagnostic and physical rehabilitation [3]. Scientific and technological advances in areas such as engineering and computer science opened the path for new approaches for SCI treatment. In particular, advances on Implantable Medical Devices (IMD) used for electrical stimulation of the spinal cord is currently being a research focus for SCI treatment. However, the design of this type of wireless implantable devices, for in-vivo electrical stimulation, poses many challenges. Since it is an wireless implantable device, it needs to be small in size and the battery's lifespan must be extended as much as possible. Therefore optimal power consumption and circuit area are requirements. In addition, biocompatibility and effective wireless communication interfaces must be assured. To tackle the biocompatibility issue, there have been research efforts on the area of neural tissue engineering. These are based on the usage of materials that act as scaffolds for the neuronal regeneration. These scaffolds are made to match the geometry of the spinal cord, providing a healthier mechanical support for neuronal regeneration [4]. Furthermore, 3D scaffolds can be used to provide alignment of the regrown fibers. Having this in mind, the usage of such scaffolds in combination with electrical stimulation is viewed as a possible for SCI treatment [3].

The work developed presents an Application Specific Integrated Circuit (ASIC) for in-vivo electrical stimulation applications, inserted in the NeuroStimSpinal (NSS) project. NSS aims to propose an effective therapy on SCI. The project proposes a scaffold for implantation on the region of injury, based on a combination of Graphene Based Materials (GBM) and adipose derived decellularized tissue (adECM) [5]. The scaffold together with an implantable electrical stimulation device aims to promote the growth and consequently, the reconnection of the ruptured nerves. This is the first time that a scaffold composition of this nature is being proposed for SCI therapy.

## 1.2 Objectives

The final goal of the presented work is the design of an ASIC able to support electrical stimulation of graphene scaffolds, for spinal cord injuries therapy, for in-vivo stimulation. To achieve this goal, the work entails:

- Understand the basics on neural stimulation, particularly electrical stimulation.
- Perform a study on current state-of-the-art on electrical stimulation systems for in-vivo stimulation.
- Propose an architecture that fit the system specifications. This entails the investigation on the most adequate circuits.
- Circuit design on Cadence software and simulation.
- Layout implementation and verification, followed by parasitic extraction and post layout simulation.

## 1.3 Methodologies

The work was developed in the Cadence integrated circuits design software. A first stage of implementation based on the simulation of the design circuits was performed in Spectre. After proving that the developed system complies with the specifications, the physical layout and verification was made in the Assura and Virtuoso design environments. Finally, parasitic extraction and post layout simulation was performed. The work was developed on the AustriaMicroSystems (AMS) 0.35$\mu$m, Complementary Metal Oxide Semiconductor (CMOS) technology.

In addition, MATLAB was used to process the simulation results, and to generate the plots included on the present document.

## 1.4 Document Organization

This dissertation is divided into seven chapters, including the present one.

- Chapter 2 starts by presenting the NeuroStimSpinal project. Then, basic concepts on electrical stimulation are presented, followed by an analysis on current state of the art stimulation circuits and devices. Finally, the general approach taken for the system developed in this dissertation is presented, as well as the system specifications.

- Chapter 3 is dedicated to present the most common architectures of the circuits needed in the system. A comparison between the different architectures is also made, in order to assess the ones that most fit the system requirements.
- Chapter 4 focuses on the system implementation. It starts by presenting a detailed architecture of the implemented system. Later, the circuits developed and details on the design are presented. This chapter also presents some preliminary simulations that helped on the circuit design and to prove the operation of the digital components. Finally, use cases of the system operation are also part of the chapter.
- In chapter 5, circuit simulation results, on Spectre, of the implemented circuits are presented. At the end of the chapter, full system operation simulations are also presented. This chapter aims to prove that the designed system complies with the specifications and is ready for the layout implementation.
- Chapter 6 is dedicated to present the implemented circuit layout and the main considerations and techniques used on the implementation. Post-extraction results and characterization of the layout of each implemented circuit component is also part of this chapter. In addition, chapter 6 also focuses on presenting the ASIC final results, after parasitic extraction. The operation of the system is demonstrated, the errors of the system are quantified and the obtained results are discussed.
- Chapter 7 aims to draw conclusions on the work developed. The implemented system and the key results are discussed. The chapter ends with possible future work directions.

CHAPTER 2

# NeuroStimSpinal

This chapter aim is to present the NeuroStimSpinal project, presenting its objectives and the project general methodology. Basic concepts on neural stimulation, in particular, electrical stimulation are also presented. Furthermore, a state of the art assessment of electrical stimulation systems for in-vivo applications is presented. Finally, the chapter ends with the presentation of the implemented ASIC general architecture, as well as, the specifications that need to be fulfilled.

## 2.1 NeuroStimSpinal: Description and Objectives

Spinal cord injuries refer to damages that happen specifically on the spinal cord or to nerves and tissue at the spinal canal's end. Spinal cord injuries may result in diagnostics, such as paraplegia and tetraplegia that are caused by the partial or complete disruption of descending motor and ascending sensory neurons [5]. This may potentially have severe consequences on the patients, since it can lead to sensory loss and paralysis. Having this in mind, NSS (logo in figure 2.1) project aims to develop an efficient treatment for spinal cord injuries.

In figure 2.2, a short schematic on the NSS project steps is presented. It follows three main steps: scaffolds preparation, in-vitro electrical stimulation tests and in-vivo electrical stimulation tests.


**Figure 2.1:** NSS Logo [5]

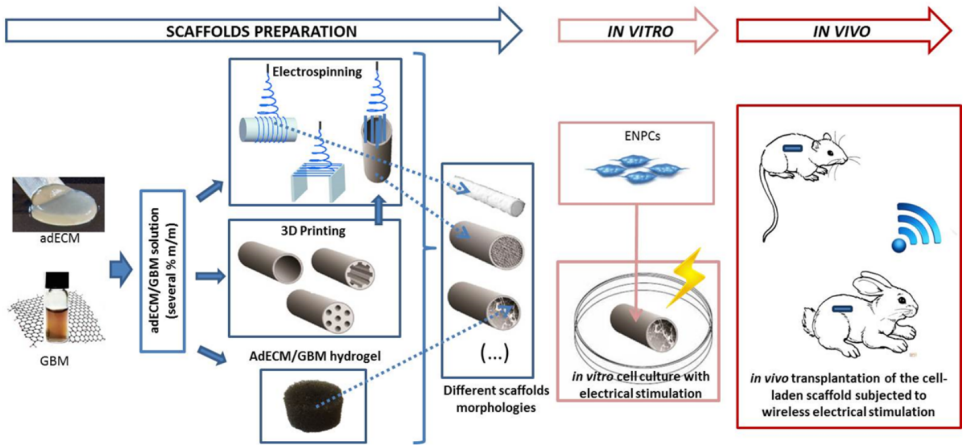


**Figure 2.2:** NeuroStimSpinal Project Overview [5]

The scaffolds are composed by a combination of GBM and adECM. The scaffold is intended to be implanted on the spinal cord, in the region of the injury, which together with electrical stimulation promotes the growth and consequently, reconnects the region that suffered partial or complete disruption. In this phase, several scaffolds of different shapes, sizes and compositions of adECM/GBM are developed, using 3D printing, in order to adapt to different spinal cord regions and to test the concentrations of adECM/GBM that provide the best results on the nerve regeneration [5].

The in-vitro stimulation tests are made in laboratory in a controlled environment. A custom off-the-shelve component stimulation system is developed and, electrical stimulation in the developed scaffolds on neural cells is performed. The objective is to assess the biocompatibility and bio-functionality of the scaffolds and to test the electrical stimulation performance.

The next step is to perform in-vivo stimulation. In-vivo refer to tests and experiments that are made in living organisms. The present work inserts in this part of the project, since it aims to develop the ASIC that is dedicated to perform the wireless electrical stimulation.

## 2.2 Neural Stimulation

Common methods for neural stimulation are: electrical, optical and chemical stimulation [6]. NeuroStimSpinal project focuses on a neural stimulation system based on electrical stimulation, therefore this topic is going to be the study focus of the present section.

### 2.2.1 Electrical Stimulation

In electrical stimulation, the main objective is to deliver a certain amount of charge to excitable cells, promoting an electric field on the tissue that potentiates ion movements on the cells. On the state of the art, there are three main techniques used for electrical stimulation: direct coupling, capacitive coupling and inductive coupling [7].

In direct coupling, the electrode is in direct contact with the cell culture or implanted on the animal. An electrical signal, being it a voltage, a current or charge is applied to a

pair of electrodes, which interacts directly with the cells. It is the simpler method to perform electrical stimulation. However, direct coupling raises issues associated with the electrodes materials biocompatibility and unwanted cells reactions [8].

In capacitive coupling, the stimulation is achieved through an electric field applied on the cells. Two metal electrodes are placed in parallel and an electric field is created between the plates. The cells are placed between the plates, being exposed to the electric field produced. An homogeneous electric field can be achieved using this method, therefore, the cells are stimulated with equal amount of charge independently of their position [8].

In inductive coupling, a magnetic field is used instead of an electric field. The magnetic fields are created with the use of coils, and the cells to be stimulated are placed in the center of the coils. An homogeneous magnetic field is produced across the cells, with the currents being generated from the magnetic field and stimulating the cells. In this method, no electrodes are required [8].

Both the inductive and capacitive coupling provide the advantage of being non-invasive, tackling the issues of the direct coupling stimulation method. However, for in-vivo stimulation these techniques do not prove to be an adequate solution, at the moment, due to high circuit area and high compliance voltages being required. Therefore, the stimulation method followed in the project is based on direct coupling [8].

### 2.2.2 Direct Coupling Stimulation

The stimulus applied with direct coupling can be generated in the form of voltage, current or charge.

Voltage stimulation circuits are based on potentiostats. A potentiostat is a device that is capable of applying a voltage potential to a certain load and, measure the generated current on the load [9]. This way, it is possible to prevent damages on the cells, by acting on the voltage that is being applied [9]. Voltage stimulation has a major drawback. It does not allow a precise control of the charge that is being stimulated. For this reason, it is usually preferred the charge and current stimulation architectures.

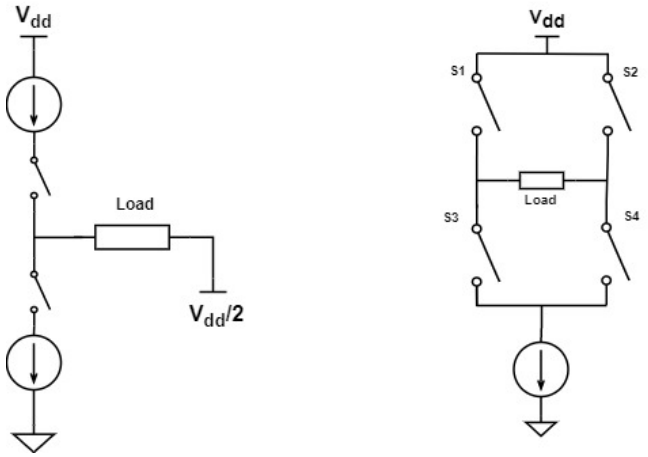


**Figure 2.3:** Curent/Charge Stimulation. At the left: half bridge circuit; at the right: h-bridge circuit

Current stimulation is achieved with the usage of programmable current sources that provide stable currents, and additional circuits to drive the cells. Furthermore, control on the current direction can be achieved using circuits such has the half bridge or the h-bridge architectures [10] (figure 2.3). However, current stimulation is limited by the supply voltage, which can be problematic for very high load impedance. Stimulation using charge control can be implemented using similar circuits. By controlling the time that the switches from the bridge circuit are active, the charge applied to the load is also controlled [10]. Current or charge stimulation are more desirable, since with these methods it is possible to apply a controlled stimulus, if the voltage drop at the load impedance ($R_L$) is lower than the supply voltage ($V_{DD}$), that is $R_{Load} \cdot I_{Load} < V_{DD}$. Furthermore, stimulus direction control can easily be achieved [10].

Important factors to take into consideration on the electrical stimulation topic is the stimulation polarity control capability, the stimulating frequencies and the current amplitude. For effective neuronal regeneration, studies report that the current amplitudes and frequencies are smaller than those used on pain relief spinal cord implants and deep brain stimulation [11]. Furthermore, bidirectional stimulation is important to provide effective regeneration of the descending motor and ascending sensory neurons.

Major constraints on the design of ASIC for in-vivo stimulation system are power consumption and circuit area. Since batteries' have limited lifespan, power efficient circuits are desirable, to maximize batteries life. In addition, with direct coupling, the stimulation circuit is in direct contact with the cells and, many times are implanted on the animal, therefore having a device small as possible is a requirement.

## 2.3 Electrical Stimulation Systems: State of the Art Review

The first studies and experiences on neurostimulation can be traced back to 1811, where Bell conducted experiments on spinal cord nerves. Several studies and discoveries followed on this topic. However, in the 20th century, with the development of powerful electronic circuits and systems the understanding on the nervous system operation and its interactions improved significantly [12]. Furthermore, with the development of these powerful electronic systems, new venues on neurostimulation have been explored, as the example of the electrical stimulation. Initially, electrical stimulation's aim was to increase SCI patients' mobility. However, with the further development on circuits and biomedical systems, electrical stimulation applications extended to applications such as heart pacemakers, cochlear implants and bladder control [2]. Today, numerous electrical stimulation systems are reported on the literature, in particular, stimulation systems using ASICs.

In 1997, a programmable current-source dedicated to implantable microstimulators was presented, in Bipolar CMOS (BiCMOS) 0.8$\mu$m technology [13]. It was based on a binary weighted current steering Digital-to-Analog Converter (DAC) that received a binary word and converted it into a proportional current. This current was amplified using current mirrors placed in parallel. Finally, the proposed solution presented an h-bridge architecture output stage to drive the nerve with bidirectional current. It provided 32 steps of stimulation (5 bits)

and up to 4mA of maximum current. In 1998, a similar stimulation system was presented for a visual microstimulator [14] in a 0.35$\mu$m technology. The main difference was on the DAC. This work proposed a current steering DAC based on thermometer decoders and similar current cells. This further increased the provided current accuracy. In 2004, an implantable electrical neural stimulation device for motor recovery for SCI patients, in a 0.8$\mu$m technology was presented [15]. The general architecture is based on a 8 thermometer decoded current steering DAC and an output stage based on a current mirror that drive the load with a maximum current of 20mA, with a resolution of 20$\mu$A. To provide higher voltage compliance, a DC-DC converter based on a charge pump architecture was developed. In the same year, a stimulation ASIC for cochlear implant was proposed, [16], using a 0.35$\mu$m technology. The general circuit architecture was similar to [15]. A thermometer decoded DAC was used to provide the necessary current and an h-bridge architecture was used to stimulate the load in both directions. A different approach was presented in 2005 [17]. The authors presented a stimulation circuit based on voltage-to-current conversion, where the current generated is controlled by switching the resistor responsible for conversion. A DAC converter with the output signal in voltage is used to maintain N-Channel Metal Oxide Semiconductor (NMOS) transistors in triode operation, region where the NMOS resistance changes linearly with the applied voltage applied. In 2012, two approaches for neural stimulation have been reported. An high voltage reconfigurable stimulator for SCI, with voltage stimulation was presented in [18]. In this approach, the amplitude of the pulses to be applied are sent to the ASIC using a binary word. Then selection logic, based on sample and hold circuits and decoders, is used to select the output channels from the 16 provided. This approach also provides control on the pulse width and frequency. Additionally, a charge pump to increase the voltage compliance is added. In [19], a wireless programmable neural stimulator is presented. The pulse frequency, amplitude and shape is controlled with a microcontroller that communicates with the implanted ASIC with an inductive link. The stimulation circuit itself is based on a voltage output DAC and a voltage-to-current converter that provides the stimulation current. To drive the load, an array of switches and additional logic is used. In 2015, an electrical stimulation ASIC in 0.18$\mu$m technology was presented by [20] for cochlear implants. It is based on a 7 bit current steering DAC composed by the combination of two subDACs. The currents from the subDACs are summed and provided to a modified half bridge architecture that stimulates the load. In 2017, [21] another architecture that provides bidirectional stimulation current was presented. Two 4 bits current steering DACs, with a R-2R architecture are used. At the output a half bridge circuit is used to drive the load, where one DAC acts as a current source and the other as a current sink, providing the bidirectional stimulation. To further increase the stimulation current accuracy, a DAC calibration circuit is introduced by the authors. Still in 2017, an ASIC capable of neural stimulation and recording was proposed [22] implemented in a 0.18$\mu$m technology. Focusing on the stimulation, it presents two DAC converters based on a current steering topology. One DAC acts as a current source and the other as a current sink. To control the current source and sink a half bridge output stage is used. Calibration on the DACs is included to increase the current accuracy and resolution. In

addition, a digital interface to control the operation flow and to communicate with an RF module that consequently communicates with the microcontroller is also part of the system. Finally, in 2020 a different approach for a implantable medical device was presented [23]. It uses a general voltage-to-current converter, however, instead of feeding at the output of the Operational Transconductance Amplifier (OTA) a voltage from an DAC, a reference voltage is used. The objective is to control current through the transistor at the output of the OTA. To provide a programmable output current, 8 replicas of this voltage-to-current converter are included, with switches to enable or disable each one. In addition, to provide bidirectional current to the load a half bridge architecture is used.

## 2.4 NeuroStimSpinal: In-Vivo System

After assessing the state of the art on the stimulation systems, the in-vivo system general block diagram is presented on figure 2.4. The microcontroller is responsible for the communications, data processing and control the current applied to the scaffold. The ASIC part is composed by a stimulation system and an acquisition system.

The acquisition system has the objective of acquiring the voltage at the terminals of the scaffold, convert this voltage into a binary word and send it to the microcontroller. This way, the scaffold impedance can be measured. Changes on the scaffold impedance can provide information on the cell growth due to stimulation, without the need of surgical intervention. The acquisition system is another work that was implemented in parallel with the stimulation system. Therefore, it is not in the scope of the presented work.

The stimulation system should provide electrical stimulation with direct coupling, with the stimulation being made with current. It is responsible for providing a stable current through the scaffold, with controlled amplitude and flow direction. The current amplitude is coded with a binary word and is sent to the ASIC, by the microcontroller, using Serial Peripheral Communication (SPI). In addition, the microcontroller has the capability of controlling the

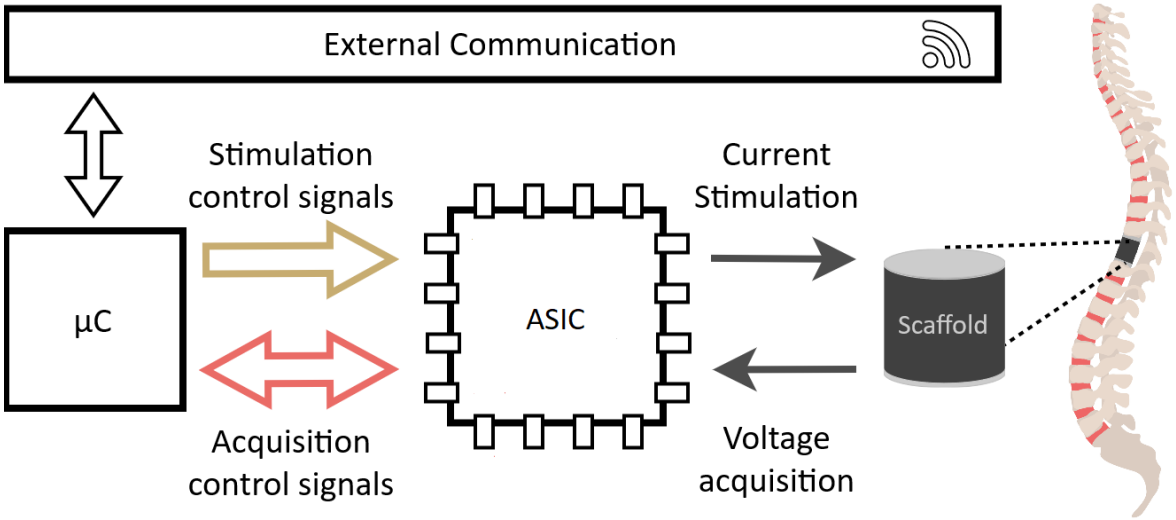


**Figure 2.4:** In-Vivo System Concept

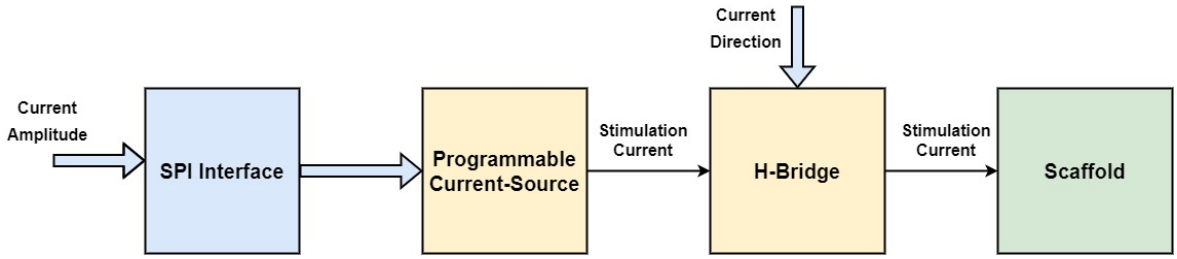


**Figure 2.5:** Stimulation System General Block Diagram

current direction and frequency by applying square signals to external pins from the ASIC. The stimulation system is responsible for converting the digital word presented at its input into a proportional current and drive it to the scaffold. The current amplitude should vary from 0 to 200$\mu$A with a step resolution of 0.5$\mu$A, which is equivalent to 400 steps. Therefore, the minimum number of bits needed for the binary word and the hardware responsible for the conversion is 9 bits.

Figure 2.5 presents the general block diagram at block level of the stimulation system. It should provide compatibility with the SPI protocol, so an interface for this feature, must be part of the system. The current amplitude data word received is converted into current using a programmable current-source, which is composed by a digital-to-analog converter and a voltage-to-current converter capable of providing the necessary current. Finally, an h-bridge architecture is used to drive the scaffold, since with this circuit it is possible to control the current direction through the scaffold, using only one current source.

The in-vivo system specifications are presented in table 2.1. In addition to this specifications, the circuit area occupation should be low, since it is intended to be an implantable device, and power consumption should be as low as possible to maximize the battery autonomy.

**Table 2.1:** In-Vivo System Specifications

| Characteristics | In-Vivo System |
|---|---|
| Stimulation Mode | Current |
| Amplitude Range | 0-200$\mu$A |
| Amplitude Resolution | 0.5$\mu$A |
| Compliance Voltage | 5V |
| Frequency | 1Hz - 100kHz |
| Acquisition Support | Voltage |
| Design Approach | ASIC |
| Communication With Microcontroller | SPI |

CHAPTER 3

# Theoretical Background

This chapter has the objective of assess the different architectures for the required circuits and to present some theoretical background on these circuits. The circuits studied are: the digital-to-analog converters, the voltage-to-current converters and the h-bridge. In addition, a comparative analysis on the different circuits architectures is performed in order to choose the architectures that most fit the system requirements. Lastly, the SPI protocol, which is responsible for interfacing the ASIC with the microcontroller, operation and main features are presented.

## 3.1 Digital-to-Analog Converters

Data converters, in particular DACs, are components that are gaining more and more importance on today's electrical systems. Digital data processing reduces systems costs and hardware requirements, therefore, there is an increasing tendency to store and process data digitally. The device capable of converting data from the digital to the analog world is called Digital-to-Analog Converter. These type of components are important to interface digital components such as microcontrollers, digital sensors and communication systems.

Digital-to-analog converters receive a binary word at its input and produces at the output an analog signal. The analog output (i.e. a voltage or current) can be expressed by expression 3.1, where $V_{ref}$ is the reference voltage, D the digital word applied at the input and N the number of bits [24].

$$V_{out} = \frac{D}{2^N} \cdot V_{ref} \tag{3.1}$$

DACs can be classified based on their conversion speed, as represented in figure 3.1. Serial or pipeline DACs are implemented with charge scaling approaches and switch capacitors. The charge redistribution and the algorithmic architectures are examples of this type of DAC. These have the advantage of being simple and optimal in area, but require one clock pulse to convert one bit. Since speed on conversion is a priority for the converter, these architectures were not considered any further. On the other hand, parallel digital-to-analog converters

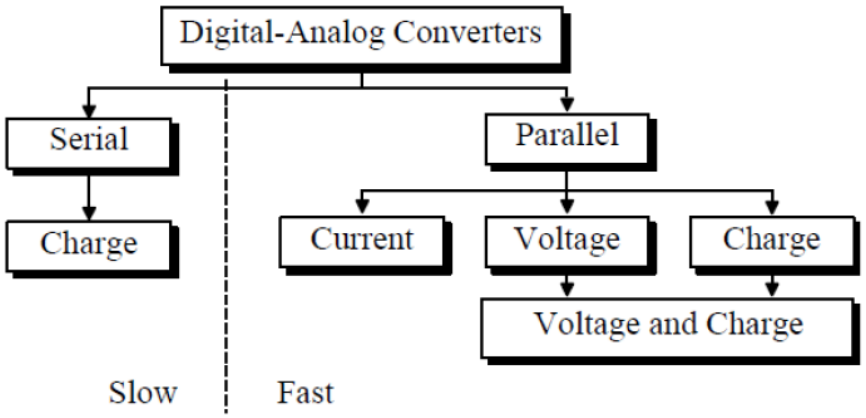


**Figure 3.1:** Digital-to-Analog Converters classifications [25]

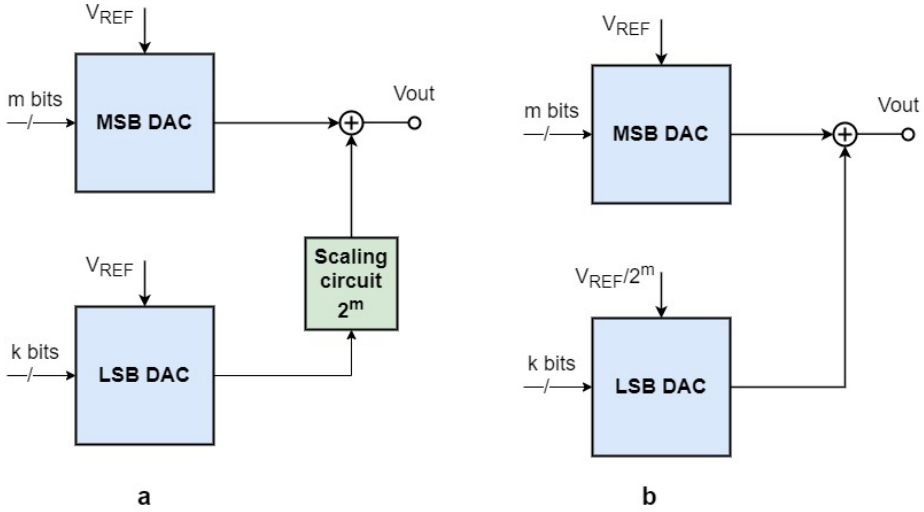


**Figure 3.2:** Subranging techniques. a - analog scaling, b - reference scaling

are faster on the digital word conversion [25]. It can use current, voltage or charge steering approaches, concepts that are going to be explored in this section.

In addition to the traditional architectures and to achieve DACs with higher resolutions, techniques of subranging are used. These techniques divide the total number of bits (N) of the DAC into k smaller sub-DACs. Sub-ranging can be made using scaling on the reference voltage (or current) or scaling the analog output of each sub-DAC. The subranging techniques are presented in figure 3.2.

### 3.1.1 General Concepts and Performance Metrics

A digital-to-analog converter converts a binary word presented at its input into an analog quantity. The N bit word presented at the input, can code $2^N$ possible analog values at the output, which is called the converter resolution. The bits presented at the input have also different weights associated. The bit with the highest value is called the Most Significant Bit (MSB) the one with the lowest is called the Least Significant Bit (LSB). In the present

document the MSB is going to be referred as the bit $b_0$ and the LSB to $b_N - 1$ [25].

A LSB can also be referred as the minimum analog output step size, which is equivalent to 3.2.

$$V_{LSB} = \frac{V_{FS}}{2^N - 1} \tag{3.2}$$

$V_{FS}$ refers to the full scale voltage. Full scale is equal to the difference between the analog output when all bits are '1' to the analog output when all bits are '0', which can be expressed by 3.3, where $V_{REF}$ is the DAC reference voltage.

$$V_{FS} = \left(V_{REF} - \frac{V_{REF}}{2^N}\right) - 0 \tag{3.3}$$

As for performance, a DAC can be characterized with static and dynamic measurements. The static measurements describe the converter behaviour when a certain word is applied at the input. The most important static characteristics are:

- Offset error: defined as the DC offset present in the DAC transfer function with reference to the ideal one. For example, when the input digital word codes an analog value of 0, the obtained analog output should also be 0.
- Gain error: defined as the difference between the slope of the actual DAC transfer function when compared to the ideal one [26].
- Differential Non-Linearities (DNL): can be defined as the maximum LSB change in the transfer function from the ideal step size. Ideally, a change of 1 LSB in digital code corresponds to a change of exactly 1 LSB of analog signal. Usually measured in LSB [26].
- Integral Non-Linearities (INL): measures the deviation from the real DAC transfer function from an ideal one in LSB [26].
- Monotonicity: A DAC is classified as monotonic when the obtained output increases with the increase of the input [26].

As for the dynamic performance, it describes the DAC behavior when digital words are changed at the input of the DAC. The dynamic errors influence mainly the conversion speed, which is the time that a converter takes to provide the analog output when digital words are changed at the input. Examples of dynamic measures used to evaluate a converter are:

- Settling Time: measures how long it takes to the converter to settle the analog output on the final value.
- Glitches: glitches are caused by changes in codes. It is defined as the overshoot and/or undershoot of the DAC output when a transition of a digital word at the input occurs. It is measured when on the highest transition of codes at the input (i.e., when it changes from 01..1 to 10..0) [26].
- Slew rate: measures the maximum rate at which a converter is capable of changing the output. Usually it is associated with the operational amplifiers needed at the output for most DAC architectures.

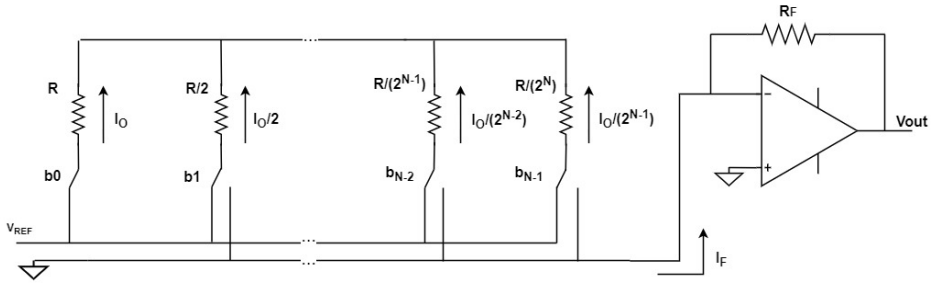


**Figure 3.3:** Binary Weighted Resistor DAC

### 3.1.2 Binary Weighted Resistor Ladder

The binary-weighted resistor DAC consists on N binary weighted resistors. The MSB is encoded with the resistance R, being the following bits resistances divided by binary factors of the MSB resistance. It is common to have the resistors connected to the inverting input of an operational amplifier in order to convert the output to voltage. In figure 3.3, it is presented a general topology of binary weighted resistor DAC.

The working principle is: based on the active switches, the resistors are connected to either the reference voltage or ground. For example, if the bit $b_i$ is 1, the resistor $2^{i-1}R$ is connected to $V_{Ref}$. In contrast, if the bit is 0 the resistor is connected to ground. In those connected to the reference voltage a binary weighted current flows through these resistors. Since at the inverting input there is a virtual ground, the current flowing on the resistors is summed up and flows through the feedback resistor $R_F$. The analog voltage at the output of the DAC is given by equation 3.4, where $b_i$ represents the logic level of the bit i. Note that the $R_F$ resistor can be used to scale the voltage at the output.

$$V_{out} = -R_F I_F = -R_F V_{Ref} \left( \frac{b_0}{R} + \frac{b_1}{2R} + ... + \frac{b_{N-1}}{2^{N-1} \cdot R} \right) \tag{3.4}$$

This architecture is simple to implement. However, increasing the resolution, requires an increase on the components value spread, which is unfeasible for high resolution DACs. Moreover, the resistors matching is low due to variations on the fabrication process, decreasing the bits accuracy. Additionally, the power dissipation is higher than in other architectures. Finally, the switches on resistance must be low, otherwise it will affect the resistors' value significantly [24].

### 3.1.3 R-2R Ladder

The R-2R ladder architecture is an alternative to the binary-weighted resistor that eliminates the large component spread from the latter. It consists on a ladder of resistors with resistances R and 2R as it is shown in figure 3.4. With this topology, binary weighted currents are achieved, since the currents are reduced by factors of two when flowing from the left side of the resistor ladder to the right side [25]. As the previous case, an operational amplifier is usually included at the output, with the current from the resistor ladder entering in the inverting output of the amplifier. This way, the currents are summed up and converted to voltage at the output through the feedback loop.

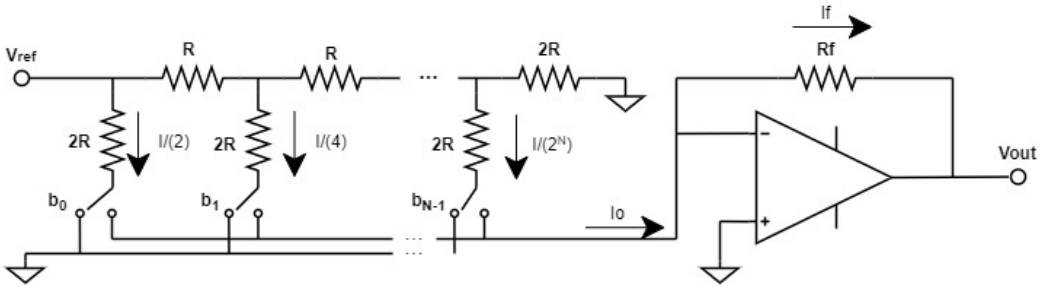


**Figure 3.4:** R-2R Ladder DAC

This DAC architecture is widely used since it is fast and simple to implement, with small components spread. However, there is always a path of resistors conducting, therefore it is not energy efficient. In addition to this disadvantage, the number of R and 2R resistors needed increase linearly with the resolution, therefore it can also be inefficient regarding area occupation. Finally, this architecture can be affected by mismatches on the resistors, due to the fabrication process, which may decrease the converter accuracy [27].

### 3.1.4 Binary Weighted Current Source

Binary weighted current scaling DACs have similar implementation as the binary weighted resistor ladder, the difference is instead of using resistors acting as current sources, transistors are used. A general schematic of this type of architecture of DAC is presented in figure 3.5. It is composed by N current sources, each one producing a binary scaled current.

To produce each of the currents, several techniques can be used, namely:

- Implement each individual current source with one transistor, where the dimension ratio of each is scaled with binary weighted dimensions ratio [14]. However, this approach leads to high spread in the transistors size ratio, if high resolution is needed. Additionally, it is sensible to layout mismatches on the transistors, which may introduce errors on the conversion.
- A second approach used to reduced the mismatch problems with the previous architecture is to use transistors with similar dimensions ratio and place the transistors in series or in parallel, creating binary weighted current sources as presented in [28], [13]. These

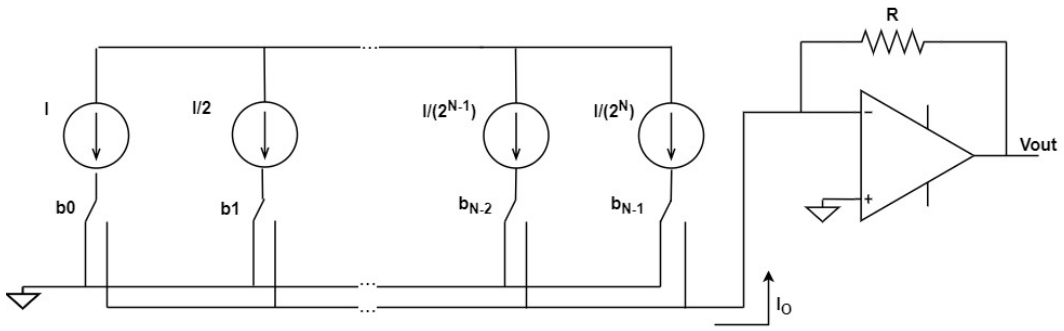


**Figure 3.5:** Binary-weighted current source

topology still presents problems. With the increase of the resolution needed, the number of components used increase, as well as the circuit complexity.

These DACs output is usually given in current, but can also have an output in voltage. For that a current to voltage converter based on an operational amplifier is used.

Overall these presented current scaling architectures provide fast conversion. However, for high resolution circuits, they get complex, power dissipation is high when compared to the charge scaling approach and components mismatch can affect significantly the DAC's performance [29].

### 3.1.5 Current Scaling with Similar Current Sources

Another approach on current scaling DACs is to use similar current sources, which divide a reference current. Digital codes are then used to activate each of the current sources. A common digital code used to enable the current sources are thermometer codes. A general representation of current scaling DACs with a thermometer decoder is presented in figure 3.6. The output of each signal from the binary-to-thermometer decoder is connected to a switch that controls a current source. To activate the equivalent to a certain binary word, the decimal number of current sources must be enabled (i.e. if the input code is 100, 4 current sources are enabled).

This type of architecture is widely used since it is always monotonic, due to the fact that for a certain binary word an equivalent number of current sources being enabled. Weaknesses on components mismatch are reduced, since to guarantee a monotonic DAC, the mismatch should be less than 50% [30]. For these reasons, the thermometer coded current scaling DACs, provides a high speed and accurate conversion. However, this architecture has also disadvantages. The number of current sources needed grows with the number of bits needed. For N bits, it is needed $2^N$ current sources, which increases the circuit's complexity and area

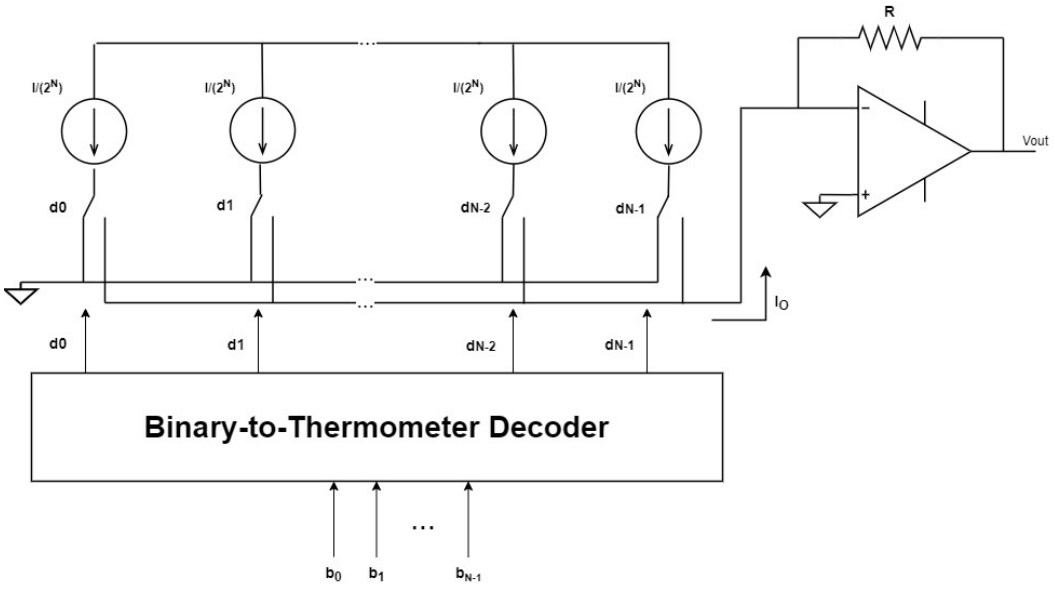


**Figure 3.6:** Current scaling with thermometer decoder

occupation. In addition, it is needed additional hardware to decode binary to thermometer, which increase the complexity, area occupation and dynamic power consumption. Finally, this architecture power dissipation is much higher than the charge scaling counterpart.

The implementation of the thermometer decoded DACs is diverse. In [16], two thermometer decoders are used, one for the MSB part of the DAC and the other for the LSB part, with the scaling being made on the reference current. In [14] and [31], a matrix of current sources is made, where a binary-to-thermometer decoder decodes the matrix rows and other the columns. In reference [32], a 10 bit DAC is presented, which combines a 6 bit thermometer decoded DAC at the MSB with a binary weighted for the 4 LSB bits.

### 3.1.6 Resistor String Voltage Scaling

A typical topology for the voltage scaling DAC is presented in figure 3.7. It consists on $2^N$ resistors in series, where all resistors have the same weight (value). Since at the top of the resistor ladder is the reference voltage and at the bottom is ground, the analog output is produced by the direct voltage division of the resistors. The switches select the resistors used for the voltage division and consequently the output voltage. The presented topology uses decoders that receive as input the bits and activate the resistor ladder taking into consideration the active bits [25].

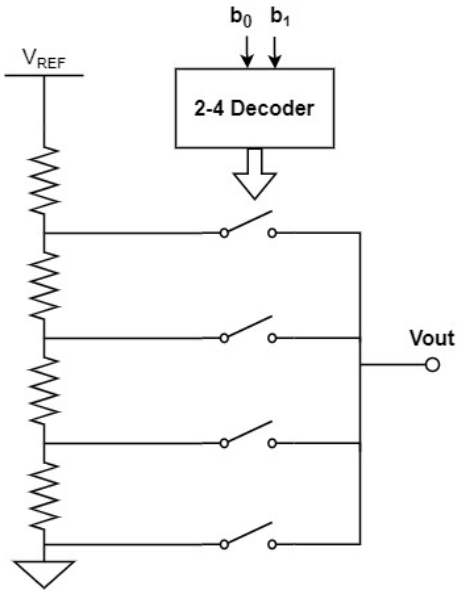


**Figure 3.7:** Voltage scaling DAC

This architecture is simple to implement and guarantees that the DAC is monotonic. However, for high resolutions, a large number of resistors is needed, which is inefficient on area occupation. Another problem of this architecture is that it is sensible to parasitic capacitances at each node, especially for higher resolutions degrading the conversion speed [25].

### 3.1.7 Binary Weighted Charge Scaling

Charge scaling digital-to-analog converters are a popular choice in CMOS technology. A binary weighted charge scaling DAC is presented in figure 3.8. The converter is composed

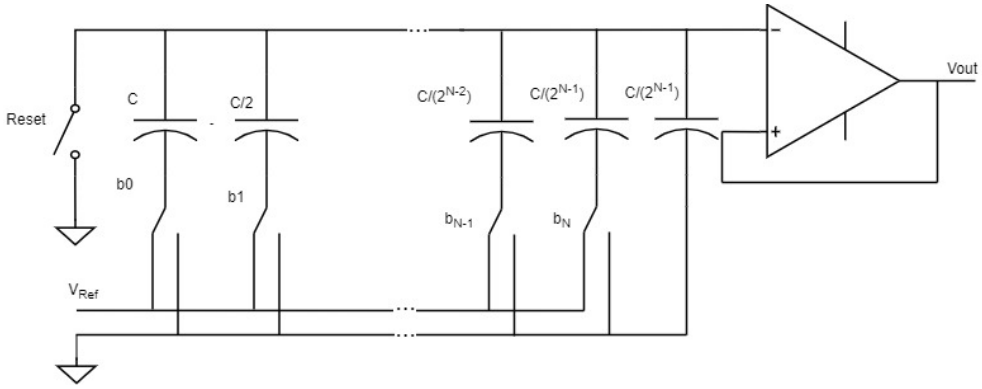


**Figure 3.8:** Binary Weighted Charge Scaling DAC

by parallel array of capacitors with binary weighted values, a switching network and an operational amplifier in buffer configuration. The operation is based on the principle of "capacitive attenuation of the reference voltage" [25]. This means that the capacitors array work as voltage attenuators of the reference voltage, being the output a function of the capacitors connected to the reference voltage. In most implementations, an operational amplifier is included at the output in order to provide a virtual ground at the output node of the converter, isolating the capacitor array from the remaining circuit and reducing capacitive load effects on the converter, which could degrade the conversion.

The operation of this converter is made in two phases. First is the reset phase where the reset switch is activated and all the capacitors are connected to ground where they discharged. The second phase happens after the capacitors being discharged. It starts when the reset switch is disabled and a digital word is presented to the switches array at the DAC input. Each of the bit connects a capacitor top plate to ground or to the reference voltage, if the bit presented is '0' or '1' respectively. After the activation of the switches with the digital word, the DAC computes the correspondent analog voltage. Applying the Thevenin equivalent at each input bit, it can be obtained the voltage expression at the DAC output 3.5.

$$V_{out} = \left[\frac{b_0}{2} + ... + \frac{b_9}{2^N}\right] \cdot V_{Ref} \tag{3.5}$$

The binary weighted charge scaling DAC is characterized for having low power dissipation since it is mainly composed by capacitors, being simple to implement, providing high accuracy and conversion speed. As for the main disadvantages, this DAC is sensible to parasitics and capacitors mismatch, which increase the inaccuracy of the converter. Additionally, for higher resolutions, the number of capacitors needed increase to $2^N$. To mitigate the second disadvantage, analog sub ranging techniques can be used. These techniques are based on dividing a N bit converter into various B bits converters with scaling capacitor in between the subDACs. As for the parasitic present on the converter, its effects can be reduced with the inclusion of certain techniques into the layout design. Some of them are: connecting the capacitors top plate to the output node and the common centroid technique [33], [34] [35]. These techniques helps improving the components matching, as well as, reducing the parasitic

effect. This converter architecture is very popular as a block for Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)s ([36]) and for low power applications where an interface from the digital to analog worlds is needed [37].

### 3.1.8 C-2C Ladder

The C-2C ladder DAC is a charge scaling DAC that aims to reduce the usage of high relations of capacitors from the binary weighted charge scaling approach, and consequently, to reduce the area consumption. The architecture of this DAC is presented in figure 3.9. This converter presents an architecture similar to the R-2R but, instead of resistors it is used capacitors. A switching network is also part of the architecture, where each switch is connected to a terminal of a capacitor with value C. These switches are responsible of enabling and disabling the capacitors used on the conversion, by connecting each capacitor to the reference voltage if the bit at the input is "1" and to ground if it is "0" [38]. Using the Thevenin equivalent recursively on each input bit, it can be proven that this DAC follows expression [38].

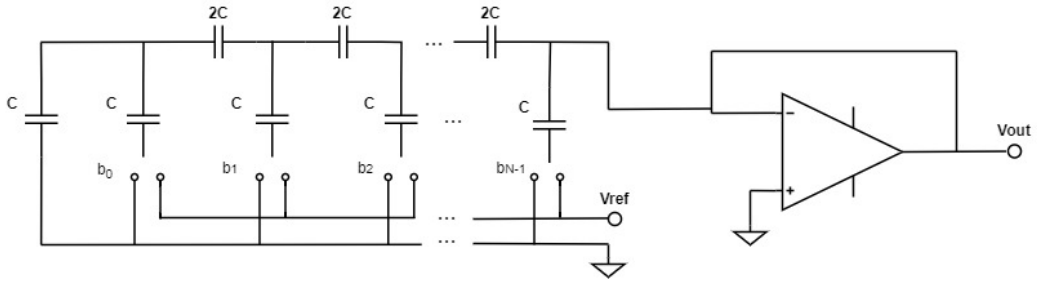


**Figure 3.9:** C-2C Ladder DAC

$$V_{out} = D_0 \frac{V_{ref}}{2} + ... + D_{N-1} \frac{V_{ref}}{2^N} \tag{3.6}$$

The advantages of this architecture include low power consumption, low area occupation and high speed on conversion [39]. The disadvantage of this converter is the fact that it is sensible to parasitics on the interconnecting nodes, which cause an increase in the converter non linearities, therefore, affecting the converter accuracy. Due to this factor the usage of this type of architectures is, usually, limited to DACs of 6 bits [40]. Reference [41], presents an implementation of a C-2C DAC with floating voltage shield to reduce the parasitic influence on the converter and increasing its usage and resolution. Finally, [39] present the usage of the C-2C with other DAC architectures such as the binary charge scaling and with the use of thermometer decodes, respectively.

## 3.2 Voltage-to-Current Converters

The Voltage-to-Current (V-I) converter is an analog block that takes at its input a voltage and converts it into an appropriate current. These blocks are important components in analog and mixed signals applications such as analog multipliers, variable gain amplifiers, sensor

interfaces, continuous-time filters and data converters [42]. A V-I converter should have a high linear relation between the input voltage and the produced current, appropriate bandwidth, be insensitive to load effects and have high input resistance [43]. Additionally, for low power and supply voltage applications, a near rail-to-rail operation and low power consumption are important factors to take into consideration on the design.

The present section is going to revise classical V-I converters architectures, as well as present current high performance architectures that were taken into consideration on the system design.

### 3.2.1 Current Mirrors

Before entering into the voltage to current converters, typical architectures of current mirrors are going to be introduced, since it is a major component for this analog block. Current mirrors are widely use as biasing elements and amplifier stages [44].

Current mirrors are important analog blocks that receive at its input a certain current and replicates it at its output. The current provided at the output can be similar or a scaled version, by applying a certain gain (K), to the input current (expression 3.7). Ideally, a current mirror should have: zero input impedance, infinite output impedance and the output to input relation should be a linear curve.

$$I_{out} = K \cdot I_{in} \tag{3.7}$$

Figure 3.10 present some of the classic current mirror approaches. In 3.10a, the simple current mirror is presented. In this topology, assuming that the transistors have equal length, the output current is given by the ratio of the width of transistor M2 over transistor M1, multiplied by the input current. However, this architecture is severely sensitive to the transistors matching. Furthermore, it is sensible to deviations on the transistors' $V_{ds}$. If these parameters are not fully matched, the current copy accuracy is poor. In addition, the output resistance which is given by $\frac{L}{\lambda I_D}$ (transistor $r_{ds}$), which can be low for several applications [44].

In 3.10b, the cascode current mirror is presented. It includes one additional transistor in each side of the mirror. M1 and M3 should have the same size ratio as well as M2 and M4. This way, if the same length is used, the relation of currents is the same as the simple current mirror case. The advantages of this architecture is that the current copy accuracy is increased since the mismatch effects are attenuated by adding the extra current mirror in series and the output resistance is increased to $R_{out} = r_{ds2} + r_ds4(1 + gm_4rds2)$ [44]. However, the compliance voltage at the output may be low for low power applications, since the maximum voltage for the circuit to operate, in saturation region, is given by $V_{DD} - V_{DS2} - V_{DS4} - V_T$ and the minimum voltage needed is $V_{DS1} + V_{DS3} + 2V_T$.

The wide swing cascode current mirror is presented in figure 3.10c. This architecture is an improvement to the typical cascode current mirror and was designed to increase the output voltage swing, while maintaining good mirroring accuracy. The maximum output voltage compliance is $V_{DD} - V_{DS2} - V_{DS4}$, which is an increase in output swing when compared to

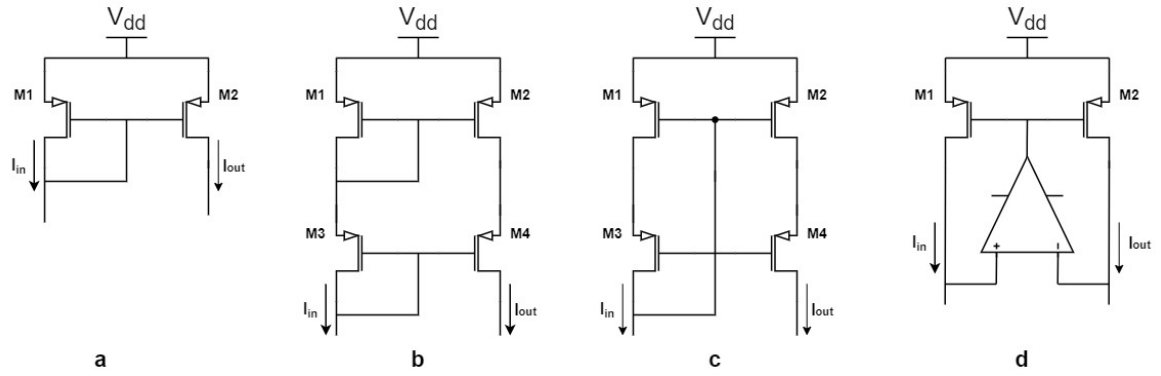


**Figure 3.10:** Current mirror architectures. a) simple current mirror; b) cascode current mirror; c) wide-swing cascode current mirror; d) regulated current mirror

the cascode current mirror. As for the minimum input voltage, it requires a voltage of at least $V_{DS1} - V_T$ to operate. Additionally, the wide swing current mirror offers a lower input resistance ($1/gm$) when compared to the regular cascode architecture, since the drain of M4 is connected directly to the gate of M1, while still offering the same output resistance [45].

The final current mirror presented is in figure 3.10d [42]. This architecture uses an error amplifier which ensures that $V_{DS1}$ is equal to $V_{DS2}$, due to the virtual short circuit. This way, it provides an accurate current mirroring and increases the current mirror working range since the minimum input voltage necessary to operate is $V_{DS1}$ and the maximum is $_{VDD} - V_{DS2}$. However, it presents the drawback of needing an additional operational amplifier, which increases the power dissipation, area occupation, circuit complexity and limits the current mirror bandwidth.

### 3.2.2 Conventional V-I Converter

The most common topology of a voltage-to-current converter consists of an operational amplifier driving a NMOS transistor, a current mirror of P-Channel Metal Oxide Semiconductor (PMOS) transistor to replicate the current to the output and a resistor to ground on a negative feedback loop as shown in figure 3.11. In this architecture, the input voltage is presented at the input of the operational amplifier and is fed to the resistor through a negative feedback loop. The resistor is responsible for converting the input voltage into the desired current. In the presented figure example, the current is mirrored and is fed onto the load. Several types of current mirrors can be used at the output as the ones described previously.

The current through the resistor can be given by equation 3.8. This current however, can be scaled by providing a current gain or attenuation (K) with the current mirror at the output, so the output current can be given by 3.9.

$$I_R = \frac{V_{in}}{R} \tag{3.8}$$

$$I_{out} = K \cdot \frac{V_{in}}{R} \tag{3.9}$$

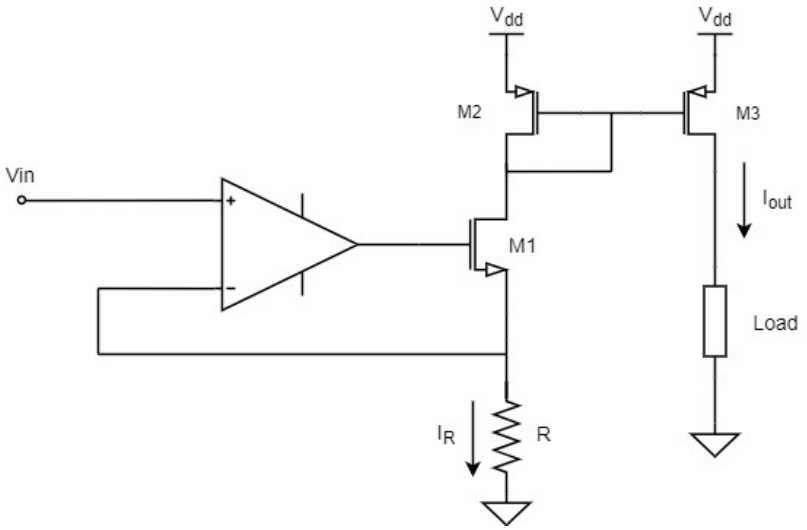


**Figure 3.11:** Conventional V-I Converter

The output swing is limited by the minimum voltage necessary for the current mirror transistors to operate in saturation region. This way, the output swing from this topology goes from 0 to $V_{DD} - V_{DS1} - V_{T1}$. Increasing the M1 transistor size ratio, $V_{DS1}$ can be reduced, but this topology still has a limited output swing, specifically low for applications where having high operating range is a priority. Furthermore, if the $V_{DS}$ of M2 and M3 transistors is not exactly the same, the current copy accuracy to the output will be degraded. Nevertheless, this architecture provides a high input impedance, since the voltage is presented to an operational amplifier input [46].

### 3.2.3 Wide-Swing V-I Converter

The wide-swing V-I converter presents a similar architecture as the conventional one, only that instead of using an operational amplifier driving a NMOS transistor, it uses an OTA driving the PMOS transistor that is responsible for the current mirroring to the output as presented in figure 3.12. The working principle is also similar the previous architecture. The voltage to convert is provided at the input of the OTA, which is presented to a resistor that is responsible for the conversion to current with a negative feedback loop. Then, the current flows through a current mirror with a gain (K) that is responsible to scale the converted current and deliver it to the output. The feedback loop appears to be positive, but transistor M1 is in a inverting common source configuration, which makes the feedback negative. The output current can be also expressed by equation 3.9.

The wide-swing V-I converter presents a major advantage. Since the OTA drives directly the current mirror PMOS transistor, the converter output swing is extended to $VDD - V_{DS2}$, which is equal to the voltage swing of a simple current mirror. When the input voltage is higher than this value, the transistor M1 leaves the saturation region and works on the triode region. As consequence, the converter stops being linear at these voltages.

To summarize, the wide-swing V-I converter presents similar operation as the conventional. It is sensitive to mismatches on the $V_{DS}$ of M2 and M3 transistors. The voltage swing is

extended, however several applications may require a higher voltage swing.

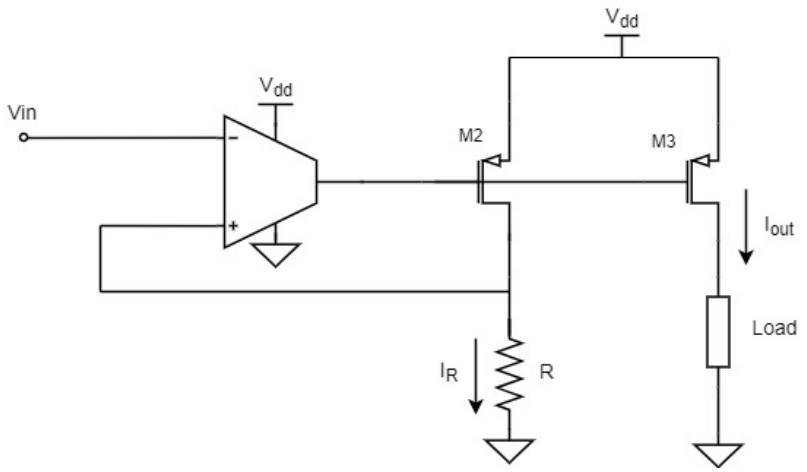


**Figure 3.12:** Wide-Swing V-I Converter

### 3.2.4 Rail-to-Rail V-I Converter

To extend even further the output swing from the wide-swing V-I converter architecture, three different architecture based on the same principle of operation have been proposed [47]. The three converters are the Feedforward Voltage Attenuation (FFVA), the Feedback Voltage Attenuation (FBVA)) and the Feedforward Current Attenuation (FFCA). The working principle behind these architectures is to attenuate the input voltage before fed it to an wide-swing V-I converter. The advantage of this, is to maintain the current mirror transistors working in the saturation region for the entire voltage swing.

*Feedforward Voltage Attenuation V-I converter*

The Feedforward Voltage Attenuation architecture is presented in figure 3.13. This circuit is composed by a main wide-swing V-I converter that is responsible for converting the input voltage to current and mirror it to the output and to a voltage attenuator (comprised by the transistor M1, the input OTA and the resistors R1 and R2) before the main converter. The principle of operation is the following: the input voltage is fed to an OTA, which, using negative feedback, presents this voltage into a resistive voltage divider that attenuates this voltage by a factor $\alpha$. The attenuated voltage ( $\alpha \cdot V_{in}$) is then fed to the main wide-swing converter. Finally, the voltage presented is buffered to the resistor Rs, which converts the voltage to current in similar fashion as previously explained.

Since the voltage presented to the main converter is between 0 and $\alpha \cdot V_{in}$, if the attenuation factor is sufficiently low, the current mirror transistors never leave the saturation region, therefore, rail-to-rail operation is achieved if the voltage presented at the input is also rail-to-rail. Again, a current gain (K) can be used on the current mirror to scale the output current. The example presented uses a cascode current mirror since it provides a good copy of the

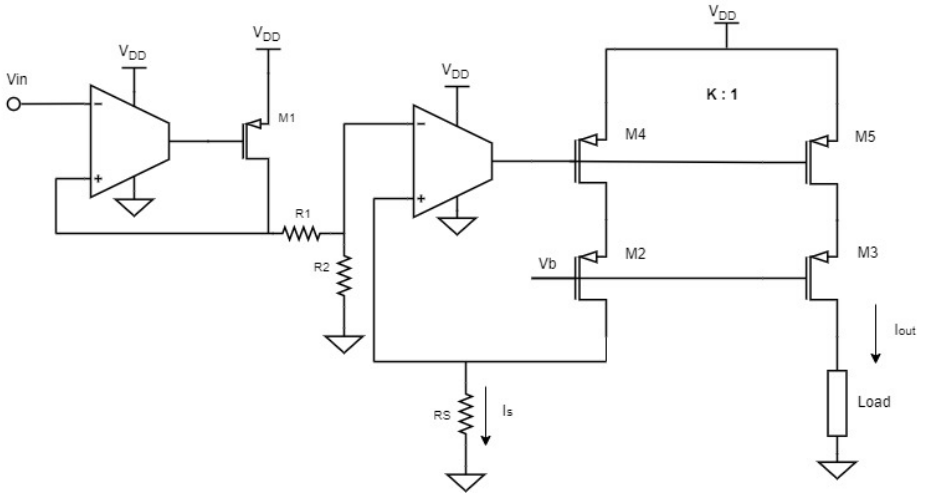


**Figure 3.13:** Feedforward Voltage Attenuation V-I Converter

current and a high output impedance. However, different types of current mirrors can be used to perform the current copy. The output current is given by expression 3.10.

$$I_{out} = \alpha \cdot \frac{V_{in}}{K \cdot R_s} \tag{3.10}$$

As it is reported in [47], high linear relation between the input voltage and output current and a near rail-to-rail operation is achieved with this topology. The factor that limits the signal excursion is that M1 for voltages above $V_{DD} - V_{DS1}$ works in the triode region. To decrease $V_{DS1}$ as much as possible, high transistors dimension ratios can be used. Increases in this transistor size relation, however, decreases the converter performance regarding bandwidth. Note that for the present application, bandwidth requirements are not demanding.

*Feedback Voltage Attenuation V-I converter*

The Feedback Voltage Attenuation V-I converter is presented on figure 3.14. In this architecture, the voltage attenuator is composed by the resistors R1 and R2, the bottom OTA and M1 transistor. The main differences of this architecture from the previous is that the OTA from the main converter is responsible for receiving the input voltage and providing it to the voltage divider, using negative feedback (provided by the OTA and the M1 transistor in common source configuration). The attenuated voltage is then provided to the resistor responsible for the voltage to current conversion by the voltage attenuator OTA. Then, the process of conversion is the same as previously described. The $R_S$ resistor converts the attenuated voltage into a proportional current and the output current source scales the current with a current gain K and provides it to the output load. This way, the obtained equation is similar as the FFVA case presented in 3.10.

The FBVA presents a very similar architecture as the FFVA, only that the voltage attenuator is placed in the main converter negative feedback loop, which may cause stability problems [47]. For this reason, this architecture is slightly more complex than the previous considered.

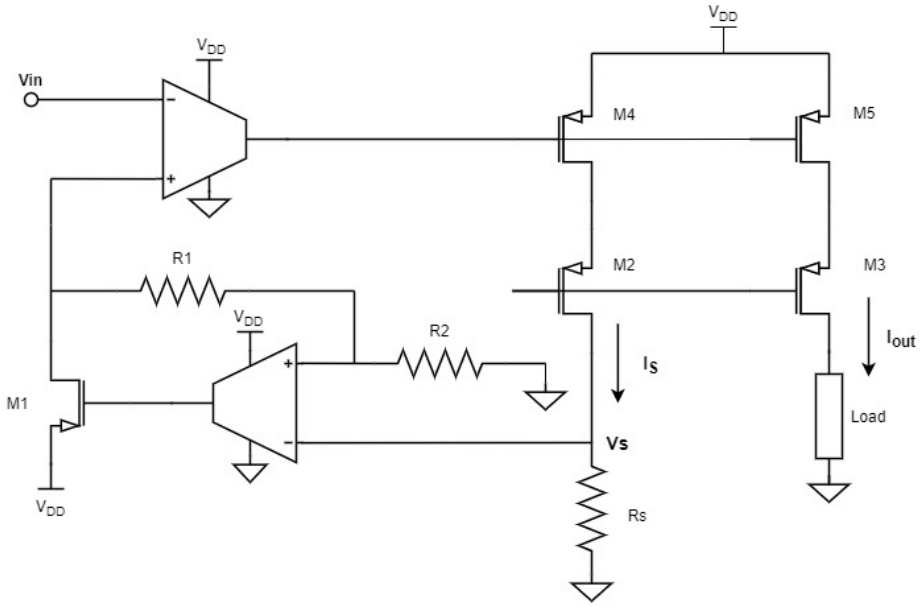


**Figure 3.14:** Feedback Voltage Attenuation V-I Converter

*Feedforward Current Attenuation V-I converter*

Finally, the Feedforward Current Attenuation V-I converter approach is demonstrated on figure 3.15. The principle of operation of this converter is similar to the other two, however it uses a slightly different architecture. In general, the FFCA is composed by two wide-swing voltage to current converters. The input voltage is presented at both OTAs' inverting inputs. The first stage, converts the presented input voltage into a proportional current by the R1 resistor. The obtained current is mirrored and provided to the second stage with a current gain K1. At this point the current can be described by equation 3.11.

$$I_{out} = \frac{V_{in}}{K1 \cdot R_1} \tag{3.11}$$

Since the OTA input resistance is high, the current $I_1$ drives the resistor $R_2$ between the non-inverting input of the OTA (from the second stage) and the $R_S$ resistor. With the inclusion of $R_2$, it is possible to attenuate the input voltage presented at the second stage.

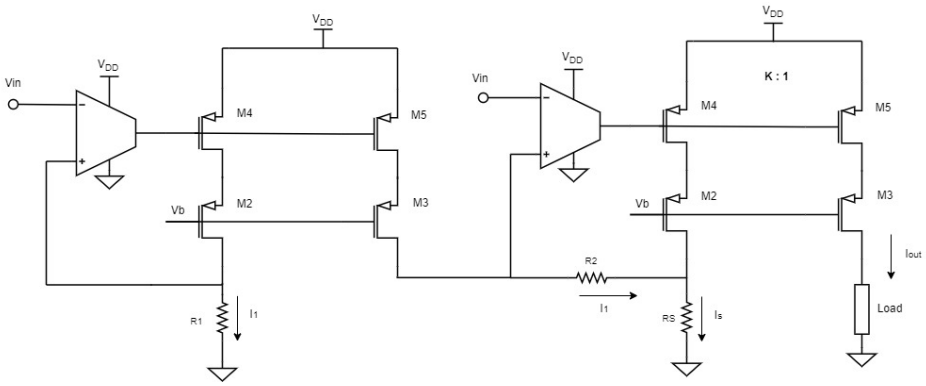


**Figure 3.15:** Feedforward Current Attenuation V-I Converter

Observing the second stage of the converter, the voltage present at the inverting input, is the input voltage and, the non-inverting input is equal to the voltage present at the resistor $R_S$ ($V_S$) plus the voltage drop at $R_2$ resistor ($V_2$). Since the voltage at both inputs from the OTA are at the same voltage, relations 3.12 and 3.13 can be used to relate the voltage presented to the resistor $R_S$.

$$V_+ = V_- <=> V_s - V_2 \cdot R_2 = V_{in} \tag{3.12}$$

$$V_s = V_{in} - \frac{V_{in}}{KA \cdot R_1} \tag{3.13}$$

From 3.13, the attenuation factor $\alpha$ can be obtained and is equal to 3.14. It is dependant on the resistors $R_1$ and $R_2$ value, as well as, the current gain from the current mirror of the first stage (K1).

$$\alpha = \frac{K1 \cdot R_1 - R_2}{K1 \cdot R_1} \tag{3.14}$$

Finally, having obtained the voltage at the resistor $R_S$, it is converted into current with the methodology previously explained for the wide-swing converter approach. This current is then mirrored with a gain K2 to the output. The output current can be given by expression 3.15.

$$I_{out} = \frac{V_S}{K2 \cdot R_S} \tag{3.15}$$

In general, this converter topology presents similar performance and characteristics as the previous, however, it is more complex to implement and to scale.

## 3.3 H-Bridge

H-Bridge circuits are commonly used to applications such as, driving DC motors, DC-DC converters, class D audio amplifiers and robotics [48].

The particularity about the h-bridge circuit is that it allows the control of the direction of a current applied to a certain load using only one current source. A general topology for this circuit is presented in figure 3.16. It is composed by 4 switches that form an H shape, with the load to drive in the middle and a current source that provides the necessary current. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) transistors can be used as the bridge switches. The working principle of this circuit is the following:

- When the S1 and S4 switches are activated and S2 and S3 are ”off”, the current flows through the load using the path formed by S1 and S4.
- When the S2 and S3 switches are activated and S1 and S4 are ”off”, the current flows through the load using the path formed by S2 and S3. So, in the reversed direction from the previous case.
- When all the switches are in the ”off” state, no current flows through the load.
- The circuit operation prevents the situation where the switches are all closed.

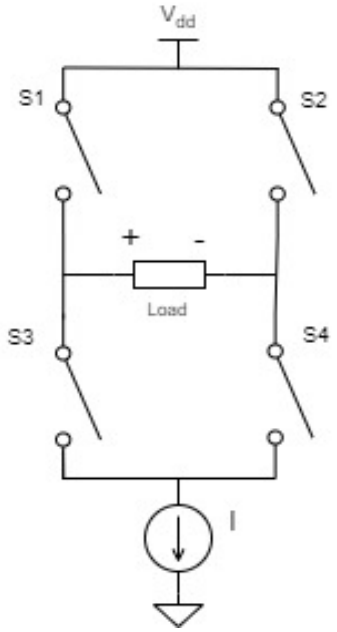


**Figure 3.16:** H-Bridge general architecture

Therefore, the current applied to a certain load can be bidirectional. A summarized h-bridge operation is presented in table 3.1.

**Table 3.1:** H-Bridge control logic truth table

| S1 | S2 | S3 | S4 | Voltage across the load |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | OFF |
| 0 | 1 | 1 | 0 | Negative |
| 1 | 0 | 0 | 1 | Positive |

Having the pair S1 and S3 or the pair S2 and S4 active simultaneously it is, in most cases, not desirable since it can damage the bridge transistors. However, in some applications, these states are desired (i.e. for braking a motor), being used diodes to protect the switches.

To complement the direction control, in applications such as DC motors driving, the motor rotation speed can be controlled by applying Pulse Width Modulation (PWM) signals to the pair of opposite transistors part of the h-bridge. For the case of the present application, the parameters that need to be controlled are the direction of the current (controlled by pulses from the microcontroller) and the current amplitude applied (controlled by the usage of the programmable current source).

### 3.3.1 MOSFET Switch

A MOSFET device can work as a switch by biasing it in the cutoff or in the triode regions. When biased in the cutoff region, no current (to be more precise, small amount of current) flows through the MOSFET, being equivalent as a switch in the open state. In contrast, when biasing the MOSFET in the triode region, the current that flows is linear to the $V_{DS}$ applied

to the transistor (which is small to keep the MOSFET device in triode). When in triode, the MOSFET is equivalent to a switch in the closed state.

Ideally, a MOSFET when working as a switch should have no voltage losses when operating in the ”on” state (zero ”on” resistance), when in the ”off” state the resistance between the source and drain should be infinite and there should be no restrictions on the commutation speed. These characteristics do not happen in practice. Namely the on resistance is a characteristic that should be focused on the switch design on low power applications. The on resistance parameter ($r_{DS}$) is given by the ratio of $V_{DS}$ and $I_{DS}$ as represented in expression 3.16 [49].

$$r_{DS} = \frac{V_{DS}}{I_{DS}} \tag{3.16}$$

Considering a NMOS transistor, the $I_{DS}$ in the triode region can be given by equation 3.17, when considering that $V_{DS}$ is much smaller than $V_{GS} - V_T$ [49].

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)V_{DS} \tag{3.17}$$

Therefore, replacing equation 3.17 in equation 3.16, the $r_{DS}$ when the transistor is conduction in the triode region can be obtained in relation to the geometry of the transistor and $V_{GS} - V_T$ (equation 3.18) [49]. Analysing expression 3.18, it can be seen that maintaining a certain $V_{GS} - V_T$, to reduce the ”on” resistance the transistor dimension ratio should be increased. So, when low resistance is required, the switches' size increase, which have consequences in area consumption. Furthermore, increasing the transistors size, the dynamic power consumption increases, being also factor to take into consideration.

$$r_{DS} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)} \tag{3.18}$$

### 3.3.2 CMOS Switch

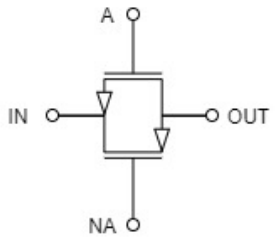


**Figure 3.17:** CMOS Switch

The CMOS switch (or transmission gate) improves the MOS switches dynamic range and reduces the resistance when conducting, by combining in parallel a NMOS and a PMOS switch as represented in figure 3.17. Since they are combined in parallel, when in conduction the equivalent resistance is also the parallel of the two transistors, therefore, the ”on” resistance is reduced [25]. Additionally, since the CMOS switch is a combination of a NMOS and a PMOS, for lower output voltages the NMOS is the only transistor conducting, being the resistance

only due to this transistor. On the other hand, if the switch voltage is near $V_{DD}$, only the PMOS is conducting and the resistance is only due to this transistor. Therefore, the dynamic range of the switch is increased, using the best operating regions of both transistors.

The CMOS switch is controlled by two complementary signals ("A" and "NA"). When "A" is in the high state, "NA" is in the low state and vice versa. When a high signal (for example $V_{DD}$) is applied to "A" the NMOS transistor conducts and a low signal (i.e. ground) is applied to the PMOS, and therefore both transistors are conducting. On the other hand, if a low signal is applied to "A", both transistors are on the off state.

In conclusion, the CMOS switch provides reasonable values for the "on" resistance, while requiring transistors with smaller dimension ratio and, therefore, occupying less area.

## 3.4 Serial Peripheral Interface

As it is presented on the system specifications, the ASIC should support communication with the microcontroller using the Serial Peripheral Interface (SPI) communication protocol. The SPI is a protocol that is suited and commonly used for communications between integrated circuits, or between integrated circuits and external peripherals and microcontrollers [50]. SPI is used in a large variety of devices such as: sensors, memory cards, ADCs, DACs, display drivers and communication between microcontrollers [50].

SPI is a synchronous communication protocol that presents a "Master-Slave" architecture with a single-master. This means that one device (called "master") is responsible for establishing communication (with the "slave" device) and controlling the data transfer. Additionally, the master is the only device of the capable of controlling the clock, synchronising the master and the slave. It is a full-duplex communication protocol, this means that it has the capability of bidirectional communication between the master and slave. However, it is possible to perform communication only from the master to the slave ("write" operation) or from the slave to the master ("read" operation). For the first case it is of the master device responsibility, to discard the received information, and on the second case it is the slave device responsibility to do so [51].

The SPI protocol requires 4 signals to operate [51]:

- Clock signal (SCLK). It is sent from the master to all slaves and synchronizes all the communication system devices.
- Chip Select (CS) or Slave Select (SS) signal. It is activated by the master and is used to select the slave to establish communication. It is usually enabled at the "LOW" state.
- Master Output Slave Input (MOSI). Serial data line, used for the master to send information to a certain slave.
- Master Input Slave Output (MISO). Serial data line, used for the master to receive information from a certain slave.

In addition to these signals, since a certain master can be connected to multiple devices ("slaves"), a slave select signal is needed for each one of the slaves. Figure 3.18a demonstrates the SPI interface for one slave device and figure 3.18b presents the signal interface for multiple slave devices, where for each slave device there is a slave select signal. It is important to note

that, even though multiple slaves can be connected to a single master, the master can only establish communication with a single slave device at a time. In addition to the presented bus architectures, a third one is presented in 3.18c, called daisy-chain. With this architecture, it is possible to have multiple slaves connected to the master using only one slave select signal. This is possible by connecting the MISO of each slave to the MOSI of the next, this way the group of slaves is seen by the master has a single slave with higher size. If each slave can work with b bits, the group of slaves (N) behave has a single slave of size N*b bits.

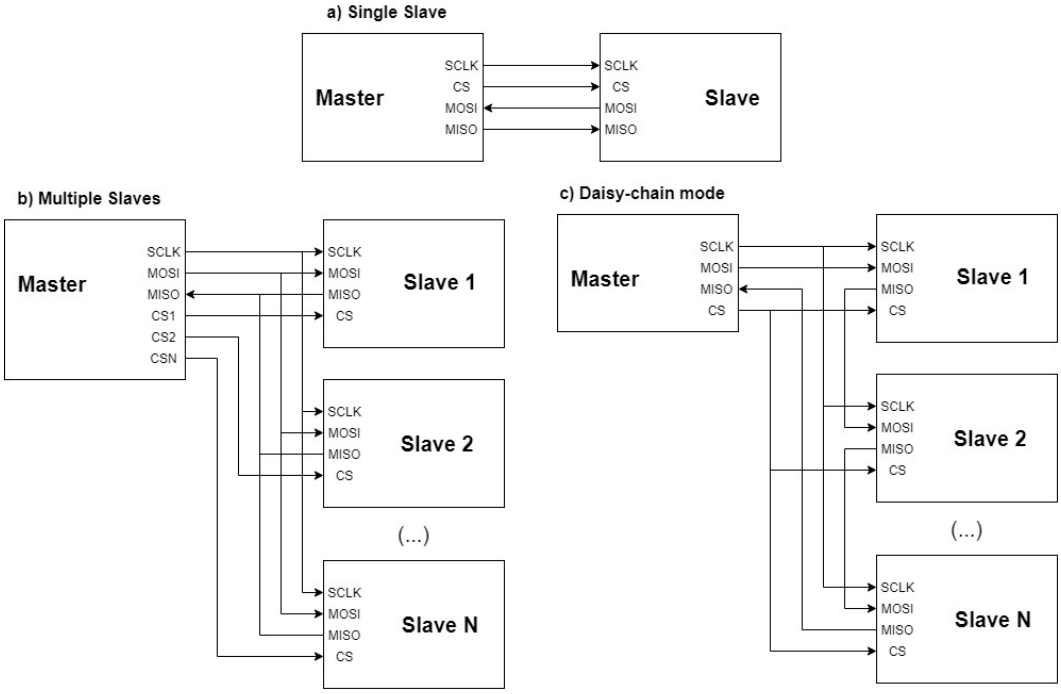


**Figure 3.18:** a. SPI master connected to a single slave, b. SPI master connected to multiple slaves, c. SPI communication in daisy-chain operation [51]

In figure 3.19, an example of the protocol operation is presented. Before the communication process, the master configures the clock signal at a frequency of operation supported by both the slave and the master devices. The SPI master starts the communication process, which can be to send or to receive information, by activating the chip select signal line (pulling low) of the desired slave device and the clock signal is enabled at the previous configured frequency. At each clock edge (in the presented case at the falling edge of the clock), an information bit generated by the master is put on the MOSI line and an information bit generated by the slave device is put on the MISO line. At the opposite clock edge (rising edge), the information on the MOSI line is sampled by the slave and the information on the MISO is sampled by the master. The information is transferred, using the described process, one bit per clock cycle until the end of the data stream. When the data transfer is finished, the slave select line and the clock signal are deactivated [52].

The SPI protocol has 4 modes of communication. These modes are dependent on two bits, the CPHA and the CPOL. The CPOL bit indicates the clock logic level when it is on the idle state (when it is not active). This means that if CPOL is set to ”1” the clock will

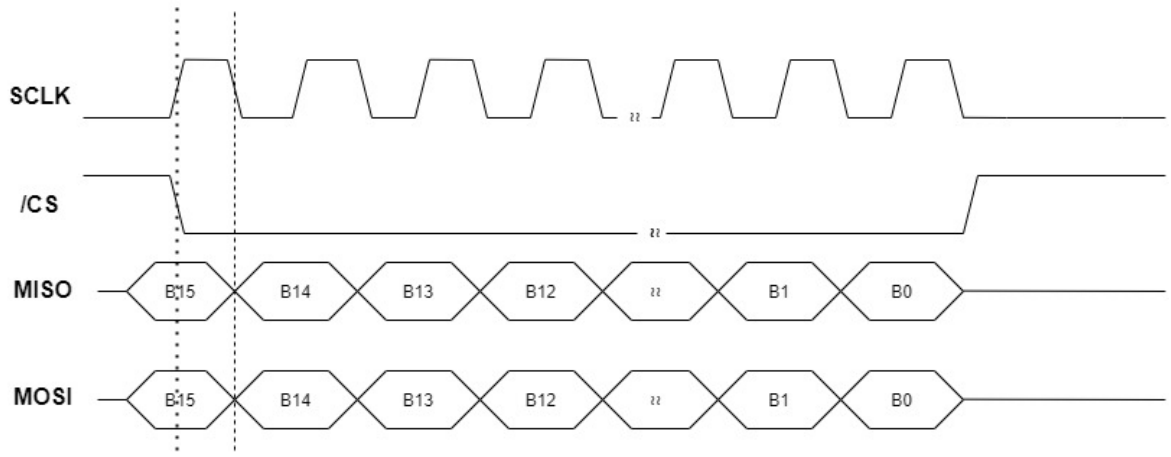


**Figure 3.19:** Typical SPI operation example

**Table 3.2:** SPI Operation Modes [52]

| Mode | CPOL | CPHA | Clock in Idle State | Clock Phase |
|---|---|---|---|---|
| 0 | 0 | 0 | Low | Data sampled on rising edge<br>Data toggled at the falling edge |
| 1 | 0 | 1 | Low | Data sampled on falling edge<br>Data toggled at the rising edge |
| 2 | 1 | 0 | High | Data sampled on falling edge<br>Data toggled at the rising edge |
| 3 | 1 | 1 | High | Data sampled on rising edge<br>Data toggled at the falling edge |

be in idle in the ”High” state, if CPOL is set to ”0” the clock will idle on the ”Low” level. The CPHA bit selects the clock phase. If CPHA is ”0” the sampling of the data will be made on the rising edge and the toggle data will be in the falling edge. On the other hand, if CPHA is ”1” the sampling will be on the falling edge of the clock and the toggle of data on the rising edge. The four operation modes (mode 0, 1, 2 and 3) and the influence of each signal is summarized on table 3.2 [52]. It is important to note that the master and the slave should have the same operation mode to be possible to establish correctly the information. If multiple slaves architecture is used and these slaves have different operation modes, the master is responsible to reconfigure itself before establishing communication [51].

CHAPTER 4

# Architecture

This chapter presents the general architecture and the circuits used on the implemented system. The approach on the design of each circuit is presented and the topology chosen for the various circuits implemented is explained.

In figure 4.1 a general architecture of the system is presented. The system is composed of a programmable current source, used to control the stimulating current amplitude, and a h-bridge to drive the load. The programmable current source requires a DAC that allows to set the desired current according to a binary word at its input. The topology chosen for the digital-to-analog converter was based on a binary-weighted with charge scaling architecture. Being the DAC output a voltage, a voltage to current converter is also necessary (part of the programmable current source), in order to convert the voltage to a proportional current with values varying in the range of the specifications. Additionally, it is a requirement for the binary word to be received from the control unit via SPI communication, so additional hardware to provide the interface for this protocol is required and is part of the system.

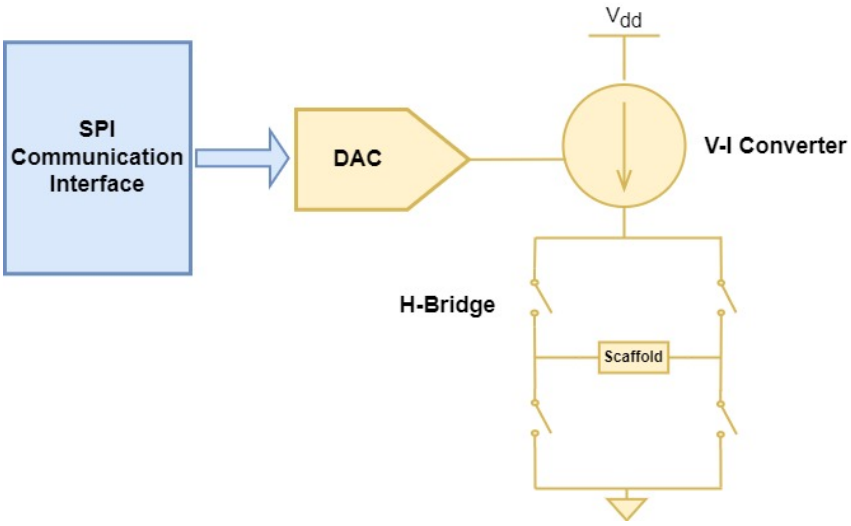


**Figure 4.1:** Stimulation system general architecture

As previously stated, the amplitude of the current applied through the scaffold is coded and sent to the system in a digital word. This word is received by the stimulation system and is converted into an analog signal using a digital-to-analog converter. The DAC should have the following main characteristics: rail-to-rail operation (operate between 0 and $V_{DD}$), high accuracy, fast conversion and low power consumption. Additionally, low area consumption is also an aspect that should be taken into consideration on the design.

The designed DAC was based on a charge scaling binary weighted topology, using the split array method with a resolution of 10 bits. Its schematic is presented on figure 4.2. The charge scaling architecture was chosen, because it is accurate and fast. Additionally, it has less power dissipation than the remmaining mentioned types of converters, since the power dissipation is mainly due to dynamic power consumption of the transistor switches required to apply the digital word at the input of the DAC. The main disadvantage of the charge scaling topology is the fact that it requires a large component spread and large sized capacitors for high resolution DACs. An example is that for a 10 bit DAC resolution it is needed, for the MSB, a capacitor with the value of 512*C, if C is the unit capacitor. This disadvantage can be diminished using the subranging technique. Dividing the 10 bit DAC into two 5 bit subDACs, the maximum capacitor value can be reduced to 16*C. To connect the LSB array with the MSB, a scaling capacitor (Cs) is used to scale the LSB array weight. At the output of the DAC, an operational amplifier in buffer configuration is included, to prevent load capacitive effects on the converter by the external circuits.

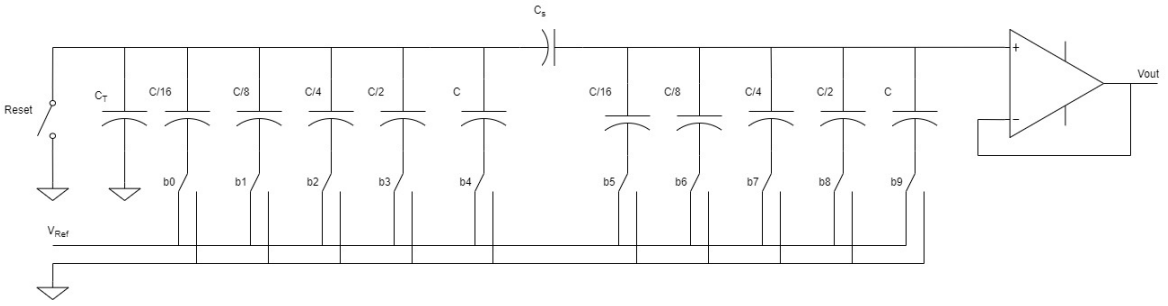


**Figure 4.2:** Implemented charge scaling split array DAC

### 4.1.1 Operation and Design

The electrical components that constitute the implemented DAC (figure 4.2) are capacitors with binary weighted values, an operation amplifier and switches. The switches are built with transmission gates and inverters, which are going to be presented in the following subsection.

The implemented DAC is composed by two 5 bit charge scaling subDACs, being the main DAC the one with the MSB capacitors array and where the output is taken. Additionally, the analog output needs to be properly scaled which is done using the scaling capacitor $C_s$. This capacitor is placed between the MSB and LSB arrays. Finally, a terminating capacitor $C_t$ is

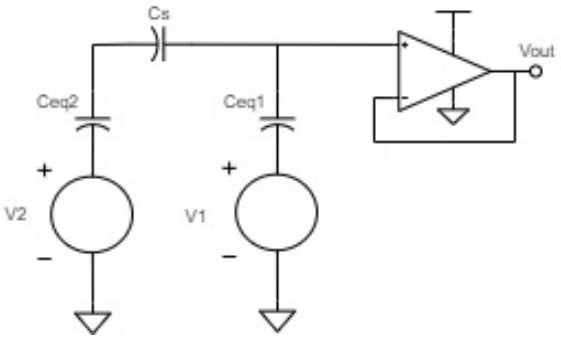


**Figure 4.3:** DAC Thevenin equivalent

included in the LSB array and has the same value of the unit capacitor ($C/16$), in order to make the LSB array equivalent capacitance 2C.

The $C_s$ can be calculated knowing that the combination in series of the LSB array with the scaling capacitor must serve has termination of the MSB array. Which means that the series of $C_s$ and the LSB array must be equal to the unit capacitor ($C/16$). This can be expressed by equation 4.1. Manipulating this expression it is obtained that Cs is equal to $2C/31$.

$$\frac{C}{16} = \frac{1}{\frac{1}{C_s} + \frac{1}{2C}} \tag{4.1}$$

The DAC expression can be obtained resorting to the DAC Thévenin equivalent presented on figure 4.3. In it, V1 and $C_{eq1}$ refer, respectively, to the equivalent voltage and capacitance of the MSB array and V2 and $C_{eq2}$ to the same metrics of the LSB array. For each array, the equivalent capacitance can be calculated by the parallel association of the capacitances in the array.

$$C_{eq1} = \frac{C}{16} + \frac{C}{8} + \frac{C}{4} + \frac{C}{2} + C = \frac{31}{16}C \tag{4.2}$$

$$C_{eq2} = \frac{C}{16} + \frac{C}{16} + \frac{C}{8} + \frac{C}{4} + \frac{C}{2} + C = 2C \tag{4.3}$$

Having obtained the equivalent voltages, V1 and V2 can be obtained and are expressed on expressions 4.4 and 4.5, respectively.

$$V_1 = \frac{C}{C_{eq1}}b0 + \frac{\frac{C}{2}}{C_{eq1}}b1 + \frac{\frac{C}{4}}{C_{eq1}}b2 + \frac{\frac{C}{8}}{C_{eq1}}b3 + \frac{\frac{C}{16}}{C_{eq1}}b4 = \frac{32}{30}\cdot\left(\frac{b0}{2} + \frac{b1}{4} + \frac{b2}{8} + \frac{b3}{16} + \frac{b4}{32}\right) \tag{4.4}$$

$$V_2 = \frac{C}{C_{eq2}}b5 + \frac{\frac{C}{2}}{C_{eq2}}b6 + \frac{\frac{C}{4}}{C_{eq2}}b7 + \frac{\frac{C}{8}}{C_{eq2}}b8 + \frac{\frac{C}{16}}{C_{eq2}}b9 = \left(\frac{b5}{2} + \frac{b6}{4} + \frac{b7}{8} + \frac{b8}{16} + \frac{b9}{32}\right) \tag{4.5}$$

Using the superposition principle and applying the voltage divider through the capacitors for V1 and V2 independently, the expression at the output can be given by equation 4.6 and simplified into 4.7.

$$V_{out} = \left( \frac{\frac{1}{2} + \frac{31}{2}}{\frac{1}{2} + \frac{31}{2} + \frac{16}{31}} \right) \cdot V_1 + \left( \frac{\frac{16}{31}}{\frac{1}{2} + \frac{31}{2} + \frac{16}{31}} \right) \cdot V_2 = \frac{30}{32} \cdot V_1 + \frac{1}{32} \cdot V_2 \tag{4.6}$$

$$V_{out} = \frac{b0}{2} + \frac{b1}{4} + \frac{b2}{8} + \frac{b3}{16} + \frac{b4}{32} + \frac{b5}{64} + \frac{b6}{128} + \frac{b7}{256} + \frac{b8}{512} + \frac{b9}{1024} \tag{4.7}$$

The value used for the unit capacitor was 400fF. The main factors for choosing the unit capacitor size are: area consumption and mismatch between the capacitors [33]. Small capacitors are usually desired since it decreases circuit area and increases the converter speed. However, the influence of mismatches between the capacitors are reduced, when the sizes of the capacitors are increased [40]. The choice of the unitary capacitor will be also discussed in chapter 6. In table 4.1 it is presented the values used for the capacitors.

**Table 4.1:** DAC Capacitor Values

| Capacitor | Value (fF) |
|---|---|
| C/16 | 400 |
| C/8 | 800 |
| C/4 | 1600 |
| C/2 | 3200 |
| C | 6400 |
| $C_T$ | 400 |
| $C_s$ | 412.9 |

### 4.1.2 Switch

As seen in figure 4.2, the DAC receives at its input digital bits. If a certain received bit has the logic value '1', the respective capacitor is switched to $V_{DD}$. If it is received the value '0', the correspondent capacitor is switched to ground. This behavior on the switches matches a 2x1 multiplexer operation. In CMOS, a 2x1 Multiplexer (MUX) can be implemented with the circuit presented on figure 4.4. The selection signal is represented by the "In" signal on the presented schematic, which can only assume the values of $V_{DD}$ or GND. If "In" is in the HIGH state, the MN1 and MP1 transistors will be active and the other two turn off and, at the output $V_{DD}$ will be presented. On the opposite side if "In" is in the LOW state, MP2 and MN2 will be the active transistors and GND will be presented at the output.

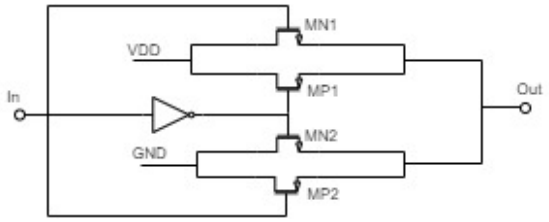


**Figure 4.4:** Implemented 2x1 multiplexer as DAC switch

### 4.1.3 Rail-to-Rail Operational Amplifier

The output of the DAC is buffered using an operational amplifier. Therefore, a rail-to-rail operational amplifier was designed, and it is presented on figure 4.5. The amplifier was designed taking in consideration the following main characteristics.

- Rail-to-rail operation at both the input and the output. This is an important feature for low voltage applications as the present one.
- High slew-rate. One of the main sources of delay for the DAC to provide the voltage at its output is the operational amplifier. In order for the conversion to be as fast as possible the slew-rate must be high.
- Low power dissipation, due to power constraints.

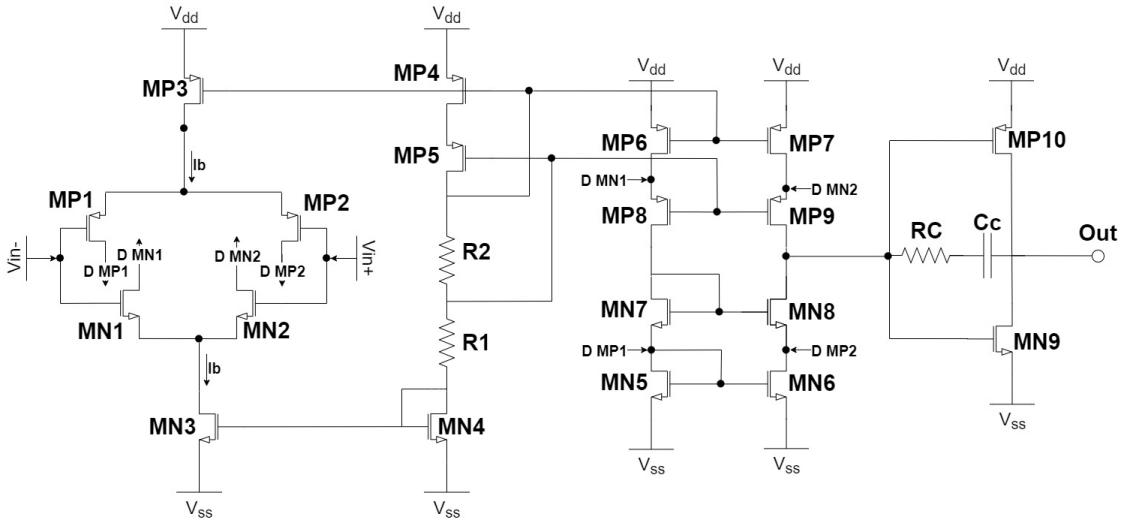


**Figure 4.5:** Implemented rail-to-rail opamp schematic

As for the topology, the designed amplifier is comprised on a parallel differential pair at the first stage (transistors MP1, MP2, MP3, MN1, MN2, MN3). Its objective is to achieve rail-to-rail operation at the input as desired. The transistors from the complementary differential pair should be small in size, to reduce their capacitance and consequently attenuate potential capacitive load effects on the DAC capacities. The second stage of the operational amplifier is based on a folded-cascode topology, which is composed of transistors MP6, MP7, MP8, MP9, MN5, MN6, MN7 and MN8. This configuration is used to sum the currents from the parallel complementary differential pair at the first stage. The folded-cascode configuration also provides an improved copy of the currents. Finally, the last stage is composed by a class

AB push-pull output stage (transistors MP10 and MN9). This last stage is used with the objective of achieving near rail-to-rail operation at the output. In addition, a RC network circuit was included between the last two stages in order to perform compensation on the stability, increasing the phase margin and avoiding oscillatory behaviour from the operational amplifier. Additionally, a loop to bias the three amplifier stages is also included, being the operational amplifier self biased (transistors MP4, MP5, MN4 and resistors R1 and R2).

The transistors dimensions are presented on table 4.2. On the compensation network, the $C_c$ capacitor has the value of 3pF and the $R_c$ resistor has the value of 2k$\Omega$.

**Table 4.2:** Opamp Transistors Dimensions

| Transistor | Width ($\mu$m) | Length ($\mu$m) |
|---|---|---|
| MP1, MP2 | 15 | 0.7 |
| MP3 | 150 | 0.7 |
| MN1, MN2 | 10 | 0.7 |
| MN3 | 12.7 | 0.7 |
| MP4, MP5, MP6, MP7, MP8, MP9 | 180 | 1 |
| MN5, MN6, MN7, MN8 | 150 | 1.4 |
| MP10 | 10 | 0.7 |
| MN9 | 5 | 0.7 |

To characterize the opamp, simulations on the Input Common Mode Range (ICMR), voltage gain, phase-margin, gain-bandwidth product, Common Mode Rejection Ratio (CMRR), slew-rate and power dissipation were performed. Corner analysis was also performed specifically for the typical operation (tm), worst power (wp) and worst speed (ws) corners. The results obtained are summarized in table 4.3. The frequency response of the designed rail-to-rail opamp, for the three considered operation corners, is presented in figure 4.6.

**Table 4.3:** Opamp Main Characteristics

| Parameter | tm | ws | wp |
|---|---|---|---|
| Offset Voltage | 46.4$\mu$V | 72.07$\mu$V | 4.73$\mu$V |
| Gain | 111.55dB | 114.47dB | 107.16dB |
| Phase-Margin | 59.55º | 46.6º | 63.17º |
| Gain-Bandwidth | 39.68MHz | 30.42MHz | 47.43MHz |
| Slew-Rate | 78.28v/$\mu$s | 63.05v/$\mu$s | 94.78v/$\mu$s |
| CMRR | 156.99dB | 164.47dB | 115.9dB |
| Power Dissipation | 6.25mW | 5.07mW | 7.9mW |

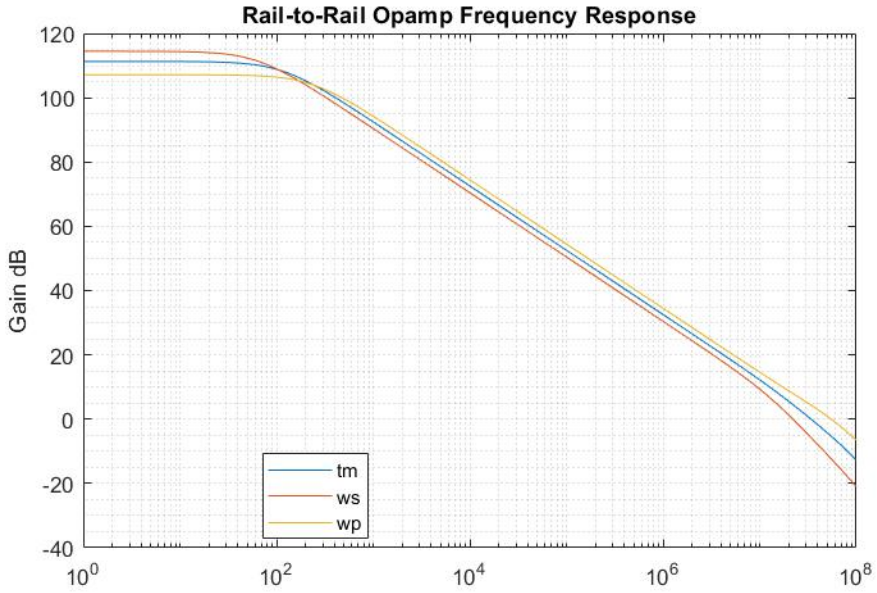


**Figure 4.6:** Rail-to-Rail Opamp Frequency Response

## 4.2 Voltage to Current Converter

To perform conversion from the voltage received from the DAC to a current directly proportional to the voltage presented at the the input a V-I converter is used. For the present application, the main aspects that should be taken into consideration are rail-to-rail operation, high linearity between the input voltage and the current produced at the output, and high output impedance since it acts as a current source for the h-bridge and the scaffold. Considering these specifications, the rail-to-rail voltage-to-current converters presented in section 3 are the ones that provide the best performance. The three rail-to-rail V-I converters considered in this section presented similar characteristics therefore, the one chosen to implement was the Feed Forward Voltage Attenuation, since it is simpler to implement.

The implemented V-I converter is presented in figure 4.7. This circuit is composed by a main enhanced V-I converter and a voltage attenuator. The principle of operation of this circuit is to attenuate the input voltage using the voltage divider (comprised by the transistor M1, the OTA and the resistors R1 and R2) by a factor $\alpha$ (expression 4.8), before applying this voltage to the input of the OTA common-source V-I converter at the second stage. Using negative feedback, this voltage is buffered to the resistor Rs responsible for the conversion to current. This way, it is possible to maintain the transistors M2, M3, M4 and M5 working in the saturation region for most of the input voltage signal excursion (0 to $V_{DD}$). The maximum signal excursion is limited by the voltage where transistor M1 enters the triode region, which can translate into a near rail-to-rail operation of the converter if this transistor size ratio is high enough.

$$\alpha = \frac{R_2}{R_2 + R_1} \tag{4.8}$$

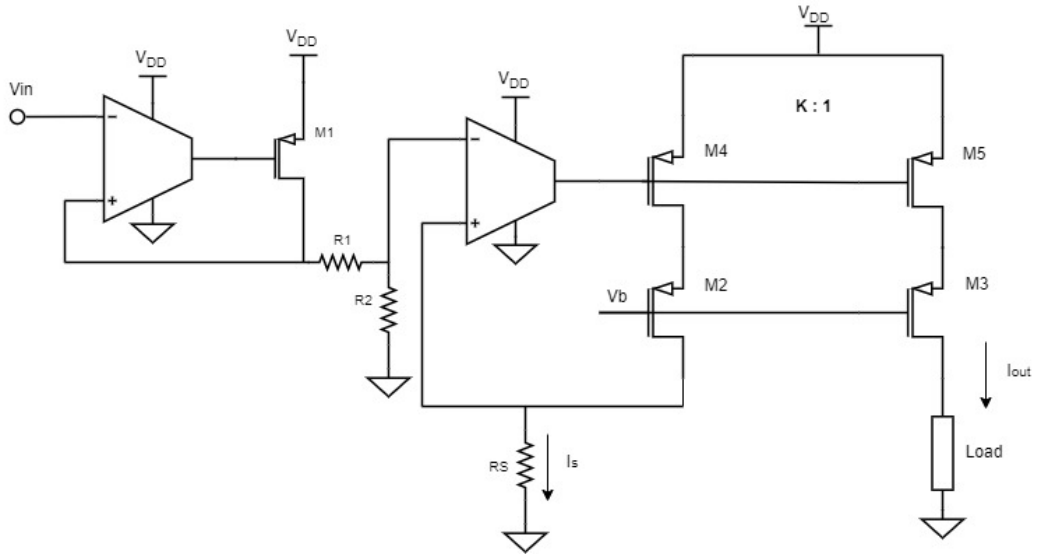


**Figure 4.7:** Implemented Voltage to Current converter

The current that was produced by the resistor Rs is copied through a current mirror, by a factor of K. A cascode current mirror is used in order to improve the current copy from the transistors M2 and M4 to the transistors M3 and M5.

As for the design followed in this work, the factor of attenuation ($\alpha$) used was 0.5. In addition, the current gain used on the current mirror (K) was 1, which makes the output current be given by expression 4.9

$$I_{out} = \frac{\alpha \cdot V_{in}}{K \cdot R_s} = \frac{V_{in}}{2 \cdot R_s} \tag{4.9}$$

The values for the transistors used are summarized on table 4.4. M1 has a high relation on the geometry ratio, to reduce the saturation $V_{ds}$ of this transistor. Additionally, it was used a length of 2.1$\mu$m for the cascode current mirror transistors to improve the current copy accuracy. For R1 and R2 it was used 1k$\Omega$ and Rs is external to the ASIC to be possible to adjust the stimulating current if needed. The implemented OTA will be presented in the following subsection.

**Table 4.4:** V-I Converter Transistors

| Transistor | Width ($\mu$m) | Length ($\mu$m) |
|---|---|---|
| M1 | 200 | 0.7 |
| M2 | 20 | 2.1 |
| M3 | 20 | 2.1 |
| M4 | 20 | 2.1 |
| M5 | 20 | 2.1 |

### 4.2.1 OTA

The operational transconductance amplifier (OTA) designed for the described V-I converter schematic is presented on figure 4.8. This amplifier topology is equivalent to the first two

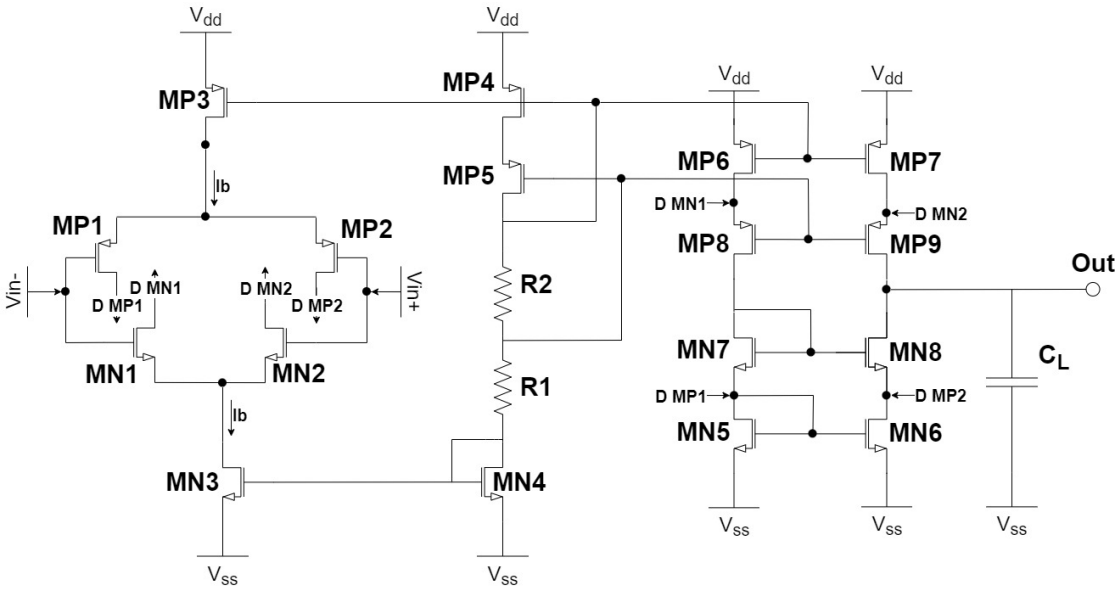


**Figure 4.8:** Implemented OTA schematic

stages of the previously described amplifier, these being: a parallel complementary differential pair at the first stage and a second stage with a folded-cascode topology to perform the current summation and mirroring from the first stage. Since, the design is mostly the same as for the operational amplifier previously designed, this section will not go to more detail. The main characteristics that were taken into consideration on the design process were, a high gain, near rail-to-rail operation at both the input and the output and a high slew-rate. Low power dissipation and low area consumption were also factors that were taken into consideration.

The OTA presents, at its output, the capacitor $C_L$. This capacitor purpose is to perform frequency compensation on the V-I converter, by limiting the OTA bandwidth. Without it, the current and the voltages on the converter have an oscillatory behaviour presenting high frequency components. This capacitor has the value of 5pF, and it was obtained by trial error, varying its value and analyzing the V-I converter output current curve.

The transistors dimensions are presented on table 4.5.

**Table 4.5:** OTA Transistors Dimensions

| Transistor | Width ($\mu$m) | Length ($\mu$m) |
|---|---|---|
| MP1, MP2 | 15 | 0.7 |
| MP3 | 60 | 0.7 |
| MN1, MN2 | 10 | 0.7 |
| MN3 | 12.7 | 0.7 |
| MP4, MP5, MP6, MP7, MP8, MP9 | 180 | 1 |
| MN5, MN6, MN7, MN8 | 150 | 1.4 |

As for the operational amplifier, simulations on the same parameters and with corner analysis was performed, being the main characteristics summarized in table 4.6. The frequency response of the designed OTA for the three considered operation corners is presented in figure

4.9.

**Table 4.6:** OTA Main Characteristics

| Parameter | tm | wp | ws |
|---|---|---|---|
| Offset Voltage | 19.28$\mu$V | 89.97$\mu$V | -18.97$\mu$V |
| Gain | 77.15dB | 75.13dB | 78.12dB |
| Phase-Margin | 85.3º | 84.87º | 87.74º |
| Gain-Bandwidth | 11.53MHz | 13.99MHz | 9.03MHz |
| Slew-Rate | 24.4v/$\mu$s | 21.01v/$\mu$s | 27.28v/$\mu$s |
| CMRR | 121.56dB | 119.6dB | 122dB |
| Dissipated Power | 3.84mW | 4.5mW | 3.36mW |

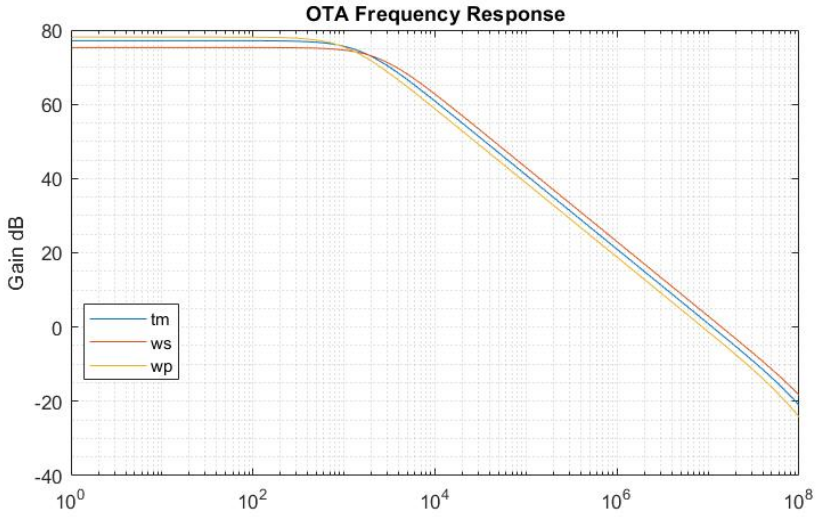


**Figure 4.9:** OTA Frequency Response

## 4.3 H-Bridge

To drive the current through the scaffold, an H-Bridge circuit was implemented and is presented in figure 4.10. This type of circuit was implemented since it provides the capability of controlling the direction of a Direct Current (DC) through the load. In addition, a circuit to drive the switches was also implemented.

Figures 4.11 present the possible operation modes for the H-Bridge circuit.

- The figure on the left demonstrates a positive current applied through the scaffold. This is done by closing simultaneously the switches S1 and S4, while maintaining S2 and S3 open.
- The picture on the middle shows the current applied on the opposite direction of the previous case (considered the negative direction). To apply the current on this direction the switches S2 and S3 must be closed simultaneously and S1 and S4 should be open.
- The figure on the right shows the case where no current is applied on the scaffold. For this all switches of the H-Bridge must be open.

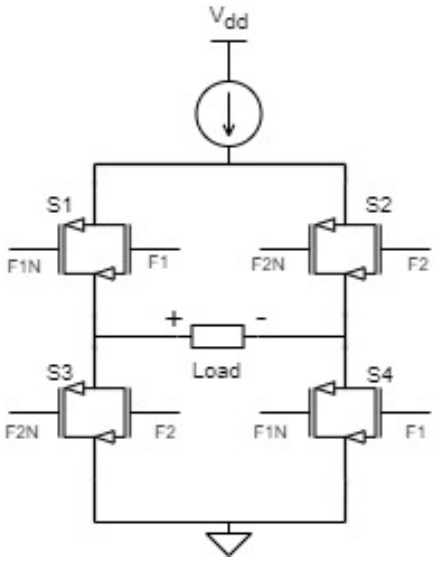


**Figure 4.10:** H-Bridge circuit schematic

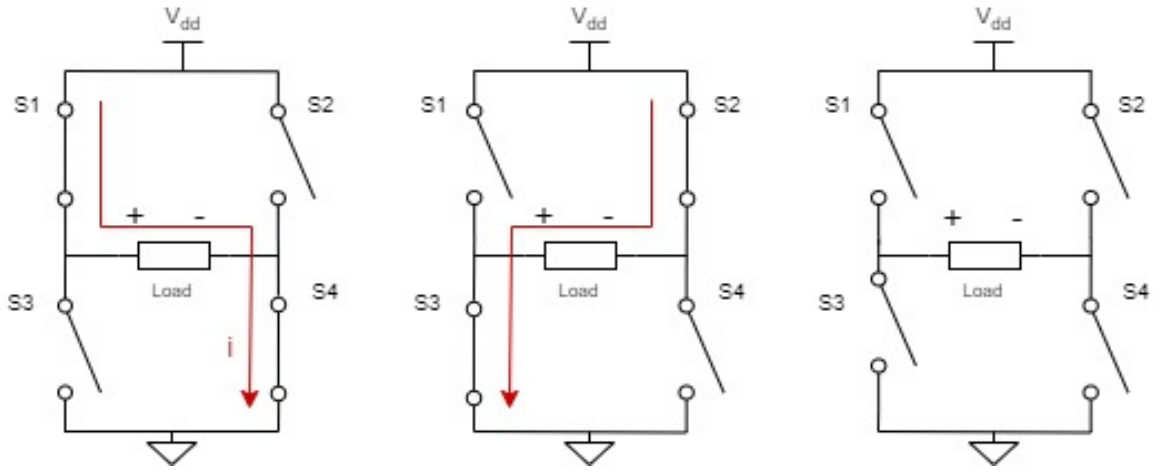


**Figure 4.11:** H-Bridge operation. Left figure shows a positive current through the load; middle figure a negative current; right picture no current is applied

The main aspects that were taken into consideration on the H-Bridge design were the switches and the control logic that drives the switches. The design of these units is going to be presented in the following subsections.

### 4.3.1 Switches

The main requirements on the switch design are: low resistance on the ”on” state and high switching speed, while maintaining low area consumption. On typical PMOS and NMOS, high speed on switching is achieved with the increase of the transistors' geometry ratio. The ”on” resistance parameter follow the same trend. If the transistors' size ratio are increase this parameter should decrease. However, to achieve negligible ”on” resistance the transistors should have a very high size ratio, which increases the area. Having this constraints in mind, the switches on the H-Bridge were implemented using transmission gates, since it provides

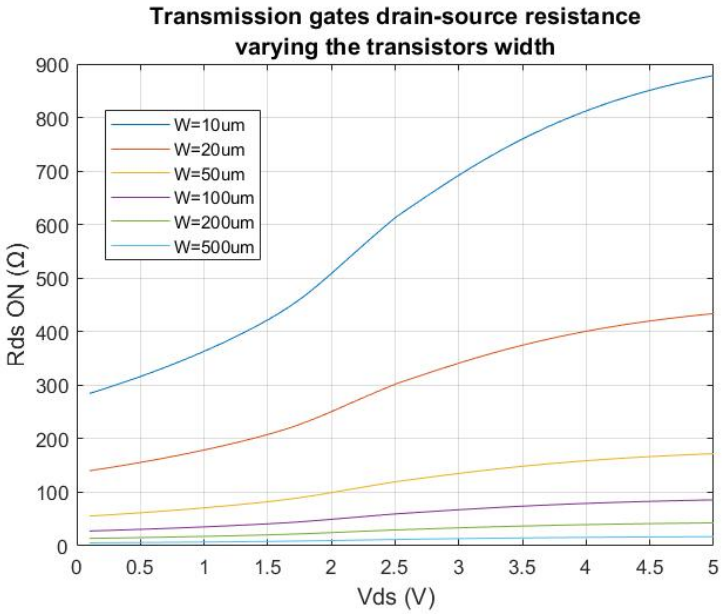


**Figure 4.12:** Transmission gate on resistance simulation

lower resistance when in conduction.

A simulation was made were the size ratios of the transistors on the transmission gate were varied and ”on” resistance was measured. The simulation results are presented on figure 4.12. This simulation shows that the higher the relation in the dimensions of the transmission gates, the lower the ”on” resistance. However, increasing the transistors sizes, has the drawback of increasing area and power consumption. Taking into account the performed simulation, the values of 50$\mu$m of width and 0.7$\mu$m of length were chosen as the best compromise in resistance, area consumption and power dissipation. With this value, the resistance is at maximum around 170Ω, which means that a maximum of around 34mV is lost in each transistor, if considering the maximum current from the specifications (200$\mu$A) flowing through the transistors. Note that during the performed simulation the width of the transistors was varied, but the length was maintained at 0.7$\mu$m.

### 4.3.2 Control Logic

A control logic to drive the switches that was implemented, is presented on figure 4.13 [13]. The control block is composed by simple logic gates (nands and inverters). It was implemented using the logic gates provided by the AMS digital libraries. For the operation of the implemented control block, two digital signals are required:

- Enable signal: digital signal responsible for enabling or disabling the current from the V-I converter. Logic level ’1’ enables the current and the level ’0’ disables it.
- Direction signal: it is responsible to determine the current through the load. Logic level ‘1’ corresponds to the considered positive direction of the current and logic level ‘0’ to the negative one.

In table 4.7, it is presented a summary of the influence of the ”Enable” and ”Direction” digital signals have on the switches and consequently on the current applied.

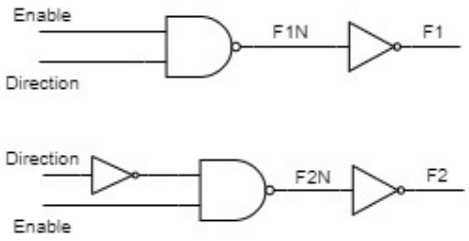


**Figure 4.13:** H-Bridge control logic

Besides determining the operation of the H-Bridge, the control logic also has the objective of guaranteeing that both pairs of opposite switches are never active at the same time. This is achieved using the ”Direction” signal which is responsible for driving the opposite pair of transistors with complementary signals. The ”Enable” and ”Direction” are inputs of the system and are external pins of the ASIC.

**Table 4.7:** H-Bridge control logic truth table

| Enable | Direction | S1 | S2 | S3 | S4 | State |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | OFF |
| 0 | 1 | 0 | 0 | 0 | 0 | OFF |
| 1 | 0 | 0 | 1 | 1 | 0 | Negative |
| 1 | 1 | 1 | 0 | 0 | 1 | Positive |

## 4.4 SPI Communication Interface

As it is expressed in the system specifications, the communication between the microcontroller and the stimulation system present in the ASIC should be performed using the Serial Peripheral Communication protocol. The stimulation system acts as a slave and the control unit a master, and the communication is performed only from the control unit to the stimulation system. This means that the stimulation system only receives information. To support this communication protocol, additional hardware in the ASIC is required to provide the necessary interface. This interface is responsible for receiving the serial bit stream from the control unit, convert the serial information into parallel and feed the parallel digital word into the DAC. Furthermore, it is required additional logic to provide the word to the DAC, only when the digital bit stream is sent correctly and reset the interface when the communication is not completed correctly.

The circuit developed to provide interface to the SPI protocol is present on figure 4.14. As it can be seen in the figure, the interface is composed by a 16 bit serial input parallel output shift register, a 16 bit parallel input parallel output register (data register), 4 bit up-counter and additional logic gates (one inverter and one nand). These circuits were implemented using the components present in the AMS digital libraries and their implementation will be discussed in the following subsections. The clock frequency considered during the development

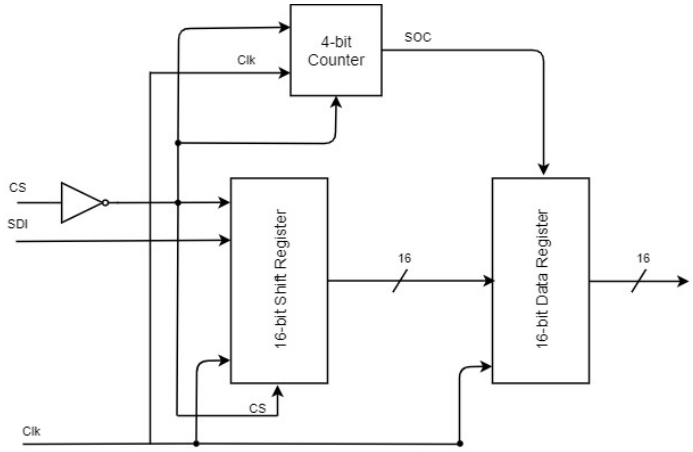


**Figure 4.14:** SPI interface schematic

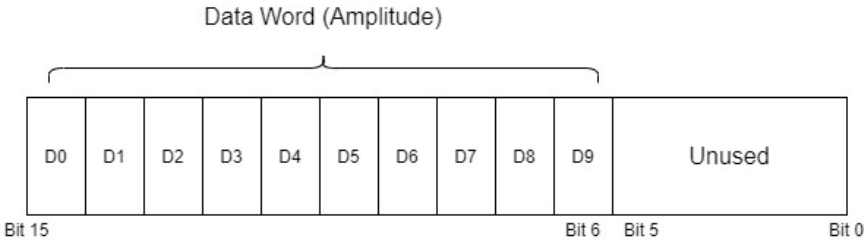


**Figure 4.15:** Bit stream

of this work was 20MHz, since it is a commonly used frequency of operation for current micro controllers.

The bit stream sent by the microcontroller is presented in figure 4.15. The bit stream is a 16 bit digital word where the 6 LSB (bit 5 to 0) are unused and the 10 MSB (bit 15 to 6) are the digital word that encodes the amplitude to be sent to the scaffold (called ”data word”). Additionally, it is important to understand that the word received on the DAC follows the received word from the data word. This means that the MSB of the data word (D0) is also the most significant bit on the DAC and the LSB of the data word (D9) is the LSB of the DAC. It is considered that the word is sent from the LSB to the MSB. A bit stream of 16 bit is used, since for typical microcontrollers the data is usually sent packages of 1 byte. Therefore, to send 10 bits of information, a package of 16 bits is required.

### 4.4.1 Interface Operation

In figure 4.16 it is presented a simplified state diagram that describes the interface operation. The communication starts when the chip select signal (CS) is activated (active-low signal). When this event occurs, the bit stream is received, by the stimulation system, one bit per clock pulse rising edge. The information is sent by the MOSI of the micro controller and received by the SDI pin on the stimulation system. The bits sent are stored on the shift register. Simultaneously, the 4-bit up-counter is enabled. When 16 clock cycles have occurred, the digital bit stream is fully transmitted and the start of conversion signal (SOC), that is ’1’ when the counter reaches ”1111” at its output, is activated. This signal enables the data

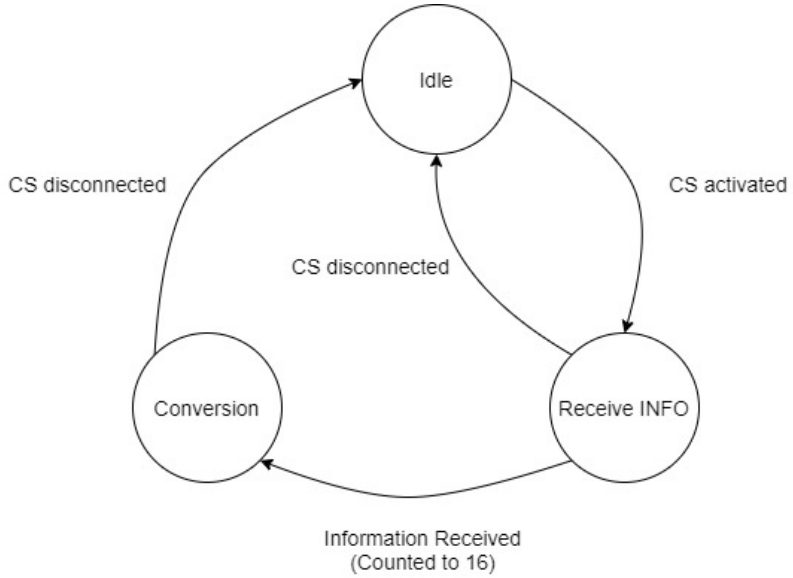


**Figure 4.16:** SPI state diagram

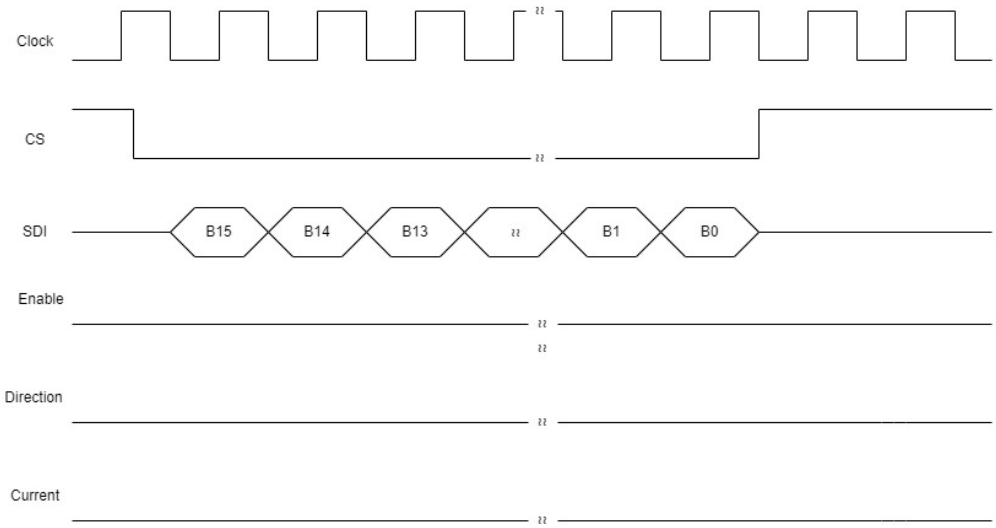


**Figure 4.17:** Turn off system protocol

register, and the word present in the shift register is stored and presented to the DAC, which starts the conversion. After the 16 clock cycles, the chip select signal must be set to ”off”. When this is done, the counter and the shift register are reset. If the CS signal is pulled high before the 16 clock cycles are completed (and therefore the communication is not completed properly), the interface is also reset.

On figures 4.17, 4.18 and 4.19 temporal diagrams that represent use cases on the communication protocol and system usage are presented. On the first case, it is demonstrated how to turn off the current applied to a scaffold. For that, the ”Enable” signal should be put to the logic value ’0’, which deactivates the current through the scaffold. Then, the word ”000000000” should be sent through SPI to guarantee the data register reset.

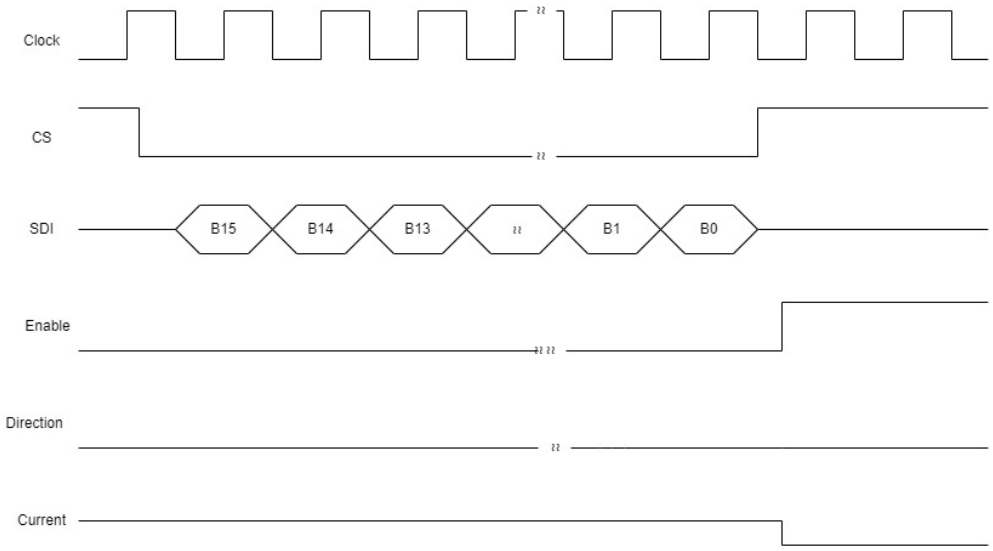


**Figure 4.18:** Apply current on the negative direction

The second use case presented (from figure 4.18), refers to the process to apply a current through the scaffold. In this case, it is demonstrated the application of a current on the negative direction. Firstly, the word is sent via the implemented SPI interface, with the same process previously explained. After the communication process is done and the DAC finished the conversion, the user must choose the current direction desired with the "Direction" signal. In the use case, it is desired for the current to flow on the negative direction, therefore this signal is '0'. After defining the direction, the current through the scaffold should be enabled, activating the "Enable" signal. Note that to apply a current on the considered positive direction, the operation would be similar, only the "Direction" signal should have the logic value '1' when the current source is enabled.

Finally, in the last presented use case (figure 4.19) it is represented the process of having applied a certain current, apply a different current on the opposite direction. On this use case, first it is sent a current on the positive direction using the same process previously explained. Then, if the user desires to apply a different current in the opposite direction, it should deactivate the current on the load and send via SPI the desired current to apply. During this process if the current source is disabled, the user can change the "Direction" signal. When the communication process is done and the DAC conversion time has passed, the user must switch the "Enable" signal to '1' once again, the current is activated and the process is finished. Note that, if it is desired to switch the current direction and maintain the applied current, the user should disable the "Enable" signal, change the "Direction" signal and, after this, activate once again the "Enable" signal. Therefore, there is no need for the microcontroller to transmit the correspondent digital word once again.

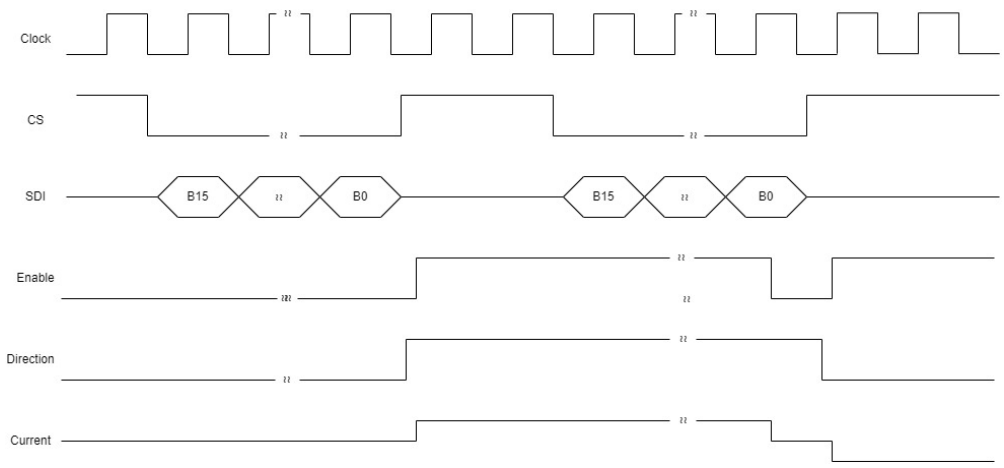


**Figure 4.19:** Transition between a positive to a negative current example

### 4.4.2 16 bit Shift Register

The implemented serial-input parallel-output 16 bit shift register is presented in figure 4.20. As previously mentioned, it receives one bit at a time through a single serial data line (from the microcontroller) and provides, at its output, the data in parallel.

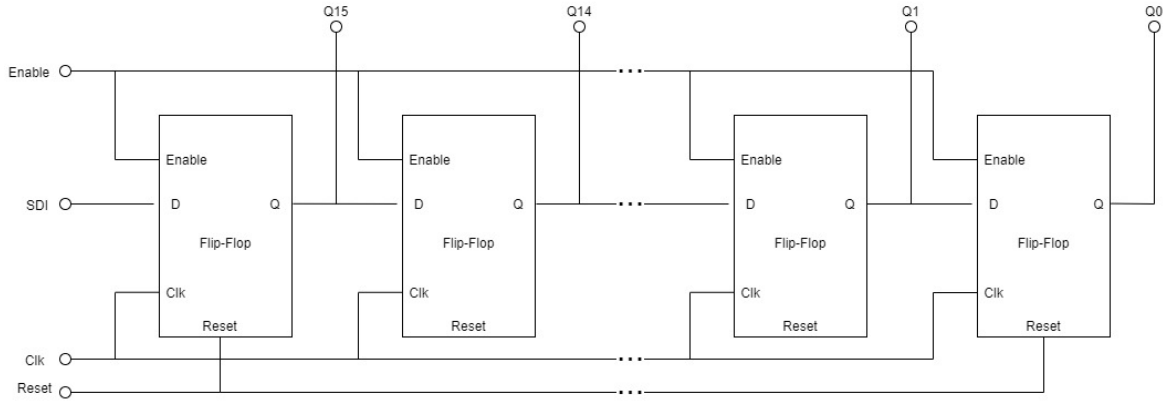


**Figure 4.20:** Implemented 16 bit shift register

The shift register is comprised of 16 type D flip flops with synchronous input data enable and data clear signals. For these flip flops it was resorted to the digital components from the AMS libraries, DFCX6_V5_3B, D flip flop with clear input. Important to notice that for these, the clear input is "active-low". Since, D flip flops with synchronous enable were not included in these libraries, for the enable functionality a 2x1 mux (MUX2X6_V5_3B) was added as it is shown in figure 4.21. If the enable is active, the input of the flip flop will be D (the signal presented at the input), if not the input of the flip flop will follow the output. In the designed SPI interface, the "Enable" and "Reset" signals are both connected to the chip select signal.

The main aspect taken into consideration when choosing the components from the digital cells was speed, since when considering a clock frequency of 20MHz, these components must

be fast to respond. So, it was used the flip flops with the largest size ratio on the libraries. As consequence, this implies a higher dynamic power consumption and area occupation.

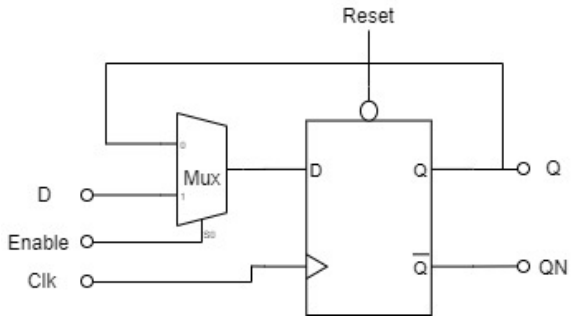


**Figure 4.21:** Implemented synchronous flip flop with enable input

*Simulation*

A simulation to verify the operation of the implemented shift register was performed in Cadence. The simulation results are in figure 4.22. The clock signal applied has a period of 50ns (frequency of 20MHz) and the rising and falling times of the control signals (clock and clear) were 1ns. The enable signal was maintained active throughout the simulation. A pulse of 10ns was presented at the data input (Input Data Signal) at the first clock rising edge. In the presented results it is possible to see that the data signal is correctly shifted through the various flip flops that implement this component. It is only presented the 10 MSB flip flop output, since these are responsible for storing the current amplitude word. It is also possible to verify the correct operation of the ”reset” signal. This signal is active in the Low state.

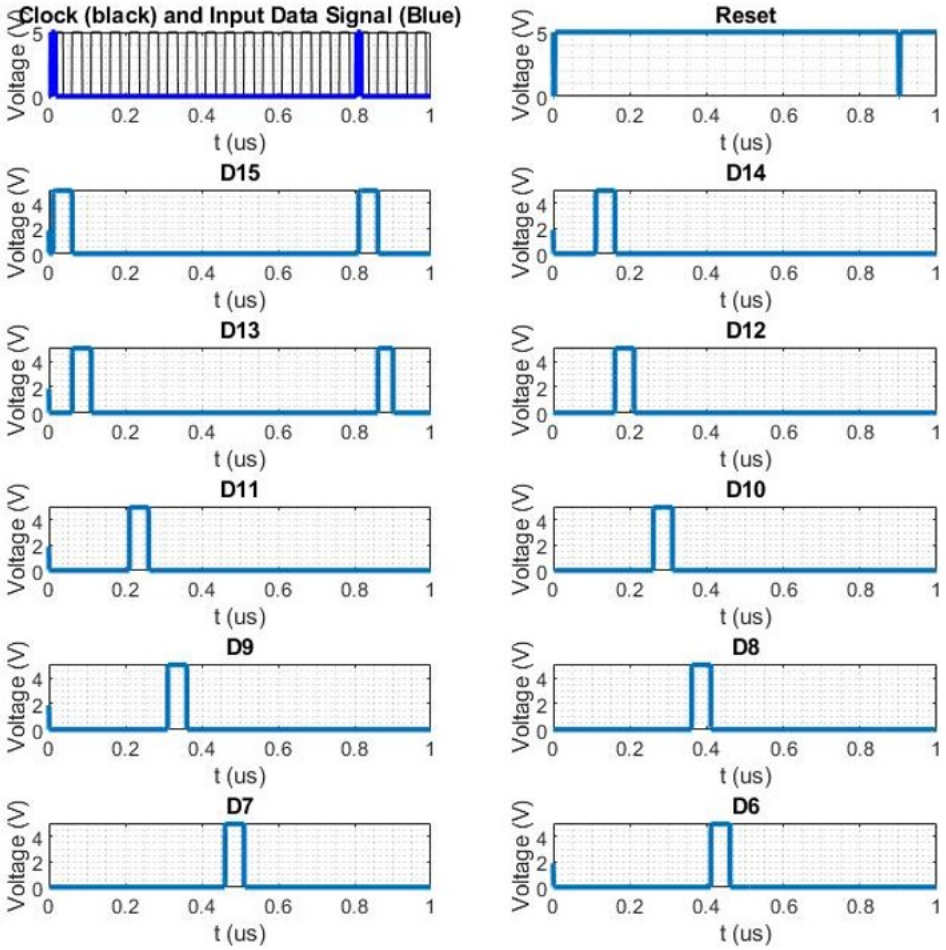


**Figure 4.22:** Shift Register Operation Test

### 4.4.3 Data Register

The data register is a 16-bit parallel-input parallel-output register, which is the unit responsible for receiving and storing the information provided by the shift register and present it to the DAC for conversion. The schematic for the implemented data register is presented in figure 4.23. The ”Enable” signal is responsible for activating the inputs of the flip flops and store the data present in the shift register. It was used the same digital libraries for the flip flop, only this time, the flip flop used was the DFX6_V5_3B, which did not include the clear input since it is not needed for this component. The same technique of using the 2x1 mux to provide the synchronous enable was again used. The components chosen from the libraries were once again the fastest ones (with higher transistors' size relation) to be fast to respond to the 20MHz signals, having the same type of constraints in power and area consumption.

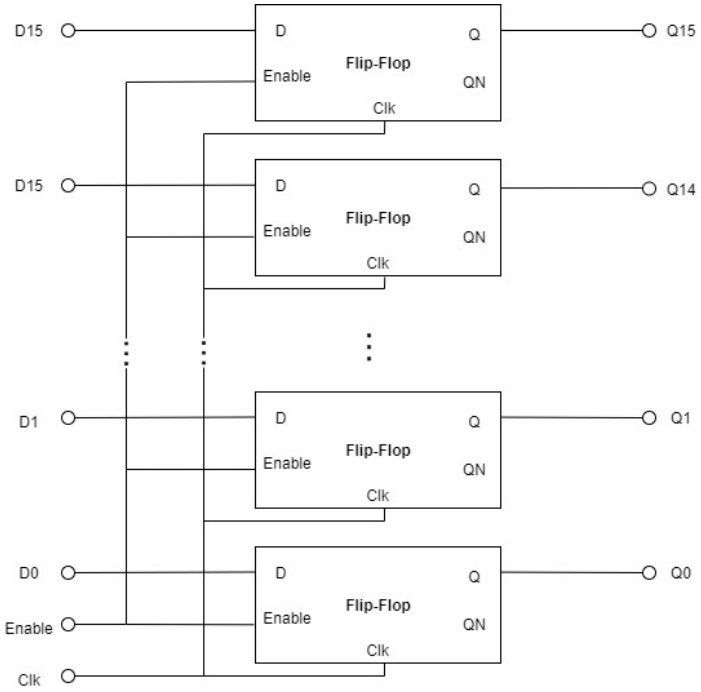


**Figure 4.23:** Implemented 16 bit register

*Simulation*

The data register operation test is presented in figure 4.24. The clock signal period, rising and falling times used were 1ns, the same for the shift register test. It was applied to the parallel inputs of the data register the binary word ”1010101010101010” and after 850ns the enable signal was activated. As it can be seen from figure 4.24, at 850ns the data word is provided to the output of the register correctly. Additionally, only the 10 MSB outputs were plotted, similar with the shift register test.

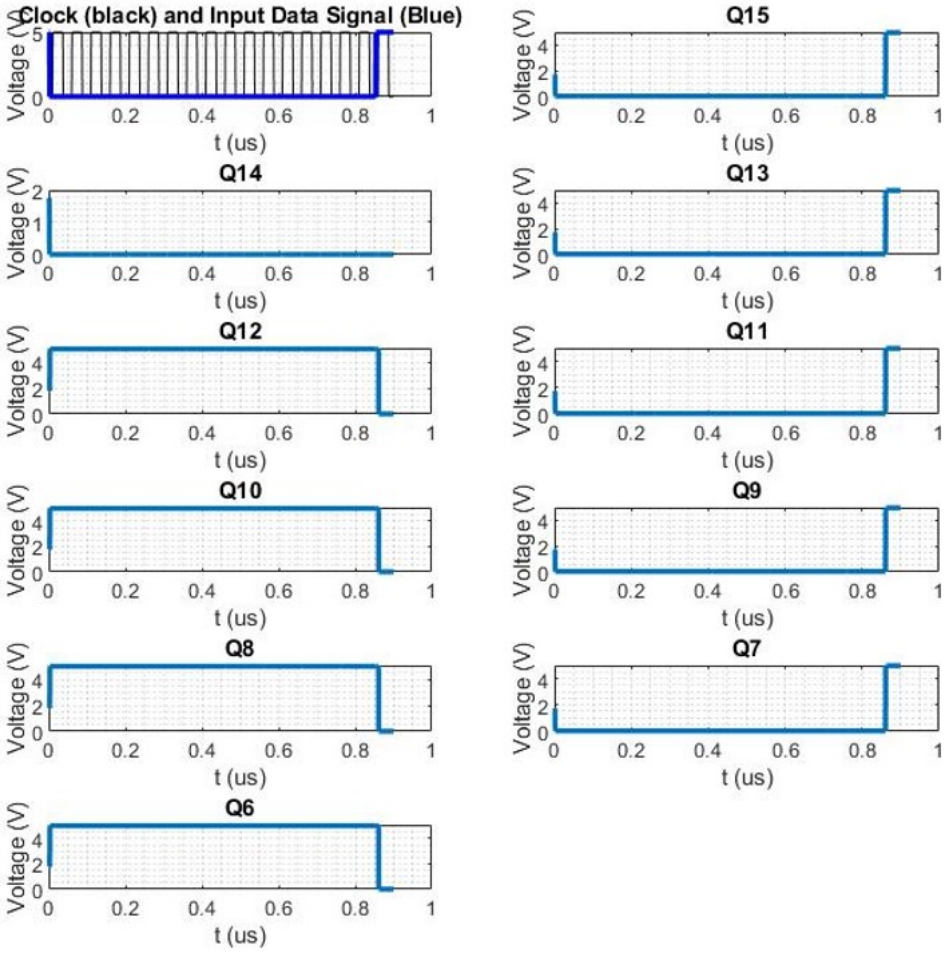


**Figure 4.24:** Data Register Operation Test

### 4.4.4 Counter

The implemented 4-bit up counter is presented on figure 4.25. It is composed of 4 D type flip flops with a signal to reset the flip flops value, 4 nand and 4 xor logic gates. The ”Enable” input, when activated, starts the up counting and the logic circuit composed by the 4 nand and 4 xor gates guarantee that a binary count is presented at the output. When the ”reset” signal is activated (it activates with the logic value ’0’), the flip flops are cleared and the count is restarted. In the SPI interface designed, these signals are both connected to the chip select. Additionally, another 4x1 nand gate and an inverter were used. The 4 input of the 4x1 nand gate are connected to the outputs of the 4 flip flops. The output of this added logic circuit is only activated when flip flops present the value ’1’ at their output. That is, when the count to 16 is finished the start of conversion signal (SOC) is activated enabling the data register. All the components used were from the AMS digital libraries. The components were chosen having in consideration similar characteristics as for the previous digital components design.

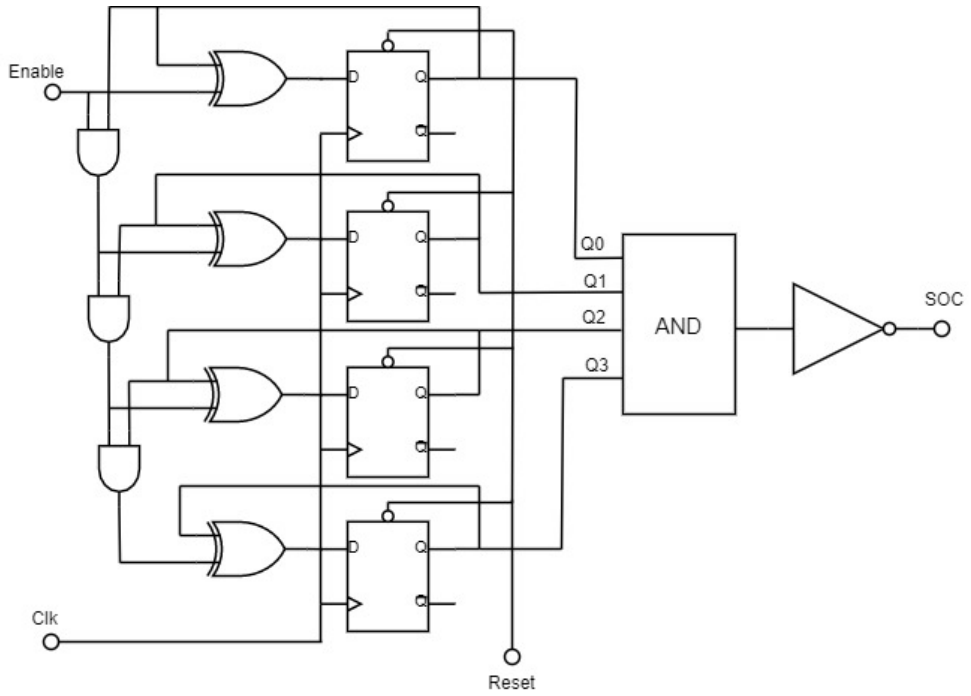


**Figure 4.25:** Implemented 4 bit up-counter

*Simulation*

A test on the implemented counter was also performed to verify its operation. The simulation results are presented in figure 4.26. The clock signal period, rising and falling times were the same as the simulations for the data and shift registers. The enable signal was maintained active throughout the simulation. From the simulation results, it is possible to see that the counter operation is demonstrated for the 20MHz operation frequency, in particular, the start of conversion signal is active when the count reaches ”1111” as expected and the clear signal resets the count properly.

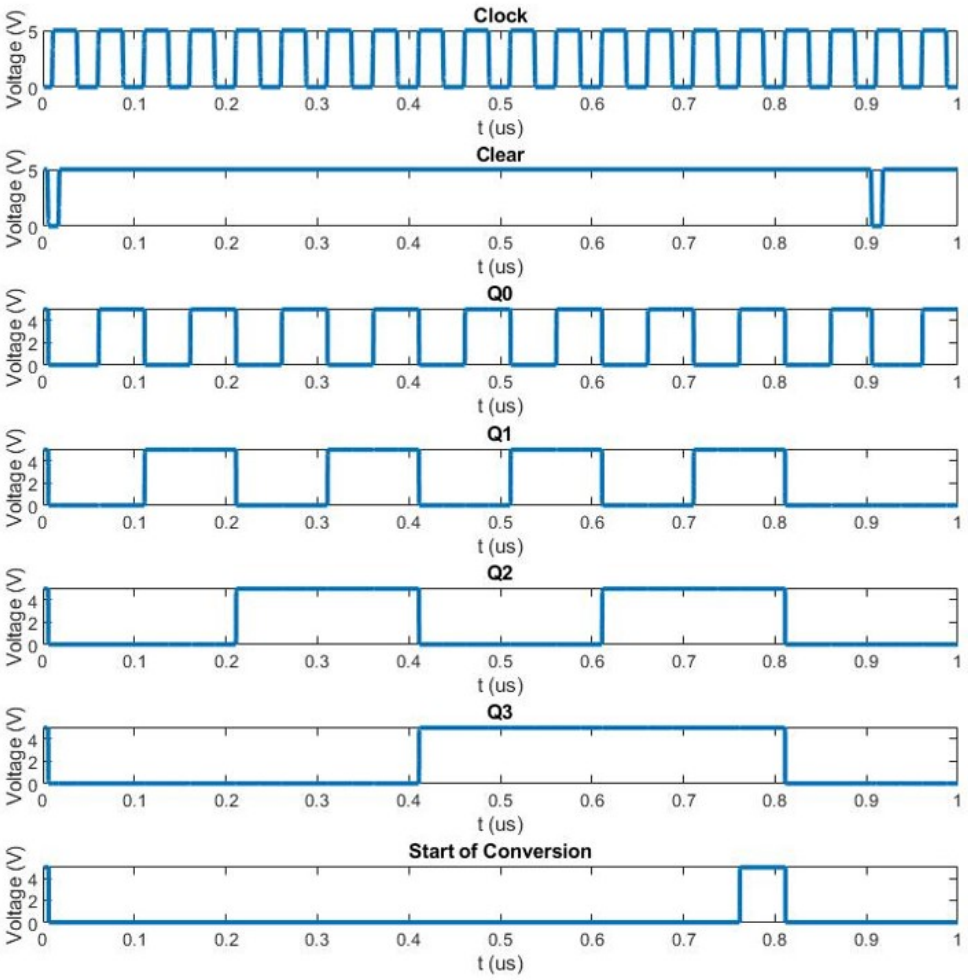


**Figure 4.26:** Counter Test

CHAPTER 5

# Simulation Results

The present chapter aims to report the simulation of the circuits implemented and present the main results. Simulations on the complete integrated system are also presented in order to evaluate if the system complies with the specifications.

## 5.1 DAC

The DAC converter was tested by applying at the input the combination of all digital values (1024 values since it is a 10-bit DAC). Since DAC receives at the input 10 digital signals, one for each of the 10 bits, a down counter emulating the ramp signal was used. The counter was implemented using ideal pulse wave sources. For the LSB, a signal with a period of $2\mu$s was used. For the remaining bits, the period of the signals applied was $2^{N-1}$ times the period of the LSB, where N is the bit to be generated. The rising and falling times of the signals used were 1ns. The test setup is represented on figure 5.1.

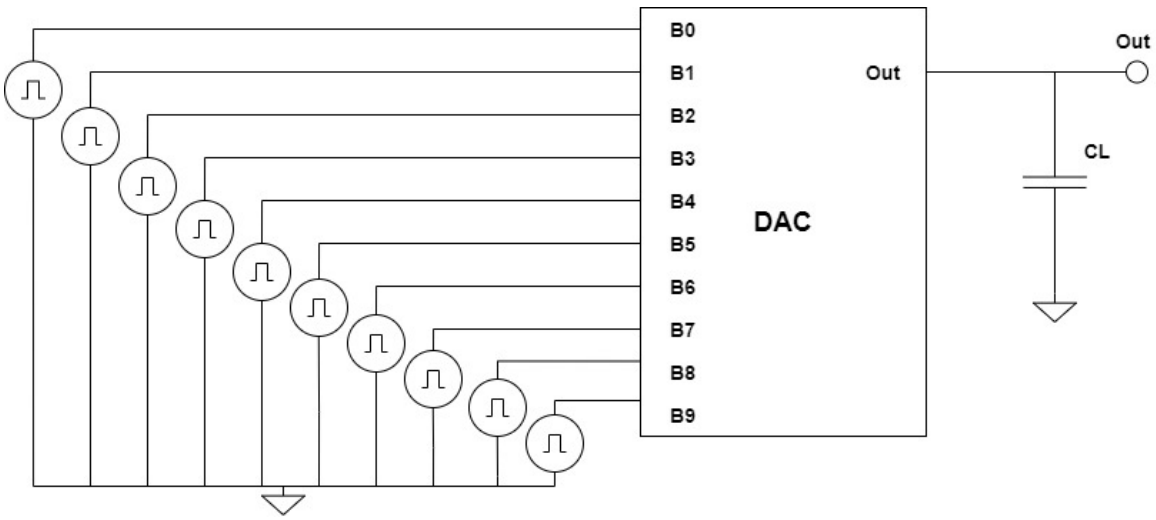


**Figure 5.1:** DAC Test Setup

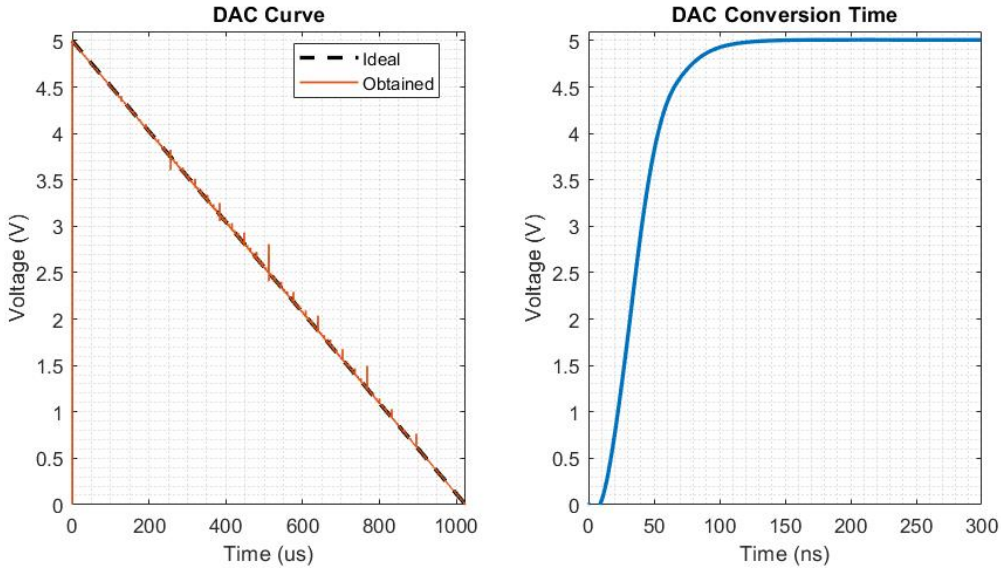


**Figure 5.2:** a - DAC Curve, b - Time the DAC takes to Stabilize the Output

Applying a ramp signal at the input of the DAC, the voltage transfer function curve was obtained, being presented on figure 5.2a. In the same plot, it is deceit the ideal transfer function for comparison purposes. Analysing the curve, on the first step of the simulation, the DAC transfer function does not start directly on 5V. This happens, due to the fact that the DAC has a delay on providing the converted voltage, at the output. The obtained transfer function is also used for the static characterization of the converter, which will be later presented.

The measurement of the DAC conversion time is presented in figure 5.2b. It was measured by applying, at the input, the correspondent word to 0 (”0000000000”) and, then, change it to the word correspondent to 5V (”1111111111”). The transition from 0 to 5V was used, since it is the highest output swing, and therefore, the transition that takes more time to be provided at the output. Analysing this curve, it is possible to see that the DAC output is fully stabilized around 200ns. The causes for the delay on the conversion time of the DAC are, mainly, the operational amplifier slew-rate limitation and the capacitors charging time.

In addition, the voltage value for each bit was measured. The measurements were made by activating a voltage pulse of each bit at a time, and measure the voltage at the output of the DAC. In table 5.1, the results for these measurements are presented as well as the ideal values of each bit.

Furthermore, the DAC was characterized on its static performance. This includes the DNL, INL and offset error. Results are presented in figure 5.3. These parameters were calculated from the curve obtained in figure 5.2 and MATLAB computations. For most codes, the obtained DNL (figure 5.3a) is around 0.03 LSB. However, it peaks at around -0.93 every 32 codes, when high transitions at the input of the DAC occur, for example when the input goes from ”0000011111” to ”0000100000” (code 31 to 32). Since the DNL is between -1 and 1, the DAC is monotonous and has no missing codes. In figure 5.3b, the obtained INL for the DAC

**Table 5.1:** Voltage Values for each Bit

| bit | Ideal Value (V) | Schematic (V) |
|---|---|---|
| B0 (MSB) | 2.5 | 2.497 |
| B1 | 1.25 | 1.248 |
| B2 | 625m | 624.16m |
| B3 | 312.5m | 312.08m |
| B4 | 156.25m | 156.13m |
| B5 | 78.125m | 80.1m |
| B6 | 39.0635m | 39.58m |
| B7 | 19.53m | 18.85m |
| B8 | 9.766m | 9.87m |
| B9 (LSB) | 4.883m | 4.79m |

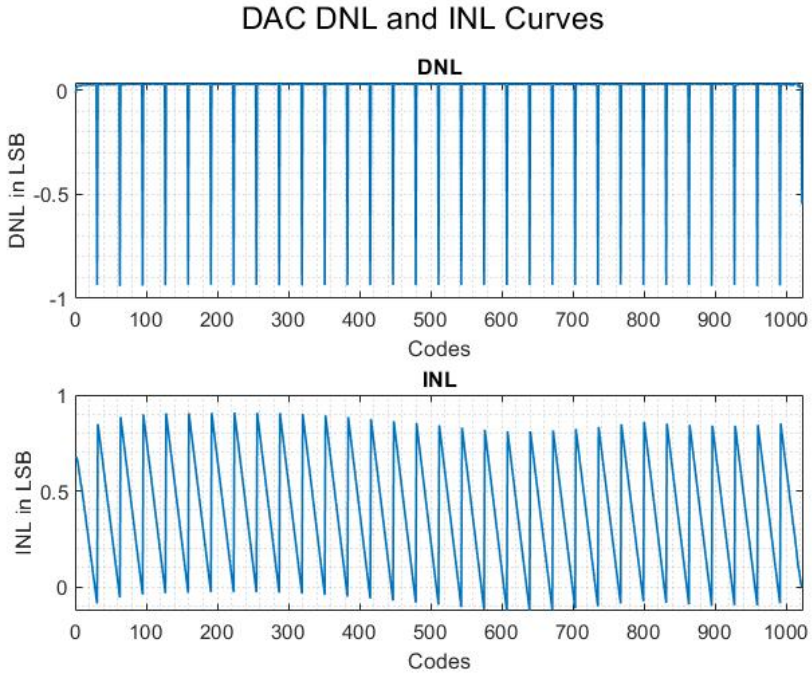


**Figure 5.3:** a - DAC DNL, b - DAC INL

is presented. It varies from around -0.087 LSB to 0.9 LSB. Observing the obtained curve, the peaks in the INL value occur on the same code interval as the DNL. The obtained INL results mean that the accuracy of the output varies between -0.087 LSB and 0.9 LSB. Finally, the DAC offset was also calculated. For that, the output voltage value for the first code (that ideally should be 0) is measured, having been obtained a voltage offset of 1.11mV.

## 5.2 V-I Converter

For the voltage-to-current converter, the main tests performed were: the input common mode range (ICMR), load dependence and the obtained current curve when applied at the input the voltage equivalent to the 1024 different codes from the DAC.

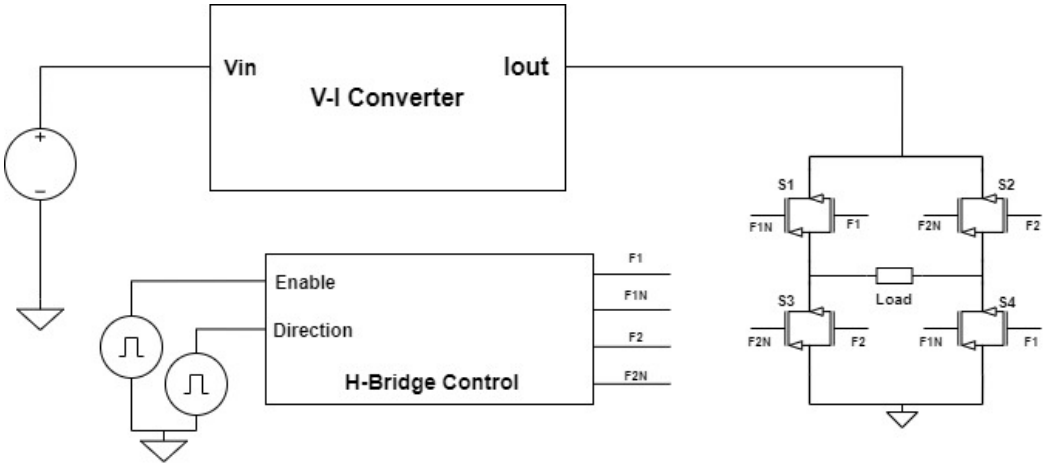


**Figure 5.4:** V-I Converter Test Setup

The first test setup used is presented on figure 5.4. It is based on the designed current source and the H-Bridge circuit at the output. For the simulations performed, the h-bridge was maintained operating with the same current flow direction (same pair of opposite transistor conducting). With this setup, the tests on the ICMR were performed.

In the first test performed, a DC voltage source was applied at the input, with the DC voltage being varied from 0 to 5V, and the current at the load was measured. The curve obtained is presented in figure 5.5. It can be seen that the V-I converter output current curve stops being linear when the voltage applied at the input is higher than 4.86V. Therefore, the compliance voltage of the converter is from 0 to 4.86V. To support this information, the derivative of the ICMR curve is also plotted in figure 5.5. The derivative presents the linearity achieved by the V-I converter and it can be seen that from 0 to 4.86V the derivative is almost constant, therefore the V-I converter achieves good linearity. For voltages higher than 4.86V of the input voltage, the derivative decays exponentially and therefore the linearity is lost.

This simulation gives information on two important aspects. The first is on the $R_s$ resistor value. Since, the maximum compliance voltage is of 4.86V, for achieving a certain current range this resistor should be scaled for 4.86V. Therefore, to achieve a current range from 0 to 200$\mu$A as presented on the specifications, the resistor value is given by 5.1, expression that was derived from equation 4.9. The second information given by this simulation is that, being the linear range between 0 and 4.86V, the voltages applied at the input should be in this range. Therefore, the digital words applied at the input of the system should be equivalent to this voltage range. As consequence, the highest 29 steps are lost. This implies a reduction on the resolution, however a resolution of $200\mu A/(1024-29) = 0.2\mu A$ can still be achieved, fulfilling the specifications.

$$R_s = \frac{V_{in}}{2 \cdot I_{max}} = 12150\Omega \tag{5.1}$$

The second set of tests performed on the V-I converter were performed using the test setup on figure 5.6. This test setup is similar to the one used in figure 5.4. However, instead of using the DC voltage source at the input, the DAC with the down counter was used. With this

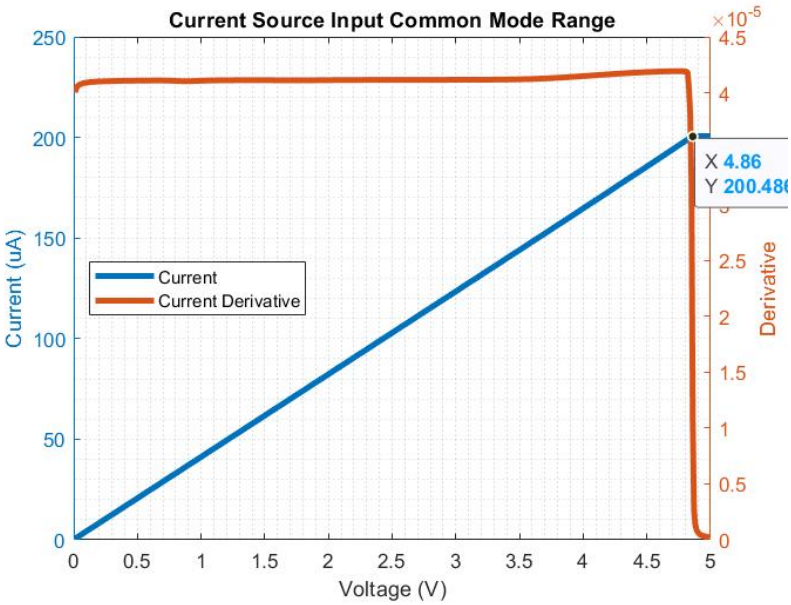


**Figure 5.5:** V-I Converter Operating Voltage

setup the current curve at the output, for a 10kΩ for the 1024 possible different input codes was obtained. In addition, the same setup was used to study the output current dependence with the load value.

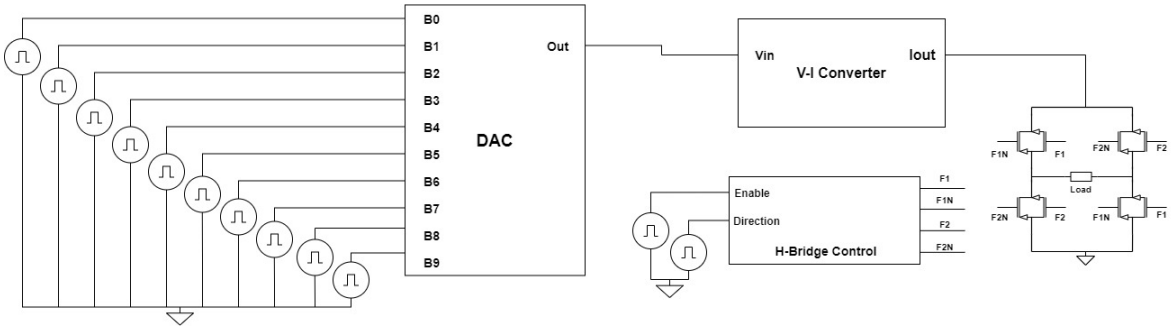


**Figure 5.6:** V-I Converter Test Setup with DAC

The equivalent voltage to the 1024 different digital steps, generated by the designed DAC, was applied at the input of the V-I converter and the current was measured on a 10kΩ load. Curves for the current when it flows on both directions of the load were recorded and the results are presented in figure 5.7. The error between the obtained current and the ideal one will be presented when simulations to the entire system are presented. However, from 5.7, it can be seen that the current presents a linear relation with the digital codes at the input. Furthermore, at the last 29 steps of the simulation, the current loses the linear characteristics, due to the V-I converter input voltage range limitations.

The simulations results performed on the current dependence on the load at the output is presented on figure 5.8. To obtained these results, the output load was varied with 6 different values (100Ω,1kΩ, 10kΩ, 15kΩ, 20kΩ, 50kΩ and 100kΩ) and the current was measured. From

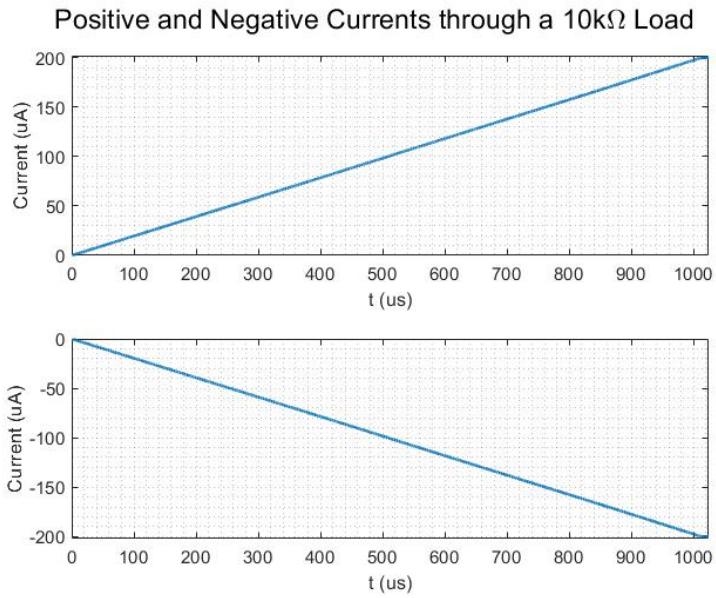


**Figure 5.7:** Current Curve on both Directions

the obtained results, it is possible to see that for loads until 15kΩ, the current curve obtained are similar. When the load is increased to 20kΩ, the maximum current is around 190$\mu$A. This is due to the fact that, there are voltage drops on the cascode current mirror and the transmission gates and therefore, a supply voltage of 5V is not enough to give the 200$\mu$A to a 20kΩ load. Furthermore, analysing the curves for 50kΩ and 100kΩ, it is concluded that, for these loads, a supply voltage of 5V is not enough to provide the currents from the specifications as expected. Therefore, the maximum load for the system correct operation is bellow 15kΩ. However, if the scaffold resistance is higher than this value, the stimulation can still be performed in a linear range, although in a smaller range of currents.

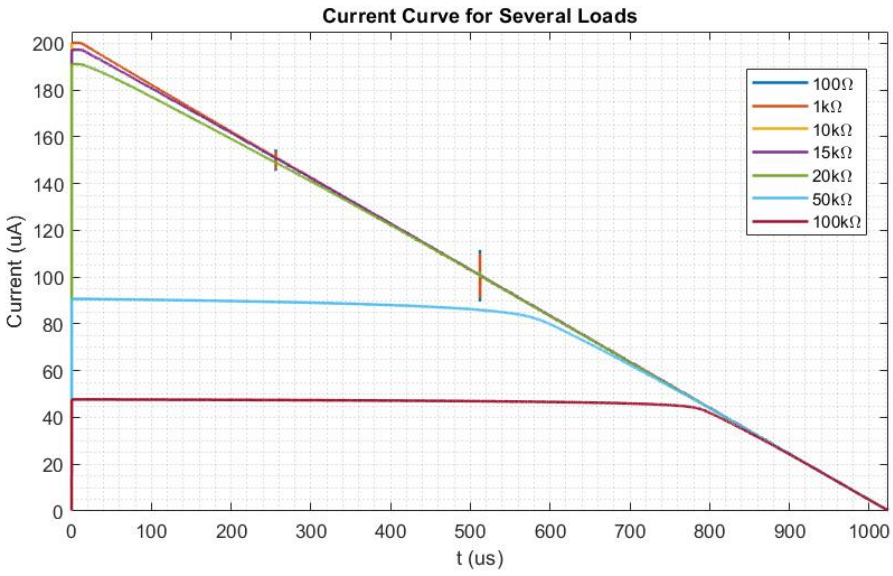


**Figure 5.8:** Current Curve for Several Loads

## 5.3 H-Bridge

The h-bridge circuit was tested with the test setup represented in figure 5.9a. The objective was to test the implemented control logic and to test the switches speed on the rising and falling edges. For the test performed on the control logic, an enable signal with frequency of 100kHz, rising and falling times of 1ns was applied. The Direction signal used has a period of 50$\mu$s, and 1ns of rising and falling times. Finally, it was applied a current of 200$\mu$A to a 10k$\Omega$ resistive load and a 1pF capacitive load. The results are presented in figure 5.9b. It is demonstrated the proper operation of these signals, since the "Enable" signal enables the current properly and the "Direction" signal changes the current flow on the load as expected.

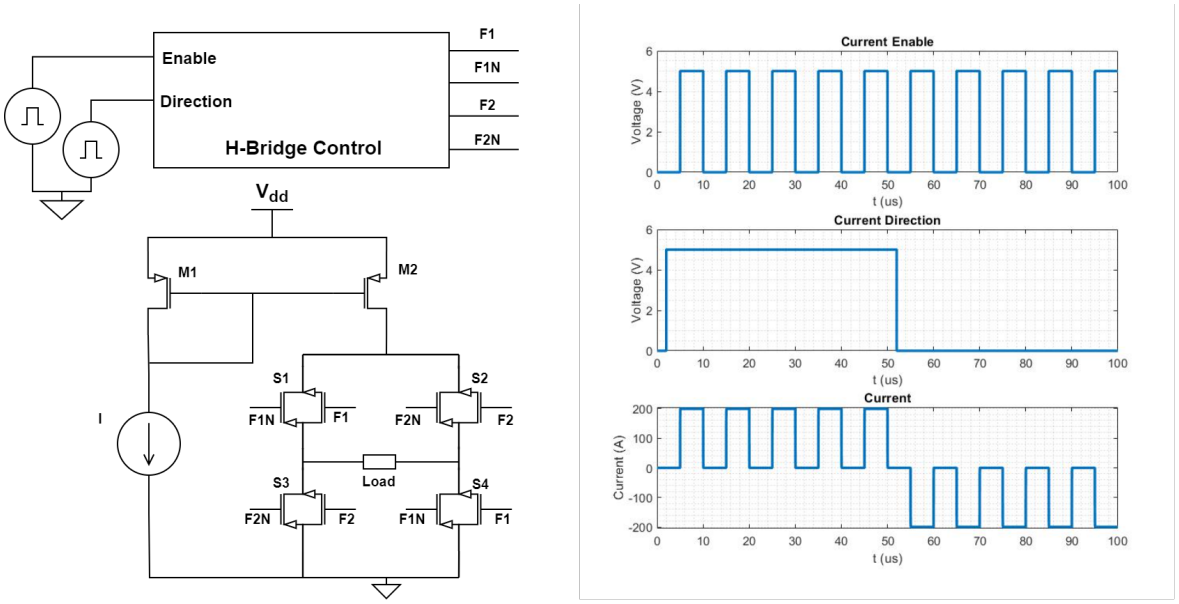


**Figure 5.9:** a. H-Bridge Test Setup, b. H-Bridge Control Signals Test

The h-bridge switches commutation speed characterization was also performed and is presented in figure 5.10b and figure 5.10c using the test setup presented from figure 5.10a. For the test, it was applied, at the input, a pulse signal with a rising (or falling) time of 1ns between 0 and 5V for the rising edge (or between 5V and 0 for the falling edge). The output signal was plotted and it was measured the time at 10% and 90% of the output, for both the falling and rising edge and the difference was computed. It was obtained a rising edge time of around 1.32ns and 0.715ns for the falling edge.

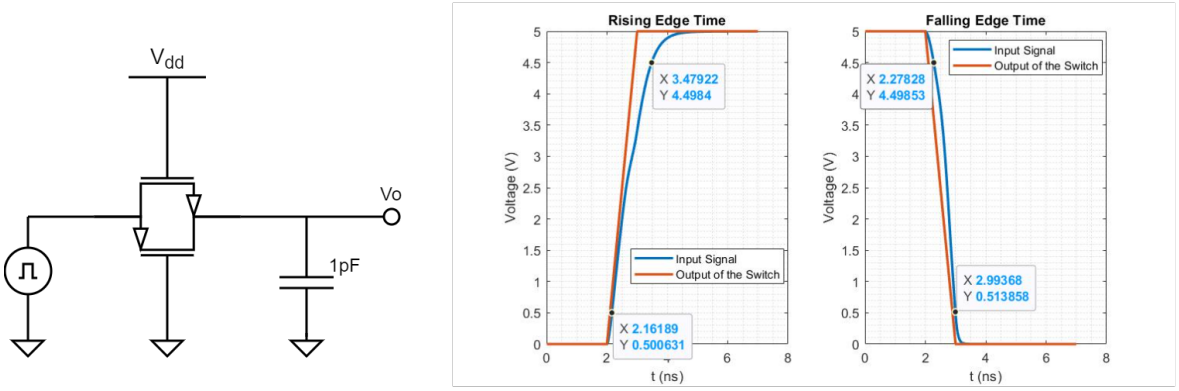


**Figure 5.10:** H-Bridge Switches Test, a. Test Setup, b. Rising Edge Test, c. Falling Edge Test

## 5.4 SPI Communication Interface

The test setup for the SPI communication interface is presented in figure 5.11. It is based on the implemented communication interface with the DAC at the output. The objective of this test was to evaluate the previous explained operation of the interface. The signals applied to the test setup were:

- *Clk* - the circuit clock signal. It is simulated by pulsed signal with a period of 50ns (frequency of operation of 20MHz), with 50% duty-cycle and falling and rising times of 1ns.
- *Chip Select (CS)* - signal sent from the microcontroller responsible for enabling communication with the stimulation circuit. It was simulated using an active-low pulsed signal. It has a period of 850ns, with a pulse width (at "0") of 16 clock cycles (800ns), since it is supposed to send 16 bits of information. Rising and falling times used were 1ns.
- *Serial Data In (SDI)* - it is responsible to send the serial data word to the system. It is a pulsed signal, with minimum voltage of 0 and maximum of 5V. It has a period of 100ns, a duty-cycle of 50% and the equal falling and rising times as the previous signals. With this period and duty-cycle, the word "1010101010" is sent to the interface.

Using the explained setup, the test was performed using a transient analysis during 1$\mu$s. The results obtained are presented on figure 5.12. The communication starts when the "Chip Select" signal is pulled down. After 16 cycles, the word is fully received and the "Start of Conversion" signal is activated. This signal enables the data register, which receives the data word in parallel from the shift register, and provides it at its output. It is presented the output of the 10 MSB of the data register (Q15 to Q6), since these are the responsible for providing the digital word to the DAC. As it can be seen by analysing figure 5.12, right after the word is provided at the output of the data register, the DAC starts the conversion and takes around 200ns to provide the output voltage. Note that, during the development of this work, the maximum frequency of operation tested was 20MHz. Therefore, 20MHz is the maximum communication frequency guaranteed. With the presented results, the communication interface correct operation and its integration with the DAC is verified.

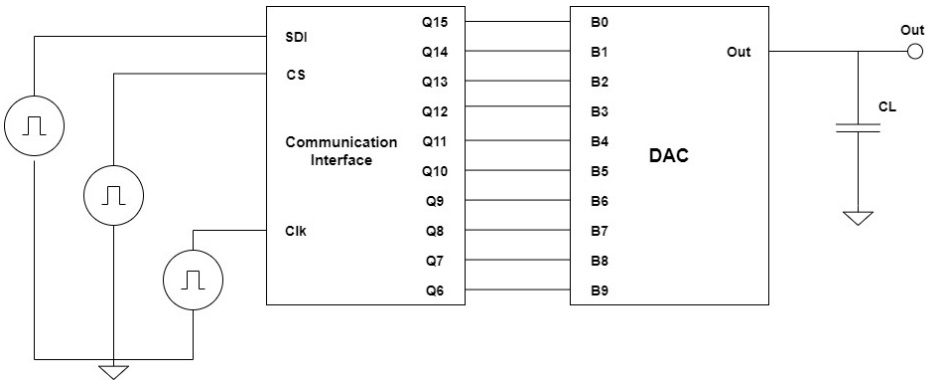


**Figure 5.11:** SPI Communication Interface Test Setup

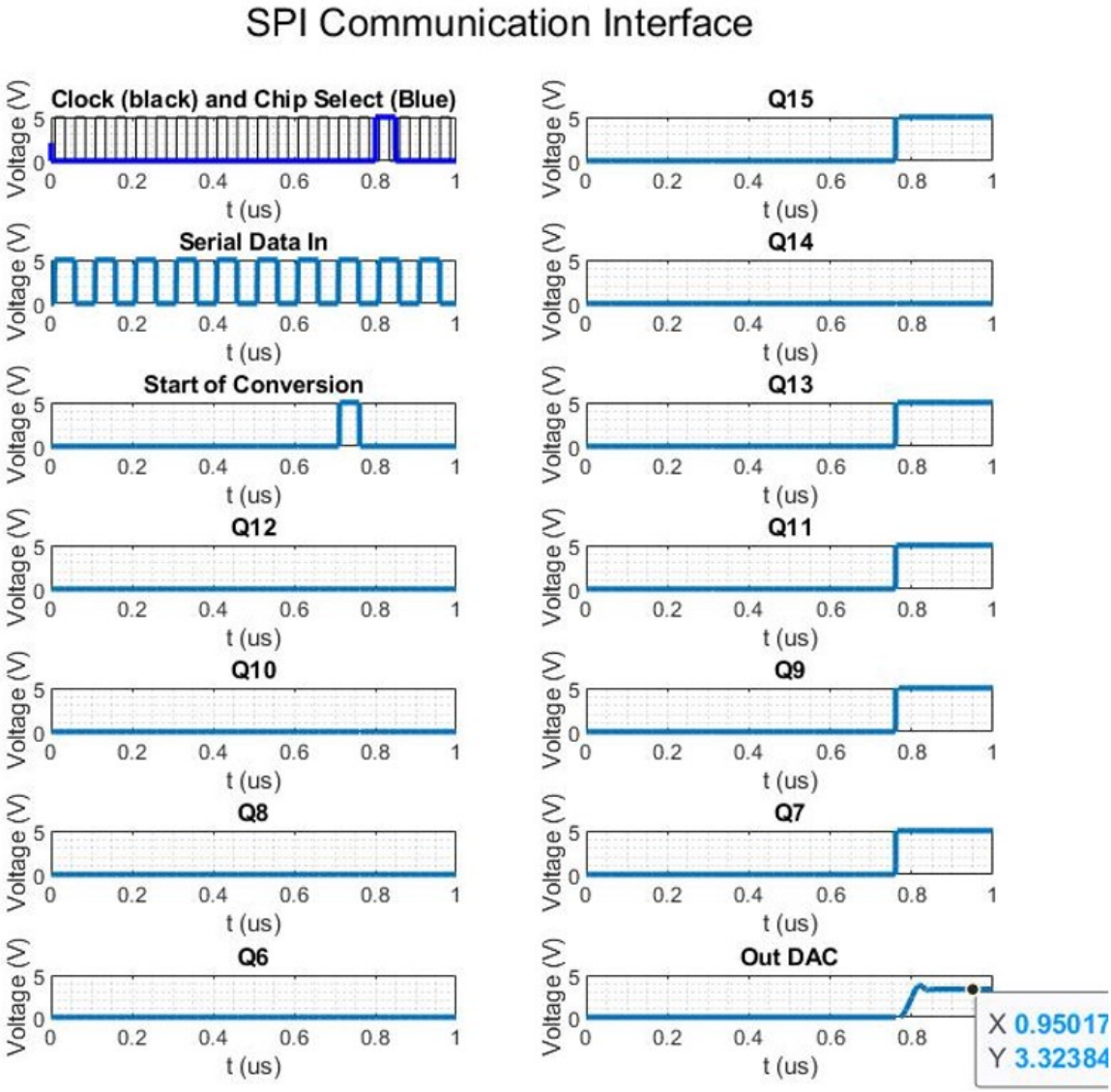


**Figure 5.12:** SPI Communication Interface Test Results

## 5.5 Full System Simulation

The various components of the system were integrated and the system was tested. For the test, it was used the setup presented in figure 5.13. The "Enable", "Direction", "Chip Select", "Clock" and "SDI" were applied as previously. The resistor $R_S$ used was the previously calculated (12.150k$\Omega$) and the load impedance was 10k$\Omega$ of resistance and a capacitance of 1pF. The tests presented in this section are: a use case of the system operation, the current curves when applied at the input the 1024 different possible codes with corner analysis, the error for each obtained current curve and the operation at the maximum frequency of the specifications (100kHz).

A system operation use case is presented in figure 5.14. The aim is to assess the operation of the whole system integrated. In this use case, firstly it is applied a digital word "1111111111" at the input of the system. Before activating the current with the "Enable" signal, the current direction is defined to the positive one. After 1.1$\mu$s of the start of the communication, the enable signal is defined in order to give time for the data word to be received and the DAC to convert it. Then, a different data word is applied ("1010101010"). Before establishing again the communication, the current on the h-bridge is disabled. The previous process is repeated, with the communication being established, the current direction being defined, and after the communication and the word conversion is finished, the current is enabled.

In figure 5.15a, the current curves for the 1024 different possible input codes were measured, with a corner analysis. The corners used on the simulation were, typical operation (tm), worst power (wp) and worst speed (ws). From the obtained plot, it is concluded that the current curves presented, are almost overlapping, which means that the corner divergence is low. However, zooming the plot, it is possible to see that the worst speed presents higher current and the worst power smaller current, when compared with the typical mode. Furthermore, this can be especially observed in the region of the maximum current.

To further quantify the divergence of the current curves, the error between the ideal current and the typical mode, worst power and worst speed currents, were computed and plotted. The results obtained are presented on figures 5.15b, c and d. Analysing the results, it is possible to see that the error on the typical corner current varies between -0.4$\mu$A and 0.3$\mu$A, being at the limits of the range higher than the ideal one and at the middle lower

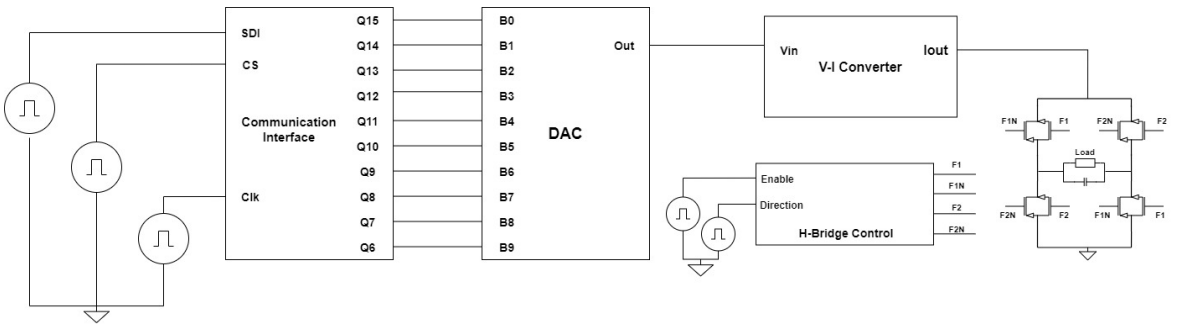


**Figure 5.13:** Integrated System Test Setup

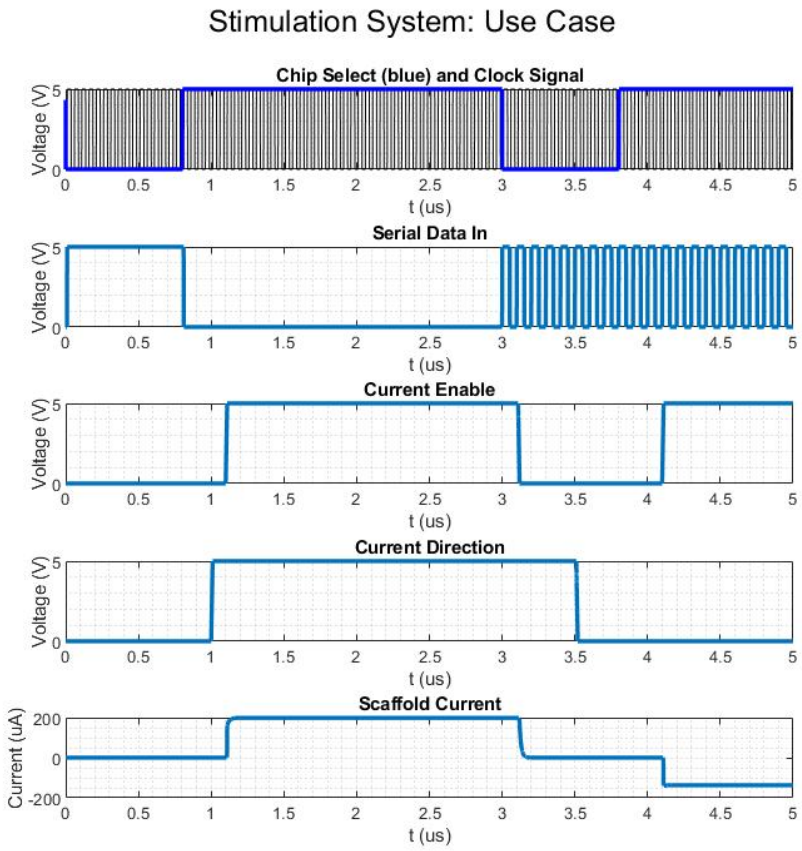


**Figure 5.14:** System Operation Use Case

than the ideal. Analysing the worst speed error curve, the error, for the most range, varies between -0.2$\mu$A and 0.5$\mu$A. On the higher codes, the error increases and peaks at around 1.5$\mu$A. However, this occurs when the V-I converter already left the linear zone of operation, therefore this range is not important on the analysis. Comparing the error from this curve with the ideal one, it is confirmed the referred tendency. On the worst speed corner, the current is higher than the obtained when considering the typical corner. Analysing the worst power operation corner, the opposite is seen. The error, for the most range, varies between around 0.1$\mu$A and -0.5$\mu$A, and for the higher digital codes, the error peaks in -1.5$\mu$A in the range where the circuit leaves operating in the linear region.

To test the developed system with the maximum frequency of operation from the specifications a simulation was performed. The word ”1111111111” was transmitted to the system, the current direction was maintained and, at the ”Enable” signal, was applied a pulse signal with a frequency of 100kHz. The simulation results are presented on figure 5.16. Therefore, the operation for the maximum frequency from the specifications is proven.

Finally, a simulation on the power consumption from the whole system was performed. The test setup was the one in figure 5.13. It was sent the word ”1111111111” to the input of the system and the current from the supply voltage was measured during the process of

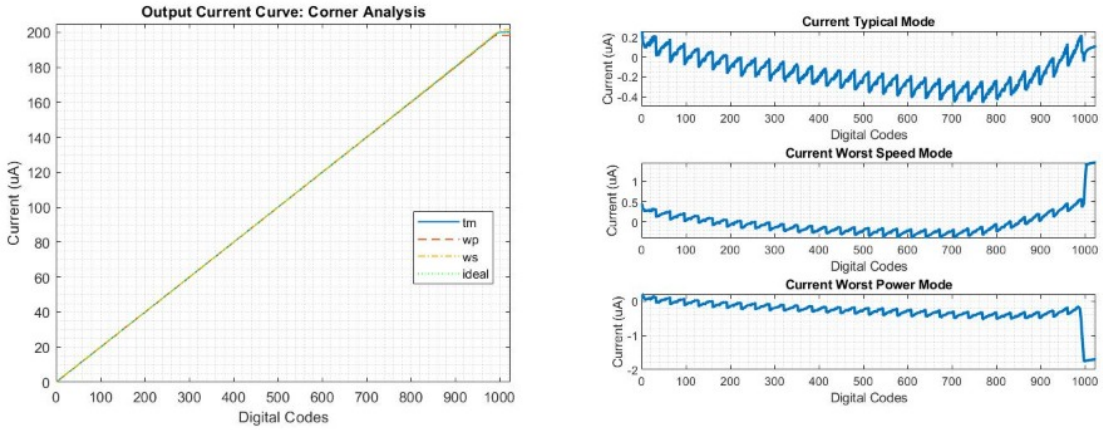


**Figure 5.15:** Output Current Curve: Corner Analysis. a) obtained current curves, b) error in typical corner, c) error in worst speed corner and d) error in worst power corner

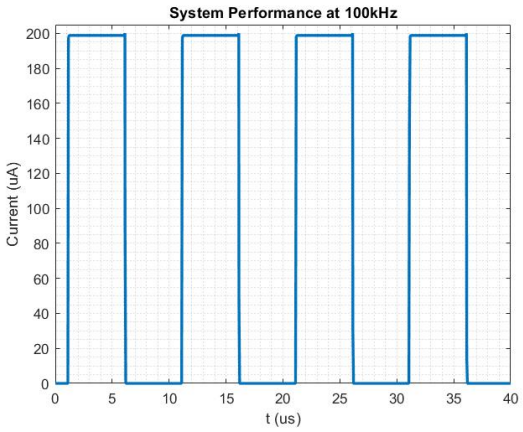


**Figure 5.16:** Output Current with a 100kHz signal

**Table 5.2:** Circuit Power Consumption

| Operation Corner | tm | wp | ws |
|---|---|---|---|
| Power Consumption | 19mW | 21.2mW | 17.3mW |

receiving the information, converting it and providing the correspondent current to the 10kΩ load. Furthermore, it was computed the average value of the current and it was multiplied by $V_{DD}$ (5V). This process was performed for the three operation corners as it is presented in Table 5.2. As expected, power consumption is higher for worst power corner and lower for the worst speed corner, when compared to the typical corner. For the typical operation corner a power consumption of 19mW was measured. During the simulation, the word "1111111111" was sent since it provides the maximum current and, therefore, maximum power consumption.

CHAPTER 6

# Layout and Results

This chapter presents the implemented circuit's layout. The main considerations and techniques used in the layout implementation are presented, followed by the post-layout simulation results and characterization.

## 6.1 Design Procedure

The layout is the physical representation of the circuit in layers. It is based on the combination of geometrical rectangles, which combined create the electrical circuit components and the connections between them. The layout design steps are described in figure 6.1. The layout design process starts after having the circuit implemented and tested in a schematic cell. The circuit elements and their connections are designed in the Virtuoso Layout environment. During the design process, the layout must be verified using the Assura verification tools, which are going to be described later in this section. When a full verified layout is obtained, the parasitic extraction process is performed using the Quantus Extraction Solution (QRC) tool and Post-Layout Simulations are performed to test the circuit operation and characteristics, comparing them to the ones obtained in the schematic. The layout design is an iterative process. During the design, the layout must be iteratively verified to comply to certain rules and adjusted if the required operation is not achieved.

The first step in the layout verification is the Design Rule Check (DRC). There are a number of rules that need to be complied during the layout development, called the"Design Rules". These are associated with the physical limitations inherent to the Integrated Circuit (IC) fabrication process, which establish the minimum size of the different layout elements and minimum distances between them. It is imperative to guarantee that all the Design Rules are ensured through the DRC, since it helps ensuring that the circuit operation and characteristics are maintained when it is fabricated. The DRC is a tool that checks if every polygon of the design complies with the specified rules. The DRC should be run frequently as the different cells and circuit components are added, to ease the process of identification of the cells with errors and correct them.

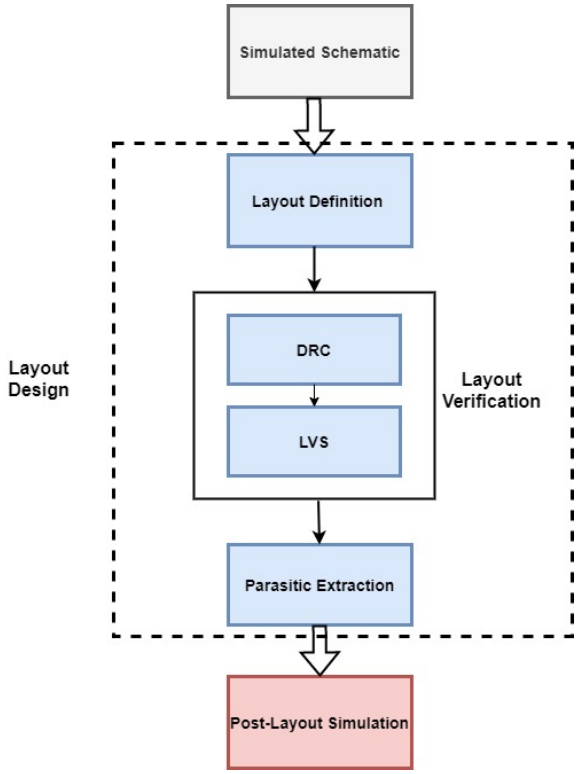


**Figure 6.1:** Layout Design Procedure

The second step of the verification makes use of the Layout Versus Schematic (LVS) tool. As the name suggests, this tool extracts a netlist of the implemented layout and compares it with the netlist from the schematic view. The comparison includes the geometry of the different components and the connections between the different elements of the circuit. This tool has the objective of ensuring that the implemented layout matches the schematic cell netlist. This way, it is guaranteed that the designed layout implements the required operation.

After the DRC and the LVS (verification process) have passed successfully, parasitic extraction is performed using the QRC tool. The QRC tool goes through all the layout components and connections between these and calculates the parasitic components present in the layout. The parasitic extraction recreates the layout with the parasitic components, creating a more realistic model of the circuit. This way, more accurate simulations on the circuit performance can be performed, which is the final step in the layout implementation, the ”Post-Layout Simulation”. The parasitic extraction can be performed using several extraction parameters. The ones used in the present work were the ”RC” (parasitic resistors and capacitors) coupling type, with reference to the ground node.

The final step of the layout design process is the ”Post-Layout Simulation”. In this step, the circuit is simulated once again using Spectre, but this time it is simulated the layout with the parasitic components extracted. The Post-Layout Simulations are important to verify if the circuit operation and characteristics are maintained with the parasitics and to characterize the circuit with a model closer to the fabricated circuit.

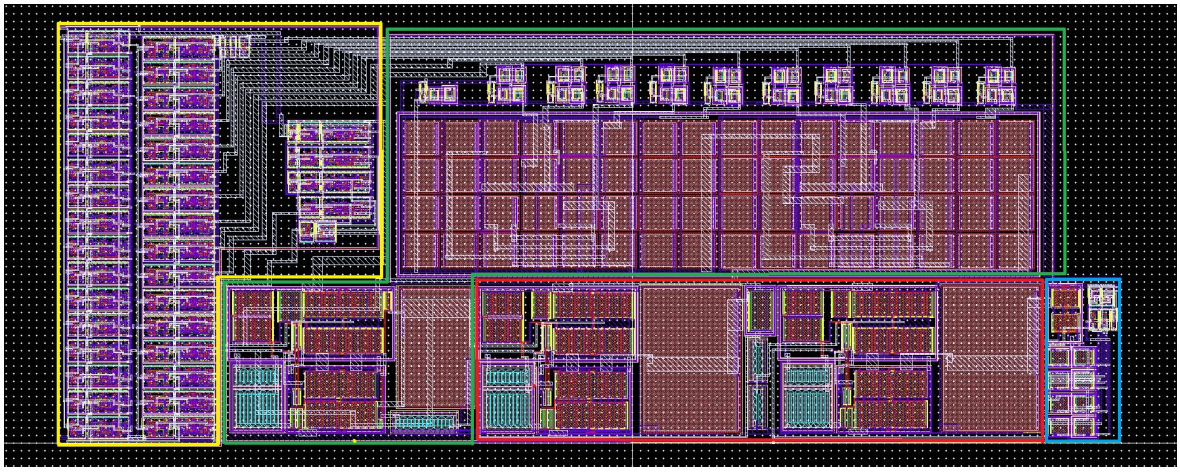

**Figure 6.2:** Stimulation System Layout. In yellow: SPI Communication interface, green: DAC, red: V-I Converter, blue: H-Bridge

## 6.2 Implemented Layout

The implemented layout is presented in figure 6.2. In the design, several techniques were used to minimize the area consumption, noise, the error introduced by the fabrication process and the influence of the parasitic components on the circuit performance.

The first technique is a "rule of thumb" on integrated circuits. It is based on positioning the transistors following the same orientation, maintaining this orientation for all elements of the circuit. In the case of the present work, the transistors were disposed in the vertical orientation. This way, the layout is uniform which improves the components matching.

Area consumption is a typical concern on integrated circuits design. ICs are required to be as small as possible, therefore optimizing the arrangement of the transistors and the other components that compose the circuit, is a key concern on the layout design.

Noise caused by the electronic components can degrade the circuit characteristics and, in worst case scenarios, can cause complete malfunctioning of the circuit. Noise is injected in the circuit substrate and is spread to all components that share the substrate. Therefore, techniques to reduce the noise spread should be used, especially when it is present a mixture of digital and analog components. Digital components inject noise in the substrate from the fast commutations that are subjected to. Since in analog components noise is a key concern, isolating the digital part from the analog one should be a priority.

A common technique to perform the isolation of circuits from the noise are guard rings. Guard rings provide low resistance paths that collect carriers from the silicon. They are structures that can be made from $p^+$ or $n^+$ diffusion layers. Typically, the $p^+$ structures are used around n type substrate and are connected to ground. On the other hand, $n^+$ structures are used on p type substrate, being connected to $V_{DD}$. Besides isolating circuits from the noise of the substrate, guard rings are also used to reduced latchup problems caused by parasitic bipolar transistors that promote low impedance paths between the power supply rails [25].

The fabrication process has limitations related to variations on the components' sizes. Smaller components are more prone to errors due to fabrication process, since a small variation

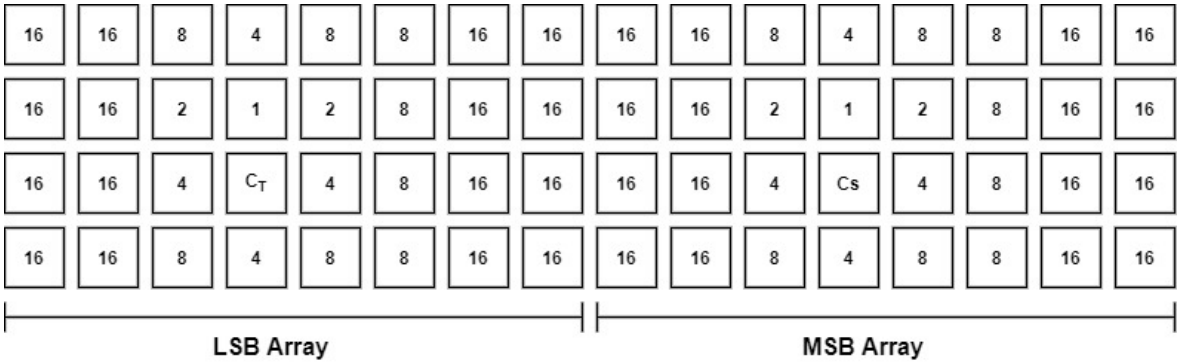


**Figure 6.3:** DAC Capacitors Array Distribution

on the fabrication process can be significant to such devices. Therefore, it is a major factor that introduces errors on the circuit and its consequences should be reduced. Several techniques were used to reduce the fabrication process influence and, therefore, the components mismatch.

- when transistors have large width, typically they are divided into several smaller transistors. This way, structures around transistors are similar which reduces the fabrication mismatches. Furthermore, this technique helps in optimizing the area.
- the use of "dummy" elements between between components (i.e. transistors) of the same geometry is a common technique. This makes the components more similar and uniform, reducing errors from the fabrication process.

Furthermore, especially on the DAC implementation, where reducing mismatches on the capacitors and the parasitic effects are important, a few more aspects were taken into account on the design. To improve the matching between the capacitors and to reduce area consumption, it was made an array of capacitors, each capacitor with the size of the unitary one 21$\mu$m per 21.8$\mu$m, which gives a value around 400fF. To form the higher valued capacitors, several capacitors were connected in parallel. The common centroid distribution technique was used on the capacitors array. It is based on the distribution of the circuit components (in this case the capacitors) in a symmetry axis, with the capacitors with lower values (and therefore, combined with the less capacitors in parallel) being on the center of the centroid and the larger valued capacitors are placed more on the periphery. This brings symmetry on the design reducing mismatch errors [33]. The common-centroid placement can be seen on the stimulation circuit layout presented in figure 6.2, however a simplified representation of the followed capacitors' distribution is presented in figure 6.3. In addition, parasitic components (capacitors) can be significant on the DAC capacitors array. In a binary charge scalling DAC, the parasitic effects can be reduced by connecting the top plate of the capacitors to the output node, instead of the back plate, which proves to be a major factor on this matter [40]. In addition, the larger the size of the capacitors, the smaller the effects of the fabrication mismatches. Therefore, the unitary capacitor was chosen to optimize the mismatches and area. Finally, the DAC capacitors were isolated with guard rings from the rest of the circuit to reduce the noise effects.

The stimulation system circuit has a size of around 700$\mu$m of width and 270$\mu$m of length, which makes a total circuit area of $0.19mm^2$.

## 6.3 Circuits Results

Following the layout design and parasitic extraction, post-layout simulations were performed on the various circuits. This section presents the results on the DAC, the V-I converter and the communication interface, evaluating if the characteristics of these components are maintained. Results on the fully integrated system are presented on the following section.

### 6.3.1 DAC

The DAC converter was the component which had its performance affected the most with the layout design, due to errors caused essentially by the parasitic capacitances. Therefore, a careful characterization of the DAC was performed. The tests performed and the setups used were similar to the ones presented in the previous chapter.

In figure 6.4a, the obtained DAC curve for all the codes is presented and compared to the ideal one. Furthermore, in figure 6.4b, the maximum conversion time of the DAC is presented. It was tested by presenting at the input of the DAC, firstly the code "0000000000" and then change it to "1111111111". It can be seen that the output stabilizes at around 250ns.

Additionally, the voltage values that corresponds to each input bit of the DAC were measured, being the results presented in table 6.1. In this table, the ideal values for each bit and the ones obtained through the schematic simulation are also presented for comparison. Analyzing the table, it can be seen that all bits present a smaller value than both the ones obtained from the schematic and the ideal value. These results are explained, mainly, by the presence of parasitic capacitors in each of the capacitors from the array. These are significant enough to change the value of each capacitor of the array and, therefore, the weights associated to each bit is changed. Furthermore, the errors increase for the more significant bits, since the scaling capacitor has a different value from the remaining of the capacitors on the array, it is sensible to mismatches and the parasitic components.

**Table 6.1:** Voltage Values for each Bit after Parasitic Extraction

| bit | Ideal Value (V) | Schematic (V) | Layout (V) |
|---|---|---|---|
| B0 (MSB) | 2.5 | 2.497 | 2.491 |
| B1 | 1.25 | 1.248 | 1.244 |
| B2 | 625m | 624.16m | 618.5m |
| B3 | 312.5m | 312.08m | 306m |
| B4 | 156.25m | 156.13m | 150.45m |
| B5 | 78.125m | 80.1m | 75.6m |
| B6 | 39.0635m | 39.58m | 37.73m |
| B7 | 19.53m | 18.85m | 18.63m |
| B8 | 9.766m | 9.87m | 8.99m |
| B9 (LSB) | 4 .883m | 4.79m | 4.76m |

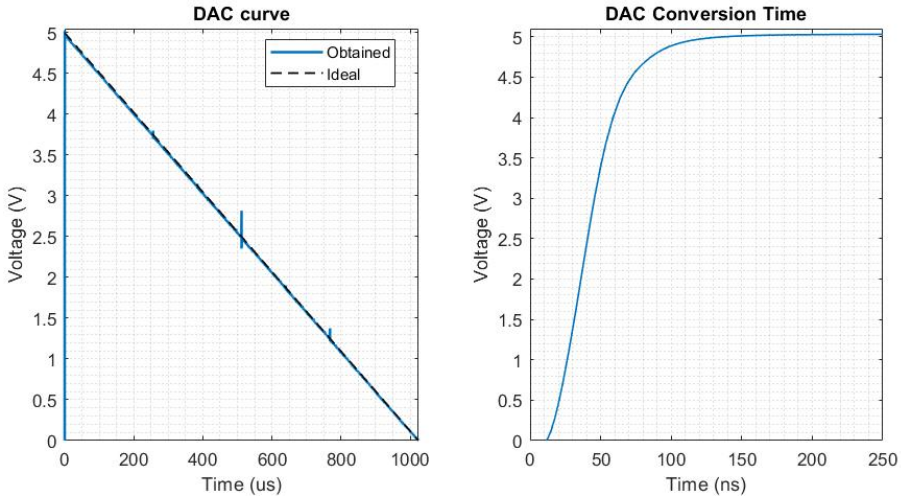


**Figure 6.4:** a. DAC obtained curve for all input codes after parasitic extraction, b. DAC conversion time after parasitic extraction

Using the curve from figure 6.4a, the DAC was characterized on its DNL, INL and offset error. The DNL and INL curves are presented in figure 6.5. Analyzing the DNL curve, it varies for most of the codes between 0.036 LSB to -0.28 LSB, where the peaks on -0.28 LSB occur every 16 codes (transitions from ”01111” to ”10000”). In addition, the DNL curve presents variations of -0.81 LSB, that corresponds to the transitions from ”011111” to ”100000”. Furthermore, at the codes 256 and 768 the DNL reaches the value of 1.24 LSB and at the code 512 reaches 1 LSB. Codes 256 and 768 happen when a transition from ”0111 11111” to ”1000 00000” occur and code 512 happen when the input of the DAC goes from ”01111 11111” to ”10000 00000”. Since it presents 3 codes where the absolute value of the DNL is above 1 LSB, the DAC is not fully monotonous in these regions. As for the INL presented in figure 6.5b, it varies from -1LSB to 1.85LSB. Differences on the DNL between two adjacent codes occur in the same transitions pointed out on the DNL. The obtained INL demonstrates that there is an inaccuracy between -1 LSB and 1.85 LSB on the DAC which, consequently, translates in errors on the stimulation current. The errors on the current are going to be quantified in the following section. Measuring the output value equivalent to the code 0 from figure 6.4a, the DAC offset was obtained, being around 1.4mV.

In summary, differences in the performance of the DAC from the schematic and the one with the layout with parasitic extraction occur mainly due to the parasitic capacitances on the capacitors array, that changes the equivalent output voltage value for each bit. In the specifications a resolution of 0.5$\mu$A is desired, however since the DAC implemented is of 10-bit, a smaller resolution is achieved (0.2$\mu$A). Therefore, the DAC designed with the presented non-linearities and errors is still appropriate for the system.

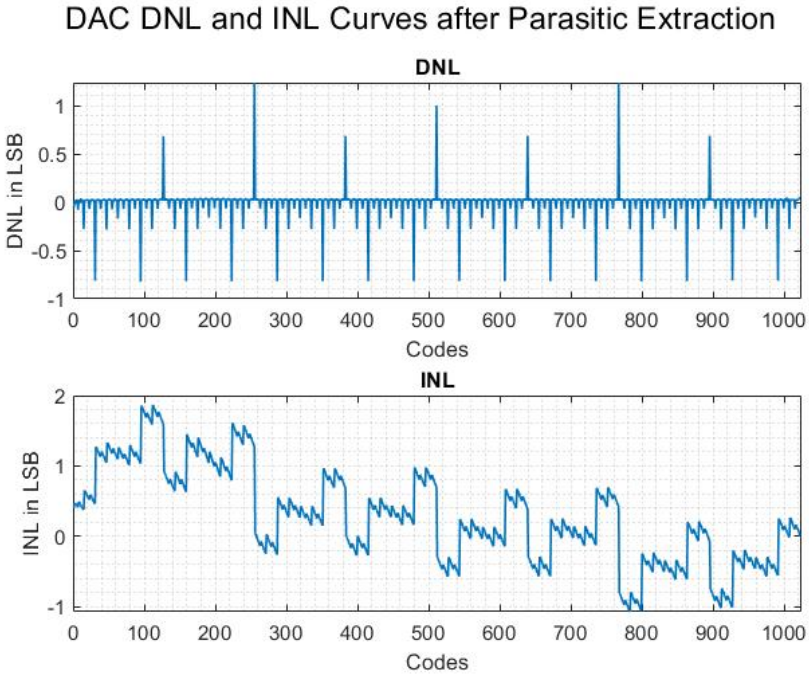


**Figure 6.5:** a. DNL Curve after Parasitic Extraction, b. INL Curve after Parasitic Extraction

### 6.3.2 V-I Converter

The V-I converter was mainly characterized, to check the input voltage common range and to obtain the current curves through all the input codes. The simulations performed and test setups used were similar to the ones from the previous chapter. The results on the first characteristic are presented in figure 6.6a. The obtained curve is very similar to the one obtained in figure 5.5. As it can be seen, the output current is linear with the input voltage in the range of 0 to 4.86V, maintaining the input voltage common range from the simulation results. The derivative of this curve is also presented, which supports the previous drawn conclusions on the converter linearity. In figure 6.6b, it is presented the output current curve for all digital input codes. This curve will be the target of a more in-depth study on the next chapter.

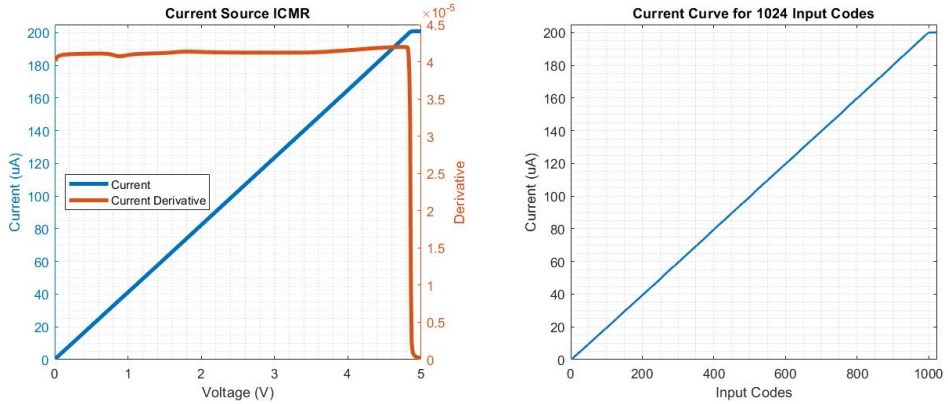


**Figure 6.6:** a. V-I Converter Input Voltage Common Range after Parasitic Extraction, b. V-I Converter Curve with the 1024 Different Input Codes after Parasitic Extraction

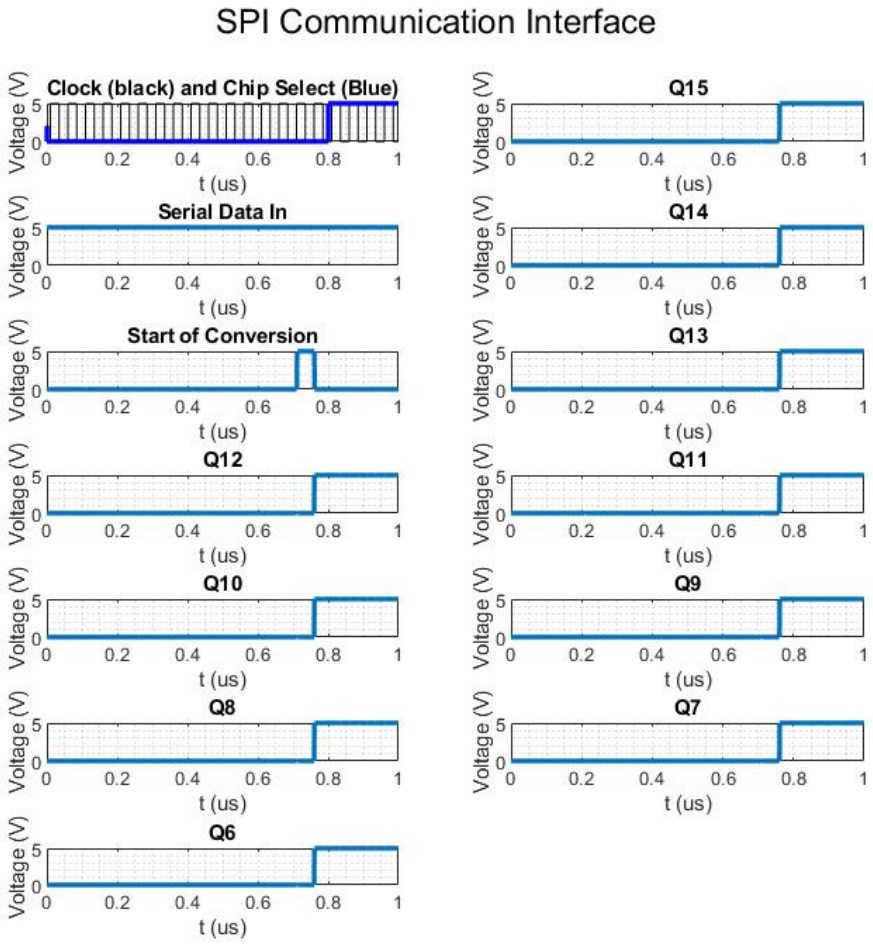


**Figure 6.7:** SPI Communication Interface Operation Test after Parasitic Extraction

### 6.3.3 SPI Communication Interface

Tests on the SPI communication interface were performed with the objective of guaranteeing that its operation is as expected, with the physical layout and the parasitic extraction. The demonstration of the operation of this interface is presented in figure 6.7. The test setup used was based on the setup from figure 5.11. The input word applied was "1111111111111111" and a clock signal with 50ns of period. As it can be seen from figure 6.7, the interface operation is as expected. When the chip select signal is active the communication starts, after 16 clock cycles, the start of conversion signal is activated and the word applied at the input is presented in parallel at the output of the interface (signals Q15 to Q6).

## 6.4 Final Results

This section highlights the main results on the stimulation system circuit layout after parasitic extraction. Main results include the system operation use case and the quantification of the the stimulation current errors. Corner analysis and power consumption simulations are also presented. Simulations were performed using Cadence software, using the Spectre simulation tool.

The setups used for the following tests were based on the one presented in figure 5.13. The clock operation frequency is 20 MHz, the rising and falling times of all pulsed signals applied are 1ns, and the load is composed by a 10kΩ resistor in parallel with a 1pF capacitor. The first test performed was a demonstration of the system operation, to check that the system behavior is as expected. Results are presented in figure 6.8. This simulation is very similar to the one performed in figure 5.14. The stimulation system receives a binary word when the chip select signal is active. The word received is "1111111111", which is applied to the system by a pulse signal connected to the SDI pin. After receiving the digital word, the current direction is defined as positive, and the current is enabled. The process is then repeated for the other direction.

A second simulation was performed to analyze the stimulation current performance for both directions for all different possible codes. 1024 different codes were applied at the input of the system and the stimulation current on both directions was measured. In addition, the difference between the obtained values and the ideal ones were computed and the curve was plotted. Results are presented in figure 6.9. The "Enable" signal used was maintained active during simulation. As for the "Direction" signal was maintained at '1' at the positive current and '0' at the negative. The load used for this test was also maintained with the parallel of a 10kΩ resistor and 1pF capacitor. Analyzing figure 6.9, it is concluded that the current error (analyzing for the positive current), varies between 0.2$\mu$A and -0.75$\mu$A, being most of the range bellow 0, which means that for the most range the stimulation current is bellow the ideal one. For the negative one, the current varies between -0.2$\mu$A and 0.75$\mu$A, which means that in absolute value the stimulation is bellow the ideal one. Therefore, comparing the curves for the current on both directions, it can be seen that the errors associated are very similar. Comparing the obtained error at this point with the one obtained in figure 5.15

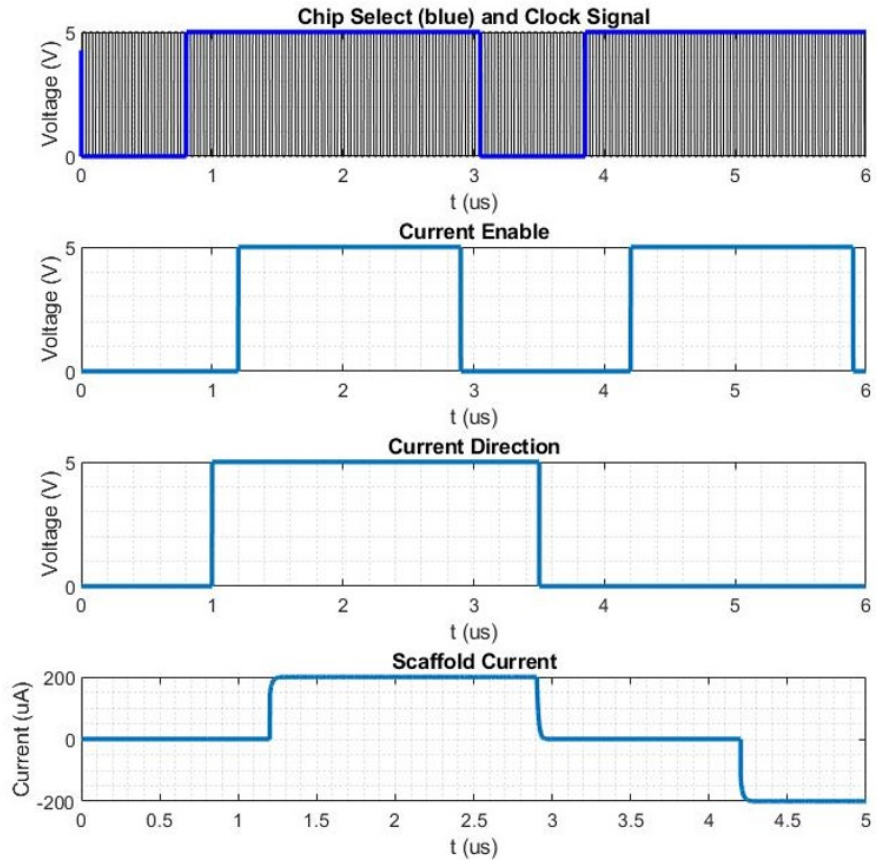


**Figure 6.8:** Post-Layout Simulation: System Operation Use Case

for the typical mode, it is concluded that the absolute errors in current increase. Furthermore, the error curves from figure 6.9, present transitions in the error curve that are not equal for the complete range, especially when high transitions of the digital codes at the input occur. For example, when the transition from ”0111111111” to ”1000000000” occurs, the current error goes from -0.22$\mu$A to -0.42$\mu$A. These errors are mainly due to the parasitic capacitances on the DAC as it was mentioned previously in this chapter. Both of these factors increase the errors on the conversion and, as a consequence, the voltage difference between two consecutive steps is not the same for all the steps, creating the behavior of the error presented.

Furthermore, the stimulation current performance was also evaluated, using the same setup for the corners performance (wp and ws). As previously done, the current curves for all possible codes were plotted and the error between these and the expected current was calculated. Results are presented in figure 6.10. The conclusions taken from the obtained results are similar as the ones presented in the corner analysis performed on chapter 5. For worst power operation, the stimulation current bellow the expected one for most input codes. At around code 800, the trend reverses and the stimulation current is above the ideal current. The error varies between -0.68$\mu$A and 0.58$\mu$A, and peaks at 1.43$\mu$A, for the 29 most significant codes. For worst speed corner operation, the current is bellow the expected one for all input codes, in exception for the first two. The error varies in the useful range between 0.08$\mu$A and -0.77$\mu$A, and peaks at -1.63$\mu$A when the circuit is operating in the non-linear region. Note

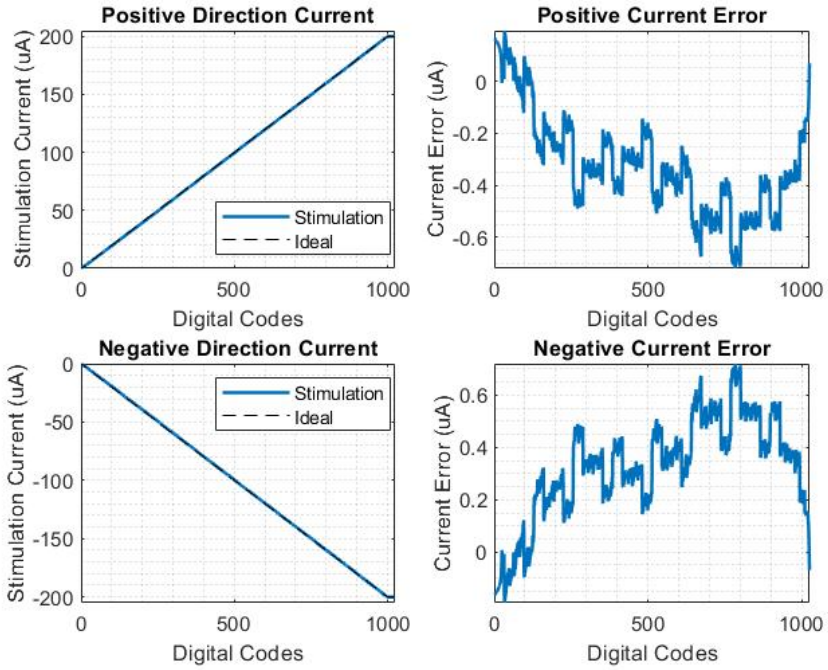


**Figure 6.9:** Post-Layout Simulation: Current Curves on both Directions

that, since the voltage-to-current converter as an operation range between 0 and 4.86V, as previously stated. This means that in this region, the circuit is not operating in the linear region and therefore the error peaks at -1.63$\mu$A (for the ws corner) and at 1.43$\mu$A (for the wp corner) are not relevant. Furthermore, since the error trend is very similar for both current directions, the corner analysis was carried out for only positive direction.

Using a similar setup as for the previous simulations, the current curves for different loads were measured on the typical operation mode. The resistive part of the impedance was varied, being used the values: 100Ω, 1kΩ , 5kΩ, 10kΩ, 15kΩ and 20kΩ. The results obtained are presented in figure 6.11. This figure shows that the loads from 100Ω to 15kΩ present similar curves. For the resistive load of 20kΩ, the maximum current is limited to around 187$\mu$A, due to the limits of the circuit voltage compliance, as pointed out in chapter 5. Therefore, it is guaranteed that the circuit operates in the current range of the specifications with a maximum load of 15kΩ. Note that the stimulation can still be performed for higher loads, however in a smaller range of currents.

To finalize the post-layout simulation, the developed layout was tested on its power consumption. The tests were performed similarly as it was described in chapter 5 on a 10kΩ load and the average power consumption was computed for the 3 considered corners. Results are presented in Table 6.2. The average power consumption obtained was around 19.5mW for the typical corner. This is around 0.5mW above the one obtained on circuit simulation. This happens, since the layout takes into consideration the parasitic elements, which cause resistive connections between the components and a higher dynamic power consumption.

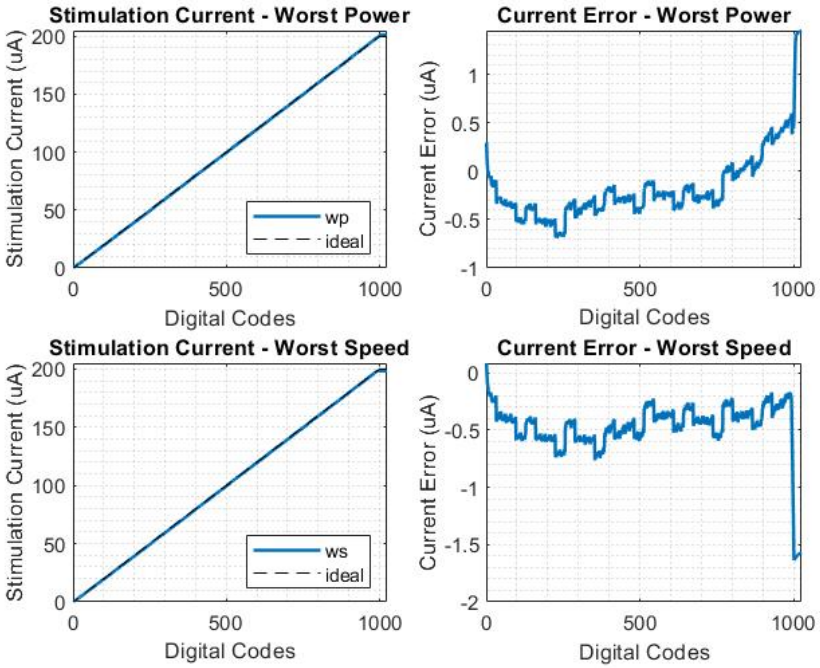


**Figure 6.10:** Post-Layout Simulation: Corner Analysis on Stimulation Current

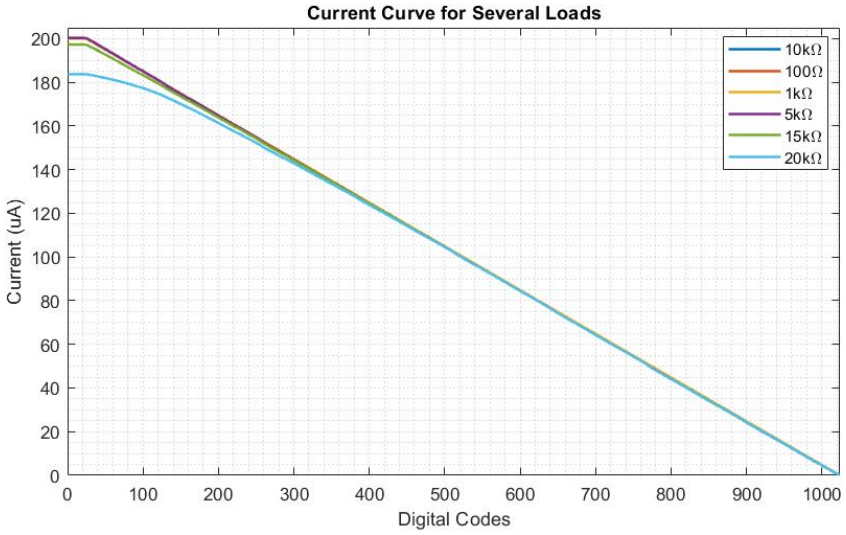


**Figure 6.11:** Post-Layout Simulation: Load Dependence

**Table 6.2:** Post-Layout Simulation: Circuit Power Consumption

| Operation Corner | tm | wp | ws |
|---|---|---|---|
| Power Consumption | 19.5mW | 21.5mW | 17.7mW |

CHAPTER 7

# Conclusion

This dissertation describes the design, implementation, simulation and results of an ASIC for current mode electrical stimulation of the spinal cord for neuronal regeneration, in a 0.35$\mu$m CMOS technology.

The work started with understanding the problem at hands, the study on basic fundamentals of electrical stimulation and the research on state-of-the-art stimulation circuits in order to reach to the architecture proposed. Having the architecture defined, studies on the necessary circuits were performed, where it was made a comparison on the different possible circuit topologies, to evaluate which are more suitable for the application. The necessary circuits schematics were implemented and validated using the Spectre simulation tool from Cadence software. At this stage, validation of the system integrated was also performed. Having the system operation verified in the schematic, the circuit layout was designed, followed by parasitic extraction and post-layout simulations. Post-layout simulations included characterizing the circuits developed and perform a comparative analysis with the results obtained from simulation. Furthermore, the integrated system operation was evaluated, the errors associated with the stimulation current were quantified, corner analysis was performed, the system output loads range was studied and the average power dissipation of the circuit was measured.

The stimulation circuit provides currents between 0 and 200$\mu$A, with current steps around 0.2$\mu$A. In addition, the errors associated with the stimulation current are lower than 0.75$\mu$A. The system errors are mainly due to the DAC. The influence of parasitic components and mismatches on the capacitors array decrease the DAC conversion performance. As consequence, the current accuracy decreases and the steps between two consecutive levels of current are not equal for all input binary codes. To increase the DAC performance, software or hardware calibration could be included, if even higher accuracy on the DAC is required. However, this would increase the system complexity, and since the accuracy achieved is satisfying for the application, calibration on the DAC was not considered. Another limitation of the system is that the V-I converter work range is limited to 4.86V, which reduces the system resolution

and the system voltage compliance. Nevertheless, a resolution of 0.2$\mu$A is achieved, higher than the 0.5$\mu$A from the specifications. Moreover, the system voltage compliance allows to provide currents in the range of 0 to 200$\mu$A to output loads below 15k$\Omega$, which is satisfying for the application. Nevertheless, the developed system is still capable of providing a linear stimulation current for higher loads, however with smaller current ranges. Furthermore, the stimulation current provided by the presented circuit, is capable of mimicking the mammalian embryonic current levels, with a high resolution, being adequate for cells regeneration purposes.

To conclude, the proposed system has a low-voltage supply (5V), an average power consumption of 19.5mW and a circuit area of $0.19mm^2$, making it suitable for an implantable device supplied by a battery.

## 7.1 Future Work

Even though the stimulation part of the proposed ASIC has been successfully implemented and simulated in the Cadence software environment, to have a fully developed prototype, further work is still required. The aspects that are suggested as future work from this dissertation include:

- Integration of the stimulation and acquisition circuits layout.
- Perform tests to evaluate the ASIC performance with the acquisition and stimulation circuits integrated.
- Inclusion of the contact pads for the input and output pins of the ASIC, and the choice of a suitable packaging for the ASIC. The choice of the packaging will depend on the total circuit area occupation including both circuits and the pads. Nevertheless, the Quad-Flat No-leads (QFN) 16 [53] is suggested as a good possibility, since it has the number of pins needed to accommodate all the ASIC pads. Furthermore, it is small in size (5mm per 5mm), making it a viable option for an implantable device.
- Tests on the produced circuit.

In addition to finalize the prototype development, implementing different architectures of the used components, especially the DAC, and comparing these with the developed on this dissertation can be useful to improve the stimulation system overall performance.

## 7.2 Contributions

In result of this work, a paper titled "ASIC with Current-mode Stimulation and Indirect Impedance Acquisition for Neuronal Regeneration", was submitted to a conference, IEEE International Symposium on Circuits and Systems 2022 (ISCAS22). Currently, it is being peer reviewed.

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