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Quelhas

ASIC para aquisição de sinais elétricos referentes a adECM/GBM scaffolds

An ASIC for electrical Probing of adECM/GBM scaffolds

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Palavras Chave   Circuito integrado, aquisição, electronica, medula espinal, implante

Resumo   Este documento tem como principal objetivo explicar o desenvolvimento dum sistema com a tecnologia de circuitos integrados. O sistema completo tem como função resolver problemas graves relacionados com a medula espinal e a sua reconstrução. Juntando um sistema de estimulação e de aquisição elétrica, cria uma forte possibilidade de uma solução robusta para o problema explicado acima.

Este circuito equivale a metade dum sistema, solução, e tem como função obter sinais elétricos à saída de uma "scaffold". Com a obtenção desses sinais é possível determinar a impedância equivalente da "scaffold". Resultando por fim numa resposta quantitativa acerca do crescimento da mesma. Nesta solução, a "scaffold" utilizada terá como base, materiais compostos por grafeno combinados com tecidos humanos. Sendo este um sistema de aquisição de sinais muito peculiar, sobretudo em termos de tamanho e consumo de potência, individualmente não possui nenhuma característica capaz de resolver o problema acima mencionado. No entanto, como circuito secundário consegue e muito, colmatar os dados adquiridos.

Primeiramente uma prova de conceito utilizando a interface Cadence Spectre foi utilizada, para desenhar e desenvolver os circuitos base. Após se obter resultados positivos, ou seja, um funcionamento esperado para cada bloco individual. Um "layout" foi desenvolvido, este também utilizando a ferramenta do Cadende Virtuoso. Este segundo passo do desenvolvimento é bastante importante, pois com poucos ajustes é possível criar um circuito equivalente em hardware.

Keywords   ASIC, acquisition, electronics, SCI, scaffold, implantable

Abstract   This dissertation document has the role of explaining how to design and develop an ASIC system. The full system has the objective to resolve a problem named, spinal cord injury, which is, as of today still an incurable illness. Merging a stimulation and an acquisition systems it might be possible to implement a reliable solution.

This circuit is a part of the full solution system and has the role to acquire electrical signals at the terminal of the scaffold being tested. This way, it is possible to indirectly determine the impedance value of the scaffold undergoing electrical stimulation. Resulting in a quantitative evaluation of the stimulation performance. For this project, the scaffold proposed is composed of graphene-based materials in combination with human adipose-derived decellularized tissue. Since this circuit is an acquisition system, by itself, it does not have the characteristics to resolve the illness stated above. However, has a secondary circuit, it is capable of complementing the results obtained even more.

First a proof of concept was achieved, in the Cadence Spectre, by designing and testing every block individually. Second, a layout was done, with the Cadence Virtuoso, this last process is very important because, with few modifications to the layout, it is possible to create an equivalent system in hardware.

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Acronyms

ADC Analog to Digital Converter. 7

adECM adipose derived decellularized tissue. 6

ASIC Application Specific Integrated Circuit. 2

BJT Bipolar Junction Transistor. 11

Clk Clock. 8

CMOS Complementary Metal Oxide Semiconductor Transistor. 11

CS0 Chip Select 0. 8

CS1 Chip Select 1. 9

EoC End of Conversion. 8

GBM graphene based materials. 6

IA Instrumentation Amplifier. 14

ICMR Input Common Mode Range. 30

LSB Least Significant Bit. 9

MOSFET Metal Oxide Semiconductor Field Effect Transistor. 11

MSB Most Significant Bit. 9

NMOS N-channel Metal Oxide Semiconductor. 12

Op-Amp Operational Amplifier. 14

PMOS P-channel Metal Oxide Semiconductor. 12

SAR Successive Approximation Register. 17

Chapter 1

Introduction

Humans as we know it today, is the result of approximately six million years of evolution. The modern form of humans only evolved about 200,000 years ago, civilization as we know it is only about 6,000 years old, and industrialization started in the 1800's [11]. In the early stages, the evolution aspect was mainly physical but, from the 1800s and beyond the evolution aspects became mostly mental, quality of life, and inventions. Even though the last century alone has more inventions/creations than a thousand years prior, making the latest human evolution almost palpable. There is still an ocean of situations and problems we still cannot overcome and resolve. Mainly in the medical area, having a body so complex, results in a wide variety of possible problems, not only physical but also mental. One of these problems is spinal cord injury (SCI).

Spinal cord injury commonly results from a sudden or traumatic impact on the spine, that fractures or dislocates vertebrae. This type of injury can be originated by traffic accidents, violence, sports, falls, cancer, or osteoporosis. This injury is mainly a debilitating neurological condition, that can lead to sensory loss, resulting in possible paraplegia or tetraplegia paralysis or even bowel/bladder dysfunctions. As can be seen (Fig.1.1), depending on what point of the spinal cord is affected, different paralysis can occur. For example, a C4 or C6 injury will result in tetraplegia, while T6 or L1 will result in paraplegia.

1.1 Problem

SCI has different tiers of severity, regarding the actual damage in the spinal cord, the four main ones are. Impact plus persistent compression, which is the most common. Typically occurs through burst fractures with bone fragments compressing the spinal cord. Impact alone with transient compression, in hyperextension injuries. Distraction injury, a stretch of the spinal cord that can occur when two adjacent vertebrae are pulled apart. Laceration/transection injuries can occur through missile injuries, severe dislocations, or sharp bone fragment dislocations [1].

Although various strategies have been tried at the research level neither of them finished with great success and to date, there is no effective SCI therapy that can
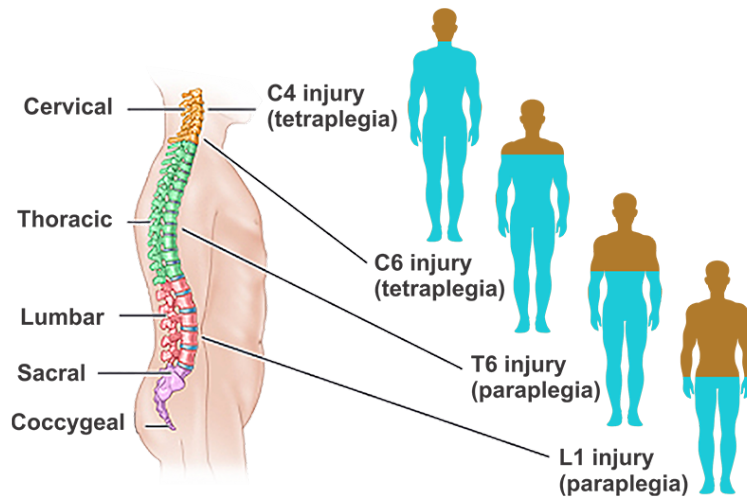
Figure 1.1: Different types of SCI injuries [24]

entirely restore neuromotor deficits. This means, that for now, this injury remains incurable. The second problem with this injury is its population ratio, "The incidence of spinal cord injury is about newly injured 10 000 people per year in the EU, and due to an almost normal life expectancy more than 200 000 patients are living with a spinal cord injury in the EU." [29]. More statistics show that "In the United States alone, over 1 million patients live with a SCI and more than 12 000 new cases occur every year." [8]. A report from the World Health Organization states that "People with a spinal cord injury are two to five times more likely to die prematurely than people without a spinal cord injury, with worse survival rates in low- and middle-income countries." [30].

In short, this injury, not only, is incurable but also represents many patients who, because of it, have the worst life quality.

1.2 Motivation

The motivation for this dissertation is to design, develop, and implement an electronic system that can acquire electrical signals (Acquisition System). This system will be a part of a larger project entitled "NeuralStimSpinal", which aims to contribute to a solution for the spinal cord injury. The project itself will be further explained, in Chapter 2.

1.3 Document Structure

This document is divided into 9 chapters. The next chapter, chapter 2, is based around the whole project, explaining the many steps and stages, the principal objective of the project, and the part developed and documented in this dissertation. The chapter 3, is the state of the art, relevant to the Application Specific Inte-

grated Circuit (ASIC) design, this chapter will explain a few solutions to resolve the problems. Chapters 4, 5 and 6, describe the types of hardware developed, as the schematics designed and also provide results in an ideal environment. These three chapters revolve around the validation of the whole system. Chapter 7 is related to a more specific way to simulate the whole system, with parasitic layout extraction, in this chapter a final layout is developed. Followed by a chapter of the whole system results and discussions, chapter 8. The final chapter, 9, presents the conclusions of this document and future work, to acquire better results in the previous chapter if needed.

Chapter 2

NeuralStimSpinal

2.1 Project

Merging an incurable injury that affects a quite large ratio of patients, decreases their life quality and quantity, results in a demand for a solution. This way various projects are created, each and every one, with a different idea/proposal to solve said problem.

The NeuroStimSpinal, (Fig.2.1), is an international project comprised of seven partners from the four European countries Portugal, Spain, the Netherlands, and Greece. The consortium members are research and technology organizations with complementary expertise and know-how in the targeted project sectors.

Figure 2.1: NeuroStimSpinal Logo [25]

The project itself aims to contribute with a solution for the spinal cord injury. SCI might result in para- or tetraplegia caused by the partial or complete disruption of descending motor and ascending sensory neurons. Once more, different techniques have been proven at research level, however, neither of them with success. Causing SCI to be a chronic illness, draining the health and economic state of every patient.

2.2 Proposed Solution

The radically new science-enabled technology proposed is to develop an innovative stimulus-responsive cell-laden bio material able to repair the SCI nervous tissue. Some reports were able to prove that nerve cells extend their projections parallel to the applied electric field and bend in order to align with its trajectory, [9]. The proposed innovative biomaterial characteristic is a scaffold for implantation in the traumatic injury point composed of graphene based materials (GBM) in combination with human adipose derived decellularized tissue (adECM). Coupled with a wireless electrical stimulation device to promote the growth and reconnection of the ruptured nerves. In short, the objective of this project is to try to repair the injury zone, by utilizing and stimulating graphene-based materials. This is the first time that a scaffold composition of this nature is proposed to solve the SCI.

This project is composed of three major parts, scaffold preparation, in vitro stimulation, and finally the in vivo stimulation, (Fig.2.2).

The first part revolves around the formulation of different adECM/GBM scaffold compositions, e.g. by shapes or porosity, the scaffolds can also be designed for different SCI locations. The in vitro charge stimulation helps to assess the biocompatibility, bio-functionality, and performance of adECM/GBM scaffolds using embryonic neural progenitor cells (ENCPs). Lastly, the in vivo system will evaluate the systemic and long-term efficacy of cell-laden and non-cell-laden scaffolds with and without electrical stimulation using rats and rabbits.
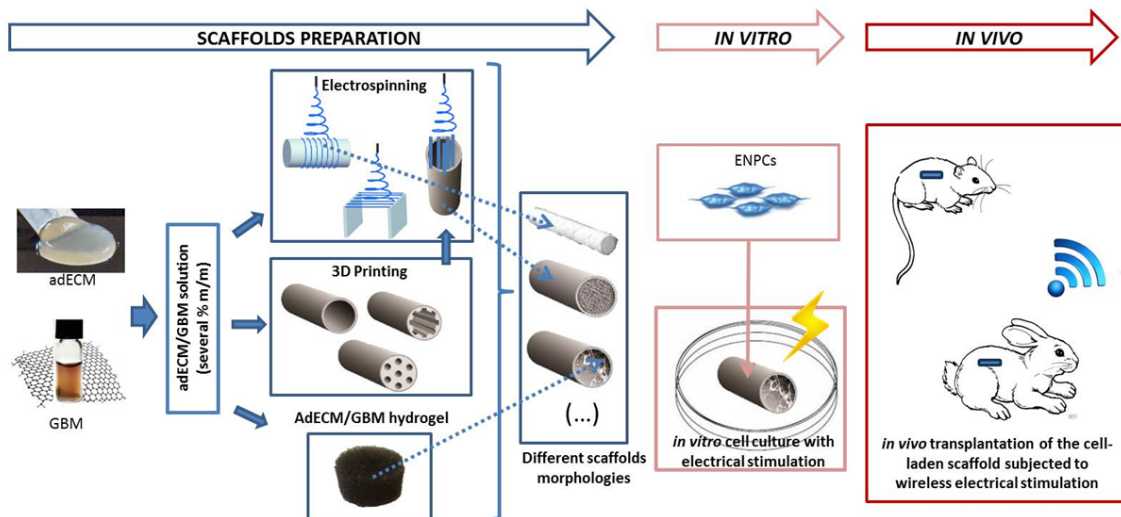
Figure 2.2: Full System [26]

The scaffolds preparation and in vitro stimulation of the project are already underway and with some conclusions. Many scaffolds with different sizes were tested and the overall understanding is that the scaffolds that are going to be used, will have impedance values between $1K\Omega$ and $100K\Omega$. The last part is quite more complex since, it needs to be implemented with a different type of electronic technology from

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the in vitro section, [12]. Because it is going to be transplanted into rodents. As so, an ASIC, needs to be designed and tested. For this specific methodology, an ASIC as follows was designed, (Fig.2.3). Having two different objectives for this ASIC, it can be divided into two. The first part, being a stimulation system, and the second part, an acquisition system.
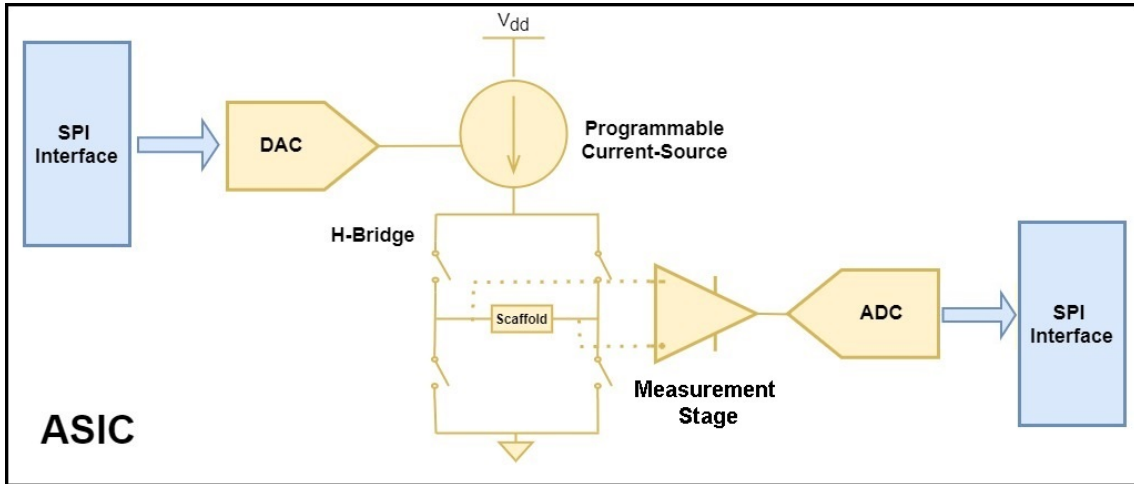
Figure 2.3: In vivo ASIC

The ASIC also has some specifications to be valid for this project application. The most important specifications are the need to have an amplitude resolution in the stimulation system, equal or lower than $0.5\mu A$ with a current range of 0 to $200\mu A$. These specifications result in a DAC of at least, 9 bits, being the final chosen DAC dimension of 10 bits. The Analog to Digital Converter (ADC) dimension must be equal or higher in order to convert with the same or lower resolution. The chosen solution was a 10bit ADC.

Characteristics	In-Vivo System
Compliance Voltage	5V
Stimulation Mode	Current
Current Range	0-200μA
Amplitude Resolution	0.5μA
Acquisition Mode	Voltage
Acquisition Range	0.067-4.86V
Frequency	1Hz - 100kHz
Communication with Microcontroller	SPI

Table 2.1: In-Vivo System Specifications

The stimulation system has the objective of applying a specific current through a scaffold, having also control over the current direction. This system is composed of four main blocks. A communication interface with the objective not only to receive and save the digital word sent by the microcontroller. But also rearranging

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the digital word from serial to parallel, making it easier for the DAC to receive the data. The next block is the DAC, the digital to analog converter, which has the objective to from any digital input recreate an analog output, proportionally. The Programmable Current-Source receives the analog voltage from the DAC and converts it, in a constant current, once more, the input voltage and output current need to be as proportional as possible. The last main block is the H-Bridge in which the scaffold will be placed and stimulated, this type of block is used because the nerve fibers can have different behaviors depending on the direction of the current flow that stimulates them [9]. This system relies upon some control signals, as the Clock (Clk) signal that will synchronize all the digital blocks with a frequency of 20MHz, the Chip Select 0 (CS0), that will select this part of the ASIC as the slave in the communication process, the "Enable" to enable or disable the Programmable Current-Source and lastly the "Direction" signal that will determine the current flow within the H-Bridge.

2.2.1 Acquisition system

Since one of the aspects that change after an injury is the electrical impedance of the neural tissue as they undergo a healing process. This was shown as a steady evolution in the electrical impedance of rat sciatic nerves [17]. The acquisition system has the objective of indirectly measuring the impedance value of the scaffold undergoing electrical stimulation. This way, it is possible to determine if the nerve fibers attached to the scaffold grew or decreased in size [22]. This conclusion would be otherwise impossible without medical intervention, being the load implanted within the patient. This way, it is possible to complement the results obtained even more.

This whole system is composed of three main blocks, (Fig.2.4), named as, Measurement Block, to determine which terminal of the scaffold is going to be amplified and tested, the ADC Block, that will make the conversion from analog to digital and lastly, the Communication Block, which communicates between the system and the microcontroller.

Figure 2.4: Acquisition System

This system as the one before also relies upon some control signals, two of them are shared between both systems, the Clk signal and the Direction signal. For the Acquisition system, this first signal synchronizes the ADC and the Communication blocks, while the second determines which terminal of the scaffold is going to be tested. The other control signals are the Start of Conversion (SoC), which has the objective of starting the ADC conversion sequence, the End of Conversion (EoC), which marks when the ADC sequence ends. It also saves the converted information

in the Communication Block and lastly the Chip Select 1 (CS1), which will select this part of the ASIC as the slave in the communication process.

One possible demonstration of how the Acquisition System should work is displayed beneath, (Fig.2.5). In the figure when both the SoC and Eoc signals go active, "1", for one and sixteen cycles, respectively. The Comp signal which is the serial output from the ADC Block will start to show the bit-by-bit response for the input voltage. In this hypothetical demonstration, we can assume it is the maximum voltage drop in the scaffold, 2V. Having also the Direction signal as, for this example, a "1" for the first conversion and a "0" for the second conversion. When the CS1, is activated, the data of Direction + Comp is saved in the Communication Block. The Direction signal represents the Most Significant Bit (MSB) saved, the Comp signal comes next in order, from the most significant to the least, the final 5 Least Significant Bit (LSB) from the 16 bits saved in the Communication Block, do not represent any value. As so, they are all grounded. After the data is saved, it starts to be sent to the micro, justified by the Serial Digital Output (SDO) signal. In this demonstration the first stream of information is 1111 1111 1110 0000, being the MSB the Direction value and the other 10 active bits the ADC converted information. On the second package of information sent to the micro, the word represents 0111 1111 1110 000, since in the second conversion the Direction signal was low "0", represented by the yellow in the graphic. To note that the Comp signal even though, it has every bit at "1", the ADC only has ten output bits that are connected to the Communication Block. The rest of the information is irrelevant. Second note, the CS1 signal works with the information from the last conversion done, not the one being done at the same time.
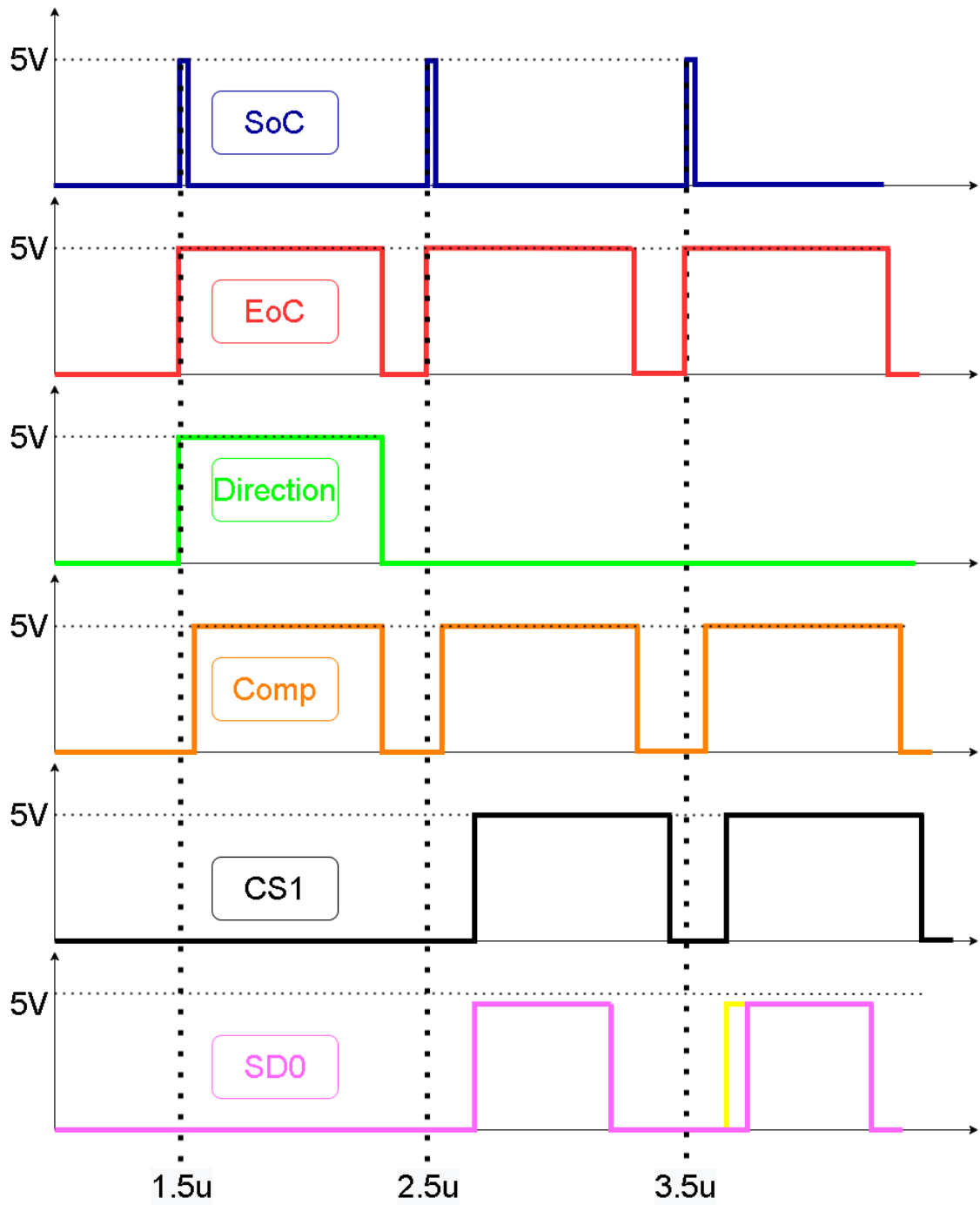
Figure 2.5: Acquisition System Demonstration

Chapter 3

Theoretical Background

This dissertation work is based on the electronic side of an acquisition system. As stated before the following objectives need to be fulfilled. Firstly, the most important features of this system are, implementing a low power consumption, and very small circuit design. This circuit will consist of.
Determining and redirecting the terminal of the scaffold with the highest voltage drop, (3.2). Amplifying that voltage, to decrease the amplitude resolution, (3.3). Lastly, converting that amplified value from analog to digital, (3.4).

3.1   Technology

The first topic that needs discussion is the technology that is going to be used in the ASIC. To implement an integrated circuit two major technologies can be used, individually or mixed. The first one is with the Bipolar Junction Transistor (BJT) and the second is the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Each one has its advantages and disadvantages, Table 3.1, e.g., for this comparison the BJT technology has a larger cutoff frequency, that can correspond to a larger bandwidth. On the other hand, the power consumption performance is lower for the MOSFET technology, which is the must important feature for the technology. Even though, from the analog viewpoint, BJT technology seems to display more advantages when compared to the MOSFET technology. However, if the comparison was made using a digital viewpoint the MOSFET side would have more advantages than disadvantages. Moreover, since the large-volume mixed-mode technology will be driven by the digital demand, the MOSFET, particularly, Complementary Metal Oxide Semiconductor Transistor (CMOS) is an obvious result as the technology of availability [2]. As so, the technology chosen is the submicron technology, 0.35μm CMOS technology.

Comparison Feature	BJT	MOSFET
Cutoff Frequency(fT)	100GHz	50GHz(0.25μ m)
Noise	Less $\frac{1}{f}$	More $\frac{1}{f}$
DC Range of Operation	9decades of exponential current versus V_{BE}	2-3 decades of square law behavior
Transconductance	Larger by 10X	Smaller by 10X
Small Signal Output Resistance	Slightly larger	Smaller for short channel
Switch Implementation	Poor	Good
Capacitor	Voltage dependent	More options
Performance/ Power Ratio	High	Low
Technology Improvement	Slower	Faster

Table 3.1: Comparison of BJT and MOSFET technology from an analog viewpoint [2]

3.2   Switch

There are many possibilities to develop a switch circuit with MOSFETs. The simpler one is just using one N-channel Metal Oxide Semiconductor (NMOS) or P-channel Metal Oxide Semiconductor (PMOS), with the right value of V_{DS} or V_{SD}, both components can be open or shorted, (Fig.3.1). Using the NMOS as an example, when the gate (G) voltage is "high" normally with the same voltage as the power supply, the transistor behaves like a closed switch, in the triode region, (Fig.3.1.B). Furthermore, its "on" resistance can be very small. However, when the gate (G) voltage drops from supply level to ground level, the transistor is cut off, behaving as an open switch, not letting any current through, 3.1.C, [33].
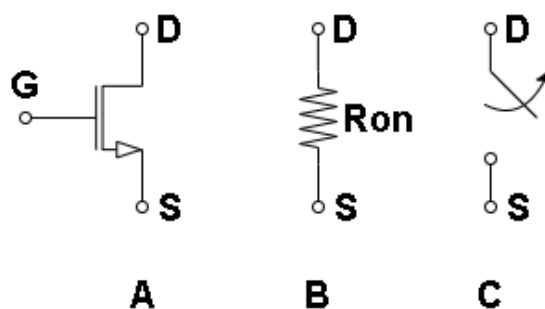

Figure 3.1: NMOS transistor as switch

Having this behavior makes the transistor, the best way to implement logic circuits. For example, if two transistors with the same polarity are used in series, it

results in a multiplication function AND gate. If the transistors are in parallel an addition is generated, OR gate.

3.2.1 NMOS as Switch

Assuming a schematic like, (Fig.3.2), that the gate (G) voltage is "high" and the drain (D) goes "high" as well, the transistor operates in the saturation region, $V_{DS} \geq V_{GS}$-V_T, for that moment resulting in a large current $i_D = \frac{1}{2}.K_N.(V_{DD} - V_S - V_T)^2; V_{DD} = 3.3V$.
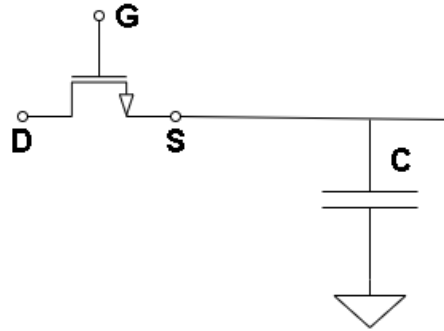
Figure 3.2: NMOS transistor as switch in PTL circuits

However, when the capacitor, C, starts to charge, Vc, V_T which is calculated by, $V_T = V_{T0} + \gamma \left(\sqrt{Vc + 2\Phi_f} - \sqrt{2\Phi_f} \right)$, grows too. Resulting in a decrease in the current i_D value. When V_C is equal to (V_{DD}-V_T) the i_D is zero and V_C does not go any higher. Resulting in a high output voltage (VOH) of $V_{DD} - V_T$. The NMOS transistor can recreate a low input voltage, 0V, at the output, just fine. However, it has some problems to recreate a high input voltage, V_{DD}, at the output. The PMOS transistor has the opposite behavior, has a good high but a poor low transmission. For these reasons, the NMOS or the PMOS transistors can work as switches for digital purposes, where the analog voltage value does not matter much. However, for analog applications, these switches have major problems. Since, when the transistor is "on" and the output voltage is stabilized, this voltage might not be equal to the input one.

3.2.2 Transmission Gate as Switch

A transmission gate is a combination of two complementary transistors, connected in parallel, (Fig.3.3). The NMOS and PMOS individually, had a few problems with the output voltage. However, if both transistors were combined in parallel, the results would be better for both cases.

Assuming that in (Fig.3.3) the (G) voltage is "high" and the ($\overline{G}$) is "low", the transmission gate is in "on" mode, the switch is shorted. Depending on the (X) voltage value, if this voltage is V_{DD} the NMOS is going to behave was state before, however this time, the PMOS transistor also operates with $V_{SG} = V_{DD}$ generating a

current $i_{DP} = \frac{1}{2}.K_P.(V_{DD} - |V_{TP}|)^2$. These two currents will charge the capacitor, C. When the voltage in the capacitor is equal to the $|V_{TP}|$ the PMOS will enter in triode mode, but the current will keep on flowing until the capacitor is all the way charged. Resulting in this way in a good high transmission. When the input voltage has a ground level, the PMOS and NMOS interchange roles. In short, with this solution, the static and dynamic performance of the switch improves greatly, however, the circuit increases in complexity, area, and capacitance [33].
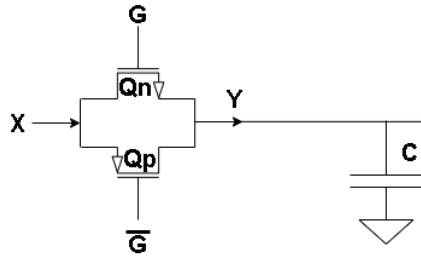
Figure 3.3: Transmission Gates as Switches

3.3 Amplifiers

To amplify one specific voltage many amplifiers can be used. However, not all can be utilized in this project. The three configurations studied, were the non inverting Operational Amplifier (Op-Amp) configuration, (Fig.3.4.B), the differential op-amp configuration, (Fig.3.4.C) and lastly the Instrumentation Amplifier (IA), (Fig.3.4.D). Every configuration results from the base block, the op-amp, (Fig.3.4.A). However, when this op-amp is wired up in feedback mode, a few configurations, with different gain equations, can surge.

3.3.1 Non Inverting Op-Amp

The non inverting operational amplifier is composed of an op-amp and two resistors. The input signal is connected to the positive input of the op-amp. Furthermore, since, there is no input offset voltage, the voltage drop between inputs, is 0V. Having high values of input impedance, the inputs of the op-amp do not flow current. As so the feedback connection represents a voltage divider, creating a relation between the input and output voltage values, gain, equation 3.4.

$$Vin_+ = Vout.\frac{R1}{R1 + R2} \tag{3.1}$$

$$\frac{Vout}{Vin_+} = \frac{R1 + R2}{R1} = 1 + \frac{R2}{R1} \tag{3.2}$$
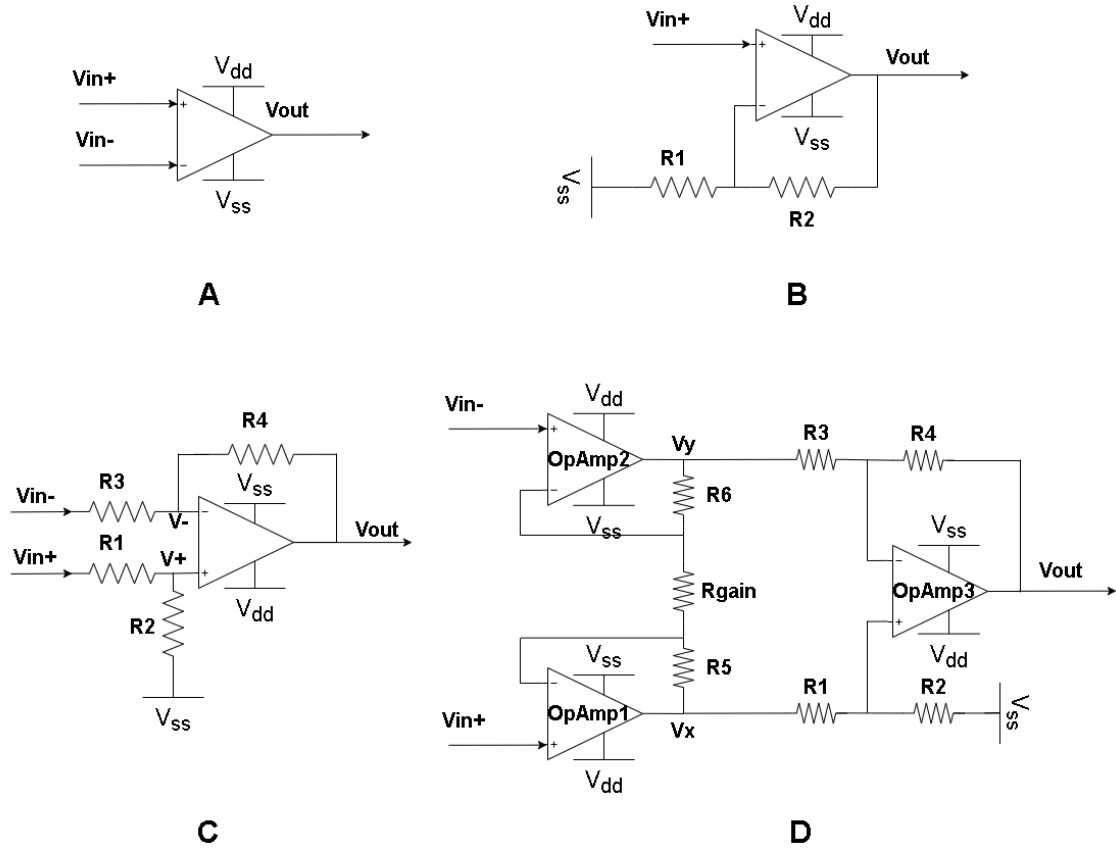
Figure 3.4: Opamps configurations

3.3.2 Differential Op-Amp

The differential amplifier is composed of an op-amp and four more resistors. This circuit amplifies the difference between two signals applied to be inputs. To make calculations easier, and to determine this circuit gain equation, a technique called superposition is used. This technique calculates the output voltage value depending on one input at a time, after both output values are determined and added, the final output value is determined.

Starting by calculating the $Vout_1$ from Vin_+.

$$V_+ = Vin_+ \frac{R2}{R1 + R2} \tag{3.3}$$

$$Vout_1 = (V_+)\frac{R3 + R4}{R3} = (Vin_+)\left(\frac{R2}{R1 + R2}\right)\left(\frac{R3 + R4}{R3}\right) \tag{3.4}$$

Calculating the $Vout_2$ from Vin_-.

$$Vout_2 = (Vin_-)\frac{-R4}{R3} \tag{3.5}$$

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$$V_{out} = (Vin_+) \left(\frac{R2}{R1 + R2} \right) \left(\frac{R3 + R4}{R3} \right) - (Vin_-) \frac{R4}{R3} \qquad (3.6)$$

If R1=R3 and R2=R4 the final gain equation is matched.

$$V_{out} = (Vin_+ - Vin_-) \frac{R4}{R3} \qquad (3.7)$$

This configuration only amplifies the differential part of the input signal, as so, it rejects the common-mode part [6].

3.3.3 Instrumentation Amplifier

The final configuration, the instrumentation amplifier, is composed of three op-amps and 7 resistors. This amplifier is a closed-loop gain block, that has a differential input and a single-ended output. This amplifier is an iteration of the differential op-amp, however, this one, has two op-amps has input stage and a differential op-amp has the second stage. This way, the IA, has lower noise and is capable of rejecting the common-mode dc voltage between the two lines. The IA is mainly used for data acquisition when the signals have very low-level output transducers in a noisy environment. However, in this project, the differences between inputs are not that low. Other uses can be, medical instrumentation, audio applications. In order to calculate the gain formula of this circuit, the technique used for the last component is going to be utilized again, superposition [13].

The relation between Vout and the outputs of the OpAmp1 and OpAmp2 are already known since it has been determined in the last component. If R1=R3 and R2=R4 the relation is, equation 3.8. Now if Vin_- is grounded, the other input of the OpAmp2 is also grounded, creating a voltage divider between Vx and Vin_+, equation 3.9.

$$V_{out_1} = (Vx - Vy) \frac{R4}{R3} \qquad (3.8)$$

$$Vx = (Vin_+) \left(1 + \frac{R5}{Rgain} \right) \qquad (3.9)$$

Ideally, the op-amps do not have any current flowing through the inputs, the current flowing in R5 and Rgain, goes directly to R6. This way using the Vx voltage is possible to determine Vy, equation 3.10. After the values, Vx and Vy are altered by their equivalent expressions, in the equation 3.8 and in order to simplify, R5=R6. Results the equation 3.11.

$$\frac{Vx}{R5 + Rgain} = \frac{Vy}{R6} \qquad (3.10)$$

$$Vy = -Vx \frac{R6}{R5 + Rgain}$$

$$Vout_1 = Vin_+ \left(\frac{R4}{R3}\right) \left(1 + \frac{2R5}{Rgain}\right) \qquad (3.11)$$

Now the Vin_+ goes grounded, the second stage, the differential stage, remains the equation as in 3.8, now with $Vout_2$ instead of $vout_1$, equation 3.12. Once again, with one input grounded, both inputs of the OpAmp1 are grounded, creating another voltage divider between Vy and Vin_-, equation 3.13.

$$Vout_2 = (Vx - Vy)\frac{R4}{R3} \qquad (3.12)$$

$$Vy = (Vin_-) \left(1 + \frac{R6}{Rgain}\right) \qquad (3.13)$$

Having the same value current passing through R6, Rgain, and R5. Vx can be determined by the following equation, 3.14. With the values of Vy and Vx altered, the final equation 3.15 determines $Vout_2$. Being once more, $Vout=Vout_1+Vout_2$, the gain of the IA can be shown as, 3.16.

$$\frac{Vy}{R6 + Rgain} = \frac{Vx}{R5} \qquad (3.14)$$

$$Vx = -Vy\frac{R5}{R6 + Rgain}$$

$$Vout_2 = -Vin_- \left(\frac{R4}{R3}\right) \left(1 + \frac{2R5}{Rgain}\right) \qquad (3.15)$$

$$Vout = (Vin_+ - Vin_-)\frac{R4}{R3} \left(1 + \frac{2R5}{Rgain}\right) \qquad (3.16)$$

3.4 ADC

In order to convert any information from analog to digital, an ADC needs to be implemented. As so, the context of the project has a major value in which ADC type to use. This component can be divided into three major groups moderate speed, high speed, and oversampling. The first two groups are characterized by their overall speed of conversion, the last is characterized by its conversion range, precision. Four different ADCs are going to be described, those ADCs are the Successive Approximation Register (SAR), Pipeline, Flash, and Sigma-Delta. The first two correspond to the moderate speed, the third is a high speed and the last one is an oversampling one [[23], [2], [15]].

3.4.1 SAR ADC

The Successive Approximation Register ADC compares an analog input voltage with a series of successively smaller voltages, these last voltages represent every single bit of the ADC. This ADC is composed of four blocks, a Sample and Hold, a Comparator, a SAR Logic Block, and lastly a DAC, (Fig.3.5).
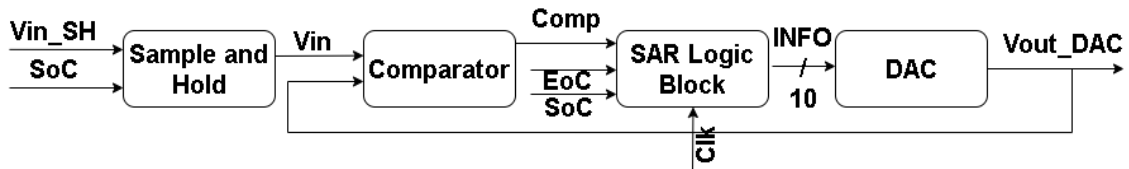
Figure 3.5: SAR ADC Block Diagram

After every comparison, the bit being tested adjusts its value to the result of the comparison. A demonstration of the Successive Approximation algorithm is displayed, (Fig.3.6), the input voltage is the red line and the yellow steps are the algorithm way to every cycle getting closer and closer to the target.
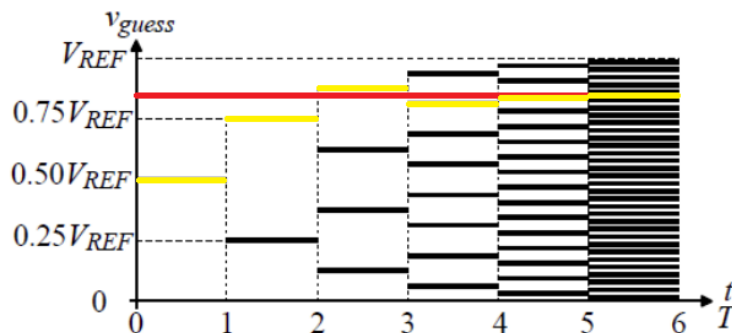
Figure 3.6: SAR Tracking Value

This type of ADC has advantages as, with a single comparator is possible to achieve high resolution, it has a small area used since it has an iterative topology. The power consumption of this type of ADC is quite low and it still permits under-sampling. A few disadvantages are, it requires N comparisons to produce N-bit resolution, the accuracy in the conversion depends on the DAC linearity and it requires considerable digital control circuitry.

3.4.2 Pipeline ADC

The next ADC type is the Pipeline one, which is also a moderate-speed ADC. This ADC divides the conversion into stages, each stage is composed of a Sample and Hold, an ADC, and a DAC. The analog input goes through the first stage where it passes in an ADC, saving the digital MSB. After that, the digital word passes a

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DAC and its value is subtracted to the original analog input. After being amplified, the analog value enters another stage, where the process repeats itself, (Fig.3.7).
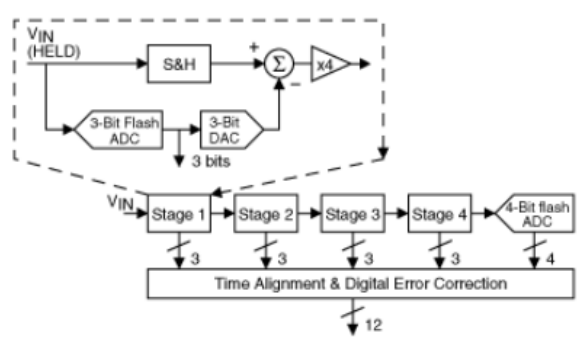
Figure 3.7: Pipeline ADC Block Diagram [20]

This type of ADC has advantages as it can achieve high resolution and dynamic range, it also is very fast after an initial latency of N cycles. The disadvantages are, its accuracy depends on the DAC linearity, also, its parallelism increases at the expense of power consumption and latency time. Lastly, because of the latency or pipeline delay, it is not suited to applications where the conversion results must be available immediately after the sample time.

3.4.3 Flash ADC

The flash or parallel ADC is a high-speed ADC, composed of 3 main blocks, a resistive voltage divider, a 2^N-1 comparators, and a 2^N-1 to N encoder, being N the number of bits to convert, (Fig.3.8). The voltage divider creates 2^N-1 values all with the same voltage drop. These voltages are connected directly to the comparators in the next stage, where the other input of the comparators is wired to the input voltage. After every comparator gives its results a "thermometer code" like response is displayed.

These ADC advantages are, being very fast, the conversion is done in one ADC clock cycle for every resolution. However, it requires 2^N-1 comparators for N bits conversion, resulting in a large area if N≥6. Extremely high power consumption and very expensive.

3.4.4 Delta-Sigma ADC

An oversampling ADC can be classified as, a straight-oversampling, a predictive oversampling, and lastly a noise-shaping oversampling, which corresponds to the Delta-Sigma ADC. This converter uses a noise-shaping modulator to reduce the in-band quantization noise to achieve a high degree of resolution. The modulator is the major difference between the speed-based and the over-sample-based ADCs. Because of this, the digital coding, the final stage in the conversion, is a decimation

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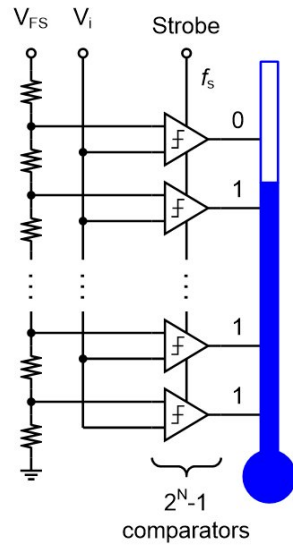
Figure 3.8: Flash ADC Block Diagram [28]

filter instead of a digital processor. General block diagram of an oversampled ADC, (Fig.3.9).
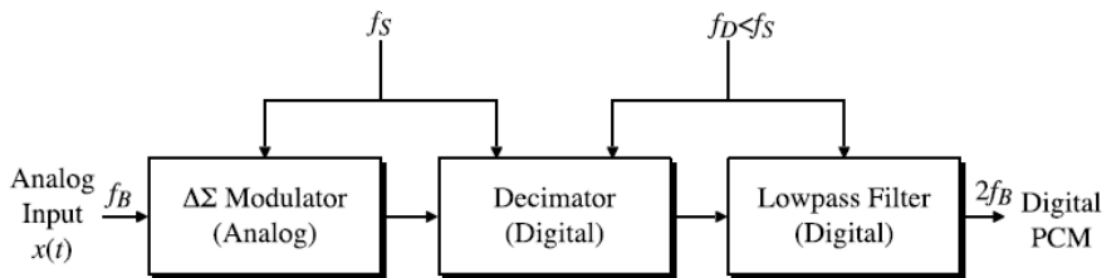
Figure 3.9: Oversampled ADC Block Diagram [2]

This ADC is very compatible with Very large-scale integration (VLSI) technology because most of the converter is digital, it has a high resolution. Moreover, the oversampling reduces the requirements for anti-aliasing filtering. However, these types of ADCs, have a latency much greater than the other architectures and they are difficult to model and simulate.

Chapter 4

Measurement Block

The Measurement Block was developed because both terminals of the load in the H-bridge can be stimulated. When the current flows from left to right, (Fig.4.1.A), the left terminal, marked as v1, has a positive voltage and the right terminal, marked as v2, is basically grounded. On the other hand, when the current flows in the opposite way, right to left, (Fig.4.1.B), the terminals voltages swap magnitude.

Using a non-inverting operational amplifier, to amplify all possible simulations of the scaffold would be impossible. Since the circuit only has one input point and after the connection between points, v1 or v2 with the input of the op-amp was done. One way of current flowing would result in a grounded input voltage, which means the whole system would only work for half the experiments.
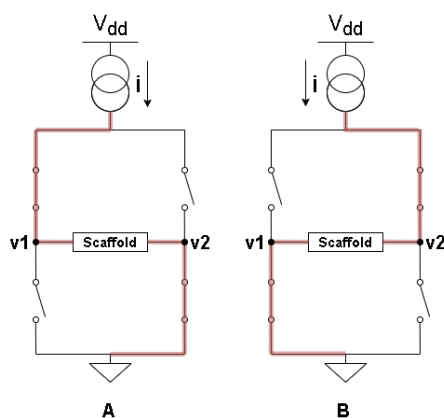
Figure 4.1: H-Bridge

4.1   Circuits/Schematics

This block is composed of three simple circuits, (Fig.4.2), a voltage switch, using primarily transmission gates, a buffer, in order to preserve the chosen voltage and to isolate the switch circuit from the op-amp, and lastly, the non-inverting op-amp, to amplify the voltage that will be converted in the next block, ADC, increasing the resolution and in contrast, decreasing the conversion errors.
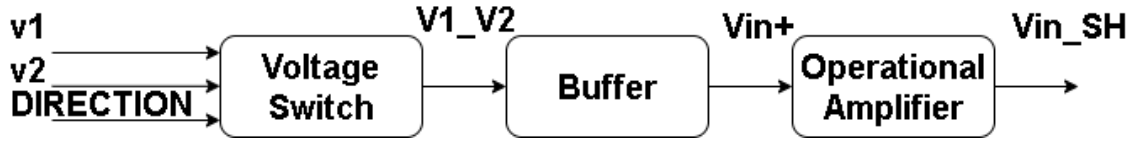
Figure 4.2: Measurement Block

4.1.1 Voltage Switch

Once more, the mission of this block is to determine which terminal of the load is being tested, letting it pass through the amplifier and conversion system. One possible way to do it is, to use an op-amp as a comparator, to determine which terminal of the scaffold has the largest voltage, choosing which terminal to use. The previous idea was not needed because the overall system, already has a signal, DIRECTION, that determines which way the current will flow in the H-bridge, simplifying the circuit. In order to design a Voltage Switch, two transmission gates and a logic NOT gate were used, (Fig.4.3.B).
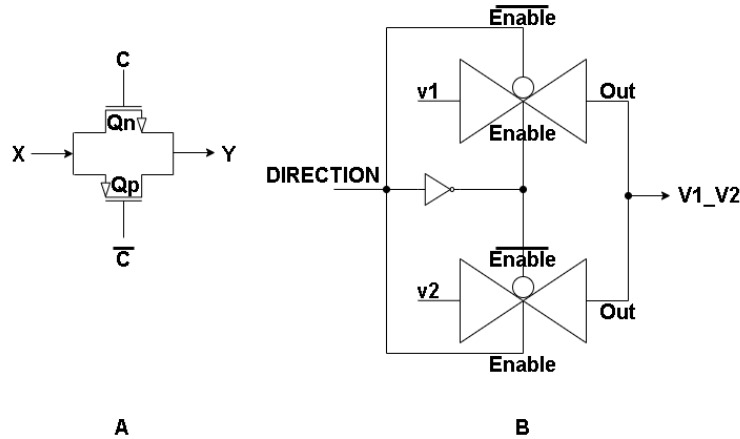
Figure 4.3: Transmission Gate & Voltage Switch

A transmission gate is composed of a pair of complementary transistors connected in parallel, (Fig.4.3.A). Depending on the value of Vgs/Vsg of the MOS pair, the circuit will let the signal through or not, acting as an excellent switch, providing bidirectional current flow. Moreover, it exhibits an on-resistance that remains almost constant for wide ranges of input voltage. These characteristics make the transmission gate not only an excellent switch in digital applications but also an excellent analog switch [33].

The final circuit has two transmission gates and a logic NOT gate, in which the input signal is the DIRECTION signal. This way, it is possible to either pass through the voltage marked as v1 or v2, in the H-Bridge, (Fig.4.3). This value that chooses the path is the DIRECTION signal, resulting in the truth table displayed beneath.

DIRECTION	V1_V2
0	v2
1	v1

Table 4.1: Voltage Switch Truth table

4.1.2 Operational Amplifier

The choice justifying the non inverting amplifier is. Since the dc voltages in both terminals are not the same, to use the IA it would have to be on single mode. Moreover, using the IA in a 0 to 5V environment is not the wisest decision, since the amplifier might need negative voltages to work properly. Deciding between the non inverting amplifier and the differential amplifier, was easy. Both amplifiers would theoretically "do the job", however, since one uses four resistances and the other only uses two, the choice was to proceed with the non inverting amplifier.

Before developing the configuration, the operational amplifier had to be designed. A component with certain specific features. The most important ones were, a near rail-to-rail input and output range, as well as a fast slew-rate and quite stable response, plus, a relatively low output resistance value.

To create an amplifier with total input flexibility, a complementary differential pair is required. Primarily, because the NMOS and PMOS, cannot work as intended, in the saturation region, for every input voltage. Moreover, if the input and output voltage ranges are not as close as perfect (rail-to-rail) the buffer will change the voltage value coming from the load, creating an error in the whole system. The second stage is a cascode stage to sum the currents output of both NMOS and PMOS input stage, respectively. At last is the output stage of the amplifier, which is a push-pull, class AB amplifier. This way, the rail-to-rail output range is practically achieved. Moreover, the output resistance decays from some MΩ, at the output of the second stage to a few KΩ at the output of the third stage, a value considered low for the type of technology used. The circuit also has a self-bias part, that biases the whole circuit, this bias is formed by two PMOS, two resistors, and an NMOS. The resistor and capacitor between the output NMOS and PMOS, gates and drains, have the purpose of compensating/stabilizing the op-amp [19]. The slew rate normally is defined as the relation between the input current and the output capacitor. However, in this circuit, since there is no current bias network at the output stage, the current is highly dependent on the size of the output transistors and not dependent on the input current. Concluding that, the slew rate for this circuit can be altered by the dimensions of the output NMOS and PMOS, (Fig.4.4).

For this op-amp, the resistor, RC_C, and capacitor, C_C have the values of 2KΩ and 1.5pF respectively, which ensures that the op-amp is stable. Having a phase margin value of about 70°.
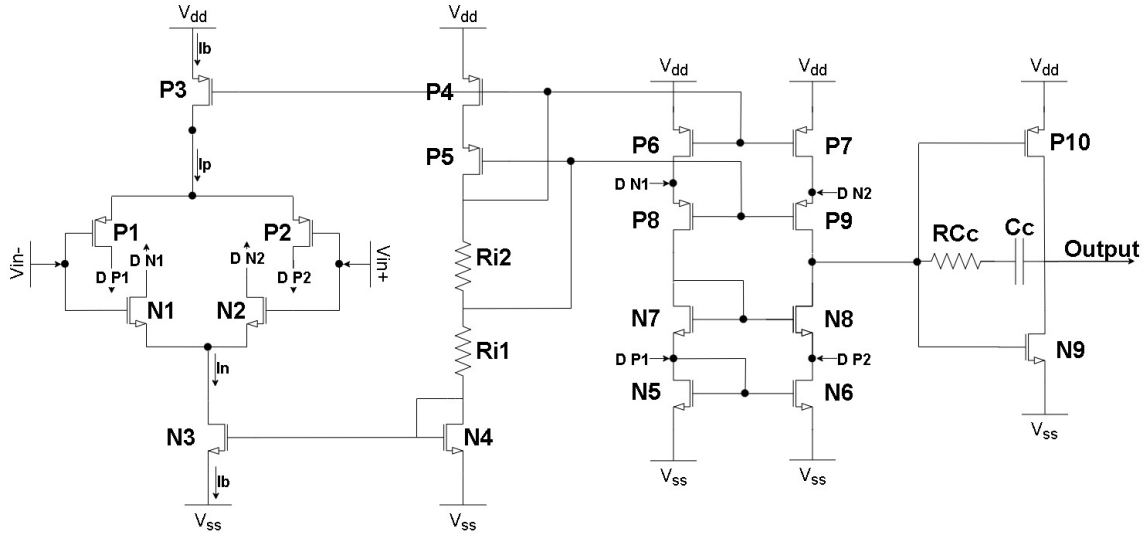
Figure 4.4: Operational Amplifier

In this system four different op-amps will be developed, two to be buffers, one that will represent a gain op-amp (Fig.4.5), and the last will be a comparator. Since all these components are going to be used in different points of the system, the overall specifications will be different as well. As so, all the MOSFET dimensions, the resistors RC_C and capacitors C_C might have different values from each other.

After having the circuit designed it is required to stipulate some initial specifications for the op-amp, Table 4.2, in this case the specifications are as follows.

Buffer Circuit	Specifications
Gain	3000V/V
Slew Rate	150V/us
Input range @3rd stage	[0;5]V
Output range @2nd stage	[0.6;4]V
Output range @3rd stage	[0;5]V
C_L	1.5pF
GB	150MHz
P_{diss}	<5mW

Table 4.2: Operational Amplifier Circuit Specifications

Some of these values are arbitrary as we do not know for sure the minimum value, e.g. the gain and unity-gain bandwidth, GB, is quite high. On the other hand, since the clock signal has a frequency of 20MHz, i.e. 50ns for a cycle, the slew rate will need to be probably even higher than the 150V/us established before. Because of the need for the buffer to go from 0V to 5V in that time frame, perhaps in half that time, just to be reliable.

Now is possible to calculate the dimensions (width and length) of every MOSFET. These dimensions are the only variables available to use. Following CMOS

Analog Circuit Design [2], as an example, the following three equations will be very useful, because they relate all the variables that are going to be needed.

$$I_D = \frac{K}{2}\frac{W}{L}(Vgs - Vt)^2 \tag{4.1}$$

$$gm = \sqrt{2K\frac{W}{L}I_D} \tag{4.2}$$

$$V_{DS_{SAT}} = \sqrt{\frac{2I_D}{k\frac{W}{L}}} \tag{4.3}$$

The first step in these calculations is to determine the minimum value for the "tail current" (Id_{P3}), from the values of the slew rate and the capacitor C_L.

$$Id_{P3} = SR.C_L \tag{4.4}$$

Utilizing the unity-gain bandwidth (GB) and once more, the capacitor (C_L), is possible to determine the transconductance (gm) of the complementary differential pair input MOSFETs.

$$GB = \frac{gm}{C_L} \tag{4.5}$$

Using the equation in 4.2, is possible to determine the S_{P1}, S_{P2}, S_{N1} and S_{N2}.

Being the MOSFET N3 connected directly to the input NMOS pair and also the ground, this MOSFET will characterize the minimum input voltage (Vin_{min}). Taking into account the Vds_{SAT} determination

$$Vds_{SAT} = Vin_{min} - V_{SS} - \sqrt{\frac{2Id_{N3}}{knS_{N1}}} + Vt_{max} \tag{4.6}$$

and the equation in 4.3, the MOSFET S_{N3} can be determined.

For the same reason as before, being connected to the input differential pair and the V_{DD}, the MOSFET P3, is responsible for the maximum input voltage. Once more, determining Vds_{SAT} is imperative. After using again the equation in 4.3 the S_{P3} is calculated.

$$Vds_{SAT} = V_{DD} - Vin_{max} - \sqrt{\frac{2Id_{P3}}{kpS_{P1}}} - Vt_{max} \tag{4.7}$$

If the maximum output voltage @2_{nd} stage is 4V, the Vds_{SAT} for the MOSFETs $P4$, $P5$, $P6$, $P7$, $P8$, and $P9$ is 0.5V, assuming they will have the same dimensions. Using the equation 4.3, the values of the MOSFETs are established.

The same method can be used to determine the dimensions for the NMOS of the cascode ($N7$, $N8$, $N9$ and $N10$). If the minimum output voltage @2_{nd} is 0.6V, the Vds_{SAT} will be 0.3V. Combining with the equation 4.3, the last part of the cascode is known.

To design the self-bias circuit MOSFET (S_{N4}) a relation of one-to-one (1:1) between the S_{N3} and S_{N4} was used.

The resistor values can be easily calculated because the voltage at their terminals and the current passing through them are already known.

Ri2:

$$Vds_{SAT} = \sqrt{\frac{2 * Id_{P5}}{kp * \left(\frac{W}{L}\right)_{P5}}} = \sqrt{\frac{2 * 225 * 10^{-6}}{19 * 10^{-6} * 105}} \equiv 0.5V \tag{4.8}$$

$$Ri2 = \frac{Vds_{SAT}}{Id_{P5}} = \frac{0.5}{225 * 10^{-6}} \equiv 2K\Omega \tag{4.9}$$

Ri1:

$$Vds_{SAT} = \sqrt{\frac{2 * Id_{N4}}{kn * \left(\frac{W}{L}\right)_{N4}}} = \sqrt{\frac{2 * 225 * 10^{-6}}{63 * 10^{-6} * 88}} \equiv 0.3V \tag{4.10}$$

$$Ri1 = \frac{5 - (0.5 * 3 + 0.3)}{250 * 10^{-6}} \equiv 13K\Omega \tag{4.11}$$

The last two components to design are the S_{P10}, which is responsible for the maximum output voltage (@3_{rd} stage) and the S_{N9}, responsible for the minimum output voltage (@3_{rd} stage). For this last stage the current established, to have a reliable slew rate, was 350uA. Knowing that the voltage of both MOSFETs Vds_{SAT} needs to be 2.5V using the equation 4.3, results in the S_{P10} and S_{N9} dimensions.

After having the calculations done, was time to implement the op-amp and adjust the previous values. As a reminder, the calculations were done making use of some variables, as kn, kp, Vt_{max}. These variables were acquired by testing, in the Cadence software, the MOSFETs that are going to be used. As so, it is expected for these values to be only for guidance. After some iterations, the final values from the op-amp are as followed, Table 4.1.2.

These values achieved the specifications established before as will be explained in further detail in the Results part of this chapter.
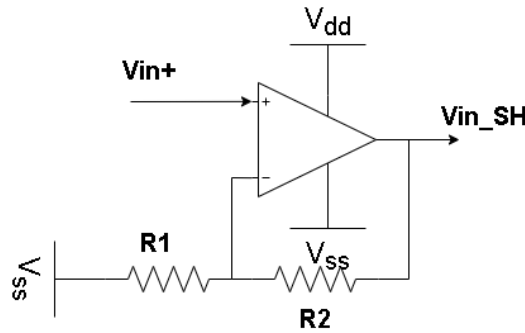
Figure 4.5: Non Inverting Op-Amp

As explained before, in chapter 2, NeuralStimSpinal, the load impedance value is not known for sure, any value between 1KΩ and 100KΩ could be expected. Even though the impedance value is such an unknown, a value needs to be chosen because otherwise, it is impossible to implement the non inverting op-amp. For this project, the load impedance has a default value of 10kΩ. Having a maximum current of

Mosfet	Dimensions ($\frac{W}{L}$)
N1	43
N2	43
P1	86
P2	86
N3	16
P3	214

Mosfet	Dimensions ($\frac{W}{L}$)
N4	18
Ri1	7K
Ri2	3k
P4	180
P5	180
N5	107
N6	107
N7	107
N8	107
P6	180
P7	180
P8	180
P9	180

Mosfet	Dimensions ($\frac{W}{L}$)
N9	7
P10	10
RCc	2K
Cc	1.5pF

Table 4.3: Operational Amplifier MOSFETs Dimensions

200uA, system specifications, and a Rload of 10KΩ, the voltage created is 2V, which means the maximum gain value possible without saturation by the op-amp is 2.5 times. This solution does not resolve all the problems directly, i.e. if the load impedance is larger than 10kΩ for the maximum current, 200uA, the voltage will be larger than the 2V, eventually causing saturation. In this situation the way to resolve the problem is, to decrease the current to a value that does not saturate the output of the amplifier. That way the impedance can be calculated anyways, without any significant increase in the error.

Having in the last stage a class AB amplifier results in the output resistance of the whole circuit to decrease. Because previously the output resistance was calculated taking into account various MOSFETs rds, such as.

$$R_{out} = Rds_{PMOS}||Rds_{NMOS};$$

$$R_{PMOS} = Rds_{P9} + (Rds_{P7}||[Rds_{N2} + Rds_{N3}]);$$

$$R_{NMOS} = Rds_{N8} + (Rds_{N6}||[Rds_{P2} + Rds_{P3}]);$$

The resistance output of the class AB amplifier can be calculated by, decreasing the resistance output significantly.

$$R_{out} = Rds_{P10}||Rds_{N9};$$

With the help of the software itself, it is possible to determine what these values are for the entire range, making it much easier to choose the lowest resistor value accordingly. Being the non-inverting configuration gain the one beneath.

$$Av = 1 + \frac{R2}{R1} \tag{4.12}$$

The resistors values chosen need to have a relation of, R2=1.5*R2. Note, the values of the resistors will be determined in the Results subsection of this chapter.

4.1.3 Buffer

This component, (Fig.4.6), was used in this point of the system, to, isolate the circuits before this one (stimulation circuit and voltage switch) from the circuits that will amplify, convert and send information. The buffer was developed with certain specific features. The most important ones were, a near rail-to-rail input and output range, as well as a fast slew-rate and quite stable response, plus, a relatively low output resistance value.
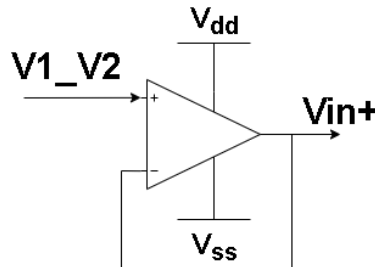
Figure 4.6: Buffer

For this configuration the operational amplifier explained in the last section was used.

4.2 Results

Once the schematics have already been design, the next task is to simulate the circuits. All of the blocks were tested in an ideal environment because in this stage of the work the most important is a proof of concept and overall behavior of all the circuits individually. Instead of an overall system good behavior. Note that, all the figures displayed in the Results sections, in this document were done by saving

the signals arrays and using the Matlab software, to better and cleaner show the graphics.

4.2.1 Voltage Switch

This test is one of the simpler ones, the way the simulation were approached was, having signals v1 and v2, with two different voltages and switching the DIRECTION signal as fast as needed, (Fig.4.7). After around 800ns, which correlates to 16 cycles of 50ns, i.e. one conversion in the ADC.
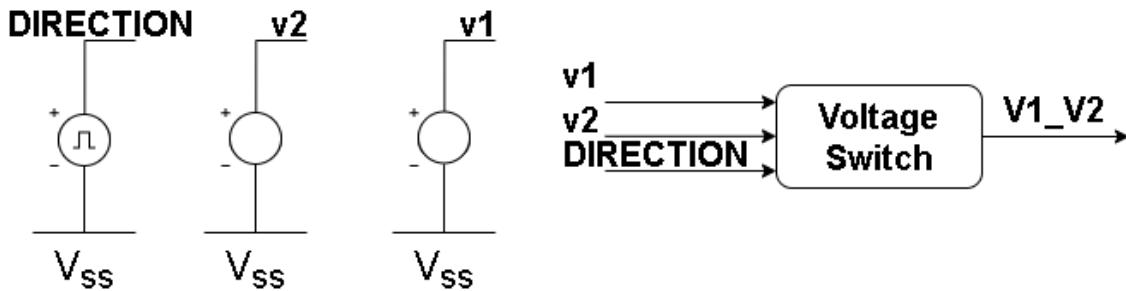
Figure 4.7: Voltage Switch Set-Up

As can be seen in the graphic beneath (Fig.4.8), the inputs are 1V and 0V, for v1 and v2, respectively. The DIRECTION and V1_V2 signals behavior are as expected and can be seen in Table 4.1.

Figure 4.8: Test of Voltage Switch

To determine the rising edge and falling edge response times, a zoom was performed, (Fig.4.9). The DIRECTION signal has a 1ns for both rising and falling edges, the circuit response time is about 0.22ns for both transitions.

Figure 4.9: Test of Voltage Switch with Zoom

4.2.2 Operational Amplifier

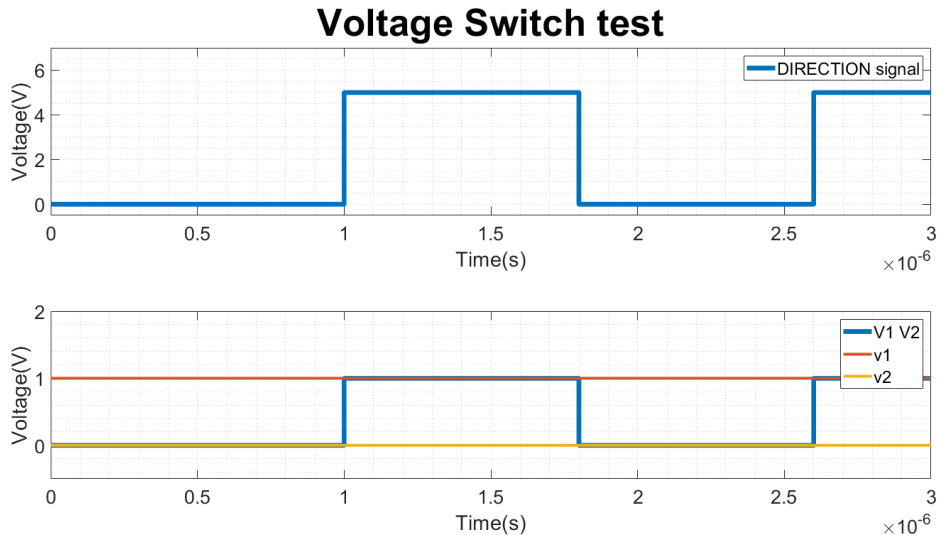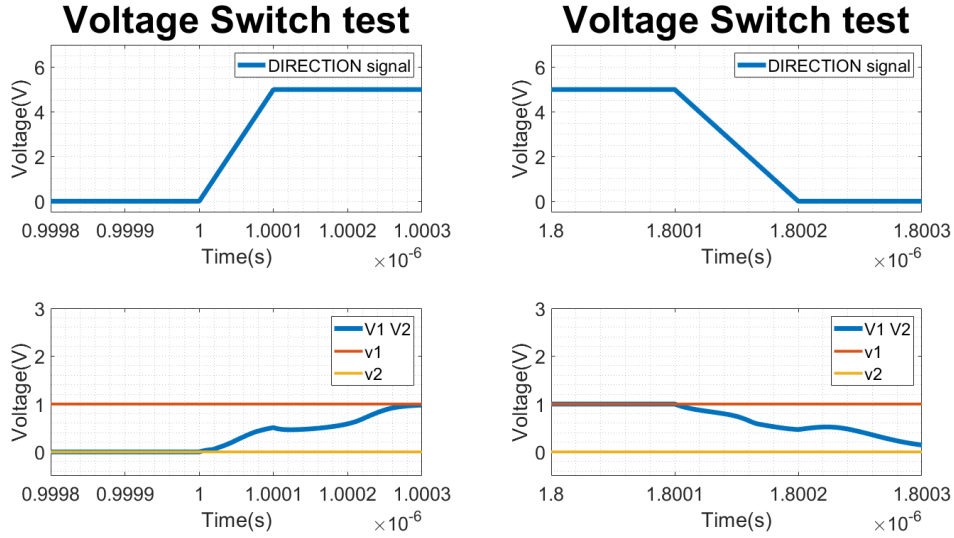In this subsection, the tests are related to the op-amp, Input Common Mode Range (ICMR), gain, phase margin, slew rate, and to the op-amp itself.

The op-amp results are shown in the table 4.4, beneath.

Voffset(V)	ICMR(V)	Gain(dB)	PM(^{o})	SR(V/us)
30.86u	[480u;4.99]	115.3	74	180

Table 4.4: Op-Amp characteristics

The offset variable is measured with the negative input connected to the output, this way it is possible to determine the intrinsic feedback value of the op-amp. This value is used for every test in which the op-amp does not have a feedback connection, e.g. the gain and phase margin tests. The rest of the simulations, as input common-mode range and slew rate, are done with the feedback connection. The ICMR does reflect the specifications, making the op-amp input and output ranges, rail-to-rail. As for the gain and the slew rate, it exceeds the expectations because it was tweaked to do so, to have the rightful values for the layout, further explained in the Results chapter.

Moreover, the simulations done for this block are, measuring the resistance output, determining the input/output range,and analyzing the response in frequency, gain, and phase. A test set-up used was the one below, (Fig.4.10), many different values, like offset voltage, the Rout (output resistance), also the ICMR analyses. The set-up is a simple, negative feedback connection.
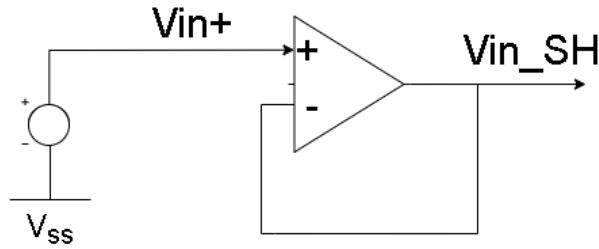
Figure 4.10: Rout Op-Amp Set-Up

In the first test, as stated previously, the resistance was measured using the Cadence software, figure below. As can be observed (Fig.4.11), the NMOS rds is much bigger than the rds of the PMOS. However the parallel of them both results in a quite smaller output resistance. Having a maximum value of about 60kΩ, which is going to be used as the R1 value, R2 is going to be 90KΩ.
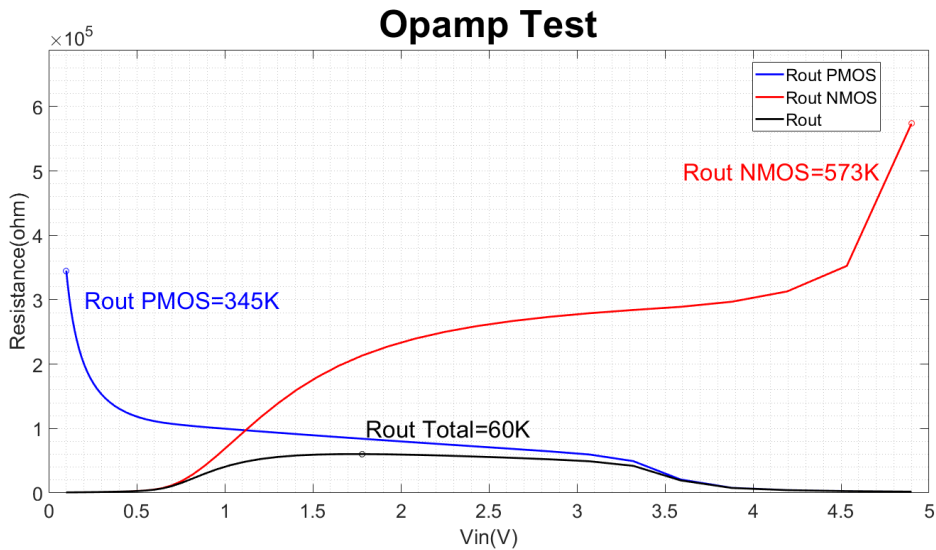

Figure 4.11: Rout Op-Amp

For the second simulation, the input signal is a voltage ramp between 0 and 2V, which should respond with a 0 to 5V ramp. Once more, the output voltage values are not as perfect as the input, however, the total working range is about 98% of the full range, (Fig.4.12).

The result is expected because of the way the non inverting op-amp is connected. Having a resistor in the feedback path provokes a loss in voltage around the rails. The lower the values of the resistors are, the more it shows. After testing different values, for the lowest resistor, it can be easily detected that for values lower than 60kΩ the overall error is quite high. Moreover for values larger than the 60KΩ the ratio between the growth of the resistor value and the decrease in the error starts to be uneven. Concluding that the resistor value chosen has the best value by error, trade-off.
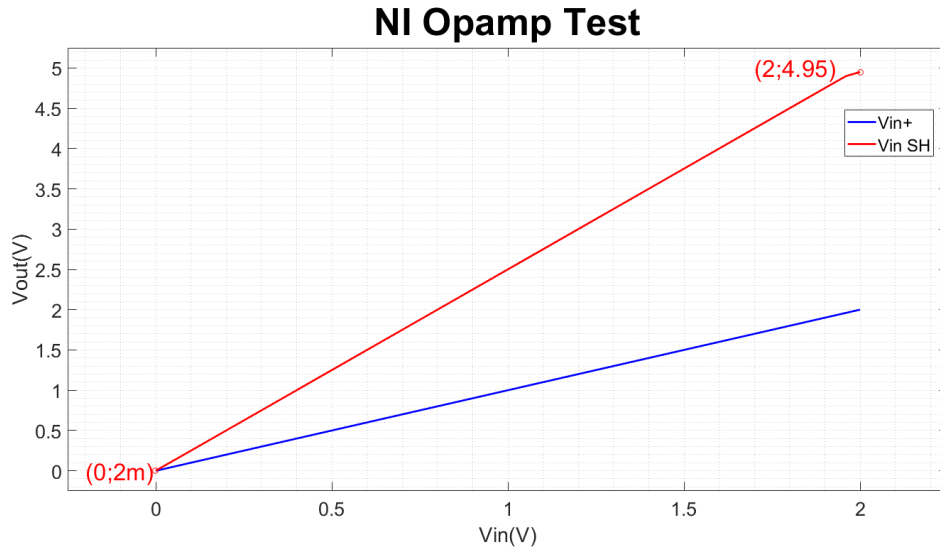
31

Figure 4.12: ICMR NI Op-Amp

For the last test, a new set-up was needed to be used, this way stimulating both inputs of the op-amp. To the positive input, Vin+, was applied a 2.5V dc and 0.5V ac. The other input, the negative, was applied with 2.5V dc and -0.5V ac. Having the Cadence tools to use, it is possible to test and determine the op-amps gain and phase margin, (Fig.4.13).
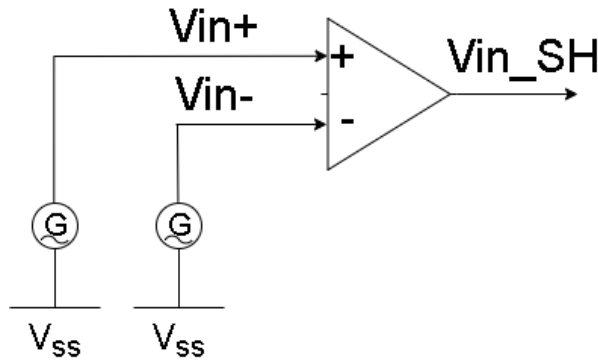
Figure 4.13: Gain/Phase Margin Set-Up Test

In order to test if a circuit is stable or not the following needs to happen. "At the frequency where the loop gain is unity, the phase shift must be greater than 0°" [2]. This phrase is justified by the equations.

$$Arg[-A(j\omega 0dB).F(j\omega 0dB)] = Arg[L(j\omega 0dB)] > 0° \quad (4.13)$$

$$|A(j\omega 0dB).F(j\omega 0dB)| = |L(j\omega 0dB)| = 1$$

The behavior observed in, (Fig.4.14), is that the maximum gain, at low frequencies, is about 76dB, the cutoff frequency is of 4.7KHz, resulting in a Band Width

of 29.7MHz, which is the exact frequency value to determine the phase margin. In this case, since the phase starts at 0° the phase can be calculated by,

$$\Phi_M = Arg[-A(j\omega 0dB).F(j\omega 0dB)] = Arg[L(j\omega 0dB)] \qquad (4.14)$$

$$\Phi_M = 360° - 180° - 109° = 71°$$
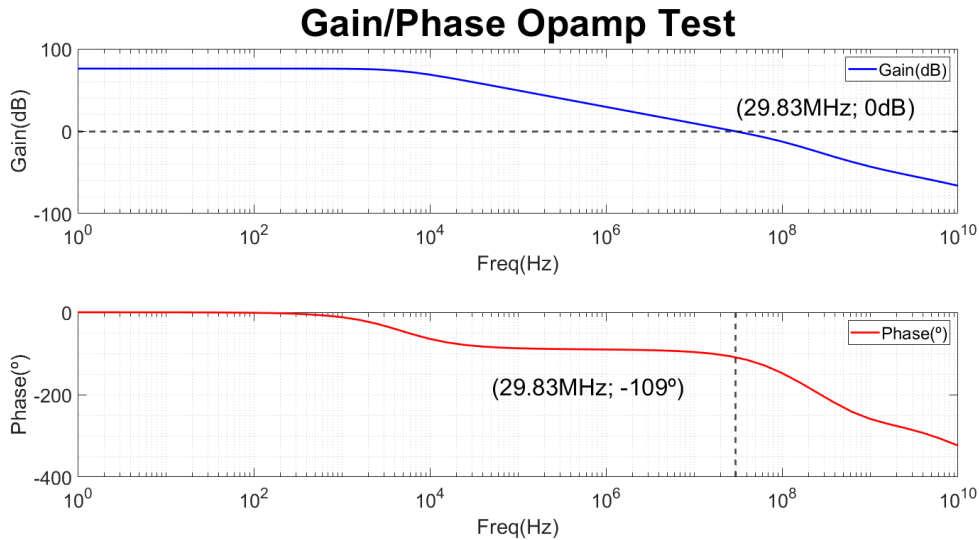
Figure 4.14: Gain/Phase Margin Test

The op-amp is stable for a single loop with negative feedback. However, being stable is not the only information this phase margin value provides. It is also capable of revealing how good of a response the op-amp will have. A good response is one that quickly reaches its final value. Therefore, we see that phase margin should be at least 45° and preferably 60° or larger, (Fig.4.15), [2]. Having the op-amp with a phase margin of 71° is very positive.
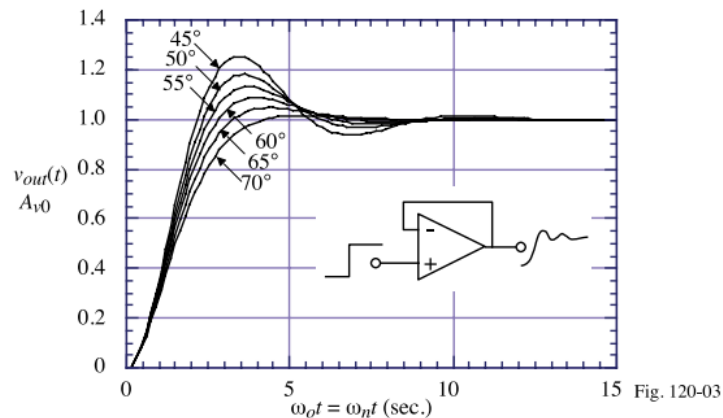
Figure 4.15: Step response vs Phase Margin [2]

4.2.3 Buffer

As said before, since the op-amp used for this block is the same used for the buffer, the results shown before can be valid here too.

This simulation revolved around having a ramp as the input voltage signal, from 0 to 2V, resulting in the same ramp-like output, (Fig.4.16).
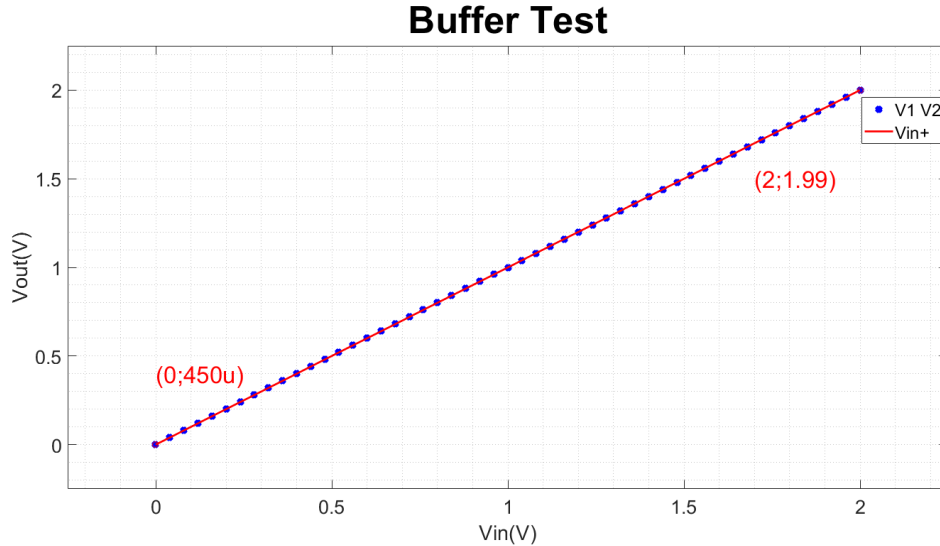
Figure 4.16: ICMR Buffer

4.2.4 Measurement Block

Lastly, after simulating every block individually, is time for the whole block test. This test is composed of two inputs signals with different voltages values and the DIRECTION signal switching at 800ns, (Fig.4.17).
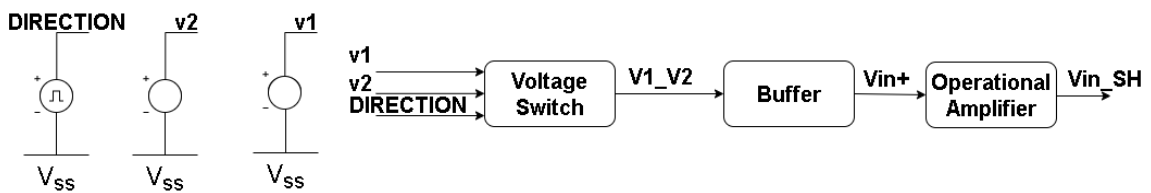
Figure 4.17: Measurement Block Set-Up

V1 signal has 0V, and V2 signal has 1.5V. The output of the first block, Voltage Switch, V1_V2 signal, is switching between 5mV and 1.499V, as expected. The second block, the buffer, has the input leading the output signal, once more, as expected. In the last block, the non-inverting op-amp, the Vin+ signal is multiplied by 2.5 times, resulting in a rectangular wave shifting between 92mV and 3.749V, (Fig.4.18). All the blocks worked properly individually and as a whole, which means the latency between blocks does not interfere.
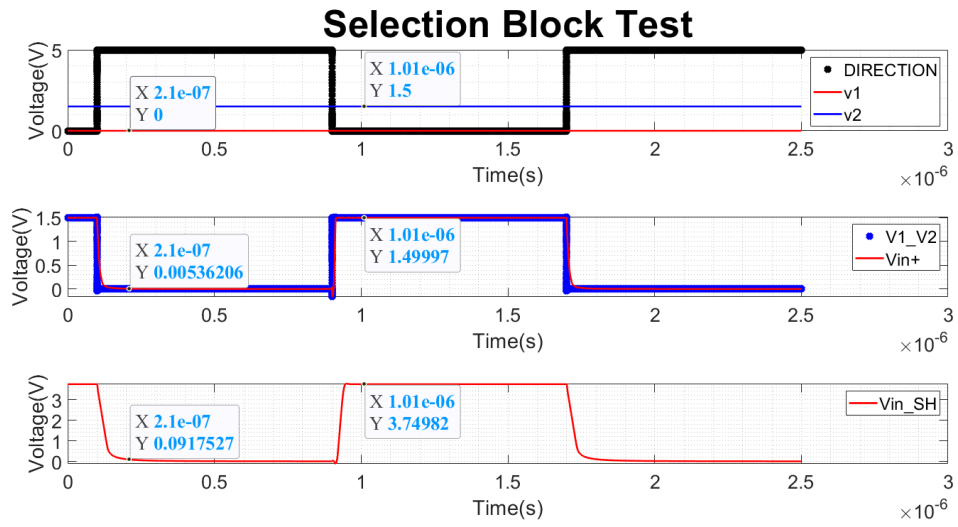
Figure 4.18: Test of Measurement Block

Chapter 5

ADC Block

When considering the various types of ADCs to develop, many criteria need to be counted for, e.g. the conversion time, the number of cycles needed to make a full conversion, the overall complexity of the ADC circuit, and the amount of space it will occupy. For this project, the best choice was to implement a SAR, successive approximation registers ADC. Even though the circuit to develop such ADC is not the simplest one, being a recursive type of ADC, which means the overall circuit space needed is smaller. Also, it is one of the most cost-efficient ADCs, having only the comparator used, as the main power consumption.

5.1 Circuits/Schematics

The main blocks to develop the ADC are a sample and hold block so that the input voltage that will be converted does not change during conversion. A comparator, to determine if the input voltages are larger or lower than the output of the DAC value. The next block is the SAR logic block, which can be composed of many D-flip flops that will create all the signals for the bits. The last block needed is a DAC of the same size. These blocks can be seen in the figure beneath, (Fig.5.1).

Figure 5.1: ADC Block Diagram

5.1.1 Sample and Hold

The Sample and Hold circuit, as said before, has the objective of keeping a certain input voltage constant for the entire time of conversion. This circuit is not the most complex, utilizing two sets of transmission gates, which were already used and explained in the subsection 4.1.1.

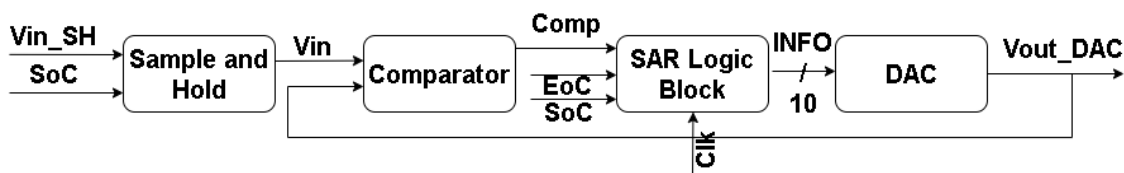This block besides looking fairly simple, which it is, went through some development iterations, as can be seen by the second pair of complementary MOSFETs, to reduce the noise [33].
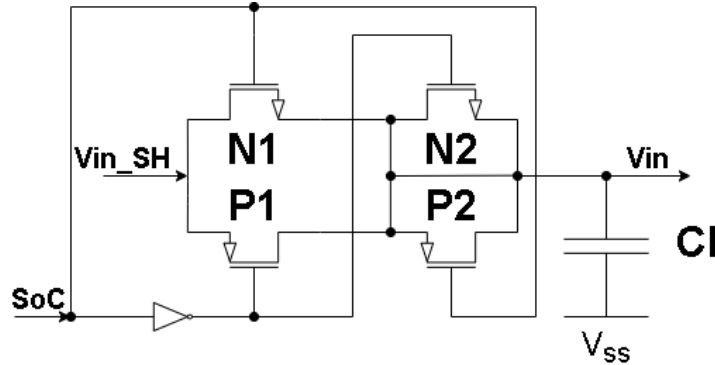

Figure 5.2: Sample and Hold Schematic

When the circuit is on sampling mode, the transmission gates will charge the capacitor with an equal value of input voltage. After that state, the circuit will enter a holding time, which means, the capacitor is now disconnected from the rest of the charging circuit and ideally does not discharge, keeping the voltage constant. This small circuit is so important for the whole ADC block because when the ADC is doing its conversion the value it will compare to, is the output voltage value of the Sample and Hold. If this value is not constant the conversion will not be accurate and reliable. The output voltage will directly connect to the negative input of the comparator, which has an approximately infinite resistance due to the technology used (CMOS).

In order to design the switch, NMOS, and PMOS, dimensions. First, a theoretical determination of the "on" resistance of each MOSFET was needed. The equation used was the following.

$$R = \frac{1}{K\frac{W}{L}(V_{GS} - V_T)} \qquad (5.1)$$

The NMOS had a relation of 14.5, $10\mu\text{m}/0.7\mu$ and the PMOS values were doubled, 29, $20\mu\text{m}/0.7\mu$. For these dimensions, the corresponding "on" resistances were, 692Ω and 811Ω, respectively.

Lastly using a capacitor of 10pF, the time constant is lower than 15ns, having about 50ns for the sampling mode. The Sample and Hold should have a response fast enough and should be reliable enough to implement the ADC.

5.1.2 Comparator

The comparator has the role of analyzing both inputs and depending on those values, output a 0V, if negative input is larger than positive input, or a 5V value, if otherwise. The inputs are, the Sample and Hold output value, the target initial

value, as negative input, and the positive input is the value outputting of the DAC. Without the comparator, this type of ADC cannot work because it is not able to seek the targetted value.

Once more, this block, (Fig.5.3), was an iteration of the op-amp done and explained in the previous chapter, 3. This time though, the most important features are not the same as before. Since the comparator output value links directly to the SAR logic block, which is a digital component, the voltage itself does not matter as much. A voltage larger than V_{DD} divided by 2, 2.5V, is seen as a "1" and otherwise, a voltage lower than 2.5V, is a "0". So, the output of this comparator does not need the full V_{DD} V_{SS} range. Excluding this way, the third stage of the op-amp. This development helps to reduce the used space, in about $8\mu m^2$, or less 42% of the area used, mainly because of the capacitor, Cl, value. The power consumption was reduced by 1.2mW, or less than 28% of power being consumed, both these features are very important to the whole project.
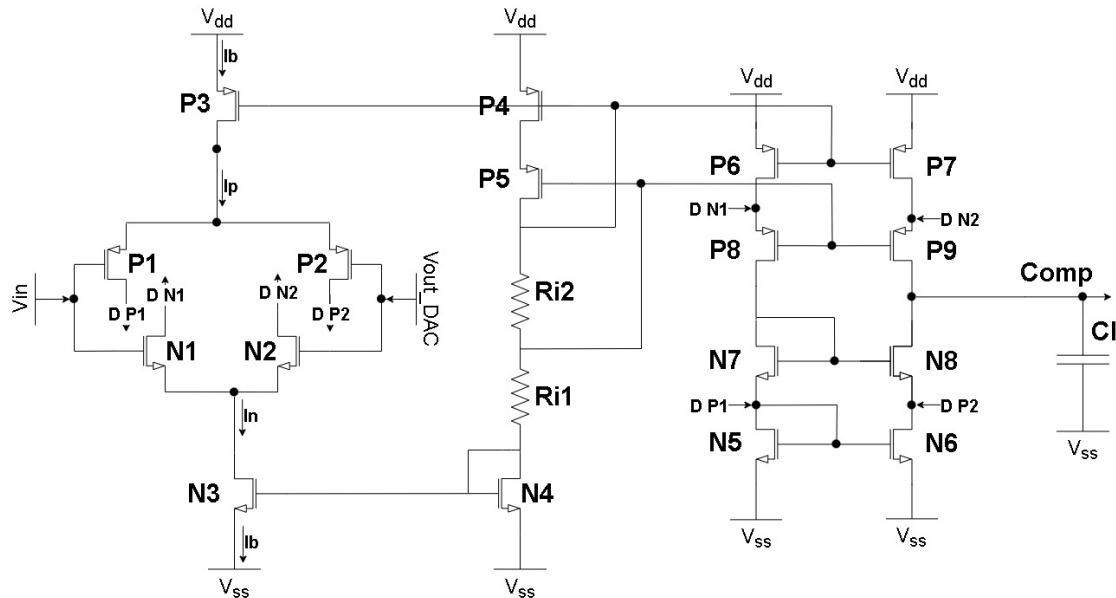
Figure 5.3: Comparator Schematic

Now, the output resistance of this comparator is extremely high, few MΩ, however, it does not influence in the slightest, because the output of this circuit is connected to a digital block, the SAR Logic Block. The rest of the features described before, are still as important, i.e., fast slew-rate and stabilized behavior. This op-amp has a single capacitor which terminals connect to the output and ground. This component has a value of 100f F, which cements the features explained before.

Since the circuit is now changed, some analyses need to be changed as well, e.g., the slew rate now is defined by the current passing through the input MOSFETs and the Cl capacitor. Because there is a ratio between the input and output currents, to achieve DC balance conditions and a phase margin of about 60º. When previously, with the third stage, there were not [2]. Moreover, since this circuit needs to respond

even faster than the previous ones, an increase in the $P3$ and $N3$ is imminent. In order to verify, the calculations done in the previous chapter, chapter 4, are recalculated for this op-amp and the final changed dimensions are.

Mosfet	Dimensions $\frac{W}{L}$
N1	120
N2	120
P1	238
P2	238
P3	221
Cl	100f

Table 5.1: Comparator Mosfet dimensions

5.1.3 SAR Logic Block

The most important circuit in the ADC is the SAR logic block. This component has the objective of generating every bit signal, in the test phase, and determining if each bit should be a zero "0" or a one "1". After analyzing a few different methodologies to implement the SAR Logic Block, as so, the Sequencer and Register Design No.1/2, [3], or the Nonredundant successive approximation register, [31], and comparing them both, [10]. The conclusion was to develop the logic block based on the method, Sequencer and Register Design No.2, [3], because it showed the lowest power consumption from them all. The circuit is comprised of two rows of asynchronous Data Flip-Flops, (Fig.5.4). The first row is a ring counter shift register with the objective to pass a one cycle up bit, resulting in initial test for every bit. The second row tests every bit as "1" and then confirms or not the previous value. The truth table of these types of Flip-Flops is as follows, Table 5.2. When $\overline{Preset}$ is "0" the block is in asynchronous set, when $\overline{Reset}$ is "0" the block is in asynchronous reset.

$\overline{Preset}$	$\overline{Reset}$	Clk	Data	Q	Qn
0	0	X	X	0	0
0	1	X	X	1	0
1	0	X	X	0	1
1	1	↑	D	D	Dn

Table 5.2: Asynchronous D-Flip-Flops Truth table

Having the first row $\overline{Preset}$ signal at one "1" and the $\overline{Reset}$ signal at "1", the output Q is dependent on the input D, which is "on", only one cycle per conversion. Forcing every FF output, Q, in the first row, to mimic the Data signal at different cycles. Moreover, the Qn being the Q output negated is only grounded at one cycle also. This signal powers the $\overline{Preset}$ inputs of the second row of FF. Having initially the $\overline{Preset}$ at one "1" and the $\overline{Reset}$ at one "1", forces the output of the first FF

of the second row to be Comp, the input signal, Q, which is zero "0" at the start. After that first instant, when the Qn of the first row changes to zero "0", the output of the 1st FF of the 2nd row is forced to be one "1", sending that value to the DAC. After the DAC and comparator determine if the value is larger than the target input voltage, the result Comp signal is changed to "0", if larger or "1" if lower. From that point on, when the Qn changes again to one "1", the 1st FF of the 2nd row has the output connected to the input, which means to the Comp signal already tested. That way, it is possible to change the output to the correct value depending on the input. This method works for every FF pair, one at a time, converting the analog value to a digital word.
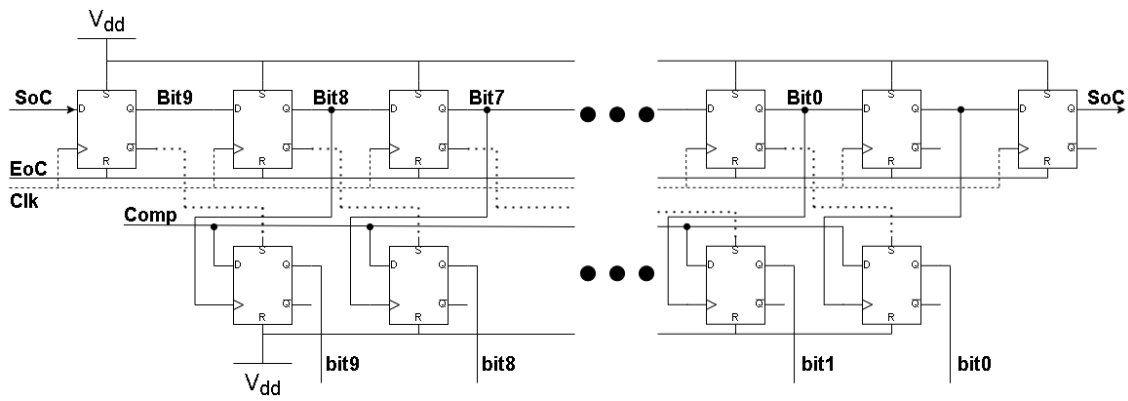

Figure 5.4: SAR Logic Block Diagram

5.1.4 DAC

The digital-to-analog converter, DAC, as in the case of the ADC, has various types, with advantages and disadvantages. For this project, once more, the space and power used, effectiveness, and speed are important properties when choosing which DAC type to develop. This way, the DAC type chosen was a charge scaling DAC using two subDACs, (Fig.5.5), [2]. The advantages of this type of DAC are, it is fast with good accuracy. The disadvantages are that the space used is quite reasonable, large element spread and it is non-monotonic, which indicates at least one or more localized maximum/minimum. The negative features once more can be decreased, the first one, by dividing the DAC into two subDACs. Instead of originating 10 capacitors correlated themselves by order of 2, the final DAC has 11 capacitors, with 5 of them are duplicated and one, the scaling capacitor, dividing the circuit of least significant bit, LSB, and the most significant bits, MSB. This results in a decrease in the area as well.

The second problem cannot be eliminated because of the methodology used, however, with the right calculations of the capacitor that divides the subDACs, C_S, this problem can be decreased as well. By using the Thevenin Equivalent is possible to determine the C_S value, that results in the best transfer function possible, as linear as possible, Equation 5.2. Something to be concerned about is the capacitor,
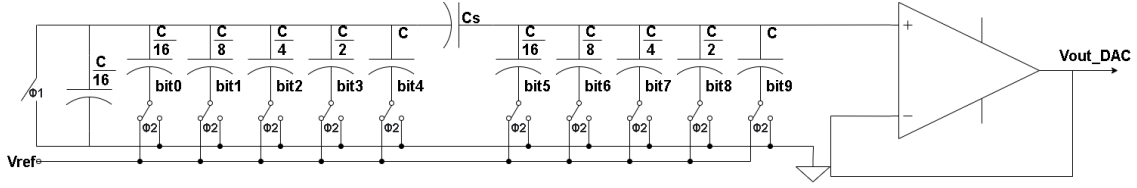
Figure 5.5: DAC Schematic

C, value, because, the lower it is, the smaller the space used is. Although, the lower it is, the higher the risk of the whole DAC being sensitive to parasitic capacitance, which increases the error of the DAC.

$$\frac{C}{16} = \frac{1}{\frac{1}{C_S} + \frac{1}{2C}}; C = 400fF \rightarrow C_s = 413fF \tag{5.2}$$

To complement the DAC, there is a buffer, at the end of it. This way the signal from the subDACs are isolated from the rest of the circuits. Moreover, being the converter quite sensitive to loads it is imperative to have the buffer there, otherwise, the DAC output signal would change or suffer distortion depending on the load. For this op-amp, the principal features are the input and output ranges, a fast slew rate, and a stabilized component. Since the third stage is going to be used for this buffer, the complementary input pair can decrease in size, not only because the slew rate is not related to them. But also, because input MOSFETs very large can distort the output voltage of the capacitor part of the DAC. Small alterations were also made in the resistor RC_C and the capacitor, C_C. The final change values are displayed beneath.

Mosfet	Dimensions
N1	14
N2	14
P1	21
P2	21
RCc	3K
Cc	1pF

Table 5.3: DAC Buffer MOSFETs dimensions

5.2 Results

This section shows another block analysis. Once more, a set of tests were needed. Some of them will be the same as done in the previous chapter, 4, and some will be quite similar, nevertheless, all equally important.

5.2.1 Sample and Hold

After utilizing the values calculated in the theoretical part for this block (section 5.1.1), was observed that even though the MOSFETs were fast enough, the output voltage was not as constant as expected. In order to resolve this problem the capacitor, Cl was increased to 10pF, and being the capacitor larger, the time needed to "fill" its capacity becomes larger as well which could represent a problem. This is because the sample time is already defined, as 50ns, however since the stimulating system is going to create a certain current and let that current pass through the load for a few minutes, at least. There will be no abrupt increases in the current or voltage input for this block, mitigating the problem as a whole. The final test of the Sample and Hold block is as followed. The Sample and Hold can respond in 50ns, (Fig.5.6), one cycle, that corresponds to the sample time. Moreover, the Vin signal, output of the block, can now recreate the voltage in the Vin_SH signal much better than before.
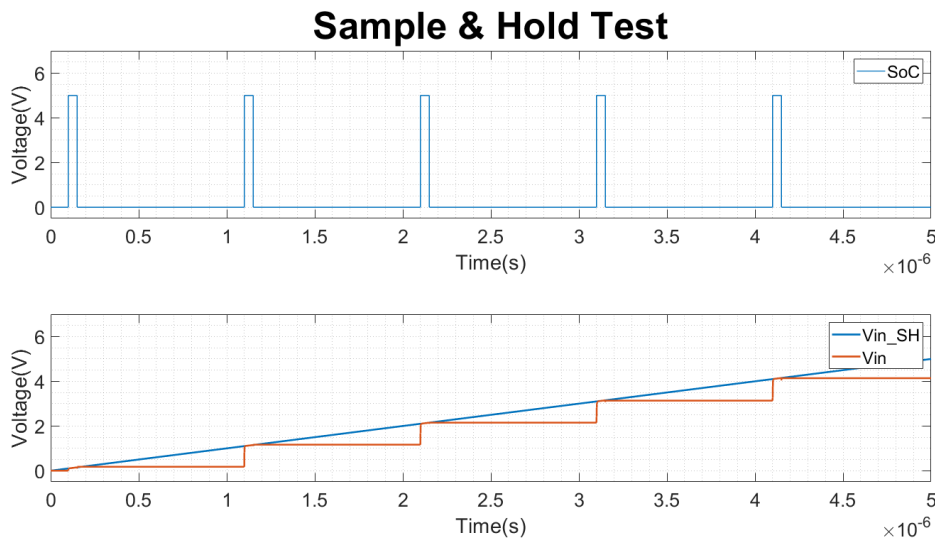

Figure 5.6: Test Sample and Hold

5.2.2 Comparator

In this subsection, the tests related to the op-amp are, ICMR, gain, phase margin, slew rate, and the comparator itself. The first iteration of this comparator had a larger output capacitor, so the slew rate was around 180V/us. The phase margin was higher, making the comparator much faster than the other op-amps. The modifications were made because of the layout, which as before, shows a loss in its slew rate, making the comparator slower and failing to respond in time. At least two approaches could be followed or increasing the input current MOSFETs dimensions, increasing the input current and the slew rate as a cause of it, or decreasing the capacitor dimensions. The first solution has the problem of increasing the space used and power consumption, which is exactly the opposite of what is intended.

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The second solution, in this case, does not have any apparent drawbacks, justified by the good response of the whole system, (Fig.5.7).

The op-amp tests and set-ups were already explained in the section 4.2.2, as so the results are.

Voffset(V)	ICMR(V)	Gain(20dB)	PM(º)	SR(V/us)
10.81u	[135m;4.87]	80.9	35	356

Table 5.4: Op-Amp characteristics

The principal difference is the ICMR, which is not quite as close to the limits as in the buffer, which was expected and is not a problem, as explained before. Not having a third stage is also the reason the gain is much lower. The slew rate is quite larger because of the complementary differential pair MOSFETs dimensions being increased. For this reason, the phase margin is lower than 60º, which might not the best alternative for an op-amp, because the time needed to reach the final value is larger. However, in this case, since the overall role of this block is to compare two input voltages and respond with a 0V or 5V this problem does not justify a larger phase margin. For this test, a set-up like the one in (Fig.4.13) was used. This time the positive input has a square signal and the negative input has a Vref of 2.5V. These inputs correspond to the output voltage from the DAC and the output voltage of the Sample and Hold block, respectively.
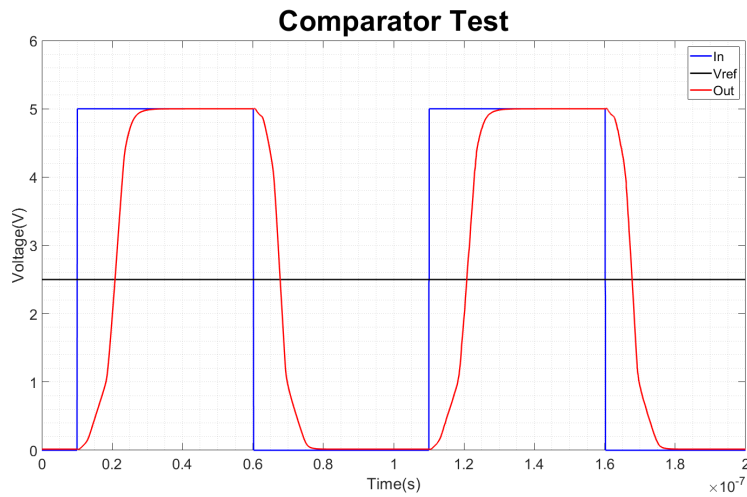

Figure 5.7: Comparator Results

5.2.3   SAR Logic Block

In this test, one modification had to be done to simulate the block. The SAR Logic Block is a middle chain/loop block, which means, it works and reacts differently depending on the information it receives from the other blocks, for example, the Comp signal. In order to test its behavior, the Comp signal was grounded, as

can be seen in the set-up, (Fig.5.8). The other signals are all square signals, as can be seen in the demonstration, (Fig.2.5).
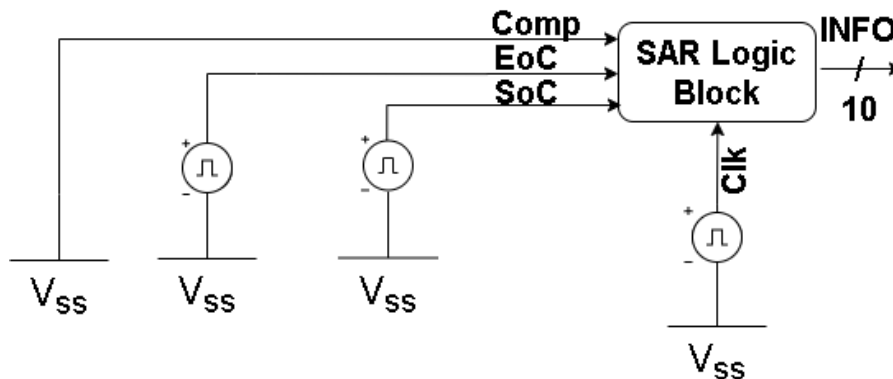

Figure 5.8: SAR Logic Block Set-Up

This way is easier to spot the post choice cycle, which is when the SAR Logic Block determines if the tested bit should stay as a "1" or change to a "0". In this test, all the bits will change to a "0" because of the Comp signal being always "0", after being "tested", as, once more, can be seen in the graphic beneath, (Fig.5.9).
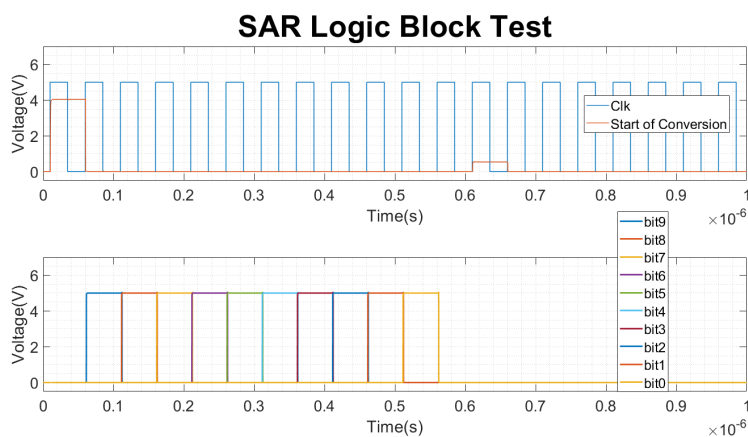

Figure 5.9: Test SAR Logic Block

If the Comp signal instead of being grounded, was shorted to V_{DD}, the post choice cycle, would be always a "1", that way the bits would never change the value after being tested, complicating the analyses. Note that, the Start of Conversion signal, effectively starts only one conversion, being possible to save power consumption, by not having excessive conversions done.

5.2.4 DAC

For this circuit two different tests were made, first, the buffer was tested as before, to understand if every alteration made to the components was successful.

After the whole DAC, with the buffer at the end of the DAC, was tested also. For this second test, since the inputs on the DAC are parallel, each one needed a different dc voltage source. The values for this buffer reflected the minor modifications made to it, the phase margin and the slew rate increased in value, and the ICMR remained the same, 99% off the full range.

Voffset(V)	ICMR(V)	Gain(20dB)	PM(º)	SR(V/us)
46.41u	[937u;4.99]	111.3	86	257

Table 5.5: DAC's buffer characteristics

Different from the last buffer, this one, has a lower gain and higher phase margin. This occurs because of the decrease in the complementary differential pairs dimensions. The values used in the last buffer were too large and as such, the output DAC signal was being distorted by them. This modification does not create any problems, since the gain is already quite high, with the three-stage op-amp. The slew rate is, again, higher than in the specifications, because of the layout problem mentioned before.
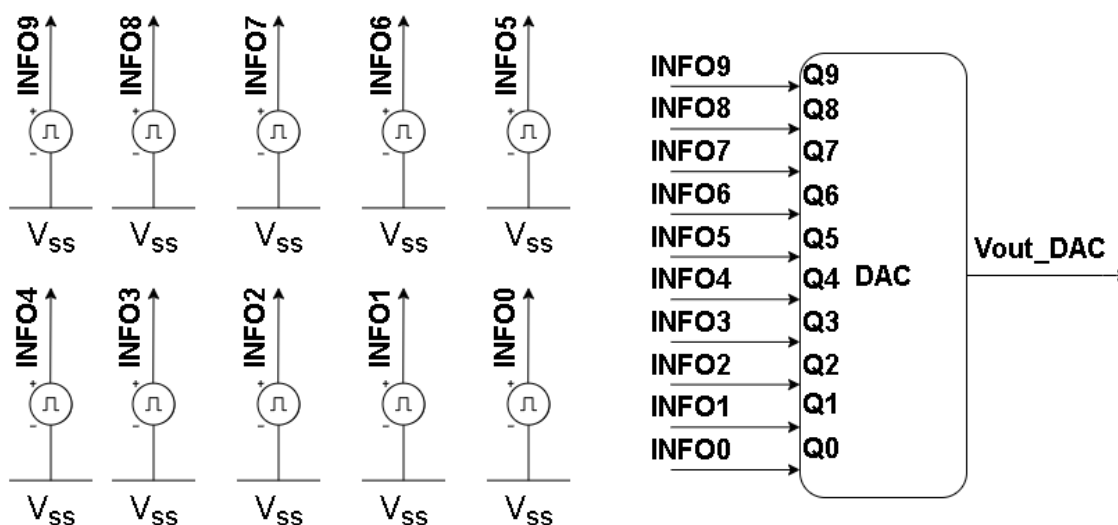

Figure 5.10: DAC Set-Up

As stated before this DAC has a parallel input methodology, as so, every input was implemented as a pulse signal switching between "0" and "1". The only difference in the inputs was the frequency at each one, (Fig.5.10). If the frequencies grew in order of two, e.g, 10KHz (INFO0), 20KHz (INFO1), 40KHz (INFO2), ..., 640KHz (INFO6), and connected to the proper same significant level input of the DAC, Q0, Q1, Q2, ..., Q6. Being Q0 the LSB and Q9 the MSB, a voltage ramp can be achieved at the output of the DAC. The 3 most significant bits can be seen beneath. The MSB (2nd graphic), has a period of 51.2us, the second MSB (3rd graphic) has 25.6us, until the LSB, which has 100ns. Switching every 50ns from "0" to "1". Having the inputs design as so provides a full binary range from every bit at level "0" to every

bit at level "1". Concluding with a 0V to 5V at the end of the DAC circuit, as can be seen, (Fig.5.11), graphic 1.
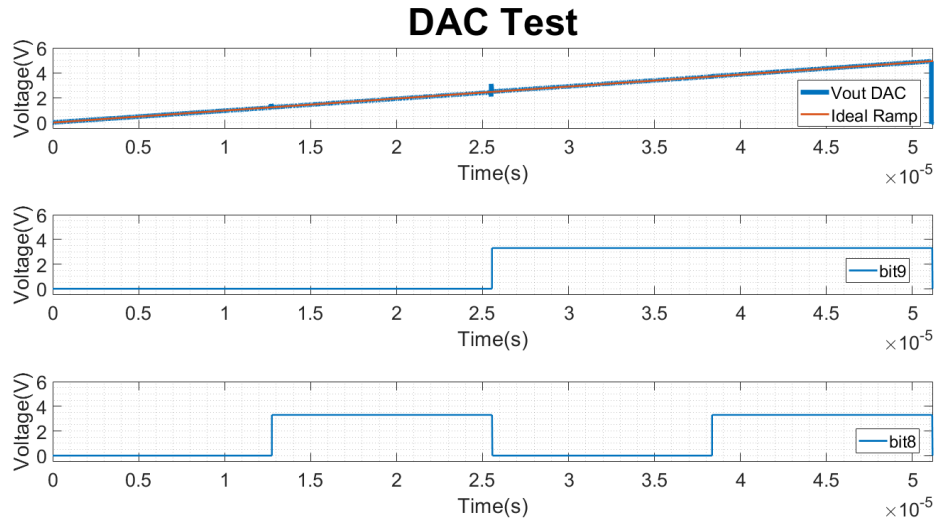

Figure 5.11: Test DAC

In the Figure above might not be possible to detect a few noise imperfections in the output ramp. However, being this DAC non-monotonic it was already expected to observe this behavior. This imperfection results by a sudden change of a large number of bits at once, e.g. at the middle range value, from "01 1111 1111" to "10 0000 0000" as all the bits change at once, the parasitic capacitance distort the output analog value. This imperfection can be easily detected when comparing the output voltage ramp of the DAC with the ideal ramp, (Fig.5.12).

In the figure, the relative error between the output voltage of the DAC and an ideal ramp is shown. For values near the 0V, the DAC response is not good, because the lowest voltage the DAC can recreate in the output is 937uV. Moreover for the first 5% of the ramp duration, even though the DAC started to respond, it is not linear yet. From that point on, the DAC becomes more linear and the error drops to lower than 5% (marked with red) for the rest of the stimulation.

5.2.5 ADC Block

For this final block validation test, the input signal, Vin_SH, (Fig.5.13), 2nd graphic in blue, is a voltage ramp between 0V and 5V, which represents the working range. The graphics will show the Vin signal, 2nd graphic in red, the output signal of the Sample and Hold block. Also the input step of the ADC block versus the Vout_DAC, 3rd graphic in black, the output signal of the DAC. Both signals are analog, which makes the comprehension/validation easier. The Vin signal is the target for the ADC block and the Vout_DAC is the seeking signal, concluding that the whole block is working properly. The real output of the ADC block is the Comp signal in parallel, which is equivalent to the Vout_DAC signal shown before.
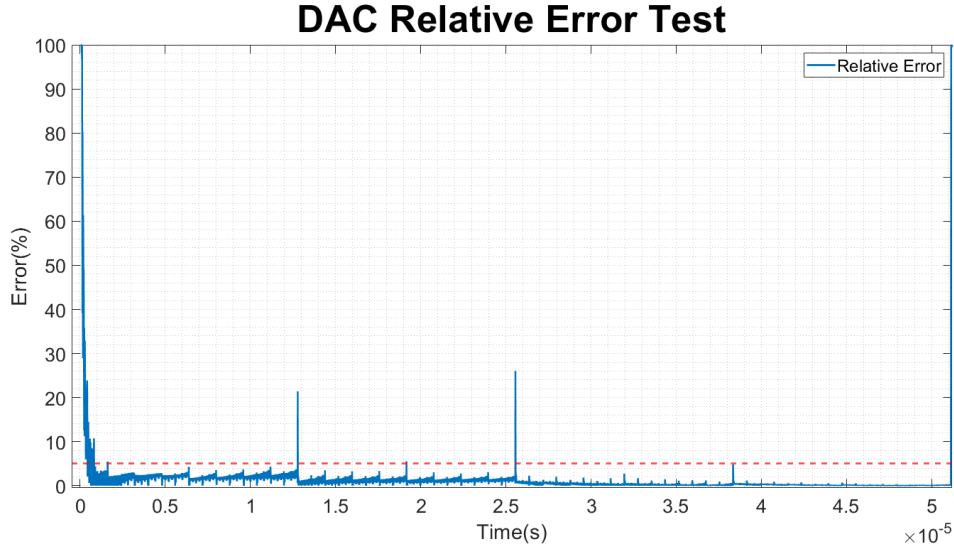
47

Figure 5.12: DAC Relative Error Test

Another very important test to make is to determine the accuracy of the ADC. As so, there are two already established techniques known by Differential Non Linearity, (DNL) and Integral Non Linearity, (INL). Both these techniques use as input, or a voltage ramp or a sinusoidal, in this case, a ramp was used [7].

The first test revolves around the difference between the actual step width output of the ADC and the ideal step width. Being a 5V powered circuit, with 10 bits of information, the LSB can be calculated by,

$$V_{LSB} = \frac{V_{DD} - V_{SS}}{2^{N_{bits}-1}} = 4.88mV \qquad (5.3)$$

Utilizing the next equation it is possible to calculate the DNL for every code possible, in this case, from 0 to 1024, $2^{N_{bits}}$.

$$DNL(i) = \left| \frac{V_{(i+1)} - V_i}{V_{LSB}} - 1 \right|, 0 < i < 2^{N_{bits}} - 2 \qquad (5.4)$$

The second test, revolves around, the deviation between the actual transfer function and an ideal one, a straight line. Once more, utilizing the following equation it is possible to determine the INL for every code input.

$$INL(i) = \left| \frac{V_{(i)} - V_{zero}}{V_{LSB}} - i \right|, 0 < i < 2^{N_{bits}} - 1 \qquad (5.5)$$

Once more, after saving the arrays from the simulations in the Cadence software and with the help of Matlab, the next graphics were created, (Fig.5.14).
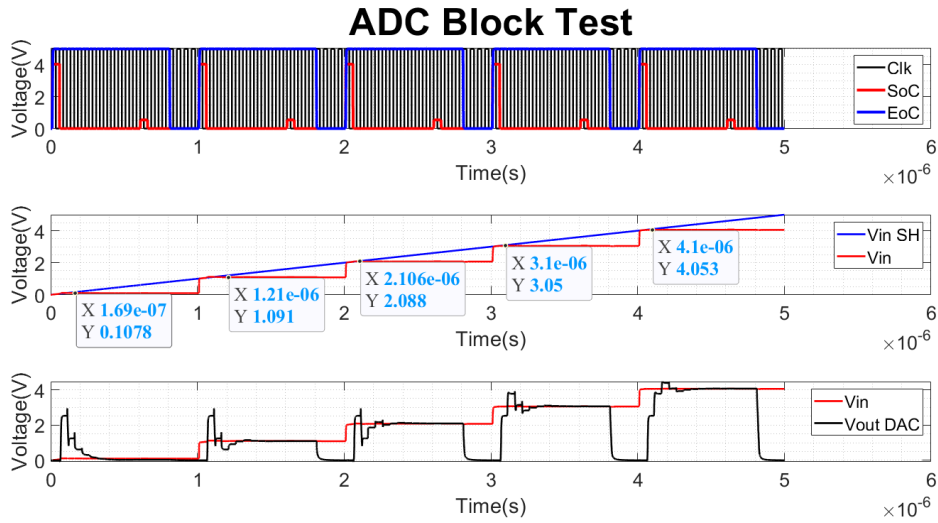
Figure 5.13: Test ADC
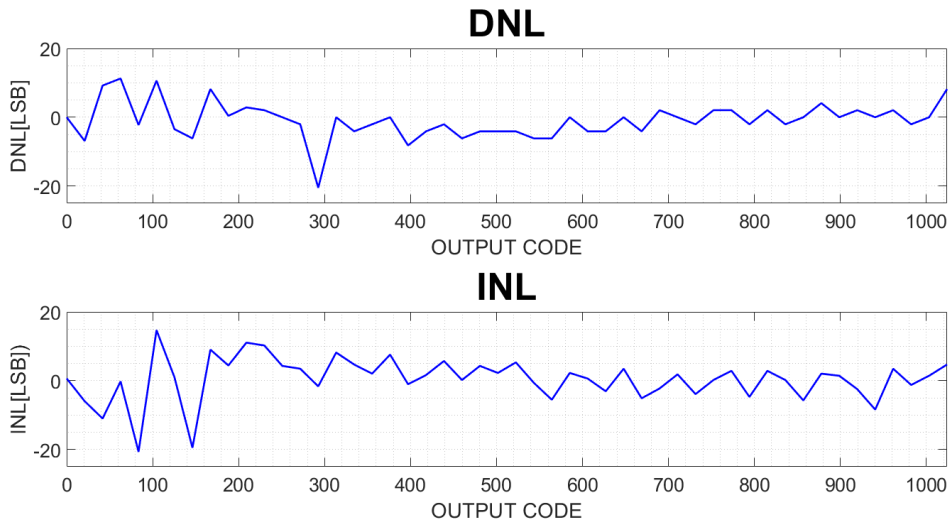
Figure 5.14: Test DNL & INL

In this graphic, the xx axis represents the full range of possible input codes and the yy axis represents the DNL or INL number of LSB bits of error. In both cases, the maximum error does not pass the 20LSB, which corresponds to a maximum of 2% error. These values are determined for the first experiments, which corresponds to the same range when the DAC has larger error values [21].

$$MaxError = \left| \frac{20 * LSB}{1024 * LSB} * 100 \right| \equiv 2\%$$

Chapter 6

Communication Block

The Serial Peripheral Interface (SPI) protocol is utilized to communicate between a wide variety of devices, like sensors, memory cards, circuits, ADCs, DACs, or even microcontrollers. All the trades are implemented at small distances. Its architecture is "Master-Slave", with a bidirectional "full-duplex". There can only be one master but many slaves, even though for communication, only one slave can be selected by the master, at any time. Being bidirectional means that, even though, e.g. the master only needs to send information to the slave, for every communication cycle the slave also sends the master information, which it can ignore if wanted, "data-exchange". The "full-duplex" transmission is based on two shift registers, one for the master and one for the slave. The communication is synchronous, having the master, generating the clock signal, handing it over to the existing slaves. This way, there is no need for great clock precision, the bits are sent at every clock transition, rising edge or falling edge. However, because the microcontroller used the word's length has three values to choose from, 8, 16, or 32 bits, which means, to send 10 bits of information it is required to send a word of 16 bits at least [16].

6.1 Circuits/Schematics

Having once more to account for the power consumption of all parts it is counterproductive to have the communication block sending undesired information all the time. Since at the end of every conversion the SAR Logic Block reset the bits converted, to be ready for the next conversion. The information needs to be saved before that, or else, it is lost. Moreover, since the data output is going to be sent in a serial type, use only 1 external pin instead of 16 pins. Results in having a transmission taking 16 clock cycles, one for each bit. Even assuming the bits were not reset after every conversion, if the data was not saved at the end of the conversion, the maximum conversion rate would be divided by two. It would take 16 cycles to convert, and 16 more to send the data, instead of the only 16 cycles to convert and save the information. With this solution, the conversion and information communication becomes two serial tasks instead of parallel tasks.

Understanding everything explained above, two circuits were developed, one to

count 16 cycles, a counter, and one to save the information at the end of the 16 cycles, a data register. This way when the ADC serial output is reset at the end of every conversion the information of the last conversion was already saved in the Data register block. After having the information of the last conversion saved another block type, a parallel input serial output, PISO, shift register, is used to decide to send or not to send the information. The choice to go with the PISO Shift Register is very simple, the input needed to be parallel to match with the output of the previous block, Data Register. Moreover, the output needed to be serial to only have one pin used, instead of 16 ports, as stated before. Being the final diagram block as can be seen beneath, (Fig.6.1).
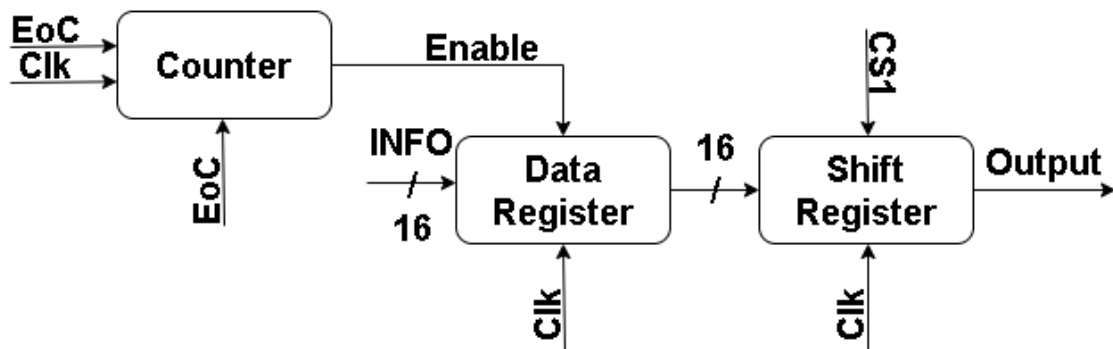

Figure 6.1: Communication Diagram Block

6.1.1 Counter

The counter block, (Fig.6.2), as stated in the name has the mission of counting, this block uses a signal generated in the microcontroller as a start of counting, Soc, after 16 cycles it generates an end of conversion, EOC, signal. Sending and saving the data converted from the ADC to the Data register block, at the same time, this EOC signal, also informs the microcontroller that the conversion is done and the data is ready to be sent to the micro.

This block is composed by 4 Data Flip-Flops and a few XOR and AND gate, in 4 different levels, that way, is possible to create 4 output signals, with 4 different frequency counters, from one that counts every up rise of the clock till one that counts every 8 up rises of the same clock. This way, utilizing a NAND gate followed by a NOT gate it is possible to create a signal always "high" when all the output signals are at level "0", which corresponds to the 16 cycles [32].
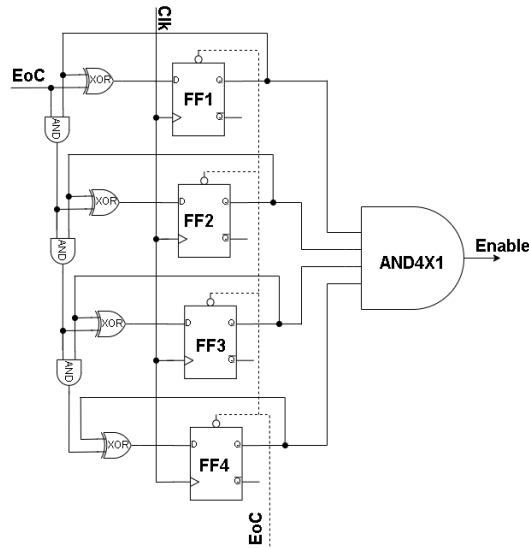
Figure 6.2: Counter Diagram Block

6.1.2 Data Register

The Data register consists of a chain of 2x1 multiplexer connected to a Data Flip-Flop, D-FF, this way, the D-FF can have an enable signal, (Fig.6.3).
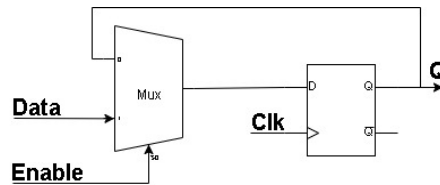

Figure 6.3: FF with Enable signal

When the enable signal is at "0" the output of the D-FF represents the previous eligible Data value, save stage. When the enable signal is "1" the output of the D-FF is the Data input, update stage, truth table beneath.

Enable	Clk	Data	Q
0	X		Previous state
1	↑	D	D

Table 6.1: FF with Enable Truth table

Making use of this new block, if the Data register is enabled at the end of every conversion before the data is reset, it will store the information until the next end of conversion, saving the data as intended. This parallel input parallel output, PIPO, (Fig.6.4), was used because the data needed to be saved all in an instant, as so, using a PISO, would not be very advantageous, because the block would have to work for a longer time, the whole conversion time.
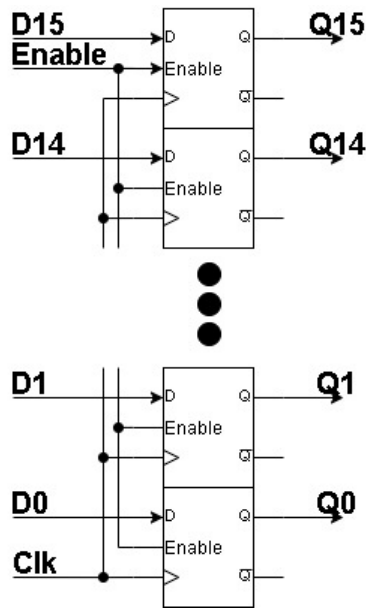
53

Figure 6.4: Data Register Diagram Block

6.1.3   Shift Register with CS1

After the data is saved the simplest way to send or not to send information can be seen beneath, (Fig.6.5), using logic gates. The output bits from the Data register will be marked as D4, D5,..., D13, being D13 the most significant bit, MSB. The D14 will be the direction bit, explained before in chapter 3 and the rest will be grounded inputs, D0, D1,.., D3 and D15. Further explained why in the results of this circuit. Having the CS1, signal as "0" keeps the block on load mode, updating the information from the output of the Data register to the outputs of every flip-flop. Having the same signal as "1", locks the outputs of the flip-flops and starts to shift them at a one-cycle paced, (Fig.6.6).
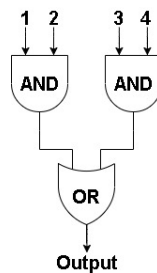

Figure 6.5: Load/Shift Schematic

Ending with a one serial output register that will be connected to the microcontroller. Done this way, because, now the data transmitted to the micro only requires one port, versus the 16 ports that would be needed if the output were parallel [27].

CS1	Clk	Data	Q
0	↑		Loading state
1	X		Locking state

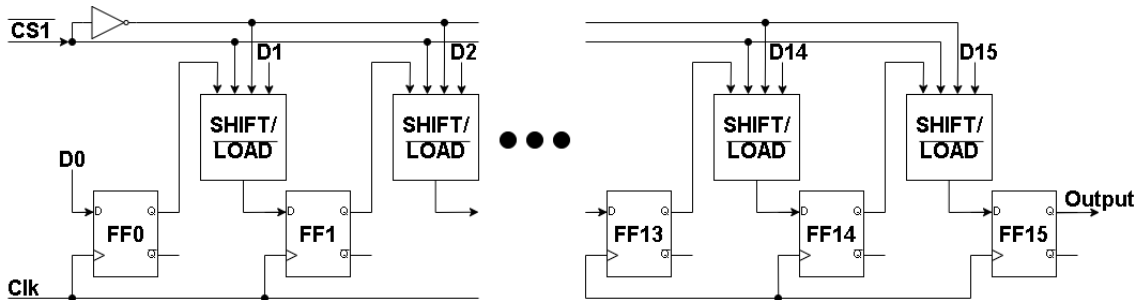Table 6.2: Shift Register + Load/Shift Truth table

Figure 6.6: Shift Register

Using both of the blocks above, the microcontroller, the master, can select/start the transmission of information with the ADC driver, the slave, at any point. The only important note of this system is, when the master demands the conversion information, is always the last completed conversion, not the one happening.

6.2 Results

In this section, it will be discussed the tests done and results obtained for the Counter, Data Register, and Shift Register Blocks. All tests are quite simple because the main objective of these blocks is to process information by counting cycles, saving, or sending data.

6.2.1 Counter

This simulation revolves around the idea of when the EoC signal is at level "1" the Counter will count every rising edge of the clock, i.e. the outputs of every FF will swap levels by frequencies of times 2, (Fig.6.7).
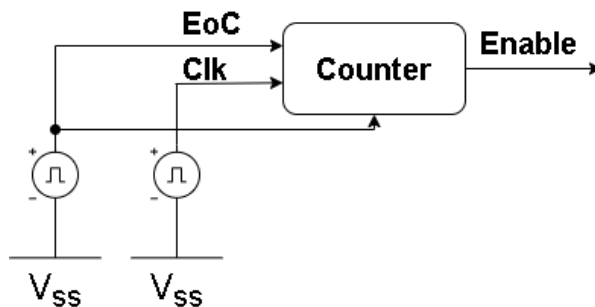

Figure 6.7: Counter Set-Up

The first level, Q0, changes at every rising edge, the second level, Q1, at every 2 rising edges, the third level, Q2, every 4, and so on and so forth. When the 4 outputs are at "1", the output of the Counter swaps states, from "0" to "1", marking the 16 cycles. This behavior can be seen in the figure beneath, (Fig.6.8). Successfully simulating the circuit.
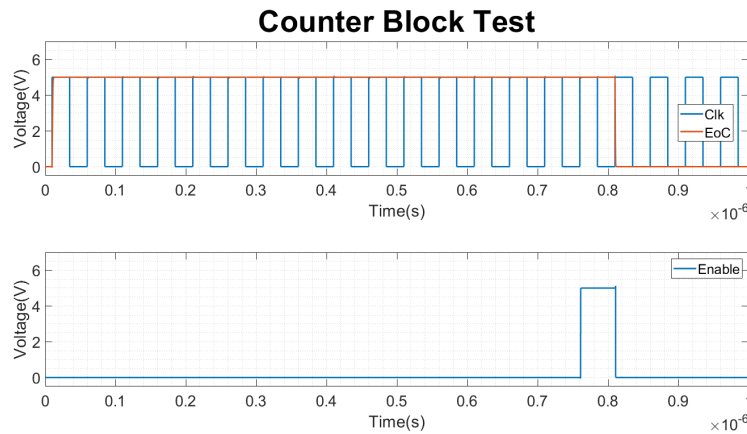

Figure 6.8: Counter Block Test

6.2.2 Data Register

This test uses once more the Clk, clock signal, and the Enable signal, which is the output of the Counter block. The inputs are again parallel, passing the data "1101 1011 0110 1100" from MSB (INFO15) to LSB (INFO0), (Fig.6.9).

The outputs of this block are also parallel, however, they only change values, storing process, when the Enable signal swaps states, from "1" to "0". This occurs at the end of the 16 cycles, right before the data inputs (INFO0 to INFO15) are reset. This way is possible to save the data of the last conversion done until the current conversion, required by the micro, is finished. In the next figure, (Fig.6.10), can be observed a few output signals (Q15, Q14, Q13, Q2, Q1, Q0), these signals should display the following data 110 100.
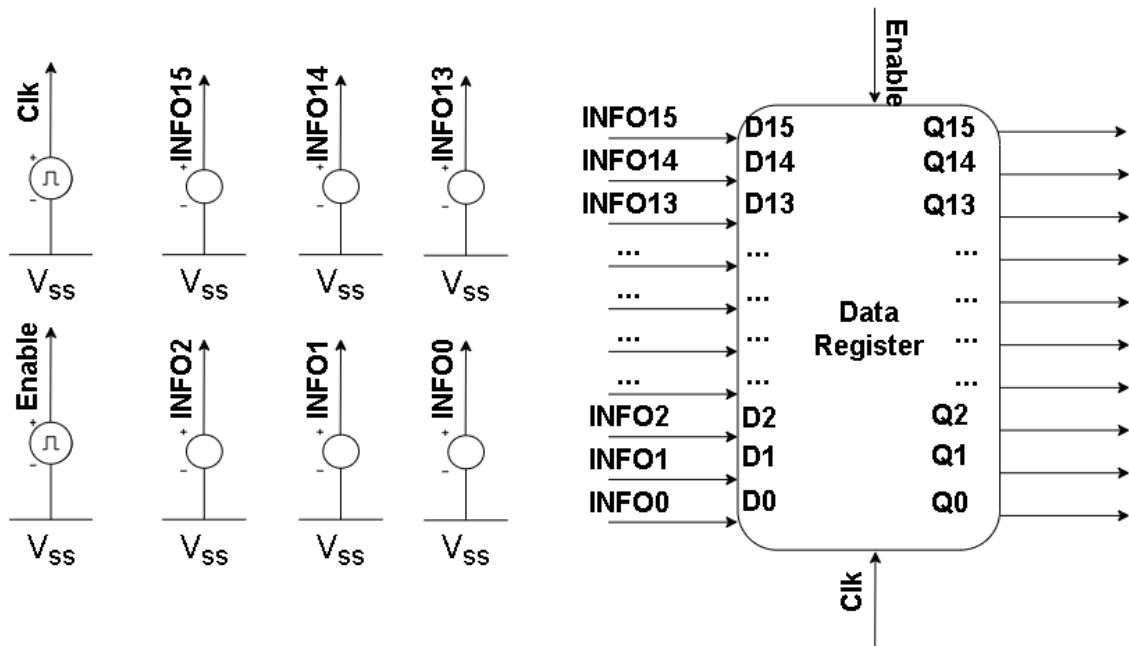
Figure 6.9: Data Register Set-Up

Figure 6.10: Data Register Test
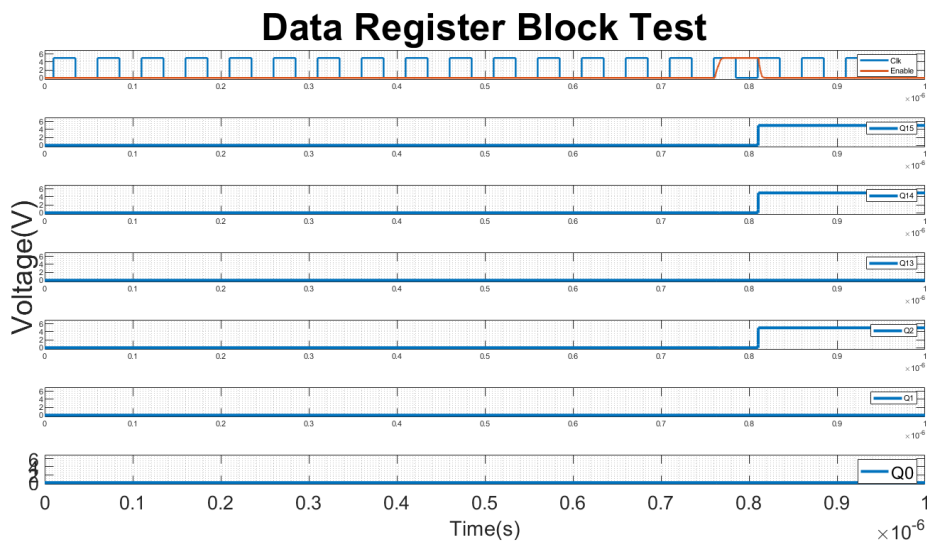
6.2.3 Shift Register

As in the block tested before, the inputs are parallel and connected to the parallel outputs of the Data register block. The CS1 signal is sent by the micro and is "1" throughout the whole process. The output of this block is serial as explained before. For this test, the information sent was "1110 0010 1100 1001", after testing the results were as followed
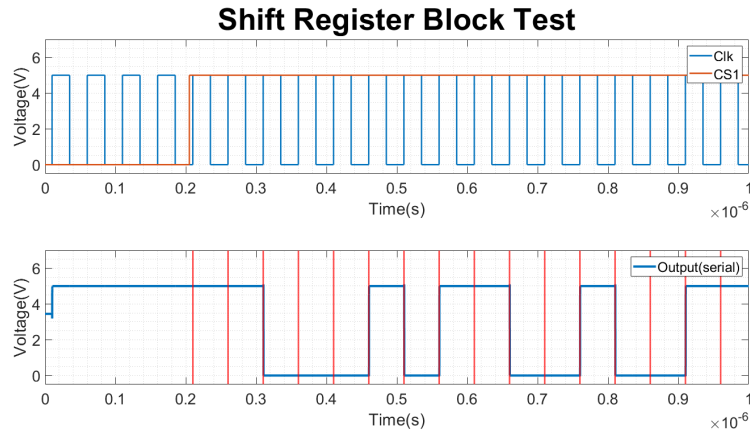
57

Figure 6.11: Shift Register

As can be seen above, (Fig.6.11), the data output was equal except the MSB which was discarded, resulting in "1100 0101 1001 001X". Since the valid information is 11 bits long, the MSB input can be grounded and the actual information enters in the second MSB, D14. A way to resolve this problem otherwise is, for example, extending the FF plus CS1 chain, giving it one more state. But that requires more space, which is very valuable and for that reason, the solution was just to ground the MSB input. This way, even though the circuit chomps on one input the overall objective of this block is reached.

6.2.4   Communication Block

For this last simulation, the inputs values were dc voltage sources, e.g. for the whole duration of the test, the inputs stayed the same. The word sent was "0100 1100 011X XXXX", being in the left the Direction signal, followed by INFO14, the MSB, INFO13, INFO12, ..., until INFO5, LSB. The final inputs, INFO4 to INFO0 are ground since they carry no valid information. The control signal resembles the signals in the demonstration, (Fig.2.5). The final set-up can be seen beneath, with the 16 inputs and four control signals, EoC, Clk, Direction, and CS1 (Fig.6.12).

The 2nd graph (Fig.6.13) shows the EoC signal, that will be sent by the microcontroller and the output of the Counter block, the Enable signal, which saves the input values from the dc voltages to the output of the Data Register block. This can be seen in the 3rd graphic (Fig.6.13), when the Enable, at yellow, goes from "1" to "0", the Data Register saves the values. In the last graphic (Fig.6.13), it can be seen another signal from the microcontroller, the CS1, and the output serial signal. When the CS1 goes rising edge, the output serial signal starts to be sent. Note the vertical red lines represent one cycle of the clock. As so, the output serial signal from left to right is "0100 1100 0110 0000", if the micro is programmed to only retain the 11 MSB the word is sent successfully.
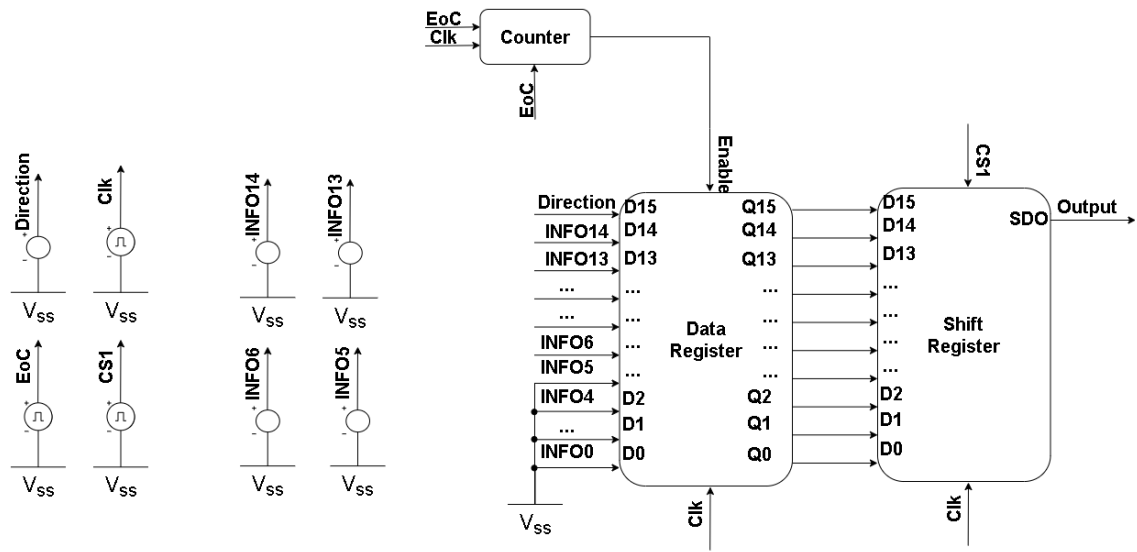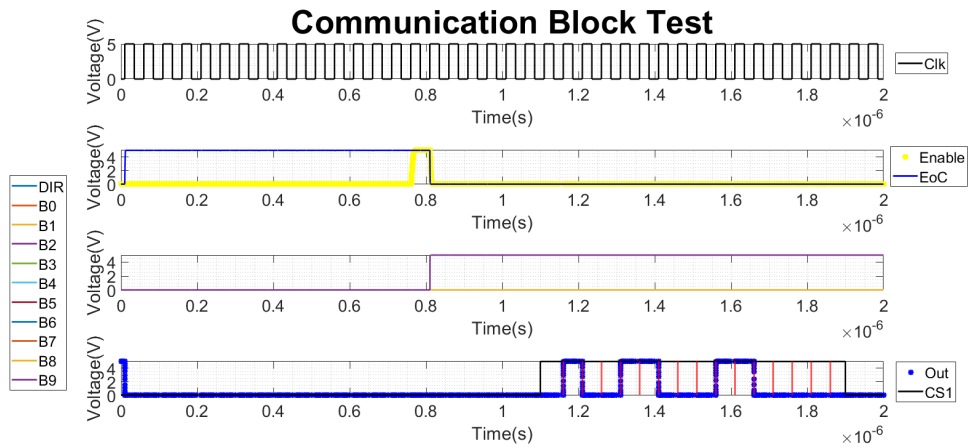
58

Figure 6.12: Communication Block Set-Up

Figure 6.13: Communication Block Test

Chapter 7

Layout design

This chapter, once again, has the objective of describing the same system as before, in a new environment capable of and ready to be exported and sent for printing. For this reason, there will be 3 subsections, related to every main block referred to before, and one last related to the whole system. In this environment, some checks need to be done, to verify the physical verification of the stripes of the material. For this dissertation document, the tests/checks have three main purposes. Verifying the physical properties of every single component or strip. Being its dimensions or the distance they are all apart, by using DRC testing with rule set dfII:no_coverage and rule set dfII-DFM:no_chip_rules. Verifying the compatibility between the layout and the schematic, Layout Versus Schematic. If the connections done in the layout are the same as in the schematic, LVS with SetSwitches:resimulate_extracted. After these few tests are checked out successfully, the last test is to extract the layout with the parasitic components, Quantus QRC extraction type: RC. This last test will create a layout as the one developed, but this one will have the parasitic components as capacitors, or resistors. This final block is the nearest recreation possible of the real-world environment, being the most trustworthy tests performed on it [4].

Before displaying the layout blocks, some notes need to be explained. For this type of technology having analog and digital Integrated Circuit, (IC), in the layout is the norm. However, these two types of circuits should not be implemented in the same area, because the digital ICs are produce much more noise when compared with analog ICs. If not addressed, the intrinsic non linearity of the digital ICs may distort the output signal from an analog IC, this way exhibiting strong non linearity. Some good practices for suppressing radiated and conducted EMI, crosstalk, and signal reflections, can be, separating the board into analog and digital functional blocks, spacing those blocks as much as possible, and lastly, contouring those blocks with a guard ring, to, diminish the noise input/output [5].

7.1   Measurement Block

The Measurement Block is composed of three minor blocks, the Voltage Switch surrounded in yellow, the buffer in orange, and the non inverting operational ampli-

fier in light green. The first block is a non linear analog block when the other two are linear analog blocks. For this reason, the two analog blocks have guard rings surrounding them, indicated for example by the white arrows in (Fig.7.1).

Another development technique used for the op-amps is the use of dummy elements, which are elements added to the circuit to unify the MOSFETs structures and to diminish the fabrication process errors, indicated by the four black rectangles in (Fig.7.1). The last technique used in the op-amp is called the symmetry constraints, which is represented by symmetry groups and gives the constraint that each pair of cells in a symmetry group must be placed symmetrically to a common vertical or horizontal axis called the symmetric axis, in this case horizontal, indicated by the red horizontal line in (Fig.7.1), [14].
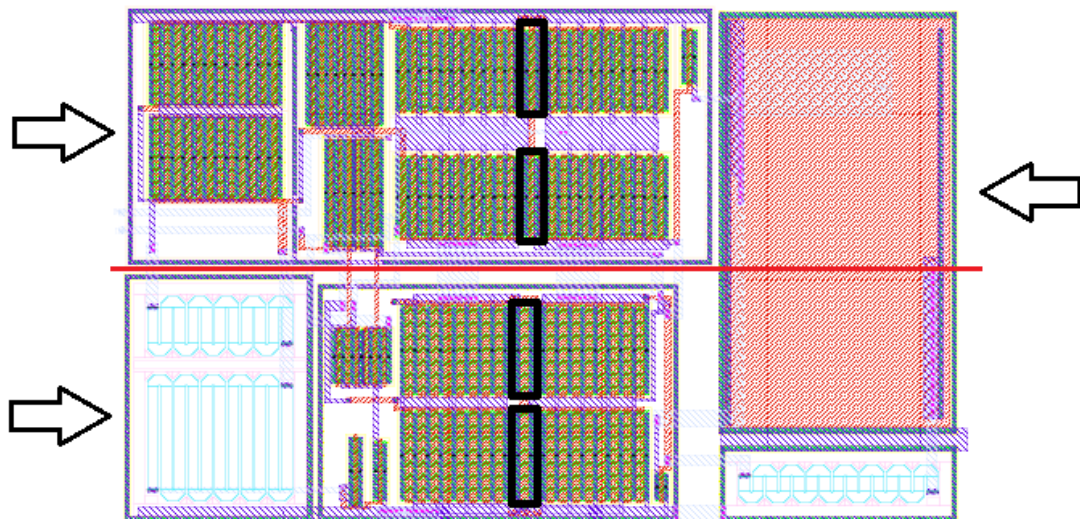
Figure 7.1: Operational Amplifier Layout

After dealing with every block individually is time for the merge and creation of the Measurement Block, (Fig.7.2). In this figure, the block surrounded in yellow represents the Voltage Switch, the block surrounded in orange represents the buffer, and the last block, the green one represents the non inverting op-amp with the respective resistors. The Measurement Block dimensions are 400μmX100μm.
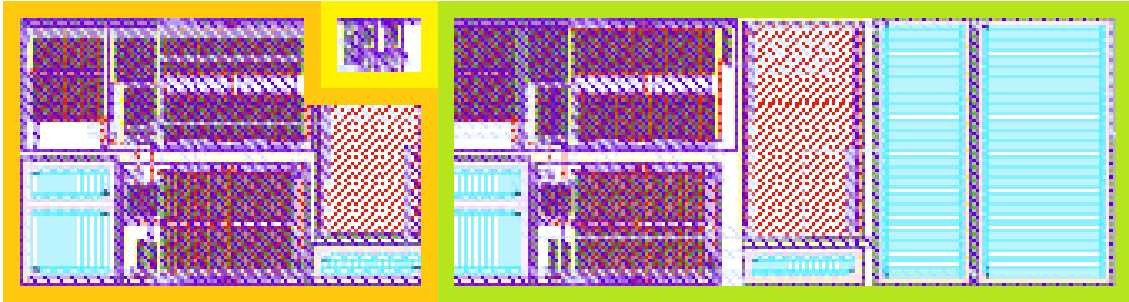
Figure 7.2: Measurement Block Layout

7.2 ADC Block

The ADC Block (Fig.7.3) is composed of 4 minor blocks, the Sample and Hold surrounded in orange, the Comparator in dark blue, the SAR Logic Block in pink, and the DAC[1] in light blue. The first and second blocks are both analog blocks when the SAR Logic Block is a digital one. The DAC has ten digital inputs and one analog output. For this reason, the connections between the output of the SAR Logic Block and the inputs of the DAC, both digital components do not need any further working around. However, this connection should not be near or overlapped with the other analog connections. As a result, the other blocks are all surrounded by guard rings. The op-amps used in this block also share the various techniques explained and used in the last section's op-amps. The use of arrays of an equally sized parallel capacitor and the common-centroid technique was used, to, improve the matching of the capacitors [[18], [34]].

The block surrounded by orange is the Sample and Hold, the one in dark blue is the comparator, the one in pink is the SAR Logic Block and the light blue is the DAC. For this block, the dimensions are around $560\mu m$X$300\mu m$, in the worst case.

7.3 Communication Block

For the final main block, (Fig.7.4), the three minor blocks are a 4bit Counter surrounded in brown, a Data Register in light grey, and a Shift Register in dark grey. This time all the blocks are digital blocks, so there are no problems between connections.

The block surrounded by brown is the 4bit Counter, the one in light grey is the Data Register and the last, in dark grey represents the Shift Register. This block has the dimensions of, $300\mu m$X$200\mu m$.

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[1]Done with the help of another student
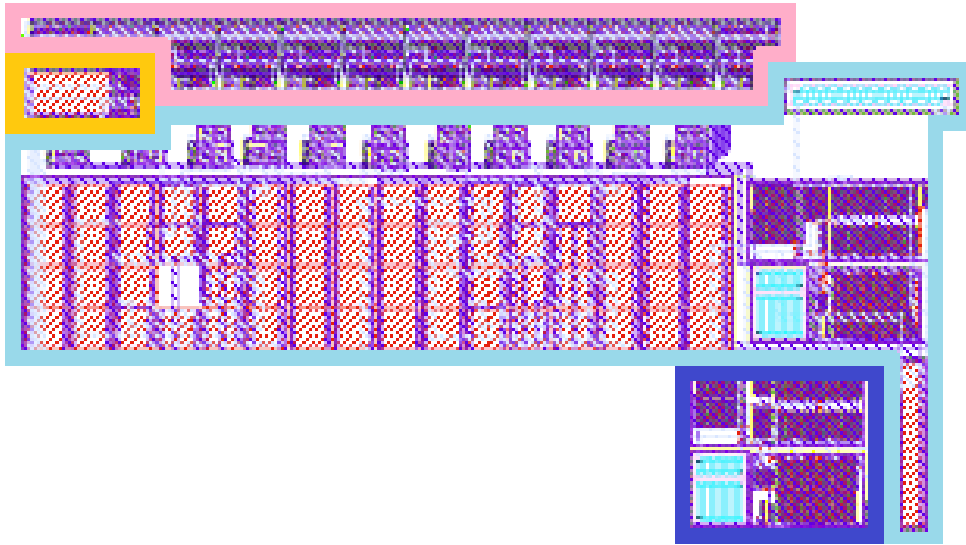
Figure 7.3: ADC Block Layout

7.4 Acquisition System

The Acquisition System represents the previous three subsections combined, even though, the last blocks were not as rectangular as possible, it was with a purpose. Merging now the three blocks results in a rectangle shape, (Fig.7.5), saving space. A guard ring was also made between the Measurement Block and the other two main blocks, diminishing the noise influence. The block surrounded by brown is the Measurement Block, the one in green corresponds to the ADC Block and the last one, in yellow represents the Communication Block. The final dimensions for the Acquisition Block are $666\mu m$X$320\mu m$, resulting in an overall space used of around $0.213mm^2$

Figure 7.4: Communication Block Layout
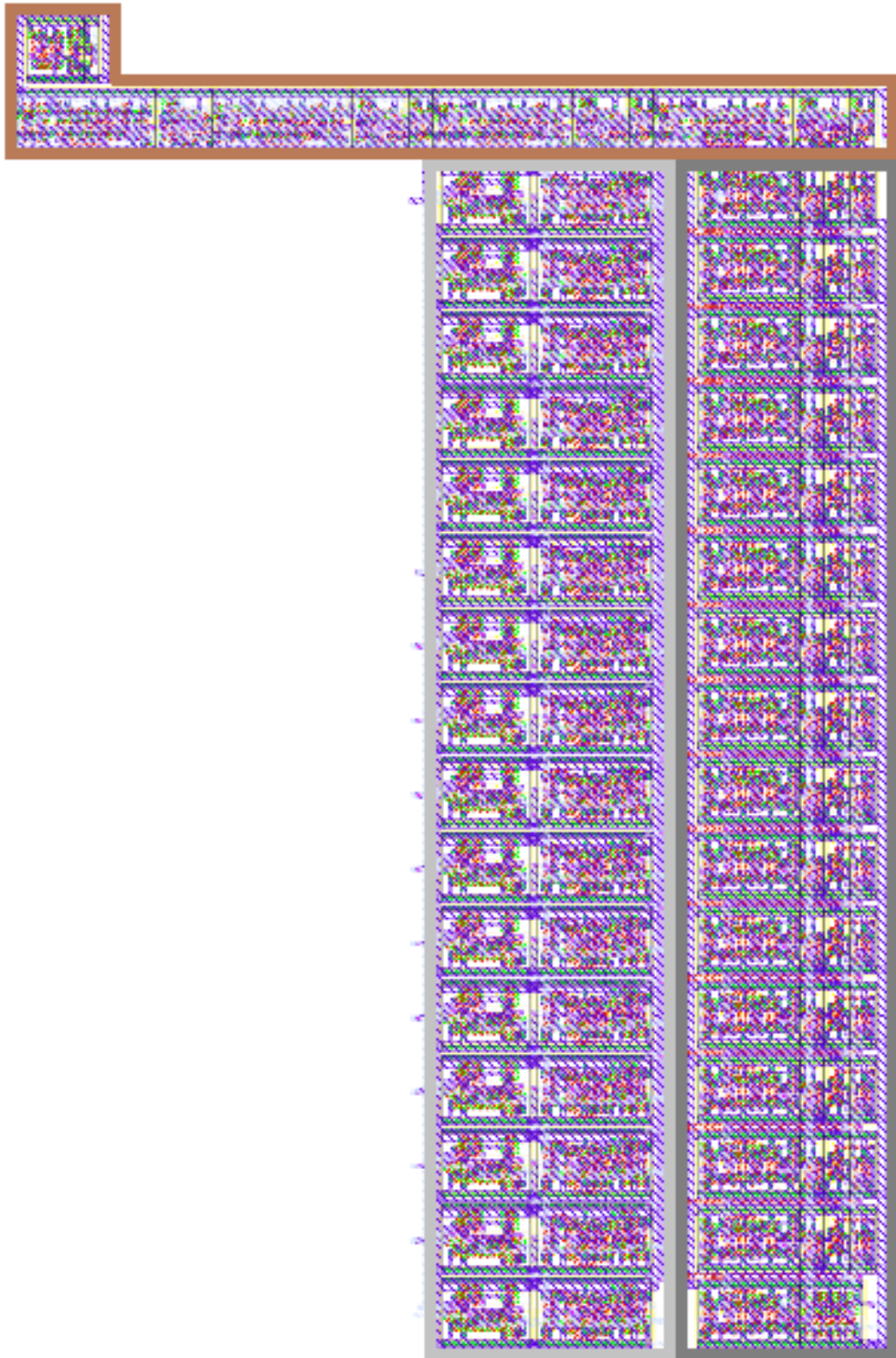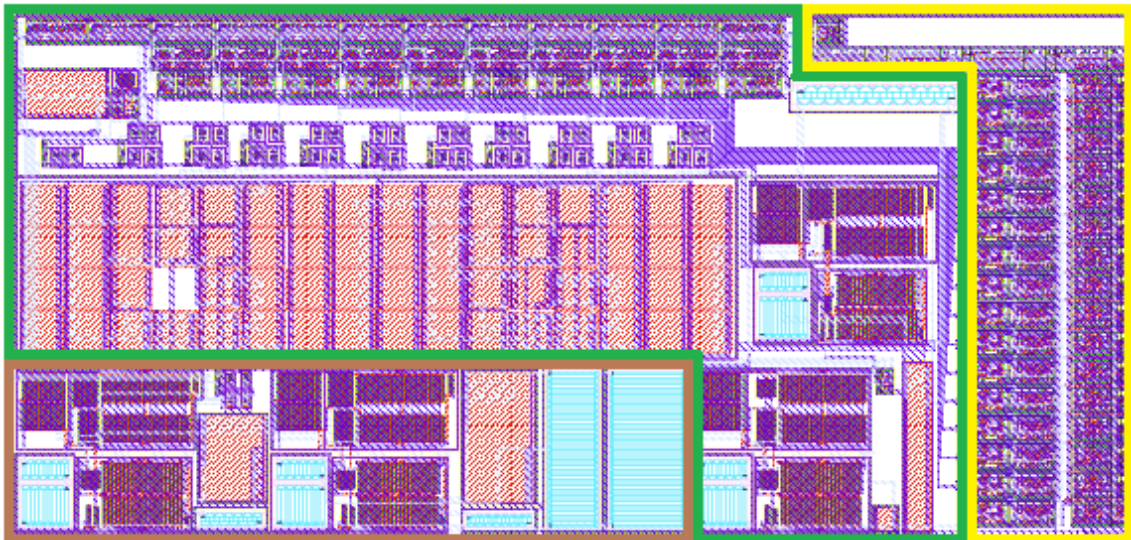
Figure 7.5: Acquisition System Layout

Chapter 8

Results/Discussion

This chapter, describes the achieved results for the whole system. In order to test the layout, a set-up like the one beneath, Fig.8.1, is required, the need for the control signals is extremely high and the way they are designed is important too.
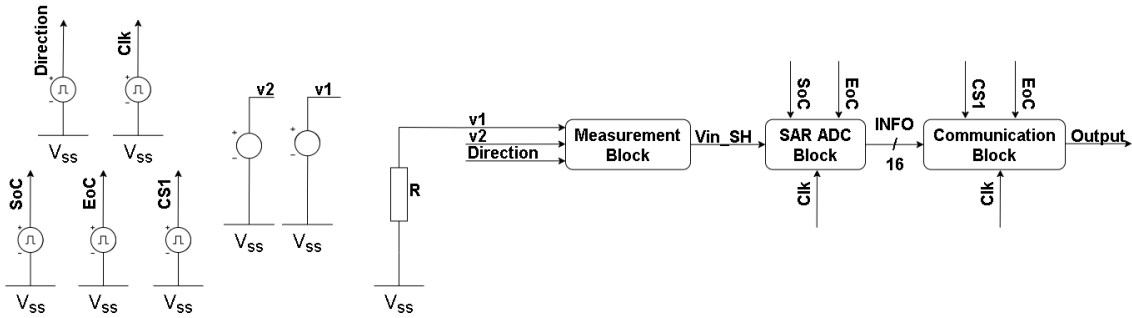

Figure 8.1: Acquisition System Set-Up

The tests made to simulate the whole Acquisition System layout consists in using a voltage ramp between 0V and 2V in one of the inputs (V1 or V2), keeping the other one grounded. Having a resistor R, to simulate the intrinsic resistance of the scaffold. Moreover, at every 1us, both, the SoC and the EoC signals go from "0" to "1". This way a one-time conversion is started. After that first conversion is done, the converted information is stored in the Communication Block, waiting for the CS1 signal to be active, "1". This activation must be done before another conversion is started and finished because when the conversion finishes the data will be overwritten. Losing the first conversion information. As long as the CS1 remains active for one conversion time, 16 cycles or 800ns the communication block, will send the information to the micro.

The principal information to save from this test is the SDO signal and the current corresponding to every voltage input, V1.

$$SD0_{bin} \rightarrow SD0_{dec} * Vref$$

$$R_{expected} = \frac{SD0_{dec} * Vref}{I_{expected}}$$

With these values and a few calculations, is possible to determine the expected resistance value of the load being tested. In this set-up, the load tested had a value of R=10kΩ, however, the impedance values calculated using the system, SDO data have a few disparities. The graphic, (Fig.8.2), shows the relative error between the resistor used and the expected resistance.
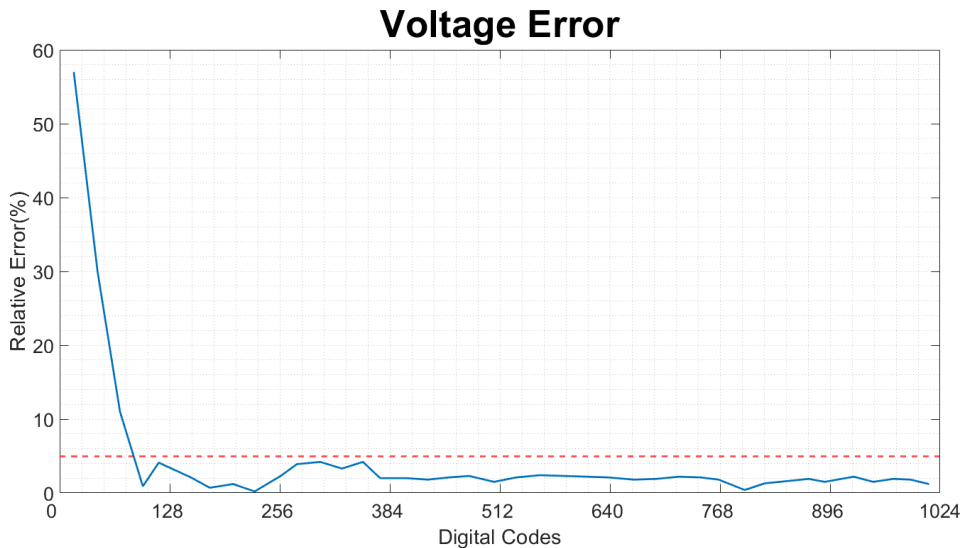

Figure 8.2: Acquisition System Relative Error

The first conclusion to take from this figure is, for a digital code with a lower value, the resistance value expected is not as close to the "real" resistance value. Once more, for values higher than 15uA, or 150mV, the relative error is lower than 5%, which corresponds to 94.2% of all the digital codes available. Moreover, this system could present better results, in the zone lower than 5%, if, for example, the sample and hold block had an output voltage even more constant. Or, if the comparator, in the ADC was even faster, to detect and respond to inputs with voltage differences in the order of the mV. Many modifications can be made to the system to lower the error even more. However, to lower that first 7% is not as easy. After making many tests in that range, it was obvious that the ADC Block was the responsible for this error. The conversions were not correct, because, for these low values the DAC used in the ADC suffers from non linearity, section 5.2.4. Moreover, as stated before in section 3.4, the overall performance of the ADC will reflect the performance of the measurement and control loop. Also, the accuracy of the conversion will depend on the DAC linearity and the comparator noise.

Chapter 9

Conclusion/Future work

The first conclusion of this document is that after designing and testing every block individually, a proof of concept was achieved. The blocks worked as intended and after designing and testing the overall layout for the Acquisition System. The errors were lower than 5% for about 94% of every possible voltage input, being the lower voltages the ones with greater error value. With results like so, it is possible to claim that the layout was successfully done, mainly because of the care taken in chapter 7. Moreover, this dissertation started as a proof of concept in circuit simulation with Cadence Spectre and evolved to a layout and verification with Assura and Virtuoso design environment.

After the realization of the work proposed and the writing of the dissertation document, a few modifications could be done to the system to improve it, future work.

- DAC - As stated before the charge scaling converter non linearity property, influences the ADC result. Since this DAC is sensitive to parasitic elements, which generate non linearity at the low voltages. A possible solution is to implement a converter with charge scaling for the MSBs and voltage scaling for the LSBs. Since the R-2R ladder DAC is not sensitive to parasitic elements, the merge of these two DAC configurations might achieve better results.

- Remove EoC - The signal EoC has the role of ending the conversion sequence and resetting the flip-flops of the SAR Logic Block. However, this signal needs to be externally generated, which might cause errors if the timing of the signal is not perfect.

  A way to recreate this signal without external help could be as follows. Using another Sample and Hold Block to keep the output value stable. The logic behind this diagram is, when SoC goes "high" the Or' signal copies the start signal, acting as the clock for the S&H Block. Since the input value is delayed, SoC', when the Or' goes "low" and the S&H goes in holding state the Soc' is still at "high". This way is possible to force the output of the S&H to be at "high". This signal will enter another Counter Block, which will count to 16, after that the Enable signal will to "high", and the Or' will recreate that signal

once more. Forcing the S&H to sample again, this time since a conversion was not asked for the SoC will be "low". Forcing the Eoc signal to go "low" as well. This way it is possible to recreate the exact EoC signal used for the whole system with two very low cost and space blocks plus two logic gates.
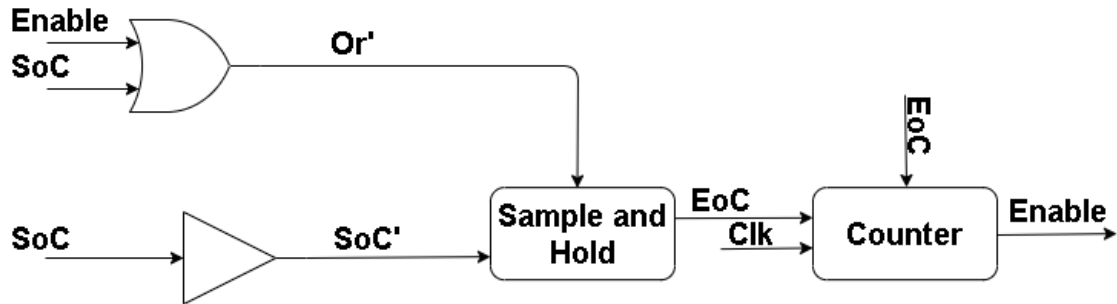

Figure 9.1: Remove EoC diagram Block

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