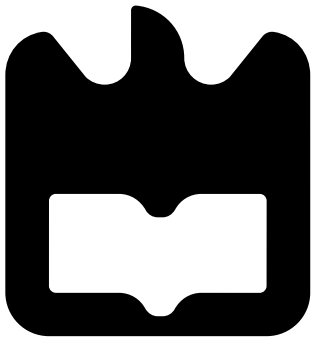
Cristiano Ferreira Gonçalves

Amplificadores de Potência para Radiofrequência Insensíveis à Impedância de Carga

Load Insensitive Radio Frequency Power Amplifiers



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Load Insensitive Radio Frequency Power Amplifiers

Tese apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Doutor em Engenharia Eletrotécnica, realizada sob a orientação científica do Doutor Pedro Miguel da Silva Cabral, Professor Auxiliar do Departamento de Eletrónica, Telecomunicações e Informática da Universidade de Aveiro e coorientação científica do Doutor José Carlos Esteves Duarte Pedro, Professor Catedrático do Departamento de Eletrónica, Telecomunicações e Informática da Universidade de Aveiro.

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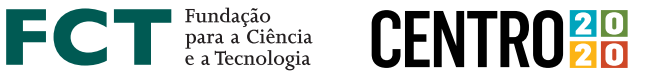

o júri

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palavras-chave

Amplificadores de potência, amplificadores Doherty, insensibilidade à carga, malhas de adaptação sintonizáveis, medição de impedância, modulação de tensão de alimentação.

resumo

Os amplificadores de potência de estado sólido (SSPAs) evoluíram significativamente nas últimas décadas, principalmente devido à utilização de novas tecnologias de transístores, como os transístores de alta mobilidade (HEMTs) de nitreto de gálio (GaN), de ferramentas muito avançadas de projeto assistido por computador (CAD) e de algoritmos de pré-distorção digital (DPD) muito evoluídos. Isto levou a uma melhoria de desempenho considerável, em termos de eficiência energética, potência de saída e linearidade. Normalmente, para obter estes níveis de desempenho, os engenheiros projetam os amplificadores permitindo que os transístores utilizados operem muito perto do seu limite físico de funcionamento seguro e considerando que vão operar para uma carga fixa. No entanto, os amplificadores projetados são utilizados em diversas aplicações industriais e/ou telecomunicações e, em alguns casos, como por exemplo fornos micro-ondas ou estações base 5G, a sua carga de saída pode variar devido a várias causas, que podem ser previsíveis ou imprevisíveis. Neste cenário não ideal, os transístores utilizados operam para cargas não ótimas e o desempenho dos amplificadores pode ser muito degradado. Além disso, em projetos muito otimizados, onde os transístores são operados perto do seu limite de funcionamento seguro, a sua durabilidade pode ser reduzida ou, em casos extremos, podem até ser permanentemente danificados. Portanto, para melhorar o desempenho dos amplificadores em cenários de carga variável, são necessárias novas arquiteturas e/ou técnicas que visam reduzir a variação da carga vista pelos transístores utilizados. Esta tese apresenta várias estratégias para melhorar a insensibilidade dos amplificadores em relação à variação de carga. As técnicas apresentadas são baseadas em malhas de adaptação dinâmicas (TMNs) e na variação da tensão de alimentação dos amplificadores. As malhas de adaptação desenvolvidas permitiram reduzir a variação de carga vista pelo amplificador e a variação da sua tensão de alimentação permitiu melhorar o desempenho para operação com cargas não ótimas. Estas abordagens foram testadas e validadas em amplificadores baseados num só transístor, e, posteriormente, com base nas suas vantagens e desvantagens, a técnica mais promissora – a modulação da tensão de alimentação – foi selecionada para o projeto de um amplificador Doherty, que é imprescindível para telecomunicações. Além disso, como em algumas aplicações a variação da carga de saída pode ser imprevisível, também desenvolvemos um sistema completo que inclui um circuito de medida de impedância e compensação do desempenho do amplificador em tempo real.

keywords

Doherty amplifiers, impedance measurement, load insensitivity, power amplifiers, supply voltage modulation, tunable matching networks.

abstract

Solid state power amplifiers (SSPAs) evolved significantly over the last few decades, mainly, due to the use of new transistor technologies, such as gallium nitride (GaN) high-electron-mobility transistors (HEMTs), very advanced computer-aided design (CAD) software, and very effective digital pre-distortion (DPD) algorithms. This led to a considerable performance improvement, in terms of energy efficiency, output power, and linearity. To achieve this performance, power amplifier (PA) designers normally push the used transistors very close to their physical safe operating limits, and consider them to operate for a fixed output load. However, the designed PAs are used for many different industrial and/or telecommunication applications, and, in some cases, such as, for example, microwave cooking or massive multiple-input multiple-output (MIMO) fifth generation (5G) base stations (BSs), the output load of these amplifiers can change. Under this non-optimal scenario, the used transistors will operate for non-nominal loads, and the PAs performance can be severely degraded. Moreover, in highly optimized designs, where the transistors are operated close to their safe limits, their reliability can be reduced or, in extreme cases, they can even be permanently damaged. Therefore, load insensitive PA architectures, and/or techniques that aim at reducing the load variation seen by the PA, are necessary to improve the performance under load varying scenarios. This thesis presents various strategies to improve load insensitiveness of PAs. The presented techniques are based on tunable matching networks (TMNs) and on the amplifiers' drain supply voltage (V_{DS}) variation. The developed TMNs successfully reduced the load variation seen by the PA, and its performance was greatly improved, for non-optimal loading, by also using the derived load dependent V_{DS} variation. These different approaches were tested and validated on single-ended PAs and then, based on their advantages and disadvantages, the most promising technique – the supply voltage modulation – was selected for the design of a Doherty power amplifier (DPA), which is of paramount importance for telecommunication applications. Moreover, since in some applications the output load variation can be unpredictable, we also developed a complete quasi-load insensitive (QLI) PA system that includes an impedance tracking circuit and an automatic real-time compensation of the amplifier performance.

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List of Acronyms

4G fourth generation

5G fifth generation

ACPR adjacent channel power ratio

BO back-off

BS base station

BST barium strontium titanate

CAD computer-aided design

CMOS complementary metal-oxide-semiconductor

CW continuous wave

dc direct current

DC duty-cycle

DE drain efficiency

DLM dynamic load modulation

DPA Doherty power amplifier

DPD digital pre-distortion

FET field effect transistor

FP full power

GaAs gallium arsenide

GaN gallium nitride

HBT heterojunction bipolar transistor

HEMT high-electron-mobility transistor

IBO input power back-off

IL insertion loss

LDMOS laterally-diffused metal-oxide semiconductor

LMBA load modulated balanced amplifier

LP load pull

MEMS micro-electromechanical systems

MIMO multiple-input multiple-output

MMIC monolithic microwave integrated circuit

mmWave millimeter-wave

MCU microcontroller unit

OMN output matching network

OBO output power back-off

PA power amplifier

PAE power added efficiency

PAPR peak-to-average power ratio

PECVD plasma-enhanced chemical vapor deposition

PWM pulse-width modulation

QAM quadrature amplitude modulation

QLI quasi-load insensitive

RCN reactance compression network

RF radio frequency

SiGe silicon-germanium

SOI silicon on insulator

SSPA solid state power amplifier

TLRCN transmission line compression network

TMN tunable matching network

TOMN tunable output matching network

$\boldsymbol{V_{DS}}$ drain supply voltage

VNA vector network analyzer

VSWR voltage standing wave ratio

Chapter 1

Introduction

Nowadays, power amplifiers (PAs) are used for various applications and their performance has a considerable impact on the overall system operation. Therefore, in order to achieve the best performance possible in terms of output power density, direct current (dc) to radio frequency (RF) conversion efficiency, and linearity, often, the used transistors are used close to their physical safe operation limits. This design approach results in better performance for operation under the expected nominal output load. However, for specific operating conditions, PAs can be forced to operate under varying output load scenarios. In this non-optimal regime, the PA performance is degraded, mainly in terms of output power, drain efficiency (DE) and linearity. Moreover, since the devices are used close to their safe operation limits, changes to the PA expected operation environment can lead to severe reliability degradation or even permanent damage.

This non-optimal operating regime can happen due to various causes, and in different scenarios. Some of these scenarios include industrial applications of PAs, such as:

- **microwave cooking,**

  where a high power solid state power amplifier (SSPA) is used as the microwave energy source for heating food in the oven cavity. In these applications, the PA output load, which is the cavity impedance, shows a strong dependency with the type of food that is inside the oven [1];

- **plasma-enhanced chemical vapor deposition (PECVD),**

  where plasma conditions inside the deposition chamber are required to vary during the deposition process. This variation also leads to changes in the output impedance of the RF generator [2];

- **particle accelerators,**

  where charged RF cavities are used to accelerate charged particle beams. In this case, the amount of reflected power changes due to the interaction between the cavity and the charged particle beam, causing an output impedance variation from the RF generator perspective [3].

Other load variation scenarios can be found in **telecommunication applications**, where the PA output load can also change due to moving objects on the antenna proximity, e.g., the hand effect [4], or also due to mutual coupling between different antenna elements on fifth generation (5G) massive multiple-input multiple-output (MIMO) base stations (BSs) [5].

In the case of massive MIMO scenarios, as illustrated on Fig. 1.1, each antenna element is affected by its neighboring elements due to mutual coupling, which will cause an apparent load change for the PAs in each transmit path [6]. So, while the use of antenna arrays enables beamforming, which leads to an overall system efficiency improvement, this load variation results in PA performance degradation, making the use of such systems less viable.

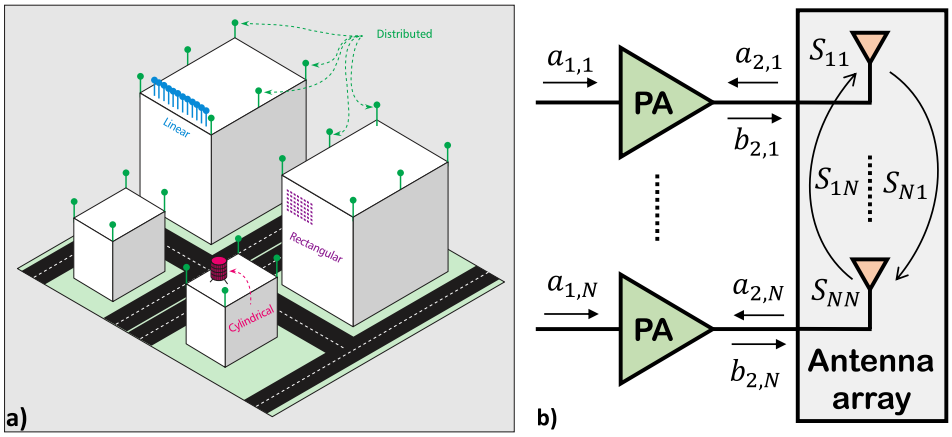

Figure 1.1: a) Likely scenario for massive MIMO deployment, where different types of antenna arrays can be spotted, from [7]. b) Mutual coupling between antenna elements and its effect on the PA output load (where $b_{2,n}$ and $a_{2,n}$ are, respectively, the incident and reflected waves on each antenna element).

The described scenarios have demonstrated the importance of considering non-optimal output load variations during the design stage of PAs. However, most of the described applications are very complex and it is impracticable for PA designers to replicate these operating conditions. Therefore, in order to quantify the performance degradation of PAs operating in these scenarios, the respective impedance variations can be mimicked by load pull (LP) analysis. Figure 1.2 shows a typical simulated LP analysis of an idealized single-ended class B PA. For practical measurements, various non-optimal impedances need to be synthesized in the laboratory using a load tuner.

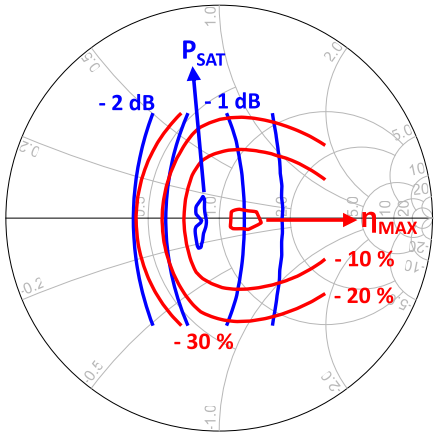

Figure 1.2: LP contours of an idealized class B PA. The DE is shown in red and the output power in blue.

In Fig. 1.2 the LP analysis was performed for non-optimal loads distributed within a 3.0 maximum voltage standing wave ratio (VSWR) circle. Even for this very simplified PA, the DE is degraded by around 30% and the output power is reduced by more than 2 dB, for the worst-case loads. In the following chapter, dedicated LP analyses based on practical implementations of state-of-art PAs are presented and discussed.

1.1 Motivation

In [8], the authors have compared the performance degradation of different PA architectures, all of them based on devices operating in ideal class B, under output load mismatch. The simulated architectures were the typical single-ended amplifier, a Doherty power amplifier (DPA), a balanced amplifier, and a load modulated balanced amplifier (LMBA). This demonstrates that different types of amplifiers have distinct behavior under load mismatch, and, therefore, different levels of performance degradation.

DPAs are widely used in fourth generation (4G) telecommunication systems and believed to continue to be very useful for the next generation 5G BSs. Therefore, their output load sensitivity is an important performance characteristic. In [9] and [10] the authors analyzed the performance degradation of a 2 GHz DPA, for mismatched loads within a worst-case 2.2 VSWR circle. Even for this small mismatch value, the power added efficiency (PAE) was reduced by around 35%, at 6 dB of input power back-off (IBO), and the output power degraded by 1.5 dB. They also showed considerable gain variations, which certainly affect the linearity of the amplifier.

Very efficient single-ended amplifiers, based on, for example, class E operation, are also very interesting for industrial applications, were continuous wave (CW) signals, or signals with very low peak-to-average power ratio (PAPR), are used. In [11] the authors evaluated the load mismatch sensitivity of class E PAs under a maximum VSWR of 10. They have developed a general class E theoretical model that was used to evaluate the output power, PAE, and reliability degradation. The performed simulations and practical measurements have shown very similar results, with up to 10 dB of output power degradation and 50% of efficiency reduction. The amplifier reliability was evaluated by measuring the maximum drain voltage applied to the device, which can increase to extremely high values for mismatched class E operation, and cause serious reliability issues. The authors measured a worst-case maximum voltage of 4.5 times the nominal drain supply voltage (V_{DS}).

These examples shown how important can be the impact of output load mismatch on the performance of PAs. In order to solve this problem, various researchers have started to evaluate different ways to isolate PAs from their output loads, so that load variations do not affect the PA performance. Unfortunately, typical magnetic isolators are unwanted, since they do not maintain the PA output power, and reduce the compound efficiency due to the reflected power dissipation on a dummy load. Moreover, they are difficult to integrate in monolithic microwave integrated circuits (MMICs) and are too bulky and heavy when compared to the PA itself [12], [13]. The last argument is especially important for telecommunication applications, where the integration of the whole RF chain is very important to reduce the cost of 5G BSs, which is decisive since they are expected to be mass deployed.

Therefore, RF engineers need to design non-typical isolators, novel load insensitive PAs architectures or specific adaptive output matching networks (OMNs). Otherwise, the output power, efficiency and linearity of PAs will be severely degraded, and, consequently, impact the system performance for the various described applications.

1.2 Outline

In Chapter 2, the state-of-the-art on techniques for the compensation of PAs operating under non-optimal loading is described. The first section presents various PA architectures that are, naturally, more insensitive to load variations in terms of output power or efficiency. The second section describes techniques that improve isolation at the PAs OMN. Some of the presented techniques are the dynamically adjustable matching networks, which are based on variable or switchable components. Therefore, we also present a brief state-of-the-art on these components and their technologies. The third section is devoted to a brief description of the latest compact and dedicated impedance measurement techniques for application on PAs.

In Chapter 3, based on the motivation that was presented during the introduction of this thesis, and on the existent state-of-the-art solutions, we define the main objective and goals of this work.

In Chapter 4, we present the developed work, and highlight its main contributions. In the second section, we introduce the implemented tunable matching network (TMN), based on switched shunt stubs, that is fully described in the paper of appendix A. The third section presents a novel technique that allows to measure the output impedance of PAs without introducing prohibitive losses. This technique is completely described and explained on the paper of appendix B. On the fourth section we introduce a new concept to compensate the performance of SSPA, without introducing additional OMN losses. The proposed technique is based on the correct variation of the transistor's V_{DS}. This concept was validated for single-ended PAs, as shown in the papers of appendices C and D. Later, it was also expanded for DPA operation, where it was shown to improve the back-off (BO) and full power (FP) amplifiers' performance, as shown in appendices E and F.

In Chapter 5, the innovative contributions of the developed work are summarized and the published papers are enumerated.

Lastly, Chapter 6 identifies the main conclusions of this PhD thesis and in Chapter 7 we propose relevant next steps to continue this research topic, and improvement tips for the developed prototypes.

Chapter 2

State-of-the-Art

This chapter presents the most recent findings on load insensitive PA topologies, and the most recently developed techniques that can be included in PA designs to improve their load insensitiveness. The first section of this chapter describes some PA architectures that are, naturally, more insensitive to load variations. On the second section, various types of matching networks with isolation or compression characteristics are shown, and its possible implementation on PAs OMNs is discussed. Lastly, on third section, some compact and low loss impedance measurement techniques are described, and evaluated for application at the output of high power amplifiers.

2.1 Load Insensitive PA Architectures

As previously explained, load insensitive PAs have great value for next generation MIMO transceivers and many other applications. Typical architectures and classes of operation are heavily affected by dynamic load variations, as shown in [9–11]. During this section various state-of-the-art load insensitive PA designs will be introduced and briefly described.

2.1.1 Quasi-Load Insensitive Class E

Class E amplifiers have been widely studied during the last years, mainly because of their high conversion efficiency. In [14], a variable slope operation mode was analyzed. This is a more general class E operation, which forces a switching $\left(t = \frac{2\pi}{w}\right)$ zero voltage condition, as defined in equation (2.1), while allowing a variable slope condition ($k \neq 0$), as presented in equation (2.2) for the operating frequency, w, and drain voltage, V_{DD}. This allows for more relaxed designs while maintaining high efficiency. In [15], different modes of operation were also deduced as a function of the resonance factor, q. This factor, defined in equation (2.3), represents the ratio between the resonance frequency of the class E parallel LC tank and the operating frequency, w.

$$V_c\left(\frac{2\pi}{w}\right) = 0 \tag{2.1}$$

$$\frac{dV_c(t)}{dt}_{\left(t=\frac{2\pi}{w}\right)} = wV_{DD}k \tag{2.2}$$

$$q = \frac{1}{w\sqrt{LC}} \tag{2.3}$$

Later, in [16] and [17], Qureshi *et al*, using the conditions derived in [14] and [15], shown that for a $q = 1.3$, the class E operation maintains optimum efficiency over a wide range of load resistances (purely real output impedances). In fact, when the design parameters are chosen for this specific value of q, the efficiency load pull contours become aligned with the real axis of the Smith chart. Therefore, optimum efficiency is achieved for real loads, as shown in Figure 2.1. The authors named this particular operation as quasi-load insensitive (QLI) class E, and it was demonstrated to be very useful for the design of Doherty and Outphasing PAs, due to the high efficiency achieved throughout the dynamic load modulation (DLM).

However, a QLI class E cannot maintain high efficiency when applied to general load variations, where the load can also become complex. A single ended QLI class E is also unable to maintain the output power constant for real load variations, since the output power contours are perpendicular to the real axis of the smith chart, as shown in Figure 2.1.

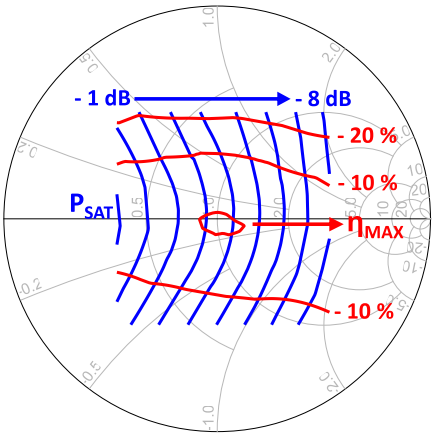

Figure 2.1: LP analysis of a class E PA based on the design equations for a $q = 1.3$. Drain efficiency in red and output power in blue.

2.1.2 Balanced PAs

Balanced PAs, as shown in Figure 2.2, composed by two amplifiers and two quadrature couplers, are known to be insensitive to load variations in terms of output power and gain. It can be shown that, for an hybrid coupler defined by the S-parameters of equation (2.4), the reflection coefficient observed by each of the amplifiers composing the balanced PA has opposite phase for any output load variation, as presented in equation (2.5). Therefore, each amplifier will experience load variations with equal amplitude but opposite phase. Consequently, if the PAs are not designed for the maximum power load, the output power of one PA will decrease, while the other's will increase, producing a constant combined output power. In figure 2.3 the output power LP contours and impedance variation of each PA is shown for better visualization of the phenomenon.

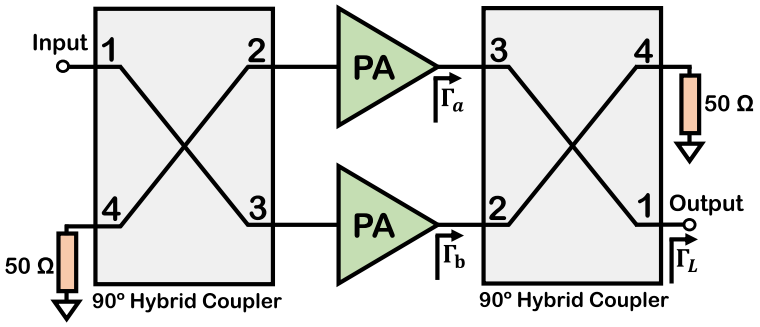

Figure 2.2: Balanced PA block diagram.

$$[S] = \begin{bmatrix} 0 & \frac{e^{-j\frac{\pi}{2}}}{\sqrt{2}} & \frac{e^{-j\pi}}{\sqrt{2}} \\ \frac{e^{-j\frac{\pi}{2}}}{\sqrt{2}} & 0 & 0 \\ \frac{e^{-j\pi}}{\sqrt{2}} & 0 & 0 \end{bmatrix} \tag{2.4}$$

$$\Gamma_a = \Gamma_L \ \ and \ \ \Gamma_b = \Gamma_L e^{-j\pi} \tag{2.5}$$

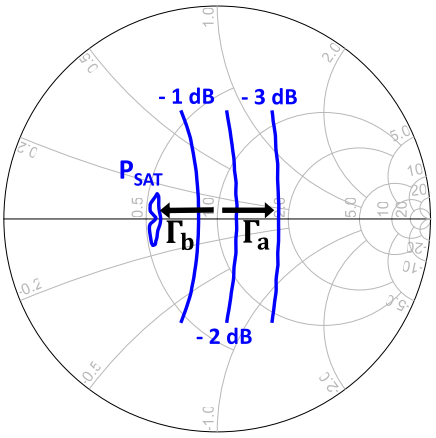

Figure 2.3: Output power LP contours and opposite phase load variations, which correspond to the Γ seen by each amplifier composing the balanced PA.

In [18], the authors designed a balanced silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) amplifier. It operates at 835 MHz with an output power of 28.5 dBm and a single tone PAE of 51%. The PA maximum output power and gain variations are 1.5 dB under a load mismatch correspondent to a maximum VSWR of 4:1.

A balanced architecture was also used in [19] and [20]. The designed complementary metal-oxide-semiconductor (CMOS) amplifier operates at 1.95 GHz with a maximum output power of 26.4 dBm and a peak PAE of 35 %. In this case, the load sensitivity analysis was performed for a VSWR of 2.5. The obtained gain variation was 1 dB for the balanced PA, while each single-ended amplifier composing it presented a 6 dB variation for the same load mismatch.

However, for unmatched output loads, the isolation port of the quadrature coupler can receive power that is dissipated on a dummy load, reducing the efficiency. In [21] the authors included an RF-to-dc rectifier between the isolation port of the coupler and the V_{DS} source to restore the power that would be dissipated at the isolation load. For a 50 Ω output load, the amplifier's single tone output power was 37 dBm with 65 % of PAE, at 836.5 MHz. Using this technique, the amplifier's efficiency variation (at 25 dBm of output power) was reduced by 4 % for a 2:1 VSWR circle and by 6 % for 4:1. This technique was proven to be very advantageous to reduce the load mismatch sensitivity of balanced amplifiers in terms of efficiency.

2.1.3 Digital Doherty PAs

DPAs are widely used in telecommunication systems, operating with high PAPR signals, due to their improved BO efficiency. However, their analog typical implementation has several disadvantages, mainly due to imperfect interaction between the carrier and peaking amplifiers, such as non-optimal phase delays or gain unbalances. Multi-input DPAs have been proposed to solve this problem. In these amplifiers the amplitude and phase of the input signals can be controlled independently, providing another degree of freedom, to achieve the best possible performance. Since their DLM can be digitally controlled, it can also be explored to dynamically compensate output load variations.

In [22], the authors demonstrated that by varying the relative phase and amplitude of the carrier and peaking input signals, the performance degradation caused by non-optimal

loading can be mitigated. For higher than optimal output loads, which are inverted and seen as smaller by the carrier amplifier, the peaking load modulation effect must be reduced by decreasing the peaking maximum current. Thus, the carrier FP load is not decreased below its optimal value. However, the amplifier's BO level is reduced, due to the decreased peaking and carrier amplifier currents ratio and, consequently, reduced load modulation. This compensation effect can be seen in Fig. 2.4 and Fig. 2.5, for FP and BO, respectively. In Fig. 2.5, for BO, the compensation is much less effective, due to the BO level reduction, as explained before.

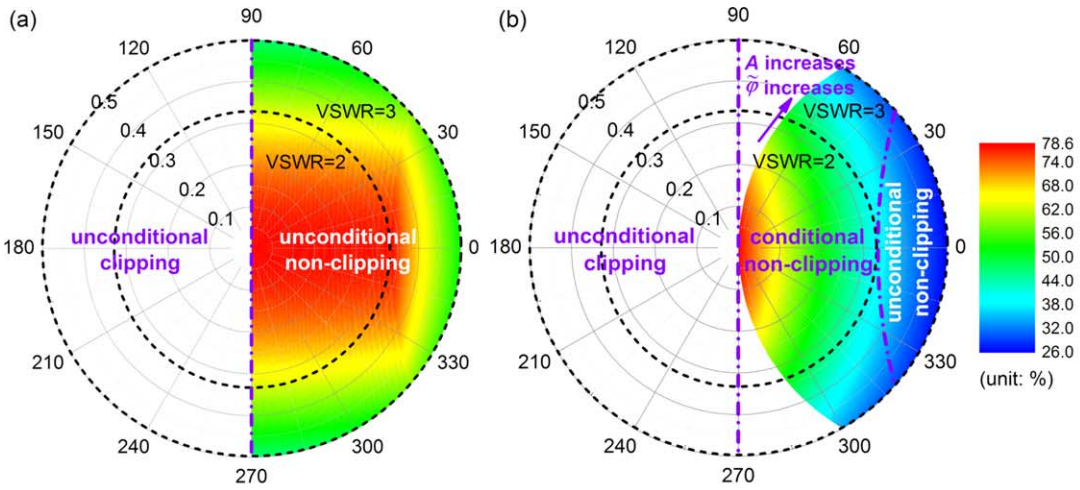

Figure 2.4: Compensated (a) and original (b) LP analysis of the digital DPA, for FP operation, from [22].

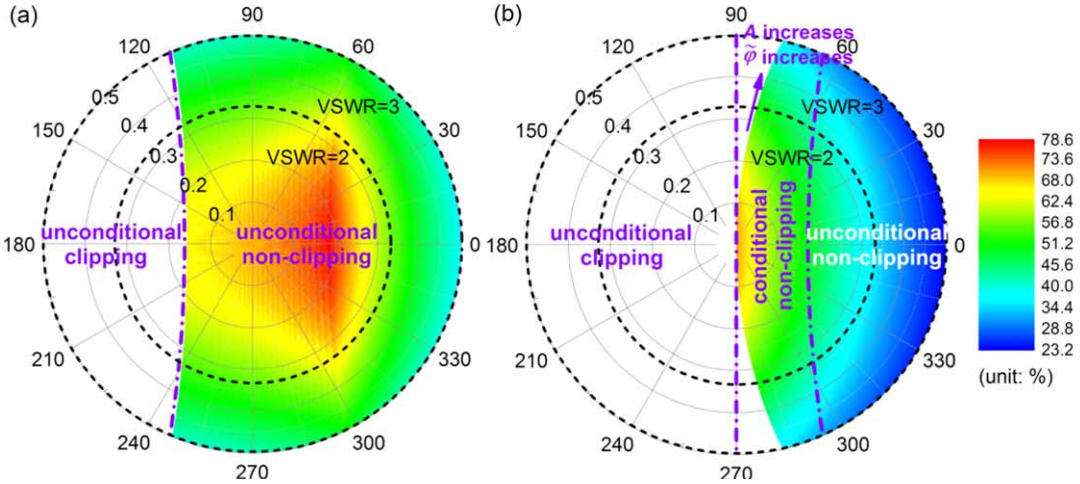

Figure 2.5: Compensated (a) and original (b) LP analysis of the digital DPA, for the 3dB OBO level, from [22].

On the other hand, for lower than optimal output loads, the carrier will see higher loads and consequently a stronger peaking load modulation would be necessary to reduce the load further. For this case, the compensation is done by increasing the peaking current. However,

this can only be done during back-off operation, since the peaking is not yet providing its maximum RF current. In this scenario, the peaking current reaches its maximum value before FP, and so, after this point the carrier amplifier will become saturated by voltage at the transistor's triode region. This effect is also shown in Fig. 2.4 and Fig. 2.5, where the authors identified the left part of the Smith as an unsafe voltage clipping area and did not characterize the amplifier for these loads. However, this region can be reduced by increasing the peaking current capability (or reducing the carrier maximum current level). This allows to further reduce the carrier load, and prevent it from voltage clipping, as shown in Fig. 2.6, where the authors considered an asymmetrical DPA with a peaking device size correspondent to twice the carrier size.

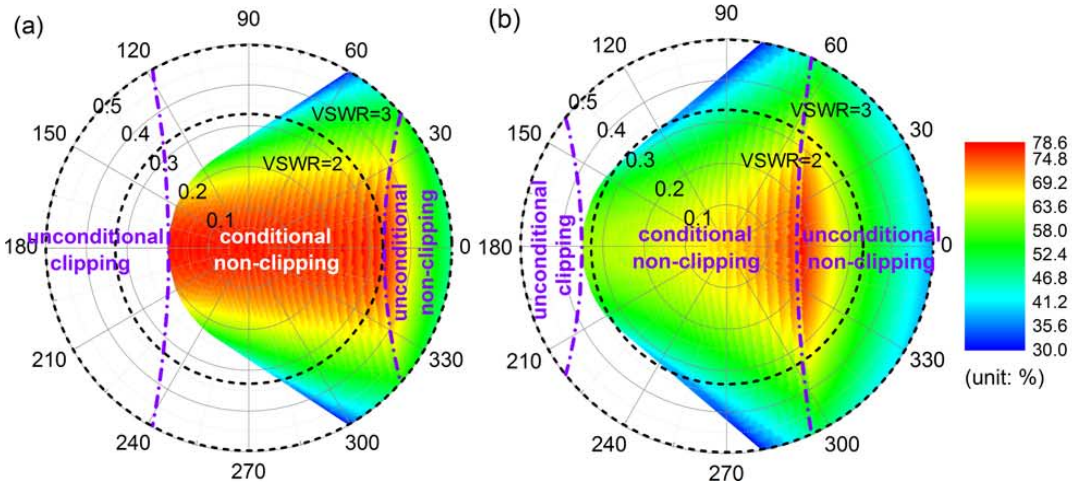

Figure 2.6: Compensated DPA FP (a) and 3dB OBO (b) DE, from [22], for an asymmetrical DPA.

So, for higher than optimal output loads, the DPA efficiency can be compensated at FP, by reducing the carrier load modulation, however the BO level is reduced and the output power decreased, due to the lower peaking contribution. Note that, in Fig. 2.6 b), the efficiency appears to be compensated at BO, for higher loads, because it is analyzed only for the 3 dB level. However, instead of reducing the load modulation, if we increase the carrier device size, the BO performance and full power level can also be restored. For this compensation method to be effective, the carrier maximum current must change depending upon the load, thus, for the nominal load only part of the available device current capability should be used.

In [23], the authors present a DPA where both the carrier and peaking drain current capability and phases can be adjusted using switched parallel transistors at the output stage, and tunable phase delay lines at the input, respectively. This design grants a good performance compensation for higher than optimal loads, but they go a step further, and design a combiner that allows to change the carrier and peaking roles to compensate the other "half" of the Smith chart, i.e. smaller than optimal loads. The reconfigurable series/parallel DPA combiner is based on a quadrature coupler, which includes a switch at the isolation port to change the operation mode. Moreover, the bias voltage sources are adaptive so the gate biasing is also interchangeable between the devices. The authors can achieve a worst-case output power and FP PAE degradation of 1.7 dB and approximately 10 %, respectively, for loads across a 3:1 VSWR circle. Note also that the drain current capability of the carrier/peaking

devices is set to approximately half of the maximum value for operation with a 50 Ω nominal load, as expected.

2.2 Isolation at OMN

None of the analyzed PA architectures is completely load insensitive in terms of efficiency, gain and output power. Therefore, since some performance degradation is still expected, it may be helpful to further improve the load insensitiveness by increasing the isolation between the PA and its output load. For this purpose, during this section, various TMN topologies and techniques are described, and their possible application on PA OMNs is discussed.

2.2.1 Magnetic Isolator

The typical magnetic isolator between the PA and its load, as shown in Figure 2.7, is still used in modern systems. Its ideal S-parameters are presented in equation 2.6. This ideal isolator delivers the incident wave to the antenna, and, in case of any load mismatch, the reflected wave is entirely delivered to the isolation load. Therefore, the amplifier do not see non-optimal load variations. However, note that real isolators have considerable insertion loss (IL) and finite isolation. Moreover, since the reflected power is dissipated at a dummy load, for large mismatch levels, the compound efficiency is greatly reduced and the delivered power to the load is decreased.

Another problem, which is very decisive for telecommunication applications, is that typical isolators are difficult to integrate in MMICs, and the RF chain of future networks will probably be fully integrated in order to reduce implementation costs. To avoid large and costly MMICs or big and heavy hybrid circuits, an effort is being made in the research for different solutions. Notice that, in order to be competitive, these solutions must protect the PA, providing satisfactory isolation, and have an acceptable IL. Unfortunately, most of the state-of-the-art integrated active isolators still have very high IL (≈2.5 dB), dramatically reducing the compound efficiency [12, 24, 25].

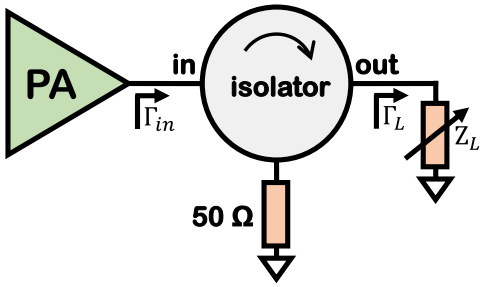

Figure 2.7: PA connected to the output load through an isolator, in this example Z_0 is equal to 50 Ω.

$$[S] = \begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix} \tag{2.6}$$

2.2.2 Compression Networks

Compression networks are capable of reducing the impedance variation at one port. However, it can be proved that, for having compression with passive and reciprocal networks they must have more than 2 ports, as shown in Figure 2.8. For this case, the input reflection coefficient, Γ_{in}, can be smaller than all the output ones, $\Gamma_{L_1} - \Gamma_{L_N}$, with $N \geq 2$.

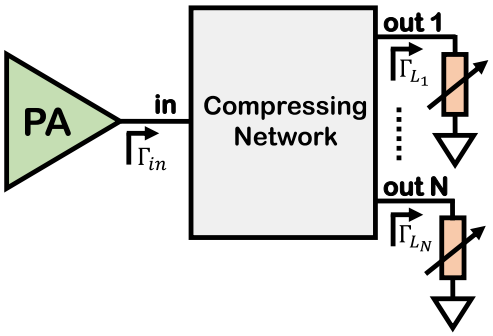

Figure 2.8: (N+1) port compression network.

One approach that has been widely explored is the network presented in Figure 2.9, based on two parallel reactive branches, one inductive and other capacitive. This network can compress load variations as long as they are equal and synchronous at both output ports [26]. It was firstly implemented in [26], with lumped elements and applied to the rectifier stage of resonant dc-to-dc converters. The objective was to improve the conversion efficiency by reducing the load variation seen by their transforming stages. The authors were able to compress load variations of 100:1 and 2:1 into 5.05:1 and 1.06:1, respectively.

After, in [27], the authors used an rf-to-dc converter at the isolation port of an outphasing PA combiner. The objective was to restore some power that otherwise would be dissipated at the isolation load. However, the rf-to-dc converter input impedance variation decreases the isolation of the PA combiner. In order to reduce this load variation, a compression network was added to the rectifier stage of the converter. The implemented system improved the overall efficiency of the outphasing PA from 17.9 % to 42 % under a 16-quadrature amplitude modulation (QAM) signal with a PAPR of 6.5 dB.

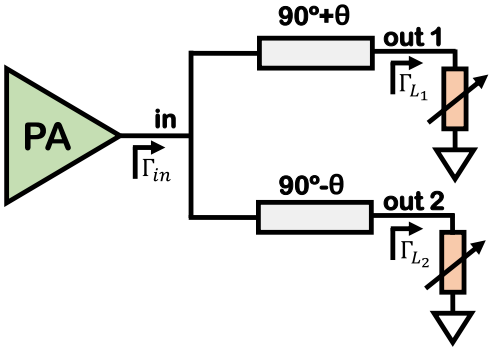

Figure 2.9: Transmission line compression network.

Later, in [28], this compression network was implemented using transmission lines, as shown in 2.9. The authors have achieved a compression of 6.7x, from an original 20:1 load variation to a compressed value of 3:1. These transmission line compression networks (TLRCNs) raised the interest of researchers due to its easier implementation at higher frequencies, and possible use on various applications, such as microwave rectifiers [29].

For the problem presented in this PhD thesis, TLRCNs would be tremendously beneficial. However, in order to use them, at least two independent and identically varying output loads are necessary. So, for the envisaged applications, TLRCNs are not straight forward

to implement, requiring the connection of one PA to two identical loads with synchronous variations.

2.2.3 Tunable Matching Networks

TMNs perform an impedance matching that can be dynamically modified by adjusting variable components, controlled by analog or digital inputs. During this section, the use of TMN techniques at the OMN of amplifiers, as shown in Figure 2.10, will be discussed.

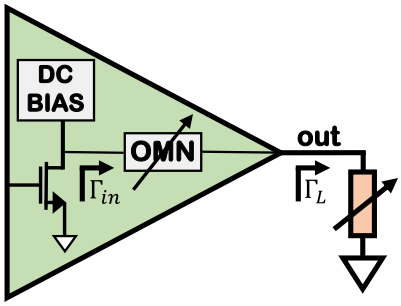

Figure 2.10: PA design including a tunable OMN.

The objective of tunable output matching networks (TOMNs) is to adjust the load presented to the transistor in order to achieve better performance for operation under specific environments. They have been successfully used for different purposes, such as:

- perform DLM, in order to improve the BO performance of amplifiers without using more complex PA architectures, such as DPAs or outphasing amplifiers;
- keep the load presented to the transistor constant, in order to maintain the PA performance under output load variations;
- change the frequency behavior of the PA to switch between different working frequency bands.

For the application presented on this PhD thesis, TOMNs are useful to restore the optimal device impedance under operation for non-optimal output loads, thus improve the PA performance under this scenario. Therefore, the control inputs of such networks should be dependent on the output mismatch level. Then, in order to make matching networks adjustable, it is necessary to dynamically change some of their components' values. Transmission lines length and width cannot be varied easily and coils are not very good at higher frequencies. However, the impedance matching of networks can be changed by using variable capacitors, variable length stubs or switched parallel transmission lines.

In what concerns variable capacitors, there are many different available technologies, as for example, varactors and barium strontium titanate (BST) capacitors. Switches can also be used to implement variable capacitor banks, using various fixed value capacitors, as shown in Fig. 2.11.

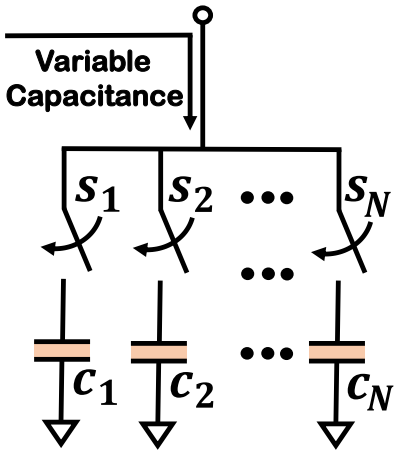

Figure 2.11: Example of a widely used capacitor bank circuit topology.

The same switch technologies can also be used to implement switched variable length stubs or switched parallel transmission lines. For example, in [30], the authors change the characteristic impedance of transmission lines by using switches to connect various lines in parallel or to change the ground plane of these microstrip lines. The length variation of shunt stubs can also be used to change their inductive or capacitive input impedance. This can be done by using shunt switches that change the effective length of the stub, as shown in Fig. 2.12.

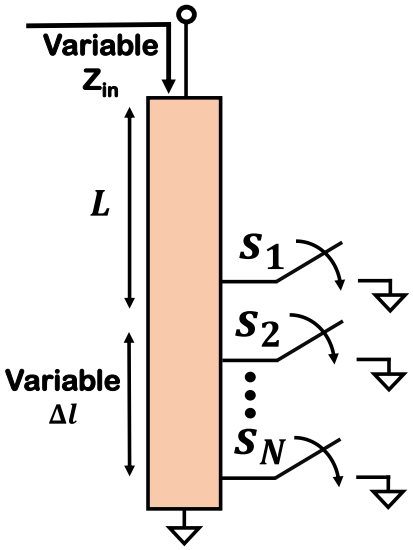

Figure 2.12: Scheme of a variable length stub.

Concluding, TMNs can be implemented with many different topologies and using various components and/or technologies. The isolation capability is obtained by dynamically changing the impedance transformation, however, further research is necessary on the added losses of these networks and on the used variable capacitors or switching elements. Varactors are known to suffer from non-linearity effects and require power from the control source. micro-electromechanical systems (MEMS) switches offer the lowest losses, however, they still need

improvement in the manufacturing process and suffer from reliability issues. CMOS switches are reliable and easy to integrate but need further research in order to reduce their losses.

Following, we present some practical implementations. Although they are used with different objectives, the aim is to evaluate the advantages and disadvantages of each technology, considering the possibility to implement them on the application that is presented during this PhD thesis.

Varactors

Varactor diodes are used as analog variable capacitors, in which the capacitance can be continuously changed by the inverse voltage applied to its terminals [31]. Therefore, TOMNs implemented with varactors can be continuously varied, while switched implementations only allow for step variations. However, varactors characteristic capacitance versus voltage is non-linear, requiring for more complicated characterization processes and control circuits. Under large signal operation they can suffer from linearity issues due to the undesired self-bias that causes a capacitance variation. Moreover, high power varactors require high control voltages (up to 70 V) and a non negligible control power [32].

In [33], the authors implemented a varactor based TOMN in order to realized a multi-band class AB PA with high back-off efficiency. The amplifier could be tuned to work from 900 MHz to 2100 MHz with more than 30 % of efficiency at 10 dB of output power back-off (OBO). The disadvantage of this design is the OMN extra IL. Depending on the output power, the losses can vary between 1 dB and 2.5 dB, which corresponds to 12 % and 30 % of efficiency degradation, respectively.

In [34], a varactor based TOMN was also explored for DLM of PAs. The authors proposed the design of a 1 GHz class E laterally-diffused metal-oxide semiconductor (LDMOS) PA with improved back-off efficiency. More than 20 % of improvement at 10 dB of OBO was expected considering the optimal load modulation and a lossless network. However, the measured results shown only 10 % of improvement at the same power back-off level, and more than 0.4 dB of losses in the varactors.

MEMS Switches

MEMS switches behave as micrometer mechanical relays. They also have metal contacts, as seen in Figure 2.13, however, they are actuated by electrostatic force instead of electromagnetic force. Due to the mechanical relay-like action, they have low IL, high isolation and broadband operation, which are great advantages for the design of tunable RF matching networks [35].

MEMS switches have been used to select different capacitors and realize a frequency reconfigurable OMN [36]. In this work, the network was used to design a frequency reconfigurable PA that can operate in different bands between 8 GHz and 12 GHz.

In [37], the authors used MEMS to realize a 5-bit switched capacitor bank and correct the output impedance change due to extreme hand-effects in mobile devices. The PA was implemented at 900 MHz and 1800 MHz for a nominal output load of 50 Ω, and was able to operate under worst case output impedances of -75j Ω.

In [38], the authors implemented a variable length switched stub with MEMS switches, and designed a TMN capable of covering the entire Smith chart. Unfortunately, no comments were made about the IL in this work.

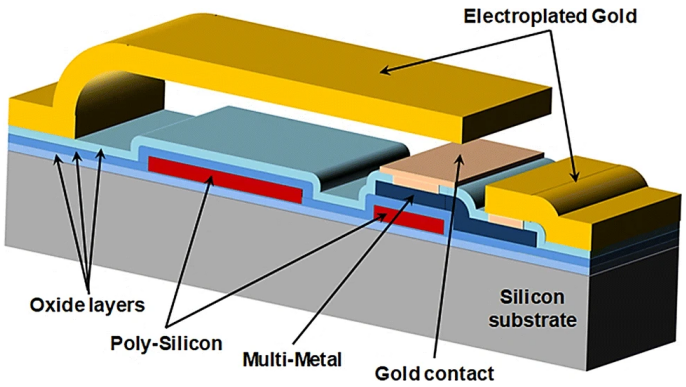

Figure 2.13: Scheme of a typical MEMS switch structure, from [39].

Transistor Switches

Transistors are also used to implement switched matching network designs. These switches impose a small resistor, R_{on}, when set ON, and a small capacitor, C_{off}, at the OFF state. For a predetermined technology, the R_{on} can be decreased at the expense of increasing C_{off}, or vice-versa, but the $[R_{on} \cdot C_{off}]$ value is constant and independent of the gate width, [40]. Based on this benchmark metric, different CMOS field effect transistor (FET) technologies have been tested, and are presented in table 2.1.

Technology	$\boldsymbol{R_{on}[\Omega \cdot mm]}$	$\boldsymbol{C_{off}[fF/mm]}$	$\boldsymbol{R_{on} \cdot C_{off}}$
0.5-μm pHEMT	1.5	240	360
0.15-μm pHEMT	1.5	290	435
0.5-μm SOS	2.8	270	756
0.25-μm SOS	1.6	280	448
0.28-μm SOI	1.2	330	396

Table 2.1: CMOS FET switches state-of-the-art, from [40].

In [41], the authors have implemented a TOMN in order to realize DLM and achieve higher back-off efficiency. They have implemented a switched capacitor bank using silicon on insulator (SOI) CMOS switches. The drain efficiency of the amplifier has been improved by 34 % for 6 dB of OBO, at 2.4 GHz.

In [42], the authors also used SOI CMOS switches to implement a capacitor bank. In this work the objective was to correct linearity issues. The implemented PA was capable of improving the adjacent channel power ratio (ACPR) by 13.7 dB at 1.95 GHz, for an output power of 28.3 dBm.

In [43], the authors compensated the PAE and output power degradation due to antenna mismatch for a maximum reflection coefficient of 0.3. They used CMOS switched capacitors to implement a TOMN for a 2.4 GHz PA, improving the minimum PAE by 14 % and the output power by 3 dB.

In [44], the authors develop tunable transmission lines, based on variable length switched stubs, using MOS and Bipolar switches.

2.3 Compact Impedance Measurement

Most of the described TMN design techniques require analog or digital control signals, which depend on the actual PA output load. Some of the presented PA architectures also require load-dependent reconfigurable circuits and load-dependent input RF signals. Therefore, it is imperative to have real-time information about the output load of the PA. In some cases, as, for example, massive MIMO antenna arrays, where the load variation depends on the mutual coupling between different antenna elements, the load variation can be predicted or pre-characterized by knowing the selected beamforming angle. However, for most of the described applications, this pre-characterization can be difficult or the load variation can be signal dependent. Consequently, it is necessary to, directly or indirectly, measure the output impedance that is actually presented to the PA in real-time.

There are various techniques and commercial equipment capable of measuring the impedance of RF circuits. However, for this application, where the PA output load needs to be measured in real-time and for high power levels, as shown in Fig. 2.14, it is more adequate to design dedicated impedance measurement circuits taking into account specific requirements:

- The acquisition hardware must have **very low IL**. This is an extremely important characteristic for this application, since the circuitry losses added between the PA and its load reduce the delivered output power, and, consequently, have a major detrimental impact on the overall PA efficiency;
- The measurement algorithm should have **low complexity**. Therefore, it will run faster in low cost microcontroller units (MCUs), and also use less power;
- The impedance measurement system should be **low cost**. This is specifically important in systems where various measurement units are necessary.

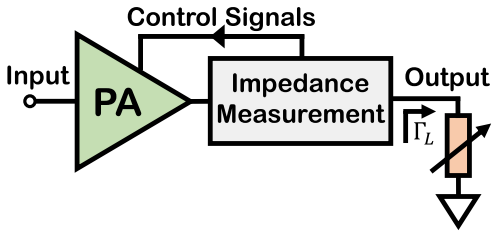

Figure 2.14: Typical application of an impedance measurement circuit between the PA and its output load.

2.3.1 Coupler Based

The latest vector network analyzers (VNAs) are complex systems, and also very bulky and expensive. Some implementations are more miniaturized now, but, even in this case, they are still composed of many sub-circuits and sub-systems, which increase the system cost and add complexity. In [45], the authors developed an Arduino-based miniaturized VNA. They have measured the reflection coefficient of an iPhone 5 antenna, for mismatch levels up to a VSWR of 10.0, and achieved a worst-case amplitude and phase measurement errors of 0.2 dB and 4^{o}, respectively. However, the used couplers introduce a worst-case IL of 0.36 dB, which

is too high for higher power applications. The impedance measurement time varies between some 100 ms and 20 ms.

Throughout time many other measurement systems, also based on bi-directional couplers, have been developed. However, the simplest ones, with lower IL and more compact implementations, have low accuracy. Moreover, some of them are not able to measure both the amplitude and phase of the reflection coefficient. These simpler ones are designed to measure only the amplitude or phase information. More accurate measurement solutions are based on more complex designs, leading to scalability issues and, consequently, an increased production cost.

In [46], the authors use a bi-directional coupler, two RF power detectors, and an analog subtractor to measure only the reflection coefficient amplitude, similarly as illustrated in the block diagram of Fig. 2.15 a).

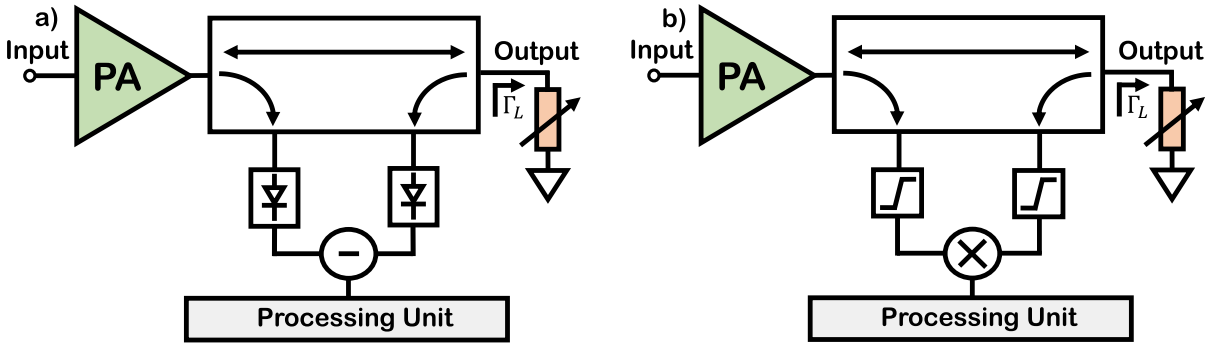

Figure 2.15: Typical system architecture for the measurement of the reflection coefficient amplitude and phase, in a) and b), respectively.

In [47], the authors were able to measure the reflection coefficient phase. However, they were not interested in measuring amplitude variations. The developed system is based on a bi-directional coupler, a 90^{o} fixed phase shifter, two amplitude limiters, and an analog multiplier, as shown in Fig. 2.15 b).

In [48], the authors used two separated circuits to measure both the amplitude and phase of the reflection coefficient. These circuits are based on the same principle as the ones described before, on [46] and [47]. However, since the phase measurement circuit is based on comparators, the authors were only able to detect if the load was inside one region of the Smith chart. This design choice leads to increased complexity and scalability issues for higher resolution measurements, due to the necessity for more hardware to reduce the Smith chart detection regions.

In [49], the authors calculated the reflection coefficient amplitude and phase and compared the obtained values with a fixed reference. The amplitude and phase references were measured, using similar circuitry, from the incident and reflected waves at the output of a reference PA, that is fed with the same signal and operates for a fixed reference load. It was claimed that this architecture performs better for measurements using non-constant envelope signals. However, the circuit is very complex and it requires one extra amplifier, operating for a dummy fixed load.

2.3.2 Sampled Line Based

Some other measurement systems that have been developed a long time ago, as, for example, slotted lines, are bulky and composed of many mechanical moving parts. The biggest disadvantage of these older measurement systems is that some of the parts must be fabricated with very precise machining processes, which are expensive. Moreover, the measurement is mostly done manually, which is time consuming. The measurement is based on the voltage standing wave, which is obtained by measuring the voltage on several positions along a $\lambda/2$ line. Then, the standing wave information (amplitude, average value and minimum position) is used to compute the output load. Some other approaches, as sampled lines [50], are based on the same principle, but, instead of using moving components along a line, the voltage is sampled by various fixed power detectors placed on a $\lambda/2$ line, as shown in Fig. 2.16. However, since various detectors are required, the introduced IL is, normally, too high for the required high efficiency applications [50].

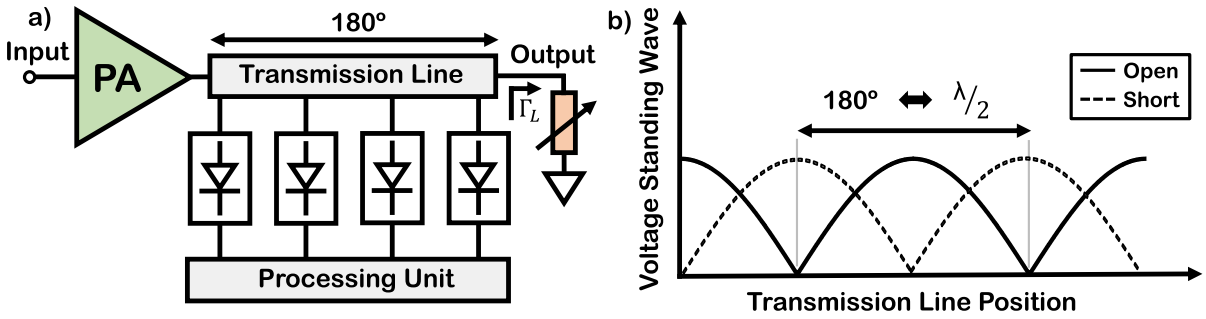

Figure 2.16: a) Sampled line typical topology. b) Normalized voltage standing wave pattern for a short circuit termination (dashed) and open circuit termination (continuous).

Six-port reflectometers can also be implemented with similar sampling architectures. Using specific algorithms, it is possible to compute the reflection coefficient from, at least, four sampling ports. This measurement technique can be implemented with various power detectors placed along a line, as sampled lines, and also from voltage samples obtained directly at different locations of the PA OMN [51], [52]. However, the OMN IL is usually increased too much due to the added power detectors, and, in some cases, the measurement accuracy is worse than it is on coupler based solutions. Moreover, the measurement circuit needs to be closely designed with the amplifier OMN, increasing the OMN complexity and adding extra constrains to its design.

Chapter 3

Objective and Main Goals

From the presented state-of-the-art we conclude that both the academia and industry already developed various PA architectures and other techniques, such as TMNs, that can be used to reduce the amplifier's performance degradation for operation under non-optimal loads. However, none of the developed PA architectures is insensitive in terms of both output power and efficiency, for real and also complex output loads. TOMNs can be used to further increase load insensitiveness of amplifiers, by increasing the isolation provided by the OMN, but variable components introduce considerable losses on the matching networks, reducing the total amplifier's efficiency.

Based on this state-of-the-art analysis and on the motivation behind the work, we present the main objective of this doctoral program. The aim is to study and develop a load insensitive PA topology, or novel methods to turn the existing architectures more insensitive to output load variations. To achieve this overall objective the following specific goals are defined:

- The PA performance degradation, for operation under non-optimal loads, should be studied and quantified, for existing PA architectures. The key figures of merit to evaluate this performance degradation are the energy conversion efficiency and the output power capability, which are of paramount importance in all PA applications. Moreover, the linearity should also be considered, which is a decisive factor for telecommunication applications;

- Tunable matching networks (TMNs) will also be studied and evaluated in terms of losses and matching range. Their possible implementation in the OMN of PAs will be considered, in order to further reduce the load variation seen by the used transistors.

- Based on the identified problems for each PA architecture, or class of operation, novel techniques should be developed to reduce the output load sensitivity of amplifiers. These techniques should be included in the design of a single-ended PA and validated with simulations and laboratory measurements.

- The developed techniques should be extended for more complex PA architectures with high efficiency at BO, such as Doherty or Outphasing amplifiers, so that, they can be implemented in telecommunication applications, where high PAPR signals are used.

- The final aim is to design a complete PA system that should be insensitive to unpredictable output load variations. Ideally, this system should not depend on any external

hardware, being able to keep its performance by itself. From the user perspective, it should behave as if it were always operating for the nominal load, providing a seamless performance. Since it should work for predictable and unpredictable load variations, an impedance measurement solution must also be designed to track the load and provide the amplifier stage with the necessary feedback.

Chapter 4

Load Insensitive Power Amplifier Solutions

This chapter presents the work developed during this PhD thesis, highlighting the main innovations. As previously said, the main objective of this PhD work is to develop a novel load insensitive PA architecture. This was accomplished by carrying out various steps towards the established final objective. In the beginning, we have started by studying the existing solutions, and the actual PA performance degradation for various classes of operation, which was crucial to implement our first prototype, based on TMNs. Then, we realized that it was very important to develop a low-loss impedance measurement system, and so, we came up with an innovative solution based on a MCU, which was adequate for implementation with various load compensation techniques due to the possibility of generating a diverse range of load-dependent control outputs. Lastly, we have developed a novel technique, based on the PA V_{DS} variation, to compensate the degradation caused by the studied PA non-optimal loading. Finally, a complete QLI DPA system was developed, including:

- real-time tracking of the DPA output stage load;
- compensation of the efficiency and output power degradation by controlling the transistors' V_{DS};
- an adaptive input stage to adjust the input RF signals, keeping the Doherty behavior and increasing the linearity under non-optimal loads;
- a common mode gain adaptation to keep the small signal gain constant under output load variations.

This chapter is organized as follows. In Section 4.1, we evaluate the advantages and disadvantages of a quasi load insensitive PA architecture combined with a low loss TMN based on adjustable length stubs. In Section 4.2, we introduce a dedicated compact and low-loss impedance measurement circuit that can track the amplifier's output impedance in real-time. Section 4.3.1 presents a novel technique to increase PAs performance under non-optimal loading based on the optimal transistors' V_{DS} variation, which was derived for single-ended class B amplifiers. Finally, Section 4.3.2 presents the extended application of te derived transistors' V_{DS} variation to DPAs, and also the complete QLI DPA system.

4.1 Tunable Matching Network

After analyzing the existing literature on load insensitive PA architectures and TMNs, we had the idea of combining a PA architecture that is already robust to load variations with a TMN, to increase the PA load insensitiveness. So, in this first part of the work, we studied different classes of operation and we have opted for a QLI class E PA due to its high efficiency under real loads. Then, the idea was to use a simpler TMN, which was required to transform any load inside the considered VSWR circle into real loads. This way, the complexity of this network is lower, since it is only used to remove the imaginary part of the output loads, and, consequently, it can be designed with less losses.

The designed network, which we named "reactance compression network (RCN)", is built by adding a variable parallel element to the complex output load. The necessary parallel reactance was calculated (Appendix A) for each load inside the worst-case considered VSWR circle and is shown in Fig. 4.1 a). The worst-case load variation considered for compensation was a 2.1 VSWR circle, which is a good estimate of the actual load variation obtained in state-of-the-art 5G massive MIMO antenna arrays [53], which is one of the most important applications for the developed work.

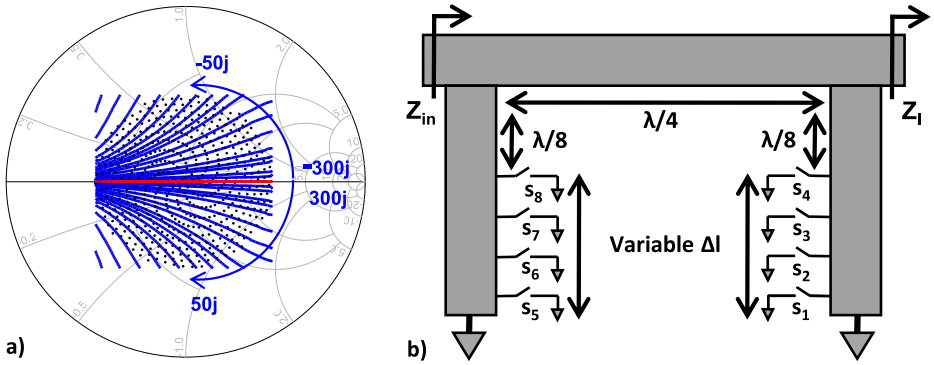

Figure 4.1: a) Contours of the calculated necessary parallel reactance to eliminate the imaginary part of each load. b) Schematic diagram of the idealized compensation network.

The necessary reactance values could be generated with only one variable length short-circuited stub, which can be implemented with various shunt switches along a shunt stub. However, since many different reactance values are needed, we would need a large number of switches, some of them placed very far from the stub end, which would then operate in high impedance regions, thus experiencing a high voltage swing. This would increase their parallel losses (since the available switches have a finite OFF resistance). In order to solve this problem, we have decided to design shorter stubs that can generate only inductive terminations, and use two of them separated by a 90^{o} transmission line. The idealized network is shown in Fig. 4.1 b), where the first stub (closer to Z_l) compensates the capacitive part of the output loads, and the other one compensates inductive loads. In order to fabricate the network, a careful switch characterization process was performed, which is completely described in Appendix A. The fabricated network is shown in Fig. 4.2 a) and the achieved measured performance is depicted in Fig. 4.2 b), where the original loads presented to the network are shown by blue squares, and the correspondent loads that are presented by the network to the PA are shown by black circles.

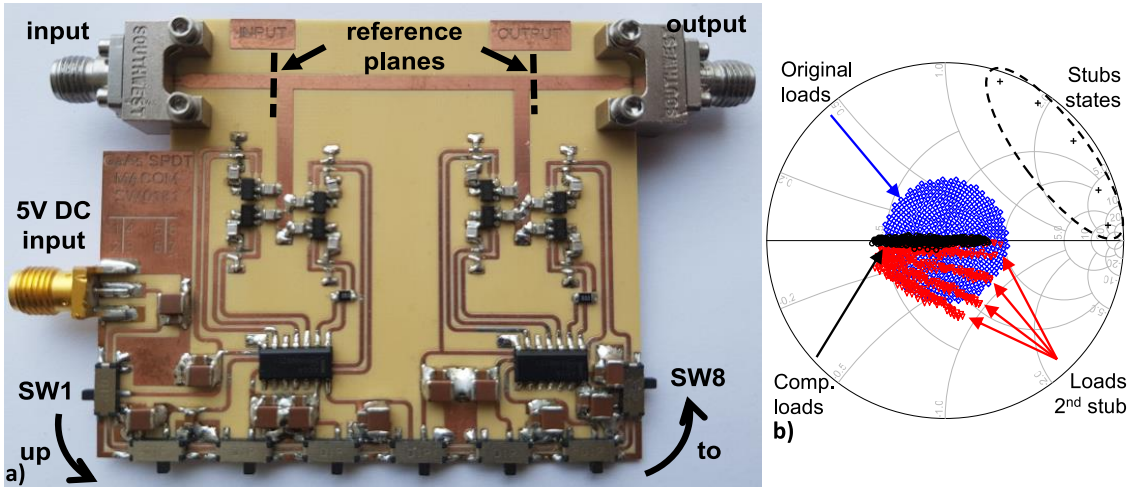

Figure 4.2: a) Photography of the fabricated RCN. b) Original output loads, in blue, and compensated loads, in black.

Then, we realized that the obtained real load variation could be rotated into other linear variations in the Smith chart, by adding specific delay lines between the network and the PA, thus extending the use of the RCN to other different purposes. As explained in the following paragraphs, the RCN was used, in simulation, at the output of two PAs.

PA 1 was designed for the maximum efficiency load, and the RCN was used to compress the output load variation into loads distributed along a constant output power contour, this way compensating the output power degradation.

PA 2 was designed for the maximum output power load, and the compensation network was used to compress the output load variation into loads distributed along a constant efficiency contour, compensating the original efficiency degradation. The obtained performance is shown in Table 4.1.

	Lowest Eff.	**Eff. Variation**	**Lowest Output Power**	**Output Power Variation**
PA 1	75%	13%	36.7dBm	**5.3dB**
Comp. PA 1	70%	12%	38.4dBm	**1dB**
PA 2	**35%**	48%	39.6dBm	3.2dB
Comp. PA 2	**57%**	12%	41.2dBm	1.2dB

Table 4.1: Simulated improvement results for PA 1 and PA 2, with and without the compensation network.

To validate the designed network with laboratory measurements, PA 1 was fabricated, and it is completely characterized in Appendix A. Here we show its synthesized performance. In Fig. 4.3 a) we show the amplifier output power variation without compensation, in blue diamonds, and using the fabricated RCN for load compensation, in black circles. In Fig. 4.3 b) we use the same symbols and color scheme to show the amplifier efficiency with and without load compensation.

These measurements validate the build prototype, showing a worst-case output power improvement of 1.6 dB, from 36.2 dBm to 37.8 dBm, and an output power variation of only 1.4 dB, for loads varying inside a 2.1 VSWR circle. The drawback of this technique is the added IL, which, although relatively low (average of 0.42 dB, for the tested loads), still causes a considerable impact on the overall PA efficiency.

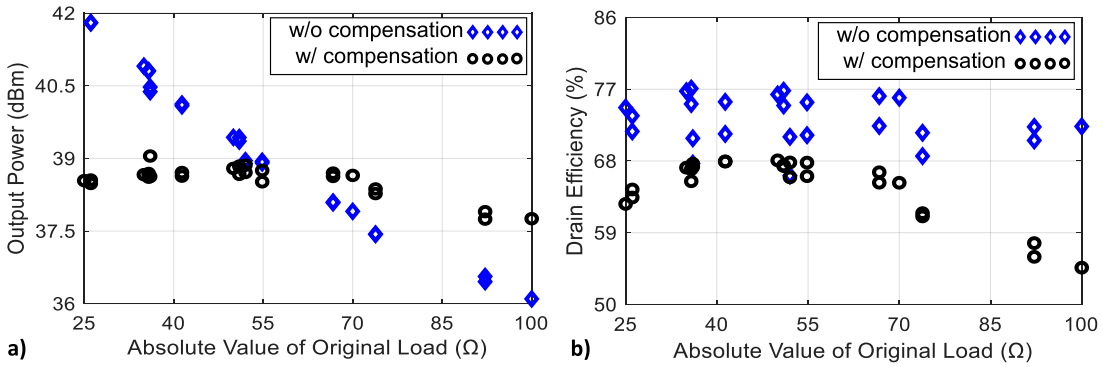

Figure 4.3: a) Measured output power of PA 1, with and without the compensation network. b) Measured DE of PA 1, with and without the compensation network.

4.2 Impedance Tracking

After the first part of the work, we focused our research on developing an impedance measurement system for PAs. The objective is to track the output load in real-time and control TMNs, like the one developed before, or any other adaptive circuits that aim at improving PA performance under load variations. We have opted for a MCU based measurement system due to its affordable cost and ability to easily generate different control signals for usage with distinct adaptive circuits.

The designed system is based on the stationary wave measurement, as slotted lines and sampled lines. However, slotted lines are made with bulky mechanical moving parts, which need to be fabricated with very precise machining processes. Sampled lines are based on a high number of power detectors, and so, they introduce a high IL. Our approach is to use weakly coupled samples of the incident and reflected waves, through a low loss bi-directional coupler, to synthesize a stationary wave replica. We use the circuit of Fig. 4.4 to sample both the incident and reflected waves at one fixed spatial position, and then, using a phase shifter, we mimic the distance-dependent phase shift that occurs between them in a physical line. Note that the phase shifter is a critical component because it will mimic the phase delay that naturally occurs on a physical microstrip line. Moreover, to synthesize a complete period of the stationary wave, it needs to be swept between 0^{o} and 360^{o}. This way, we mimic the phase delay that would occur in a 180^{o} ($\lambda/2$) line, because, in a transmission line, the waves travel in opposite directions. The complete description of the fabricated circuit can be found in Appendix B.

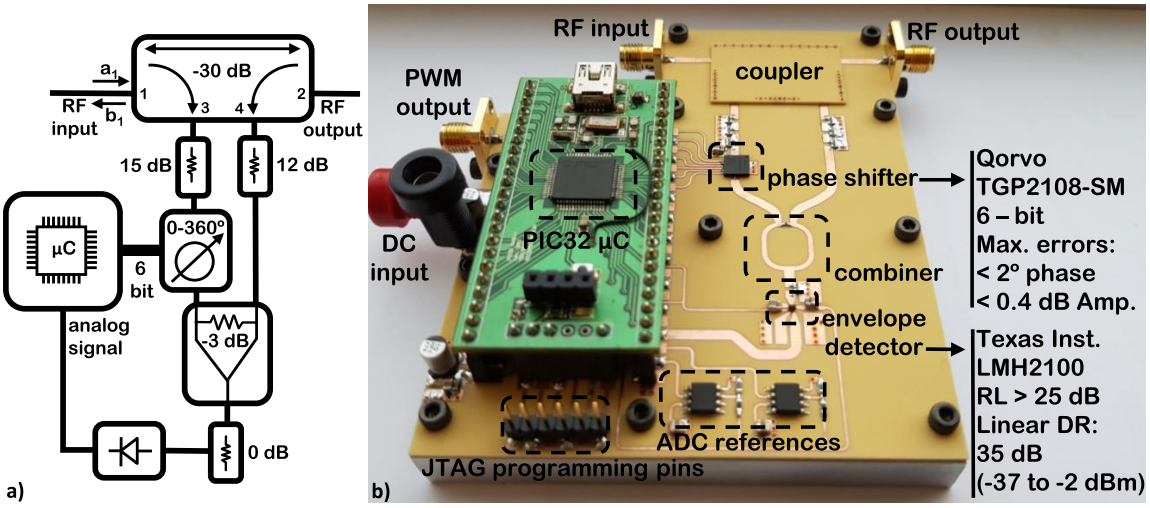

Figure 4.4: a) Impedance measurement circuit schematic. b) Fabricated impedance measurement circuit and brief description of its main components.

By using this circuit, we are able to measure the stationary wave at one fixed spatial point, which introduces less losses and lower complexity. However, in order to synthesize one complete period of the stationary wave, we need to acquire various voltage samples for different phases selected at the phase shifter. Summarizing, we are measuring the stationary wave using serial sampling instead of using parallel sampling (as in sampled lines), which increases the measurement time. In order to compensate for this effect, we first noticed that although the

standing wave is a complicated function of its variables, its square is simply a pure cosine of the phase difference between the incident and reflected waves, plus an offset. So, profiting from this observation we developed a Fourier-based impedance calculation algorithm that is able to compute the output load from very low phase resolution incident wave measurements. This way, we need to acquire a lower number of samples, making the measurement much faster. The algorithm is shown in (4.1), where V_{SW0} and V_{SW1} are the zero-order and fundamental terms of the Fourier transform, respectively. The complete derivation of the algorithm can be found in Appendix B.

$$\Gamma_U = \left(\frac{V_{SW0}(|a_{1U}|, |\Gamma_U|)}{2|V_{SW1}(|a_{1U}|, |\Gamma_U|, \theta)|} \pm \sqrt{\left(\frac{V_{SW0}(|a_{1U}|, |\Gamma_U|)}{2|V_{SW1}(|a_{1U}|, |\Gamma_U|, \theta)|} \right)^2 - 1} \right) e^{-j\angle V_{SW1}(|a_{1U}|, |\Gamma_U|, \theta)} \tag{4.1}$$

In Fig. 4.5 we show the practical validation of the fabricated impedance measurement circuit used at the output of a PA capable of delivering up to 43 dBm, and for various loads, synthesized using a stub based manual load tuner. In Fig. 4.5 a) we show the measured loads versus the synthesized ones, which were measured with a calibrated VNA. This validation was performed for various power levels, from 27 dBm up to 43 dBm, and using a phase resolution of 11.2º for the stationary wave measurement, which means that 32 serial samples are necessary to acquire one replica of the stationary wave, and 6 ms are required to measure the output load.

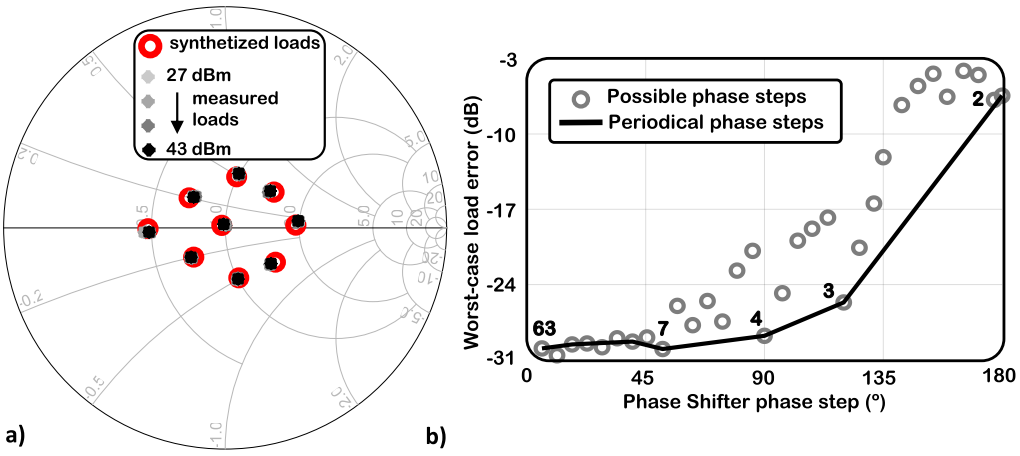

Figure 4.5: a) Synthesized (red circles) and measured loads (gray scale dots) for various PA output power levels, using a 11.2º phase shifter step. b) Worst-case measurement error for all the possible phase shifter steps. In black we show the available periodical phase steps and the correspondent number of measured samples.

In Fig. 4.5 b) we show the load measurement worst-case error (over the load and output power ranges) for various phase shifter steps. For a phase step correspondent to seven or more samples, the error is around -30 dB, which is enough for the required application, as seen in Fig. 4.5 a). If it is necessary to reduce the measurement time, we can increase the phase step. However, note that, for higher phase steps, it is important to keep them equal to sub-multiples of 360º, so that the measurements are periodical. If this condition is

satisfied, we can estimate the load with an acceptable error because the developed Fourier-based model is a good approximation of the stationary wave. Note that, using a phase step of 90^{o} (correspondent to 4 sampled points), the error is -28.8 dB, and the measurement time is already reduced to below 1 ms. For a 120^{o} phase step (correspondent to 3 sampled points), the error is -25.7 dB, and the measurement time is only 800 μs.

4.3 Supply Voltage Modulation

This section is devoted to the supply voltage modulation technique, which was developed to increase PA performance for operation under load varying scenarios. The approach is to change the supply voltage of the amplifier to increase its output power or its efficiency for operation under non-optimal loads, for which the performance was degraded. The simplified schematic for implementation of this technique is shown in Fig. 4.6, where the PA is composed by a static OMN and a variable dc supply.

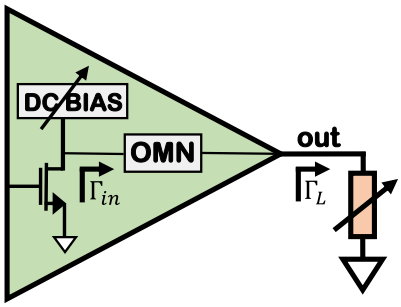

Figure 4.6: Schematic of a RF PA with an adaptive drain supply voltage.

This section is divided in two sub-sections. The first one is dedicated to the technique itself, providing a generic explanation, and to its application on a single-ended PA prototype. In the second sub-section, the introduced technique is further expanded for application in DPAs. We present the results obtained for this new scenario, a qualitative explanation, and its application on a fabricated QLI DPA prototype. Then, we also present a complete QLI PA system, which is based on a DPA output stage, on the impedance measurement circuit presented on Section 4.2, and on a pre-amplifier and adaptive input driving stage.

4.3.1 Single-Ended PA

In this subsection we will briefly describe the developed V_{DD} modulation technique. The main objective is to restore the output power capability, i.e., the maximum output power that can be delivered by an amplifier, when operating with non-optimal output loads.

The V_{DD} derivation is based on an ideal class B PA, as shown in Fig. 4.7 a), where the transistor is approximated by a piece-wise linear current source with R_{ON}. First, it is necessary to calculate the output power for a specified supply voltage, V_{DD}, and fundamental load termination, Z_L. Then, this output power expression is set equal to the constant output power value that is obtained for the nominal supply voltage, V_{DD_0}, and nominal fundamental design load, $R_{L_{eff}}$. Finally, this expression can be solved for V_{DD}, obtaining the required load-dependent supply voltage values that must be applied to the PA so that its output power is kept constant for operation with different loads, Z_L. The complete derivation can be found on Appendix C and Appendix D, and the final result is the expression (4.2). In Fig. 4.7 b), we show the derived V_{DD} values plotted on the Smith chart, for various loads distributed inside a maximum VSWR circle of 2.0.

$$V_{DD}(Z_L) = \sqrt{\frac{R_{L_{eff}}}{\text{real}(Z_L)}}\,\frac{V_{DD_0}(|Z_L| + 2R_{ON})}{(R_{L_{eff}} + 2R_{ON})} \tag{4.2}$$

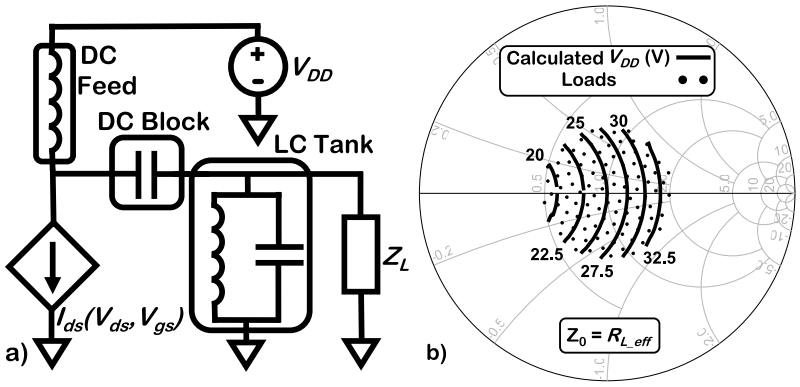

Figure 4.7: a) Simplified PA output circuit considered during the theoretical analysis. b) Calculated V_{DD} values for the used Wolfspeed device and for a nominal V_{DD_0} of 25 V.

Now, to qualitatively understand how the compensation is performed, consider that the amplifier suffers a load variation towards (i) a higher real load, $R_L > R_{L_{eff}}$ or (ii) a lower real load, $R_L < R_{L_{eff}}$. For higher loads, (i), the fundamental current will be lower, as shown in Fig. 4.8 (a). And so, in this situation, the V_{DD} should be increased to raise the voltage excursion and restore the output power capability of the amplifier. For lower loads, (ii), the maximum current becomes higher, which increases the output power capability of the amplifier. However, for the designed output power, the efficiency becomes lower because the PA is operating in BO, as shown by the non-optimal load line in Fig. 4.8 (b). So, in this case, the V_{DD} should be reduced to increase the efficiency for the designed output power level. For complex loads, the same principle can be applied to improve the output power and/or efficiency of the PA. Naturally, for operation with complex loads, it is not possible to completely restore the nominal DE, since this technique does not eliminate the load line hysteresis caused by complex loads.

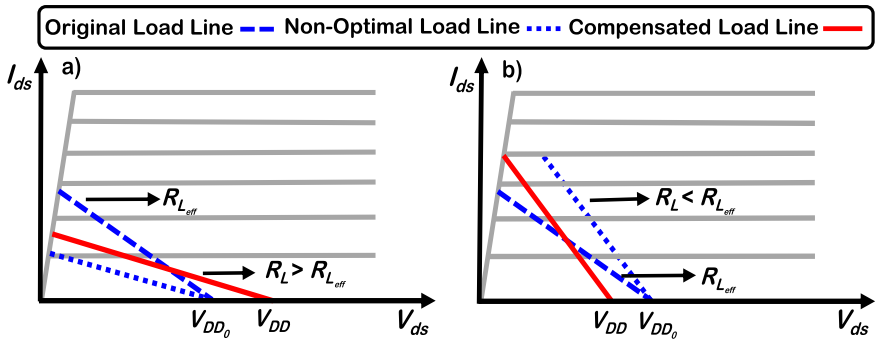

Figure 4.8: Load line explanation of the compensation method for higher real loads, in a), and for lower real loads, in b).

Note that this technique is not effective when the device saturates in current, because we cannot increase the output power by increasing the supply voltage. So, for lower loads, this technique can only be used up to the point where the device clips in current. Therefore, the PA cannot be designed for the typical maximum power load of the used transistor; otherwise it would become current saturated for a slightly output load reduction. So, in Appendix D, the implemented PA prototype is designed for the maximum efficiency load, enabling higher

efficiency and compensation for loads lower than the nominal one.

To validate the developed theory, we have fabricated a class B PA prototype, which is shown in Fig. 4.9 a). This prototype is based on a class B PA with a dc-to-dc converter that allows to change the amplifier supply voltage, depending on the duty-cycle (DC) of an input pulse-width modulation (PWM) signal. This control input is generated by a MCU and it depends on the real-time output load of the prototype PA. The used MCU also senses the output load of the amplifier, by running the load computation algorithm and controlling the impedance measurement circuit described in Section 4.2.

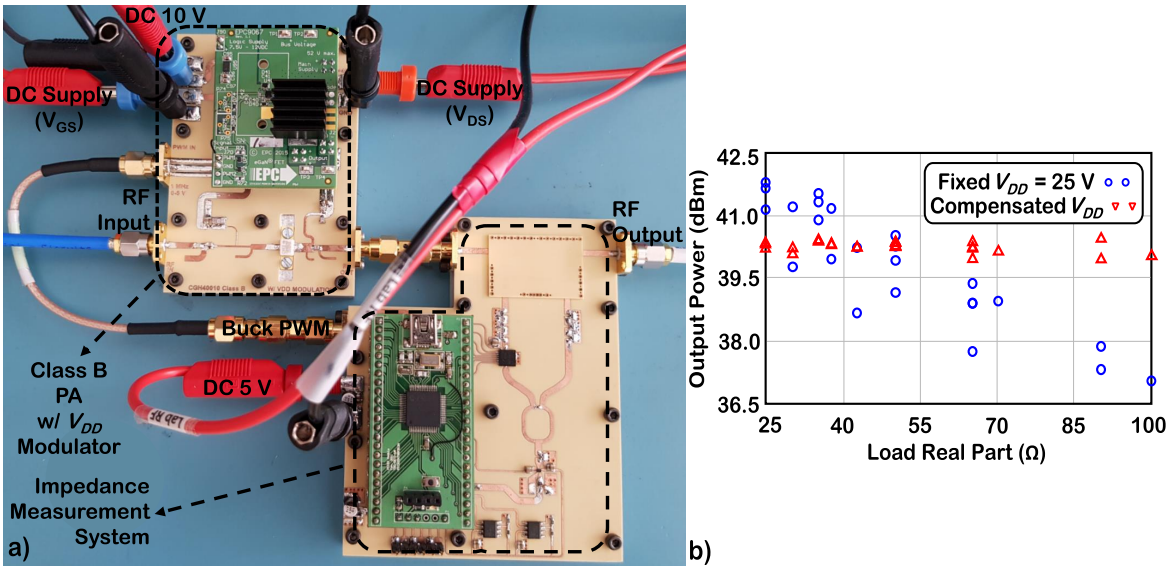

Figure 4.9: a) Photography of the final prototype, which includes the V_{DD} modulated class B PA prototype and the impedance meter of Section 4.2. b) Measured output power of the implemented PA prototype for a fixed V_{DD} of 25 V, and for the optimal derived values.

Since the main objective of the derived theory is to maintain the output power of an amplifier for non-optimal loading, in Fig. 4.9 b), we show the measured output power of the implemented prototype, at the 1-dB gain compression point, for various loads distributed within a maximum VSWR circle of 2.0. It is shown that, using the derived V_{DD} values, the gain variation is 0.5 dB and its minimum value is 39.9 dBm, which corresponds to a reduction of 4.2 dB in the variation and a worst case output power improvement of 2.9 dB. The detailed results are presented in Appendix D, where we also show the system behavior for a continuous load variation, where we explain the time limitations of the system, and the performance for operation under modulated signal excitations.

4.3.2 Doherty PA

This sub-section briefly describes the derivation and test of a V_{DD} modulation technique for application on DPAs. The complete technical explanation and mathematical derivation can be found in Appendix E. Then, its application on a system that is composed by a DPA output stage, an impedance measurement circuit and also an adaptive input splitting stage can be found in Appendix F. In Appendix F, we also show the optimal load-dependent input splitting ratio.

The expressions that are presented here were obtained from derivations that assumed an ideal two-way symmetrical Doherty, as shown in Fig. 4.10 a). Moreover, we assumed independent V_{DD} sources for the carrier and peaking devices, and also that both devices operate in class B. Summarizing, to maintain the DPA behavior for non-optimal loads, it is necessary to guarantee that both the BO and FP output power levels are kept constant. This condition can be accomplished by ensuring that the maximum output power of the carrier for the BO load is constant, and also that the maximum combined output power of both the carrier and peaking PAs, when operating for their FP loads, is kept constant and equal to 4 times the BO output power (for a 6 dB BO design).

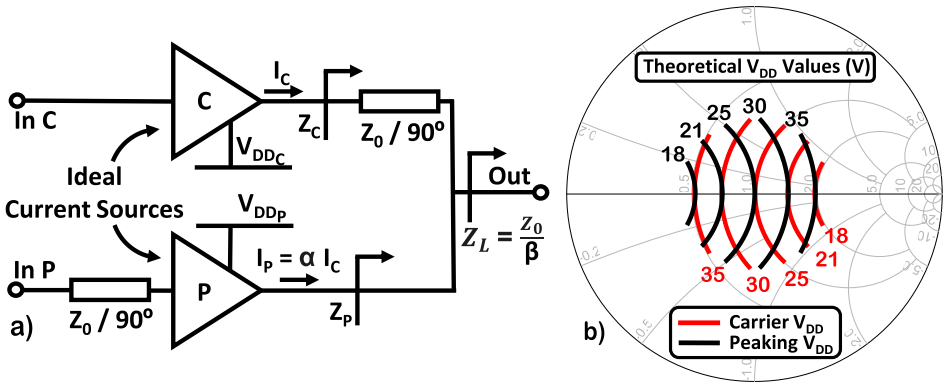

Figure 4.10: a) Ideal two-way symmetrical DPA schematic considered during the theoretical analysis. b) Theoretical V_{DD} values for the carrier and peaking devices, for a nominal V_{DD_0} of 25 V. Note that the Smith chart reference Z_0 is the nominal design load of the DPA.

At BO, since the peaking PA is off, the DPA operation is determined by the carrier PA, and so, the derivation of its optimal supply voltage is very similar to what we have done for a single-ended amplifier in Section 4.3.1. The final expression is shown in (4.3), where $\beta = \frac{Z_0}{Z_L}$, for an output load, Z_L, and for a design load (nominal FP load of the devices), Z_0. For the nominal output load, $Z_L = \frac{Z_0}{2}$, $\beta = \beta_0 = 2$, and $V_{DD_C} = V_{DD_0} = 25\,V$.

$$V_{DD_C}(\beta) = \frac{|\beta|}{\sqrt{\beta_0 \mathrm{Re}(\beta)}} V_{DD_0} \tag{4.3}$$

Then, by ensuring that the combined FP of both devices is also preserved, and that they maintain a full voltage excursion (saturation at the triode region), we can derive the V_{DD} for the peaking device. The obtained expression is shown in (4.4), and the optimal load dependent voltages for the carrier and peaking devices are also plotted in the Smith chart of Fig. 4.10 b).

$$V_{DD_P}(\beta) = \frac{2}{\sqrt{\beta_0 \mathrm{Re}(\beta)}} V_{DD_0} \tag{4.4}$$

In the previous section, we have explained that, to correctly compensate the PA performance using V_{DD} modulation, the PA cannot be designed to the typical maximum power load of the used devices, R_{opt}. Now, in this work, we also show that the optimal design load for a pre-specified compensation area is $\sqrt{x}R_{opt}$, with x being the maximum VSWR considered for correction. Moreover, since the gain of each amplifier also changes with the output load and

V_{DD}, to keep the Doherty behavior, it is also necessary to change the input driving signal of each amplifier. In Appendix F we also calculate and present these load-dependent input signals.

In Fig. 4.11 a) we show the simulated efficiency performance of a typical DPA, designed to the regular FP load, R_{opt}, and without any compensation technique. In Fig. 4.11 b) we show the simulated performance of the proposed QLI DPA, which was designed to the derived FP load, $\sqrt{2}R_{opt}$ (in order to allow compensation on a maximum VSWR circle of 2.0), and with the proposed V_{DD} compensation technique. For the nominal load, the typical amplifier has an output power level of 43.1 dBm and the expected conventional Doherty efficiency shape. But, for operation with lower loads, the output power level is degraded and the efficiency is reduced, both at FP and BO. For higher loads, the efficiency is extremely degraded at BO and the output power capability also reduced. For this last case, the obtained efficiency shape changes so drastically that it becomes similar to what is obtained for a single-ended PA. The proposed QLI DPA delivers a lower output power of 42.3 dBm for operation under the nominal load, because it is designed for a higher FP load, but it is able to maintain the output power capability and its efficiency profile for operation under non-optimal loads.

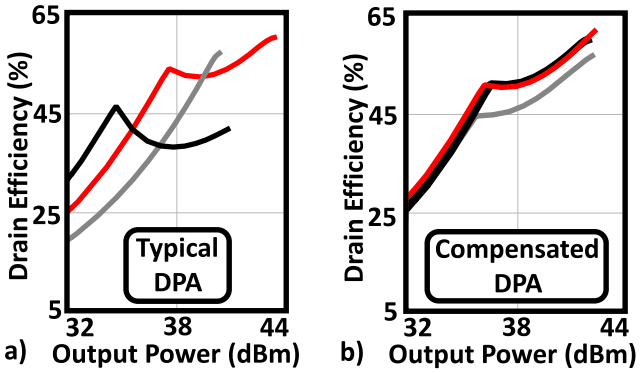

Figure 4.11: a) DE profile of a typical DPA operating for the nominal load (red), half the nominal load (black), and twice the nominal load (gray). b) DE profile of the proposed QLI DPA for the same loads.

Then, to validate the proposed technique with laboratory measurements, we have designed and fabricated a complete PA system for 3.6 GHz, which is shown in Fig. 4.12. It is composed by the QLI DPA output stage, by a medium power 2-channel driver that also acts as an isolation stage, by an adaptive input splitting pre-driver stage, which enables the use of real-time variable splitting ratios, and by the impedance measurement circuit that was presented in Section 4.2. A more detailed description of this system is found on Appendix F.

This prototype was characterized under CW and modulated signal excitations, and for static and dynamic (real-time adaptation) operation. All the acquired measurements are shown on Appendix F, while here we only show its LP characterization, in Fig. 4.13.

Note that these LP contours are plotted for the 1-dB gain compression point. In red we show the proposed QLI DPA performance, while in black we show the performance of the same prototype, but without applying the developed V_{DD} modulation technique. In Table 4.2, we show the summarized measured performance of the developed prototype. By analyzing the provided data, it can be concluded that the output power capability of the amplifier is improved up to 1.3 dB when applying V_{DD} modulation. The worst-case efficiency is kept

almost the same with and without compensation, but, note that for most loads, the efficiency is also greatly improved. As an example, for higher real loads, the BO efficiency is improved by almost 20 % (from 30 % to 50 %).

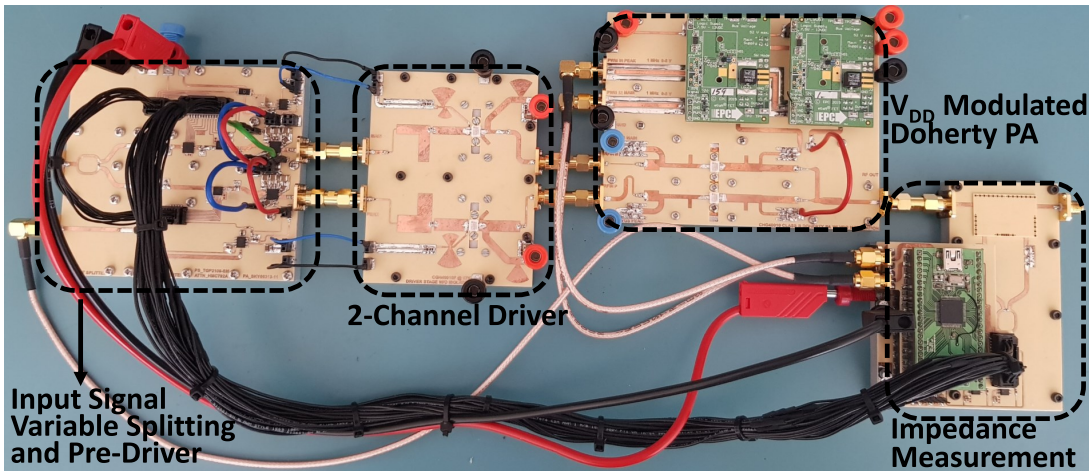

Figure 4.12: Photograph of the fabricated system, including V_{DD} modulation, impedance tracking and input splitting control.

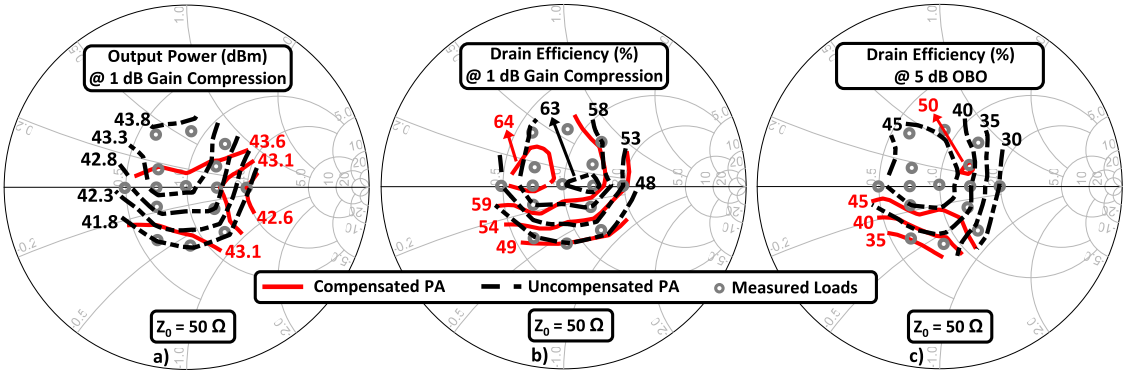

Figure 4.13: LP of the fabricated prototype with and without V_{DD} compensation. The output power and DE at FP are presented in a) and b), respectively, and the BO DE in c).

Table 4.2: Summarized performance improvement of the proposed QLI DPA.

	Worst-case P_out (dBm)	**P_out Degradation (dB)**	**Wors-case BO eff. (%)**	**Worst-case FP eff. (%)**
Uncompensated DPA	41.8	2	30	48
QLI DPA	**42.6**	**1**	35	49

Chapter 5

Main Contributions and Innovations

The work developed during this PhD program produced several publications in various international conferences and journals. The main scientific contributions will be presented next.

A Class E amplifier was integrated with a TMN based on switched variable length stubs, and since the amplifier already maintains high efficiency for a broad range of loads, the designed TMN was only required to compress complex load variations into loads within a constant output power contour. This way, it was possible to achieve lower losses due to the reduced number of variable components used. This work culminated in the following contributions:

- **C. F. Gonçalves**, F. M. Barradas, P. M. Cabral and J. C. Pedro, "Switch-Based Variable Length Stubs Network for PA Load Sensitivity Reduction," in IEEE Access, vol. 7, pp. 152576-152584, 2019. DOI: 10.1109/ACCESS.2019.2948277.

  (attached to this thesis in Appendix A)

After, we developed an impedance measurement solution for high power amplifiers, required to generate load-dependent control inputs for the developed TMN or any other adaptive technique that requires load-dependent inputs. The designed measurement solution is capable of measuring the load from voltage standing waves, using a novel algorithm. However, instead of using mechanical components or several power detectors, only one bi-directional coupler and one power detector are used, at a fixed location. This allows to perform fast and accurate measurements without introducing too much losses at the PA output, and using simple and affordable hardware. The circuit design and algorithm are completely described in:

- **C. F. Gonçalves**, F. M. Barradas, L. C. Nunes, P. M. Cabral and J. C. Pedro, "A Compact Impedance Measurement Solution for Systems Operating in Load Varying Scenarios," in IEEE Access, vol. 9, pp. 38757-38766, 2021. DOI: 10.1109/ACCESS.2021.3063915.

  (attached to this thesis in Appendix B)

After that, a novel method to improve amplifiers performance under output load variations was developed. The method is based on the dynamic variation of the amplifier V_{DS}, and is

comprehensively described using load line theory. Summarizing, the supply voltage can be modified in order to restore the nominal output power for operation under higher loads, and also to keep the output power constant and restore the drain efficiency, for operation under lower loads. For the V_{DS} variation, we have used a commercial available PWM controlled gallium nitride (GaN) buck converter. This work resulted in the following contribution:

- **C. F. Gonçalves**, F. M. Barradas, L. C. Nunes, P. M. Cabral and J. C. Pedro, "Dynamic Supply Voltage Control for PA Output Power Correction Under Variable Loading Scenarios," in IEEE Transactions on Microwave Theory and Techniques, vol. 69, no. 1, pp. 745-755, Jan. 2021. DOI: 10.1109/TMTT.2020.3037963.

  (attached to this thesis in Appendix C)

- **C. F. Gonçalves**, F. M. Barradas, L. C. Nunes, P. M. Cabral and J. C. Pedro, "Optimal Supply Voltage for PA Output Power Correction under Load Varying Scenarios," 2020 IEEE MTT-S International Microwave Symposium (IMS), Los Angeles, CA, 2020. DOI: 10.1109/IMS30576.2020.9223898.

  (attached to this thesis in Appendix D)

Finally, to fulfill the final objective of this work, the previous supply voltage variation theory was expanded for usage in DPAs, and thus possible application on telecommunications. For Doherty amplifiers, two distinct voltages are required, one for the carrier and one for the peaking, since they experience opposite load variations due to the carrier impedance inverter. The optimal voltages were calculated from BO and FP conditions, for the carrier and peaking devices, respectively. This theory was validated on a fabricated DPA. Then, a QLI PA system was designed and assembled, including the previously developed DPA output stage and a specifically designed adaptive input stage that allows to generate load-dependent driving signals. The impedance measurement system designed on task 2 is used to track the load in real-time and generate the load-dependent driving signals and supply voltages. The designed QLI prototype and derived theory resulted in the following contributions:

- **C. F. Gonçalves**, F. M. Barradas, L. C. Nunes, P. M. Cabral and J. C. Pedro, "Load Insensitive Doherty PA Using Supply Voltage and Input Excitation Adaptation," in IEEE Transactions on Microwave Theory and Techniques, vol. 69, no. 1, pp. 745-755, Jan. 2022. DOI: XX. (accepted)

  (attached to this thesis in Appendix E)

- **C. F. Gonçalves**, F. M. Barradas, L. C. Nunes, P. M. Cabral and J. C. Pedro, "Load Insensitive Doherty PA Using Load Dependent Supply Voltages," 2021 IEEE MTT-S International Microwave Symposium (IMS), Atlanta, GA, 2021. DOI: XX. (presented)

  (attached to this thesis in Appendix F)

Moreover, during this PhD program, it was also required to characterize transistors, variable components for TOMNs, and other active or passive devices used in the developed prototypes. Therefore, some contributions have been made also on measurements and modeling:

- J. L. Gomes, L. C. Nunes, **C. F. Gonçalves** and J. C. Pedro, "An Accurate Characterization of Capture Time Constants in GaN HEMTs," in IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 7, pp. 2465-2474, July 2019. DOI: 10.1109/TMTT.2019.2921338.

- **Gonçalves, CF**, Nunes, LC, Cabral, PM, Pedro, JC. "Pulsed I/V and S-parameters measurement system for isodynamic characterization of power GaN HEMT transistors." Int J RF Microw Comput Aided Eng. 2018. DOI: 10.1002/mmce.21515.

- J. L. Gomes, L. C. Nunes, **C. F. Gonçalves** and J. C. Pedro, "Deep-Level Traps' Capture Time Constant and its Impact on Nonlinear GaN HEMT Modeling," 2018 International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMIC), Brive La Gaillarde, 2018, pp. 1-3. DOI: 10.1109/INMMIC.2018.8429992.

- **C. F. Gonçalves**, L. C. Nunes, P. M. Cabral and J. C. Pedro, "Conservative current and charge data extracted from pulsed S-parameter measurements for GaN HEMT PA design," 2017 IEEE MTT-S International Microwave Symposium (IMS), Honololu, HI, 2017, pp. 1065-1068. DOI: 10.1109/MWSYM.2017.8058778.

Lastly, although uncorrelated with the presented PhD thesis topic, I have participated in the European Microwave Week competition on enhancing the video bandwidth of PAs with some of my PhD colleagues of the RF circuits and systems group of IT-Aveiro. The design was based on a DPA with state-of-the-art biasing techniques and we received the 1st prize.

- D. R. Barros, **C. F. Gonçalves**, J. L. S. Pereira, 1st Prize at EuMW Student Design Competition, by Ampleon - Video Bandwidth Enhancement for High Power Amplifiers, September 2018.

  (Link: https://www.ampleon.com/news/events/student-design-competition-2019.html)

Chapter 6

Conclusions

This thesis reports the work that have been developed during this PhD program on load insensitive PA architectures and techniques. We have addressed the performance degradation of PAs operating under load varying scenarios, which arise on a broad range of applications, and causes an output power, DE, and linearity reduction. Therefore, increasing the amplifiers load insensitivity is of paramount importance for both the scientific community and industry. This performance degradation is caused by the non-optimal loading of the used transistors. Thus, we developed various prototypes that aim at improving the performance by reducing the load variation seen by the transistors, and by applying novel compensation techniques, as described in the following paragraphs.

The first two goals of this work stated that we should study various PA and TMN architectures, analyzing the possible use of TMNs to increase PA performance under load varying scenarios. So, we started by studying various PA architectures, and we identified the class E as a great candidate for load insensitiveness in terms of DE, and the balanced amplifier as a good option from an output power perspective. Then, we evaluated various TMN architectures, and we came up with a new one based on switched variable length short-circuited stubs. Moreover, we included it in the design of a PA to reduce its load sensitivity. This work has demonstrated that, if we choose a PA architecture that is already more insensitive to load variations, we are able to relax the TMN requirements, and thus, the TMN losses can be reduced and it can be a viable option to improve the PA overall performance. With this work we have accomplished the first two goals of this PhD program.

Then, we presented a novel technique to improve amplifiers' load insensitiveness, based on their supply voltage variation. The optimal load-dependent V_{DS} was derived and validated both by simulations and laboratory measurements. We showed that, for real loads, in theory, we can completely restore both the DE and output power capability of PAs. However, for complex loads, the efficiency is not completely restored. Nonetheless, we received good feedback from the scientific community, and so, we have considered our goal of developing a novel load insensitive technique accomplished.

Then, we moved forward starting to expand the developed technique for application in DPAs. This task was more demanding, but we have completed it by assuming independent supply voltages for the carrier and peaking PAs. The carrier amplifier optimal V_{DS} was derived to keep the BO efficiency and output power level constant. And the peaking amplifier V_{DS} was derived to maintain the FP efficiency and the BO level constant. This technique was validated both in simulation and in laboratory for a specifically designed DPA prototype,

validating our goal of developing a load insensitive PA architecture with high efficiency at BO.

The final aim of this work was accomplished by developing and presenting a QLI PA system that includes V_{DS} variation at the DPA output stage, an adaptive input stage to generate load-dependent input driving signals, and real-time tracking of the amplifier output load. In order to track the PA output load in real time, we developed a compact and low loss impedance measurement system based on a novel algorithm that enables load measurements using a very simple circuit.

Chapter 7

Future Work

Throughout this work we have developed and proposed various techniques that aim at reducing the performance degradation of PAs operating with non-optimal loads. The first attempt was to use a simple, and low loss, TMN to reduce the load variation seen by the amplifier. Although this method was able to keep the PA output power level constant, the added IL slightly reduced the amplifier efficiency. Then, we have proposed a novel method, based on the V_{DS} modulation, to keep both the efficiency and output power constant under load variations. However, this method is not able to completely restore the efficiency under operation for complex loads with high imaginary part, as seen in Fig. 7.1.

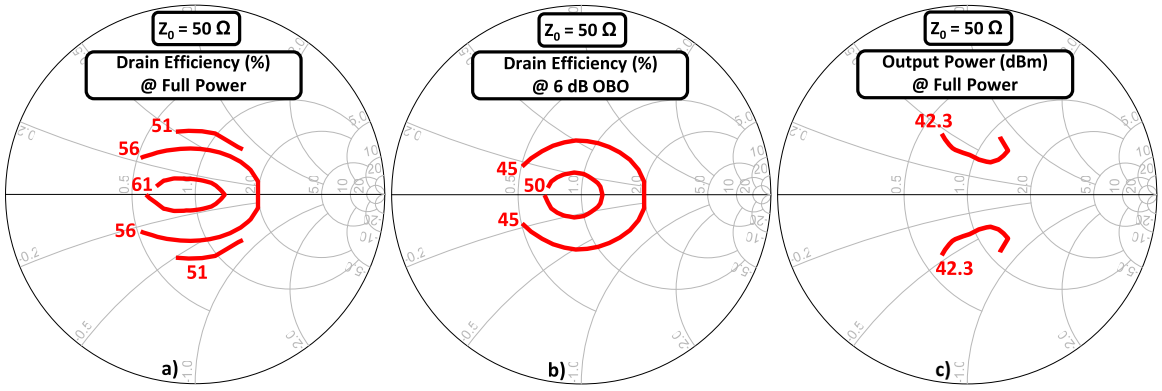

Figure 7.1: Simulated DE of the developed QLI DPA prototype at FP, a), and BO, b), and FP output power capability, c).

Therefore, to complement the developed final prototype it would be necessary to improve its performance under complex loads. One possible approach would be to include a compression network capable of eliminating the imaginary part of complex loads, as shown in Fig. 7.2 a). During the first task of this work a similar network, based on gallium arsenide (GaAs) switches, was already designed and implemented. The obtained simulated load compression is shown in Fig. 7.2 b), but the losses are still considerable for high efficiency applications. Consequently, future research could be focused on reducing the TMN losses.

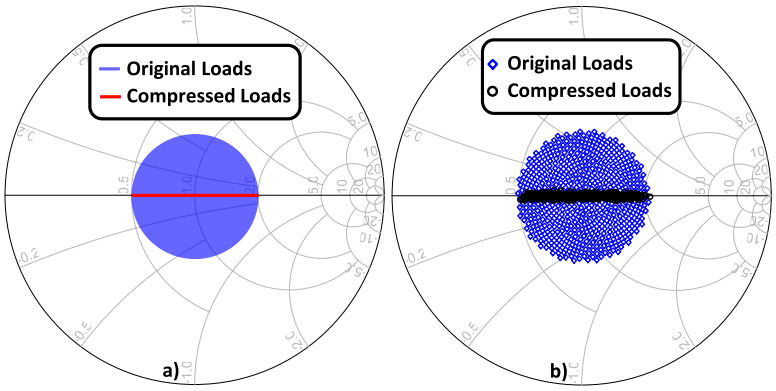

Figure 7.2: a) Desired load compression for improvement of the developed DPA prototype performance. b) Simulated load compression obtained from the network designed in the first task of this PhD work.

Other problem that we have identified in the developed prototype is the efficiency degradation caused by the added hardware, mainly, due to the dc-to-dc converters. This reduces the amplifier performance even for operation under the optimal load, i.e., when the output load variation is very small or nonexistent. Thus, further research could also be focused on dedicated dc-to-dc converters, which should be specifically designed for the application that was presented during this PhD work.

Moreover, we have also identified some performance degradation when using the developed prototype under modulated signal excitation. Since telecommunications are one of the most important applications for the developed system, this issue should be addressed in the future. Although we have not closely evaluated this problem, we expect some degradation to come from the impedance measurement and also from the optimal V_{DD} computation. In most of the cases, we will have a filter and/or other components between the PA and the antenna, introducing a significant electrical delay. In this scenario, the actual load that is presented to the PA can vary over the signal bandwidth and be difficult to measure. Moreover, even if it can be measured, it would produce various optimal V_{DD} values. Thus, further research would be necessary in order to solve this problem and be able to choose the best V_{DD} value for these scenarios.

Lastly, other future research could also include the presented prototype integration, including all the sub-circuits, to reduce the number of coaxial transitions and associated losses. A MMIC implementation of the impedance measurement circuit and QLI DPA prototype is also preferable for future tests at higher millimeter-wave (mmWave) frequencies, and advantageous for usage in 5G massive MIMO transmitters.

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Appendices

Appendix A

Tunable Matching Network

Switch-Based Variable Length Stubs Network for PA Load Sensitivity Reduction

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Switch-Based Variable Length Stubs Network for PA Load Sensitivity Reduction

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ABSTRACT In Fifth Generation (5G) Multiple-Input Multiple-Output (MIMO) transceivers, Power Amplifiers (PAs) driving antenna arrays experience varying loading conditions. In fact, the input impedance of each antenna element changes within a Smith chart region, a phenomenon attributed to mutual coupling, which will affect PA behavior. Although PA performance is load dependent, its output power and drain efficiency contours are nearly constant along specific straight lines in the Smith chart, a characteristic that can be exploited to improve PA performance in variable load scenarios. This work presents a compression network, featuring switch-based variable length stubs, capable of transforming any load within a 2.1 Voltage Standing Wave Ratio (VSWR) circle into a purely resistive load. This network was designed, implemented, measured and used in the Output Matching Network (OMN) of two Class E PAs being able to compensate the output power variation of the first PA and the efficiency degradation of the second PA under the defined load variation. The innovation of this network is the capability to reduce output power or efficiency load sensibility, which is very much desired in many applications, by using an easily implementable and low loss (0.3dB-0.5dB) network. By properly adjusting the distance between stubs and switches it is also able to transform slightly different load patterns into other optimal lines or curves.

INDEX TERMS Compression network, load insensitiveness, load modulation, MIMO, mutual coupling, power amplifiers.

I. INTRODUCTION

Many microwave circuits require matching networks to achieve maximum power transfer, higher linearity or higher conversion efficiency. Typical matching networks perform a static impedance matching that fails under variable load scenarios. Such scenarios can be found on RF-to-DC converters [1], on the design of load modulated Power Amplifiers (PAs) [2], in PAs driving antenna arrays, and in antennas presenting variable mismatch. Antenna mismatch, in particular, can occur due to various environmental reasons, typically due to perturbations in its near field. In the case of Multiple-Input Multiple-Output (MIMO) transceivers, each antenna element is affected by its neighboring elements due to mutual coupling, which will cause an apparent load change for the PAs in each transmit path [3]. So, while the use of antenna arrays enables beamforming, which leads to an overall system efficiency improvement, this load variation results in PA performance degradation, making the use of such systems less viable. Even though PA performance is degraded when operating for this wide range of loads, Pedro et. al. have demonstrated that, at the intrinsic device plane, efficiency is maintained high for a wide range of real loads, due to the elongated contours along the real axis of the Smith chart [4]. The output power, on the contrary, varies very much along this axis, but is constant along vertical straight lines that are perpendicular to it. On the other hand, for the maximum output power region, constant efficiency and power vary along the same direction.

In this work, these particularities are exploited during the design of two PAs. One is designed for maximum efficiency, in which the compression network is used to reduce the output power variation. Another one is designed for maximum output power, in which both efficiency and output power variations are reduced, by taking advantage of their parallel constant lines. It is also important to consider that, at the

The associate editor coordinating the review of this manuscript and approving it for publication was Luyu Zhao.

TABLE 1. Comparison between different methods used to compensate PA behaviour under undesired dynamic load modulation.

Methods/Techniques	Advantages	Disadvantages
Magnetic Isolator [6]	Very good isolation between PAs and antennas.	Difficult to implement in MMIC. Heavier and larger circuits.
Antenna Decoupling Networks [7] - [11]	Reduction of load variations due to mutual coupling on antenna arrays, mitigates the problem reducing its cause.	Difficult to implement on large antenna arrays. Not helpful for load variations due to other causes.
Balanced Amplifiers [12]	Compensates the output power variation without adding extra complexity on the antenna.	Each amplifier is composed by two smaller amplifiers and two 90º hybrid couplers. Under mismatch the efficiency is lower due to dissipated power on the isolation load.
Digital Doherty (peaking usage to attenuate load variations) [13]	Takes advantage of the extra complexity of such design. Uses the peaking current to compensate the load seen by the carrier.	Cannot maintain the same back-off efficiency. To compensate higher loads the peaking is turned off, while for lower loads the peaking current must be very high.
Passive Compression Networks [14]	Simplicity and good reduction of the load variation range.	Require more than one antenna behaving as identically varying loads.
Tunable Matching Networks [15] - [18], **[This Work]**	**Can be used in a broad range of applications. Accurately compresses load variation by changing the impedance transformation depending on the control inputs.**	Requires adjustable components in the design. **Losses in the dynamic network present a bottleneck to the technique in terms of efficiency.**

extrinsic device's drain terminal, these contours are elongated along lines in the Smith chart that depend on the device's operation class, intrinsic and extrinsic equivalent circuit elements.

There are various methods to improve the immunity of PAs to load variations, each of them with advantages and disadvantages, as shown in Table 1. Some methods are designed to solve this problem on MIMO arrays by reducing the mutual coupling level between elements (i). Other methods are applicable to a broader range of cases since their focus is to reduce the load variation seen by the PA, independent of its cause (for example hand-effects [5]). These last methods can be characterized in three classes: Typical magnetic isolator [6]; Load insensitive PA topologies (ii); Compression or tunable matching networks (TMNs) to be added between the PA and antenna (iii).

(i) The methods that are focused on reducing the coupling between antenna elements can be based on different structures [7], [8]. The usage of matching and decoupling multi-port networks on the antennas to reduce the mutual coupling and consequently the impedance variation, as theoretically used in [9], is also a widely known strategy. The problem with this strategy is the synthesis of the decoupling network, which can be very difficult for higher density arrays. Some implementations can be found for 2x1 arrays but with higher antenna count are seldom found due to scalability problems [10], [11].

(ii) Regarding PA topologies, some can be more insensitive to load variations, such examples are balanced amplifiers [12] or properly controlled digital Doherty PAs [13]. However, these PA designs are more complex and do not completely solve the problem. Thus, the inclusion of compressing or TMNs is beneficial on such systems.

(iii) Passive compression networks, based on fixed components, would be alluring due to their lower complexity and losses. However, it can be shown that reciprocal, passive and non-dissipative two-ports cannot compress the Voltage Standing Wave Ratio (VSWR) (they simply shift impedances to a different reference impedance). It has also been shown that (reciprocal, passive and non-dissipative) multiport (three ports or more) networks can compress the VSWR at one port, when terminated with synchronously varying loads at other ports [14]. However, this is a requirement that is not met, except for a very specific set of applications. TMNs are the most versatile option. They are able to perform a dynamic load transformation, can be adjusted after their implementation and are useful in distinct applications. However they require variable components, typically capacitors which tend to have low quality factors. One alternative is to use switches to implement commutable capacitors and/or variable length stubs.

Some applications based on switched capacitor banks have already been used to correct the performance of PAs. This approach is used in [15] with low tunability range, and in [16] with broader compression range but with losses up to 2dB. Thus, the number of switches required to accurately compress the necessary Smith chart area into a line would be too high, resulting in prohibitive high losses and implementation difficulties. In [17] the authors implemented a variable length stub based on MOS switches. However the phase variation obtained is low and no comments are made on the dissipation losses of the network, which is a determinant factor in power applications. In [18] the authors design a reconfigurable stub impedance matching network using Micro-Electro-Mechanical (MEM) switches. However it only compresses loads inside a 1.3 VSWR circle, which is not enough for the expect load variation in MIMO applications, and has high losses (1dB - 1.7dB).

This work presents an easily implementable solution, based on switched variable length stubs that compensate the reactance of output loads, compressing any load inside a 2.1 VSWR circle into the real axis of the Smith chart.

This real axis line is then rotated, by adding a phase delay, into any other line on the Smith chart. The proposed network constitutes an optimized solution for the compromise between impedance compression (circle to line) and small complexity, i.e. low losses (0.3dB - 0.5dB).

This paper is organized as follows, Section II presents the theory and design of the compression network. Section III shows the fabricated network and explains the optimization process and validation measurements. Section IV demonstrates, by simulations, the advantage of using such network on the design of Output Matching Networks (OMNs) for two PAs. Section V presents the measurements of a fabricated PA with and without the compression network. Finally, Section VI presents the conclusions of this work.

II. REACTANCE COMPRESSION NETWORK

Many efforts are being made on reducing the mutual coupling between each element of an antenna array. However in many cases, for patch planar antenna arrays, a mutual coupling of around −18dB is still expected [7], [8]. If each element is considered to be surrounded by eight other (center element of a 3x3 array), a coupling level of around −9dB or higher can be expected. During this work, the input impedance of each element, Z_l, is considered to vary within a worst-case 2.1 VSWR circle that is equivalent to a total coupling level of −9dB and has been verified in MIMO antenna arrays dynamic impedance measurements [19], [20]. In order to eliminate the reactance of every load inside this circle, we tested the possibility to perform the compensation with a parallel element. The parallel compensation reactance, X, must be determined to eliminate the imaginary part of Z_{in} (1), as stated in (2) and further developed in (3).

$$Z_in = \frac{Z_l \cdot jX}{Z_l + jX} \tag{1}$$

$$imag(Z_in) = 0 \tag{2}$$

$$\frac{X \cdot real(Z_l)^2 + imag(Z_l) \cdot X \cdot (imag(Z_l) + X)}{real(Z_l)^2 + (imag(Z_l) + X)^2} = 0 \tag{3}$$

Figure 1 shows the calculated compensation reactance, X, for each load within the considered circle. This reactance values can be generated with one variable length short circuit stub, implemented using shunt switches [17]. However, this solution requires a wide range of reactance values from $[-\infty, -50]$ and $[50, \infty]$ that would lead to a very long stub with switches placed far apart from each other. The switches placed further from the end of the stub will operate in high impedance regions and, consequently, experience higher voltage swing. For this higher voltage swing the "off-state", parallel, losses of the switches are much higher due to the finite off resistance. The alternative is to use shorter stubs that synthesize only the inductive reactance values, $[50, \infty]$. The stubs were designed with four switches, which allow for a total of five different lengths. This length-resolution is enough to obtain quasi-real loads. Yet, with inductive terminations, only capacitive loads are compensated.

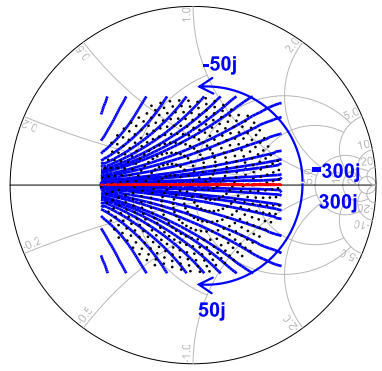

FIGURE 1. Contours of the calculated parallel compensation reactance (solid blue) for each load inside the 2.1 VSWR circle (black dots).

In order to solve this problem (without using longer stubs) two identical stubs, separated by a quarter wavelength line, have been used, as shown in Fig. 2. For this particular separation, the loads seen by the second stub (s5-s8) are rotated by 90°. Thus, the non-compensated inductive loads are now capacitive and can be compensated by the same inductive reactance terminations.

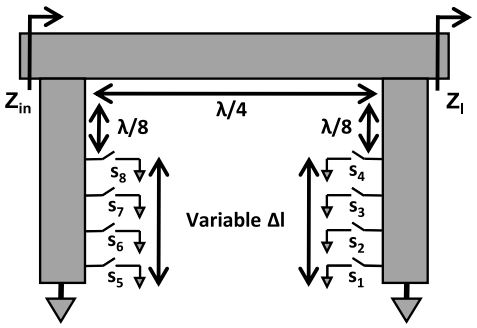

FIGURE 2. Schematic of the designed compression network.

If it is desired to transform a slightly different load variation pattern into a line or curve (that is optimal for a specific case), one will have to deduce the necessary parallel reactance values. Then, these reactance values can be obtained in practice by adjusting the distance between the stubs and switches. This makes the presented network adaptable for many cases and applications.

III. FABRICATION AND MEASUREMENT

This section describes the practical implementation and the measurement of the designed compression network (Fig. 2). In order to implement the variable length stubs with the available technology, we chose commercial packaged Gallium Arsenide (GaAs) RF switches (MACOM MASWSS0181). These switches were measured as part of a sub-circuit including proper DC and RF block capacitors, on RF and DC control ports, respectively. The measured s-parameter data of the switch blocks was used to re-tune the stub design prior to fabrication. The stubs have also been measured before the fabrication of the complete compression network, allowing

for a final tuning of the distance between stubs. These intermediate circuits are shown in Fig. 3. The calibration was performed using a specifically designed Thru Reflect Line (TRL) calibration kit. The digital control of the RF switches is differential due to their internal design. So, their state was controlled by physical switches and inverters, in order to generate the required differential control voltage. The complete circuit can be seen in Fig. 4.

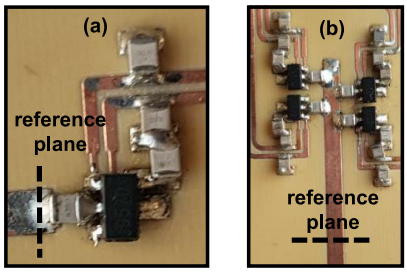

FIGURE 3. Switch block (a) and stub (b) characterization fixtures.

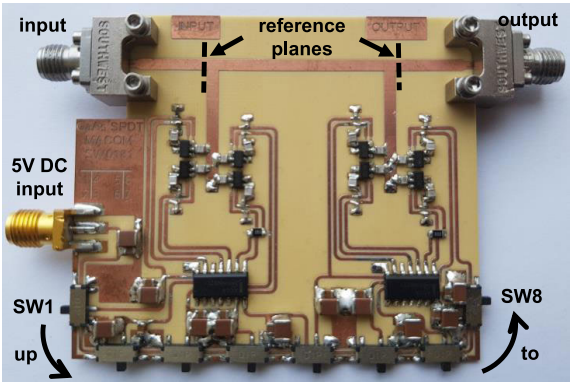

FIGURE 4. Implemented compression network.

The circuit was measured using the previously developed calibration kit, for the twenty-five possible states. The results were imported to Advanced Design System (ADS), and used to validate the reactance compensation behavior of the fabricated network. The compensated loads obtained using the optimal states for each original load are presented in Fig. 5 (b). It is also shown the shape of the loads before the second stub, which was optimally distributed by the first stub along the lines that are better compensated by the 5 possible terminations of the second stub. The imaginary part of the loads within the initially determined circle was successfully reduced, as shown in Table 2. However, comparing to the simulated results of Fig. 5 (a), there is a deviation towards lower real loads. This happens due to a lower impedance line between stubs, which can be explained by the imprecision on the fabrication process. Nevertheless, this compression can be used to reduce PA efficiency and/or output power degradation due to load variation, by keeping the operation for fewer loads distributed along specific lines. The fabricated compression network measured results show an average 0.42dB loss, which is determinant for success of the inclusion of such network in OMNs. These losses have been found to be caused by the non-idealities of the used switches: the package, the non-zero Ron and the finite Roff. Losses in the transmission lines account for a maximum of 0.1dB.

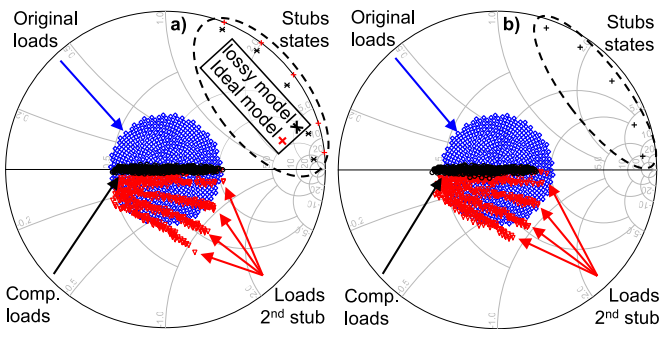

FIGURE 5. Simulated (a) and measured (b) stub states, uncompensated loads, load presented to the 2nd stub and compensated loads.

TABLE 2. Measured losses and residual reactance after compensation.

Average Losses	Worst Case Losses	Average Reactance	Worst Case Reactance
-0.42 dB	-0.532 dB	0.77j	4.75j

IV. APPLICATION TO THE DESIGN OF PA's

This section demonstrates, in simulation, the benefits of using the fabricated compression network at the output of two Class E PAs, designed for 2GHz. The first one (PA 1) operates at the maximum efficiency load, whereas the second one (PA 2) was tuned for the maximum output power load. The inclusion of the compression network in the design follows the block diagram of Fig. 6, and two simulation models of the network are used. An ideal lossless model and a more realistic one that accounts for the switch losses.

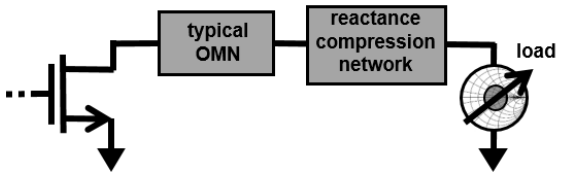

FIGURE 6. Block diagram of the PA output matching networks.

The OMN of the amplifier can be designed following the usual procedures. It is only required that harmonic terminations are isolated from the load, assuring that neither the output load nor the compression network influences them. Following this procedure, two OMNs were designed. One for the maximum drain efficiency load and another for the maximum delivered power load of the used Gallium Nitride (GaN) device (Wolfspeed CGH40010).

Figure 7 (a) presents the simulated load pull data of the PA 1, at 6dB of gain compression. The drain efficiency contours are plotted in red with a maximum value of 87.7% and a step of 5%. The output power is plotted in blue with a 1dB step. Figure 7 (b) shows the load variation both at the load and

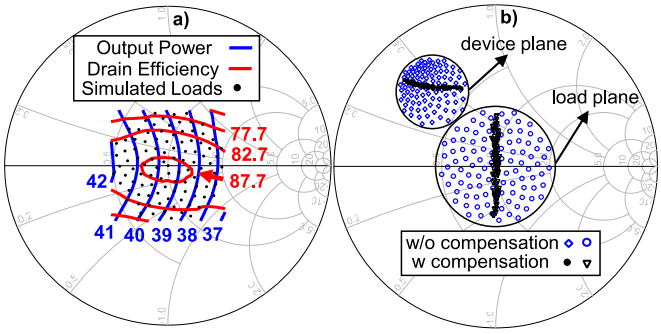

FIGURE 7. Load pull (a) and load compensation (b) of the PA 1.

device planes. The original load variation, without using the compression network, is shown by the blue diamonds (device plane) and circles (load plane). The load variation when the compression network is used between the PA1 and its original varying load (blue circles) is presented by the black dots (device plan) and triangles (load plane). As explained and shown in Section II, by using the compression network, it is possible to compress the loads inside a circle into the real axis of the Smith chart. For this amplifier, which presents a very high efficiency, it should be used to reduce the output power variation. Thus the PA must operate for loads distributed along a vertical line in the Smith chart, as shown by its Load Pull (LP) contours. Consequently the real loads presented by the compression network are rotated into the desired line by adding a phase delay before the PA. The chosen output power was 39.5dBm, which is the nominal power delivered to a 50Ω load.

The output power variation for the loads presented in the Smith chart is shown at Fig. 8. For the case without any compression network the variation is 5.3dB, and it is higher than 39.5dBm for loads lower than 50Ω and lower for higher loads. Using ideal lossless switches on the compression network, the output power variation is 1dB and its maximum is slightly higher than 39.5dBm. Using the measured model of the switches the variation is 1dB but its maximum slightly lower than 39.5dBm due to the added losses.

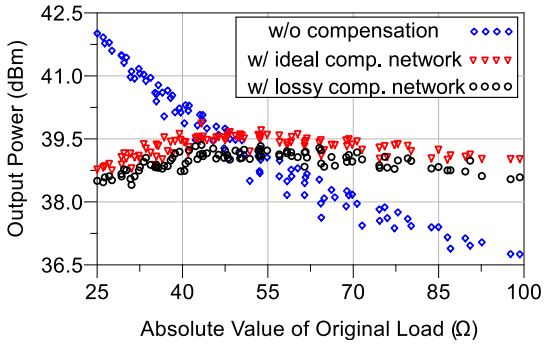

FIGURE 8. Output power before and after compensation (PA 1).

PA1 efficiency is shown at Fig. 9. Without compression network, the efficiency varies from 75% to 88%. By adding the lossless compression network the variation is still the same, however with the lossy compression network the efficiency becomes lower, varying from 70% to 82%. This 5% reduction in the efficiency is explained by the added losses after the OMN of the PA. The compression network added between 0.3dB and 0.5dB of losses, as shown in Fig. 8, which is translated into between 5% and 10% of efficiency degradation, depending also on the original efficiency of the PA. The efficiency degradation can be calculated from expression 4.

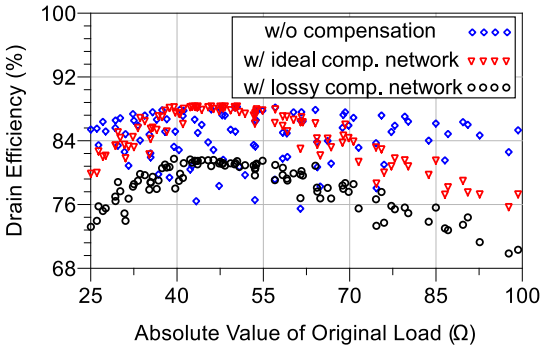

FIGURE 9. Drain efficiency before and after compensation (PA 1).

$$Eff_{lossy} = 10^{\frac{Loss_{dB}}{10}} \cdot Eff_{ideal} \tag{4}$$

PA 1 behaviour is clearly improved using the designed compression network. The output power becomes almost constant at 38.9±0.5dBm for any load inside a 2.0 VSWR circle at the cost of around 5% of efficiency. Without the compression network the output power can be as low as 36.5dBm for the worst case load, which is half of the nominal power of the PA.

When used in transceivers, PAs are required to guarantee some specified output power level. In the case of 5G networks using antenna arrays, the load of each PA changes due to coupling effects between antenna elements, thus without any compensation, PA 1 would not be able to guarantee the nominal output power of 39.5dBm. In order to expose this problem the Fig. 10 shows the output power of PA 1 with and without compensation when the specified output power level is 39.5dBm. For this application the amplifier without compensation is being operated at back-off for lower loads,

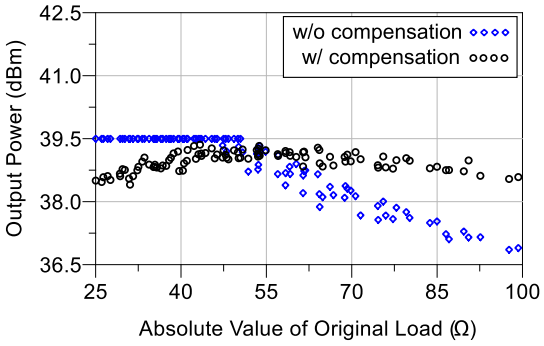

FIGURE 10. PA 1 output power limited to 39.5 dBm.

reducing its efficiency, and cannot guarantee the required power for higher loads. On the contrary, the compensated PA is able to guarantee an output power that is always higher than 38.4dBm and never higher than 39.5dBm.

For this application, the drain efficiency of the PA without compensation can become even lower than it is for the compensated PA, as shown in Fig. 11, due to the back-off operation for lower loads. The uncompensated PA would only be able to deliver a constant output power of 36.5dBm, meaning even more back-off for the lower loads and even lower efficiency.

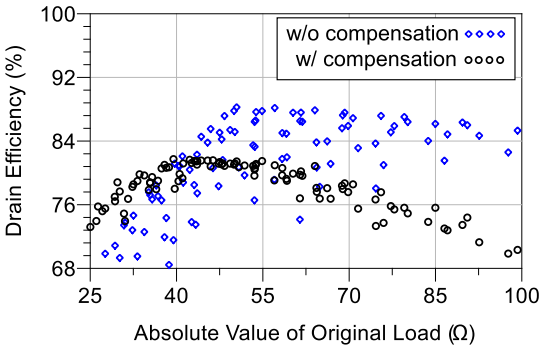

FIGURE 11. PA 1 drain efficiency for a limited output power of 39.5 dBm.

In Fig. 12 (a) the simulated load pull data of PA 2 is presented, for the same gain compression of PA 1 (6dB). Drain efficiency is plotted in red with steps of 10%. The output power is plotted in blue with a maximum value of 42.6dBm and steps of 1dB. Figure 12 (b) shows the load variation with and without the compression network at the device and load planes using the same symbols as Fig. 7 (b). For this amplifier, the focus is reducing the efficiency degradation for loads at the top region of the 2.0 VSWR circle. The output power of this PA is much higher, thus operating with very low efficiency significantly increases the dissipated power in the device, degrading its lifetime. In order to solve this problem, the compression network is used without any phase delay in order to present real loads to the PA, eliminating the top lower efficiency loads. For these real loads, after compensation, the output power is also maintained higher because of the PA's elongated power contours along the real axis.

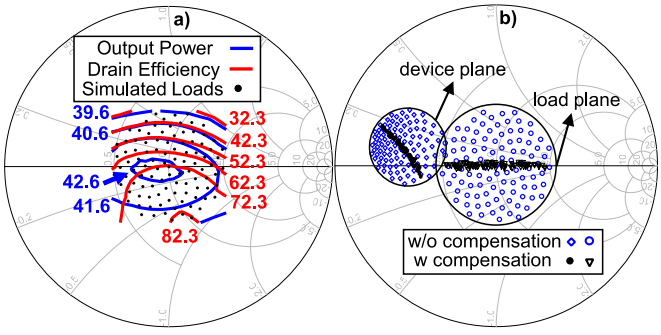

FIGURE 12. Load pull (a) and load compensation (b) of the PA 2.

Figure 13 shows the drain efficiency variation for PA 2. Without any compensation, the efficiency varies from 36% up to 84%. With compensation its lowest value is 61% using ideal switches model, and 57% for the lossy model.

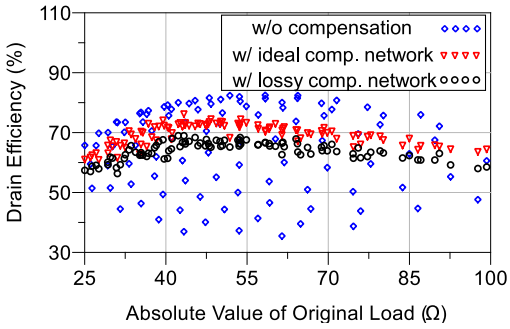

FIGURE 13. Drain efficiency before and after compensation (PA 2).

The output power variation of PA 2 is shown in Fig. 14. The amplifier, without compression network, has a variation of 3.2dB, from 39.6dBm to 42.8dBm. After compensation, this variation becomes 1.2dB. Its maximum output power is 42.8dBm and 42.4dBm, respectively, for the lossless and lossy models of the compression network.

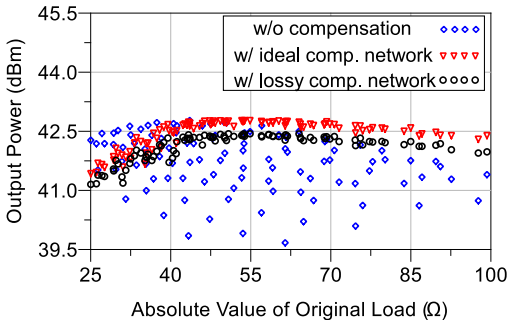

FIGURE 14. Output power before and after compensation (PA 2).

By using the designed compression network, the worst case of drain efficiency is successfully improved by more than 20%, from 35% to 57%, at the cost of 0.4dB on the maximum output power. Note that, although the maximum PA output power value is reduced, its minimum output power value was improved 1.6dB. After compensation, PA 2 is able to deliver more than 41dBm of output power with higher than 57% of efficiency to all the loads inside a 2.0 VSWR circle.

Table 3 synthesises all simulation results that were presented during this section. The results in bold represent the

TABLE 3. Concise simulated improvement results of PA 1 and PA 2.

	Lowest Eff.	Eff. Variation	Lowest Output Power	Output Power Variation
PA 1	75%	13%	36.7dBm	**5.3dB**
Comp. PA 1	70%	12%	38.4dBm	**1dB**
PA 2	**35%**	48%	39.6dBm	3.2dB
Comp. PA 2	**57%**	12%	41.2dBm	1.2dB

metric that was intended to improve with the use of the compression network.

V. PA MEASUREMENT VALIDATION

During this section the practical implementation and measurement of PA 1 is presented. This PA was chosen due to its higher drain efficiency. The objective is to validate the reduction of output power variation with measurements.

The used transistor was Wolfspeed CGH40010F, the capacitors are from ATC ceramic 800A series and the used substrate was Isola Astra 3. The PA was designed at 2GHz for the maximum drain efficiency load, and to the specific harmonic terminations that ensure a class E behaviour. Since the compression network does not ensure any specific load at the harmonics, it is necessary to guarantee harmonic isolation at the OMN. This was accomplished with harmonic traps close to the transistor's drain, which consist on very small parallel capacitors that ensure a short circuit at harmonic frequencies. Input and output matching networks were fabricated and assembled on an aluminium base with the transistor and two panel connectors, as shown in Fig. 15.

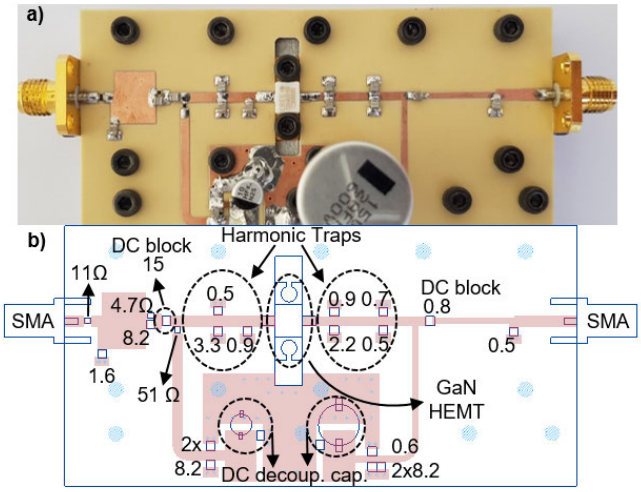

FIGURE 15. Photograph of the fabricated amplifier (a) and fabrication schematic including the value of all components, resistors in Ω and capacitors in pF (b).

The PA was measured on the setup shown in Fig. 16. The input signal was generated by a VSG, pre-amplified using a driver and calibrated at the input connector of the PA. The output is based on a mechanical load tuner (DS109L from WEINSCHEL ASSOCIATES), three 10dB attenuators and a Power Meter. The output calibration plane is at the output connector of the compression network. The losses of the tuner were measured and de-embedded for all the different synthesised loads.

Figure 17 (a) presents the interpolated LP of the fabricated amplifier and the measured loads, in black. The efficiency maximum is 76.3% with steps of 2%, while the output power step is 1dB. The measured LP is very similar to the simulated one, from Fig. 7 (a), with only 0.1dB of difference on the output power for the 50Ω load. The efficiency is 11.4% lower,

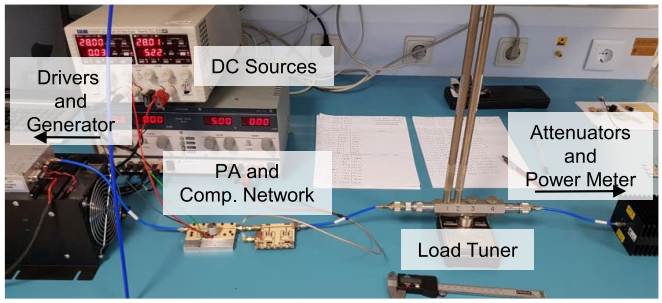

FIGURE 16. Laboratory measurement setup, where it is shown the PA connected to the compression network and the load tuner used to synthesise various loads.

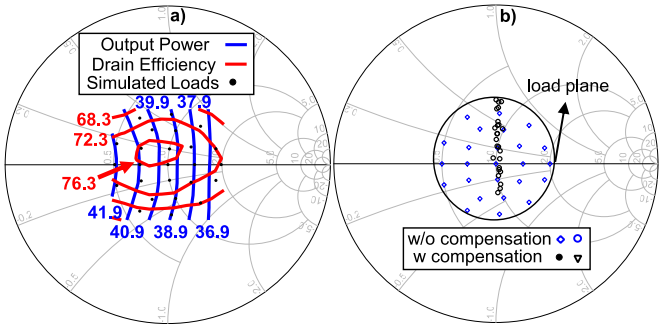

FIGURE 17. Measured load pull (a) and load compensation (b) of the implemented PA.

which can be explained by the losses in the fabricated OMN. In Fig. 17 (b) the loads presented by the tuner to the compression network are shown in blue diamonds. Also in Fig. 17 (b), the resulting loads after compensation are presented in black circles. The loads were measured both at the planes of the compression network and PA using a VNA. The compensated loads are aligned on a vertical line ($\angle\Gamma = 90°$), as expected. However, there is a deviation towards the top of the Smith chart that corresponds to the deviation to lower loads previously observed at Fig. 5 (b).

Figure 18 shows the output power of the implemented amplifier with and without compensation. This measured data can be compared to the simulations presented on Fig. 8. Without compression network, the variation of output power is almost 6dB and is reduced to 1.4dB after compensation.

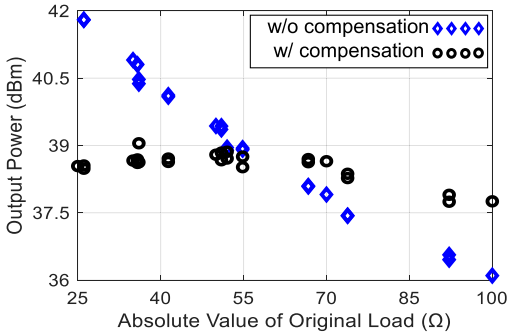

FIGURE 18. Measured output power before and after compensation.

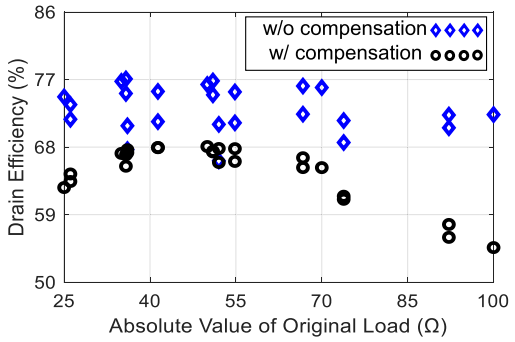

FIGURE 19. Measured drain efficiency before and after compensation.

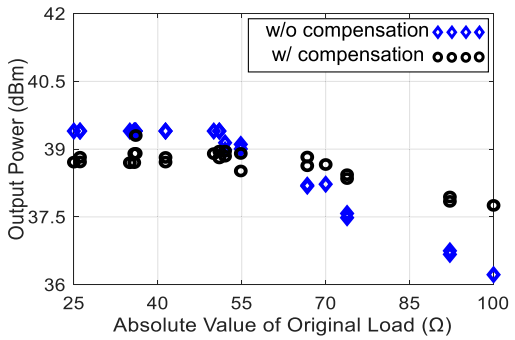

FIGURE 20. Output power of the implemented PA, limited to 39.4 dBm.

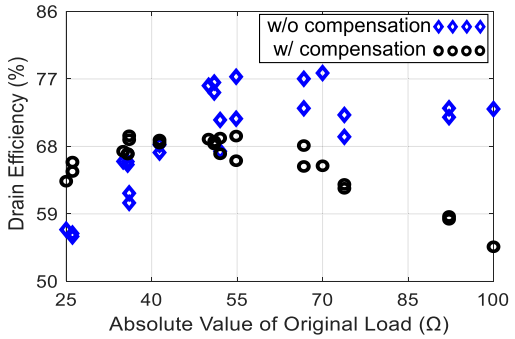

FIGURE 21. Drain efficiency of the implemented PA for a limited output power of 39.4 dBm.

However, the variation is only 0.9dB without considering the last three loads that have been deviated to the top of the Smith chart, due to imprecisions on the fabrication of the compression network, as mentioned on Section III. Figure 19 shows the correspondent drain efficiency that is slightly lower after compensation, as expected and previously seen in Fig. 9. Note that the three last points again differ from simulation results.

In Fig. 20 the output power is presented, limited to 39.4dBm. In Fig. 21 the drain efficiency corresponding to the output power values in Fig. 20 is shown. The correspondent simulations are presented on Fig. 10 and Fig. 11. Table 4 presents the results for a target output power of 39.4dBm. Without considering the three incorrectly compensated loads, the lowest output power after compensation is 38.3dBm while before compensation it was only 36.2dBm.

TABLE 4. Measured output power and efficiency w/ and w/o compensation. The results within parentheses do not consider the last three loads.

	Lowest Efficiency	Efficiency Variation	Lowest Output Power
W/O Compensation	56%	22%	36.2dBm
W/ Compensation	54 % (62%)	16 % (8%)	37.8dBm (38.3dBm)

VI. CONCLUSION

This work presented a compression network based on variable length stubs implemented with switches. These switches are placed close to the end of the stub in order to reduce off-state losses due to the high voltage swing. The fabricated network compensated the imaginary part of the loads distributed within a 2.1 VSWR circle. The measured input real loads vary between 20Ω and 85Ω instead of 25Ω and 100Ω, due to fabrication imprecisions. The compression network was used in the design of two class E PAs using Wolfspeed GaN devices at 2GHz. PA 1, designed for the maximum efficiency load, was improved using the compression network that successfully reduced its output power variation. PA 2 was designed for the maximum output power load and the compression network was used to improved the worst case efficiency. In this case it also reduced the output power variation significantly. PA 1 was fabricated and measured with and without the compression network. Its output power variation was significantly reduced, as expected. A slightly higher degradation was measured on both drain efficiency and output power for the three loads that suffer deviations from the initial design, due to fabrication imprecisions on the compression network. The losses of the compression network have been attributed mainly to the switches. These losses are caused by the package, the non-zero ON-resistance and finite OFF-resistance. Thus, in MMIC implementations, where the switches can be designed specifically for this purpose the losses are expected to be lower, making the usage of the designed network valuable to a broad range of applications.

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Prof. Pedro received various prizes, namely the Marconi Young Scientist Award in 1993, the 2000 Institution of Electrical Engineers Measurement Prize, the 2015 EuMC Best Paper Microwave Prize and the Microwave Distinguished Educator Award.

Appendix B

Impedance Measurement

A Compact Impedance Measurement Solution for Systems Operating in Load Varying Scenarios

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A Compact Impedance Measurement Solution for Systems Operating in Load Varying Scenarios

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ABSTRACT This paper presents a compact solution for impedance calculation obtained from low phase resolution stationary wave measurements, for RF power systems operating in load varying scenarios. The implemented system is based on a bi-directional coupler and makes use of the stationary wave periodicity, which is synthesized and measured via a digital phase shifter, a power combiner, and an envelope detector, in a specific arrangement. Instead of sampling a transmission line at various spatial points (sampled line architectures), both incident and reflected waves are sampled at one specific position, the stationary wave is obtained by sweeping the incident or reflected waves' phase, mimicking the slotted line principle and, from there, the impedance is obtained using a new signal processing algorithm that is now presented. Taking advantage of the developed technique, this can be done for only three phase shifter states, making the measurement fast and accurate. This compact measurement solution can compute the impedance of both real and complex loads inside a 2.1 voltage standing wave ratio circle with high accuracy (−28.8 dB) at a rate of 1 kHz and is appropriate for high power systems due to its simple architecture and very low total losses (0.075 dB).

INDEX TERMS Impedance measurement, impedance mismatch, power systems, stationary waves.

I. INTRODUCTION

The radio frequency (RF) and microwave worlds are crowded with systems that operate in many different frequency bands, with distinct output power and efficiency capabilities, as well as linearity, and bandwidth limitations. Changes to their expected operation environment can lead to severe performance degradation or even produce irreparable damages. One of the most relevant causes of performance degradation is related to load variations, which can occur in many different scenarios such as: phased arrays for satellite communications [1], or fifth-generation (5G) massive multiple-input multiple-output (MIMO) beamforming networks [2]; the hand effect while holding a mobile phone [3]; microwave cooking [4]; during plasma heating in, e.g., plasma-enhanced chemical vapor deposition (PECVD) process [5]; or in PAs charging cavities of particle accelerators [6].

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Various attempts have been made to solve, or at least mitigate, the consequences of load variations in these diverse applications. Isolators are the most common solution, being able to reduce the load variation presented to the system, dissipating the reflected power in a dummy load [7], unfortunately, at the expense of an overall system efficiency reduction. Moreover, isolators are bulky and expensive devices that are also very difficult to integrate. Sometimes, a different approach is followed considering more sophisticated output stage topologies, which are, by their nature, more insensitive to load variations, such as, for example, balanced power amplifier (PA) architectures [8]. However, these architectures introduce additional complexity and can only maintain performance up to a certain voltage standing wave ratio (VSWR).

Another alternative approach is to use controlled tunable matching networks (TMNs) that perform a dynamic load matching. They can be implemented with variable capacitors [9] or switched networks, such as, for example, capacitor

banks [10] and variable length stubs [11]. Despite its inherent high length and losses, this solution is very versatile, has a good tunability range, and its losses are becoming less restrictive as the switch and capacitor technology evolves.

Load dependent bias voltages (for drain or both drain and gate) can also be used to improve system performance under load varying scenarios [12], [13], without requiring extra components or added complexity in the RF path.

However, most of the described techniques require load-dependent analog or digital control voltages. The load variation can be predicted or pre-characterized in some cases, as phased arrays, where it depends on the selected beam-forming angle, but it comes from unpredictable causes in most of the cases. Consequently, there must be some way of, directly or indirectly, measuring the impedance that is being presented to the system. Of course, vector network analyzers (VNAs), slotted lines [14], or six-port reflectometers [15] can be used to measure the impedance seen by the considered systems. In the scope of this work, techniques with low insertion loss (IL), reduced cost, and low complexity are the most attractive ones and will be briefly described. VNAs are very complex and expensive systems, which, even in their most straightforward implementations, are still composed of many sub-circuits and sub-systems with significant IL [16]. Slotted lines and other systems based on reflectometer techniques, [17], that have been developed a long time ago are bulky and composed of mechanical moving parts that must be fabricated with very precise machining processes. Some approaches based on the same principle have been implemented, as is the case of sampled lines [18], in which, instead of using moving components, the voltage is sampled by various power detectors placed over a line. However, the used detectors introduce high IL [18]. Six-port reflectometers implement a technique that needs at least four sampling ports to measure the load. This can be implemented with various power detectors placed along a line or in different positions at the output matching network [19], [20]. However, the IL is usually high due to the added power detectors, and, in some cases, the measurement accuracy is poor.

Many measurement systems that have been developed throughout time can also be based on bi-directional couplers. The simplest ones have low accuracy and, in some cases, can only measure the reflection coefficient amplitude or phase information [21], [22]. The more complex ones, which are also more accurate, suffer from scalability issues [10], [23]. Among all of them, we highlight one that was originally conceived in [24] to increase the sensitivity of a bio-medical system, destined to measure small mismatch variations around an average value, without distinguishing between phase and amplitude variations. In this work, we will use a circuit topology based on the one presented in [24], but that is capable of measuring the absolute load in amplitude and phase, not only the magnitude of its relative variations with respect to an average value. For that, the novel technique described in this manuscript, artificially synthesizes the stationary wave by setting a few different phase-shifter states – a method that was implemented in the past using bulky mechanical moving parts [17] –, making it possible to determine the complex impedance from the synthesized wave using a specially designed signal processing algorithm.

This paper is structured as follows. Section II explains the used hardware and presents the theoretical formulation for the stationary wave synthesis. Then, in Section III, the impedance computation algorithm is presented. Section IV shows the practical prototype implementation and the measurement setup. Finally, in Section V, the proposed method is tested, and the measurement results are discussed, while Section VI summarizes the main conclusions of this work.

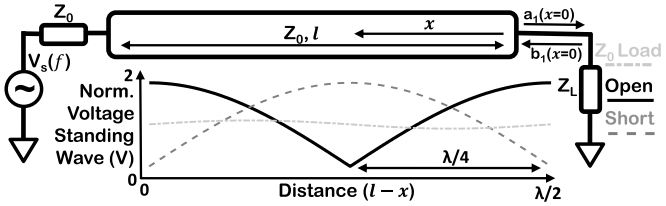

FIGURE 1. Voltage standing waves normalized to the incident wave along a λ/2 line for three loads. An open circuit in solid black, a short circuit in dashed gray and a near matched load (close to Z_0) in dash-dot lighter gray.

II. MEASUREMENT TECHNIQUE AND ASSOCIATED HARDWARE CONSTRAINTS

In a physical line, as shown in Fig. 1, the stationary wave is generated by the superposition of the incident wave, $a_1(x)$, and reflected wave, $b_1(a_1, \Gamma, x)$. The amplitude of this stationary interference pattern, V_{SW}, depends on the sampling position, x (note that x is defined here as the distance to the load), the line termination (or load), Γ, and the incident wave amplitude, $|a_1|$. The dependence of V_{SW} on the position is due to the variable phase difference between $a_1(x)$ and $b_1(a_1, \Gamma, x)$ due to their opposite propagation directions. Hence, the value of V_{SW} can be given by the voltage standing wave:

$$V_{SW}(|a_1|, \Gamma, x) = |a_1||e^{j\beta x} + \Gamma e^{-j\beta x}|, \tag{1}$$

for a line of length l, angular wavenumber β and terminated with a load Z_L, resulting in a reflection coefficient Γ.

The measurement of the stationary wave has been used for a long time to compute the reflection coefficient, Γ, or, similarly, Z_L, in slotted lines. The absolute value is calculated from the V_{SW} maximum and minimum values, and the phase is obtained from the position of the first minimum:

$$\begin{aligned} \Gamma &= \left(\frac{\mathrm{VSWR}(\Gamma) - 1}{\mathrm{VSWR}(\Gamma) + 1}\right) e^{j(2\beta x_0 - \pi)}, \\ x_0 &= \underset{x\in[0,\lambda/2[}{\arg\min}\,(V_{SW}(a_1, \Gamma, x)), \\ \mathrm{VSWR}(\Gamma) &= \left(\frac{\max_{x\in[0,\lambda/2[}\,(V_{SW}(a_1, \Gamma, x))}{\min_{x\in[0,\lambda/2[}\,(V_{SW}(a_1, \Gamma, x))}\right). \end{aligned} \tag{2}$$

For cases where it is difficult to measure the distance to the load, x_0 is the relative distance between the measured

minimum and a reference minimum obtained with a short-circuit termination.

Using bulky mechanical moving parts or various lossy voltage detectors in different spatial points is not always possible depending on the envisaged application due to concerns of complexity, size, and insertion losses.

Our approach to this problem is based on the fact that, as it can be seen from (1), the V_{SW} can be artificially synthesized by a phase variation between $a_1(x)$ and $b_1(a_1, \Gamma, x)$. For that purpose, in this work, we use the system of Fig. 2 to sample both the incident and reflected waves at one fixed spatial position and then, using a phase shifter, mimic the distance-dependent phase shift that occurs between them in a physical line.

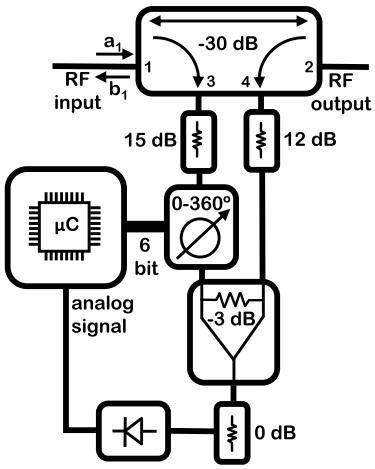

FIGURE 2. Functional block diagram of the designed impedance meter system.

As mentioned in the Introduction, this system is similar to the one first proposed in [24], where a sensitivity enhancement technique was developed. In that work, the phase shifter was not of primary importance because the technique – aimed at detecting amplitude variations of the load with respect to an average value – is equally effective in a broad range of phase values (at least 90° around 180°) and is fixed at a particular state. In our case, where the absolute load value is to be measured in amplitude and phase, the phase shifter is a critical component since it needs to be swept between 0° and 360° to mimic the phase delay that would occur in a 180° ($\lambda/2$) line, as seen in (1). The resulting synthesized V_{SW} (obtained using a conceptual system implementation in simulation) is shown in Fig. 3, for three different loads.

Besides that, in [24], the attenuation is chosen to null the sum between the incident and reflected waves for a specific phase delay. Here, the different attenuation values are chosen to control the generated stationary wave amplitude. Setting the incident wave attenuation higher is necessary to maximize the amplitude of the synthesized stationary wave (to reduce the analog-to-digital converter (ADC) quantization error) while keeping it within the allowed detector range for all the expected loads. The two used attenuators are also

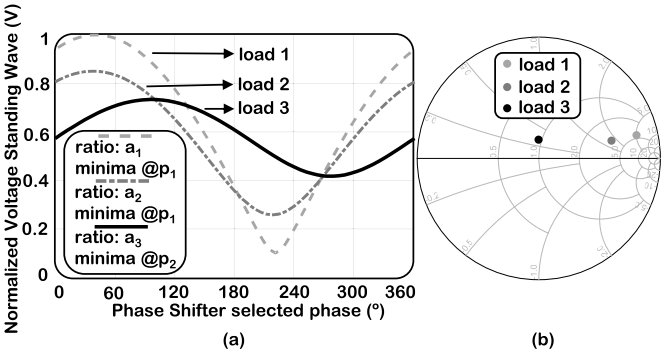

FIGURE 3. a) Simulated voltage standing waves for various loads resulting in different maxima to minima ratios and minima positions. b) The correspondent loads plotted on the Smith chart. The lighter dashed plot corresponds to load 1, with higher $|\Gamma_U|$, that produces the ratio a_1, with minima at p_1. The dash-dot plot corresponds to load 2, with minima for the same phase, p_1, but with a lower ratio, a_2, that corresponds to a lower $|\Gamma_U|$. The solid black plot is the stationary wave for load 3 with minima corresponding to a different phase, p_2, and the lowest ratio, a_3, since it is the closest to 50 Ω.

important to match the coupled outputs of the coupler and isolate it from the rest of the circuit. Another attenuator can be added before the envelope detector, which can be used to attenuate the stationary waveform average value. Thus, this attenuator can be selected to adjust the detected signal for different power levels without changing the first two attenuators' values. Note that all the attenuators' values are fixed for all the measurements performed in this work.

The bi-directional coupler must be carefully selected (or designed) having some important figures-of-merit in consideration: its IL should be as low as possible since the coupler is connected in the main RF path and its directivity should be maximized because the coupler samples the main line and should provide information of $a_1(x)$ and $b_1(a_1, \Gamma, x)$ on ports 3 and 4, respectively. Note that, the dependence of the reflected wave sample (port 4) on the incident wave (typically much higher than the reflected one) would make the measurement inaccurate.

The envelope detector should be linear in dB, so that the ADC sampling resolution is independent of the input power level, P_{in}. Note that its dynamic range can be traded-off with ADC resolution, since, in order to maintain the measurement accuracy for a specified maximum VSWR and P_{in} range, a lower envelope detector dynamic range requires stationary waves to be synthesized with a lower amplitude that will require higher ADC resolution. Finally, the ADC sampling rate and microcontroller performance set the impedance measurement maximum time rate.

Assuming a high directivity coupler, an ideal phase shifter, and a linear envelope detector, the resulting synthesized stationary wave is mathematically described. The incident and reflected wave samples will be, from now on, referred to as a_{1U} and b_{1U}, respectively (U for uncalibrated, as they represent an uncalibrated measurement of these waves). As explained before, to synthesize V_{SW}, a_{1U} and b_{1U} are

added with a variable phase difference, as described in:

$$V_{SW}(a_{1U}, b_{1U}, \Phi) = |a_{1U}e^{j\Phi} + A_d b_{1U}|, \quad (3)$$

where A_d represents the attenuation difference between the two paths, and Φ is the variable phase delay introduced by the phase shifter. As previously mentioned, the goal is to mimic the phase difference due to opposite propagation directions in a physical line. For this, and as is shown in Fig. 3, the phase-shifter must vary between 0° and 360° since the phase-shift due to distance in a line is applied to both waves, whereas here we apply the phase-shift only to one of them. The phase shifter can be included either in the incident or reflected wave paths. However, since it has a considerable IL ($\approx$ 5 dB) and the incident wave attenuation should be higher, we decided to include it there using its IL as part of the needed attenuation.

It is also still possible to describe b_{1U} as a function of a_{1U} and an uncalibrated load that is described as a complex reflection coefficient, $\Gamma_U = |\Gamma_U|e^{j\theta}$. Thus, the reflected wave can be written as a function of a_{1U} and Γ_U:

$$b_{1U}(a_{1U}, |\Gamma_U|, \theta) = a_{1U}|\Gamma_U|e^{j\theta}. \quad (4)$$

Finally, (3) and (4) can be further developed into

$$V_{SW}(|a_{1U}|, |\Gamma_U|, \theta, \Phi) = |a_{1U}||e^{j\Phi} + A_d|\Gamma_U|e^{j\theta}|, \quad (5)$$

where the attenuation difference, A_d, can be seen as part of the uncalibrated reflection coefficient magnitude, and since it is a linear error, it can be later corrected with a SOL calibration. The term $|a_{1U}|$ is just a scaling factor that depends on the input power level, P_{in}. This term does not contribute to the ratio between the maxima and minima of the synthesized wave, and thus the load computation algorithm is insensitive to its value.

III. LOAD COMPUTATION ALGORITHM

Comparing the waveforms of Fig. 3 a) with the loads plotted in the Smith chart of Fig. 3 b) it can be seen that, as expected, the amplitude of the stationary wave is higher for more reflective loads, whereas its phase is directly related to the phase of Γ_U. So, the synthesized wave amplitude and phase can be used to calculate the uncalibrated load, as previously shown by (2). However, this method can be very inaccurate because it only considers two measured points (the maximum and minimum), which can be affected by measurement imprecisions, fixed phase-shifter resolution, and noise. Moreover, the maximum and minimum values can happen for different phase-shifter delays, depending on the measured load. This leads to the necessity of a low phase-shifter step or to the use of search algorithms, which will increase the measurement time due to the high number of acquisitions.

Contrary to these traditional methods, a different technique that uses the available measured points to approximate the known model to the stationary wave is now presented and constitutes one of the main novelties of this work. We start by noting that, although $V_{SW}(|a_{1U}|, |\Gamma_U|, \theta, \Phi)$ is a complicated function of its variables, its squared value is simply a cosine function of Φ plus an offset. Therefore, it can be described by only three numbers (cosine amplitude and phase, and average) enabling an easier fitting using known signal processing tools, such as the Fourier transform.

$$V_{SW}(|a_{1U}|, |\Gamma_U|, \theta, \Phi)^2 = |a_{1U}|^2(1 + |\Gamma_U|^2 + 2|\Gamma_U|\cos(\Phi - \theta)). \quad (6)$$

Since ${V_{SW}}^2$ is a cosine function of Φ with a constant (dc) pedestal, it can be fitted to the measured data by calculating its average, and its fundamental amplitude and phase. The average value is calculated from the Fourier transform zero-order term,

$$V_{SW0}(|a_{1U}|, |\Gamma_U|) = \frac{1}{2\pi}\int_0^{2\pi} V_{SW}(|a_{1U}|, |\Gamma_U|, \theta, \Phi)^2\, d\Phi. \quad (7)$$

And the amplitude and phase of the cosine component are given by the Fourier transform fundamental term,

$$V_{SW1}(|a_{1U}|, |\Gamma_U|, \theta) = \left(\frac{1}{2\pi}\int_0^{2\pi} V_{SW}(|a_{1U}|, |\Gamma_U|, \theta, \Phi)^2\cos(\Phi)d\Phi\right) - j\left(\frac{1}{2\pi}\int_0^{2\pi} V_{SW}(|a_{1U}|, |\Gamma_U|, \theta, \Phi)^2\sin(\Phi)d\Phi\right). \quad (8)$$

At this stage, the load can either be calculated from the amplitude and phase of the model using (2) (but no longer depending on two single measurements), which is the approach in Appendix A, or by further developing (7) and (8) to obtain their dependency with Γ_U, as:

$$V_{SW0}(|a_{1U}|, |\Gamma_U|) = |a_{1U}|^2(1 + |\Gamma_U|^2), \quad (9)$$

and

$$V_{SW1}(|a_{1U}|, |\Gamma_U|, \theta) = |a_{1U}|^2|\Gamma_U|e^{-j\theta}. \quad (10)$$

By solving (9) and (10) in respect to Γ_U (in its absolute and phase values), it is shown that it only depends on the calculated dc and fundamental components, as:

$$\Gamma_U = |\Gamma_U|e^{-j\angle V_{SW1}(|a_{1U}|, |\Gamma_U|, \theta)}, \quad (11)$$

for a

$$|\Gamma_U| = \frac{V_{SW0}(|a_{1U}|, |\Gamma_U|)}{2|V_{SW1}(|a_{1U}|, |\Gamma_U|, \theta)|} \pm \sqrt{\left(\frac{V_{SW0}(|a_{1U}|, |\Gamma_U|)}{2|V_{SW1}(|a_{1U}|, |\Gamma_U|, \theta)|}\right)^2 - 1}. \quad (12)$$

As seen, (12) presents two possible solutions, but only one produces a magnitude of Γ_U lower than one (resulting in a passive load), i.e. a solution where the condition $|b_{1U}| < |a_{1U}|$ is satisfied. Note that the $V_{SW}(|a_{1U}|, |\Gamma_U|, \theta, \Phi)^2$ wave will go from being a constant dc value (when there is no reflected wave) to a sinusoidal wave that exactly touches zero

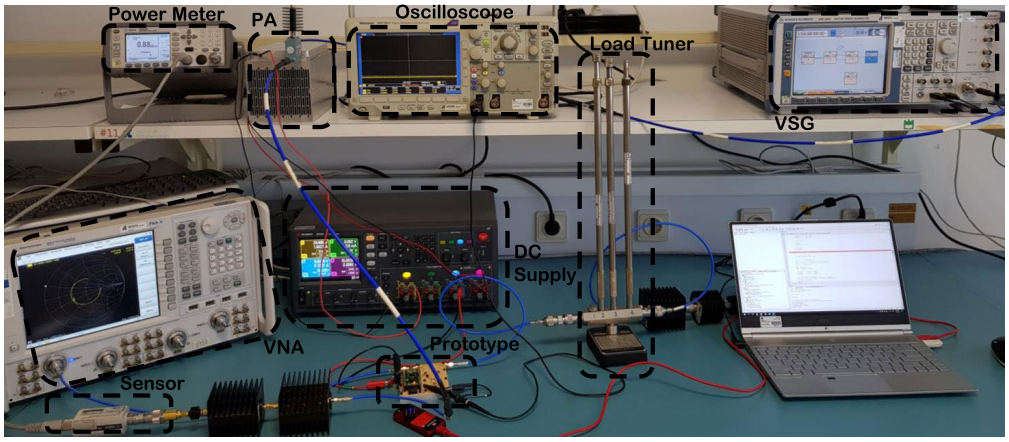

FIGURE 4. Photography of the measurement setup.

(when the magnitude of the reflected wave equals the one of the incident wave), meaning that

$$\frac{V_{SW0}(a_{1U}, |\Gamma_U|)}{2|V_{SW1}(a_{1U}, |\Gamma_U|, \theta)|} \geq 1 \tag{13}$$

is always valid. Therefore, the solution where $|\Gamma_U| < 1$, can only be obtained when one chooses the negative sign in (12). The mathematical proof for this is shown in Appendix B. Another issue worth to be noted in this formula is that $|V_{SW1}|$ tends to zero when there is no reflected wave at the load, making the ratio in (13) tend to infinity and $|\Gamma_U|$ asymptotically to zero. This is not a friendly implementation for a microprocessor. Therefore, in Appendix A, a formula better suited for implementation is also derived based on (2). Note that, due to this limitation, it is essential to correctly adjust the asymmetric attenuators' values to keep the synthesized wave in the same condition ($|b_{1U}| < |a_{1U}|$) for the whole VSWR measurement range. Note that the system can also measure the loads outside of this condition by selecting the positive sign solution of the quadratic equation in (12). However, it is required that the measurement condition is *a priori* known.

IV. CIRCUIT PROTOTYPE IMPLEMENTATION AND MEASUREMENT SETUP

In this section, the measurement setup (Fig. 4) and the developed circuit prototype are described and tested at 3.55 GHz. For validation purposes, we picked up a 3.55 GHz PA available at our laboratory that could be tested within the implemented impedance measurement solution which, for its current implementation has 1250 MHz of usable bandwidth (between 2.75 GHz and 4 GHz). Fig. 5 shows a photograph of the implemented prototype, based on the functional block diagram presented in Fig. 2, with the main components identified and some of their main specifications.

As previously explained, the bi-directional coupler is one of the most important elements of this circuit. For this purpose, a coupled line structure was specifically designed using a directivity enhancement technique based on the inclusion of a substrate layer above the coupled copper lines. With this overlaid dielectric layer, the air region's fringing

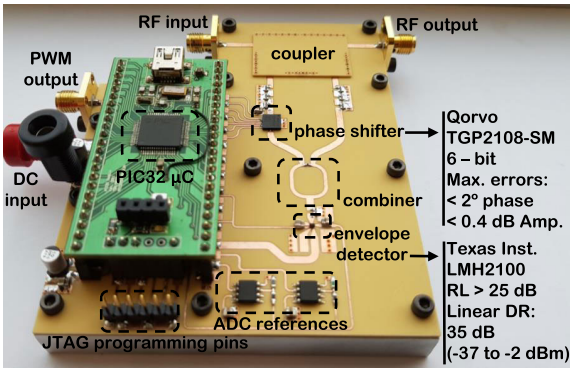

FIGURE 5. Photography of the implemented prototype and brief description of its main components characteristics.

field is reduced, equalizing the odd and even velocities of propagation, increasing the directivity [25]. The measured performance, expressed in terms of return loss, coupling, directivity, isolation, and insertion loss of the implemented coupler, is reported in Table 1 for 3.55 GHz.

TABLE 1. Measured performance of the overlay coupler at 3.55 GHz.

Coupling Factor (dB)	Insertion Loss (dB)	Unbalance (dB)
-27.450	0.087	0.020
Return Loss (dB)		**Directivity (dB)**
21.300 (main ports) / 26.400 (coupled ports)		25.000

The asymmetric attenuators, placed after the coupler, are set to accommodate the stationary wave in the detector's dynamic range for loads varying inside a 2.1 VSWR circle and a P_{in} variation of 16 dB, from 27 dBm to 43 dBm.

The stationary wave synthesized by the developed circuit is sampled by a 1 MHz 10 bit internal ADC of a Microchip PIC 32 microcontroller. Two voltage references are also included in the board to set the ADC input range to the output signal swing of the used envelope detector. The microcontroller is also used to perform the load computation and to generate the phase shifter control signals. The acquisition of one waveform takes around 10 μs per phase point with the presented hardware. The system's losses are mainly dependent on the

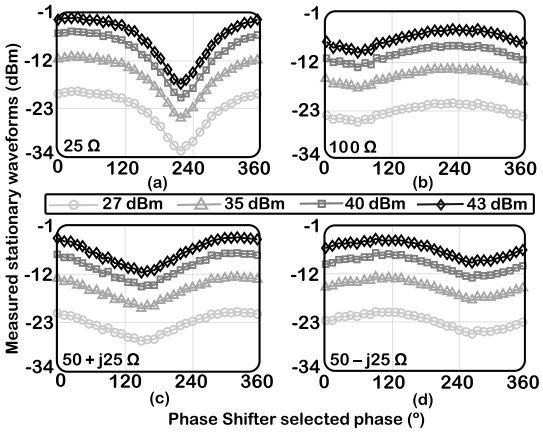

FIGURE 6. Measured standing wave in dBm for four loads and four P_{in} levels, using 32 phase steps that correspond to 11.2 ° of phase resolution.

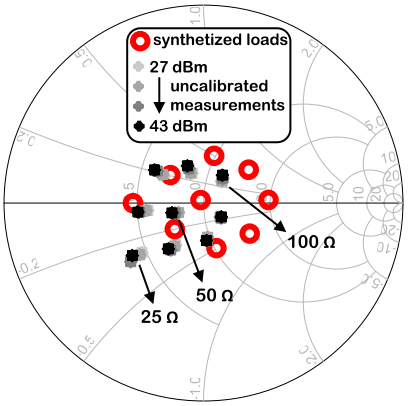

FIGURE 7. Synthesized and computed (uncalibrated) impedances for various incident power levels, using a 11.2 ° phase step.

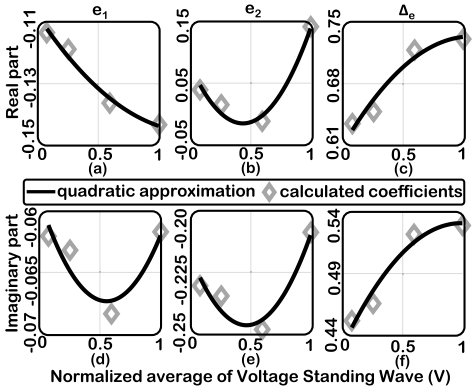

FIGURE 8. SOL calibration coefficients variation with average incident power level and its quadratic approximation.

coupler. In the VSWR circle of interest they are always lower than 0.1 dB, which, as an example, is equivalent to a 1.5 % efficiency degradation in a PA with a 65 % nominal efficiency and 40 dBm of maximum output power. The dc power is 350 mW, which also reduces the efficiency by about 1.5 % for the previously described PA.

Figure 4 shows the setup used to test the prototype. A commercial PA was used to scale the RF signal generated by the Vector Signal Generator (VSG) to the necessary input power level. At the output, a manual load tuner and some high power 50 Ω attenuators are used. Finally, a low-frequency oscilloscope was used to confirm the values read by the microcontroller ADC. The power calibration is performed using a power meter and the load calibration with a VNA. The reference plane is the input port of the impedance measurement circuit for both calibrations.

The impedance measurement system was tested with CW excitation for various loads and several P_{in} levels. For the highest output power level, the used PA is operating close to its maximum output power, yet the delivered power at harmonic frequencies is negligible.

V. STATIONARY WAVE MEASUREMENTS AND IMPEDANCE CALCULATIONS

Using the implemented circuit prototype and the assembled measurement setup, four different loads (25 Ω, 100 Ω, 50+j25 Ω and 50-j25 Ω) were adjusted using the manual load tuner (verified with calibrated VNA measurements properly referenced to the circuit's plane) and, for each one, four input power levels (27 dBm, 35 dBm, 40 dBm and 43 dBm) were used to synthesize the stationary wave. The measurements are shown at Fig. 6 for an 11.2° phase resolution step.

It can be observed that the stationary wave amplitude is higher for 25 Ω than it is for 100 Ω. This happens due to the finite directivity of the coupler, which slightly modifies the reflected wave sample. The undesired coupling between the coupler ports 4 and 1 has a fixed phase delay, which, in this case, reduces the reflected wave amplitude for the 100 Ω load and increases it for 25 Ω. However, this effect is linear and can be corrected using an SOL calibration.

So, Fig. 6 a) corresponds to the load with highest stationary wave amplitude, which is the worst-case in terms of detector's input dynamic range, and so, it is used to evaluate the waveform conditioning to the optimal levels. From Fig. 6, it is concluded that from 27 dBm to 43 dBm, the minimum and maximum values are, respectively, −33 dBm and −2 dBm that are within the envelope detector's optimal range. A consistent phase variation of the waveforms is also already perceptible, as expected.

Figure 7 shows the loads computed using (11) and (12) from the approximated model using 32 measured points. These loads do not match the synthesized ones due to the coupler non-idealities and branch asymmetries on the built circuit, e.g., the introduced attenuation. For some loads, there are also small differences for different P_{in} levels, which indicate some non-linearity.

Afterwards, a SOL calibration [26] was used to correct the linear measurement errors. The calibration error terms have been obtained using a least-squares regression for more than three measured loads. This way, better results are obtained for the whole load range since, for an overdetermined system, the sensitivity to the calibration loads measurement

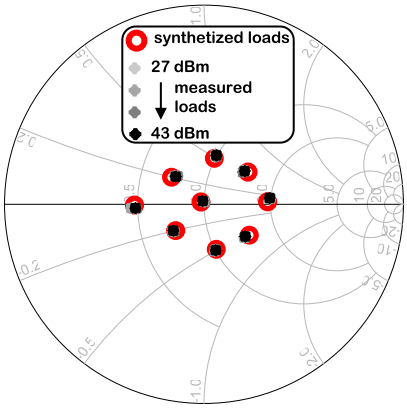

FIGURE 9. Synthesized and calibrated computed loads for various incident power levels, using a 11.2 ° phase step.

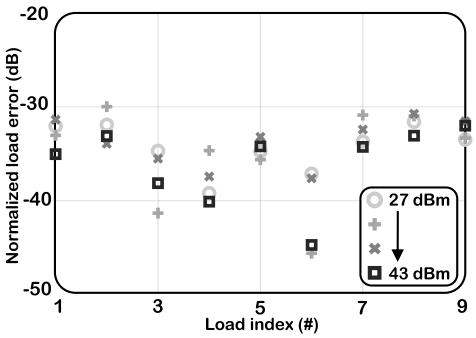

FIGURE 10. Measurement error normalized to the target impedance, for loads computed from measurement with a 11.2 ° of phase step.

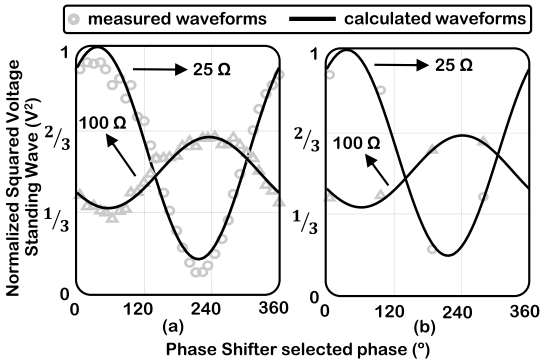

FIGURE 11. Measured and modelled voltage standing wave for 25 and 100 Ω loads, using (a) 32 and (b) 4 phase shifter states.

TABLE 2. Numeric values obtained for 25 and 100 Ω loads, using 32 and 4 measured phase shifter points for each load.

	100 Ω 32 Pts.	100 Ω 4 Pts.	25 Ω 32 Pts.	25 Ω 4 Pts.
$\max(V_{SW}{}^2)(V^2)$	0.63	0.65	0.99	1.00
$\min(V_{SW}{}^2)(V^2)$	0.34	0.36	0.14	0.16
$\arg\max(V_{SW}{}^2)()$ $\Phi \in [0, 360[$	233.1	239.4	35.3	35.3
$V_{SW0}(V^2)$	0.49	0.50	0.56	0.58
$\lvert V_{SW1}\rvert(V^2)$	0.07	0.07	0.21	0.21
$\angle V_{SW1}()$	124.4	118.6	-36.4	-35.7
$\lvert\boldsymbol{\Gamma_U}\rvert$	0.150	0.149	0.453	0.429
$\angle\boldsymbol{\Gamma_U}()$	55.6	61.4	-143.6	-144.3
$\lvert\boldsymbol{\Gamma}\rvert$ — SOL cal	0.337	0.334	0.326	0.326
$\angle\boldsymbol{\Gamma}()$ — SOL cal	4.3	4.8	-178.0	-176.7

Note that $V_{SW}{}^2$, V_{SW0} and $\lvert V_{SW1}\rvert$ are normalized to the their maximum for better comparison among different loads.

accuracy is reduced. This calibration was also independently performed for various P_{in} levels to further check on the previously detected nonlinearities. The calculated coefficients are shown in Fig. 8 for different average P_{in} levels, using gray diamonds. The plots from a) to c) represent the real part of the error coefficients (e_1, e_2 and Δe). In Fig. 8 d) to f) are plotted the imaginary parts of the same coefficients. Their behavior is non-linear, which was already expected from the analysis of the computed loads. Thus, to achieve better results for every P_{in} level, they are approximated by quadratic functions ($ax^2 + bx + c$), which are shown by the solid black lines in Fig. 8.

Figure 9 shows the calibrated loads with an SOL algorithm using the quadratic approximation of the calculated coefficients. As it is shown, they correspond to the synthesized loads for all the input power levels, which validates both the measurement technique and the quadratic approximation used for the SOL coefficients (that corrects the non-linearity previously detected).

The normalized error between the measured and synthesized loads was calculated in dB using:

$$Err = 20\log_{10}\left(\frac{Z_{meas} - Z_{target}}{Z_{meas} + Z^*_{target}}\right), \tag{14}$$

and the result is shown in Fig. 10. As it can be seen, the error is below -30 dB for all the loads and in the entire range of input power levels (27, 35, 40, and 43 dBm), which validates the utility of the presented system and computation algorithm.

After sampling the waveforms, the computation time necessary to approximate the previously presented model to the measurements is around 140 μs per phase point. The required time to compute and calibrate the load is around 500 μs. So, if 32 measured points (11.2° phase step) are used to obtain the load, the time necessary to measure the data, fit the model to the measurements, compute and calibrate the load is almost 6 ms. This leads to a maximum measurement rate of around 160 Hz, which is believed to be slow for some of the proposed applications. Thus, trying to improve the system speed, the load was computed using higher phase steps.

Going back to the number of measurements needed to perform the impedance calculation, Fig. 11 presents the comparison between the measured data and the model predictions for two distinct loads, 25 Ω and 100 Ω. In Fig. 11 a), the model is extracted with 32 measured points, while in Fig. 11 b) it is extracted with four measured points. From this comparison, it can be concluded that the model provides a good fitting to the measurements, even for a low number of measured points, which suggests a correct load prediction. Nonetheless, using more measurements makes the load computation less sensitive to measurement imprecision, ADC quantization errors, and phase/amplitude errors of the phase shifter, as is evident for the case of 100 Ω (Fig. 11 a)). This happens due

TABLE 3. Summary of the comparison with other works.

	Operating Frequency	Output Power	Implemented Technique	Insertion loss (dc power)[1]	Accuracy*	Measurement Time	Measurement Region	Design Complexity
[16]	0.90 GHz 1.80 GHz	0 - 33 dBm	Output coupler (VNA like)	0.36 dB (165 mW)	High	18.46 ms	9.0:1	High
[18]	0.81 GHz	15 - 20 dBm	Sampled Line (Stationary wave based)	0.40 dB (N/A)	Low	N/A	9.0:1	Low
[19]	10.00 GHz	15 dBm	Sampled Line (Stationary wave based)	0.50 dB (N/A)	Low	N/A	4.0:1	Low
[20]	3.00 GHz	6 - 15 dBm	OMN integrated detection (Reflectometry based)	0.30 dB (N/A)	Moderate/ Low[2]	N/A	9.0:1	Low
[10]	1.95 GHz	24 - 28 dBm	Output coupler (Waves comparison)	0.25 dB (N/A)	Low[3] (8 regions)	N/A	2.5:1	High
[23]	1.95 GHz	10 - 30 dBm	Output coupler (Mixer based)	N/A	Moderate	N/A	6.0:1	High
This Work	3.55 GHz	27 - 43 dBm	Output coupler (Stationary wave based)	0.09 dB (330 mW)	High	<1.00 ms	2.1:1	Low

*Following the definition in (14), the accuracy is considered low, moderate or high for an worst-case error at around -15 dB, -20 dB or -30 dB, respectively.
[1]The dc power is the consumed power by the acquisition and processing circuit. Normally, it depends on the measurement time of the system, which is an important dynamic characteristic for further implementation of these techniques.
[2]In this work the impedance measurement accuracy is enough for a 6 dBm power level, but it is much degraded for 15 dBm.
[3]In this work the impedance is measured by comparison, so the measurement region is divided in 8 areas. To further reduce the size of these areas the authors would need to replicate some of the used hardware blocks, making the system even more complex.

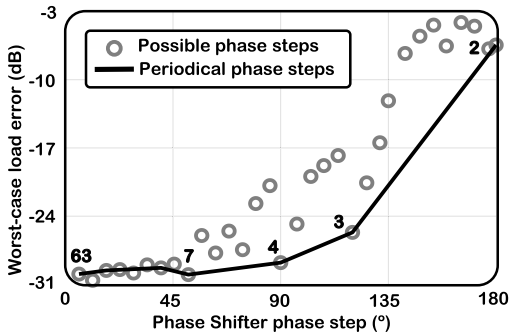

FIGURE 12. Worst-case measurement error for the various possible phase shifter steps, in gray. Available periodical phase steps and the correspondent number of measured phase points, in black.

to the proposed method using the Fourier transform, which averages the measured points in the integration, resulting in a suppression of the mentioned errors when more phase values (Φ) are considered.

Table 2 shows the numeric values of the variables in the "squared standing wave model" and computed reflection coefficient for two loads (25 Ω and 100 Ω), considering 32 and 4 measured points for each one.

Now, in Fig. 12, it is shown the load measurement worst-case error (over the load and input power ranges) for various phase steps (Φ). For loads computed from measurements using seven or more points, the error is around −30 dB, which is a reasonable estimate of the actual load. If fewer points are used, it is essential to choose a phase step (from the phase shifter available ones) that is an exact sub-multiple of 360° to keep the measurements periodical. If this condition is satisfied, the Fourier-based model that was developed is still a good approximation of the wave, and, consequently, a reasonable estimate of the actual load for phase steps of 90° and 120°, which correspond to 4 and 3 measured points, respectively, is obtained. Using a phase step of 90°, the error is −28.8 dB, and the measurement time is reduced to below 1 ms. For a 120° step, the error is −25.7 dB, and the measurement time is 800 μs, and so, a compromise can be made between accuracy and measurement speed.

Table 3 shows a comparison between the summarized performance of this and different previous works. Note that this comparison table only includes works in which both the amplitude and phase of the reflection coefficient are measured. As expected, the presented work results in a low complexity design with high accuracy for a restricted region of the Smith chart, which is practical for use in power systems under load varying scenarios.

VI. CONCLUSION

This work presented an original technique to compute the reflection coefficient from low phase resolution stationary wave measurements and a prototype capable of applying the technique. The developed method is based on the Fourier series, and so it is robust to measurement imprecision and can compute the impedance from a reduced number of measured points. The implemented circuit prototype can measure the load reflection coefficient as is done in a slotted line but eliminates the need for moving mechanical parts or multiple envelope detectors placed along a single transmission line. It is based on a bi-directional coupler and a single variable phase shifter, which changes the delay between the incident and reflected waves to synthesize the stationary wave.

The compact impedance measurement system was tested for loads varying inside a 2.1 VSWR circle and for different input power levels between 27 and 43 dBm. It revealed capable of computing the impedance in less than 1 ms with an error below −28 dB and of reducing the error to below −30 dB when higher precision is desired. Thus, this system is appropriate for usage in RF power systems with reduced impact in their efficiency, due to its low insertion losses. Furthermore, beyond its applicability herein illustrated for CW

signals, it can also be applied to modulated signal excitations, as was previously shown in [13].

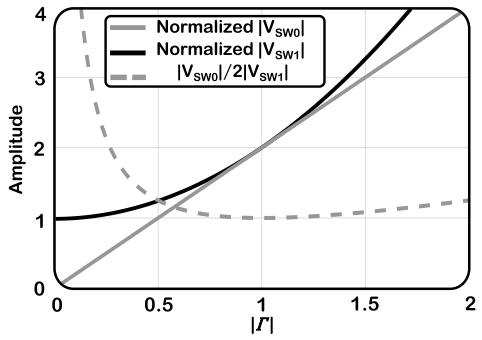

FIGURE 13. Magnitudes of the dc component, V_{SW0}, and the double of the fundamental component, $2V_{SW1}$, of the $V_{SW}{}^2$ along with the ratio between them, $\frac{V_{SW0}}{2|V_{SW1}|}$.

APPENDIX A

This appendix is dedicated to derive a $|\Gamma_U|$ formula more friendly for microprocessor implementations. The formula of the quadratic solution (12) relies on the division of V_{SW0} by the fundamental component, V_{SW1}. As noted, this fundamental component tends to zero when there is no reflected wave, which may be problematic for implementation.

knowing that the maximum of the stationary wave is given by

$$\sqrt{V_{SW0} + 2|V_{SW1}|}, \tag{15}$$

and the minimum by

$$\sqrt{V_{SW0} - 2|V_{SW1}|}, \tag{16}$$

$|\Gamma_U|$ can be computed, using (2), from

$$|\Gamma_U| = \frac{\sqrt{\frac{V_{SW0}+2|V_{SW1}|}{V_{SW0}-2|V_{SW1}|}} - 1}{\sqrt{\frac{V_{SW0}+2|V_{SW1}|}{V_{SW0}-2|V_{SW1}|}} + 1}, \tag{17}$$

which can be further developed into

$$|\Gamma_U| = \frac{\sqrt{V_{SW0} + 2|V_{SW1}|} - \sqrt{V_{SW0} - 2|V_{SW1}|}}{\sqrt{V_{SW0} + 2|V_{SW1}|} + \sqrt{V_{SW0} - 2|V_{SW1}|}}. \tag{18}$$

In this last formula the denominator does not tend to zero in any case, making it more friendly for evaluation in a computer.

APPENDIX B

This appendix is devoted to demonstrate that the solution where $|\Gamma_U| < 1$, can only be obtained when choosing the negative sign in (12). First, note that the double of the magnitude of the fundamental component, $2V_{SW1}$, is always lower than the dc component, V_{SW0}. This can be seen in Fig. 13, where these magnitudes are plotted versus the magnitude of the reflection coefficient. We can thus conclude that the ratio in (13) is always higher or equal to one, as shown in Fig. 13, which guarantees the existence of a real solution.

Now it is shown that the choice of the negative sign in (12) always leads to a passive load, i.e. the measured reflection coefficient will always have a magnitude lower than one. This can be proved by noting that (suppressing V_{SW0} and V_{SW1} arguments for simplicity),

$$\left(\frac{V_{SW0}}{2|V_{SW1}|}\right)^2 - 1 \geq \left(\frac{V_{SW0}}{2|V_{SW1}|} - 1\right)^2 \Leftrightarrow \tag{19a}$$

$$\sqrt{\left(\frac{V_{SW0}}{2|V_{SW1}|}\right)^2 - 1} \geq \frac{V_{SW0}}{2|V_{SW1}|} - 1 \Leftrightarrow \tag{19b}$$

$$1 \geq \frac{V_{SW0}}{2|V_{SW1}|} - \sqrt{\left(\frac{V_{SW0}}{2|V_{SW1}|}\right)^2 - 1} \Leftrightarrow \tag{19c}$$

$$|\Gamma_U| \leq 1. \tag{19d}$$

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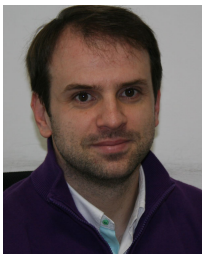

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Appendix C

Supply Voltage Modulation on Single-Ended PAs

Optimal Supply Voltage for PA Output Power Correction under Load Varying Scenarios

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Optimal Supply Voltage for PA Output Power Correction under Load Varying Scenarios

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***Abstract*— Power Amplifiers (PAs) are usually designed for fixed load terminations, which implies that their performance can be severely degraded for varying load operation. This paper presents a load dependent supply voltage (V_{DD}) adaptation that can be used to correct PAs' output power in these non-optimal scenarios. The calculated V_{DD} values are verified in simulation and laboratory measurements for a 3.55 GHz PA based on a Cree CGH40010F Gallium Nitride (GaN) device. To dynamically vary the V_{DD}, a GaN buck converter, based on the commercial EPC 9067 Demo Board, was used. In addition, to preserve the compression level, the excitation amplitude is accordingly adjusted. The measured output power of the PA was corrected from 37.0 dBm to 39.9 dBm - a 2.9 dB improvement for the worst case loads inside a 2.1 Voltage Standing Wave Ratio (VSWR) circle.**

***Keywords*— load insensitivity, power amplifiers, V_{DD} modulation.**

I. Introduction

Power Amplifiers (PAs) operating with varying load conditions appear in various applications and due to different causes. In mobile devices, the load impedance presented to the Radio Frequency (RF) PA can change due to objects on the proximity of the antenna or the hand effect [1]. In Fifth Generation (5G) massive Multiple-Input Multiple-Output (MIMO) Base Stations (BSs) with beamforming capabilities, the input impedance of different antenna elements can also change due to their high mutual coupling level [2]. Various techniques have been studied to improve the PA operation under such scenarios. In 5G massive MIMO antenna arrays, techniques that aim at reducing the mutual coupling at the antenna level are extensively described in the literature. However, they do not completely solve the problem and, as expected, they can only correct it in case of impedance variation due to mutual coupling, since they do not solve the problem but eliminate its source [3].

Some complex PA architectures, for instance, balanced and Doherty PAs, have also been used to reduce load sensitivity in various applications. Balanced amplifiers are based on two transistors operating in quadrature and on two quadrature couplers. Balanced PAs can deliver an almost constant output power under mismatch conditions but, unfortunately, at the expense of sending to a dummy load the power not delivered to the changing load, this way reducing the amplifier efficiency [4]. Digital Doherty PAs (i.e., Doherty PAs of two independent analog inputs in which the signal separation is performed at the digital level) can be driven with the appropriate signals to reduce the load variation seen by the carrier PA. In this case, some power of the peaking amplifier will be used to correct the load and this will degrade the back-off efficiency of the PA. Moreover, this method is only able to compensate variations towards loads lower than the nominal value, which is not always the case [5].

Solutions implemented at the Output Matching Network (OMN) have also been tested. Transmission Line Resistance Compression Networks (TLRCNs) are very promising, but they require at least two loads varying synchronously [6]. Various Tunable Matching Networks (TMNs), using varactors, switched capacitor banks, or switched stubs have also been implemented. However, they still suffer from the extra losses added by these additional components [7].

This work presents a technique that uses supply voltage (V_{DD}) variation to compensate the output power of PAs operating under varying loading conditions. This technique can be physically implemented with a supply modulator made with a fast and efficient Gallium Nitride (GaN) based switched DC-DC converter, imposing a very small overall efficiency degradation, and making its architecture similar to Envelope Tracking (ET) applications, but of easier implementation. While in ET PAs the V_{DD} must track the RF envelope, requiring fast supply modulators that considerably reduce the total efficiency [8], in our case, the V_{DD} should track the movement of users, or obstacles near antennas, which is usually much slower than the RF envelope signals.

The paper is organized as follows: Section II derives the theoretical load dependent V_{DD} values that correct the amplifier's output power; Section III shows the design and simulation of a Class B GaN PA using the obtained V_{DD} values; Section IV presents the practical validation of the proposed technique; Section V describes the most important conclusions of this work.

II. Supply voltage Variation Theory

Our objective is to make a load insensitive PA from an output power perspective, while maintaining high efficiency operation. So, first of all, we have to calculate the output power dependency with the V_{DD} and load terminations. Then, for each load (Z_L), we can determine which drain voltage has to be applied so that the desired output power is obtained.

In order to achieve a constant output power, we cannot design the PA for the maximum power load. This happens because when the load is shifted towards a lower value,

increasing the V_{DD} would not compensate the output power, since the transistor would become current limited. Having this in mind, and also ensuring high efficiency operation, we design the PA for the maximum efficiency load ($R_{L_{eff}}$). For this load, the output power delivered by the PA will be $P_{out_{eff}}$ and after applying V_{DD} compensation the output power will be constant and equal to this value.

Going back to PA fundamentals, we start by considering a simplified circuit for the output of the amplifier, which includes a piecewise linear current source model with R_{ON}, as shown in Fig. 1 a) and b).

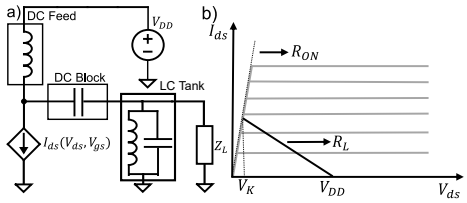

Fig. 1. Simplified output circuit for the theoretical analysis (a); Considered piecewise current source model (b).

The first step is to calculate the output power of the PA. The expression is shown in (1), for a fundamental current component, I_1, and load Z_L with real part, R_L.

$$P_{out} = \frac{1}{2} R_L |I_1|^2 \tag{1}$$

The fundamental component of the drain current is given by $\left(\frac{I_P}{2}\right)$, for class B operation and a peak current, I_P. The latter is defined by the selected load and the maximum voltage excursion imposed by the triode region as described in (2), where V_K is the knee voltage of the I/V curves.

$$I_P = 2\frac{V_{DD} - V_K}{|Z_L|} \tag{2}$$

This expression can be further developed by including the widely used constant R_{ON} approximation model [9]. The peak current is then given by (3) and the corresponding output power is given in (4).

$$I_P = \frac{2V_{DD}}{|Z_L| + 2R_{ON}} \tag{3}$$

$$P_{out} = \frac{1}{2}\frac{R_L}{(|Z_L| + 2R_{ON})^2} {V_{DD}}^2 \tag{4}$$

The output power for the maximum efficiency load, which is real, is given by (5), for the design supply voltage of V_{DD_0}.

$$P_{out_{eff}} = \frac{1}{2}\frac{R_{L_{eff}}}{(R_{L_{eff}} + 2R_{ON})^2} {V_{DD_0}}^2 \tag{5}$$

Finally, the expression (6) is obtained by solving (4) in order to V_{DD}.

$$V_{DD}(Z_L) = \sqrt{\frac{R_{L_{eff}} {V_{DD_0}}^2 (|Z_L| + 2R_{ON})}{R_L (R_{L_{eff}} + 2R_{ON})^2}} \tag{6}$$

We will now consider that the amplifier suffered a variation of the load real part (due to mutual coupling between antenna elements or any other case) so that it now sees: (i) a higher R_L or (ii) a lower R_L both compared with the one considered in the design stage ($R_{L_{eff}}$). The input power level is increased for operation under lower loads, and decreased for higher loads, in order to maintain the device on the onset of saturation. (i) For higher loads, the fundamental current will be lower, as shown in Fig. 2 a). Thus, in this situation, the V_{DD} given by (6) will be higher in order to restore the power (raising the voltage excursion). (ii) For lower loads, the maximum current swing becomes higher, increasing the maximum output power. However, the efficiency for the nominal power is reduced, as shown by the non-optimal load line of Fig. 2 b). So, in this case, the V_{DD} calculated using (6) will be lower in order to increase the efficiency for the designed output power.

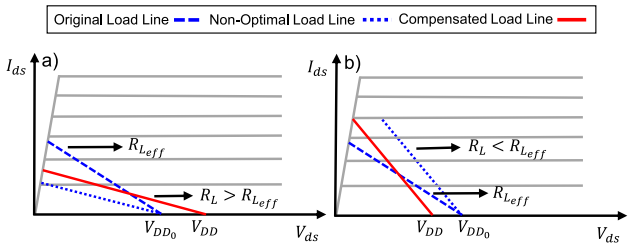

Fig. 2. Correction of variations towards higher real part loads (a); Correction of variations towards lower real part loads (b).

After this qualitative explanation using a simplified circuit, we will now solve the expression (6) for a real transistor. To determine $R_{L_{eff}}$, we can use the expression deduced in [9] for a known quiescent current, I_{dq}. A possible class B definition uses a V_{GS} bias (and therefore I_{dq}) that corresponds to the zero of the I_{DS} third-order derivative w.r.t. V_{GS}, $\left(\frac{d^3 I_{DS}}{dV_{GS}^3}\right)$. Then, R_{ON} can be approximated using the I/V characteristics of the device, as shown in Fig. 3 a) for the device adopted in this work (Cree CGH40010F). In this case, the efficiency load is equal to 30 Ω and the R_{ON} to 1 Ω. Since, we observed that the V_{DD} model (6) is not very sensitive to R_{ON}, a DC estimate is enough to compute it. The V_{DD} was calculated for loads within a 2.1 Voltage Standing Wave Ratio (VSWR) circle, as shown in Fig. 3 b). This load variation corresponds to typical cases in active phased arrays [10].

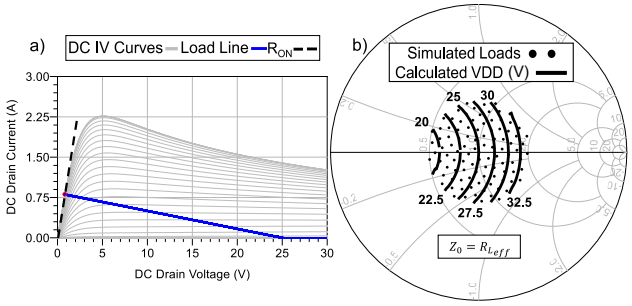

Fig. 3. DC I/V characteristic of the used device, maximum efficiency load line, and calculated R_{ON} (a); Calculated V_{DD} values for this device (b).

III. PA Design and Simulation

In order to test the developed theory, a class B PA was designed. The PA operates at 3.55 GHz and the above referred GaN device was used. The OMN was designed to convert 50 Ω to the maximum efficiency load and to present short circuit harmonic terminations at the current source plane, ensuring class B operation at this frequency.

The simulated output power and drain efficiency of the PA at the 1 dB gain compression point are shown in Fig. 4 a) respectively in blue and red. The simulations were made for 100 different loads, distributed inside a 2.1 VSWR circle, and the input power was adjusted to maintain the compression level at 1 dB for all these loads. The maximum output power is 41.4 dBm and the contours' step is 1 dB. The maximum efficiency is 64.7 % with a contours' step of 5 %.

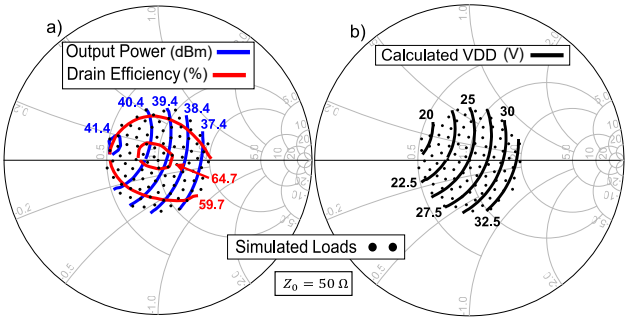

Fig. 4. Simulated load pull of the designed PA (a); Calculated V_{DD} at the load plane (b).

The calculated V_{DD} values plotted at the load plane of the amplifier are shown in Fig. 4 b). To calculate these values, the expression in (7) was used to obtain the Γ_{int} at the current source plane of the device, for each Γ_L calculated from the output load. Then, the expression in (6) was used for a Z_L calculated from Γ_{int}. The S-parameters used in (7) correspond to the network between the current source and load planes. These parameters were extracted by optimization to match the load plane output power contours with the current source plane ones, which are aligned with the real axis.

$$\Gamma_{int} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{7}$$

The output power obtained for each tested load is presented in Fig. 5, using a fixed V_{DD} of 25 V and with the V_{DD} shown in Fig. 4 b), in blue circles and red triangles, respectively.

The output power variation without V_{DD} compensation is 4.6 dB with a minimum value of 36.9 dBm. Using the calculated V_{DD}, the variation is reduced to 0.7 dB and the minimum value increases to 39.3 dBm, which corresponds to an increase of 2.4 dB.

The drain efficiency of the amplifier with and without compensation is shown in Fig. 6, using the same colors and symbols of Fig. 5. The variation, maximum and minimum values are identical before and after compensation. On average, the efficiency across the loads was kept at 61.9 %.

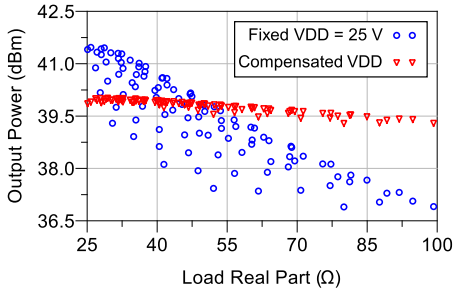

Fig. 5. 1dB gain compression point simulated output power of the designed PA for fixed and calculated supply voltages.

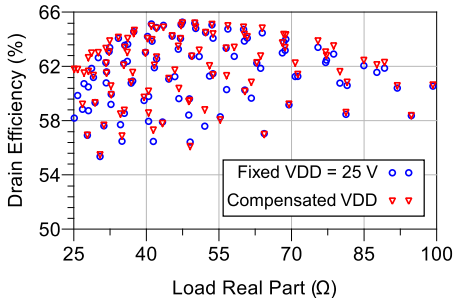

Fig. 6. 1dB gain compression point simulated drain efficiency of the designed PA for fixed and calculated supply voltages.

IV. Experimental Validation

The designed PA was fabricated and assembled, and is shown Fig. 7 (a). In order to validate the simulated results, a buck converter was added to the board. The EPC 9067 GaN demo board was used for this purpose. It uses two EPC8009 devices, in switched operation, and the switching frequency was set to 1 MHz.

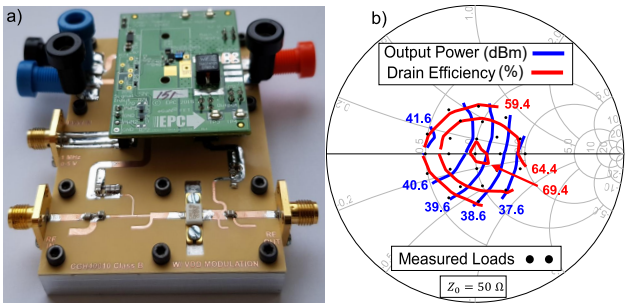

Fig. 7. Photograph of the implemented Class B PA with the used EPC GaN buck converter (a); Measured load pull for a fixed V_{DD} of 25 V (b).

The amplifier was measured without the buck converter, for a 25 V fixed drain voltage. The obtained load pull contours, measured at the 1 dB gain compression point, are presented in Fig. 7 (b). The maximum output power is 41.6 dBm and the contours are shown with a step of 1 dB. The maximum efficiency is 69.4 % and the contours' step is 5 %. These contours have been compared with the simulated ones in order to verify their alignment. This comparison revealed a small phase rotation between the measured and simulated data. This small error corresponds to an offset in the simulation reference

plane, and was corrected using a small (ideal) offset line. Using these corrected S-parameters in (7), the V_{DD} values for the laboratory measurements were calculated.

The measured output power for the 25 test loads synthesized in the laboratory, using a load tuner, is shown in Fig. 8. The results for a fixed V_{DD} are plotted using blue circles, showing a variation of 4.7 dB and a minimum value of 37.0 dBm. Using the calculated V_{DD} for compensation, the obtained results are plotted using red triangles, showing a variation of 0.5 dB and a minimum value of 39.9 dBm, wich corresponds to a worst case value increase of 2.9 dB.

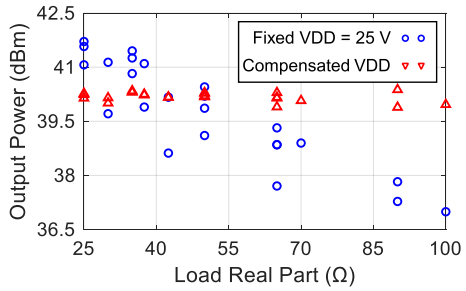

Fig. 8. 1dB gain compression point measured output power of the implemented PA for fixed and calculated supply voltages.

The drain efficiency corresponding to the output power measurements of Fig. 8 is shown in Fig. 9. The average efficiency without V_{DD} compensation is 64.7 % with a variation of 12.9 %. With V_{DD} compensation the variation is the same for an average of 63.0 %, which is 1.7 % lower. Note that this efficiency includes the power dissipated in the buck converter only for the case of variable V_{DD}.

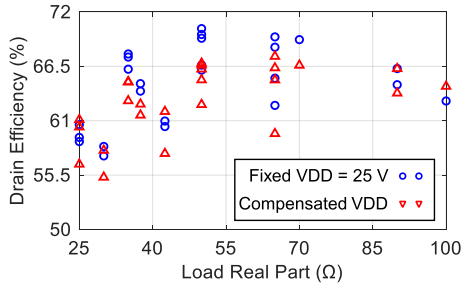

Fig. 9. 1dB gain compression point measured drain efficiency of the implemented PA for fixed and calculated supply voltages.

The measured results validate the theory presented in this paper, showing a compensation of the PA output power and only slightly reducing its average efficiency. This reduction is attributed to the losses in the buck converter, which increase with the switching frequency and with the voltage (duty-cycle) reduction. The 1 MHz switching frequency is believed to be enough to vary the V_{DD} and compensate the load variation due to moving objects or beamforming on MIMO antenna arrays, even for extreme cases like High Speed Trains (HSTs) [11].

V. Conclusion

This work presented a theory-based V_{DD} variation to compensate the output power capability of PAs operating under varying loading scenarios. The calculated values have been validated in simulation and laboratory measurements for a 3.55 GHz GaN class B PA. The output power variation, at the 1 dB gain compression point, was reduced by 4.2 dB. Moreover, the power capability of the PA was improved by 2.9 dB, for the worst case loads. The cost is the added complexity and a slight (1.7 % for 1 MHz DC-DC switching frequency) reduction of average drain efficiency. The compensation was effective for any load within a 2.1 VSWR circle. For the chosen 1 MHz switching frequency, the reduction on total efficiency is higher than for lower switching frequencies. However, it was selected to permit dynamic control of V_{DD} at the time rate required for future implementations on the proposed applications.

Acknowledgment

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Appendix D

Supply Voltage Modulation on Single-Ended PAs - Extended

Dynamic Supply Voltage Control for PA Output Power Correction Under Variable Loading Scenarios

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Dynamic Supply Voltage Control for PA Output Power Correction Under Variable Loading Scenarios

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***Abstract*— This article presents an automatic system that is able to dynamically restore the output power capability of a power amplifier (PA) under variable loading scenarios. This is accomplished by dynamically adapting the supply voltage, V_{DD}, of the PA according to the developed theoretical model. To dynamically vary V_{DD}, a GaN dc–dc converter, based on the commercial EPC 9067 Demo Board, was used. The load is measured using an impedance meter, which is based on the slotted line principle and was specifically designed for low insertion loss. This impedance meter also generates a load-dependent pulsewidth modulated signal that controls the dc–dc converter switching, regulating V_{DD}. The prototype was designed for 3.55 GHz and tested with CW and modulated signal excitations, being able to compensate the output power degradation under variable loading conditions inside a 2.1 voltage standing wave ratio circle. For a constant gain compression level, the average efficiency degradation over the tested range of impedances is less than 5%, and the average power improvement is 0.7 dB. The worst case measured output power of the PA is compensated from 37.0 to 39.9 dBm, which corresponds to a 2.9 dB improvement. Using a modulated signal excitation, the peak envelope power, which is compressed by almost 3 dB without V_{DD} compensation, is restored, and the average output power is improved by 0.6 dB. The system can track the load and adjust V_{DD} with a worst case step-up delay of 25 ms.**

***Index Terms*— Load insensitivity, power amplifiers (PAs), V_{DD} modulation.**

I. Introduction

POWER amplifiers (PAs) are usually designed for a fixed output load, which implies that their performance can be severely degraded when operating with variable loading conditions, namely, in terms of conversion efficiency, linearity, output power capability, and even reliability. This load variation can happen due to the change of the load physical proprieties, in applications such as microwave cooking [1], plasma heating in, e.g., plasma-enhanced chemical vapor deposition (PECVD) processes [2], or cavities charging on particle accelerators [3]. In mobile communication devices, the load impedance presented to the radio frequency (RF) PA can also change due to moving objects in the proximity of the antenna, e.g., the hand effect [4], caused by the proximity between the hand and the antenna while holding a mobile phone. In fifth-generation (5G) massive multiple-input multiple-output (MIMO) base stations (BSs) with beamforming capabilities, the input impedance of different antenna elements also changes due to their mutual coupling [5].

Various techniques have been studied to improve PA's performance under variable loading operations. Circulators have been used for many years, being able to reduce the load variation seen by the PA by dissipating the reflected power in a dummy load, but do not maintain the delivered power [6]. In 5G massive MIMO antenna arrays, techniques that aim at reducing the mutual coupling at the antenna level can reduce the load variation seen by the PA, but they are dedicated only to MIMO applications [7].

Some complex PA architectures, for instance, balanced, Doherty, and outphasing PAs, have also been used to reduce load sensitivity in various applications [8]–[10]. Balanced amplifiers are based on two transistors operating in quadrature and on two quadrature couplers. They can deliver an almost constant output power under mismatch conditions at the expense of power dissipation in a dummy load when mismatched, as the combination becomes unbalanced, reducing the amplifier efficiency [8]. Digital Doherty PAs (i.e., Doherty PAs of two independent inputs in which the signal separation is performed at the digital level) can be driven with the appropriate signals to reduce the load variation seen by the carrier PA. In this case, some power of the peaking amplifier will be used to correct the carrier's load, but this will degrade the back-off efficiency of the PA and reduce its maximum delivered power. Moreover, this method is only able to compensate for variations toward loads lower than the nominal value, which is not

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always the case [9]. Sánchez-Pérez *et al.* [10] designed a tunable Chireix-type combiner to reduce the efficiency and output power variation of the amplifier under mismatch. However, the implemented combiner is tuned by manually changing the used components, and the extra losses added by tunable components are not measured.

Solutions implemented at the PA's output matching network (OMN) have also been tested. Transmission line resistance compression networks (TLRCNs) are very promising, but they require at least two loads varying synchronously [11]. Various tunable matching networks (TMNs), using varactors [12], [13], switched capacitor banks [14], or switched variable-length stubs [15] to perform a dynamic load matching, have also been implemented. This approach is very versatile and has a good tunability range but suffers from the extra losses added by the additional tunable components. These extra losses can be compensated by the increased efficiency for operation under the adjusted optimal load. However, note that just 0.3 dB of extra losses already cause a constant efficiency degradation of around 5% (for a 70% nominal efficiency), even when the amplifier operates under the nominal load. Thus, this technique is challenging in terms of losses, and it is only effective for a large mismatch, where the amplifier efficiency is degraded by more than 5%.

Load-dependent bias voltages can also improve PA performance under variable loading scenarios [9], [16], [17]. This can be done by controlling only the drain, or both the drain and gate, dc voltages to improve the performance of the PA for some loads. This solution becomes more attractive as the efficiency of dc–dc converters become higher. It is also implementable without adding extra components or added complexity in the RF path of the designed PAs.

This work is an extended version of [16] in which a theory-based load-dependent supply voltage, V_{DD}, variation that compensates the output power capability of PAs operating under variable loading conditions is developed. In [16], a PA was also developed under the introduced theory, and it was shown that the V_{DD} variation is a practical method to compensate the power degradation under variable loading conditions. Now, a complete system based on an impedance meter and the PA introduced in [16] is presented. This system is able to track the output load of the PA and dynamically change its V_{DD} according to the previously developed theory in a fully autonomous way, both under CW and modulated signal excitations. This system is physically implemented with a supply modulator made with a fast and efficient gallium nitride (GaN)-based switched dc–dc converter and an impedance meter that was specifically designed for low insertion loss, imposing a very small overall efficiency degradation. The architecture of the presented system makes it similar to envelope tracking (ET) applications, but with lower timing constraints. While, in ET PAs, V_{DD} must track the carrier envelope, requiring fast supply modulators that considerably reduce the total efficiency [18], in our case, V_{DD} should only track the movement of users, moving obstacles near antennas or other sources of load variation, which are typically much slower than the carrier envelope of telecommunication signals. Moreover, the required V_{DD} amplitude variation is lower than it is in ET PAs, so the necessary slew rate is much lower both due to the reduced speed and voltage swing requirements.

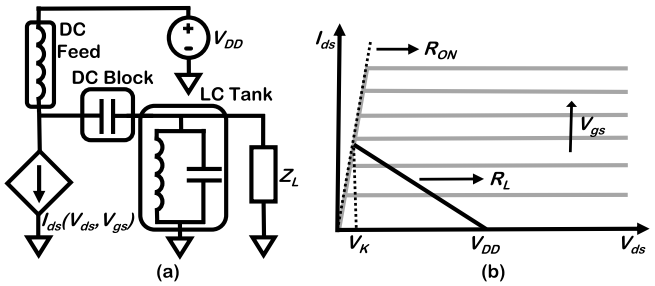

Fig. 1. (a) Simplified PA output circuit for the theoretical analysis. (b) Considered piecewise linear current source model.

This article is organized as follows. Section II demonstrates the derivation of the theoretical load-dependent V_{DD} values that correct the amplifier's output power capability. Section III presents the design and simulation of a Class B GaN PA using the derived V_{DD} values. Section IV shows the practical static validation of the proposed V_{DD}. Section V introduces the automatic V_{DD} controlled PA and its behavior under CW excitation. Section VI presents the system behavior under modulated signals. Section VII addresses the dynamic performance of the system and identifies its possible improvements. Section VIII presents the conclusions of this work.

II. Supply Voltage Variation Theory

The objective of this work is to achieve a load insensitive PA, from an output power capability perspective, while maintaining high-efficiency operation. To do this, first, it is necessary to calculate the dependence of the output power capability on V_{DD} and load terminations. Then, the drain voltage to be applied for each load, Z_L, needed to maintain the desired maximum output power, can be determined.

In order to achieve a constant maximum output power, the PA cannot be designed for the maximum power load. This happens because, when the load is shifted toward a lower value, increasing the V_{DD} would not compensate the power capability of the PA since the transistor would become current limited. Having this in mind, and also ensuring high-efficiency operation, the PA is designed for the maximum efficiency load, $R_{L_{\mathrm{eff}}}$. After applying the V_{DD} compensation, the maximum output power of the PA will be constant for every load within a voltage standing wave ratio (VSWR) circle centered on the efficiency load and equal to the maximum power delivered by the PA at the efficiency load, $P_{\mathrm{out}_{\mathrm{eff}}}$.

Going back to PA fundamentals, this analysis starts by considering a simplified circuit for the output of the amplifier, as shown in Fig. 1(a). The transistor current source is approximated by a piecewise linear model with a constant R_{ON}, as shown in Fig. 1(b).

The first step is to calculate the output power of the PA. It is calculated for a fundamental current component, I_1, and load, Z_L, as

$$P_o = \frac{1}{2}\mathrm{real}(Z_L)|I_1|^2. \tag{1}$$

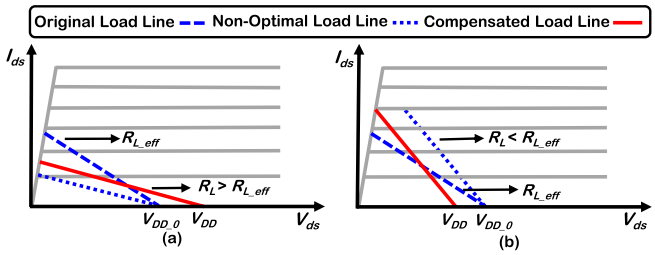

Fig. 2. Correction of the variations toward (a) higher real part loads and (b) lower real part loads.

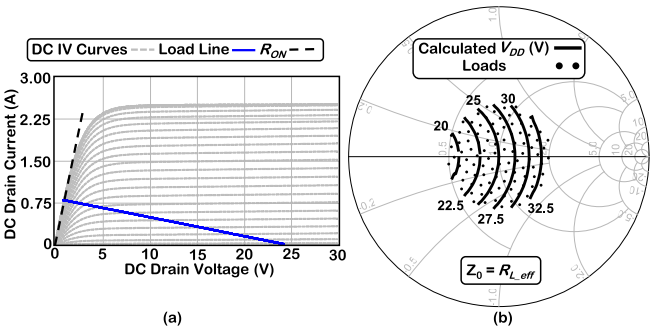

Fig. 3. (a) DC I/V characteristic of the used device, maximum efficiency load line, and calculated R_{ON}. (b) Calculated V_{DD} values for the used Wolfspeed device at the intrinsic current source plane. Please note that the design V_{DD}, V_{DD0}, is 25 V; therefore, it is the optimal V_{DD} for the designed load, $R_{L_{\mathrm{eff}}}$.

The fundamental component of the drain current is given by $(I_P/2)$ for a half-sine wave assuming a peak current equal to I_P. For loads higher than the maximum power load, I_P is defined by the load and the maximum voltage excursion imposed by the triode region, as described in

$$I_P(Z_L, V_{\mathrm{DD}}) = 2\frac{V_{\mathrm{DD}} - V_K}{|Z_L|} \tag{2}$$

where V_{DD} is the supply voltage and V_K is the I/V curve's knee voltage. This expression can be further developed by including the widely used constant R_{ON} approximation model [19]. The peak current is then given by

$$I_P(Z_L, V_{\mathrm{DD}}) = \frac{2V_{\mathrm{DD}}}{|Z_L| + 2R_{\mathrm{ON}}} \tag{3}$$

and the corresponding maximum output power by

$$P_{\mathrm{out}}(Z_L, V_{\mathrm{DD}}) = \frac{1}{2}\frac{\mathrm{real}(Z_L)}{(|Z_L| + 2R_{\mathrm{ON}})^2}{V_{\mathrm{DD}}}^2. \tag{4}$$

Then, the maximum delivered power for the efficiency load, which is real and equal to $R_{L_{\mathrm{eff}}}$, is given by

$$P_{\mathrm{out_{eff}}} = \frac{1}{2}\frac{R_{L_{\mathrm{eff}}}}{(R_{L_{\mathrm{eff}}} + 2R_{\mathrm{ON}})^2}{V_{\mathrm{DD}_0}}^2 \tag{5}$$

for the designed supply voltage equal to V_{DD_0}.

Finally, since the goal is to keep the maximum output power constant and equal to its value for the designed load, it is necessary to solve

$$P_{\mathrm{out}}(Z_L, V_{\mathrm{DD}}) = P_{\mathrm{out_{eff}}} \tag{6}$$

for V_{DD}, which results in the following expression:

$$V_{\mathrm{DD}}(Z_L) = \sqrt{\frac{R_{L_{\mathrm{eff}}}}{\mathrm{real}(Z_L)}}\,\frac{V_{\mathrm{DD}_0}(|Z_L| + 2R_{\mathrm{ON}})}{(R_{L_{\mathrm{eff}}} + 2R_{\mathrm{ON}})} \tag{7}$$

that gives a load-dependent V_{DD} that maintains the maximum output power at the required constant value, $P_{\mathrm{out_{eff}}}$.

Now, for better understanding, consider that the amplifier may suffer a variation of the real part of the load ($R_L = \mathrm{real}(Z_L)$) so that it now sees either a higher R_L or a lower R_L compared with the one considered in the design stage ($R_{L_{\mathrm{eff}}}$). Then, for higher loads, the fundamental current will be lower, as shown in Fig. 2(a). Thus, in this situation, V_{DD} given by (7) will be higher in order to restore the power capability of the PA (raising the voltage excursion). For lower loads, the maximum current swing becomes higher, increasing the maximum output power. However, the efficiency for the designed power is reduced (since the PA operates in back-off), as shown by the nonoptimal load line of Fig. 2(b). Thus, in this case, V_{DD} calculated using (7) will be lower in order to increase the efficiency, by keeping the maximum output power limited to its design value of $P_{\mathrm{out_{eff}}}$. In this analysis, it is assumed that the input power level is increased for operation under lower loads and decreased for operation under higher loads. This will maintain the device on the onset of saturation. Furthermore, this technique can only be used up to the point where the device clips in current for lower loads or enters into breakdown for higher loads.

After this qualitative explanation, using a simplified example for real load variations, expression (7) will be solved for various loads (including complex values) and using the design parameters of a real transistor. In this work, a class B design was used, and the chosen class B definition assumes a V_{GS} bias that corresponds to the I_{ds} third-order derivative null (for $V_{\mathrm{DD}} = V_{\mathrm{DD0}}$) with respect to V_{gs}. Thus, the maximum efficiency load, $R_{L_{\mathrm{eff}}}$, can be determined by the expression deduced in [19] that depends on the quiescent current, I_{dq}. R_{ON} can be approximated using the simulated I/V characteristics of the device, as shown in Fig. 3(a), for the device adopted in this work (Wolfspeed CGH40010F). These estimations using the I/V curves are correspondent to the intrinsic impedances at the current source plane but are useful to understand the behavior of the V_{DD} model. For this device, the estimated efficiency load, at the intrinsic plane, is 30 Ω, and the R_{ON} is 1.1 Ω. Since the V_{DD} model (7) is mostly insensitive to R_{ON}, a dc estimate is enough to compute it. As shown in Fig. 3(b), V_{DD} was calculated for loads within a 2.1 VSWR circle, which is a good estimate of the variation in active phased arrays [20].

III. PA Design and Simulation

In order to test the developed theory, a class B PA was designed. The PA operates at 3.55 GHz and is based on the Wolfspeed GaN device used in Section II. The OMN was designed to convert 50 Ω to the maximum efficiency load and to present short circuit harmonic terminations at the current source plane, ensuring class B operation at the design frequency.

The simulated output power and drain efficiency of the PA at the 1-dB gain compression point are shown in Fig. 4(a), in blue and red, respectively. The simulations were made for

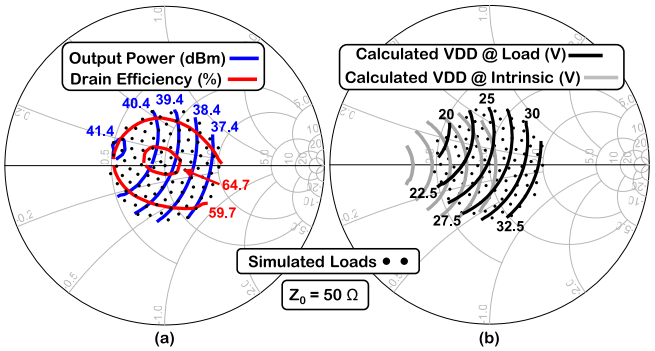

Fig. 4. (a) Simulated load–pull of the designed PA, with drain efficiency in red and output power in blue. The maximum output power is 41.4 dBm, and contours' step is 1 dB. The maximum efficiency is 64.7% with a contours' step of 5%. (b) Calculated V_{DD} at the intrinsic source (gray) and load (black) planes of the designed PA.

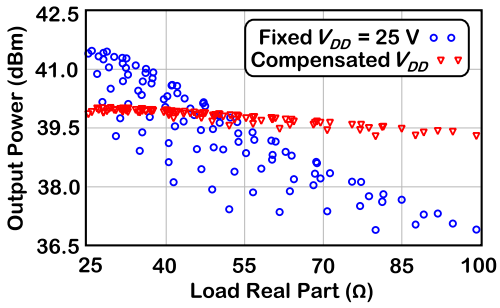

Fig. 5. Simulated output power of the designed PA for a fixed 25 V and the calculated supply voltages at the 1-dB compression point.

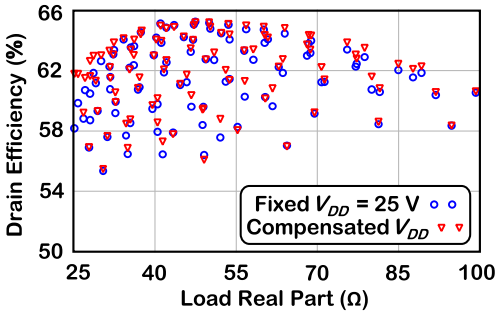

Fig. 6. Simulated drain efficiency of the designed PA for a fixed 25 V and the calculated supply voltages at the 1-dB compression point.

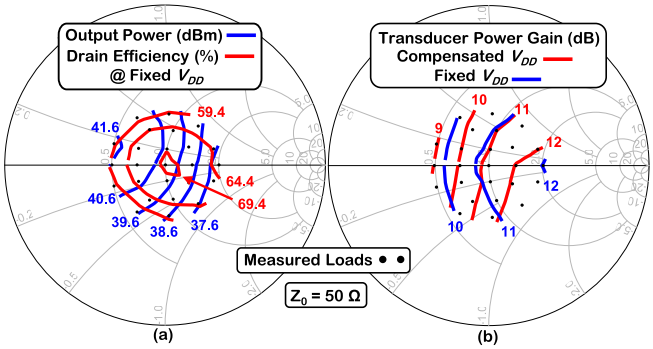

Fig. 7. (a) Measured load–pull of the fabricated amplifier for a fixed V_{DD} of 25 V. The maximum output power is 41.6 dBm, and the contours are shown with a step of 1 dB. The maximum efficiency is 69.4%, and the contours' step is 5%. (b) Measured transducer gain of the fabricated amplifier for a fixed V_{DD} of 25 V and the compensated V_{DD} values.

100 different loads, distributed inside a 2.1 VSWR circle, which corresponds to the typical magnitude variation expected in antenna arrays [21]. The input power was adjusted to maintain the compression level at 1 dB for all the tested loads.

Now, in order to test the designed PA with the predicted optimal V_{DD} values, these values [as plotted in Fig. 3(b)] need to be transformed from the current source plane of the used device to the load plane of the designed PA. To perform this reference plane shift, the used S-parameters correspond to the network between the device current source plane and PA load reference plane, which includes the intrinsic and extrinsic elements of the device, as well as the designed OMN. These S-parameters were extracted by optimization to match the load plane output power contours with the current source plane ones, which are aligned with the real axis. The V_{DD} values plotted at the load plane of the PA are shown in Fig. 4(b).

The simulated output power for each tested load is presented in Fig. 5, for the 1-dB gain compression point. The output power variation without V_{DD} compensation is 4.6 dB with a minimum value of 36.9 dBm. Using the calculated optimal V_{DD} values, the variation is reduced to 0.7 dB, and the minimum value is increased to 39.3 dBm, which corresponds to an increase of 2.4 dB of the output power capability of the PA for the worst case load.

The simulated drain efficiency of the amplifier is shown in Fig. 6. The variation, maximum, and minimum values are identical before and after compensation. The drain efficiency varies from 65.5% down to 56.0%, and on average, for the tested loads, it is 61.9%.

IV. Static Experimental Validation of the Load-Dependent V_{DD}

Before performing a full dynamic validation, it is necessary to verify if the developed load-dependent V_{DD} theory can indeed be used to correct the output power capability of the fabricated PA. The fabricated PA can be seen in [16] or in Fig. 11. Although, for validation purposes, the V_{DD} bias could be manually changed according to the measured load, a dc–dc buck converter, based on the EPC 9067 GaN demo board, has already been incorporated in the implemented class-B amplifier so that it can be used later on during the dynamic measurements that will be presented in Section V. The dc–dc converter is designed using two EPC8009 devices, in switched operation, with a switching frequency of 1 MHz, and the V_{DD} is varied using a pulsewidth modulation (PWM) signal. For this validation, V_{DD} is manually varied by setting the duty cycle that controls the buck converter according to the output load, which is measured using a vector network analyzer (VNA).

First, the amplifier was measured without the buck converter, for a 25-V fixed drain voltage and for 25 test loads synthesized in the laboratory using a manual load tuner. The obtained load–pull contours, measured at the 1-dB gain compression point, are presented in Fig. 7(a); for completion, the transducer gain is shown in Fig. 7(b) by the blue contours.

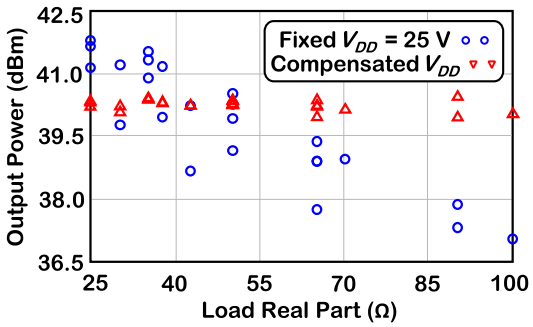

Fig. 8. Measured output power of the implemented PA for the fixed and optimal supply voltages at the 1-dB compression point.

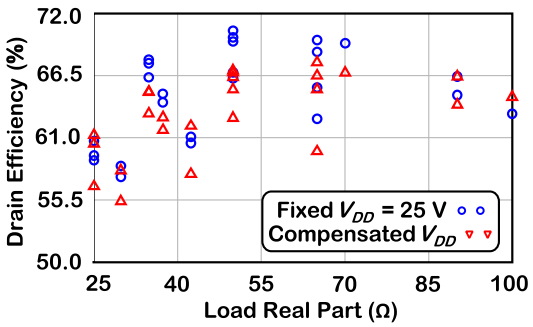

Fig. 9. Measured drain efficiency of the implemented PA for the fixed and optimal supply voltages at the 1-dB compression point.

The output power contours were compared with the simulated ones in order to verify their alignment. This comparison revealed a small phase rotation between the measured and simulated data. This small error can be corrected with an offset in the simulation reference plane and was corrected using a small (ideal) 50-Ω offset line at the load plane of the PA. Thus, in order to obtain the V_{DD} values for the laboratory measurements, this line was considered, and V_{DD} was recalculated for this corrected load reference plane.

The PA was then measured using the recalculated V_{DD} values. Now, the variation of the transducer gain using the compensation V_{DD} values is almost 4 dB, as shown by the red contours in Fig. 7(b), which is 2 dB higher than without V_{DD} compensation. This variation is taken into account in Sections V and VI to equalize the system small-signal gain, for both the fixed V_{DD} and compensated V_{DD} cases.

The output power is shown in Fig. 8 for the 1-dB gain compression point. The uncompensated PA shows a maximum output power variation of 4.7 dB and a minimum value of 37.0 dBm. Using the optimal V_{DD}, the obtained results show a variation of 0.5 dB and a minimum value of 39.9 dBm, which corresponds to a reduction of 4.2 dB in the variation and a worst case output power capability improvement of 2.9 dB. The average output power improvement over the range of tested impedances is 0.4 dB. This value increases to 0.7 dB if the uncompensated PA is operated at back-off for the lower loads to keep its output power at the nominal value of 40 dBm.

The drain efficiency, measured at the same gain compression point, is shown in Fig. 9. Without V_{DD} compensation, the efficiency varies between 56.6% and 69.5%, a variation of 12.9%, and on average, for the tested loads, it is 64.7%. With V_{DD} compensation, the efficiency is, on average, 1.7% lower for the same amount of variation. Note that the average efficiency over the tested range of loads would be lower for the uncompensated PA if it would be operated at back-off for lower loads to keep its output power at the nominal value of 40 dBm. Moreover, the efficiency includes the power dissipated in the buck converter only for the case of the variable V_{DD}. The presented measurements are static, i.e., the supply voltage was manually adjusted, and the load was measured with a VNA.

The measured output power and efficiency validate the developed theoretical load-dependent V_{DD} model, showing a compensation of the PA output power, though slightly reducing its average efficiency. This reduction is attributed to the losses in the buck converter, which increases with the switching frequency and with the V_{DD} (duty-cycle) reduction. The 1-MHz switching frequency was chosen to permit varying the V_{DD} fast enough to compensate load variations due to moving objects or beamforming on MIMO antenna arrays, even for extreme cases such as high-speed trains (HSTs) [22]; 1 MHz allows a variation of the PA supply at a rate below 1 ms, but, later, it is shown that the limiting factor for the compensation speed is not due to the switching frequency but due to the computation time necessary to calculate the load during the impedance measurement.

V. Automatic V_{DD} Control Integrated With an Impedance Meter

In Section IV, we have validated the correction of the output power capability variation with the load using the theoretical load-dependent V_{DD} model. However, to use this method as a fully operational system, it is necessary to integrate the V_{DD} control with impedance tracking so that V_{DD} can be automatically adjusted according to the load. This section is devoted to presenting this automatic V_{DD} controlled PA prototype, as well as its behavior under CW excitation. The measurement setup used to validate the integration of the fully automatic V_{DD} correction, as shown in Fig. 10, is composed of the system under test (SUT), a vector signal generator (VSG), one driver to feed the prototype, a load tuner to permit varying the loading conditions of the SUT, and a power 50-Ω load. The impedance measurements were acquired by a 16-GHz oscilloscope that was connected to the mainline through a bidirectional coupler. A 500-MHz oscilloscope is also used to measure the dc voltage that is actually applied to the PA. A one-port short-open-load (SOL) calibration was performed to correctly track the impedance using the oscilloscope, and an additional power calibration was also performed using a power meter, allowing power measurements directly from the oscilloscope measured waves.

The built prototype is shown in Fig. 11. It is composed of the previously presented class B PA with the dc–dc converter and by an accurate and low loss impedance meter system. The impedance measurement method is based on the slotted line theory and the synthesis of a standing wave replica by adding

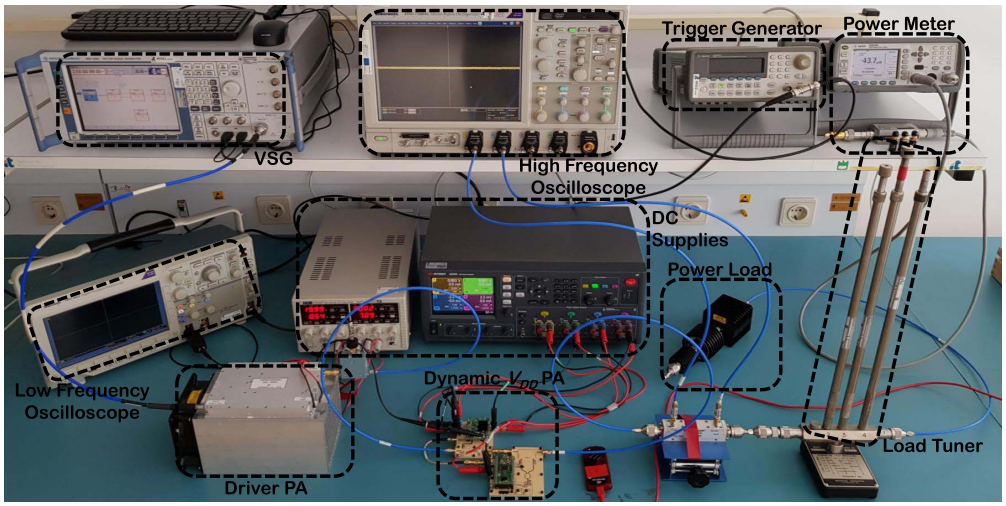

Fig. 10. Photography of the measurement setup. On the right half of the image, notice the manual stub-based load tuner that was used to vary the loading conditions of the SUT. Due to the limitations of manually varying the load conditions of the SUT, the load varies at slightly different time rates in multiple tests, as shown in Figs. 12 and 14.

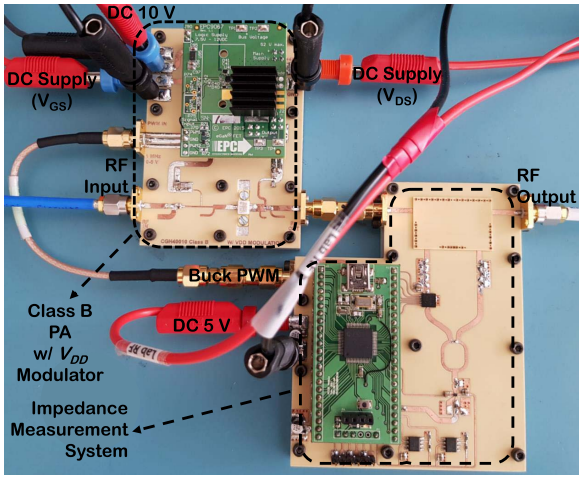

Fig. 11. Photography of the Class B PA with the impedance meter, resulting in the final system prototype.

the reflected wave with phase delayed versions of the incident wave (using a phase shifter). The time required to complete one measurement is around 12 ms, of which 11 ms is the time required for the computation of the measurement algorithm, and could be reduced by increasing the computational power or improving the algorithm. The used microcontroller runs the calibration and the measurement algorithm and is also responsible for generating a PWM signal to control V_{DD} by changing the duty cycle of the buck converter. Due to the limitations of the used PIC 32 internal PWM generator, the switching frequency of the buck converter was reduced to 500 kHz. Nevertheless, the time required to change V_{DD} is still limited by the impedance measurement time ($\approx$12 ms). By adding this system to the PA, a reduction of its maximum drain efficiency of around 4.2%, on average for all the loads inside a 2.1 VSWR circle, is expected. The causes of this efficiency degradation were attributed to different elements of the built system and are described in Table I.

TABLE I
CAUSES OF EFFICIENCY DEGRADATION ON THE BUILT SYSTEM

Buck Converter (applying optimal VDD)	Impedance Meter (insertion loss)	Impedance Meter (consumed dc power)
1.7 %	1.3 %	1.2 % (380 mW)

Contrary to Section IV, where the amplifier characterization was presented for the 1-dB compression point, here, the input excitation amplitude was computed to compensate for the small-signal gain variations with the change of the output impedance, Z_L. Thus, assuming linearity, this would lead to constant output power, as intended. Consequently, it is necessary to perform a small-signal analysis to create a model for $P_{\mathrm{in}}(Z_L, V_{\mathrm{DD}})$. However, for the case where no V_{DD} compensation is applied to the PA, it will operate in deep saturation due to its reduced output power capability.

In this test, the load is slowly varied within a 13.5-s window, and the synthesized variation is shown in Fig. 12 along with the variation on the intrinsic current source plane. Note that the load impedance starts at lower real part loads and varies toward higher real part loads. Fig. 13 shows the PA metrics for this load variation with the automatic V_{DD} control to maintain the RF output power capability, as well as the results for a fixed V_{DD}. The optimal V_{DD} for compensation is plotted along with the measured compensation V_{DD}, and it can be seen that the circuit correctly tracks the optimal values. As a result, the output power degradation is compensated for the higher loads (by 1.7 dB) and the efficiency, which already includes the power dissipated in the sensing circuit and buck converter, slightly improved for lower loads (by 5%).

Note that, in Fig. 13, the efficiency reduction is higher than expected by analyzing Table I, reaching 11% for some loads. This happens for loads where the efficiency degradation caused by the dc–dc converter (applying the optimal V_{DD}) is higher than its average of 1.7%. It is also aggravated by the

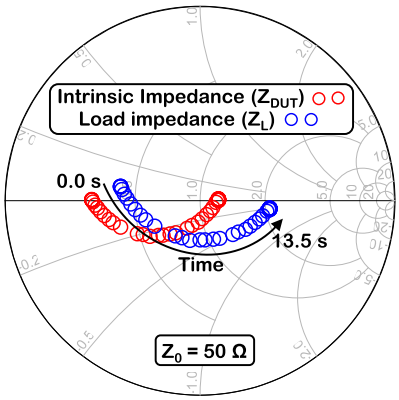

Fig. 12. Synthesized load trajectory for CW measurements (blue) and correspondent intrinsic current source plane impedance (red).

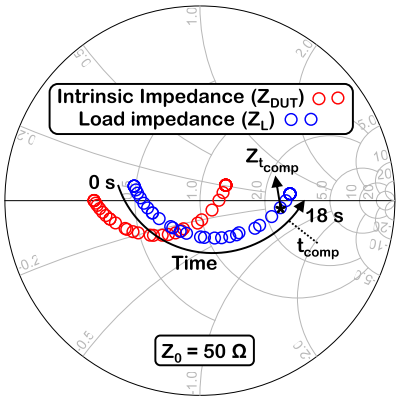

Fig. 14. Synthesized load trajectory for modulated signal measurements (blue) and correspondent intrinsic current source plane impedance (red).

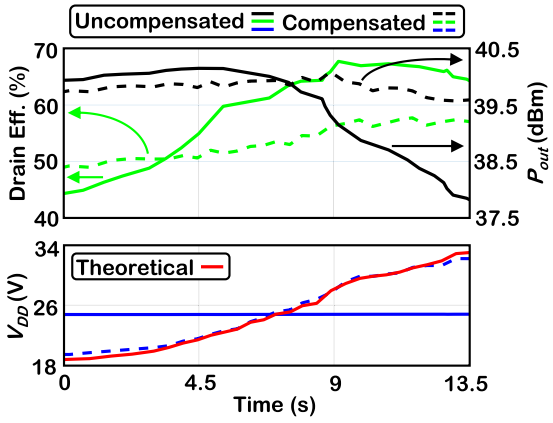

Fig. 13. Compensated and uncompensated output power and efficiency of the PA, along with the fixed and compensation V_{DD}'s that were used in the uncompensated and compensated cases, respectively. In addition, the theoretical optimal V_{DD} calculated from the measured load is plotted in red.

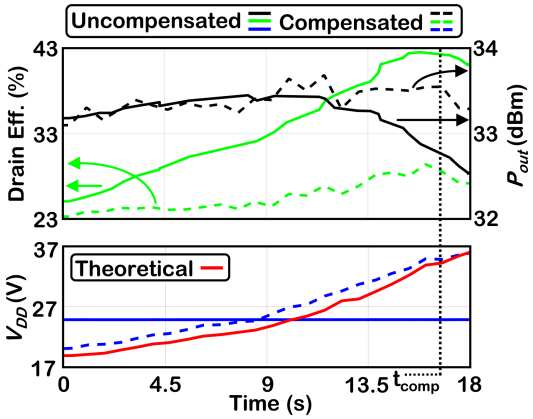

Fig. 15. Compensated and uncompensated average output power and average efficiency of the PA operating with modulated signal excitation, along with the fixed and variable V_{DD} used in the uncompensated and compensated cases, respectively. In addition, the theoretical V_{DD}, calculated from the measured load, is plotted in red.

higher gain compression of the PA when the V_{DD} is fixed at 25 V. This higher compression happens due to: 1) V_{DD} being lower and 2) the used input power being computed from the small-signal gain to try to achieve a constant output power, as previously explained. Up to around 7 s, there is also an error of a few tenths of dB on the targeted output power, causing the compression level to be slightly higher for the uncompensated case, which can also substantially increase the measured drain efficiency.

VI. Load Insensitiveness Under Modulated Signal Excitation

In PAs operating with telecommunication signals, the amplitude of the incident and reflected waves is time-dependent, due to the amplitude modulation. Therefore, other challenges arise, namely, on the impedance measurement under modulated signals. This section is dedicated to test the impedance measurement system under modulated signal and presenting the advantages of using the V_{DD} compensation for these telecommunication signals. For these tests, an OFDM signal with 20-MHz bandwidth and approximately 9.4-dB peak-to-average power ratio (PAPR) was used. Fig. 14 shows the synthesized load variation for the modulated signal test, simulating the movement of users or any obstacle near the antenna. Please note that the load impedance will vary in a much slower time scale than the envelope rate, and so a low-pass filter was added on the envelope detector used in the impedance meter. The impedance variation with time goes from lower to higher real part loads and one specific load, $Z_{t_{comp}}$, is marked at t_{comp}. This is the load for which the RF envelope of the modulated signal will be analyzed and compared with the envelope for operation under the nominal load, Z_{ref}.

Fig. 15 shows the automatic V_{DD} control performance under modulated signal excitation, presenting the measured average output power and efficiency versus time when the load is varying. The error in tracking the optimal V_{DD} is higher when compared with the CW case. This is caused by an increased imprecision on the load measured by the impedance meter. The actual V_{DD} is higher, which will slightly reduce the average drain efficiency. Nevertheless, the reduction should be small as the maximum error in voltage is 2.4 V. The sources of drain efficiency reduction between the uncompensated and compensated cases are the same that have been identified

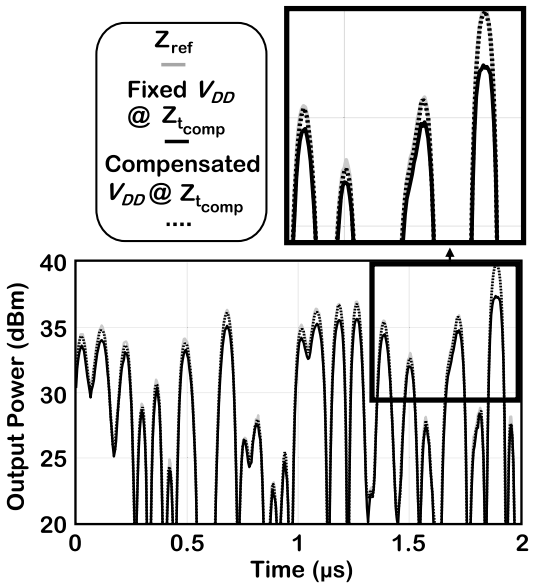

Fig. 16. Output power envelope for a section of the used signal for two load conditions: Z_{ref} (gray) and $Z_{t_{comp}}$ (black). For $Z_{t_{comp}}$, which produces a high output power degradation, a comparison of the output signal envelopes with and without V_{DD} compensation, in dashed and solid black lines, respectively, is shown.

in Section V. However, the efficiency degradation is slightly higher because the PA is less compressed due to the higher actual compensation V_{DD}. In addition, in the time region where the uncompensated PA compresses, a larger efficiency drop is observed. However, in this time region, the efficiency of the uncompensated case is higher than it should be, due to the PEP compression of the signal envelope and consequent PAPR reduction, which causes an increase in the average output power and average efficiency. The average output power is also presented in Fig. 15 for a fixed V_{DD} of 25 V and the compensated V_{DD}. Now, due to the high PAPR of the used signal, only the peak power of the signal is degraded. This causes a degradation of the average output power of only 0.7 dB that was compensated to 0.1 dB. Fig. 16 presents the instantaneous output power envelope captured with the oscilloscope (which was previously calibrated) for two different impedance load conditions: 1) Z_{ref}, which is the reference and no compensation is needed and 2) $Z_{t_{comp}}$, with output power degradation (which is the load marked at t_{comp} in Figs. 14 and 15) and so requiring V_{DD} compensation. By analyzing Fig. 16 for a fixed V_{DD}, a reduction of almost 3 dB on the peak power and a distorted envelope are noticeable. However, for the compensated V_{DD}, the peak power is restored, and the envelope shape is almost entirely corrected.

Figs. 17 and 18 show the amplifier's dynamic transducer gain and phase shift under the same modulated signal excitation (for the same three cases considered before). In Fig. 17, it is shown that applying V_{DD} compensation slightly increases the small-signal gain, as shown in Section IV. Also, the peak power of the signal is restored, and the abrupt gain compression is eliminated. However, the output signal phase shift is slightly increased, as shown in Fig. 18.

In order to further check the amplifier's linearity when V_{DD} is compensated through the presented system, the signal

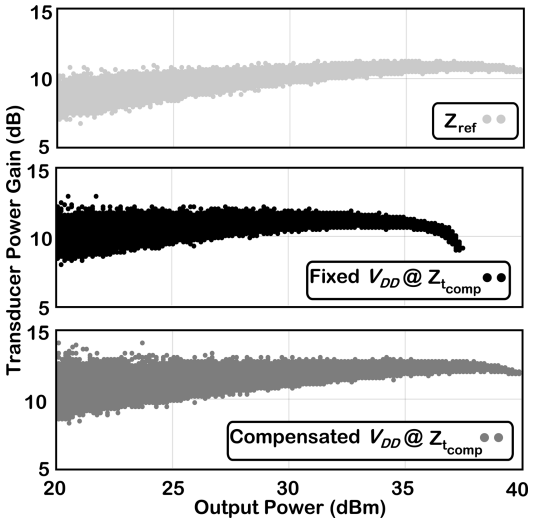

Fig. 17. Dynamic transducer gain of the amplifier for two load conditions: Z_{ref} (light gray) and for $Z_{t_{comp}}$, which shows a high output power degradation. For $Z_{t_{comp}}$, the black plot corresponds to the case where no V_{DD} compensation is applied, and the darker gray plots the case with V_{DD} compensation.

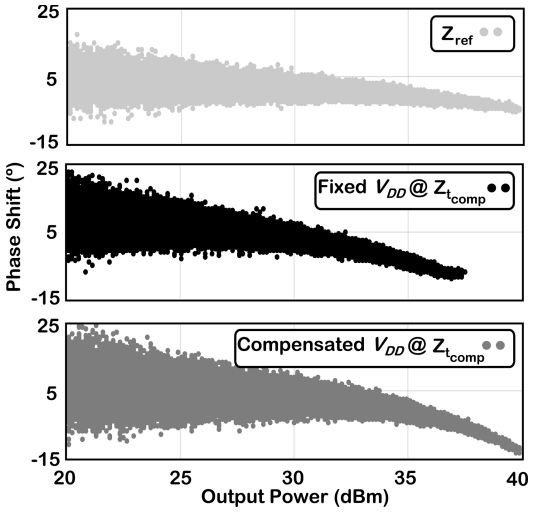

Fig. 18. Dynamic phase shift of the amplifier for two load conditions: Z_{ref} (light gray) and for a $Z_{t_{comp}}$, which shows a high output power degradation. For $Z_{t_{comp}}$, the black plot corresponds to the case where no V_{DD} compensation is applied, and the darker gray plots the case with V_{DD} compensation.

spectra (once again for the three cases considered before) are shown in Fig. 19. The adjacent channel power ratio (ACPR) was calculated for all cases and presented in Table II. These results show that the system's linearity under V_{DD} compensation is not degraded. In fact, the ACPR is slightly lower than it is under the same load variation but without V_{DD} compensation. Although the distortion power is not reduced with the V_{DD} compensation, this reduction of ACPR is justified by an increase of the channel power.

VII. System Time Performance

In the previous sections, the built prototype was validated as an automatic V_{DD} controlled PA under CW and modulated

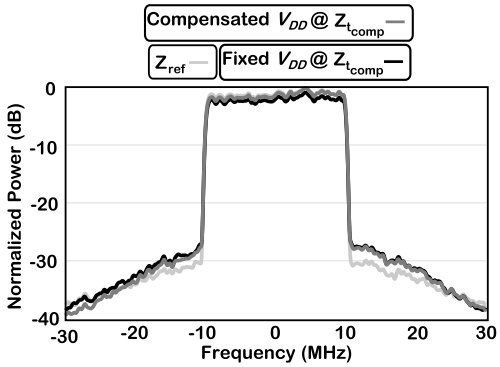

Fig. 19. Spectra of the output signal of the amplifier for three different cases: Z_{ref} (light gray) and $Z_{t_{comp}}$ (black), where there is high output power degradation without V_{DD} compensation. The same load, $Z_{t_{comp}}$, with V_{DD} compensation, in darker gray.

TABLE II

CHANNEL POWER, DISTORTION POWER, AND ACPR FOR THE THREE DIFFERENT CASES

	Reference Load	High Load Fixed VDD	High Load Comp. VDD
Norm. Channel Power (dB)	0.0	-1.0	-0.2
High Band Power (dB)	-31.7	-29.6	-29.8
Low Band Power (dB)	-32.0	-30.3	-31.0
ACPR Low (dB)	**-31.7**	**-28.7**	**-29.6**
ACPR High (dB)	**-32.0**	**-29.4**	**-30.8**

signal excitations. However, the synthesized loads for validation were slowly varying (13- and 18-s time frames with around 15 V of V_{DD} variation). In this section, the prototype is tested for faster load variations, which mimics load variations that would occur in real applications, in order to analyze its time constraints. Fig. 20 presents a comparison between the developed theoretical V_{DD} model, which was calculated from the measured load, and the actually measured V_{DD} for different-shaped pulses that correspond to the synthesized load variations. In Fig. 20(a), a sequence of different pulses with different shapes and time characteristics is presented. The prototype is able to correctly track the optimal V_{DD} for the presented transitions, which validates the capability of the proposed system to compensate for V_{DD} under different variable loading profiles. In order to check the response of the system to fast load variations, Fig. 20(b) and (c) presents a fast optimal V_{DD} step-up and step-down profiles, respectively. The maximum delay between the optimal and measured V_{DD} is expected to be, roughly, the time necessary to measure the load and change the V_{DD} twice and occurs when the waveform acquisition for the load computation happens right before the steady state of the optimal V_{DD} step, as shown in Fig. 21. In this case, V_{DD} will not change to its final value, and a second measurement will be needed, delaying the final V_{DD} value by 2×13 ms. However, although there may be some inaccuracy associated with the time axis of the presented

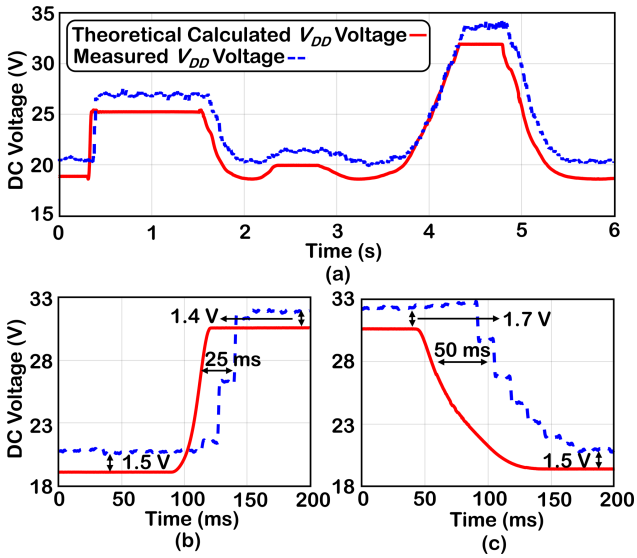

Fig. 20. Comparison between the measured supply voltage used on the compensated PA and calculated optimal supply voltage, for three cases. (a) Variable loading sequence of 6 s. (b) Fast step-up transient. (c) Fast step-down transient.

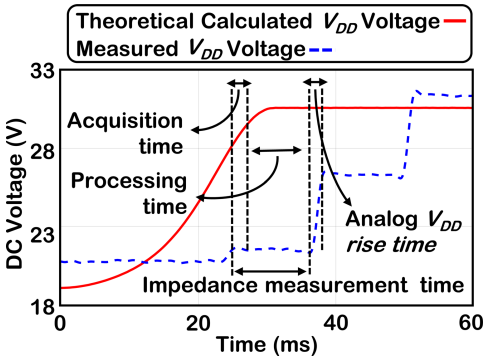

Fig. 21. Analysis of the rise time of V_{DD}, as well as the acquisition and computation times of the impedance measurement under a fast step-up pulse.

measurements, due to different trigger delays and response times of the used measuring instruments, the maximum step-up delay between the optimal and measured V_{DD} is around 25 ms. During the step-down, the delay can achieve higher values, up to 50 ms, but, since the actually applied V_{DD} is higher than the optimal one, this will cause a hardly noticeable reduction on the average drain efficiency of the PA but will have no effect on the output power capability compensation. It is suspected that these higher than expected measured delays are caused by imprecision on the impedance measurement, resulting in an underestimated V_{DD} during the optimal V_{DD} step-up and an overestimation during the step-down. The impedance measurement imprecision is probably caused because the impedance meter is acquiring data to compute the load value, while the load is varying at a similar time rate. However, this phenomenon is not further investigated since it is considered more important to first reduce the computation time, which is the highest temporal limitation, as shown in Fig. 21.

Fig. 21 shows that the time required to change the V_{DD} of the PA, which is roughly 13 ms, is imposed by the time required to measure the output impedance of the PA ($\approx$12 ms). This measurement time can be divided into the acquisition time ($\approx$1 ms), which is the time required to acquire the synthesized stationary wave, and the computation time ($\approx$11 ms), which is the time necessary to compute the algorithm that gives the output load of the PA. Thus, as previously introduced, the computation time is the highest temporal limitation of the built prototype, and since it can be reduced by increasing the computational power or improving the control algorithm, the time performance of the dynamic V_{DD} control can be greatly improved.

VIII. Conclusion

This work presented an automatic system that is able to restore the output power capability of a PA, by dynamically changing its V_{DD}, under variable loading scenarios. The calculated V_{DD} values have been validated in simulation and laboratory measurements for a 3.55-GHz GaN class B PA. The presented prototype is able to track down the output load of the PA and dynamically change its supply voltage accordingly. For that, a high-efficiency GaN dc–dc converter was used and controlled by a low loss impedance meter. The presented system is able to correctly track down the load and apply the calculated V_{DD} to the PA, for CW and modulated signals. For a fixed gain compression of 1 dB, the output power was compensated by 4.2 dB, and the power capability of the PA was improved by 2.9 dB, for the worst case loads. Under the modulated signal excitation, the proposed system is able to restore the peak power of the output signal, which was degraded by almost 3 dB for the worst case loads using a fixed V_{DD}, and the ACPR is maintained. The cost is the added complexity and a reduction in the drain efficiency due to the losses added by the dc–dc converter (1.7%) and the impedance meter (2.5%). The compensation was effective for all the loads within a 2.1 VSWR circle. The time limitation of this system is the required time for the microcontroller to compute the load and generate the PWM signal, causing delays up to 25 ms on the V_{DD} step-up. Nevertheless, this is believed to be enough for the time rate required by most of the proposed applications and can also be improved by increasing the computational power of the system or the control algorithm.

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The authors would like to acknowledge Ampleon Netherlands, namely, Dr. Sérgio Pires and Dr. Alireza Shamsafar, for interesting technical discussions regarding some of the observations dealt with in this article during the collaboration project with the Instituto de Telecomunicações—Aveiro Team.

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Appendix E

Supply Voltage Modulation on Doherty PAs

Load Insensitive Doherty PA Using Load Dependent Supply Voltages

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Load Insensitive Doherty PA Using Load Dependent Supply Voltages

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***Abstract* — This paper presents optimal carrier and peaking drain voltages to preserve the output power capability and back-off level of Doherty power amplifiers (PAs) operating for non-optimal loads. These voltages are theoretically obtained from back-off and full power conditions. A performance comparison between simulations of a conventional Doherty and the proposed load insensitive version is presented, showing that the introduced theory can be very advantageous for operation under load varying scenarios. A 3.6 GHz load insensitive Doherty PA was designed, implemented and measured for loads distributed inside a 2.0 voltage standing wave ratio circle. These measurements validated the introduced theory, showing an almost constant maximum output power (42.9 - 43.2 dBm), and a back-off level varying between 5.0 dB and 6.2 dB. The 6-dB output power back-off efficiency varies between 42 % and 53 %, in which the highest degradation corresponds to loads with high imaginary parts.**

***Keywords* — power amplifiers, Doherty, load insensitivity, V_{DD} compensation.**

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I. Introduction

Power amplifiers (PAs) can operate with varying loading conditions due to various causes. Under this non-optimal operation, their performance is degraded, mainly in terms of output power and drain efficiency. Various techniques have been proposed to compensate this degradation and restore the original performance of the PA, without using isolators, which are bulky and difficult to integrate. For example, tunable matching networks (TMNs) based on variable length stubs [1], or varactors [2], offer a good tunability range of the output load but suffer from considerable added losses. More complex PA topologies, as for example balanced PAs [3], can be used to reduce the performance degradation but not to completely eliminate it. Lastly, the dynamic control of supply voltages can be used to improve the performance of PAs operating in these scenarios, and this solution becomes more attractive as the efficiency of dc-dc converters becomes higher [4].

In [4] a load dependent supply voltage was successfully used to reduce the maximum output power variation of PAs. However, modern telecommunication signals have a high peak-to-average power ratio (PAPR) and this technique is only effective for single-ended PAs that are very inefficient at back-off (BO). In [5] a digital Doherty PA was presented, where appropriate driving signals are used to reduce the performance degradation under load varying conditions. Driving signals of digital Doherty PAs can be designed to use some power of the peaking amplifier to correct the carrier load, but this will degrade the back-off efficiency of the PA and can only compensate variations towards lower loads.

This paper proposes a theoretical-based load dependent supply voltage variation to correct the performance of Doherty PAs operating under non-optimal loads. It is shown that two independent drain voltages should be used for the carrier and peaking devices. In addition, this technique requires designing the PA for a different full-power (FP) load, which must be higher than the devices' optimal one. This slightly reduces the output power for operation under the nominal load, but allows achieving load insensitiveness by properly controlling the drain voltages of the devices.

II. Doherty Carrier and Peaking Drain Voltages

The theoretical derivation of the load dependent supply voltages (V_{DD}) assumes an ideal two-way symmetrical Doherty PA. To maintain both the FP output power and BO level constant for non-optimal loads, it is necessary to ensure a constant output power at the 6-dB output power back-off (OBO) point. This condition can be used to obtain the carrier drain voltage as a function of the load, $V_{DD_C}(\beta)$, where $\beta = \frac{Z_0}{Z_L}$. To do this, note that the output power at the 6-dB OBO point corresponds to the saturated power of the carrier, $P_{O_C}(\beta)$, for the BO load, $Z_C^{BO}(\beta) = \beta Z_0$. Thus, we have to choose $V_{DD_C}(\beta)$ so that,

$$P_{O_C}(\beta) = P_{O_C}(\beta = \beta_0) \tag{1}$$

where $\beta_0 = 2$, corresponding to the load $Z_L = \frac{Z_0}{2}$, i.e. to the nominal BO load.

For a piece-wise linear current source without R_{ON}, the saturated power, $P_O(Z_D)$, for operation with a load, Z_D, higher or equal to the maximum power load (ensuring saturation at the triode region) is given by

$$P_O(Z_D) = \frac{1}{2}\frac{{V_{DD}}^2}{{|Z_D|}^2}\mathrm{Re}(Z_D). \tag{2}$$

From where it is determined $V_{DD_C}(\beta)$ by replacing Z_D with the carrier BO load, $Z_C^{BO}(\beta)$, and equating the power to the nominal one:

$$\frac{{V_{DD_C}(\beta)}^2}{{|\beta|}^2}\mathrm{Re}(\beta) = \frac{{V_{DD_0}}^2}{{|\beta_0|}^2}\mathrm{Re}(\beta_0) \tag{3}$$

where V_{DD_0} is the nominal supply voltage. The previous expression can then be solved for $V_{DD_C}(\beta)$, obtaining

$$V_{DD_C}(\beta) = \frac{|\beta|}{\sqrt{\beta_0 \mathrm{Re}(\beta)}}V_{DD_0} \tag{4}$$

which gives the supply voltage of the carrier amplifier that maintains the 6-dB OBO output power.

Now, in order to maintain the OBO level equal to 6 dB and, consequently, the FP output power of the Doherty PA,

the maximum output power of the amplifier is set equal to 4 times (6 dB) the BO power, as described in

$$P_{O_C}(\beta) + P_{O_P}(\beta) = 4 \cdot P_{O_C}(\beta = \beta_0). \tag{5}$$

The previous expression can be further developed using (2) with Z_D equal to the carrier and peaking FP impedances, $Z_C^{FP}(\beta, \alpha) = (\beta - \alpha)Z_0$ and $Z_P^{FP}(\alpha) = \frac{Z_0}{\alpha}$, respectively, where $\alpha = \frac{I_P}{I_C}$, obtaining:

$$\frac{V_{DD_C}(\beta)^2}{|\beta - \alpha|^2}\mathrm{Re}(\beta - \alpha) + V_{DD_P}(\beta)^2\mathrm{Re}(\alpha) = 4\frac{V_{DD_C}(\beta)^2}{|\beta|^2}\mathrm{Re}(\beta). \tag{6}$$

Then, to ensure that the devices operate at the on-set of saturation, the voltage excursion should be equal to the V_{DD} bias:

$$\begin{cases} 2V_{DD_P}(\beta) = |I_P||Z_P^{FP}(\alpha)| \\ 2V_{DD_C}(\beta) = |I_C||Z_C^{FP}(\beta, \alpha)| \end{cases} \tag{7}$$

and so, it is possible to obtain another expression for $V_{DD_C}(\beta)$, as

$$V_{DD_C}(\beta) = V_{DD_P}(\beta)|\beta - \alpha|. \tag{8}$$

Finally, by replacing the obtained $V_{DD_C}(\beta)$ in (6), the following relationship is obtained,

$$|\beta| = 2|\beta - \alpha| \tag{9}$$

which then can be used in (8) to remove the dependence with α and further develop the expression using (4) to achieve

$$V_{DD_P}(\beta) = \frac{2}{\sqrt{\beta_0 \mathrm{Re}(\beta)}} V_{DD_0} \tag{10}$$

which gives the supply voltage for the peaking amplifier to maintain the 6-dB OBO level.

III. Simulated Performance Improvement

For this technique to be effective, the amplifier must be designed for a FP load higher than the devices' maximum power one, R_{opt}, ensuring that none of the used devices will be current saturated for any of the loads considered for correction. The optimal value, Z_{FP}, can be calculated using the load line expression, $|I_{MAX}| = 2V_{DD}/|Z_L|$, for the carrier and peaking FP impedances and supply voltages, obtaining:

$$Z_{FP} = R_{opt}\sqrt{\frac{x}{\beta_0}} \tag{11}$$

with

$$x = \max\left(\frac{4}{\mathrm{Re}(\beta_{min})}, \frac{|\beta_{max}|^2}{\mathrm{Re}(\beta_{max})}\right) \tag{12}$$

which gives the optimal impedance that is limited by the carrier for higher loads and by the peaking for lower loads. This assures that I_{MAX} is only reached for the highest mismatch load, within the targeted correction region. For $\beta_0 = 2$ and a load variation of 4:1 ($\frac{Z_0}{4} < Z_L < Z_0$) the optimal FP load is equal to $\sqrt{2}R_{opt}$.

Figure 1 presents the load lines for a conventional Doherty, a) to c), and for the proposed load insensitive version, d) to f).

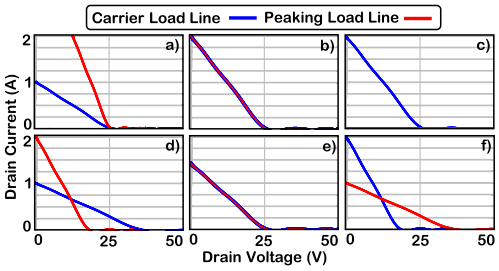

Fig. 1. Comparison between the load lines of conventional Doherty PAs and the proposed load insensitive version, for half the nominal load, a) and d), the nominal load, b) and e), and twice the nominal load, c) and f).

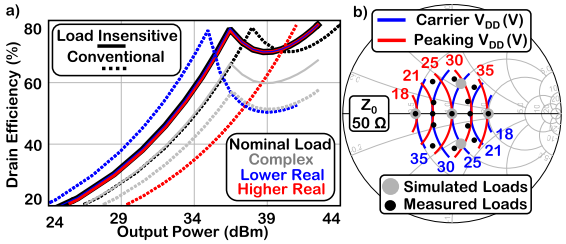

Fig. 2. a) Drain efficiency comparison between a conventional Doherty and the proposed one. b) Carrier and peaking V_{DD} values for the tested loads.

For these simulations, both the conventional and the proposed Doherty PAs have been considered digital, i.e. they are both driven with different input signals for each load. These input signals have been calculated to keep the carrier operating close to the triode region from BO to FP, ensuring high efficiency.

For the conventional case and lower loads, a), the peaking load becomes lower, degrading the efficiency and output power; the carrier load becomes higher reducing the output power. For higher loads, c), the carrier load becomes lower, degrading the BO efficiency; the peaking is not used because it would load pull the carrier to even lower loads, decreasing its output power and efficiency, due to current saturation.

For the proposed PA, the load lines do not reach I_{MAX} for the nominal load, e), as expected, since the PA was designed for $\sqrt{2}R_{opt}$. However, none of the devices becomes current saturated for any load in the design range. For lower/higher loads, d)/f), the carrier maximum current becomes lower/higher and its V_{DD} is increased/decreased to maintain its output power. On the other hand, the peaking maximum current becomes higher/lower and its V_{DD} is decreased/increased also to maintain the delivered power.

Figure 2 a) presents the drain efficiency of the conventional and proposed Doherty PAs for the gray loads of Fig. 2 b). As expected from the load line analysis, the proposed PA maintains its efficiency profile, guarantying a constant 6-dB OBO and output power of 42.5 dBm for every load. For complex loads the performance is also maintained, but with some efficiency degradation, as already observed for a single-ended PA in [4]. The conventional PA has 6-dB of OBO and a slightly higher output power of 44 dBm for the nominal load. However, for lower loads its output power is degraded to 41 dBm and the efficiency reduced by almost 30 % at FP.

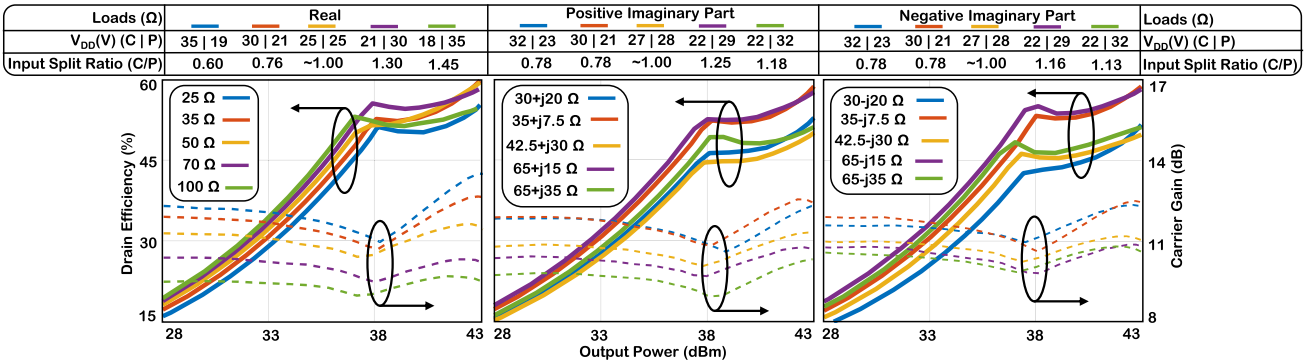

Fig. 3. Measured drain efficiency (continuous) and carrier gain (dashed) of the propsoed Doherty PA for various loads distributed inside a 2.0 VSWR circle.

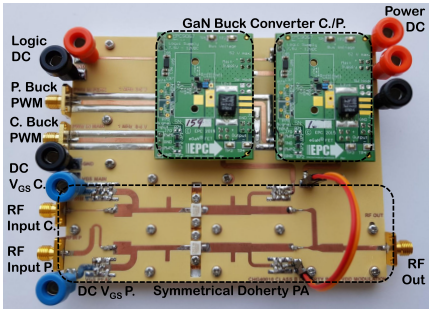

Fig. 4. Photograph of the implemented Doherty prototype.

For higher loads its output power is also degraded to 41 dBm and the 6-dB OBO efficiency reduced by more than 20 %.

IV. Experimental Validation

To validate the proposed Doherty V_{DD} compensation theory, a Doherty PA was designed for 3.6 GHz, with digital inputs. The design uses two Wolfspeed CGH40010F devices biased with a nominal V_{DD_0} of 25 V. Both devices operate with class B harmonic terminations. The carrier is biased with 25 mA of quiescent current and the peaking is in shallow class C. The built prototype is shown in Fig. 4.

The measurements were done using a manual load tuner to synthesize the impedances and Through Reflect Line (TRL) calibration to measure them at the simulation reference plane. The amplifier was designed to present real impedances at the devices' intrinsic current source for output real impedances, so the practical V_{DD} values, have been obtained directly from the theory presented in Section II and plotted in Fig. 2 b).

Figure 3 shows the measured drain efficiency (continuous) profiles of the implemented prototype for the black loads presented in Fig. 2 b), and the correspondent V_{DD} values and input split ratios. Note that a Z_L of 50 Ω is the optimal impedance, for which the intrinsic FP load of both devices is equal to $\sqrt{2}R_{opt}$. Analyzing this figure it is possible to see that the amplifier maintains a Doherty behavior for all the tested loads, keeping the output power very close to 43 dBm (target output power) and the OBO level very close to 6 dB. The efficiency is also maintained high, a reduction of around 10 % is observed for the loads with higher imaginary part, as already expected from the simulations shown in Fig. 2, in gray. Table 1 summarizes the performance for some of the tested loads. The carrier gain (dashed) shows a maximum expansion/compression of 2.6 dB. However, the PA characteristics change with the load and its linearization would require the DPD to change accordingly.

Table 1. Measured FP and OBO performance of the implemented prototype.

Load (Ω)	**25**	**50**	**100**	**65 +j15**	**30 +j20**	**65 -j35**	**42.5 -j30**
FP (dBm)	43.1	**43.2**	42.9	43.2	43.2	43.2	43.2
OBO (dB)	5.0	**6.0**	5.8	5.2	5.1	6.2	5.9
FP Eff. (%)	55.9	**60.2**	54.6	58.2	53.5	51.5	50.1
6-dB OBO (%)	45.9	**50.1**	53.1	49.4	44.1	48.0	46.2

V. Conclusion

In this paper, the optimal load dependent V_{DD} voltages for the carrier and peaking devices of a two-way 90° Doherty PA were derived. When used in a properly designed PA (designed for FP impedance of $\sqrt{2}R_{opt}$), these supply voltages adjust the amplifier load lines maintaining its output power and OBO level for operation under non-optimal loads. The proposed theory was validated with laboratory measurements for a digital Doherty prototype operating at 3.6 GHz, with an output power of 43 dBm and 6 dB of OBO. The worst case measured output power and OBO were 42.9 dBm and 5 dB, respectively, for operation under several non-optimal loads distributed inside a 2.0 VSWR circle. The drawback of this load insensitivity Doherty PA is the reduced (by 1.5 dB) output power for the nominal load.

Acknowledgment

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Appendix F

Supply Voltage Modulation on Doherty PAs - Extended

Quasi-Load Insensitive Doherty PA Using Supply Voltage and Input Excitation Adaptation

Cristiano F. Gonçalves, Filipe M. Barradas, Luis C. Nunes, Pedro M. Cabral, José C. Pedro

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Quasi-Load Insensitive Doherty PA Using Supply Voltage and Input Excitation Adaptation

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***Abstract*— This article presents a quasi-load insensitive (QLI) Doherty power amplifier (DPA). The proposed theory makes the amplifier load insensitive in terms of output power, while its efficiency is slightly degraded for complex loads. The load insensitiveness is achieved by dynamically changing the supply voltages (V_{DD}) and the input power splitting for both the carrier and peaking transistors. The optimal, load-dependent, V_{DD} values are theoretically derived from back-off (BO) and full power conditions using load line theory. The optimal input excitation signals for the carrier and peaking devices are also derived for these variable V_{DD} conditions. A 3.6-GHz QLI DPA was designed, and a complete system, composed of the DPA output stage, a two-channel medium power driver, an adaptive input driving stage, and a load sensing system, was implemented. The laboratory measurements have been performed for loads distributed inside a 2.0 maximum voltage standing wave ratio (VSWR) circle and show an output power variation between 43.8 and 42.6 dBm and a BO efficiency between 50% and 35%. Under modulated signal excitation, for the worst case loads, the peak output power capability of the DPA is improved from 41.7 to 43.1 dBm, and the average efficiency is increased from 32.6% to 43%.**

***Index Terms*— Doherty power amplifier (DPA), load insensitivity, power amplifier (PA), supply voltage modulation.**

I. Introduction

POWER amplifiers (PAs) are used for various applications, and their performance has a considerable impact on the overall system operation. Normally, PAs are designed to operate with a fixed output load. However, they can be forced to operate under varying load conditions due to various causes and in different scenarios, such as microwave cooking [1], plasma heating in, e.g., plasma-enhanced chemical vapor deposition (PECVD) processes [2], or in the charging of particle accelerators cavities [3]. In telecommunication applications, the PA output load can also change due to moving objects on the antenna proximity, e.g., the hand effect [4], or also due to mutual coupling between different antenna elements on fifth-generation (5G) massive multiple-input multiple-output (MIMO) base stations (BSs) with beamforming capabilities [5].

In this nonoptimal regime, the PA performance is degraded, mainly in terms of output power, drain efficiency, and linearity. In order to compensate for this performance degradation, various techniques have been proposed during the last years. Using tunable matching network (TMN) techniques, such as switched variable length stubs [6], varactors [7], or switched capacitors [8], [9], on the PA output matching network (OMN) is one possibility. However, these techniques, being based on variable components, result in an increase in the output losses of the PA, reducing its efficiency. Moreover, it can be difficult to design the required variable elements for higher power applications, and the design complexity of the OMN becomes much higher. Other techniques are based on the PA supply voltage (V_{DD}) variation, which can be very attractive with modern dc-to-dc converters that are highly efficient and can provide high output power. Paul *et al.* [10] use a combination of adaptive power supply and adaptive impedance tuning to compensate for load variations and also to increase back-off (BO) efficiency when lower output power levels are required. However, the load compensation is still mainly based on TMN techniques with the previously introduced disadvantages. In [11], a load-dependent supply voltage was derived and successfully used to reduce the maximum output power variation of single-ended PAs under load varying conditions. However, the efficiency is not compensated, even reduced in some cases, due to the power dissipated in the dc-to-dc converter.

Although many of the described techniques are effective and have been proven for single-ended PAs, in modern telecommunication applications dealing with high peak-to-average power ratio (PAPR) signals, this should be extended to PAs based on topologies with high BO efficiency, such as the Doherty or Outphasing PAs. In fact, the performance degradation and, consequently, the expected correction also depends on the considered PA topology [12], so the following approaches are focused on reducing the performance degradation due to load variations on PA topologies with higher BO efficiency.

Chappidi *et al.* [13] exploit active load pulling in a multiport combiner to improve voltage standing wave ratio (VSWR) tolerance at peak power. For the theoretical analysis, they consider a digital-to-analog converter (DAC)-based PA and a specifically designed two-way combiner. Moreover, the

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nominal output power is set to half of each channel's full power (FP) capability, by using only half of the DAC cells. Then, by turning on or off some of the cells, they are able to compensate the output load of the ON-state cells and, consequently, achieve performance correction for mismatched loads. However, the presented practical implementation is based on a two-cell Doherty-like PA and shows 2 dB of output power and more than 10% of power-added-efficiency (PAE) degradation for a 4:1 VSWR circle. Lyu and Chen [14] present a reconfigurable PA that can work in quasi-balanced DPA (QB-DPA) and balanced modes. The selection between modes is based on the control of a switch at the isolated port of the output quadrature coupler. The amplifier operating in QB-DPA mode was demonstrated to ensure high efficiency across the test loads distributed in a 2:1 VSWR circle. For operation in balanced mode, the linearity is increased for some loads, despite the reduced efficiency. In [15], a digital Doherty PA was presented, where appropriate driving signals are used to reduce the performance degradation under load varying conditions. Driving signals of digital Doherty PAs can be designed to use some power of the peaking amplifier to correct the carrier load, but this will degrade the BO efficiency of the PA and can only compensate for variations toward lower loads. In [16], a reconfigurable series/parallel DPA is designed using adaptive bias voltage sources (for the gate biasing) and a quadrature-coupler-based combining, which includes a switch at the isolation port to change the operation mode. This allows a reconfigurable DPA operation, changing the carrier and peaking roles. The carrier/peaking drain current capability and phases can also be adjusted using switched parallel transistors at the output stage and tunable phase delay lines at the input, respectively. The authors can achieve a worst case output power and FP PAE degradation of 1.7 dB and approximately 10%, respectively, for loads across a 3:1 VSWR circle. Note also that the drain current capability of the carrier/peaking devices is set to approximately half of the maximum value for operation with a 50-Ω nominal load.

In summary, analyzing the described techniques, we can conclude the following.

1) In order to maintain BO performance, the output stage devices' peak current must be reduced for operation under the nominal load.
2) In order to compensate for load variations for both higher and lower (than nominal) loads, it is necessary to include some kind of switched-mode operation at the combiner.
3) For most cases, neither the output power nor the drain efficiency have been completely restored.

This article presents a technique that is able to completely restore the DPA output power for nonoptimal real and complex loads. The drain efficiency is also completely compensated for nonoptimal real loads, while, for complex ones, some degradation is still expected. The peak current of the devices is also reduced for operation under the nominal load, but a typical, static, DPA combiner is used at the output.

This article is an expanded version of [17], in which a load-dependent supply voltage variation was proposed to correct the performance of DPAs operating under nonoptimal loads.

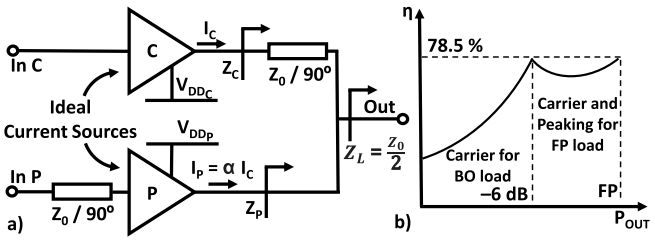

Fig. 1. (a) Ideal two-way symmetrical DPA considered during the theoretical derivations. (b) Ideal efficiency profile of the considered DPA under nominal load operation.

In [17], it was demonstrated that two independent drain voltages should be used for the carrier and peaking devices. It was also shown that, for this correction technique to be effective, the PA should be designed for a different FP load, which must be higher than the devices' maximum power one, resulting in the lower current (and power) for the nominal load. This design case guarantees higher current capability for mismatched loads. Then, by properly controlling the drain voltages of the devices, we achieve reduced load sensitivity. In this expanded version, we go one step further, showing that this correction technique is only effective if the radio frequency (RF) input signals of the carrier and peaking devices are load-dependent. These optimal input signals are derived, presented, and implemented using an analog adaptive input driving stage. The complete system is composed of the DPA output stage, an impedance tracking circuit, a two-channel medium power driving stage, and an adaptive input stage.

This article is organized as follows. Section II presents the theoretical derivation of the optimal carrier and peaking supply voltages and RF input signals for Doherty operation under nonoptimal loads. Section III shows a comparison between a typically designed Doherty, a Doherty designed for a higher nominal load, and the proposed quasi-load insensitive (QLI) one (designed for the higher load and including V_{DD} compensation). Section IV validates the introduced theory with static measurements and load—pull (LP) results of the QLI Doherty prototype. Section V presents the dynamic performance of the system for a fully automated operation under synthesized load variations, using continuous wave (CW) and modulated signal excitations. Finally, Section V summarizes the advantages and drawbacks of the proposed technique.

II. Carrier and Peaking Supply Voltage and Input Signal Theoretical Derivation

This section is devoted to the theoretical derivation of the optimal:

1) load-dependent V_{DD};
2) FP design impedance for the QLI DPA;
3) driving signals for both the carrier and peaking devices.

The presented derivation assumes an ideal two-way symmetrical Doherty PA, as shown in Fig. 1(a), as well as independent V_{DD} sources for the carrier and peaking devices (V_{DD_C} and V_{DD_P}, respectively). Class B operation is assumed, leading to optimal loading of the devices on the real axis.

To maintain the DPA ideal behavior for nonoptimal loads, it is necessary to guarantee that both the BO and FP output

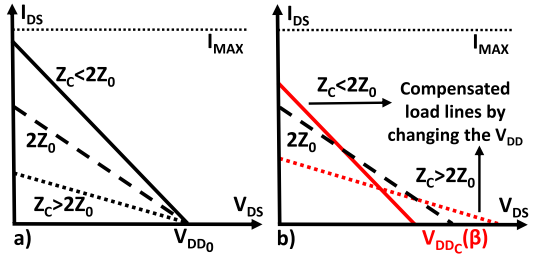

Fig. 2. (a) Uncompensated carrier load lines for three output loads: lower than optimal (continuous), optimal (dashed), and higher than optimal (dotted). (b) Load lines for the same loads when V_{DD} compensation is applied (in red).

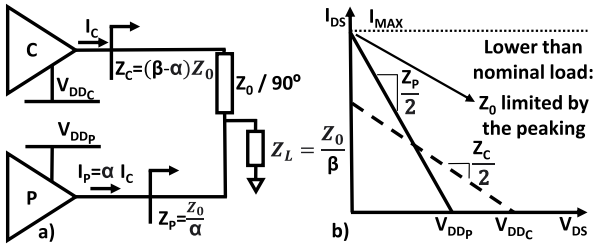

Fig. 3. (a) Considered DPA output combiner and correspondent carrier and peaking impedances. (b) Load lines illustrating the case where Z_0 is limited by the peaking load, for lower than nominal output impedances.

power levels are kept constant. As illustrated in Fig. 1(b), to fulfill this condition, it is necessary to ensure that the maximum output power of the carrier device for the BO load is constant. Moreover, the maximum combined output power of the carrier and peaking devices for their FP loads must also be kept constant and equal to four times (6 dB) the BO output power.

At BO, since the peaking is OFF, the DPA operation is determined by the carrier. When there is an output load change, the voltage and/or current excursions at the intrinsic drain change, as illustrated in Fig. 2(a). Consequently, the output power and efficiency vary, and so, as introduced in [11], we can compensate for these variations by modifying the drain supply voltage, V_{DD_C}, as shown in Fig. 2(b).

The condition for preserving the BO output power level is given by

$$P_{O_C}^{\mathrm{BO}}(\beta) = P_{O_C}^{\mathrm{BO}}(\beta = \beta_0) \tag{1}$$

where β represents the output load variation and is equal to (Z_0/Z_L), Z_0 is the devices' nominal FP load, and Z_L is the DPA output load. Note that, for the nominal operation condition, $\beta = \beta_0 = 2$, which corresponds to $Z_L = (Z_0/2)$.

As known [18], for a piecewise linear current source with an ideal $R_{\mathrm{ON}} = 0$, the saturated output power, $P_O(Z_D)$, for operation with a load, Z_D, higher or equal to the maximum power load (ensuring saturation at the triode region) is given by

$$P_O(Z_D) = \frac{1}{2}\frac{{V_{\mathrm{DD}}}^2}{|Z_D|^2}\mathrm{Re}(Z_D). \tag{2}$$

Note that this expression will be used to calculate the output power of the carrier and peaking PAs in different scenarios, by replacing the generic load, Z_D, with their correspondent output loads. Now, to preserve the BO power, it is possible to further develop (1) using (2) and replace Z_D with the carrier BO load, $Z_C^{\mathrm{BO}}(\beta) = \beta Z_0$

$$\frac{V_{\mathrm{DD}_C}(\beta)^2}{|\beta|^2}\mathrm{Re}(\beta) = \frac{{V_{\mathrm{DD}_0}}^2}{|\beta_0|^2}\mathrm{Re}(\beta_0) \tag{3}$$

where V_{DD_0} is the nominal supply voltage. Note that, as expected from class B terminations, Z_0 is a real impedance. The previous expression can then be solved for $V_{\mathrm{DD}_C}(\beta)$, assuming β_0 real, resulting in

$$V_{\mathrm{DD}_C}(\beta) = \frac{|\beta|}{\sqrt{\beta_0 \mathrm{Re}(\beta)}}V_{\mathrm{DD}_0} \tag{4}$$

which gives the carrier amplifier supply voltage that maintains the BO output power level constant.

As previously introduced, the combined FP of both the carrier ($P_{O_C}^{\mathrm{FP}}$) and peaking ($P_{O_P}^{\mathrm{FP}}$) PAs must also be preserved to ensure the correct DPA operation. This condition can be described as

$$P_{O_C}^{\mathrm{FP}}(\beta) + P_{O_P}^{\mathrm{FP}}(\beta) = 4 \cdot P_{O_C}^{\mathrm{BO}}(\beta = \beta_0). \tag{5}$$

Equation (5) can be further developed using (2), considering the carrier and peaking FP impedances, $Z_C^{\mathrm{FP}}(\beta, \alpha) = (\beta - \alpha)Z_0$ and $Z_P^{\mathrm{FP}}(\alpha) = (Z_0/\alpha)$, respectively, as shown in Fig. 3(a), where $\alpha = (I_P/I_C)$; this results in

$$\frac{V_{\mathrm{DD}_C}(\beta)^2}{|\beta-\alpha|^2}\mathrm{Re}(\beta-\alpha) + V_{\mathrm{DD}_P}(\beta)^2\mathrm{Re}(\alpha) = 4\frac{V_{\mathrm{DD}_C}(\beta)^2}{|\beta|^2}\mathrm{Re}(\beta). \tag{6}$$

Then, to ensure that both devices operate at the on-set of saturation at FP, their voltage excursion should be equal to twice their V_{DD} bias

$$\begin{cases} V_{\mathrm{DD}_P}(\beta) = |I_P| \cdot \left|Z_P^{\mathrm{FP}}(\alpha)\right| \\ V_{\mathrm{DD}_C}(\beta) = |I_C| \cdot \left|Z_C^{\mathrm{FP}}(\beta, \alpha)\right| \end{cases} \tag{7}$$

and so, it is possible to obtain a relationship between $V_{\mathrm{DD}_C}(\beta)$ and $V_{\mathrm{DD}_P}(\beta)$ as

$$V_{\mathrm{DD}_C}(\beta) = V_{\mathrm{DD}_P}(\beta)|\beta - \alpha|. \tag{8}$$

Finally, by replacing the obtained relationship in (6), the following equation is obtained:

$$|\beta| = 2|\beta - \alpha| \tag{9}$$

which can be used in (8) to remove the dependence with α. The obtained expression can then be further developed, using (4), to achieve

$$V_{\mathrm{DD}_P}(\beta) = \frac{2}{\sqrt{\beta_0 \mathrm{Re}(\beta)}}V_{\mathrm{DD}_0} \tag{10}$$

which gives the peaking amplifier supply voltage to maintain the correct DPA operation. The obtained V_{DD} values for the carrier and peaking devices are plotted in Fig. 4, using a V_{DD_0} of 25 V.

Analyzing the carrier and peaking load lines is relevant to understand how these variable supply voltages maintain a constant output power. Fig. 5 presents these load lines for a conventional Doherty (a)–(c) and for the proposed QLI version (d)–(f).

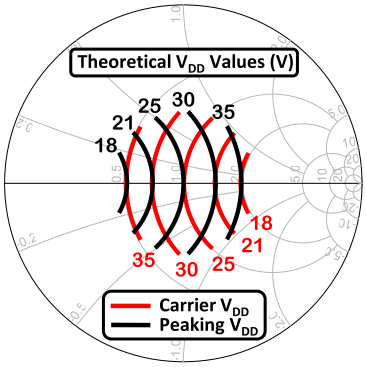

Fig. 4. Theoretical drain voltage values for the carrier and peaking devices for a nominal V_{DD} of 25 V. The Smith chart Z_0 is the nominal design load.

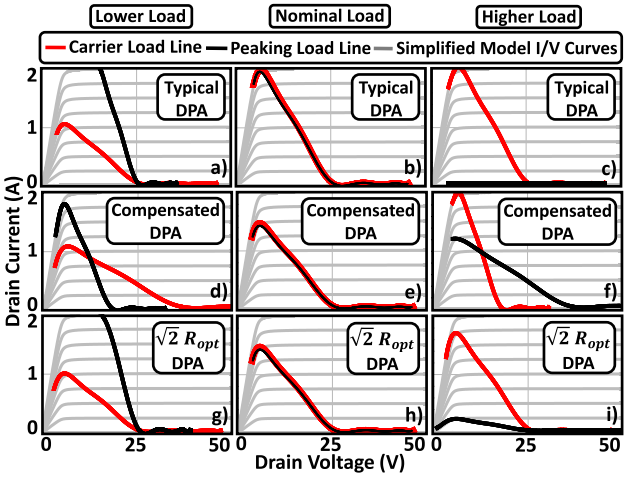

Fig. 5. Load lines of the carrier and peaking devices of the DPA designed for (a)–(c) typical nominal load, (d)–(f) for the optimal nominal load with V_{DD} compensation, and (g)–(i) for the optimal nominal load without V_{DD} compensation. Each of the cases is shown (b), (e), and (h) for operation under the nominal load, (a), (d), and (g) half the nominal load, and (c), (f), and (i) twice the nominal load.

Considering the conventional DPA operating for lower than nominal output impedances (a), the peaking load becomes lower, degrading the efficiency and output power, and the carrier load becomes higher, reducing the output power. For higher output impedances (c), the carrier load becomes lower, degrading the BO efficiency. In this last scenario, the peaking PA is not used because it would LP the carrier to even lower loads, decreasing its output power and efficiency, due to current saturation.

Instead, in the proposed DPA operating for lower than nominal output impedances (d), the carrier load becomes higher, and its maximum current becomes lower. Thus, its V_{DD_C} is increased to maintain the output power. On the other hand, the peaking load becomes lower, and its maximum current becomes higher. Thus, its V_{DD_P} is decreased to keep the device on the on-set of saturation, increasing its efficiency. For higher output impedances (f), the carrier load becomes lower, and its maximum current becomes higher. Thus, its V_{DD_C} is decreased to keep the device on the on-set of saturation, increasing its efficiency. The peaking load becomes higher, and its maximum current becomes lower, and so its V_{DD_P} is increased to guarantee the necessary output power.

As it is also seen in Fig. 5, the load lines of the proposed PA do not reach the maximum current, I_{MAX}, for the nominal load (e). This happens because, as previously introduced, the PA was designed for a higher nominal FP load. In this way, none of the devices becomes current saturated for any load in the VSWR design range. If this is not taken into consideration, the peaking would be current saturated for lower loads (d), and the same would happen to the carrier under operation for higher loads (f). Thus, in order to assure that I_{MAX} is only reached for the worst case loads, it is necessary to calculate the optimal nominal FP load, Z_0. This can be calculated using the load line expression, $|I_{MAX}| = 2V_{DD}/|Z_L|$, with V_{DD} equal to the carrier and peaking derived supply voltages, and $|Z_L|$ equal to their FP impedances, as illustrated in Fig. 3(b) and described by the following equations:

$$\begin{cases} Z_{0_C} = R_{opt}\sqrt{\dfrac{4}{\beta_0 \,.\, \mathrm{Re}(\beta)}} \\ Z_{0_P} = R_{opt}\sqrt{\dfrac{4|\alpha|^2}{\beta_0 \,.\, \mathrm{Re}(\beta)}} \end{cases} \tag{11}$$

where $R_{opt} = 2V_{DD0}/|I_{MAX}|$ is the device's maximum power load [corresponding to the load line shown in Fig. 5(b)].

It is also important to notice that, from (9), we can obtain various solutions for α. However, only the solution $\alpha = (\beta/2)$ guarantees an equal peak current for the peaking and carrier devices at the nominal load. Furthermore, it is also the only alpha that guarantees an equally limited nominal FP impedance, Z_0, for a symmetrical load variation (around the nominal load). Thus, (11) must be calculated using $\alpha = (\beta/2)$. The output impedance, Z_L, used to calculate the β value, should be chosen considering the worst case scenarios, i.e., the output load with higher real part for the carrier expression, Z_{0_C}, and the output load with lower real part for the peaking expression, Z_{0_P}. Thus, for a $\beta_0 = 2$ and a load variation of 4:1 ($(Z_0/4) < Z_L < Z_0$), equivalent to a maximum VSWR of 2.0, the optimal FP load is equal to $\sqrt{2}R_{opt}$. This analysis can be expanded for other mismatch levels, as long as the load variation is centered on the nominal load. For these cases, the optimal Z_0 can be obtained by $\sqrt{x}R_{opt}$, with x being the maximum VSWR considered for correction. Thus, we sacrifice power (i.e., the power that we can obtain for a certain device area operating at the nominal output load) in exchange for the correction radius.

However, it is important to notice that designing the DPA for the calculated FP load is necessary, but not sufficient, to compensate for load variations, as shown in Fig. 5(g)–(i), where the V_{DD} is fixed at the nominal value. It is shown that, for lower loads, the peaking is severely reducing the FP efficiency, and for higher loads, the carrier is reaching the maximum current earlier.

To reach the optimal operation shown in Fig. 5(d)–(f), the designed Doherty PA also requires digital input splitting, i.e., it is driven with different input driving signals for each load. These input signals have been calculated so that the carrier reaches the on-set of saturation for BO and FP, and

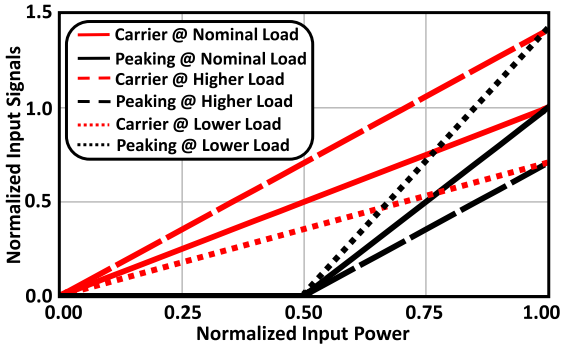

Fig. 6. Optimal input splitting ratio for the nominal load, twice, and half the nominal load.

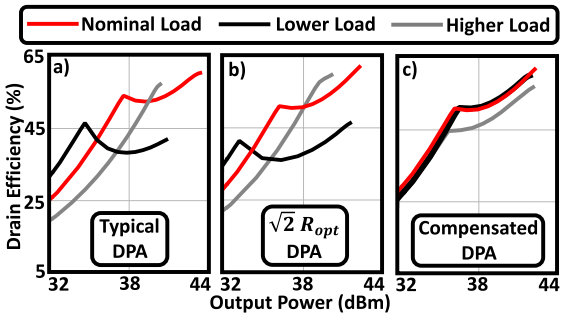

Fig. 7. Drain efficiency profile comparison between the DPA designed (a) for the typical nominal load and for the optimal nominal load without and with V_{DD} compensation, respectively, at (b) and (c).

the peaking also reaches the same condition for FP, ensuring high efficiency.

For the proposed QLI DPA, the peak current of the carrier at BO and FP can be calculated as

$$\begin{cases} \mathrm{IC_{BO}} = \dfrac{2V_{\mathrm{DD}_C}}{|\beta| Z_0} \\ \mathrm{IC_{FP}} = \dfrac{2V_{\mathrm{DD}_C}}{|\beta - \alpha| Z_0} \end{cases} \tag{12}$$

where $|\beta - \alpha|$ is equal to $(|\beta|/2)$ [from (9)]. Consequently, the FP peak current becomes twice the BO value, resulting in linear driving signals.

The peaking FP current is calculated as

$$\mathrm{IP_{FP}} = \frac{2V_{\mathrm{DD}_P}}{\frac{Z_0}{|\alpha|}} \tag{13}$$

where $\alpha = (\beta/2)$, as previously explained.

From the peak currents that have been calculated and knowing the transconductance, g_m, of the used devices, the optimal driving signals' amplitude was obtained and is shown in Fig. 6. Finally, since $\alpha = (\beta/2)$, $\beta = (Z_0/Z_L)$, and $\alpha = (I_P/I_C)$, the input driving signals phase should be

$$\angle V_{\mathrm{in}_P} - \angle V_{\mathrm{in}_C} = -\angle Z_L + \Phi \tag{14}$$

where Φ is the required input phase delay to align the carrier and peaking currents at the combiner node, i.e., compensate for the different phase lags between the peaking and carrier input matching networks (IMNs), OMNs, and imposed by the different biasing of the devices.

III. Simulated Performance Improvement

Fig. 7 presents the simulated drain efficiency of various DPAs: 1) the conventional DPA designed for the typical nominal load, R_{opt}; 2) the DPA designed for the optimal nominal load, $\sqrt{2}R_{\mathrm{opt}}$, with a fixed V_{DD}; and 3) the DPA designed for the optimal nominal load and with V_{DD} compensation (QLI DPA). Please note that, within this section, the presented DPA designs are based on a real transistor model, but their matching networks are based on ideal S-parameter blocks.

The conventional PA has a typical DPA efficiency shape and an output power of 43.1 dBm for the nominal load. However, for lower loads, its output power is degraded, and the efficiency is reduced, both at FP and BO. For higher loads, its output power is also degraded, and the BO efficiency is extremely reduced. For this case, the efficiency shape changes drastically, becoming similar to the one of a single-ended PA. The amplifier that was designed for the FP load of $\sqrt{2}R_{\mathrm{opt}}$, but operates for a fixed V_{DD}, presents a lower output power of 42.3 dBm for the nominal load. For lower loads, its output power is degraded, its efficiency is reduced, and the BO level increases. For higher loads, the output power is also decreased, and the DPA efficiency shape is lost, degrading the BO efficiency. Thus, comparing the amplifier designed for the nominal load of $\sqrt{2}R_{\mathrm{opt}}$ with the typical case, the output power relative reduction is mitigated, but the worst case value is lower. In terms of efficiency, for lower loads, the degradation is smaller at FP, and for higher loads, the efficiency shape is slightly less degraded. The proposed PA, with V_{DD} compensation, also delivers a lower output power of 42.3 dBm for operation under the nominal load but maintains its efficiency profile for nonoptimal loads, guarantying higher BO efficiency and constant maximum output power.

TABLE I
Summarized LP Performance Comparison for the Three PAs

	Worst-case $\mathrm{P_{out}}$ (dBm)	$\mathrm{P_{out}}$ Degradation (dB)	Wors-case FP eff. (%)	Worst-case BO eff. (%)
Typical PA	40.6	2.5	43	29
$\sqrt{2}\mathrm{R_{opt}}$ PA	40.4	2	49	33
Comp. PA	**42.3**	**0.3**	51	**45**

The LP contours presented in Fig. 8 compare the performance of the DPA designed for the typical load (black) and the proposed QLI version (red). These two cases correspond to the cases already presented in Fig. 7(a) and (c), respectively. In Fig. 9, the presented LP contours correspond to the PA that was designed for the optimal nominal load of $\sqrt{2}R_{\mathrm{opt}}$, without V_{DD} compensation (black) and the proposed QLI PA (red), which corresponds to (b) and (c) PAs of Fig. 7, respectively. The performance of the three presented cases is summarized in Table I for mismatched loads up to a VSWR of 2.0.

From the analysis of the presented simulation results, it is concluded that the proposed QLI DPA is able to maintain its efficiency profile and the output FP for all the tested loads.

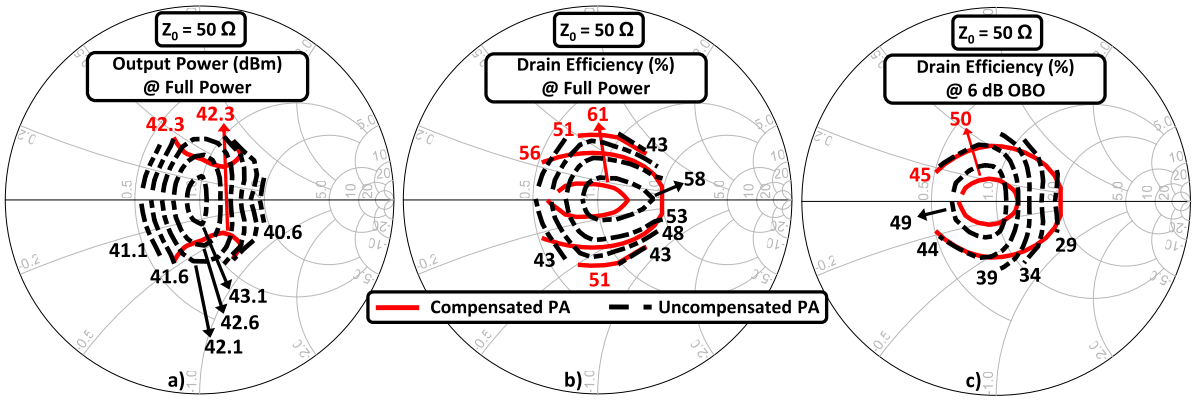

Fig. 8. Simulated LP comparison between the V_{DD} compensated DPA and the DPA designed for the typical FP load (R_{opt}) without V_{DD} compensation. The output power and efficiency at FP are presented in (a) and (b), respectively, and the 6-dB OBO drain efficiency in (c).

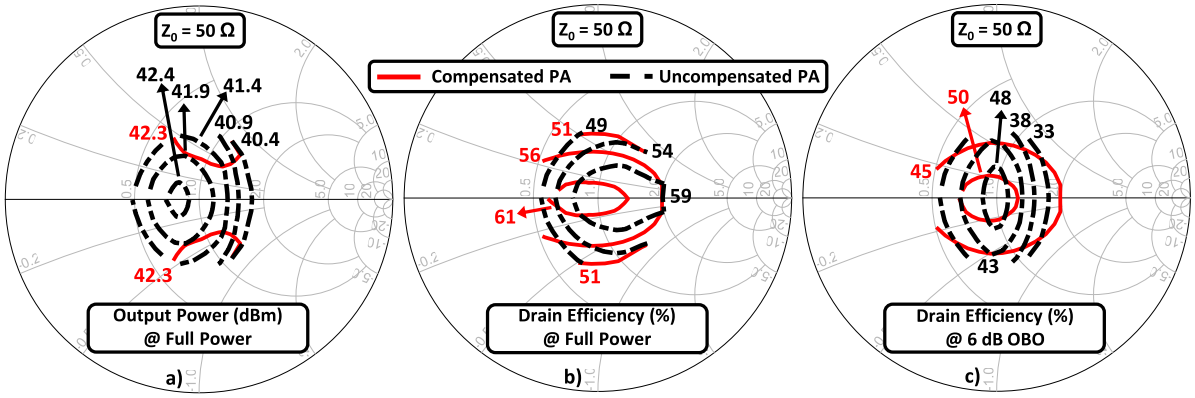

Fig. 9. Simulated LP comparison between the V_{DD} compensated DPA and the DPA designed for the same load ($\sqrt{2}R_{opt}$) but without V_{DD} compensation. The output power and efficiency at FP are presented in (a) and (b), respectively, and the 6-dB OBO drain efficiency in (c).

The efficiency value is slightly degraded for complex loads, as expected. Nonetheless, the worst case output power of the QLI DPA is almost 2 dB higher than it is for any of the uncompensated cases and almost 15% more efficient at BO.

IV. System Architecture and Static Experimental Validation

In this section, a QLI DPA prototype, designed using the derived theory, is presented. Various static measurements characterizing the operation with different loads are also shown, with the objective of testing the performance under load varying scenarios that can happen in various applications, as described in Section I. The system was designed for 3.6 GHz and is shown in Fig. 10. It is composed of the DPA output stage, a medium power two-channel driver, an adaptive input splitting predriver stage, and also an impedance measurement circuit. The impedance measurement stage was already extensively described and presented in [19].

The DPA output stage is based on two Wolfspeed CGH40010F devices biased with a nominal V_{DD_0} of 25 V. Both devices operate with class B harmonic terminations, the carrier is biased with 25 mA of quiescent current (1.2% of I_{MAX}), and the peaking is in shallow class C. The amplifier was designed to present the optimal impedance of $\sqrt{2}R_{opt}$ at the devices' intrinsic current source plane, in FP,

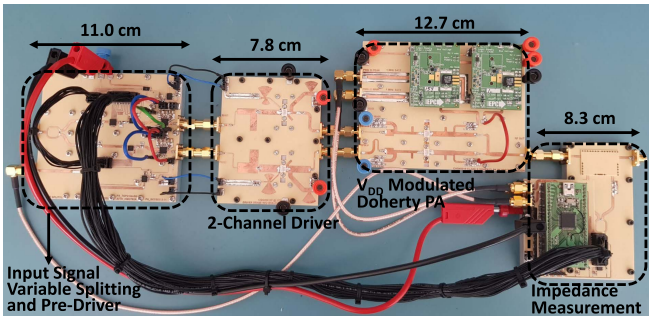

Fig. 10. Implemented DPA system with input splitting control and impedance tracking. The dimensions of each stage are displayed in cm.

for an output load of 50 Ω. This DPA stage was also designed to present real impedances at the devices' intrinsic current source planes for real load impedances. This allows us to obtain the load-dependent V_{DD} values directly from the theory presented in Section II, from load measurements at the PA output port. In order to change the drain supply voltage of both devices, two dc-to-dc gallium nitride (GaN) buck converters from EPC, based on EPC8009 transistors and supplied by the same voltage source, were also added to the design. Note that, although we have used commercial dc-to-dc converters, for the required frequencies, they can be designed to be very compact and efficient. Please also note that, as shown in Fig. 4,

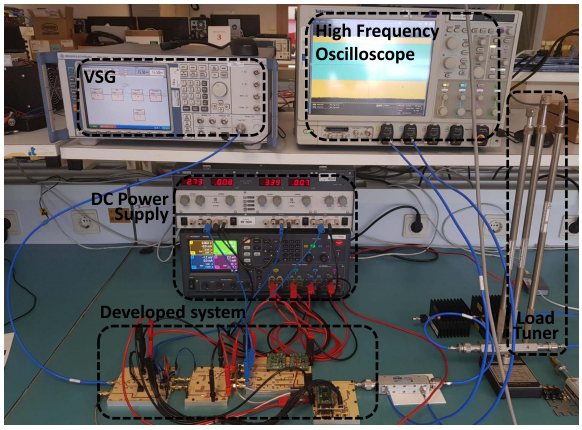

Fig. 11. Measurement setup, including the stub-based manual load tuner that was used to synthesize nonoptimal loads.

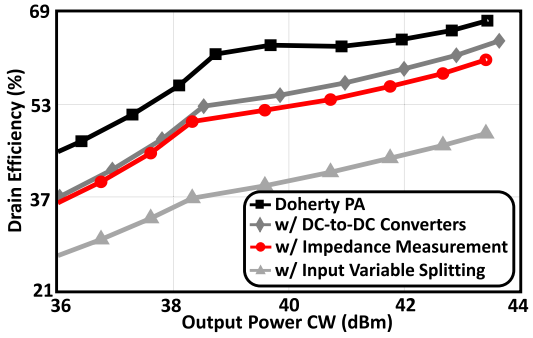

Fig. 12. Drain efficiency of the DPA alone, including the dc-to-dc converters, the dc-to-dc converters and impedance tracking circuit, and all the previous plus the variable input splitting circuit.

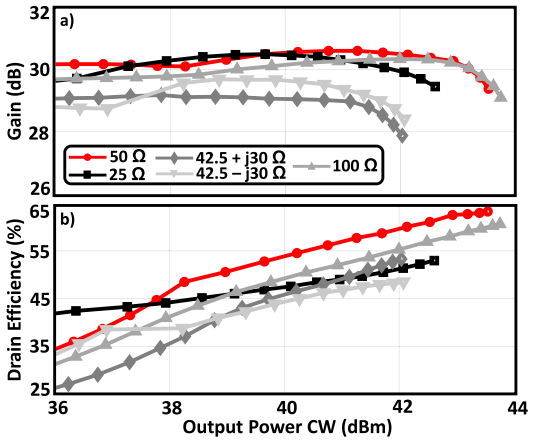

Fig. 13. (a) Measured gain and (b) drain efficiency of the complete DPA (excluding the power dissipated at the driving stage) for various output loads without V_{DD} compensation. We present two traces (gain and efficiency) for each load, which corresponds to one specific color and symbol as represented in the plot legend.

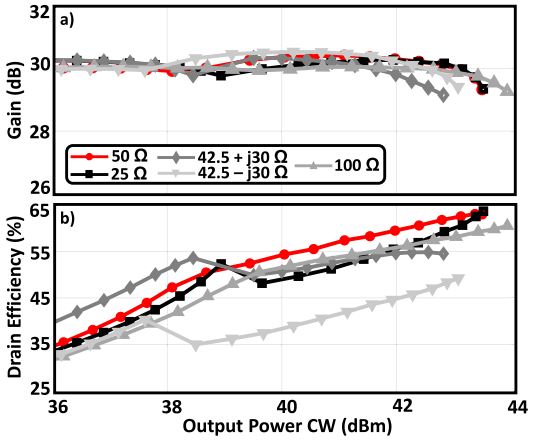

Fig. 14. (a) Measured gain and (b) drain efficiency of the complete DPA (excluding the power dissipated at the driving stage) for various output loads with V_{DD} compensation. We present two traces (gain and efficiency) for each load, which corresponds to one specific color and symbol as represented in the plot legend.

for the worst case loads, the drain voltage of the devices is increased above their recommended nominal voltage of 28 V. However, since the PA is not expected to operate for long amounts of time under extreme mismatched loads, this should not significantly affect the devices' reliability, especially for modern GaN devices with breakdown voltages of 120 V. If, for some application/reason, it is necessary to operate under higher mismatch levels, the nominal voltage (V_{DD_0}) should be reduced trading between load compensation zone and required device area, for a specific output power.

The medium power driving stage is composed of two independent drivers, for the main and peaking channels. It was also designed using two Wolfspeed CGH40010F devices. However, since the required maximum output power is lower than it is at the output stage, the devices are biased at 17 V, ensuring high efficiency. This stage has three purposes: 1) amplify the input signals to the required level; 2) change the peaking turn-on point, using a load-dependent gate bias voltage for the peaking driver; and 3) isolate the input and output stages since the drivers were designed for the impedance presented by the main and peaking output amplifiers, and their IMNs present 50 Ω to the input stage.

The input stage is composed of a Wilkinson power divider, a phase shifter from Qorvo (TGP2108-SM), two variable attenuators from Analog Devices (HMC792ALP4E), and also two amplifiers from Skyworks (SKY66313-11). This stage is used to split the input signal for the carrier and peaking channels and to preamplify each channel. Moreover, it includes an adaptive phase and amplitude relation between the two channels, which can be modified according to the output load to implement the optimal input driving signals. The common-mode amplitude is also controllable to keep the amplifier gain constant with load variations. Please note that this input variable splitting is performed automatically by the fabricated system, and it is controlled by the impedance measurement system using real-time load measurements.

The PA was measured using the setup shown in Fig. 11. Since the complete PA has a single input, the input RF signal was generated using a single channel vector signal generator (VSG). A high-frequency oscilloscope was used to sample the incident and reflected waves at the output of the PA in order to measure the delivered power. Finally, a manual load tuner from Weinschel Associates was used to synthesize various output loads.

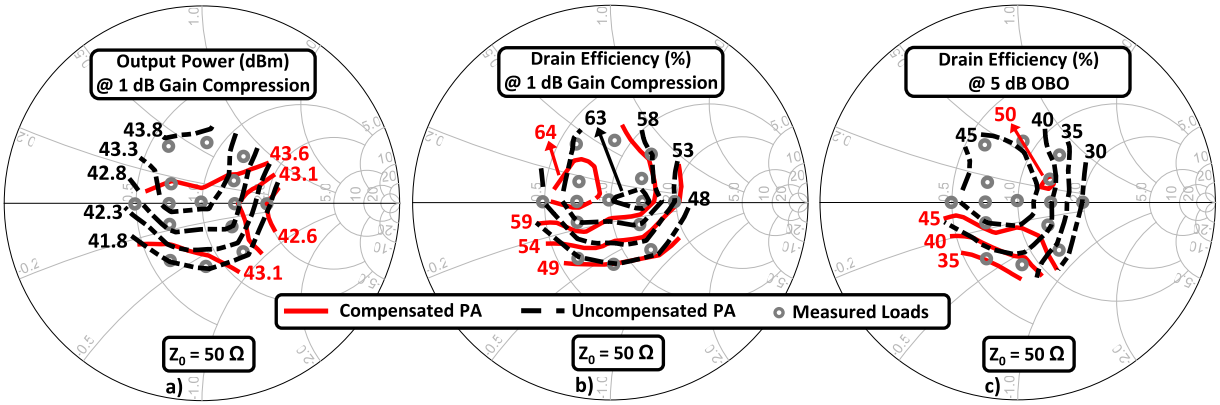

Fig. 15. Measured LP comparison between the V_{DD} compensated DPA and the DPA designed for the same load but without V_{DD} compensation. The output power and efficiency at FP are presented in (a) and (b), respectively, and the BO drain efficiency in (c).

In order to validate the Doherty behavior of the PA and check the impact of its various stages on the compound efficiency, it was first measured for operation with the nominal output load of 50 Ω. Fig. 12 shows the drain efficiency profile of the PA. The BO level is almost 6 dB, as expected for a symmetrical Doherty. The DPA output stage, in black (squares), shows efficiency of 62% and 68% at BO and FP, respectively. The dark gray plot (diamonds) presents the efficiency of the output stage, including the used dc-to-dc converters, and the efficiency is reduced to 53% at BO and 64% at FP. Including the impedance measurement circuit at the PA output further reduces the efficiency by around 3%, due to the added insertion loss, as shown by the red plot (circles). In light gray (triangles), the efficiency of the PA including the dc-to-dc converters, the impedance measurement circuit, and also the power dissipated in the driver and predriver stages is shown. Accounting for the power dissipated in the driving stages corresponds to an efficiency reduction of 12%, both at FP and BO. The drain efficiency presented in the following tests corresponds to the red plot, which includes only the dc-to-dc converters and the impedance measurement circuit. The input driving stage is excluded as it was not designed for high efficiency and is not mandatory to validate the presented technique. Moreover, most of the dissipated power comes from the predriver, whose objective is to increase the gain of the PA, and so, it would also be necessary for the typical DPA without V_{DD} compensation.

Fig. 13 shows the measured gain and drain efficiency of the fabricated PA for various loads without V_{DD} compensation. This case corresponds to the "$\sqrt{2}R_{opt}$ PA" of Section III, which was designed for the calculated load of $\sqrt{2}R_{opt}$ but operates for a fixed V_{DD}. In this case, as expected, the PA output power capability and BO level are not maintained for nonoptimal loads. The nominal load of 50 Ω is shown in red (circles) and presents an output power capability of around 43.5 dBm and a BO level of more than 5 dB with an efficiency above 46%. For the worst case load, which corresponds to the higher load of 100 Ω, in dark gray (diamonds), the amplifier is only capable of delivering 42 dBm, the Doherty efficiency profile is degraded, and the efficiency at BO is greatly reduced (below 30%). For lower loads, such as 25 Ω, shown in black (squares), the amplifier is still not able to deliver the required output power (43 dBm), and the efficiency is higher at BO, but it is degraded by around 10% at FP.

TABLE II
SUMMARIZED MEASURED LP PERFORMANCE COMPARISON FOR THE TWO PAS

	Worst-case P_out (dBm)	P_out Degradation (dB)	Wors-case BO eff. (%)	Worst-case FP eff. (%)
$\sqrt{2}R_{opt}$ PA	41.8	2	30	48
Comp. PA	**42.6**	**1**	35	49

Fig. 14 presents the measured efficiency and gain of the amplifier applying the derived V_{DD} compensation theory and optimal input signals. For these measurements, the common-mode amplitude of the input signals is also load-dependent in order to keep the small-signal gain constant and equal to 30 dB. For this amplifier, the gain and efficiency profiles are similar to the optimal ones obtained for the nominal load of 50 Ω. The worst case, in terms of the maximum delivered power, is still the 100-Ω load, in dark gray (diamonds), but, now, the amplifier can reach more than 42.5 dBm (whereas, without V_{DD} compensation, it was only 42 dBm). The efficiency is degraded for loads with lower imaginary parts, as $42.5 - j30$ Ω, in light gray (nablas); however, for loads with high imaginary part, the behavior is correctly compensated. This indicates that there may have been some inaccuracy in the manufacturing process, and so the optimal load of the fabricated amplifier can be slightly deviated from 50 Ω.

The LP contours for both amplifiers are plotted, for the 1-dB gain compression point in Fig. 15, and their performance is summarized in Table II. From these measurements, it is concluded that there is a significant improvement in the output power capability of the DPA (up to 1.3 dB). The DPA worst case efficiency is almost the same with and without compensation, as shown in Table II. However, for most of the loads, there is also a great efficiency improvement, such as, for example, for higher real loads, where the BO efficiency is improved from 30% to almost 50%. As previously mentioned,

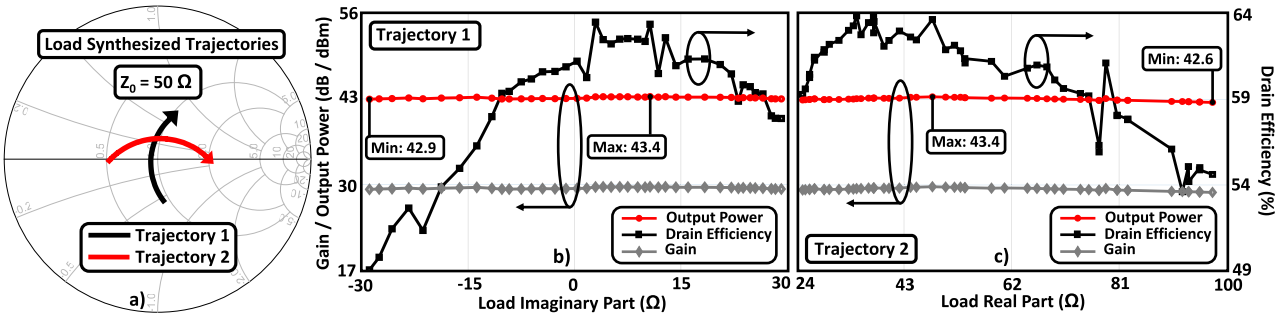

Fig. 16. DPA system performance under a continuous load variation. The load trajectories 1 and 2, in (a), correspond to plots (b) and (c), respectively. (b) and (c) Output power, gain, and efficiency over the synthesized load variations.

the QLI DPA presents these lower efficiency values for a restricted area of the Smith chart, where the compensation method was not able to restore the DPA efficiency shape, probably due to some deviation on the amplifier's nominal load.

V. Dynamic Characteristics Under Output Load Variation

This section presents the DPA CW performance under continuous load variations. During these load sweep measurements, the RF input level is kept constant, and the amplifier is automatically adjusting both supply voltages, as well as the input signal splitting. The operation with modulated signals excitation is also presented for various nonoptimal loads.

Fig. 16 presents the measured data during the load sweep tests. In Fig. 16(a), two load trajectories are presented: the first one, in black, along the 50-Ω real part circle, corresponds to the data of Fig. 16(b); the second one, in red, along the real axis, corresponds to the data shown in Fig. 16(c). Because of the time limitations on the measurement setup, namely, on the oscilloscope acquisition time, the load trajectories presented here have a duration of some seconds. However, the used microcontroller and dc-to-dc converters are capable of performing this compensation at the tens of milliseconds range, [11]. Note that, since the input excitation is constant, the output power and gain variations are equal.

During the first load sweep, the output power varies between 42.9 dBm, for the first loads with lower imaginary parts, and 43.4 dBm, for the loads closer to 50 Ω. This validates the load measurement and automatic adaptation performed by the PA since the performance is similar to what was expected from the LP presented in Fig. 15. The efficiency is also very similar, varying between 49% and 63%.

In Fig. 16(c), the load variation starts at the lower real values and moves toward the higher real values. Consequently, the output power varies between 43.4 and 42.6 dBm, reaching its minimum for the loads around 100 Ω. The efficiency is higher during this test, varying between 54% and 64%, since the load imaginary part does not pass through low negative values.

Now, the performance of the fabricated prototype under modulated signal excitation is presented. For these measurements, a long-term evolution (LTE)-like signal with 5 MHz of bandwidth and 5.5 dB of PAPR was used. The prototype was

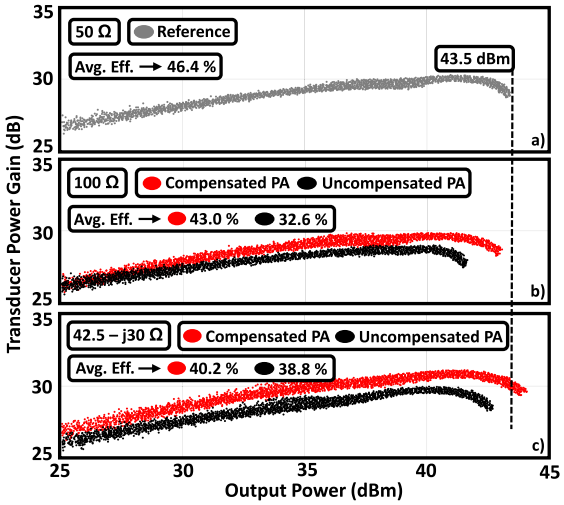

Fig. 17. Dynamic transducer power gain of the fabricated prototype with and without V_{DD} compensation for operation with modulated signal excitation under various output loads. The reference, for a 50 Ω load, in (a). For nonoptimal loads of 100 and 42.5 - j0 Ω, in (b) and (c), respectively.

measured for the nominal load of 50 Ω, which is the reference for comparison with other loads, and also for 100 and $42.5 - j30$ Ω, which are the worst case loads both in terms of output power and efficiency, as seen in the LP presented in Fig. 15. Note that the gain compression is the same for all the presented measurements, guaranteeing a fixed PAPR of the output signal of the amplifier.

In Fig. 17(a), the dynamic gain of the DPA for the reference load is presented, with a peak output power of 43.5 dBm and average efficiency of 46.4%. Then, in Fig. 17(b), the dynamic gain is shown for the 100-Ω load. As expected from the CW characterization, by using the proposed technique, the peak output power level is almost completely restored, and the average efficiency is increased by more than 10%. For the $42.5 - j30$ Ω load, as shown in Fig. 17(c), the output power is completely restored, and the average efficiency is maintained.

In Fig. 18, the phase shift of the implemented prototype with and without V_{DD} compensation is presented for the same three loads. From these plots, the output power compensation is also evident, but a slightly higher phase dispersion is noticed for the compensated amplifier.

In Fig. 19, the spectra of the DPA output signal are shown for the reference load of 50 Ω and for a nonoptimal load of 100 Ω. By comparing the spectra of the amplifier operating

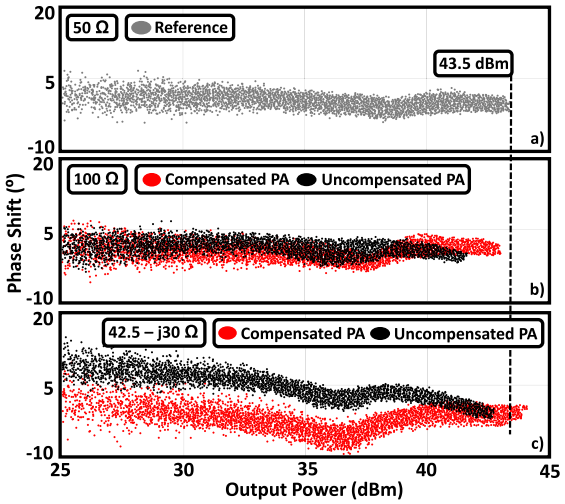

Fig. 18. Dynamic phase shift of the fabricated prototype with and without V_{DD} compensation for operation with modulated signal excitation under various output loads. The reference, for a 50 Ω load, in (a). For non-optimal loads of 100 and 42.5 - β0 Ω, in (b) and (c), respectively.

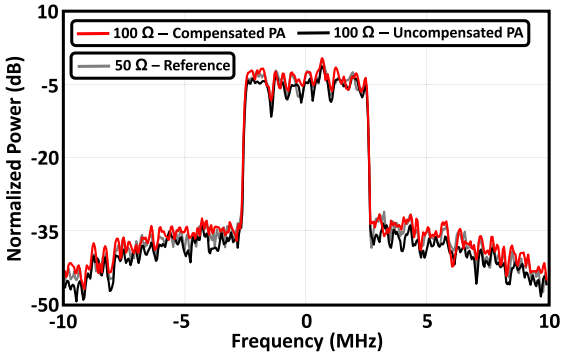

Fig. 19. Spectra of the DPA output signal for three different scenarios. The reference case, where the amplifier operates for a nominal 50-Ω output load, in gray. The case where the amplifier operates for a nonoptimal output load of 100 Ω, with and without V_{DD} compensation, in red and dark, respectively.

TABLE III
SUMMARIZED RAW ACPR AND NMSE OF THE DPA FOR DIFFERENT LOADS, WITH AND WITHOUT V_{DD} COMPENSATION

Load (Ω)	ACPR (dB) High Band	ACPR (dB) Low Band	NMSE (dB)
50 (reference)	-31.8	-32.6	-25.3
100 (w/o compensation)	-32.6	-32.9	-26
100 (w/ compensation)	-31.4	-32.1	-25.1
42.5-j30 (w/o compensation)	-28.8	-29.8	-22.8
42.5-j30 (w/ compensation)	-30.1	-30.9	-23.9

for an output load of 100 Ω, with and without V_{DD} compensation, it is concluded that the system linearity is not degraded by using the proposed technique. Moreover, in Table III, the raw (i.e., uncorrected) adjacent channel power ratio (ACPR) and normalized mean squared error (NMSE) values are shown, before and after compensation, for two different nonoptimal output loads, showing that the proposed technique does not degrade the linearity.

VI. CONCLUSION

In this article, a technique capable of improving the performance of a two-way symmetrical DPA operating for nonoptimal loads was presented. The optimal load-dependent V_{DD} voltages and input signals for the carrier and peaking devices were derived. The required devices' nominal design load for the compensation method to be effective was also shown to be $\sqrt{2}R_{opt}$, for load variations inside a maximum VSWR circle of 2.0. In the simulation, the proposed method has been shown to completely restore the DPA output power capability and efficiency profile, showing an improvement of 1.7 dB on the amplifier's worst case output power and 15% on its BO efficiency. The experimental validation was performed on a 3.6-GHz symmetrical DPA with a maximum nominal output power of 43.5 dBm and 5.1 dB of OBO with a drain efficiency above 50%. The tested system was composed of a DPA output stage, featuring a load-dependent adaptive supply voltage control, an impedance measurement circuit, and an input driving stage capable of implementing load-dependent amplitude and phase adjustments on the carrier and peaking channels. This system proved to be capable of automatically tracking load variations and correct the output stage amplifier's performance. The worst case measured output power capability of the PA was improved up to 1.3 dB and the BO efficiency by almost 20% using the proposed compensation method for loads varying inside a 2.0 maximum VSWR circle. Under modulated signal excitation, the PA peak output power was improved by 1.4 dB and the average efficiency by more than 10% for the worst case loads.

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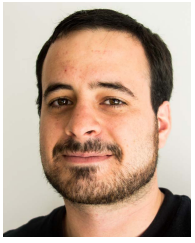

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