

# Loss Reduction in Substrate Integrated Waveguide Structures

Pejman Mohammadi<sup>1,\*</sup> and Şimşek Demir<sup>2</sup>

**Abstract**—A method for decreasing the loss in substrate integrated waveguide (SIW) structures is introduced. In this method, the dielectric substrate is partially removed. Accordingly, dielectric loss reduction has been explicated analytically. Its equivalence to the rectangular waveguide of solid walls which is partially filled with dielectric has been identified. A novel topology for demonstrating the idea is established and a low loss three port substrate integrated waveguide power divider is presented. This SIW power divider shows lower loss than conventional SIW power dividers. Proper TRL standards are realized for removing the effect of transition and/or matching sections in measurement process. For a low-loss three-port PSIW power divider, the return loss below 10 dB and transmission coefficients between  $-3$  dB to  $-3.5$  dB from 8.75 GHz to 10 GHz have been achieved. The measured amplitude imbalance is less than  $\pm 0.2$  dB, and the measured phase difference between  $\angle S_{21}$  and  $\angle S_{31}$  is about  $4^\circ$  in the same frequency band.

## 1. INTRODUCTION

Compact and low-loss integrated components are key elements in the design of telecommunication systems, which operate in the microwave and millimeter-wave frequency ranges. Although metallic waveguides have been widely adopted, their weight, size and integration issues with planar structures make them less practical. Substrate integrated waveguide (SIW) is an interesting alternative that alleviates the mentioned problems. Similar to the metallic rectangular waveguide (RW), it is an electromagnetic interference free component. Lower design and production cost, and easier integration with microwave and millimeter wave components and keeping the insertion loss lower in common are the main advantages of SIW.

SIW concept and its integration with planar structures have been investigated thoroughly [1–4]. One of the major issues with the SIW application in the millimeter wave component design is its losses. The study of SIW loss mechanisms shows that these structures suffer from ohmic, radiation and dielectric losses [5, 6]. Incomplete shielding of the gaps between vias results in the radiation loss from the possible leaking waves. The ohmic loss is related to finite conductivity of metal walls, and loss tangent of dielectric material leads to dielectric loss.

It is shown in [5] that minimum losses have been accomplished with the vias that have large diameter and are close together. Dielectric loss is the major source of loss in SIW and is significantly larger than the two other losses. Decreasing the dielectric loss has significant contribution to decreasing the total dissipated power in SIW. The main idea in order to achieve the lowest dielectric loss is using air instead of dielectric substrate as the transmission medium in SIW. Removing the dielectric substrate in middle part of the SIW as illustrated in Fig. 1 is a desired method to reducing the dielectric loss.

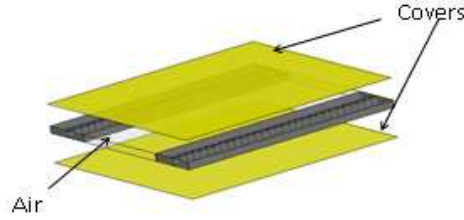
Partially filled SIW (PSIW) in Fig. 1 consists of air in the middle part and two substrate parts on the sides. It is covered by two metal plates as top and bottom walls of the waveguide. In PSIW structure, the transmission medium is composed from combination of air and dielectric material. As shown in Fig. 1, most part of the structure is air, and there are two small dielectric parts in the corners.

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\* Corresponding author: Pejman Mohammadi (pe.mohamady@gmail.com).

<sup>1</sup> Department of Electrical and Electronic Engineering, Urmia Branch, Islamic Azad University, Urmia, Iran. <sup>2</sup> Department of Electrical and Electronic Engineering, Middle East Technical University, Ankara, Turkey.



**Figure 1.** Proposed substrate integrated waveguide.

Therefore, the dielectric loss reduction is expected. The equivalent RW of SIW is a well acknowledged method for modelling the SIW. Hence the PSIW structure can be modelled as a partially filled RW. This model is used for analyzing the PSIW. The propagation constant and dielectric loss are computed in section 2. Then a low-loss SIW with this technique is designed and fabricated, and a low-loss power divider is manufactured. Power dividers are one of the key elements in microwave and millimeter wave systems. However, available SIW power dividers [7–9] in the multi-way port environment suffer from large size due to the lateral port distribution and loss problems. In the available SIW power dividers [10–13], the size problem has been improved by stacking the layers, but the loss problem still exists. In our proposed PSIW power divider, both problems have been investigated and improved.

Firstly, the size reduction is achieved by stacking the proposed PSIW power divider layers. Therefore, by increasing the number of ports, only the length of the structure increases, and its width remains unchanged. Secondly, insertion loss is decreased by removing the dielectric. Comparison of the  $S$ -parameters of this power divider with similar power dividers shows that the total loss is decreased due to decrease in the dielectric loss. The low profile property of SIW is utilized in [11] by developing a multilayer structure, which is similar to the presented configuration in the current study. However, the proposed method is very straightforward for applications like antenna array feed network.

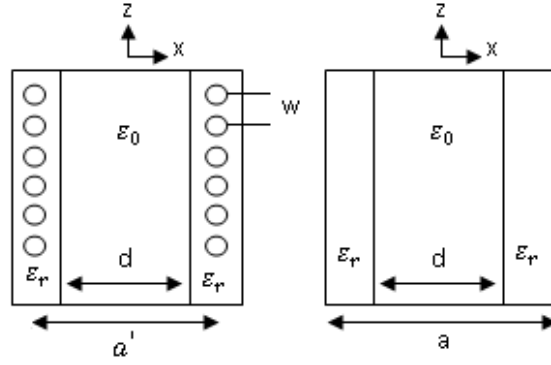
In order to set up a measurement on SIW structure, tapered transition parts should be used [1]. These parts can affect the loss property of the structures. Measuring the whole structure without transition parts is a matter of concern. This leads us to the use of Thru-Reflect-Line (TRL) calibration technique. So in the light of appropriate PSIW TRL standards, the undesired effects of transition parts are removed.

## 2. DIELECTRIC LOSS IN PSIW

The RW equivalent of SIW is a well-known concept. By a similar approach a partially filled RW can be used as the equivalent for PSIW. It is developed by using the link between the surface impedance of the two structures. The surface impedance of SIW at the side walls was calculated [16]. The side walls of the PSIW are the same as the SIW implemented with metallized via. For partially filled rectangular waveguide, the impedance can be calculated by transverse  $E$  field and  $H$  field components. The propagation constant will be found by using boundary conditions. Then dielectric loss of the equivalent partially filled RW can be analytically computed. A top view of a PSIW and its equivalent RW are shown in Fig. 2.

For  $TE_{10}$  mode propagation in a rectangular waveguide, field expressions are as follows [14]:

$$\begin{aligned}
 E_x &= 0 & H_x &= \frac{1}{\hat{z}} \left( \frac{\partial^2}{\partial x^2} + k^2 \right) \Psi \\
 E_y &= -\frac{\partial \Psi}{\partial z} & H_y &= \frac{1}{\hat{z}} \frac{\partial^2 \Psi}{\partial x \partial y} \\
 E_z &= \frac{\partial \Psi}{\partial y} & H_z &= \frac{1}{\hat{z}} \frac{\partial^2 \Psi}{\partial x \partial z} \\
 \hat{z} &= j\omega\mu
 \end{aligned} \tag{1}$$



**Figure 2.** Top view of PSIW and its equivalent RW.

$$\begin{aligned} \Psi &= A \sin k_{x1} \left( \frac{a}{2} + x \right) \cos(k_{y1}y) e^{-jk_z z} & \text{if } -\frac{a}{2} \leq x \leq -\frac{d}{2} \\ &B \cos(k_{x0}x) \cos(k_{y0}y) e^{-jk_z z} & \text{if } -\frac{d}{2} < x < \frac{d}{2} \\ &A \sin k_{x1} \left( \frac{a}{2} - x \right) \cos(k_{y1}y) e^{-jk_z z} & \text{if } \frac{d}{2} \leq x \leq \frac{a}{2}. \end{aligned} \quad (2)$$

$k_{x1}$  and  $k_{y1}$  are the propagation constant of the dielectric part in  $x$  and  $y$  direction, respectively.  $k_{x0}$  and  $k_{y0}$  are related to the air part of PSIW. The surface impedance of the structures is given as follows [15]:

$$\eta_{s0} = \frac{j\omega\mu W}{4} \ln \frac{W}{4R} \quad (3)$$

in which  $R$  is the radius of cylinder and  $W$  the space between two cylinders and  $\omega = 2\pi f$ . The surface impedance for RW is:

$$\eta_s = \frac{E_y}{H_z} \quad \text{at } x = \frac{a'}{2} \quad (4)$$

$$E_y = -\frac{\partial \Psi}{\partial z} = jk_z \Psi \quad (5)$$

$$H_z = \frac{1}{\hat{z}} \frac{\partial^2 \Psi}{\partial x \partial z} = -jk_z \frac{1}{\hat{z}} \frac{\partial \Psi}{\partial x}$$

Then,  $\eta_s$  of RW can be calculated by using (4) and (5). The equality  $\eta_{s0} = \eta_s$  gives:

$$\begin{aligned} \frac{W}{4} \ln \frac{W}{4R} &= \frac{1}{\sqrt{(\omega^2 \mu \epsilon - k_z^2)}} \tan \left( \frac{(a-a')}{2} \sqrt{(\omega^2 \mu \epsilon - k_z^2)} \right) \\ \frac{W}{4} \ln \frac{W}{4R} &= C \end{aligned} \quad (6)$$

$C$  is a constant because after designing the SIW the value of  $R$  and  $W$  are constant. Boundary condition will be applied as follows:

$$E_z(y=0, b) = 0 \quad k_{y1} = k_{y0} = \frac{n\pi}{b} \quad n = 0, 1, 2, \dots \quad (7)$$

$b$  is height of PSIW. Continuity of fields at  $x = \frac{d}{2}$ :

$$E_y \left( x = \frac{d}{2} \right) \Rightarrow A \sin \left( k_{x1} \frac{(a-d)}{2} \right) = B \cos \left( k_{x0} \frac{d}{2} \right) \quad (8)$$

$$H_y \left( x = \frac{d}{2} \right) \Rightarrow k_{x1} \cos \left( k_{x1} \frac{(-d+a)}{2} \right) = B k_{x0} \sin \left( k_{x0} \frac{d}{2} \right) \quad (9)$$

from (8) and (9)  $\Rightarrow$

$$k_{x1} \cotan \left( k_{x1} \frac{(a-d)}{2} \right) = k_{x0} \tan \left( k_{x0} \frac{d}{2} \right) \quad (10)$$

$$k_1^2 = \omega^2 \mu \epsilon = k_z^2 + k_{y1}^2 + k_{x1}^2 \quad (11)$$

$$k_0^2 = \omega^2 \mu_0 \epsilon_0 = k_z^2 + k_{y0}^2 + k_{x0}^2 \quad (12)$$

it is known that  $k_{x1}$  and  $k_{x0}$  are the wavenumbers in dielectric substrate and free space, respectively. For  $TE_{10}$  mode ( $n=0$ )  $k_{y1} = k_{y0} = 0$ , so by using (10), (11) and (12) one can write:

$$\sqrt{\omega^2 \mu \epsilon - k_z^2} \cotan \left( \sqrt{\omega^2 \mu \epsilon - k_z^2} \left( \frac{a-d}{2} \right) \right) = \sqrt{\omega^2 \mu_0 \epsilon_0 - k_z^2} \tan \left( \sqrt{\omega^2 \mu_0 \epsilon_0 - k_z^2} \left( \frac{d}{2} \right) \right) \quad (13)$$

from (6) it can be found that

$$a = a' + \frac{2}{\sqrt{\omega^2 \mu \epsilon - k_z^2}} \tan^{-1} \left( C \sqrt{\omega^2 \mu \epsilon - k_z^2} \right) \quad (14)$$

then  $a$  can be substituted by  $a'$  in (14) and becomes:

$$\begin{aligned} & \sqrt{\omega^2 \mu \epsilon - k_z^2} \cotan \left( \sqrt{\omega^2 \mu \epsilon - k_z^2} \left( \frac{a'}{2} + \frac{2}{\sqrt{\omega^2 \mu \epsilon - k_z^2}} \tan^{-1} \left( C \sqrt{\omega^2 \mu \epsilon - k_z^2} \right) \right) \right) \\ & - \sqrt{\omega^2 \mu_0 \epsilon_0 - k_z^2} \tan \left( \sqrt{\omega^2 \mu_0 \epsilon_0 - k_z^2} \left( \frac{d}{2} \right) \right) = 0 \end{aligned} \quad (15)$$

In Equation (15), the only unknown parameter is  $k_z$ , and it can be found by a proper MATLAB program. This is done for our design. Then the equivalent RW length can be found from (14).

Attenuation constant due to dielectric loss can be computed by using the well-known formula.

$$\begin{aligned} \alpha_d &= \frac{P_d}{2P} \\ P_d &= \frac{1}{2} \omega \epsilon'' \int |E|^2 dv \\ P &= \frac{1}{2} \text{Re} \int [E \times H^*] ds \end{aligned} \quad (16)$$

where  $\alpha_d$ ,  $P_d$  and  $P$  are the attenuation constant due to dielectric loss, power loss in dielectric and power through the waveguide, respectively.

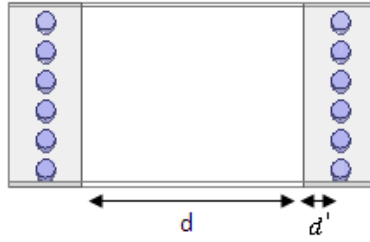
$$P_d = \frac{\omega \epsilon'' l b A^2 k_z^2}{2} \left( \frac{a-d}{2} - \frac{\sin(k_{x1}(a-d))}{2k_{x1}} \right) \quad (17)$$

$$P = \frac{B^2 k_z b}{2\omega \mu} (k^2 - k_{x0}^2) \left( \frac{d}{2} + \frac{\sin(k_{x0}d)}{2k_{x0}} \right) + \frac{k_z A^2 b}{2\omega \mu} (k^2 - k_{x1}^2) \left( \frac{a-d}{2} - \frac{\sin k_{x1}(a-d)}{2k_{x1}} \right) \quad (18)$$

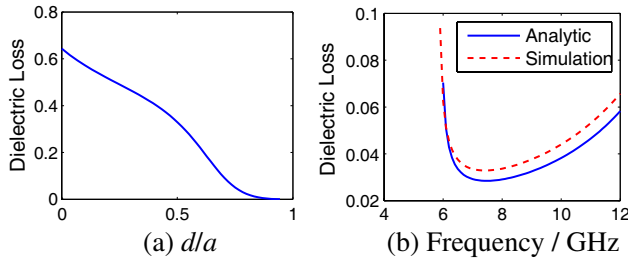
The mentioned analytical solution will be examined with an example. A PSIW structure with  $d = 19$  mm,  $d' = 3$  mm,  $b = 0.51$  mm (Substrate height) and RO4003 as a substrate is shown in Fig. 3. The simulations are carried out in Ansoft HFSS software, and the simulation results are compared with analytical results.

The dielectric loss as a function of  $\frac{d}{a}$  by considering the RW equivalent of PSIW in Fig. 2 is shown in Fig. 4(a). The dielectric loss can be calculated from (16) where  $a$  is width of the equivalent RW. As expected by increasing the air part in PSIW, dielectric loss is decreased. Practical considerations limit  $d$  which cannot be equal to  $a$ , because a small part of dielectric around the via must remain unchanged. The analytic solution for dielectric loss coincides with simulation results is shown in Fig. 4(b).

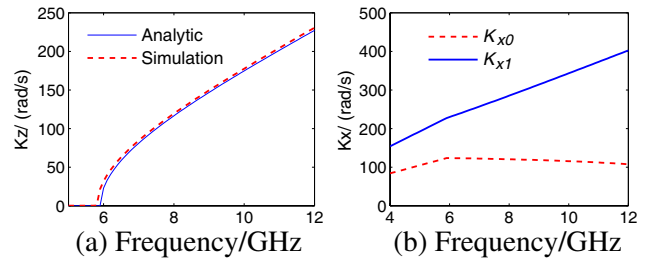
Propagation constants of PSIW in  $z$  and  $x$  directions that have been found from simulation is compared with analytical solution in Fig. 5. There is a good agreement between them.  $K_{x0}$  and  $K_{x1}$  are the propagation constants in  $x$  direction due to air part and dielectric part of PSIW, respectively, as illustrated in Fig. 5(b).



**Figure 3.** DUT of proposed PSIW structure.



**Figure 4.** (a) Dielectric loss variation with respect to  $\frac{d}{a}$ . (b) Dielectric loss of PSIW.



**Figure 5.** Propagation constant of PSIW. (a) In  $z$  direction. (b) In  $x$  direction.

### 3. DESIGN OF PARTIALLY FILLED SIW POWER DIVIDER

#### 3.1. PSIW Line Design

PSIW can be considered as an artificial rectangular waveguide that is produced by top and bottom metal covers and two side walls of vertical conducting cylinders. PSIW is operated in the  $TE_{no}$  modes. With the knowledge of pitch between consecutive vias and via diameters, PSIW can be replaced by an equivalent partially air-filled rectangular waveguide. The equivalent width ( $a$ ) has been computed. The dominant mode cut-off frequency of the rectangular waveguide is given as follows:

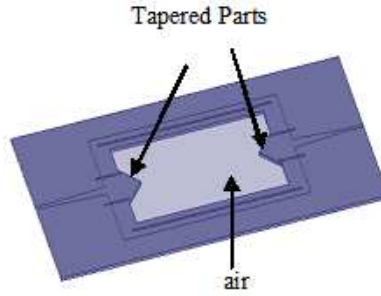
$$f_{cmn} = \frac{k_c}{2\pi} = \frac{1}{2\pi\sqrt{\mu\epsilon}} \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \tag{19}$$

$$f_{10} = \frac{1}{2a\sqrt{\mu\epsilon}}$$

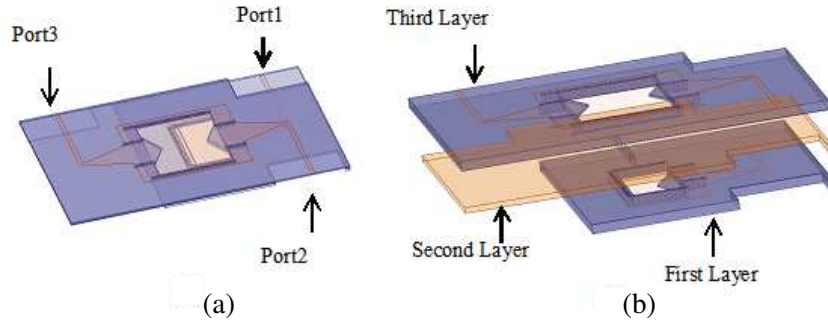
where  $b$  is the substrate thickness,  $a$  the SIW equivalent width, and  $\epsilon_0$  and  $\mu_0$  are the permittivity and permeability of the free space, respectively. By using the above formula, the PSIW width corresponding to cut-off frequency will be calculated.

The proposed PSIW in Fig. 3 must be adopted for measuring with vector network analyzer (VNA). The adopted PSIW line is shown in Fig. 6.

There are two tapered parts for reducing the unwanted effects associated with the transmission media change from air to dielectric. The electromagnetic waves have been coupled from dielectric to air in input side of the PSIW line and also from the air to dielectric at its output by using these tapered sections. There are two covering parts at the top and bottom of the PSIW line. These covering parts are easily attached to the tapered parts without any effect on the electrical performance of the component. There are two other tapered parts in connection points between SIW and the microstrip line. Their function is to match the SIW mode to microstrip line mode. These tapered lines' parameters can be computed from [4].



**Figure 6.** Proposed PSIW line.



**Figure 7.** (a) The proposed PSIW power divider. (b) Configuration of PSIW with three different layers.

### 3.2. PSIW Power Divider Design

The similarity of PSIW power divider to  $E$ -plane power divider encourages the use of  $E$ -plane power divider design procedure for designing PSIW counterpart.  $E$ -plane SIW power divider design procedure and its equivalent circuits are given in [16, 17].

Our proposed PSIW power divider is illustrated in Fig. 7. It consists of three layers. The first and third layers are made from RO4003 with  $\epsilon_r = 3.55$  and  $\tan \delta = 0.0027$  which is removed in the middle part. The second layer consists of copper with 0.3 mm thickness. There is a slot in the second layer for coupling the electromagnetic wave from layer 1 to layer 3. Two covering PCBs (RO4003) shield the bottom side of the first layer and top side of the third layer. The first- and third-layer structures are similar to PSIW line, unless the first layer is closed with the metallized vias at the end to control the wave toward the slot. This structure simply realizes an  $E$ -plane PSIW power divider in a small size.

The design procedure of PSIW power divider is similar to fully dielectric SIW power divider in [16]. Therefore, the width of the first layer is determined corresponding to the cut-off frequency. The second-layer width has been worked out by impedance matching between the two layers at the equivalent circuit of  $E$ -plan power divider.

By increasing the number of ports, only the length of the structure increases, and its width is unchanged. So this method can be developed to design an  $n$ -way PSIW power divider.

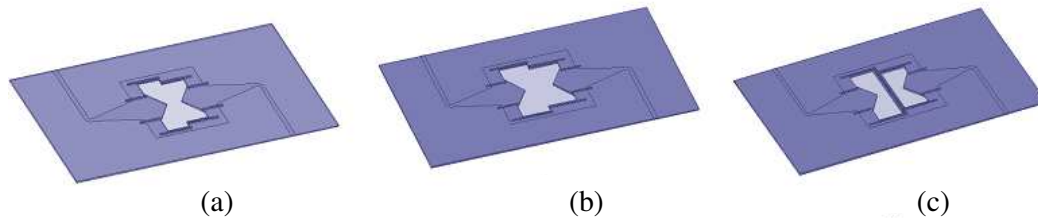
The PSIW power divider dimensions are shown in Table 1. These dimensions are for the structure without transition part.

### 3.3. TRL Calibration

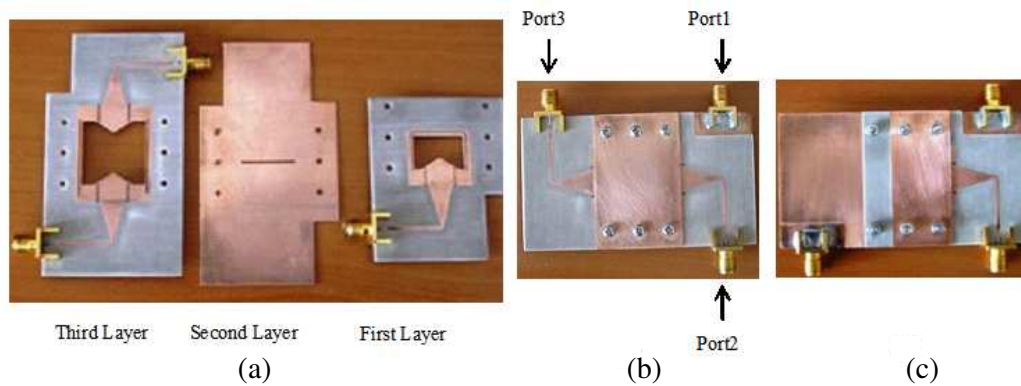
SIW structure must be connected to microstrip lines with tapered parts, which makes it suitable for measuring with the VNA. The tapered part and microstrip line influence the loss of SIW structure. Therefore, their contributions must be removed. This is achievable in the light of TRL calibration. Three TRL calibration standards for PSIW power divider measuring are shown in Fig. 8. As shown, these standards are hollow inside and contain two different error boxes. The widths of PSIW in the

**Table 1.** Dimensions of PSIW power divider (mm).

	Length	Width
First Layer	4	16
Slot	16.6	1
Third Layer	8	20.6
Transition Part	4.6	1.5



**Figure 8.** TRL standards. (a) True. (b) Line. (c) Reflect.

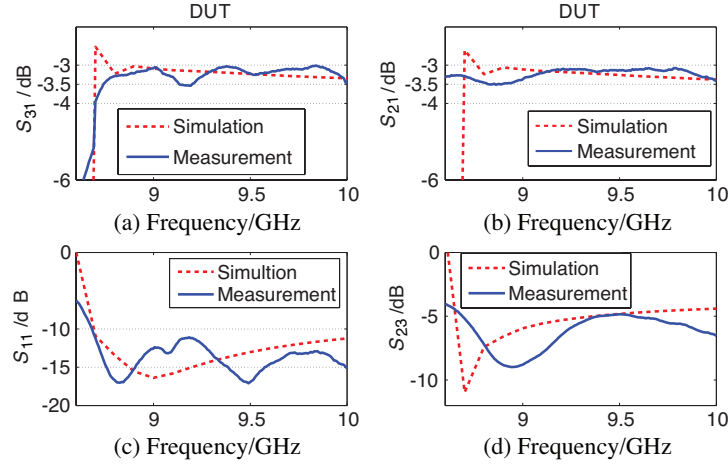


**Figure 9.** (a) Three layers of PSIW. (b) Top view. (c) Bottom view.

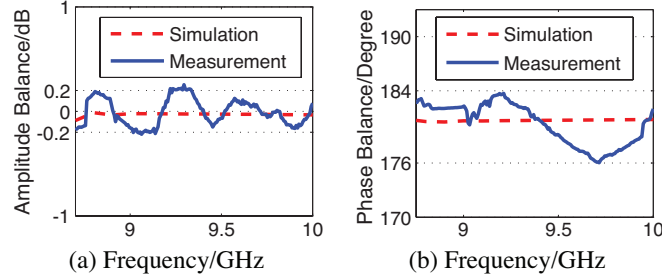
first and third layers are different, which leads to two different error boxes in the TRL standards. It should be noted that measurement method in [16] has been used for the  $S$ -parameters reconstruction. In order to avoid any radiation effects, the reflect standard is a short circuit. The through standard is made by connecting two error boxes directly together.

### 3.4. Simulation and Experimental Results

A picture of the fabricated PSIW power divider is shown in Fig. 9. Port 1 is the input port, and ports 2–3 are the output ports. Two RO4003 substrate with  $\epsilon_r = 3.55$ ,  $\tan \delta = 0.0027$  and 0.51 mm thickness are used to the first and third layers. The second layer is copper with 0.3 mm thickness. These layers are covered with two RO4003 PCBs as top and bottom walls of the structure. Return loss, transmission coefficients and isolation between output ports of PSIW power divider are shown in Fig. 10. The measurement process has been carried out with the TRL standards. The  $S$ -parameters of the DUT have been reconstructed according to the measurement set up in [16]. Therefore, any effects of transition parts and tapered sections are removed. Transmissions between  $-3$  dB and  $-3.5$  dB from 8.75 GHz to 10 GHz have been measured. Return loss is less than 10 dB in the same frequency band. Isolation between output ports is not as good as expected, because there is no any resistance between output ports. There are some differences between simulation and measurement results in Figs. 10(c) and (d). This may be related to top and bottom covering plate's connecting points to the main structure,



**Figure 10.** Simulation and measurement results of PSIW power divider. (a), (b) Transmission coefficients. (c) Return loss. (d) Isolation between output ports.



**Figure 11.** (a) Amplitude balance. (b) Phase balance of PSIW power divider.

**Table 2.** Comparison of PSIW and conventional SIW power divider.

PSIW	SIW
$-3.5 \text{ dB} < S_{21} < -3 \text{ dB}$	$-4 \text{ dB} < S_{21} < -3.5 \text{ dB}$
$-3.5 \text{ dB} < S_{31} < -3 \text{ dB}$	$-4 \text{ dB} < S_{31} < -3.5 \text{ dB}$
$S_{11} < -10 \text{ dB}$	$S_{11} < -10 \text{ dB}$

although by tapering these connecting sections, unwanted effects have been reduced significantly.

As shown in Fig. 11, the measured amplitude imbalance is less than  $\pm 0.2$  dB from 8.75 GHz to 10 GHz. The measured phase difference between  $\angle S_{21}$  and  $\angle S_{31}$  is about  $\pm 4^\circ$ . It is shown that the amplitude balance and phase balance are not sensitive to frequency of operation in the design frequency band. The comparison of the PSIW power divider with conventional SIW power divider [16] is summarized in Table 2, which shows that with suitable return loss, transmission toward port 2 and 3 becomes better at PSIW in desired frequency band. Therefore, the loss reduction has been deduced.

#### 4. CONCLUSION

A significant reduction in the dielectric loss is achieved by applying the novel approach proposed in this work. The idea is based on the removal of the central section in SIW. An equivalent waveguide model has been obtained in order to calculate the propagation constants and the dielectric attenuation constant of the proposed PSIW structure. It is shown that the dielectric loss variation is proportional to the width of the dielectric section in PSIW as expected. The design concept is validated by an experimental



prototype PSIW power divider. The good conformity between simulation and measurement results and also small size of the structure motivate to outline the power divider with more output ports. This method can be applied to realization of the other SIW components in which loss is a matter of concern.

## REFERENCES

1. Deslandes, D. and K. Wu, "Integrated microstrip and rectangular waveguide in planar form," *IEEE Microwave and Wireless Components Letters*, Vol. 11, 68–70, 2001.
2. Ke, W., D. Deslandes, and Y. Cassivi, "The substrate integrated circuits — A new concept for high-frequency electronics and optoelectronics," *6th International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Service, TELSIKS 2003*, Vol. 1, P-III–P-X, 2003.
3. Germain, S., D. Deslandes, and K. Wu, "Development of substrate integrated waveguide power dividers," *Canadian Conference on Electrical and Computer Engineering, IEEE CCECE 2003*, Vol. 3, 1921–1924, 2003.
4. Deslandes, D., "Design equations for tapered microstrip-to-substrate integrated waveguide transitions," *2010 IEEE MTT-S International Microwave Symposium Digest (MTT)*, 704–707, 2010.
5. Bozzi, M., L. Perregrini, and W. Ke, "Modeling of conductor, dielectric, and radiation losses in substrate integrated waveguide by the boundary integral-resonant mode expansion method," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 56, 3153–3161, 2008.
6. Ranjkesh, N. and M. Shahabadi, "Reduction of dielectric losses in substrate integrated waveguide," *Electronics Letters*, Vol. 42, No. 21, 1230–1231, 2006.
7. Kaijun, S., F. Yong, and Z. Yonghong, "Eight-way substrate integrated waveguide power divider with low insertion loss," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 56, 1473–1477, 2008.
8. Songnan, Y. and A. E. Fathy, "Synthesis of an arbitrary power split ratio divider using substrate integrated waveguides," *IEEE/MTT-S International Microwave Symposium*, 427–430, 2007.
9. Ning, Y., C. Caloz, and W. Ke, "Substrate integrated waveguide power divider based on multimode interference imaging," *2008 IEEE MTT-S International Microwave Symposium Digest*, 883–886, 2008.
10. Mohammadi, P. and S. Demir, "Two layers substrate integrated waveguide power divider," *2011 XXXth URSI General Assembly and Scientific Symposium*, 1–4, 2011.
11. Eom, D., J. Byun, and H.-Y. Lee, "Multi-layer four-way out-of-phase power divider for substrate integrated waveguide applications," *IEEE MTT-S International Microwave Symposium Digest, MTT'09*, 477–480, 2009.
12. Smith, N. A. and R. Abhari, "Compact substrate integrated waveguide Wilkinson power dividers," *IEEE Antennas and Propagation Society International Symposium, APSURSI'09*, 1–4, 2009.
13. Wenjie, F., C. Wenquan, and D. Kuan, "Compact planar magic-T using *E*-plane substrate integrated waveguide (SIW) power divider and slotline transition," *IEEE Microwave and Wireless Components Letters*, Vol. 20, 331–333, 2010.
14. Harrington, R. F., *Time Harmonic Electromagnetic Fields*, Wiley-IEEE Press, 2001.
15. Che, K. D. W., D. Wang, and Y. L. Chow, "Analytical equivalence between substrate-integrated waveguide and rectangular waveguide," *IET Microw. Antennas Propag.*, Vol. 2, No. 1, February 2008.
16. Mohammadi, P. and S. Demir, "Multi-layer substrate integrated waveguide *E*-plane power divider," *Progress In Electromagnetics Research C*, Vol. 30, 159–172, 2012.
17. Marcuvitz, N., *Waveguide Handbook*, McGraw-Hill Book Company, Inc., 1951.