© Universiti Tun Hussein Onn Malaysia Publisher's Office

IJIE

Journal homepage: http://penerbit.uthm.edu.my/ojs/index.php/ijie
ISSN : 2229-838X e-ISSN : 2600-7916

The International Journal of Integrated Engineering

Improvement of Single-Switch Bridgeless PFC Cuk Converter for Circulating Current Elimination and Components Maximum Current Stress Reduction

Mohamad Kamil Romai Noor[1], Asmarashid Ponniran[1*], Jumadril JN[1], Munirah Az Zahra Abdul Rashid[1], Mohd Amirul Naim Kasiran[1], Mohd Hafizie Yatim[1], Suhaimi Saiman[1], Abdul Fatah Mat Said[1]

[1]Faculty of Electrical and Electronic Engineering,
Universiti Tun Hussein Onn Malaysia, 86400 Parit Raja, Johor, MALAYSIA

*Corresponding Authors

DOI: https://doi.org/10.30880/ijie.2022.14.01.016
Received 29 April 2021; Accepted 02 November 2021; Available online 07 March 2022

Abstract: This paper presents the improvement of single-switch bridgeless PFC Cuk converter for circulating current elimination and maximum current stress reduction on components. On the existing converter structure, circulating current at diodes causes conduction losses and maximum current stress that increase the component size. Therefore, circulating current is eliminated by rearranging the position of input diodes thus the input diodes in which can block the returning path of current through the input inductors. The principle of circulating current elimination is also discussed in detail in this paper. A 100 W converter with output voltage of -48 V has been tested to verify the principle. The results of the experimental hardware show the removal of the circulating current, the maximum current stress in input diodes are reduced from 8 A to 2.8 A and the maximum current stress in input capacitors also reduced from 10.3 A to 6.5 A.

Keywords: Bridgeless PFC Cuk converter, circulating current, power factor, power factor correction, Cuk converter

1. Introduction

In recent years, power converter plays an important part in power conversion system. The available source in worldwide that is commonly used is AC source. However, some applications such as EV systems, DC motors, LED, electrical machines, datacom and telecom require input DC to operate [1]–[6]. The telecom application requires negative polarity as the input voltage while other DC applications require positive polarity [7]–[10]. The nominal input supply for telecom system is -48 V thus, a suitable AC-DC converter such as conventional buck-boost and Cuk converter must be employed to convert input AC to output DC. In this paper, the Cuk converter is selected to step down the input supply to -48 V [8], [9], [11]. Basically, the AC-DC converter is required to convert AC to DC while DC-DC converter is used for stepping up or stepping down the voltage. The integration of rectifier with Cuk converter is classified as passive PFC circuit but has the disadvantage of high conduction losses due to the presence of four diodes.

The PFC circuits without the full-bridge rectifier are bridgeless PFC structures. D.M Mitchell suggests the very first bridgeless PFC structure in 1983 [12]. The bridgeless PFC structure combines the operation of full-bridge rectifier and DC-DC converter in a circuit [13]. However, the structure has some drawbacks; presence of electromagnetic interference (EMI), switching losses, conduction losses, many components, discontinuous output current, high output voltage ripple, and circulating current losses [14]–[19]. Several bridgeless PFC Cuk converters were proposed to overcome the major

*Corresponding author: asmar@uthm.edu.my

drawbacks of the existing structures by eliminating the circulating current that exists at the input inductors and also by reducing the maximum current stress at the line diodes and input capacitors [14] [20]–[24].

A modified single-switch bridgeless PFC Cuk (SSBPFC) converter is presented in this paper as the proposed structure to solve the drawbacks of the existing structures. Circulating current elimination as well as maximum current stress reduction at line diodes (D_1 and D_2) and input capacitors (C_1 and C_2) are several advantages of the proposed structure. The design of the bridgeless PFC Cuk converter is based on discontinues conduction mode (DCM). Improvement of the SSBPFC Cuk converter structures will be discussed in terms of circulating current elimination in input inductor from the existing structures as well as on the improvement structures.

2. Principle of SEPIC-Cuk Converter

This section addresses the principle of circulating current elimination at input inductors, principle of maximum current stress reduction at line-diodes, principle of maximum current stress reduction at input capacitor, operation mode of proposed single-switch bridgeless PFC Cuk converter, and design of parameters of the modified SSBPFC Cuk converter.

2.1 Principle of Circulating Current Elimination at the Input Inductors

Fig. 1 shows the different position of the diodes between the existing structure and the proposed structure of the modified Cuk SSBPFC structure. Fig. 1(a) indicates that the diodes (D_1 and D_2) which are connected with MOSFET, S in series. When the MOSFET, S is turned-on, the L_1 and L_2 stores energy from AC source. The energy circulates between L_1 and L_2 during the charging process. When the MOSFET, S turns off, the diodes, D_1 and D_2 are in turn-off condition, while the L_1 and L_2 will be discharged. Thus, the circulation of current occurs between L_1 and L_2. The current circulates for both cycles and during the turned-on and turned-off condition. Ideally, L_1 and L_2 must operate in half a cycle to ensure that the input inductor is in DCM condition on the basis of the current flow to the input inductors.

The position of the diodes is rearranged to be in series with the input inductors in order to eliminate circulating current at L_1 and L_2 in positive-half and negative-half cycles. MOSFET, S turned-on during positive-half cycle, the AC source current flows to the L_1 while diode D_2 is in blocking state for positive-half cycle. When the MOSFET, S turns off, the inductor current flows directly to the C_1 due to the D_2 is in blocking condition. Thus, the circulating current during positive-half cycle at L_2 is eliminated whereas elimination of the circulating current at L_1 occurs during the negative-half cycle in the same state as the positive-half cycle.

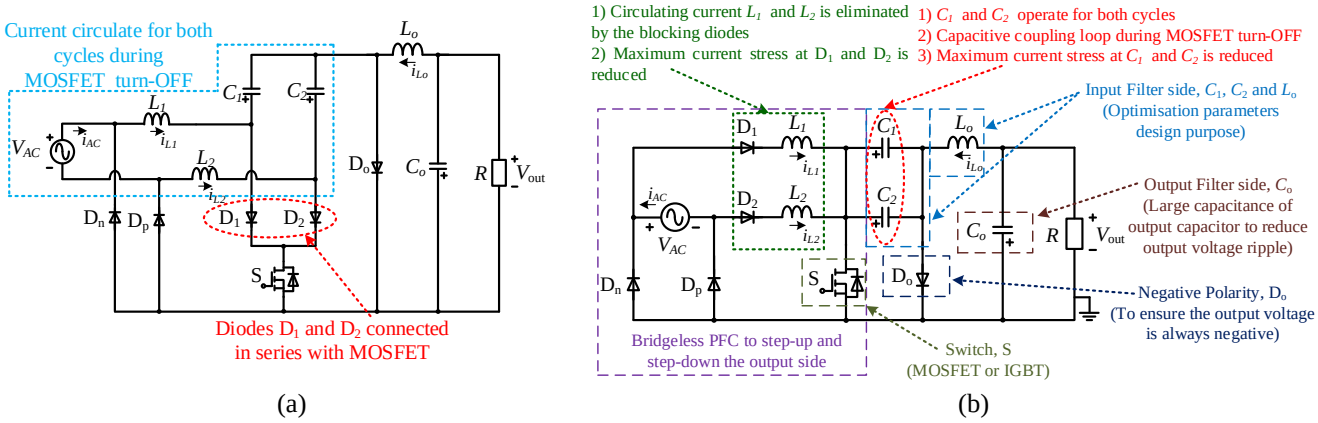


Fig. 1 - Different position of diodes between the existing structure and proposed structure of modified SSBPFC Cuk structure (a) Existing structure; (b) Modified SSBPFC Cuk structure

2.2 Principle of Maximum Current Stress Reduction at Line-Diodes

The input diodes, D_1 and D_2 shown existing structure is equal to maximum current stress at MOSFET, S due to the series connection of the input diodes with the MOSFET as shown in Fig. 1(a). Meanwhile, the proposed structure of the modified SSBPFC Cuk converter shows that the maximum current stress in line-diodes D_1 and D_2 is the same with the input inductors L_1 and L_2 as shown in Fig. 1(b). The input diodes and line-diodes operate in different cycles for both structures. The advantage of the proposed modified structure is that the maximum current stress at D_1 and D_2 is reduced. The choice of the D_1 and D_2 depends on the structure in which, the proposed modified SSBPFC Cuk structure can use either standard diodes or fast-recovery diodes compared to the existing structure which can only use fast-recovery diodes.

2.3 Principle of Maximum Current Stress Reduction at Input Capacitors

Fig. 1(a) shows the current circulates and current loops between the input capacitors C_1 and C_2 in the existing structure. The circulating current is different from the looping current for C_1 and C_2. The circulating current is the current flows from the AC source to the C_1 and C_2. The looping current is the current that loops from the AC source between C_1 and C_2 during MOSFET, S turned-off. The modified structure proposes that the loop current between C_1 and C_2 may reduce the maximum current stress at C_1 and C_2. As it is known, the current flow to the capacitor is divided into two when the capacitors are connected in parallel. When the capacitor is connected in series, the current flow through to the capacitor is the same. Thus, the maximum current stress at C_1 and C_2 for existing structure is therefore reduced significantly.

2.4 Operation Mode of Proposed Single-Switch Bridgeless PFC Cuk Converter

Duty cycle controlled the proposed single-switch structure. The circuit has twelve operation modes which comprises of positive-half and negative-half cycles. During the both cycles, Fig. 2 indicates the operating modes.

Mode-1 and Mode-7: Mode-1 is cycle for positive-half and mode-7 is cycle for negative-half. The energy is stored during positive half-cycle in L_1 and at the negative half-cycle in L_2 when the switch, S turns on. Simultaneously, the L_1 stores energy at the positive half-cycle and L_2 at the negative half-cycle when the switch S turns on. The capacitor C_o is discharged in this period of time, the diode D_o is blocked, The load is supplied with power, and is shown in Fig. 2(a) and 2(b) respectively.

Mode-2 and Mode-8: Mode-2 is cycle for positive-half and mode-8 is cycle for negative-half. The inductor L_1 at the positive half-cycle, L_2 at the negative half-cycle stores energy continuously from the AC supply in the very same state as when the switch S is on. Meanwhile, the capacitors C_1 and C_2 are discharging through to the inductor L_o. C_o is discharged during this period of time, the diode D_o is still in blocking mode, the load is supplied with power and shown in Fig. 2(a) and 2(b) respectively.

Mode-3 and Mode-9: Mode-3 is cycle for positive-half and mode-9 is cycle for negative-half. When the S switch is turned on in the same state, the inductor L_1 at positive-half cycle, L_2 at negative-half cycle stores energy continuously from the AC supply. In the meantime, the C_1 and C_2 discharge through the inductor L_o. C_o is charged in this period of time, the diode D_o is blocked, the load is supplied with the power as can be seen in Fig. 2(a) and 2(b).

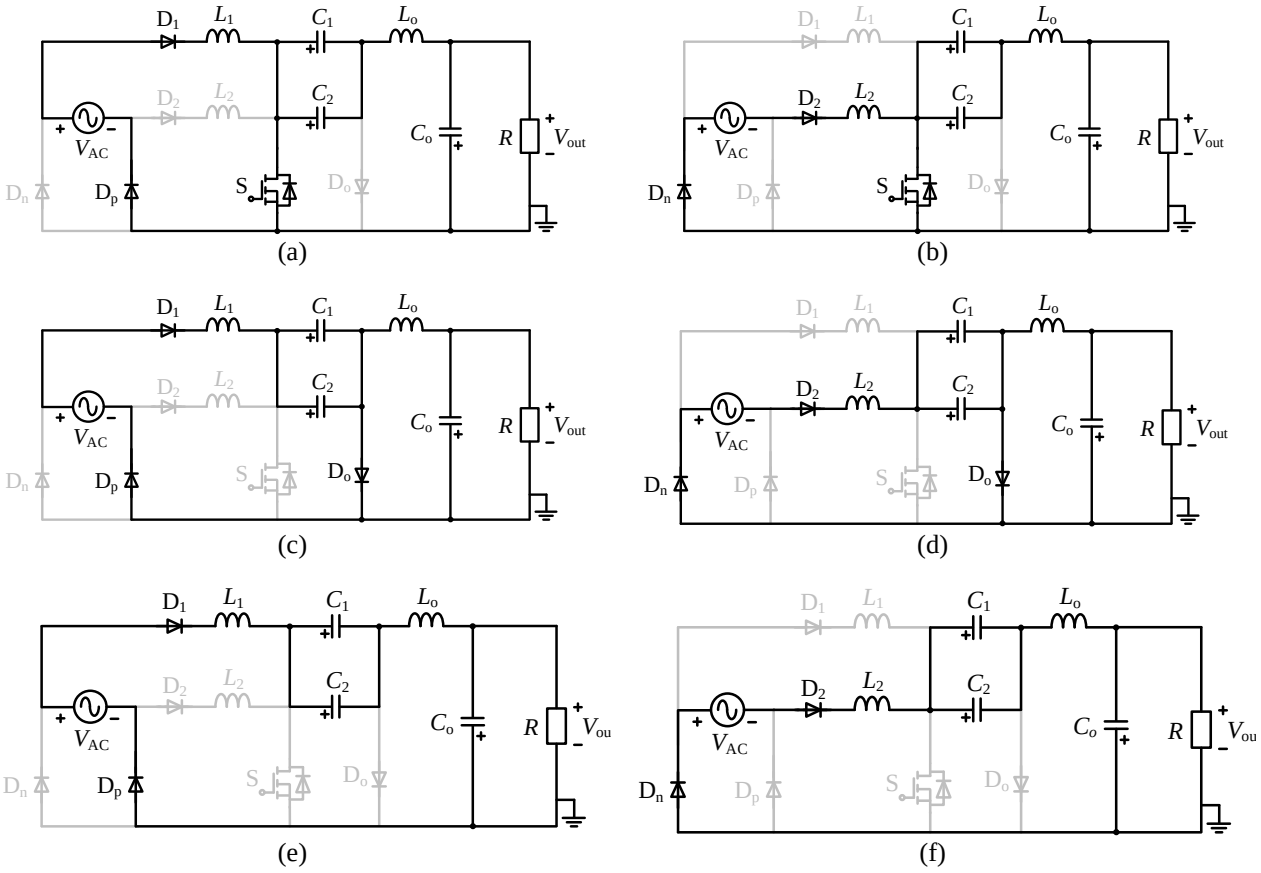


Fig. 2 - Mode operation of proposed structure (a) Mode-1, Mode-2, and Mode-3; (b) Mode-7, Mode-8, and Mode-9; (c) Mode-4 and Mode-5; (d) Mode-10 and Mode-11; (e) Mode-6; (f) Mode-12

Mode-4 and Mode-10: Mode-4 is cycle for positive-half and mode-10 is cycle for negative-half. The inductors L_1 are at the positive half-cycle when the switch S turns off, L_2 is at the negative half-cycle, and L_o is discharged. In the meantime, through the freewheeling diodes D_o, the capacitors C_1, C_2 and C_o charge the power to the load as can be observed in Fig. 2(c) and 2(d) respectively.

Mode-5 and Mode-11: Mode-5 is cycle for positive-half and mode-11 is cycle for negative-half. As switch S turns off, the inductors L_1 at the positive half-cycle and L_2 at the negative half-cycle are discharged in the same state. Meanwhile, through the freewheeling diodes D_o, the inductor L_o and capacitor C_o also discharges. The load is supplied with power, which can be seen in Fig. 2(c) and 2(d) respectively.

Mode-6 and Mode-12: Mode-6 is cycle for positive-half and mode-12 is cycle for negative-half. The capacitors C_1 and C_2 store energy through the looping state of the L_1 at the positive half cycle and L_2 at the negative half cycle in the very same state when the switch S turns off. The capacitor C_o and inductor L_o discharge during this period of time, diode D_o is turned-off, the load is supplied with power and shown in Fig. 2(e) and 2(f).

2.5 Parameters Design of Modified SSBPFC Cuk Converter

The passive element specifications of the SSBPFC Cuk structure are listed in Table 1. The passive elements are estimated from the mode of operation in Section 2.4 to be in the DCM state.

Table 1 - Specifications of SSBPFC Cuk structure

Parameters	Values
Voltage Input, V_{AC}	(50-100) V
Line Frequency, F_{SW}	50 Hz
Output voltage (DC), V_o	-48 V
Output power, P_{out}	100 W
Frequency of switching, f_s	50 kHz
Maximum input current ripple, Δi_{L1}	< 25% of fundamental current
Ripple of output voltage, ΔV_o	< 5% of V_o

SSBPFC Cuk circuit structure specifications are enlisted Table 2 after every parameter is calculated by taking into consideration the market availability of components.

Table 2 - Design of parameter for passive components

Parameters	Values
Input inductors, L_1 and L_2	2.2 mH
Output inductor, L_o	22 µH
Input capacitors, C_1 and C_2	1 µF
Output capacitor, C_o	3300 µF

2.5.1. Voltage Conversion Ratio, *M*

The ratio of voltage conversion, $M = V_o/V_m$ is achieved by implementing the power-balance principle [31],[68] with regard to circuit structure parameters and the ratio of voltage conversion is equivalent to:

$$M = \frac{V_{out}}{\sqrt{2} \cdot V_{AC}} = \sqrt{\frac{R}{2 \cdot R_e}} = \frac{D_{t_{on}}}{\sqrt{2 \cdot K_e}} \quad (1)$$

2.5.2. Gain Ratio as a Function of Duty Cycle, *D*

The duty cycle can be found as:

$$D = \frac{M}{M + 1} \quad (2)$$

2.5.3. Design of Input Inductors, L_1 and L_2

Input inductance of the input inductor value can be found as:

$$L_1 = \frac{V_{AC} \cdot D}{\Delta I_{L1} \cdot f_{sw}} \quad (3)$$

2.5.4. Design of Output Inductor, L_0

During one line-cycle of the AC source, the average diode output current, I_{Do}, can be determined by:

$$I_{AC,Avg} = \frac{D_{t_{on}} \cdot T_S \cdot V_{AC}^2}{2 \cdot L_e \cdot V_o} \quad (4)$$

The K_e is dimensionless parameter and can be represented as:

$$K_e = \frac{D^2}{2 \cdot M^2} \quad (5)$$

The L_e can be found by:

$$L_e = \frac{R \cdot T_s \cdot K_e}{2} \quad (6)$$

The output inductor can, therefore, be determined by the application of (3) and (6):

$$L_o = \frac{L_1 \cdot L_e}{L_1 - L_e} \quad (7)$$

2.5.5. Design of Input Capacitor, C_1

An essential component in the topology of Cuk is the input capacitor, C_1, as the quality waveform of AC source current may be distorted and can be found as:

$$C_1 = \frac{1}{\left(2\pi \cdot f_r\right)^2 \cdot \left(L_1 + L_0\right)} \quad (8)$$

2.5.6. Design of Output Capacitor, C_0

As the converter input is an AC source, as for reducing the output voltage ripple, the output capacitor should be sufficiently large. Hence, the output of the voltage ripple should be chosen according to the required application, and C_o is achieved as follows:

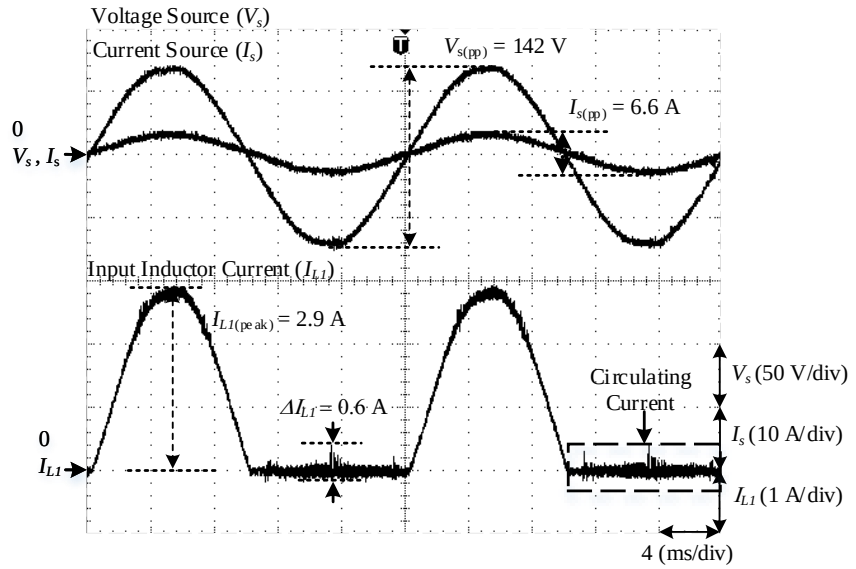
$$C_o = \frac{P_{out}}{4 \cdot f_L \cdot V_o \cdot \Delta V_o} \quad (9)$$

3. Results and Analysis

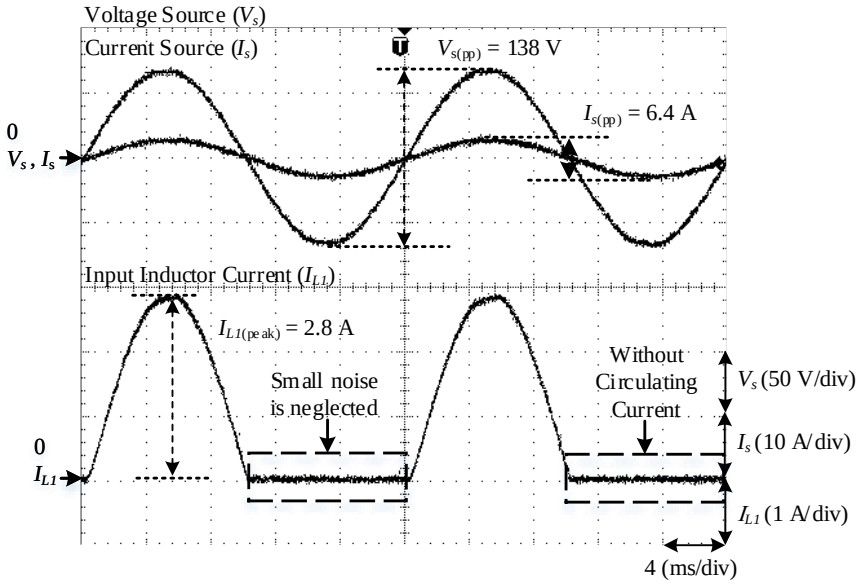
The results of the prototypes focus on eliminating the losses of the circulating current, reducing of line diodes D_1 and D_2 and reducing of the maximum current stress at maximum stress current at input capacitors C_1 and C_2 are discussed with reference to Table 1. The results of the prototypes are confirmed and are in agreement with the parameters designed.

3.1 Eliminating of Circulating Current at Input Inductors, L_1 and L_2

Fig. 3 displays the experimental results of the existing structure and the proposed structure of modified SSBPFC Cuk converter. All parameters have been mentioned in Table 1 and Table 2. The waveform demonstrates the elimination of the circulating current in the proposed structure, which is consistent with the analysis of theory in Section 2.1. Fig. 3(a) displays the results for both cycles of an existing structure containing circulating current in input inductors, L_1 and L_2. During a positive half-cycle operation of input inductor L_1, the input inductor's peak current $I_{L1(peak)}$ is 2.9 A. In the meantime, the circulating current losses during the negative half-cycle are 0.6 A with a peak-to - peak input line current of 6.6 A and a peak-to-peak input line voltage of 142 V. Comparing it with Fig. 3(b), there is no circulating current and the input inductors $I_{L1(peak)}$ is 2.8 A. The input line current of peak-to-peak is 6.4 A and the input line voltage of peak-to-peak is 138 V. The verification of experiment demonstrates the circulating current has been significantly eliminated by the proposed structure.



(a)

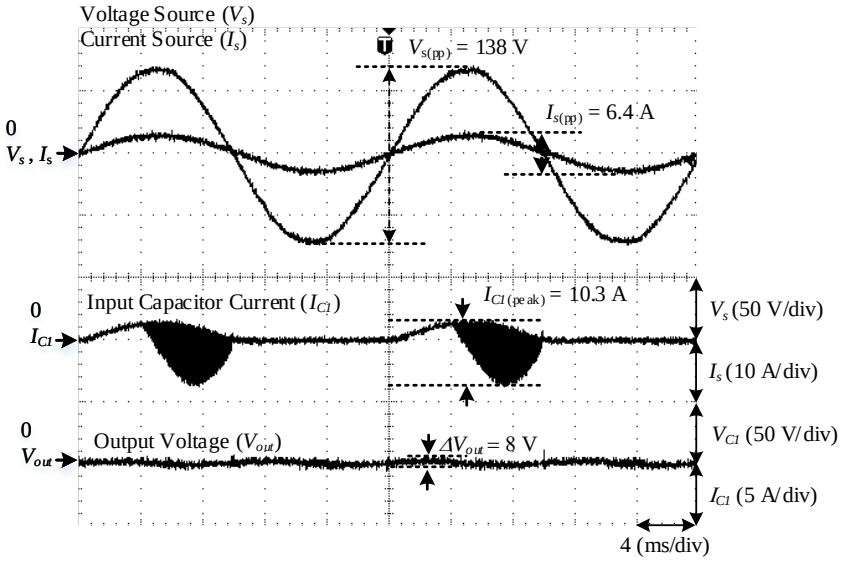


(b)

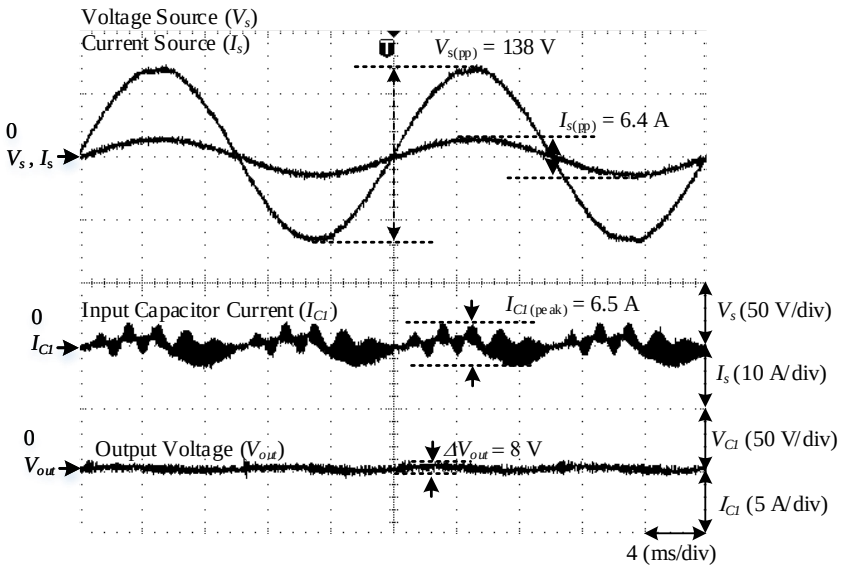
Fig. 3 - Elimination of circulating current at the input inductors, L_1 and L_2 (a)Existing structure, and (b) Proposed structure of SSBPFC Cuk converter

3.2 Maximum Current Stressed Reduction at Input Capacitors, C_1 and C_2

Fig. 4 clearly shows the results of the experimental for the existing structure also the proposed modified structure to decrease the input capacitors' maximum current stress, C_1 and C_2. Taking account of the cycle for half positive, Fig. 4(a) indicates capacitor C_1 that operates only during positive half-cycle. The input capacitor's peak current $I_{C1(peak)}$ is 10.3 A, while the input line current of peak-to-peak is 6.4 A and the input line voltage of peak-to-peak is 138 V. At input capacitors, the maximum current stress is high due to each capacitor that only operates in half-cycle mode. Comparing it with the Fig. 4(b), the peak current of the input capacitor $I_{C1(peak)}$ is 6.5 A while the input line current of peak-to-peak is 6.4 A and input line voltage of peak-to-peak is 138 V. In both cycles, capacitor C_1 operates, so the maximum current stress of the input capacitors is reduced. The results are consistent with the analysis of theory discussed in Section 2.3 for both structures.



(a)

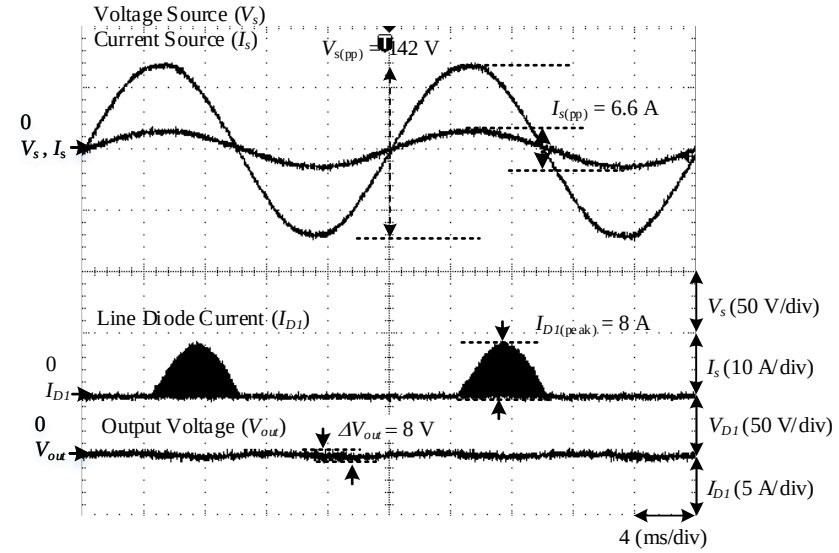


(b)

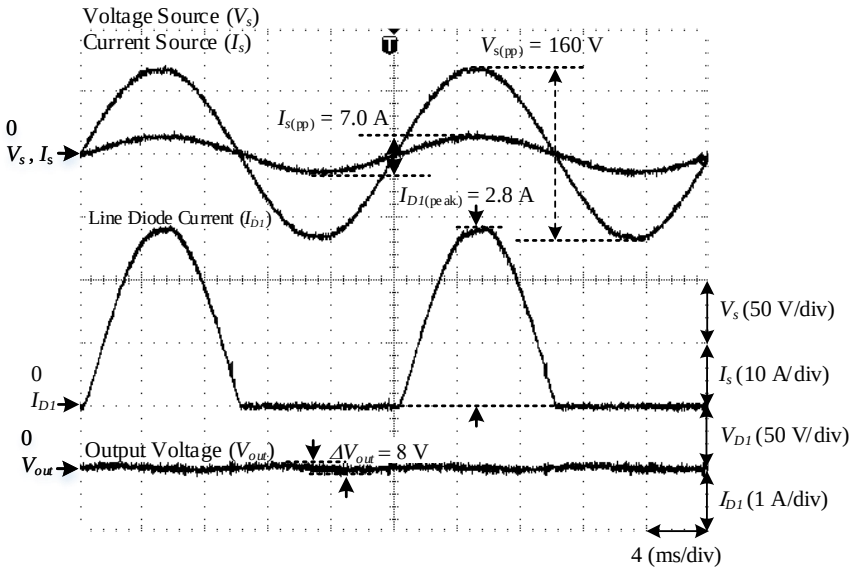
Fig. 4 - Maximum current stressed reduction at input capacitors (a) Existing structure, and (b) Proposed structure of SSBPFC Cuk converter

3.3 Maximum Current Stressed Reduction at Line Diodes, D_1 and D_2

The line diodes D_1 and D_2 maximum current stress is significantly reduced by positioning the line diodes serial with MOSFET, S to be serial with the input inductors L_1 and L_2 with 50 Hz line frequency of. Fig. 5 shows the experimental results of the existing structure and the proposed structures to decrease the maximum current stress at line diodes, D_1 and D_2. Taking account of the cycle for half positive, Fig. 5(a) demonstrates that operation of D_1 only occurs during positive half-cycle. The line diode $I_{D1(peak)}$ highest current is 8 A and the input line current of peak-to-peak is 6.6 A and input line voltage of peak-to-peak is 142 V. As the position of the components is serial with the MOSFET, S, the maximum current stress at C_1 and D_1 is the same. The current flows are high through the C_1 and D_1 are high because the switching frequency is 50 kHz. To compare this with Fig. 5(b), the line diode's peak current $I_{D1(peak)}$ is 2.8 A, whereas the input line current of peak-to-peak is 7.0 A, while the input line voltage of peak-to-peak is 160 V. In addition, the output voltage ripple of both structures are 8 V. For both of the structures, the maximum current stress of C_1 and D_1 is not the same because of different frequency of both components, i.e. f_{Line} is 50 Hz and f_{sw} is 50 kHz. Maximum current stress of the C_1 and D_1 can be observed to be significantly reduced after repositioning of the input diodes.



(a)



(b)

Fig. 5 - Reduction of maximum current stressed at line diodes (a) Existing structure, and (b) Proposed structure of SSBPFC Cuk converter

4. Conclusion

This paper presents the improvement of SSBPFC Cuk converter for circulating current elimination and components maximum current stress reduction. The results of the prototype agrees well with the results designed. Furthermore, circulating current losses have been eliminated. The maximum current stress at D_1 and D_2 is decreased from 8 A to 2.8 A which is 65% reduced, while maximum current stress at C_1 and C_2 is decreased from 10.3 A to 6.5 A which is 37% reduced. The advantages of having low current stress in diodes and capacitors are that when the current stress at the passive or active component is low, the selection of the rating components and, as a result, the size of the components is reduced. This prototype uses switching frequency 50 kHz for single-switch (MOSFET) with the output power of 100 W and output voltage is fixed to -48 V. By implementing any PWM switching pattern, this SSBPFC structure can achieve a high-power factor.

Acknowledgement

The authors would like to show gratitude to Universiti Tun Hussein Onn Malaysia (UTHM) from the financial support by GPPS Vot. H536 grant and Research Fund, UTHM.

References

[1] H. H. Kasiran, A. N., Ponniran, A., Harimon, M. A., & Hamzah, "A Study of 4-level DC-DC Boost Inverter with Passive Component Reduction Consideration," *J. Phys. Conf. Ser.*, vol. 995, no. 1, p. 12062, 2018.

[2] A. B. Ponniran and M. A. N. B. Kasiran, "Parameters design evaluation in 3-level flying capacitor boost converter," in *2017 IEEE Symposium on Computer Applications & Industrial Electronics (ISCAIE)*, 2017, pp. 195–199.

[3] M. H. Yatim *et al.*, "Symmetrical and asymmetrical multilevel inverter structures with reduced number of switching devices," *Indones. J. Electr. Eng. Comput. Sci.*, vol. 11, no. 1, pp. 144–151, 2018.

[4] A. N. Kasiran, A. Ponniran, A. A. Bakar, and M. H. Yatim, "4-Level Capacitor-Clamped Boost Converter With Hard-Switching and Soft-Switching Implementations," *Int. J. Power Electron. Drive Syst.*, vol. 10, no. 1, p. 288, 2019.

[5] M. A. Harimon, A. Ponniran, A. N. Kasiran, and H. H. Hamzah, "A Study on 3-phase Interleaved DC-DC Boost Converter Structure and Operation for Input Current Stress Reduction," *Int. J. Power Electron. Drive Syst. (IJPEDS); Vol 8, No 4 December 2017*, vol. 8, no. 4, pp. 1948–1953, 2017.

[6] M. H. Yatim, A. Ponniran, A. A. Bakar, A. N. Kasiran, M. K. R. Noor, and J. N. Jumadril, "Analysis of Symmetric and Asymmetric Multilevel Inverter Topologies Using Reduced Number of Switching Devices Circuit Structure," in *International Journal of Engineering & Technology*, 2018, vol. 7, pp. 234–239.

[7] A. Bin Ponniran *et al.*, "Fundamental Operation of Marx Topology for High Boost Ratio DC-DC Converter," *IEEJ J. Ind. Appl.*, vol. 5, no. 4, pp. 329–338, 2016.

[8] A. Bin Ponniran, S. Member, K. Orikawa, and M. Jun-ichi Itoh, "Minimization of Passive Components in Multi-level Flying Capacitor DC-DC Converter," *IEEJ J. Ind. Appl.*, vol. 5, no. 1, pp. 10–11, 2015.

[9] H. T. Yang and H. W. Chiang, "Implementation of bridgeless Cuk power factor corrector with positive output voltage," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, 2014, pp. 2100–2107.

[10] M. S. Ali, S. K. Kamarudin, M. S. Masdar, and A. Mohamed, "An Overview of Power Electronics Applications in Fuel Cell Systems: DC and AC Converters," *Sci. World J.*, vol. 2014, pp. 1–9, 2014.

[11] A. Ponniran, K. Orikawa, and J. Itoh, "Fundamental Operation of Marx Topology for High Boost Ratio DC-DC Converter," *IEEJ J. Ind. Appl.*, vol. 5, no. 4, pp. 329–338, 2016.

[12] D. M. Mitchell, "AC-DC Converter having an improved power factor," Sep-1982.

[13] H. T. Yang, H. W. Chiang, and C. Y. Chen, "Implementation of Bridgeless Cuk Power Factor Corrector With Positive Output Voltage," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3325–3333, 2015.

[14] E. H. Ismail, "Bridgeless SEPIC Rectifier With Unity Power Factor and Reduced Conduction Losses," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1147–1157, 2009.

[15] A. M. A. Gabri, A. A. Fardoun, and E. H. Ismail, "Bridgeless PFC SEPIC rectifier with extended gain for universal input voltage applications," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, 2014, pp. 1277–1284.

[16] A. M. A. Gabri, A. A. Fardoun, and E. H. Ismail, "Modelling and simulation of bridgeless PFC modified SEPIC rectifier with multiplier cell," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 2739–2745.

[17] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "A comparison between three proposed bridgeless Cuk rectifiers and conventional topology for power factor correction," in *2010 IEEE International Conference on Sustainable Energy Technologies (ICSET)*, 2010, pp. 1–6.

[18] A. M. Al Gabri, A. A. Fardoun, and E. H. Ismail, "Bridgeless PFC-Modified SEPIC Rectifier With Extended Gain for Universal Input Voltage Applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4272–4282, 2015.

[19] A. J. Sabzali, E. H. Ismail, M. A. Al-Saffar, and A. A. Fardoun, "New Bridgeless DCM Sepic and Cuk PFC

Rectifiers With Low Conduction and Switching Losses," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 873–881, 2011.
[20] K. K. M. Siu and C. N. M. Ho, "A critical review of Bridgeless PFC boost rectifiers with common-mode voltage mitigation," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, 2016, pp. 3654–3659.
[21] M. Jovanovic and Y. Jang, "Power factor correction rectifier having independent inductive components," 2007.
[22] S. A. F. De and B. Ivo, "High power factor rectifier with reduced conduction and commutation losses," in *21st International Telecommunications Energy Conference. INTELEC '99 (Cat. No.99CH37007)*, 1999, p. pp.158.
[23] C. Zheng, H. Ma, B. Gu., "An improved bridgeless SEPIC PFC rectifier with optimized magnetic utilization, minimized circulating losses, and reduced sensing noise," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 1906–1911.
[24] H. Ma, Y. Li, J. S. Lai, C. Zheng, and J. Xu, "An Improved Bridgeless SEPIC Converter without Circulating Losses and Input Voltage Sensing," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. PP, no. 99, p. 1, 2017.