Improved Noise Immunity for Two-Sample PLL Applicable to Single-Phase PFCs

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***Abstract*— Synchronization in a single-phase Power Factor Correction (PFC) is deteriorated, among others, by the combination of the noise introduced by the grid voltage sensing, conducted EMI, the ADC resolution and the sampling frequency used. Low signal-to-noise ratios (SNR) reduce the performance of the Two-Sample (2S) Phase Locked Loop (PLL). This effect can be compensated by including a smoothing filter action without increasing the overall complexity significantly. The resulting 2S with smoothing (2SS) is evaluated and validated by simulation and experimentally over a Totem Pole PFC.**

***Index Terms*—PLL, synchronization, noise immunity.**

I. INTRODUCCIÓN

Power Factor Correction (PFC) stages require simple and effective controllers to achieve the cost and performance targets [1], [2]. Power quality disturbances and events can deteriorate the PFC performance [3]. A key element of these systems, which determine performance and reliability under such conditions, is the phase locked loop (PLL). However, its use is marginal in this type of controls, because the control of the grid current has been satisfactorily solved with other methods since the quality standard refers to the power factor and harmonic content, but does not provide specifications for the dynamic response nor the interaction with other loads and generators with power electronics frontend [4]. So, including this type strategies in PFC control and providing the system with higher immunity to noise will allow reaching a new level of operation quality.

PLLs are used to track the phase of the grid voltage to synchronize the line current of the power converters connected to it [5]. The simplest PLL structure consists of a phase detector (PD), a loop filter (LF) and a voltage-controlled oscillator (VCO). The PD compares input and VCO signals to generate an error signal whose DC component corresponds to the phase error. The LF attenuates other frequency components present in the error signal with a low pass filter typically carried out by a PI controller. The VCO generates an oscillating signal, whose frequency, in steady state, is equal to that of the grid and is in phase with it once the PLL is locked. In the case of single phase PLLs with a PD based on the Park transformation, it is also necessary to use a subsystem generating an in-quadrature signal from the instantaneous values of the grid voltage. The way to obtain this signal has been deeply analyzed in the technical literature proposing different circuits and filters [6].

The Two-Sample (2S) Phase Locked Loop (2S-PLL), proposed in [7], which obtains the virtual in-quadrature component, β_k, by applying finite differences to the acquired signal from the grid voltage, whenever the grid voltage frequency is around its operation point, which can be dynamically adjusted as a function of the PLL frequency, ω. However, noisy grid voltages and quantization errors deteriorate the output of the quadrature signal generator (QSG) in the 2S PLL, making it at some point difficult to use. For this reason, this proposal slightly modifies the 2S-PLL in [7] to include a smoothing filter action [8] in the structure of the QSG without increasing the overall complexity significantly and maintaining the synchronization performance under noisy operation conditions. The work is organized as follows: Section II describes the 2S-QSG with the proposed smoothing filter. Section III the evaluation of the proposal through the simulation results. Section IV contains the results of the circuit and its implementation. And the work finalizes with conclusions in Section V.

II. TWO-SAMPLES QSG WITH SMOOTHING FILTER ACTION

Fig. 1 shows the controller of the Totem Pole PFC used. The control consists of two decoupled current and a voltage loops. The faster inner current loop takes advantage of the PLL to ensure that the line current waveform results in a high fundamental PF, PF_1 [9], i.e. sinusoidal current synchronized to the grid voltage, while the slower output voltage loop controls the DC voltage by adjusting the amplitude of the reference current. Sensors and signal conditioning circuits are kept as simple as possible: one current shunt and two voltage dividers are used for line current, AC and DC voltages measurements. Moreover, the AC voltage is rectified before sensing to increase the measurement resolution. The polarity is provided digitally. As a result, the PLL input must be reconstructed, which also deteriorates the PLL performance.

In the 2S-PLL proposed in [7], at instant *k*, β_k is generated with only two samples of the grid voltage acquired in three consecutive sampling instants:

$$\beta_k = (\alpha_{k-2} - \alpha_k)\frac{1}{sin\left(\frac{4\pi}{N_k}\right)} + \alpha_k\, tan\left(\frac{2\pi}{N_k}\right) \quad (1)$$

$$N_k = \frac{2\pi}{T_s\omega} \quad (2)$$

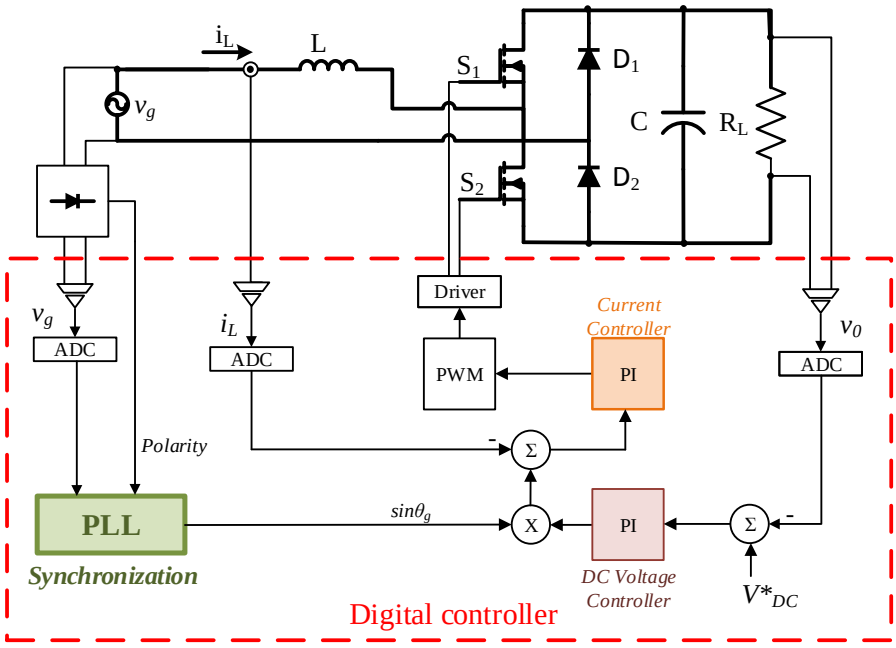


Fig. 1. Totem Pole controller.

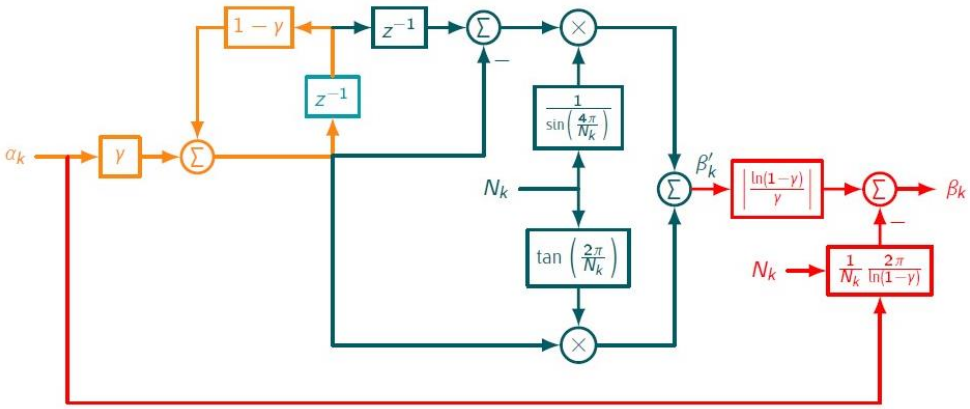


Fig. 2. Proposed 2S with Smoothing filter.

where α_k is the sampled grid voltage and T_s is the sampling time.

This QSG ensures orthogonality with low harmonically distorted grid voltages and sampling frequencies above 1 kHz while minimizing the memory requirements. However, its performance is affected by the presence of noise in the input signal and its use is not recommended when this type of interference is detected.

Conversely, smooth filtering has been used in technical literature to improve the accuracy of discrete derivatives when used with noisy signals [10], [11]. The simplest smoother in [8] is characterized in the z-domain by

$$G(\gamma, z^{-1}) = \frac{\gamma}{1-(1-\gamma)z^{-1}} \tag{3}$$

and in frequency domain by

$$\begin{cases} |G(\gamma,\omega)| = \dfrac{\dfrac{\gamma}{T_s}}{\sqrt{\left(\dfrac{ln(1-\gamma)}{T_s}\right)^2 + \omega^2}} \\ \angle G(\gamma,\omega) = arctan\dfrac{\omega T_s}{ln(1-\gamma)} \end{cases} \tag{4}$$

where γ ϵ (0,1) is the smoothing factor.

The 2S QSG structure in [7], depicted in green and cyan in Fig. 1, uses two sample delays. The first delay, in cyan, can be shared, according to (3), to embed a simple smoothing action (in orange and cyan).

Given the k^{th} sample of the in-phase signal $\alpha_k = A\,cos\left(\frac{2\pi}{N_k}k\right)$, and due to the smoothing action in (4), the 2S QSG output, at $\omega_{PLL} = 2\pi/(N_k T_s)$, would result in

$$\beta_k' = H_k A \sin\left(\frac{2\pi}{N_k}k + \phi_k\right)$$

$$= H_k \left[\underbrace{A \cos\left(\frac{2\pi}{N_k}k\right)}_{\alpha_k} \sin\phi_k + \underbrace{A \sin\left(\frac{2\pi}{N_k}k\right)}_{\beta_k} \cos\phi_k \right] \quad (5)$$

with $H_k = \frac{N_k\gamma}{\sqrt{(N_k\, ln(1-\gamma))^2+4\pi^2}}$ and $\phi_k = arctan\frac{2\pi}{N_k\, ln(1-\gamma)}$. The smoother action attenuates and delays the in-quadrature values at the fundamental grid frecuency.

These issues are compensated by

$$\beta_k = \frac{\beta_k'}{H_k \cos\phi_k} - \alpha_k \tan\phi_k. \quad (6)$$

By increasing the sampling frequency, reducing the smoothing action, or both, $N_k >> \left|\frac{2\pi}{ln(1-\gamma)}\right|$ and, then, $H_k \approx \left|\frac{\gamma}{ln(1-\gamma)}\right|$, $\phi_k \approx \frac{2\pi}{N_k\, ln(1-\gamma)}$, and, at constant sampling frequency, the attenuation only depends on the smoothing factor γ and the phase shifting changes with N_k linearly. By replacing these approximations in (6)

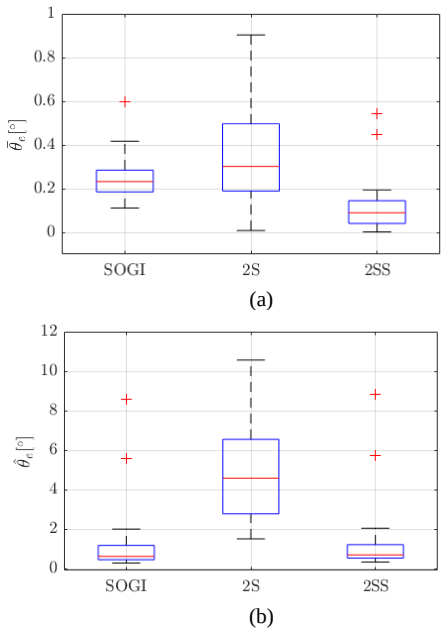
$$\beta_k \approx \frac{\beta_k'}{H_k \cos\phi_k} - \alpha_k\phi_k \quad (7)$$

The proposed structure is shown in the block diagram in Fig. 2, where the 2S-QSG is printed in green, the smoother in orange and the attenuation and the phase compensation in red.

III. SIMULATION RESULTS

The proposed 2S, using γ = 0.03125, the 2S and the Second-Order Generalized Integrated (SOGI) PLLs, are evaluated by means of a Monte Carlo (MC) tests using Matlab/Simulink® focusing on evaluating the noise rejection capability. The same tests and conditions have been run. Also, these PLLs have been designed with the same PI controller parameters, according to [12] (proportional, K_p = *46* and integral gain, K_i = *1024*). The sampling time, T_s, is 156.25 µs.

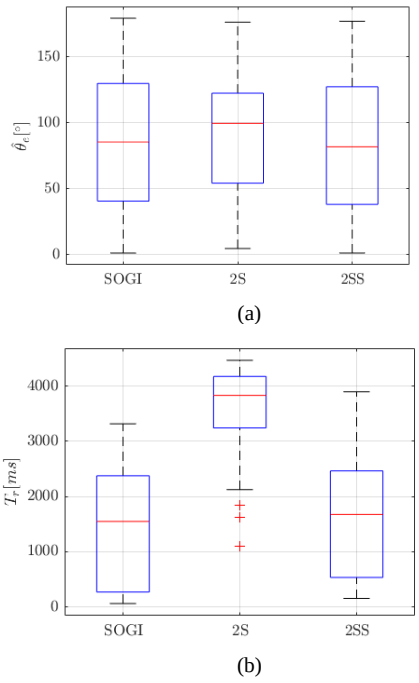
All the MC tests consider noisy distorted grid voltages (with normal distribution) and with DC components (until 2 % of the V_g). A total of 203 simulation conditions are generated through Latin Hypercube Sampling (LHS), which allows the representative number of MC tests to be reduced. Results are presented according to a uniform probability density function (PDF). The response to frequency jumps has been evaluated in the range *[0º, 360º)* and *[-5 Hz, 5Hz]* and the magnitude of the phase jumps is uniformly distributed in the range *[-90º, +90º]* and the starting point is applied at different phase instants in the range *[0º, 360º)*. Algo, the voltage dip depths are in the range *[20%, 90%]*, its durations, in the range *[10 ms, 200 ms]* and its initial phases *[0, 360º)*.



(a)

(b)

Fig. 3. Results of MC tests in steady state. Harmonic content and the nominal grid frequency are combined through LHS. a) Mean phase error and b) Ripple of the phase error.



(a)

(b)

Fig. 4. Results of MC tests with frequency jumps. Starting phase angle and jump magnitude are varied through LHS. a) Overshoot of the phase errors and b) response times.

The resulting PDFs for the measured mean phase error ($\overline{\theta_e}$) in steady state are shown in Fig. 3.a, where 2SS is lower with a median of 0.08º. The 2S obtained the higher medians with 0.3º. The measured phase error ripple ($\widehat{\theta_e}$) under the same steady-state test is shown in Fig. 3.b where the ripple to the range in 2SS and SOGI are lower and similar ([0.4º, 1.2º]). And, again, 2S-PLL obtained the worst results ([2.4º, 6.2º]).

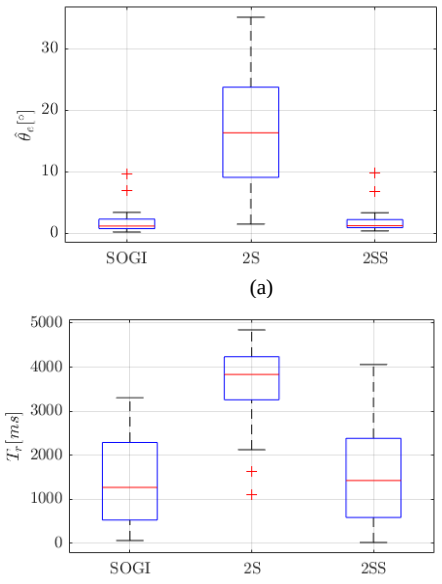


Fig. 5. Results of MC tests with phase jumps. Starting phase angle and jump magnitude are varied through LHS. a) Overshoot of the peak phase error and b) response times.

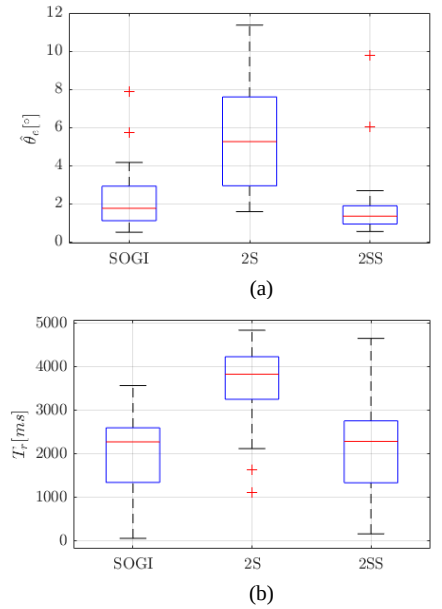


Fig. 6. Results of MC tests with voltage dips. Starting phase angle and dip depth and duration are varied through LHS. a) Overshoot of the peak phase error and b) response times.

In Fig. 4 and 5 show the overshoot of the phase errors and response times of the PLLs before frequency jumps and phase jumps where SOGI and 2SS present a similar behavior and significantly lower than the 2S. While, Fig. 6 shows the behavior of the PLLs before voltage dips where the 2SS presents a median of the overshoot of the peak phase error (1.4º) and a response time similar to the SOGI (2275 ms).

Figure 7 shows the waveforms measured in the converter in simulation using PLECS® from Plexim. The mains voltage includes a noise until 5% that the PLL can filter to generate a sinusoidal signal (in yellow) that is insensitive to noise. For its part, the current measured in the coil presents a deformation in the passage through zero of the positive half cycles due to the subsequent reconstruction of the input voltage from the polarity signal. Also, the ripple of the output signal is not affected by noise in the input voltage.

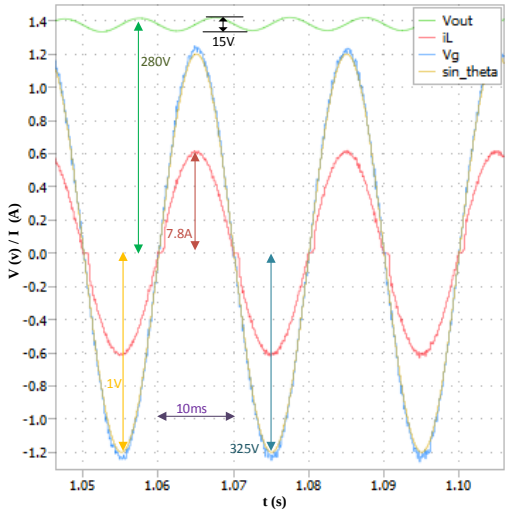


Fig. 7. Grid voltage (blue), current (red), output voltage (green) and sinϴ (yellow) waveforms using proposed 2SS PLL in steady-state with noise until 2 % of the V_g.

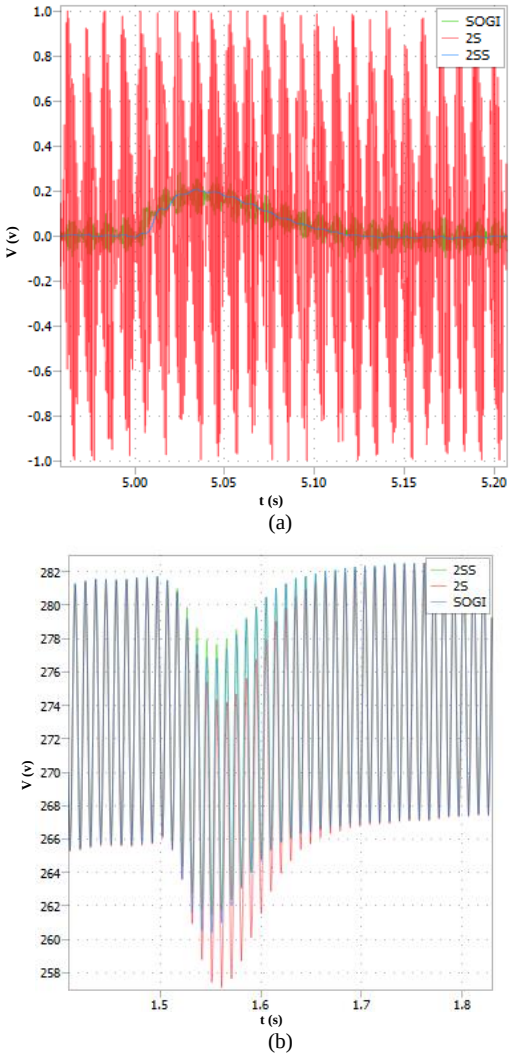
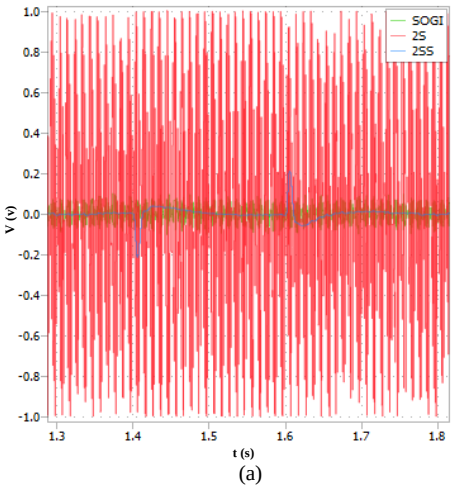
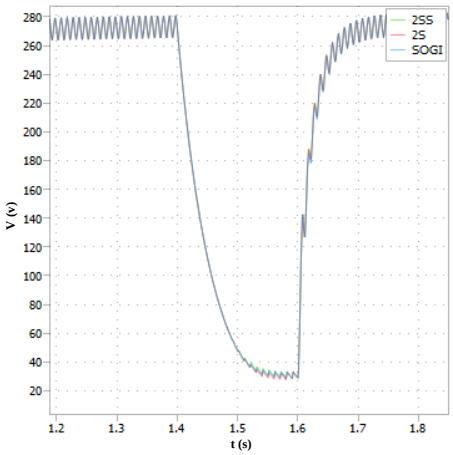


Fig. 8. Waveforms of the a) phase error of the analyzed PLLs and b) output voltage under frequency jumps of +2 Hz (from 49 to 51 Hz) and noise of 5% of V_g.



(a)



(b)

Fig. 9. Waveforms of the a) phase error of the analyzed PLLs and b) output voltage under voltage dips of 50% during 200 ms and noise of 5% of V_g.

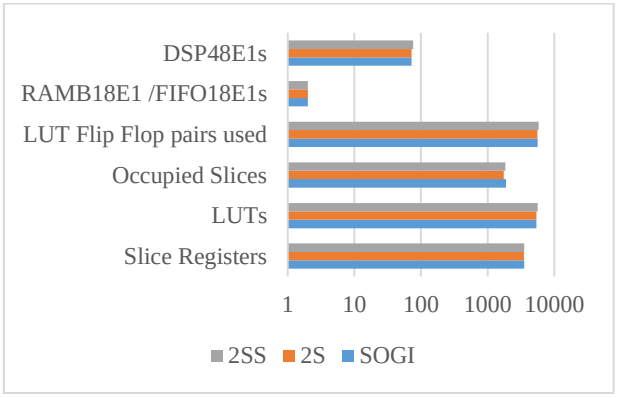
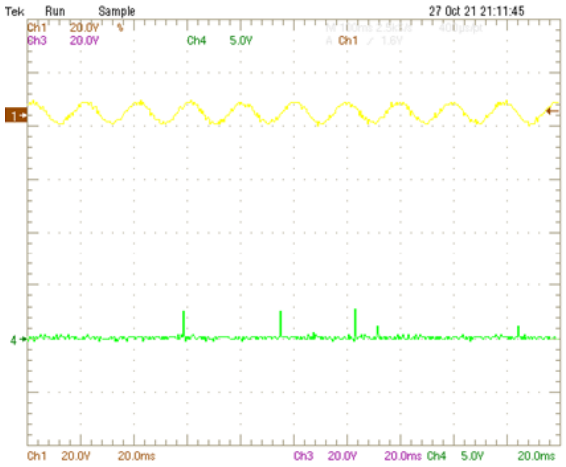


Fig. 10. Summary of the FPGA resources used by different methods analyzed using Sysgen.

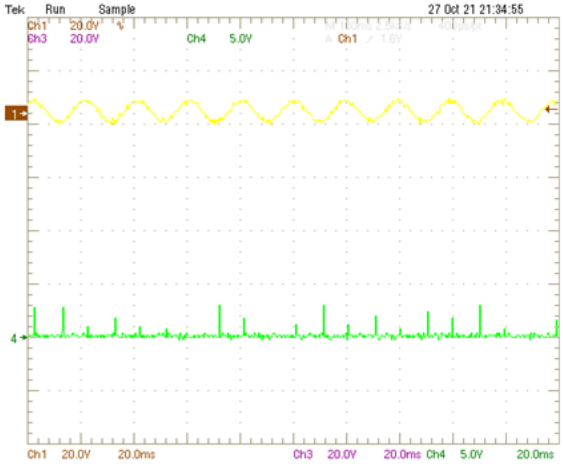
Figure 8 shows the phase error of the PLLs implemented in the control (Fig. 8.a) and how their performance affects the output voltage of the Totem Pole converter. In it, it can be seen that the 2SS shows a phase error without ripple which means a smaller reduction in the output voltage in the converter. While the 2S is highly affected by noise, which is the largest drop in output voltage values. For its part, Fig. 9 shows the behavior of the same parameters but before a voltage dip of 50% of 200 ms, where the phase error presents values equivalent to those of Fig. 8.a but its influence the output voltage is very similar in all cases. Although, again, the 2SS shows a smaller decrease and the 2S a greater one.

IV. EXPERIMENTAL RESULTS

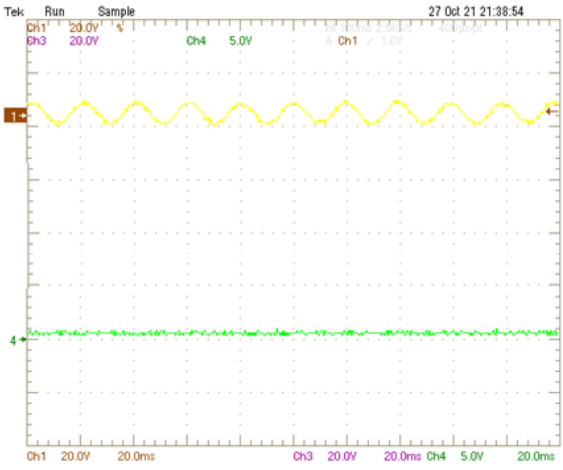
Analyzed PLLs have been implemented in a FPGA to study their behavior and computational burden. In Fig. 10, a summary of the resources used in the FPGA is presented for the different strategies analyzed.



(a)



(b)



(c)

Fig. 11. Grid voltage (yellow) and phase error (green) in steady state. a) SOGI, b) 2S and c) 2SS PLL.

Figure 11 shows the performance of the PLLs in a steady state in a FPGA, where the phase error committed by the 2SS PLL is minimal, while the SOGI and the 2S PLL present peak values that raise both average phase errors. However, comparatively, the 2S is the PLL that is most affected by noise due to these peak values.

V. CONCLUSIONS

A new smoothing filtering structure has been embedded in the 2S-PLL synchronization circuit; whose original version lacks noise filtering capacity. Based on this approach, the PLL has been implemented, tested and verified, observing that the phase error that occurs with the proposed PLL is lower, both at steady state and under different perturbations, than the original 2S and similar to the behavior of the SOGI PLL, while the circuit uses similar hardware resources than SOGI.

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