Study of Drain Injected Breakdown Mechanisms in AlGaN/GaN-on-SiC HEMTs

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***Abstract*—Breakdown mechanism in 0.25 µm gate length AlGaN/GaN-on-SiC iron doped HEMTs with background carbon is investigated through the drain current injection technique. The measurement results reveal that it can be divided into two distinct stages according to the gate voltage levels. The first stage of the measured drain injected breakdown is mainly due to the initiation of the punch-through process under the gate, and the second stage of breakdown is associated with the potential barrier between the unintentionally doped GaN and the Fe doped p-type GaN buffer layer which also has a higher carbon density. The electroluminescence (EL) results suggest that the first stage shows uniform punch-through current flow, but localized leakage current flow associated with a snapback breakdown mechanism replaces the uniform punch-through current flow and dominates the second stage. A 2D-TCAD simulation has been implemented and shows the current paths under uniform flow conditions.**

***Index Terms*—GaN, HEMT, breakdown, punch-through, impact ionization.**

I. Introduction

Large bandgap enables GaN to withstand high breakdown fields which with high mobility and saturation velocity makes it suitable for high power/RF applications. Recent advancement in epitaxy and device processing has enabled excellent performance during RF and high-power switching applications for AlGaN/GaN high electron mobility transistors (HEMT) [1][2]. However, the high-power RF application is still a vulnerable regime for device breakdown since a high voltage may be reached for instance during switching or with a mismatched load.

Several drain breakdown mechanisms have been suggested taking part in different regions of the device. Meneghesso et al. [3] summarized four types of breakdown mechanisms – vertical breakdown, drain-gate breakdown due to surface/gate issues, source-drain punch-through and impact ionization. Vertical breakdown is usually limited by the maximum breakdown voltage of the bulk GaN buffer and the substrate. An increase in drain current at high drain voltages (and in pinch-off conditions) can be ascribed to punch-through effects [4], i.e., to the flow of source-drain current within the bulk of the GaN layer under the gate. Using a 2D-TCAD simulation it was demonstrated that like other types of field-effect devices AlGaN/GaN single heterojunction devices are vulnerable to short-channel effects and demonstrated the necessity for deep acceptors to be incorporated in the GaN buffer to make it more insulating and confine the carriers in the channel. This is now normally achieved by the use of Iron (Fe) or Carbon deep acceptors. In another model, Tan et al. [5] explained the surface breakdown model as they attributed the breakdown at high drain voltages to a thermal surface-hopping process, which occurs when a certain power threshold is reached by surface current conduction, however, the current generation of devices shows much-improved surface passivation which suppresses that effect.

Most conventional breakdown measurements involved irreversible damage or degradation to the device until Bahl et al. [6] first reported a current controlled breakdown method and called it drain-current injection technique, which enabled a study of the physics of breakdown in InAlAs/InGaAs HFETs. In this method, the source is kept grounded, and a constant drain current is injected into the device. The gate voltage is then ramped down to shut the device off leading to a rise of the drain-source voltage. This off-state drain-source voltage in-principle represents an unambiguous definition of three-terminal breakdown voltage. This unique technique gives the advantage of avoiding repetitive scanning and reduced the risk of burnout in unstable and fragile devices. Using this technique Wang et al. [7] suggested that the source injection through the buffer can also induce impact ionization and cause a premature three terminal breakdown in conventional AlGaN/GaN HEMTs.

In this work, we present a new breakdown study using drain current injection and electroluminescence (EL) for an Fe doped GaN-on-SiC HEMT with known distribution of unintentionally incorporated carbon. Simultaneous measurements of the drain, source and gate current allows us to present direct evidence of high source current injection under OFF-state condition through the buffer (punch-through effect) dominating over gate current. In these devices the breakdown can be divided into two distinct stages with varying gate voltages. We use 2D-TCAD device simulation to replicate the uniform current flow measurement scenario, and propose that the two stages can be explained by the presence in these devices of two distinct densities in the

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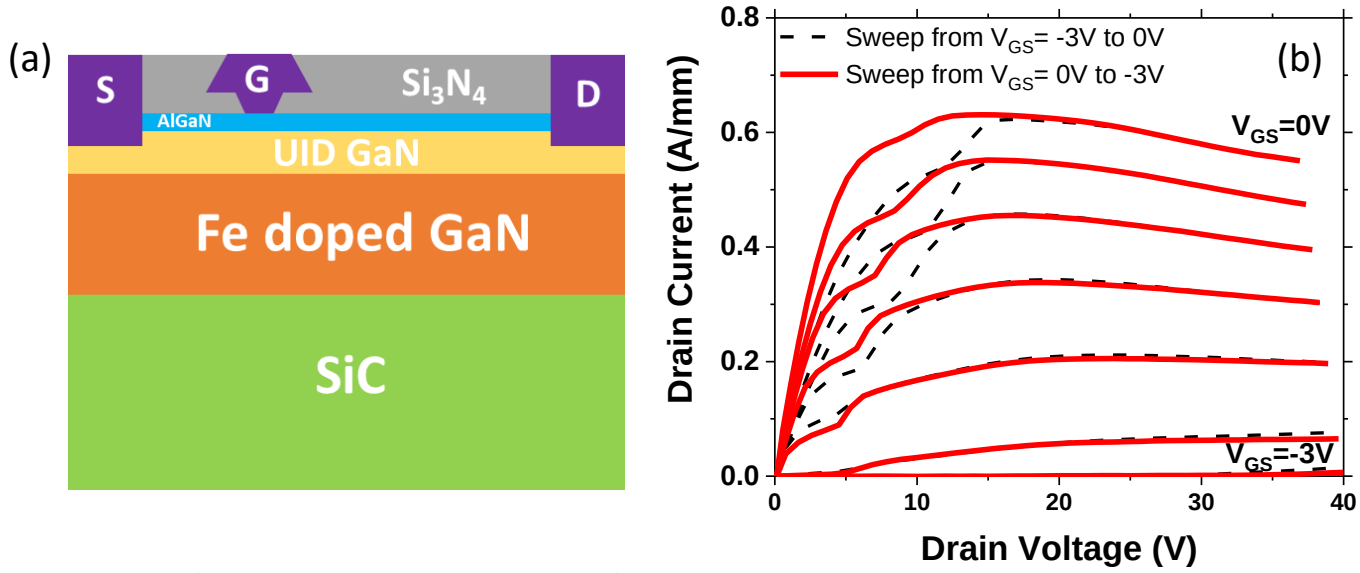

Fig. 1. (a) Schematic of the device under test. (b) DC measurements performed on the device under test.

background carbon density as a function of depth. From the EL measurements, we show that in the second phase uniform punch-through is suppressed and replaced by a strongly localized breakdown with associated negative resistance requiring significantly lower field than punch-through. This study provides further insights into the range of possible breakdown mechanisms for AlGaN/GaN HEMTs.

II. Experimental Results

In this study, the device under test uses a MOCVD grown structure of an AlGaN barrier, a GaN buffer and an AlGaN nucleation layer on an insulating SiC substrate. Fe as a dopant has been used and SIMS measurements show a conventional Fe doping profile in the GaN bulk with a peak density of 3×10^{18} cm^{-3} which decreases exponentially to 7×10^{15} cm^{-3} at the surface. Carbon is always incorporated unintentionally during MOCVD growth. In this case SIMS measurements showed that as a result of a change in growth conditions 0.2 µm below the AlGaN barrier, the carbon density was 5×10^{16} cm^{-3} in the 0.2 µm channel layer whereas the deeper bulk of the GaN had a higher carbon density of $3 \pm 1 \times 10^{17}$ cm^{-3} (we note that a density of carbon contaminants in the 10^{17} cm^{-3} range has been reported for Fe doped Cree epitaxy [8]). Oxygen and silicon were below the SIMS background of 5×10^{15} cm^{-3}. The device schematic can be seen in Fig. 1 (a). The device under study has a width of 2 × 125 µm, a gate length of 0.25 µm, a source-drain spacing of 4 µm, and source-gate spacing of 1 µm. It was fabricated using Ti/Al/Ni/Au and Ni/Au for Ohmic and Schottky contact respectively, and with silicon nitride as a passivation layer. The 2DEG Hall mobility, the 2DEG sheet density and the sheet resistance are 1770 cm^2/Vs, 1.143×10^{13} cm^{-2} and 340 Ω/sq.

DC measurements up to 40 V drain bias with 1 V/sec sweep rate are shown in Fig. 1 (b) with kink seen at 3-5 V above the knee. A detailed study on the origin of kink in this wafer, explained using the p-type floating buffer that results from the presence of the relatively high background carbon level in the bulk, can be found in [9][10] and RF measurements in [11].

Conventional voltage-driven off-state breakdown measurements were performed as shown in Fig. 2 (a). When the gate-source voltage (V_{GS}) is below threshold and between -3 and -6 V, the breakdown voltage (at the compliance current of 1mA) increases from -10 to -40V. For V_{GS} < -6 V, the off-state breakdown voltage increases rapidly to above 210 V. However when measured using the current-driven drain injected breakdown technique, as shown in Fig. 2 (b), (c) and (d), a complementary and somewhat different behavior is observed. A fixed predefined current is injected into the drain, V_{GS} is ramped down from 0 V to below the threshold, and the drain voltage, gate current (I_G) and source current (I_S) are monitored. Fig. 2 (b) shows the measured V_{DS} for different I_D starting from 1 nA and all the way up till 1 mA. At low drain current ($I_D \leq 1$ µA), the drain voltage appears to be almost negligible with the current supplied from the gate leakage, and there is no breakdown. At higher drain current which exceeds the gate leakage ($I_D \geq 100$ µA), the results show there are two distinct stages of drain breakdown. The first stage appears below the threshold when V_{GS} = -2.5 V with V_{DS} in the range 30 - 40V, with the second stage when V_{GS} < -7 V associated with a rapid increase in V_{DS} to 90-120V. We note that this is significantly lower than that observed with the voltage-driven measurement where the breakdown voltage was > 210V. To clearly identify the leakage/breakdown paths, in Fig. 2 (c) and (d) the gate and source currents are plotted as V_{GS} is swept from 0 V to -10 V. For I_D < 100 µA, the gate-to-source leakage current is significant and is much larger than the drain injected current as V_{GS} swept to -10 V. For $I_D \geq 100$ µA, the drain-to-source current dominates, although the gate current starts to contribute to the drain injected current for more negative V_{GS} (nevertheless drain-source dominates with $\{I_G/I_D\}_{max}$ < 35% and $\{I_S/I_D\}_{min}$ > 65%).

To help understand the breakdown mechanism, electroluminescence (EL) microscopy was carried out with a 50× objective and Opticstar charge-coupled device (CCD) camera under biased conditions. EL emission measured is shown in Fig. 3 for I_D of 1mA, together with the points on the V_{DS}-V_{GS} curve at which the EL was measured. Although there is significant hysteresis between forward and reverse sweeps,

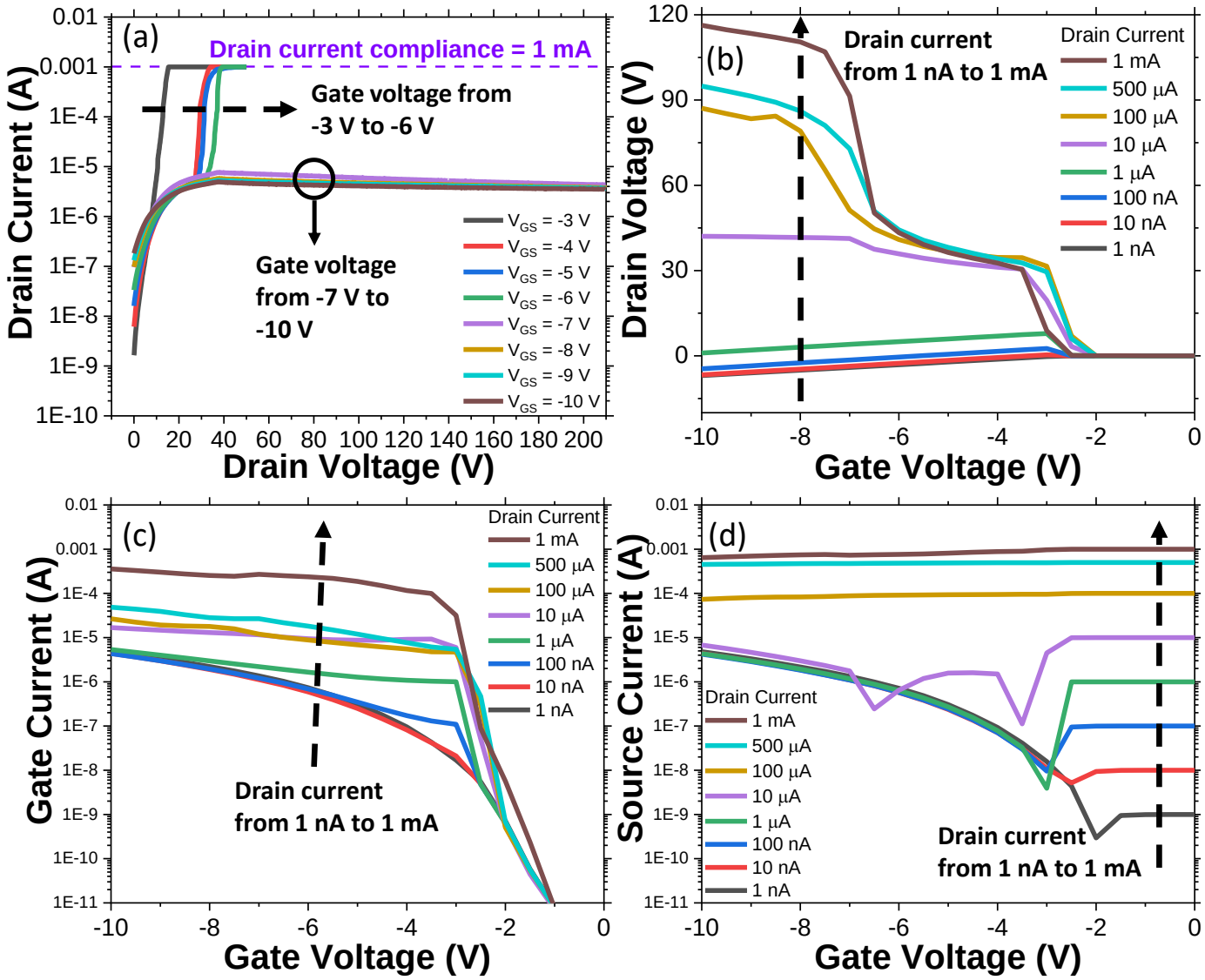

Fig. 2. (a) Shows off-state breakdown measurement results with a drain current compliance 1 mA (V_{GS} is swept from -3 V to -10 V). (b) Shows the measured drain voltage during the drain injected breakdown measurements for a range of I_D bias changing from 1 nA up to 1 mA (V_{GS} is swept from 0 V to -10 V). (c) Shows the measured gate current during the drain injected breakdown measurements for a range of I_D bias changing from 1 nA up to 1 mA (V_{GS} is swept from 0 V to -10 V). (d) Shows the measured source current during the drain injected breakdown measurements for a range of I_D bias changing from 1 nA up to 1 mA (V_{GS} is swept from 0 V to -10 V).

they show basically similar EL results. In Fig. 3, at the first stage of the breakdown (-6 V ≤ V_{GS} ≤ -3 V), the EL is observed reasonably uniformly across the width of the gate finger. However, at the second stage when V_{GS} < -6 V, the EL emission splits into several localized bright spots which appear in the middle of the gate finger in the reported device, and are associated with locations where there was no EL emission during the first stage. The second stage was accompanied by a strong reduction in uniform emission across the width of the gate, and this suppression was not simply due to the change of the image contrast but was a real reduction of the EL emission. This suppression, and the associated increase in breakdown voltage, means that this stage is not just the result of the onset of localized gate leakage. This measurement has been repeated across several devices on two different processed wafers with the same epitaxy design, and similar behavior was observed and was repeatable.

EL spectra were recorded with a broad-spectrum fibre coupled to a compact spectrometer (Maya 2000–Ocean optics QEPro) sensitive in the range 200–1100 nm and measured across different bias points shown here in Fig.4. To access light emitted under the gate, the EL spectra measurements were performed from the back side of the device through the transparent GaN layer and SiC substrate. No significant EL signal was observed till V_{GS} = -4 V and beyond that broad EL distributions can be found between the photon energy of 2.4 to 3.6 eV. Correction of interference fringes due to the multi-layer buffer/substrate has not been applied to Fig. 4, so the data was not used for quantitative analysis of the electron temperature [12].

III. Simulation

2D-TCAD simulation using Silvaco Atlas has been implemented to help to interpret our measurement results. The simulated device is represented by a broadly similar structure which consists of a 22-nm AlGaN barrier, a 0.2-µm unintentionally doped (UID) GaN channel layer, a 1.6-µm

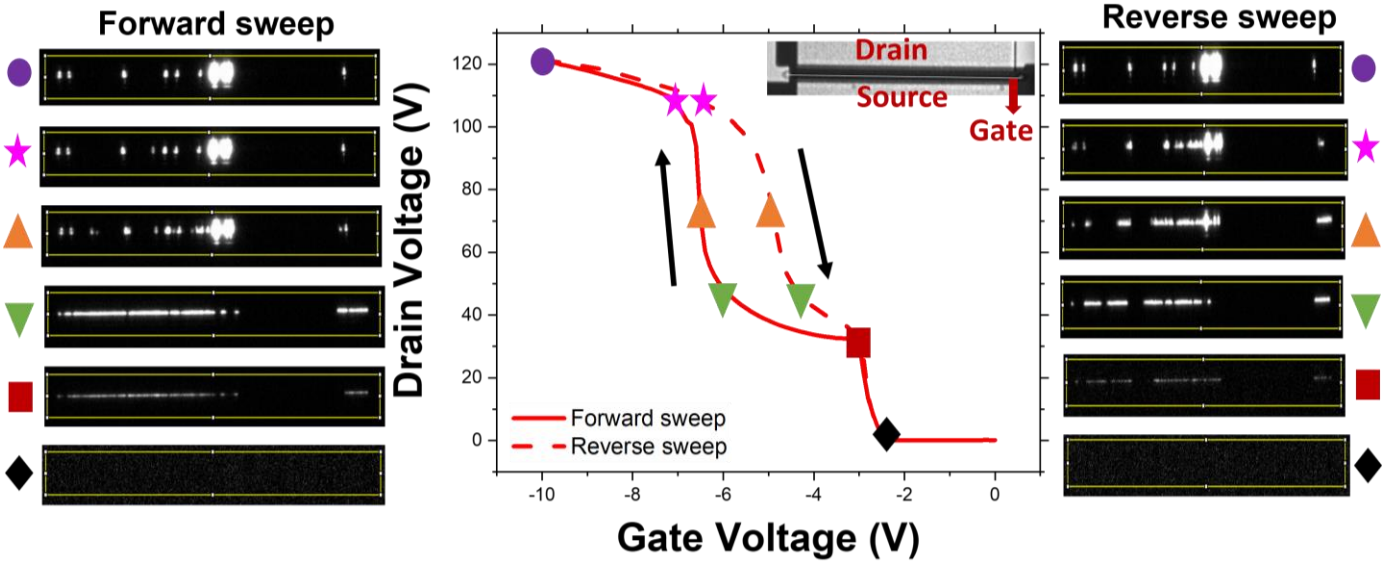

Fig. 3. Measured EL intensity for range of V_{GS} bias between 0 V and -10 V (I_D = 1 mA) with forward and reverse sweeps.

doped GaN layer, and a 2-µm SiC substrate. The doping density profile matches the measured secondary ion mass spectrometry SIMS profiles of Fe and C [9]. The Fe acceptor (E_c-0.7 eV) has been doped with the density of 7×10^{15} cm^{-3} at the GaN surface and it increases exponentially with depth to 3×10^{18} cm^{-3} at 1.1 µm below the GaN surface and then keeps constant. The C atoms in GaN can be deep acceptors (C_N), shallow donors (C_{Ga}), or complexes, and there can also be intrinsic donors. The modelled UID GaN is doped with 3×10^{16} cm^{-3} carbon deep acceptor (C_N, E_v+0.9 eV) and 2×10^{16} cm^{-3} shallow donors (C_{Ga} and intrinsic donors, E_c-0.03 eV). The doped GaN is doped with 2×10^{17} cm^{-3} C deep acceptor (C_N, E_v+0.9 eV) and 1×10^{17} cm^{-3} shallow donors (C_{Ga} and intrinsic donors, E_c-0.03 eV) giving a compensation ratio of 0.5. This doping profile will finally result in a p-type buffer as the Fermi level is pinned at about E_v+0.97 eV with the Fe neutral except near the surface [10]. Band-to-band leakage paths have been added under the source and drain contacts by adding heavily doped p-type shorts, which allows hole flow from the contact to the buffer [13]. The impact ionization model is enabled in this simulation.

Fig. 5 (a) and (b) shows the simulated current density profiles

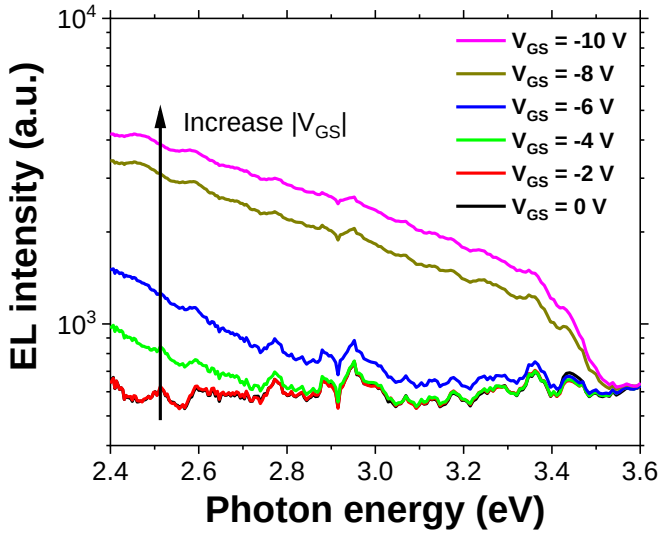

Fig. 4. The EL spectra measured from the backside of the device at different gate bias (I_D = 500 µA).

with I_D = 1 mA and V_{GS} = -3 and -10 V respectively. In Fig. 5 (a), the 2DEG under the gate is just fully depleted, and a punch-through current path can be found within the UID GaN. In Fig. 5 (b), when V_{GS} = -10 V, the trace of punch-through current is pushed down further into the p-type doped GaN layer. In this simulation, the high electric field near the gate edge in Fig. 5 (b) leads to impact ionization which generates free holes and the hole current to the gate which is labelled as "gate leakage". However, in the real device, the gate leakage mechanism can be defect-related, and the impact ionization may not be the primary reason for the gate leakage.

IV. Discussion

The questions we have to answer are, why do devices with this epitaxial design show the unusual and interesting feature of a two-stage breakdown, and why is the breakdown voltage in the second stage different for voltage and current-driven measurements. To help us understand this phenomenon, an equivalent circuit of the device is plotted in Fig. 6, where the channel is represented by resistors (R_S, $R_{G,2DEG}$, R_D) in series, and the gate is represented by a Schottky diode ($D_{Schottky}$) under reverse bias. The highly resistive buffer is connected by diodes and resistors in parallel, and the left diodes ($D_{L,i}$) are under reverse bias and the right diodes ($D_{R,i}$) are under forward bias with a pinched-off gate voltage. However, for the GaN buffer, the barrier on the left side of the gate ($D_{L,i}$) for electron flow can be lowered (as gate voltage becomes less effective in the deep GaN buffer) as a result of back-gating by the drain field. This would result in a punch-through minority carrier electron current flowing through $R_{G,i}$ to the drain [4].

The first drain voltage plateau is observed below the threshold voltage once the 2DEG channel at the AlGaN/GaN interface has been depleted by the gate. That means, in the equivalent circuit, $R_{G,2DEG}$ is highly resistive and it requires the punch-through electron current flowing through $D_{L,1}$, $R_{G,1}$ and $D_{R,1}$. It finally leads to a high drain voltage plateau. The simulation in Fig. 5 (a) shows the same process. The EL plots in Fig. 3 indicate that the punch-through current is flowing reasonably uniformly across the entire width of the gate.

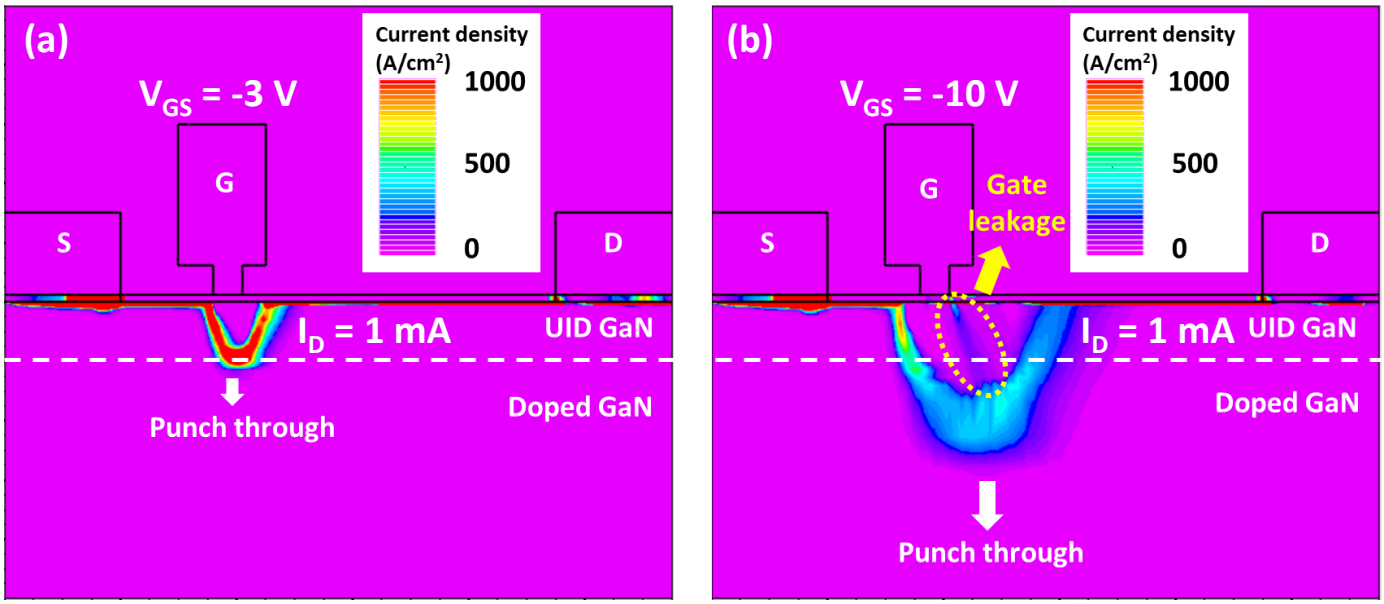

Fig. 5. Simulated current density distribution (a) When V_{GS} = -3 V and I_D = 1 mA, the 2DEG under the gate is fully pinched-off and the remaining electrons within the UID GaN provide a path for the punch-through current. (b) When V_{GS} = -10 V and I_D = 1 mA, the punch-through path has been pushed down to the heavily doped GaN layer.

As the gate voltage is swept to beyond -6 V, a second drain voltage plateau can be found. Guided by the simulation in Fig. 5 (b), we propose that during the second stage the UID GaN channel layer has been depleted completely by the gate and as a result the punch-through current path has been pushed down further into the more heavily doped GaN layer. In the epitaxy used here, the C concentration is higher than that in the channel UID GaN guaranteeing that the doped GaN layer is p-type. Note that the Fe doping is also more heavily doped, but it is neutral and therefore has relatively little effect on the transport. Meanwhile, the junction between the UID GaN and the doped GaN serves as a potential barrier for the current flowing through it. The higher doping and Fermi-level pinning in the lower half of the gap increases the barrier for punch-through, and lowers electron lifetime, providing a plausible explanation for an abrupt increase of drain voltage during the second stage required to force a current-driven punch-through current to flow through $D_{L,i}$, $R_{G,i}$, $D_{R,i}$.

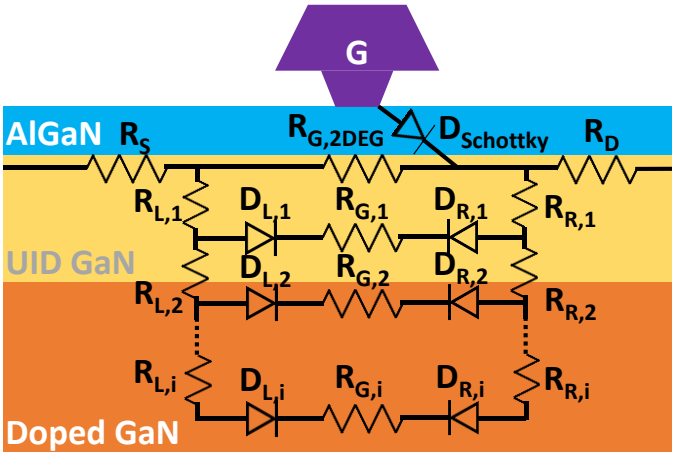

Fig. 6. Shows the equivalent circuit under the gate. The resistances of the resistors in parallel ($R_{G,2DEG}$, $R_{G,1}$, $R_{G,2}$,…, $R_{G,i}$) under the gate are dependent on the gate voltage. As the gate voltage is swept to negative, these resistors ($R_{G,2DEG}$, $R_{G,1}$, $R_{G,2}$,…, $R_{G,i}$) will become less conductive from the top to bottom. The diodes ($D_{L,i}$, $D_{R,i}$) represents the condition for the electron current when a pinched-off gate voltage is applied.

The EL results show a key difference between the stages. In the second stage, the EL distributed across the gate width is suppressed as bright spots appear somewhere near the gate finger. For these locations with the bright spots, a plausible explanation is that these are associated with defect regions which will only conduct when the electric field is high enough. Once these preferential leakage paths are formed locally, they show strong conductivity, and sustain the majority of the injected source-drain current, while the resulting voltage drop across the rest of the gate width is still not sufficient to allow punch-through. Therefore, the regions without localized leakage do not show EL emission during the second stage. This new breakdown mechanism is highly localized and it is worth reiterating that the bright spots found in the second stage correspond to the dark spots in the first stage, consistent with a defect origin. Therefore, the simulation result in Fig. 5 (b) only shows the ideal case without the localized leakage paths. The fact that the measured off-state voltage-driven breakdown voltages are larger than that of the drain injected measurements during the second stage in Fig. 2 suggest the presence of a snap-back or negative-resistance mechanism associated with the localized transport through the more heavily carbon doped layer. We note that Koller et al [14] have reported negative resistance and a localized breakdown mechanism in carbon doped bulk GaN structures, with associated localized EL light emission. Some of their localized breakdowns were pinned to dislocations, although here the precise nature of the defects is unknown. The forward and reverse sweeps shown in Fig. 3 confirm that the process is reversible and does not lead to a permanent device failure. The strong hysteresis observed in the transition between uniform conduction in stage 1 and localized conduction in stage 2 is also consistent with the presence of negative resistance similar to that seen in [14]. There may also be negative charge trapping in the buffer. Negative charges due to ionized carbon deep acceptors (C_N) can accumulate under the high drain bias and back-gate the channel and reduce the carrier density in the UID GaN leading to hysteresis [13].

The broad emission spectra in Fig. 4 suggest that the EL emission in both stages primarily originates from Bremsstrahlung radiation as hot electrons lose their energy when deflected by charged particles rather than band-to-band emission [12]. Hence, the presence of EL emission indicates where the high electrical fields and current densities are simultaneously present [15][16] but does not necessarily indicate strong impact ionization. The increase in gate leakage seen as the injected drain current increases is presumably associated with the presence of impact ionization. However, since the majority of drain current flows to the source, it is reasonable that a mechanism is occurring which does not necessarily rely on impact ionization, as is suggested here.

V. Conclusion

In this paper, we compare conventional voltage-driven and the drain-current injection technique to investigate how the breakdown mechanism evolves under different bias conditions in a Fe doped AlGaN/GaN-on-SiC HEMT with moderately high lower-buffer carbon concentration. We show that the measurement approaches are complementary and together deliver additional insight. Initially, when the device is pinched-off, the punch-through mechanism dominates the process. However, as the channel is fully depleted, the punch-through path will be forced down into the heavily doped and Fermi-level pinned p-type GaN buffer, and the drain voltage reaches a higher plateau. At this stage, the EL results reveal a new breakdown mechanism where the localized current associated with pre-existing defects becomes dominant while the punch-through current flow in the rest of the device is not significant due to the high potential barrier between the GaN layers. This study helps to understand the relationship between the breakdown mechanism, the punch-through effect and the buffer conditions in RF GaN HEMTs.

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