Comparison of Short Circuit Failure Modes in SiC Planar MOSFETs, SiC Trench MOSFETs and SiC Cascode JFETs

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***Abstract*—In this paper, a comprehensive comparative analysis is performed on the short circuit (SC) withstand time and failure modes between a 650 V SiC Planar MOSFET, a 650 V SiC Trench MOSFET and a 650 V SiC Cascode JFET. The short circuit tests have been performed at a DC link voltage of 400 V with gate turn-OFF voltages at 0 V and -5 V. The results show that the SiC Cascode JFET failed in a source-to-drain short circuit with the gate still capable of blocking voltage while the SiC Planar and Trench MOSFETs failed with the Gate-Source (V_{GS}) terminal short circuited and Drain-Source (V_{DS}) terminals still capable of blocking voltage. Furthermore, short circuit withstand times measured on the SiC Planar and Trench MOSFETs showed an increase (20% for the Planar MOSFET and 9% for the Trench MOSFET) when the device gate voltages were turned-OFF with -5V compared to 0V. This was due to the increased inductance of the negative voltage gate driver reducing the peak short circuit current. In the case of the SiC Cascode JFET, there was no dependence of the short-circuit withstand time on the V_{GS} turn-OFF voltage.**

Keywords—short circuit, SiC MOSFET, cascode, planar, trench

I. INTRODUCTION

As SiC devices are increasingly gaining popularity in low and medium voltage power electronic applications, the failure mode of the different devices under short circuit (SC) conditions is increasingly important to assess. The higher junction-to-case thermal impedance and reduced oxide quality in SiC MOSFETs compared to silicon devices means reduced SC robustness (measured by the SC withstand time) compared to comparatively rated silicon devices [1, 2]. Furthermore, the gate oxide in SiC MOSFETs has been observed to fail during short circuits [3-7]. The input of a SiC Cascode JFET is a low voltage silicon MOSFET (driving a high voltage SiC JFET), hence, the failure mechanism is SiC Cascode JFETs under short circuits is different. This paper compares SC failure modes in SiC MOSFETs and Cascode JFETs and also investigates the impact of the turn-OFF V_{GS} on the short circuit withstand time for both technologies.

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II. EXPERIMENTAL RESULTS

Fig. 1(a) shows the short circuit test set-up while Fig. 1(b) shows the circuit diagram. The test set-up comprises of a high current silicon IGBT (with datasheet reference FF1000R17IE4) for isolating the devices under test from the DC power supply. Fig. 2 shows the short circuit measurements performed on the 650V SiC Cascode JFET (with datasheet reference UJ3C065080K3S).

Fig. 2(a) shows the short circuit currents for different durations while Fig. 2(b) and Fig. 2(c) shows the corresponding V_{GS} and V_{DS} transient voltages. The turn-OFF V_{GS} voltage of these measurements was set at 0V.

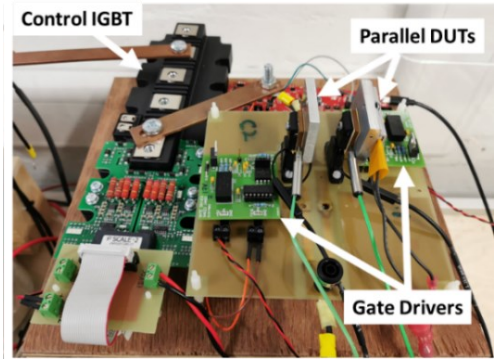

Fig. 1(a). Short circuit test rig

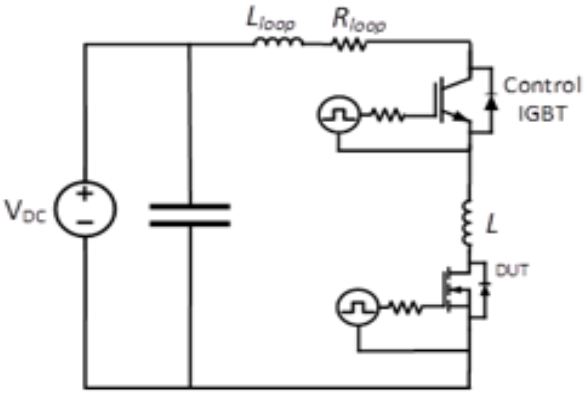

Fig. 1(b). Short circuit test circuit schematic

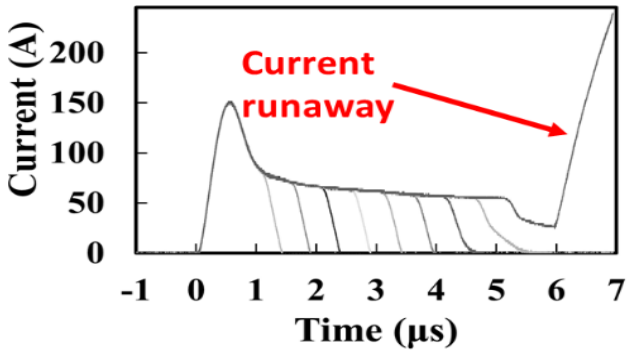

Fig. 2(a). Short circuit withstand time measurement for SiC Cascode JFET

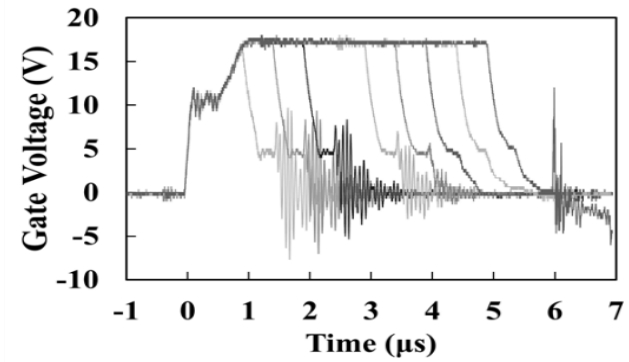

Fig. 2(b). Short circuit V_{GS} transients for different short circuit durations

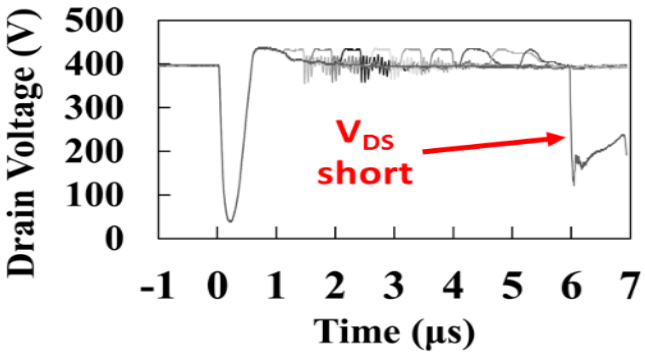

Fig. 2(c). Short circuit V_{GS} transients for different short circuit durations

The maximum measured short circuit withstand time for the Cascode JFET is 5µs (this was confirmed on 4 more devices). Subsequent failure analysis showed a drain-source short circuit with the gate terminal still able to block voltage. SC measurements performed on the SiC Cascode JFET with turn-OFF V_{GS}=-5V yielded identical results.

Fig. 3(a) compares the measured SC currents for the SiC Cascode JFET with turn-OFF V_{GS} voltages at 0V and -5V while Fig. 3(b) compares the measured drain-source voltages during the SC measurements. The measurements in Fig. 3 are the last pass measurements before device failure.

SC measurements are shown in Fig. 4 for the 650V SiC Planar MOSFET (with datasheet reference C3M0120065D) with V_{GS} turn-OFF voltage set at 0V. Fig. 4(a) shows the SC current, 4(b) shows the V_{GS} and 4(c) shows the V_{DS}. Unlike the SiC Cascode JFET, the SiC MOSFET failed with the gate-source terminal shorted and the drain-source still capable of blocking voltage (there is no rising current).

Similar measurements (shown in Fig. 5) performed with turn-OFF V_{GS} set at -5V for the planar MOSFET showed a 20% increase in the maximum short circuit withstand time. Comparative analysis shows that as the turn-OFF V_{GS} is reduced from 0V to -5V, the peak short circuit current reduces, hence, the maximum withstand-time increases. The short circuit energy is 251 mJ and 246 mJ for V_{GS}=0V and V_{GS}=-5V respectively

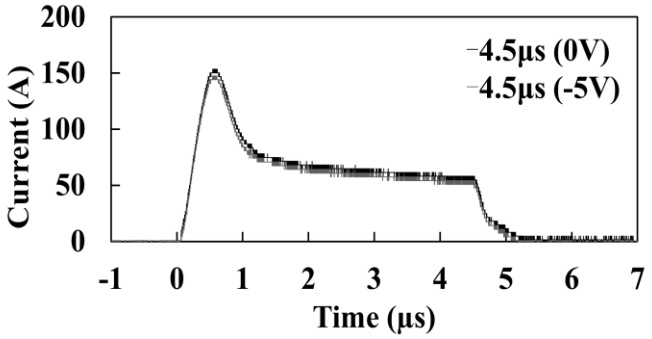

Fig. 3(a). Short circuit current measurements for the SiC Cascode JFET with turn-OFF V_{GS}=0V and -5V

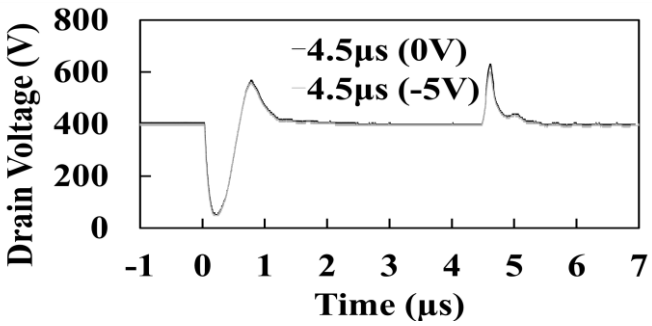

Fig. 3(b). Short circuit V_{DS} measurements for the SiC Cascode JFET with turn-OFF V_{GS}=0V and -5V

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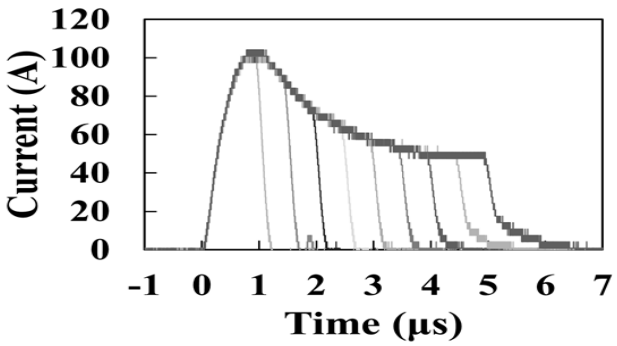

Fig. 4(a). SC withstand time measurement for Planar SiC Planar MOSFET

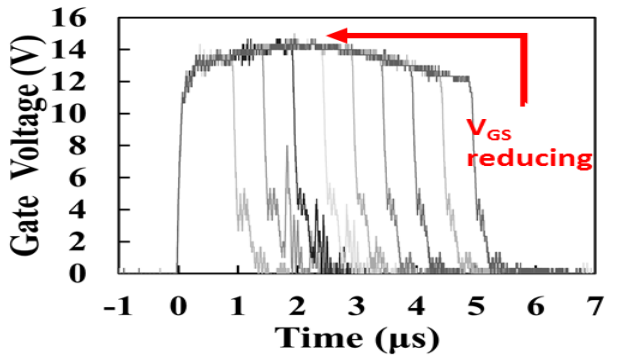

Fig. 4(b). Short circuit V_{GS} transients for different short circuit durations

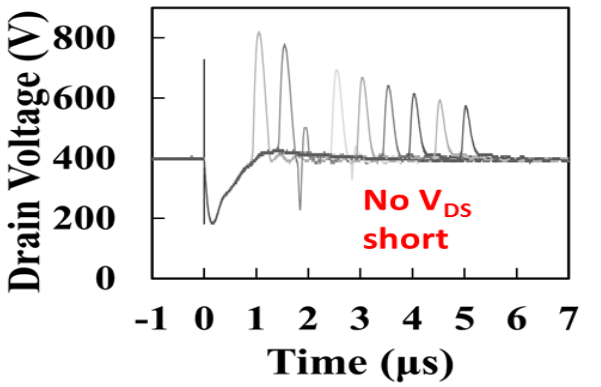

Fig. 4(c). Short circuit V_{DS} transients for different short circuit durations

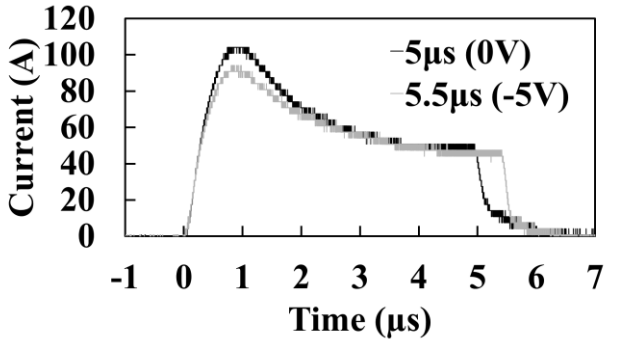

Fig. 5(a). Short circuit current measurements for the SiC Planar MOSFET with turn-OFF V_{GS}=0V and -5V

Fig. 6(a) and Fig. 6(b) show the last pass SC measurements performed on a 650V SiC Trench MOSFET with datasheet reference SCT3080AL. Similar to the SiC Planar MOSFET, the SC withstand-time increases as the turn-OFF V_{GS} is set to -5V instead of 0V (and also, the device V_{GS} fails in short indicating gate oxide failure). The SC withstand time is higher for the SiC Trench MOSFET because it is a larger chip and therefore has a higher thermal resistance (0.86 K/W for the Trench, 1.53 K/W for the Planar MOSFET and 0.70 K/W for the SiC Cascode JFET). The chips were de-capsulated, and the die dimensions were measured as 2.92 mm^2, 2.89 mm^2 and 6.25 mm^2 for the SiC Cascode JFET, SiC Planar MOSFET and the SiC Trench MOSFET respectively. This yielded a short circuit energy density of 87.4 mJ/mm^2, 87 mJ/mm^2 and 127 mJ/mm^2 for the SiC Cascode JFET, SiC Planar MOSFET and the SiC Trench MOSFET respectively. It is clear from the measurements that the SiC Cascode JFET has a different failure mechanism hence, the next section uses finite element simulations to investigate SC failure in the SiC Cascode JFET.

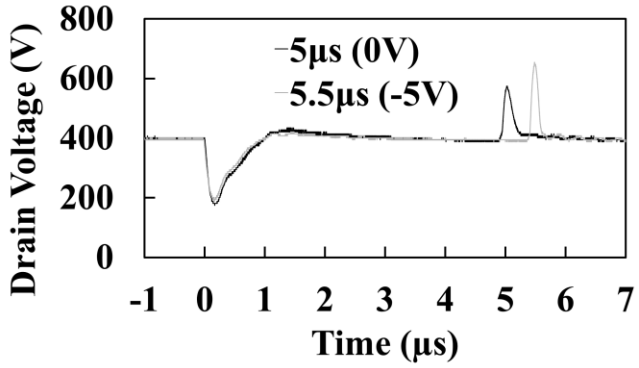

Fig. 5(b). Short circuit V_{DS} measurements for the SiC Planar MOSFET with turn-OFF V_{GS}=0V and -5V

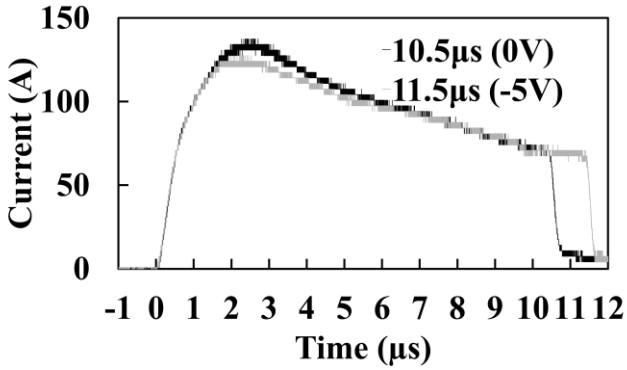

Fig. 6(a). Short circuit current measurements for the SiC Trench MOSFET with turn-OFF V_{GS}=0V and -5V

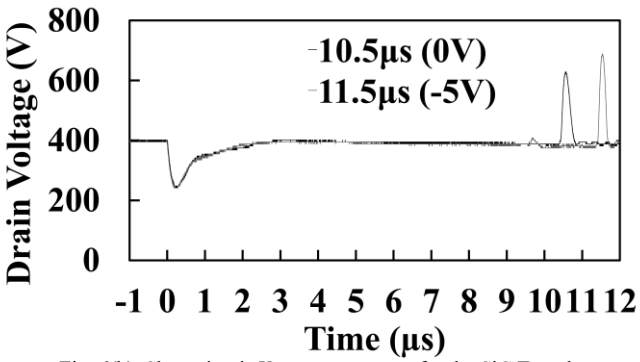

Fig. 6(b). Short circuit V_{DS} measurements for the SiC Trench MOSFET with turn-OFF V_{GS}=0V and -5V

III. FINITE ELEMENT SIMULATIONS

Finite element simulations of the SiC Cascode JFET under short circuit conditions have been performed in SILVACO to understand the failure mode. In the simulations, the JFET source doping is $1x10^{19}$ cm^{-3}, the gate doping is $1x10^{19}$ cm^{-3}, drift layer doping is $2.33x10^{16}$ cm^{-3}, the drift layer thickness is 6 µm, the channel width is 1 µm. Fig. 7(a) shows the simulated short circuit current characteristics including failure by thermal runaway. Fig. 7(b) shows the simulated 2D current density contour plots extracted from the simulator at a time instant during thermal runaway. Fig. 7(b) shows high current density levels (between 10 and 100 A/cm^2) in the gate PN junction which should normally be depleted during turn-OFF since the gate PN junction is reverse biased.

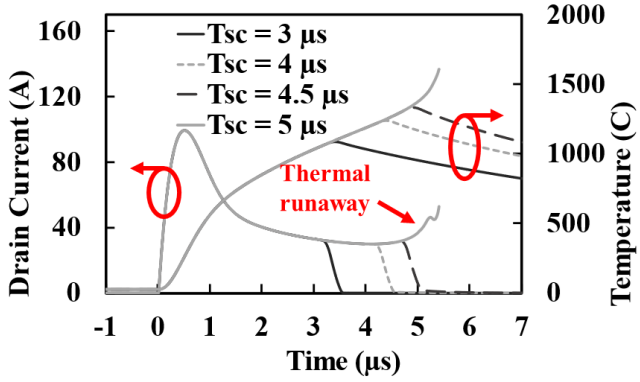

Fig. 7(a). Simulated short circuit current characteristics of the SiC Cascode JEFT

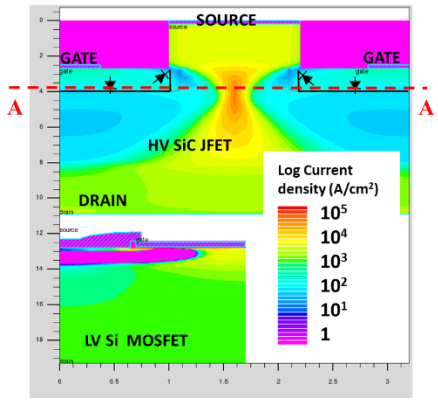

Fig. 7(b) Simulated 2D current density contour plots of the SiC Cascode JFET

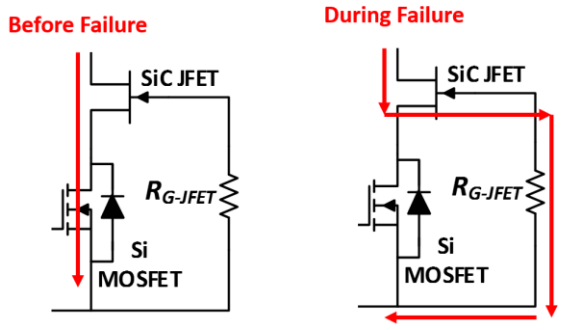

Fig. 8(a) Cascade Schematic showing current directions

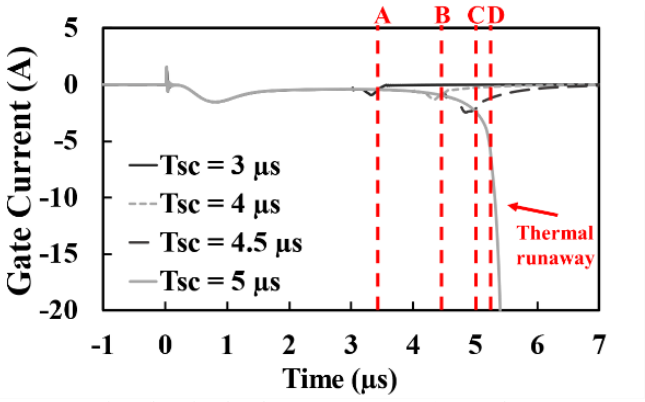

Fig. 8(b). Simulated JFET gate current (current between SiC JFET gate and LV MOSFET source)

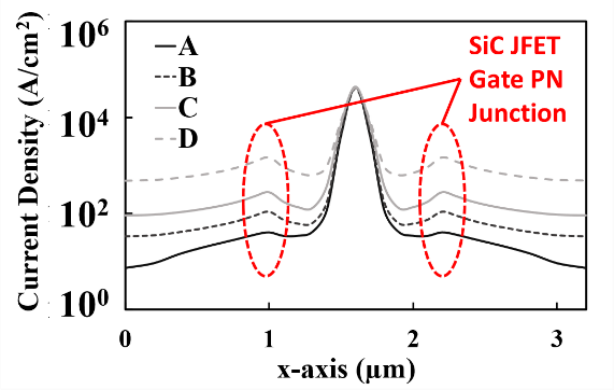

Fig. 8(c) Simulated carrier density across the JFET gate source

The finite element simulations show that the JFET internal gate is conductive after the LV MOSFET is turned OFF. It should be noted that JFET gate current being referred to here is the internal JFET gate current flowing between the JFET gate and the MOSFET source and not the gate current of the Cascode structure. The carriers flowing through the gate are thermally generated carriers due to Joule heating in the JFET. Fig 8(a) shows the Cascode structure and the direction of short circuit current flow during before and after failure. Fig. 8(b) shows the simulated gate current in the JFET (with different time instants identified) and Fig. 8(c) shows the carrier density extracted from the cut-line shown in Fig. 7(b). The JFET gate current should ideally be on the magnitude of tens of nano-amperes since it is a leakage current in a reverse biased PN junction however, the simulations show that this current increases to several amperes as shown in Fig. 8(b). Fig. 8(c)

shows that the simulated carrier density increases as the short circuit time proceeds from A to D indicating continuous Joule heating leading to increased gate leakage and source/drain short circuiting of the Cascode.

IV. Conclusions

Short circuit measurements have been performed on SiC Trench MOSFETs, SiC Planar MOSFETs and SiC Cascode JFETs. Measurements were performed with turn-OFF V_{GS} set at 0V and at -5V and the Short-Circuit-Withstand-Time (SCWT) was measured for each technology. For the SiC MOSFETs, the SCWT increases as the turn-OFF V_{GS} is reduced from 0V to -5V. For the SiC Cascode JFETs, there is no relationship between the SCWT and the turn-OFF V_{GS}. While the SiC MOSFETs failed with V_{GS} short, the SiC Cascode JFET failed with V_{DS} short. Subsequent failure analysis revealed that the gate-source terminal of the SiC Cascode JFET was still operational and capable of blocking voltage whereas the gate-source terminals of the SiC MOSFETs were shorted (due to thermally generated carriers damaging the gate dielectric). Finite element simulations of the SiC Cascode JFET showed that the bulk of the thermally generated carriers during the short circuit of the Cascode JFET flows through the gate terminal of the JFET bypassing the low voltage silicon MOSFET that is already turned-OFF. The internal connection between the SiC JFET gate and the LV silicon MOSFET source is likely damaged from excessive current density therefore causing damage to the Cascode structure.

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