Investigation of Performance of Double-Trench SiC Power MOSFETs in Forward and Reverse Quadrant Operation

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Abstract

In this paper, dynamic switching performance at 1st quadrant and 3rd quadrant operation of Silicon and Silicon Carbide (SiC) trench, double-trench, superjunction and planar power MOSFETs is analysed through a wide range of experimental measurements. The devices are evaluated on a high voltage clamped inductive switching test rig and switched with a range of switching rates at elevated junction temperatures. It is shown experimentally that, at 1st quadrant, CoolSiC MOSFET and SiC Double trench MOSFET show good stability in regard to temperature variations. Silicon superjunction MOSFETs perform unacceptably at turn-OFF transient due to their large input capacitance and are unstable with temperature variation due to the more temperature-dependent C_{GD}. SiC Planar MOSFET also performs poorly at turn-ON switching due to its low transconductance and gate threshold voltage variation leading to variations of switching rate with temperature at both turn-ON and turn-OFF transients. At 3rd quadrant, Silicon Superjunction MOSFET causes large switching loss due to its long reverse recovery process, while SiC Double trench MOSFET and CoolSiC MOSFET show stable performance with temperature variation due to the negligible reverse recovery charge.

1 Introduction

Wide-bandgap devices are now considered established device candidates in power electronics. The wide bandgap property of SiC enables high breakdown voltage, while its good thermal conductivity allows the devices to operate at high temperature. Another advantage is the high carrier saturation velocity making the devices capable of high frequency operation. Literature has reported small power loss and high conversion efficiency in power electronics [1], [2]. With the increasing requirement on operating temperature, studies have been done on the dynamic performance of 2nd generation 1.2 kV SiC planar power MOSFETs compared with Silicon IGBTs to demonstrate its superiority [3]. Power MOSFETs have a parasitic P-i-N diode, as a bipolar device, which switch in hard switching converter. The MOSFET body diode conducts current before turn-OFF [4], [5], and the stored charge in its drift region leads to current overshoot in the switching transistor during the reverse recovery of the paired diode. This reverse recovery current is temperature-dependent due to the temperature sensitivity of minority carrier lifetime. The high built-in voltage in SiC due to its wide-bandgap also increases the conduction loss, so usually a SiC Schottky barrier diode (SBD) is connected anti-parallel to the MOSFET to avoid excessive losses. However, addition of an external SBD increases the cost while its junction capacitance enhances the switching losses. To this end, researchers have investigated the performance of body diode of power MOSFETs. The SiC MOSFETs body diode has similar reverse recovery performance to SiC Schottky diode in synchronous rectification [6] while the surge current capability of SiC MOSFETs body diode is even better [7], [8]. The SiC MOSFET body diode reverse recovery is shown to be worse than SiC SBD but superior to Silicon power MOSFET body diode [9].

The aforementioned studies have mainly covered the planar SiC MOSFET structures. The JFET

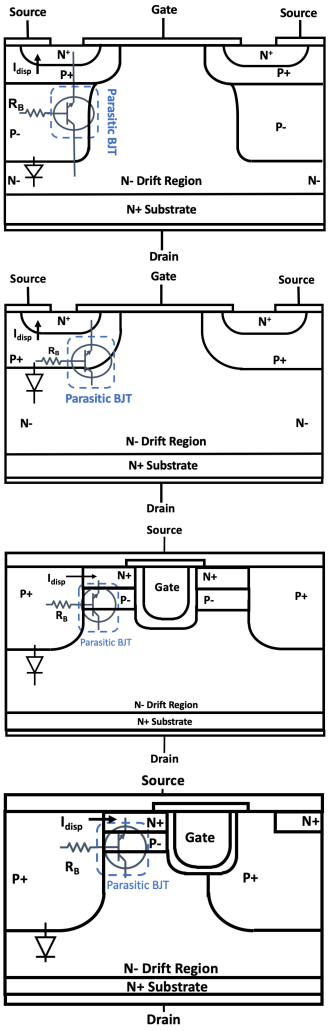

Fig. 1: Cross-section schematics of four MOSFET structures: Silicon Superjunction MOSFET, SiC Planar MOSFET, SiC Double-Trench MOSFET & CoolSiC MOSFET.

region in planar structure yields an optimum JFET dimension beyond which the on state resistance increases. This limits the scaling down of unit cells, and the gate oxide is exposed to high electric field strength which leads to reliability concerns [10]. The double-trench power MOSFETs introduce deep P pillars within every source/body cell to protect the trench gate, and reshapes the E-field distribution so the stress on the gate oxide layer is alleviated [11]. The more compact structure achieves low on-state resistance with increasing cell density, but increases the junction capacitances. The deep P pillars may re-introduce the JFET effect and limit the current spreading into the drain drift region, which is an issue in unit cell scaling down. The asymmetric double trench structure implemented in CoolSiC MOSFET by Infineon® overcomes this JFET limitation, and allows theoretical unlimited scaling down of the cell without affecting the avalanche ruggedness [11]. The higher density of cells further reduces the on-state resistance, and the P pillars induce low gate-drain capacitance enabling high frequency operation with low switching loss. Another important point is that it also effectively suppresses the parasitic BJT turn-ON.

In this paper, 1.2 kV double-trench SiC MOSFETs, 1.2 kV CoolSiC MOSFET along with 1.2 kV SiC planar MOSFET and 900 V Silicon Superjunction MOSFET are tested on clamped inductive switching test rig to evaluate and compare their switching characteristic under 8 A and 800 V for 1st quadrant and 8 A and 600 V for 3rd quadrant. The ambient temperature ranges from 25℃ to 175℃ to investigate the impact of temperature. The MOSFETs are also operated in the 3rd quadrant on the same clamped inductive switching test rig as the freewheeling diode for the inductive load. The switching device is fixed to make a fair comparison. The ambient temperature ranges from 25℃ to 175℃ to investigate the impact of temperature on the dynamic performance.

2 1st Quadrant Measurements

Experiments are performed on Infineon's Silicon Superjunction MOSFET (IPW90R340C3, 900 V, 15 A), Rohm's SiC Planar MOSFET (SCT2160KE, 1200 V, 22 A), Rohm's SiC Double trench MOSFET (SCT3160KL, 1200 V, 17 A) and Infineon's CoolSiC MOSFET (IMW120R140M1H, 1200 V, 19 A). The measurements are done on a clamped inductive switching test board shown in Fig. 2. The freewheeling diode is SiC SBD C4D08120A which is later replaced by MOSFETs body diode to test 3rd quadrant transients. The MOSFET is driven by a gate driver that provides +15V/-3V output. The current is measured with Rogowski coils and voltage is measured with GW-Instek GDP-100 100 MHz voltage probe on a Keysight MSO7104A 1-GHz & 4 GSa/s oscilloscope.

There are three factors that impact temperature dependency of MOSFET current turn-ON [12]: threshold voltage (V_{TH}), input capacitance (C_{iss}) and inversion carrier mobility (μ_{ni}). Intrinsic carrier

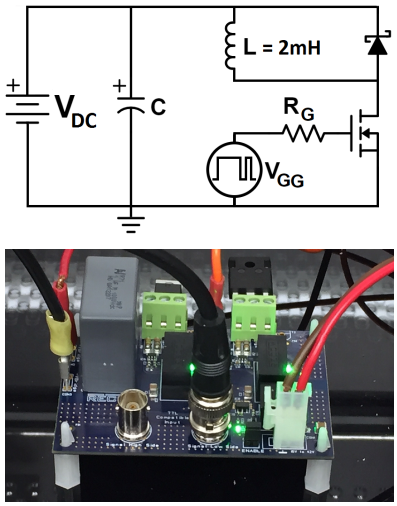

Fig. 2: The clamped inductive switching test board.

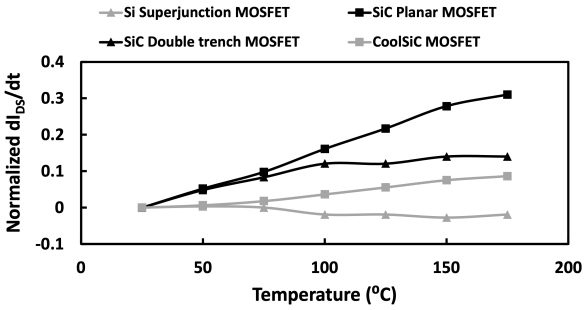

Fig. 3: Normalized current turn-ON rate to temperature with 10 Ω external gate resistance.

density and interface traps both are responsible for V_{TH} decrease as temperature rises [13] and enable MOSFET to turn-ON faster and more easily. To identify which factor is the main contributor requires further measurement on the interface traps density on DUT which is left for future work. The enhanced dopant ionization rate as well as intrinsic carrier density at higher temperature [3] [14] reduces depletion region width, yielding an increase in C_{iss} so that turn-ON process is slowed down. Silicon has negative temperature coefficient in μ_{ni} due to more significant scattering [12]. However, μ_{ni} in SiC MOSFET is reported to have a positive temperature coefficient below around 200°C and then decrease at further increased temperature due to the participation of electrons released from oxide interface traps [15]. Fig. 3 shows normalized current turn-ON rate with respect to temperature for four DUTs. Slightly negative trend with temperature is observed on Silicon superjunction MOSFET which means the three factors almost balances each other, though the effect from μ_{ni} and C_{iss} is more pronounced. Three SiC MOSFETs show faster current switching speed as temperature rises with SiC planar MOSFET being the most temperature sensitive. The reason comes from its V_{TH} which drops by around 1.5 V drop according to datasheet while it is less than 1 V for SiC double trench MOSFET and CoolSiC MOSFET over the experiment temperature range. From 100℃ onwards, SiC double trench MOSFET shows a reduced temperature dependency, indicating that C_{iss} counterbalances the influence of V_{TH} and μ_{ni}. This phenomenon could be attributed to the larger gate-drain capacitance as a feature of double trench structure [11].

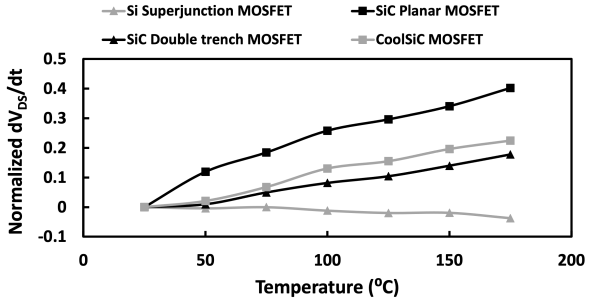

Fig. 4: Normalized voltage turn-ON rate to temperature with 10 Ω gate resistance for four DUTs.

Figure 4 shows normalized voltage turn-ON rate with respect to temperature for four DUTs. According to [12], MOSFET drain-source voltage transition is essentially charging of gate-drain capacitance given by:

$$\left.\frac{\mathrm{d}V_{DS}}{\mathrm{d}t}\right|_{ON} = \frac{V_{GG+} - V_{GP\_ON}}{C_{GD} \cdot R_G} \tag{1}$$

where V_{DS} is drain-source voltage, V_{GG+} is positive gate voltage output, V_{GP_ON} is Miller plateau at turn-ON, C_{GD} is gate-drain capacitance and R_G is total gate resistance.

Factors that affect the temperature dependency of voltage turn-ON rate are threshold voltage (V_{TH}), gate-drain capacitance (C_{GD}) and inversion carrier mobility (μ_{ni}). Negative temperature coefficient of V_{TH} and positive temperature coefficient of μ_{ni} in SiC MOSFETs would accelerates voltage transition in the means of decreasing V_{GP_ON}. Negative temperature coefficient of μ_{ni} in Silicon MOSFET hinders voltage transition by increasing

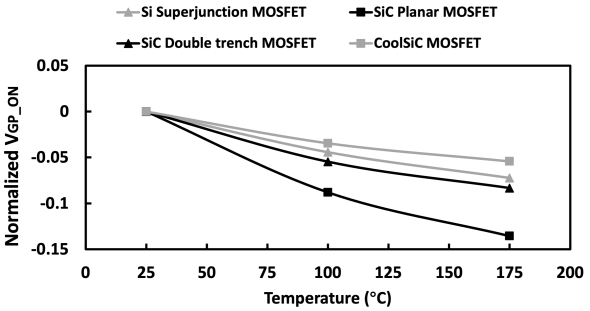

Fig. 5: Normalized Miller plateau voltage at turn-ON to temperature with 10 Ω external gate resistance for four DUTs.

V_{GP_ON}. The normalized value of V_{GP_ON} is calculated by averaging the gate-source voltage (V_{GS}) over drain-source voltage transition and is plotted on Fig. 5 against temperature. The decline of V_{GP_ON} in Silicon superjunction MOSFET suggests that the impact of V_{TH} reduction is more significant than the decreased μ_{ni}. However, Silicon superjunction MOSFET exhibits slower voltage turn-ON rate at higher temperature which means that the dominated factor is the increased C_{GD}. With the p doped source region extended into drift region in superjunction structure as shown in Fig. 1, its drift region is easily depleted at low drain bias [16]. The deep depletion region at the C_{GD} of Silicon superjunction MOSFET would amplify the temperature dependency of depletion region width, hence, it has the determinant influence on Silicon superjunction MOSFET drain-source voltage turn-ON rate. In Fig. 5, the large drop of V_{GP_ON} in SiC planar MOSFET leads to a noticeable increase in drain-source voltage turn-ON rate shown in Fig. 4 with SiC double trench MOSFET and CoolSiC MOSFET exhibiting a medium temperature sensitivity.

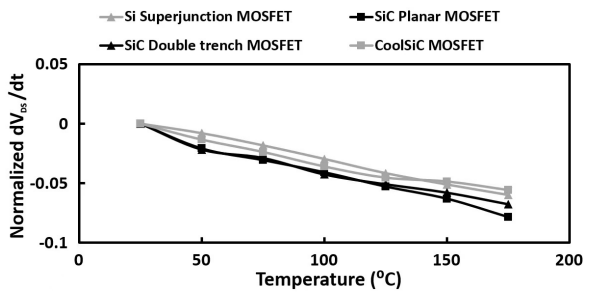

Fig. 6: Normalized voltage turn-OFF rate to temperature with 10 Ω external gate resistance for four DUTs.

Figure 6 shows normalized voltage turn-OFF rate

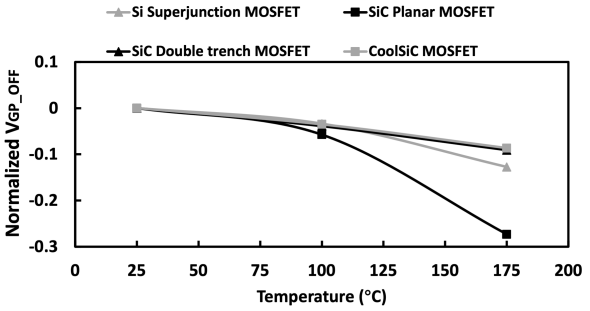

Fig. 7: Normalized Miller plateau voltage at turn-OFF to temperature with 10 Ω external gate resistance for four DUTs.

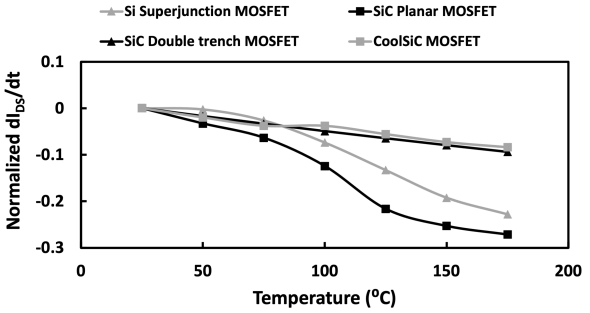

Fig. 8: Normalized current turn-OFF rate to temperature with 10 Ω external gate resistance for Four DUTs.

with respect to temperature for four DUTs. The process is an reversion of voltage turn-ON with gate current flowing out from gate terminal at Miller plateau and the equation is given by [12]:

$$\left.\frac{\mathrm{d}V_{DS}}{\mathrm{d}t}\right|_{OFF} = -\frac{V_{GP\_OFF} - V_{GG-}}{C_{GD} \cdot R_G} \qquad (2)$$

where V_{GP_OFF} is Miller plateau at turn-OFF, V_{GG-} is negative gate driver output voltage, C_{GD} is gate-drain capacitance and R_G is total gate resistance.

The value of V_{GP_OFF} is extracted by averaging the gate-source voltage during drain-source voltage turn-OFF. Its normalized value is plotted in Fig. 7 against temperature. The decreasing Miller plateau, previously enabling fast switching at turn-OFF, now impedes at turn-OFF from Eq. 2. Although different varying degree of V_{GP_OFF} is observed on DUTs, as shown in Fig. 6, the negative output voltage from a bipolar gate driver (V_{GG-}) damps the temperature dependency of voltage turn-OFF rate to a similar extent.

The normalized current turn-OFF rate with 10 Ω external gate resistance is plotted in Fig. 8

against temperature. Current turn-OFF begins simultaneously with voltage turn-OFF since there is current drawn to freewheeling SBD from DUT. According to [17], the amount of current drop during this period can be written as:

$$\Delta I = \left.\frac{\mathrm{d}V_{DS}}{\mathrm{d}t}\right|_{OFF} \cdot C_{FWD} \tag{3}$$

where C_{FWD} is the capacitance of freewheeling SBD.

Hence, the averaged switching rate for this current drop can be written as:

$$\overline{\frac{d(\Delta I)}{dt}} = \frac{(\left.\frac{\mathrm{d}V_{DS}}{\mathrm{d}t}\right|_{OFF})^2 \cdot C_{FWD}}{V_{DC}} \tag{4}$$

where V_{DC} is the DC voltage to the test circuit.

Therefore, the current turn-OFF rate for this period follows the temperature dependency of drain-source voltage turn-OFF rate which is decreasing with temperature rise. The subsequent current drop after voltage transition completed which is decay with gate voltage is determined by V_{GP_OFF} and C_{iss}. The largest drop of current turn-OFF rate for around 30% in SiC planar MOSFET comes from its similarly large drop of V_{GP_OFF} over the experiment temperature range, as shown in Fig. 7. Silicon superjunction MOSFET has only 10% drop on V_{GP_OFF} while there is 20% drop on current turn-OFF rate which can be explained by the significant impact of temperature on C_{iss} that further slows down current turn-OFF.

Device	Turn-ON Energy (μJ)	Turn-OFF Energy (μJ)
Silicon superjunction MOSFET	476	198
SiC planar MOSFET	957	130
SiC double trench MOSFET	731	113
CoolSiC MOSFET	576	94

Tab. 1: Turn-ON energy and turn-OFF energy for four DUTs at 25°C, with 10 Ω external gate resistance.

At turn-ON, Silicon superjunction MOSFET outstands from three SiC MOSFET, shown in Table. 1 in terms of energy, even with large C_{iss} as a common disadvantage of Silicon MOSFET due to large die size. This is achieved by its large transconductance parameter which can be observed from comparison of Miller plateau at turn-ON V_{GP_ON} and threshold voltage V_{TH}. These two parameters for DUTs are presented on Table. 2 with V_{GP_ON} and V_{GP_OFF} extracted by averaging gate-source voltage V_{GS} during drain-source voltage transition and V_{TH} obtained by datasheet. It can be seen Silicon superjunction MOSFET has the largest transconductance parameter with the lowest V_{GP_ON} while the smallest value for SiC planar MOSFET with highest V_{GP_ON}. Lower Miller plateau contributes to both fast current transition and voltage transition [18]. However, large transconductance does not grant benefits to Silicon superjunction MOSFET at turn-OFF since lower V_{GP_OFF} slows down switching as opposite to turn-ON. Its large C_{iss} could further worsen the situation as a large portion of turn-OFF delay of Silicon superjunction MOSFET would come from the slow decay of gate voltage to V_{GP_OFF}. At both turn-ON and turn-OFF, the two double trench MOSFETs exhibits improved performance from SiC planar MOSFET, majority of improvement are due to the reduced input capacitance. CoolSiC MOSFET even achieves better performance than SiC double trench MOSFET as a result of reduction of C_{GD} from its asymmetric double trench structure.

Device	V_{GP_ON} (V)	V_{GP_OFF} (V)	V_{TH} (V)
Silicon superjunction	6.44	2.67	2.5∼3.5
SiC planar	12.65	2.78	1.6∼4
SiC double trench	11.1	3.85	2.7∼5.6
CoolSiC	10.4	3.7	3.5∼5.7

Tab. 2: Threshold voltage and Miller plateau voltage for four DUTs at 25°C with 10 Ω external gate resistance.

3 Measurement on 3rd Quadrant Operation

Measurements have indicated that the reverse recovery charge increases with temperature because of the increase of the carrier lifetime in the body diode drift region. This charge can be approximated by:

$$Q_{RR} = I_F \cdot \tau$$

where τ is the high-level minority carrier lifetime in the body diode drift region and I_F is the forward current.

Silicon Superjunction MOSFET has a very large stored charge during conduction. In addition to the higher minority carrier lifetime in Silicon, the charge storage mechanism in the superjunction structure is significantly contributing to this. The structure is effectively a $P^+N^-N^+$ diode in parallel with a $P^+P^-N^+$ diode at 3rd quadrant operation, so both electrons and holes act as stored charge while the body diode is conducting [9]. SiC MOSFET show smaller reverse recovery current at 3rd operation. On one hand, this is due to the low carrier life time in Silicon Carbide which stores little charge during conduction of MOSFET body diode; on the other hand, the high knee voltage of SiC MOSFET body diode as well as strong body effect as a consequence of the physical nature of Silicon Carbide suppresses the trigger-on of body diode but conduct current in channel which is unipolar [19]. With temperature rise, increased scattering raises the channel resistance thus a higher voltage is applied to the body diode of SiC MOSFET. Along with the drop of knee voltage due to enhanced thermal generation, the likelihood of turning on body diode of SiC MOSFET is increased which yields a more significant reverse recovery in addition to longer carrier lifetime.

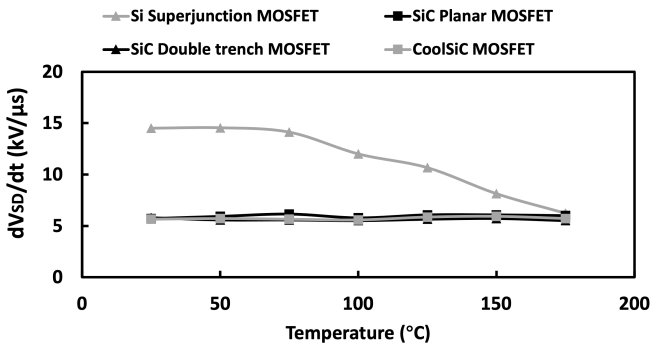

Fig. 9: Voltage turn-OFF rate to temperature of DUTs at 3rd operation.

The temperature has almost no impact on the switching rate at 3rd operation except in Silicon superjunction MOSFET, the high temperature significantly reduces the voltage turn-OFF rate, as shown in Fig. 9. The reason for this phenomenon is the huge reverse recovery current of Silicon superjunction MOSFET. At 25°C, voltage transition happens when the reverse recovery current is returning to zero as shown in Fig. 10 which means the drain current through the bottom-side MOSFET is declining. This declining drain current at bottom-side MOSFET, incorporating the source inductance, results in a larger effective gate-source voltage and would accelerate the switching. Therefore, Silicon superjunction MOSFET also has the leading voltage transition rate than other DUTs. As the peak reverse recovery current increases with temperature, voltage transition on Silicon superjunction MOSFET at 3rd quadrant takes place earlier when its reverse recovery has not reaching the negative peak, shown as 175°C in Fig. 10. This appears as increasing drain current to the bottom-side MOSFET and results in smaller effective gate-source voltage by incorporating source inductance.

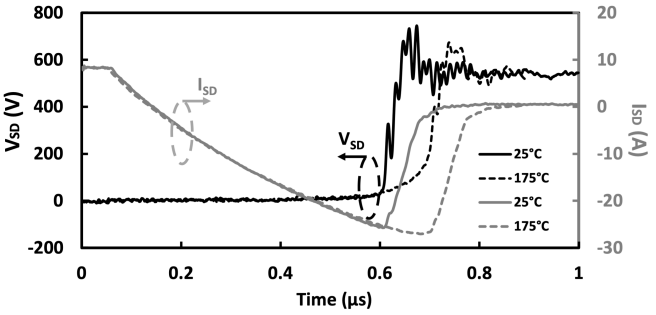

Fig. 10: Voltage and current transient of Silicon Superjunction MOSFET 3rd quadrant operation at turn-OFF at 25°C and 175°C.

The reverse recovery becomes more significant in Silicon Superjunction MOSFET with increased forward current level in terms of reverse recovery current, reverse recovery time and reverse recovery charge as shown in Fig. 11. This means more charge is stored in the device at conductivity modulation, so these charge will take longer to recombine when the MOSFET body diode is turned-OFF. As for the other three SiC MOSFETs, this trend is opposite. The reason is the extended switching time. Although higher current accumulates more charge on the device, the longer switching time means more charge would recombine during the switching process and yields a net decrease in the residual charge when the reverse recovery takes place. SiC double trench MOSFET and CoolSiC MOSFET both show less reverse recovery peak current, charge and time than SiC planar MOSFET which suggests the charge storage is minimized at 3rd quadrant by implementing double trench structure.

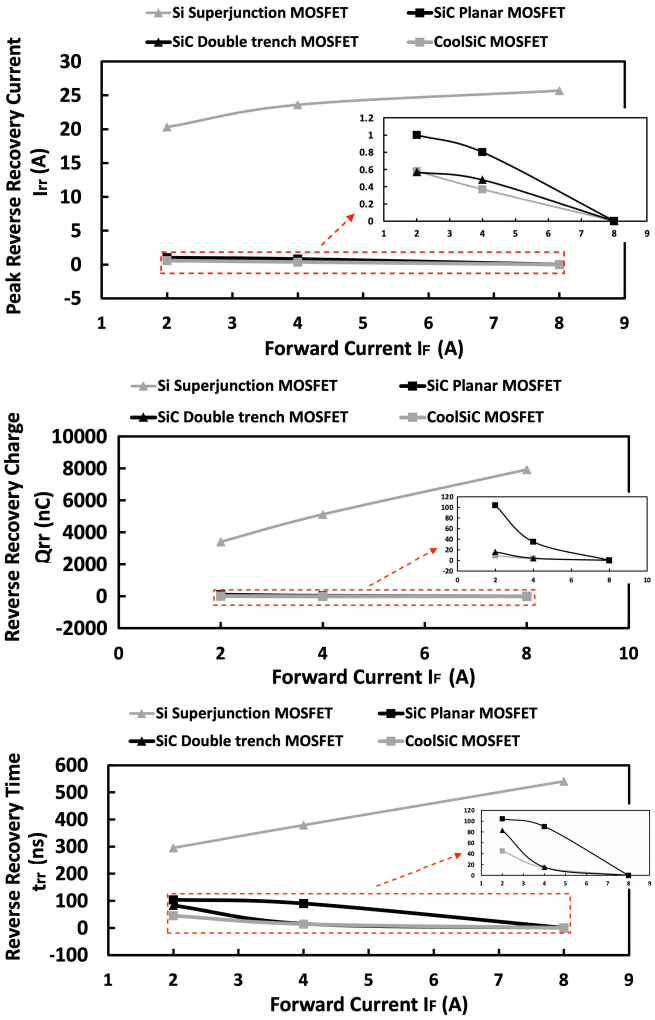

Fig. 11: The peak reverse recovery current, reverse recovery charge, and recovery time of DUTs to forward current level at 25°C with 10 Ω gate resistance.

4 Conclusion

The switching performance of 1.2 kV SiC planar MOSFET, 1.2 kV SiC double trench MOSFET, 1.2 kV CoolSiC MOSFET and 900 V Silicon superjunction MOSFET are compared experimentally along with their 3rd quadrant operation. Silicon superjunction MOSFET performs unacceptably due to its temperature-dependent C_{GD} and high input capacitance, though it benefits from the large transconductance parameter at turn-ON. Its 3rd quadrant operation has large switching losses as a result of the reverse recovery charge which rises further at high temperature due to its increased lifetime and reduced voltage turn-OFF rate. SiC planar MOSFET exhibits slow switching at turn-ON as a consequence of its small transconductance parameter which generates large switching losses, though its highly temperature-dependent threshold voltage is able to reduce switching energy loss at high temperature. At 3rd quadrant operation, its reverse recovery charge would result in more switching loss, especially at high temperature. SiC double trench MOSFET and CoolSiC MOSFET maintain excellent switching performance at all temperatures, due to the reduced C_{iss} by their specific structure. The switching loss of the CoolSiC MOSFET is even less than that of the SiC double-trench MOSFET. When operated at 3rd quadrant, SiC double trench MOSFET and CoolSiC MOSFET both shows good suppression on charge storage than conventional planar structure.

References

[1] Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, B. J. Blalock, and et al., "Design and performance evaluation of overcurrent protection schemes for silicon carbide (SiC) power MOSFETs," in *IEEE Energy Conversion Congress and Exposition*, 2013, pp. 5418–5425. DOI: 10.1109/ECCE.2013.6647436.

[2] S. Jahdi, O. Alatise, C. Fisher, L. Ran, and P. Mawby, "An Evaluation of Silicon Carbide Unipolar Technologies for Electric Vehicle Drive-Trains," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 517–528, 2014. DOI: 10.1109/JESTPE.2014.2307492.

[3] J. Qi, K. Tian, Z. Mao, S. Yang, W. Song, and et al., "Dynamic performance of 4H-SiC power MOSFETs and Si IGBTs over wide temperature range," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 2712–2716. DOI: 10.1109/APEC.2018.8341400.

[4] Z. Wang, X. Wu, J. Zhang, and K. Sheng, "Evaluation of reverse recovery characteristic of silicon carbide metal–oxide–semiconductor field-effect transistor intrinsic diode," *IET Power Electronics*, vol. 9, no. 5, pp. 969–976, 2016. DOI: 10.1049/iet-pel.2014.0965.

[5] J. O. Gonzalez, R. Wu, S. Jahdi, and O. Alatise, “Performance and Reliability Review of 650 V and 900 V Silicon and SiC Devices: MOSFETs, Cascode JFETs and IGBTs,” *IEEE Transactions on Industrial Electronics*, vol. 67, no. 9, pp. 7375–7385, 2020. DOI: 10.1109/TIE.2019.2945299.

[6] S. Yin, Y. Liu, Y. Liu, K. J. Tseng, J. Pou, and et al., “Comparison of SiC Voltage Source Inverters Using Synchronous Rectification and Freewheeling Diode,” *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1051–1061, 2018. DOI: 10.1109/TIE.2017.2733483.

[7] B. Heinze, J. Lutz, M. Neumeister, R. Rupp, and M. Holz, “Surge Current Ruggedness of Silicon Carbide Schottky- and Merged-PiN-Schottky Diodes,” in *20th Int. Symposium on Power Semiconductor Devices and IC’s*, 2008, pp. 245–248. DOI: 10.1109/ISPSD.2008.4538944.

[8] S. Jahdi, O. Alatise, J. A. Ortiz Gonzalez, R. Bonyadi, L. Ran, and P. Mawby, “Temperature and Switching Rate Dependence of Crosstalk in Si-IGBT and SiC Power Modules,” *IEEE Transactions on Industrial Electronics*, vol. 63, no. 2, pp. 849–863, 2016. DOI: 10.1109/TIE.2015.2491880.

[9] S. Jahdi, O. Alatise, R. Bonyadi, P. Alexakis, C. A. Fisher, and et al., “Analysis of Switching Performance and Robustness of Power MOSFETs Body Diodes: A Technology Evaluation,” *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2383–2394, 2015. DOI: 10.1109/TPEL.2014.2338792.

[10] T. Nguyen, A. Ahmed, T. V. Thang, and J. Park, “Gate Oxide Reliability Issues of SiC MOSFETs Under Short-Circuit Operation,” *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2445–2455, 2015. DOI: 10.1109/TPEL.2014.2353417.

[11] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and et al., “The Trench Power MOSFET: Part I—History, Technology, and Prospects,” *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 674–691, 2017. DOI: 10.1109/TED.2017.2653239.

[12] B. J. BALIGA, *Fundamentals of power semiconductor devices*. SPRINGER NATURE, 2019.

[13] S. Chen, C. Cai, T. Wang, Q. Guo, and K. Sheng, “Cryogenic and high temperature performance of 4H-SiC power MOSFETs,” in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 207–210. DOI: 10.1109/APEC.2013.6520209.

[14] Q. Min, E. Li, and J. Jin., “Modeling and Analysis for MOS Capacitance of TSV Considering Temperature Dependence,” in *Joint International Symposium on Electromagnetic Compatibility*, 2019, pp. 350–353.

[15] J. Sun, H. Xu, X. Wu, S. Yang, Q. Guo, and K. Sheng, “Short circuit capability and high temperature channel mobility of SiC MOSFETs,” in *2017 29th International Symposium on Power Semiconductor Devices and IC’s (ISPSD)*, 2017, pp. 399–402. DOI: 10.23919/ISPSD.2017.7988988.

[16] B. J. Daniel, C. D. Parikh, and M. B. Patil, “Modeling of the CoolMOS/sup TM/ transistor - Part I: Device physics,” *IEEE Transactions on Electron Devices*, vol. 49, no. 5, pp. 916–922, 2002. DOI: 10.1109/16.998603.

[17] J. Wang, H. S. Chung, and R. T. Li, “Characterization and Experimental Assessment of Effects of Parasitic Elements on MOSFET Switching Performance,” *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 573–590, 2013. DOI: 10.1109/TPEL.2012.2195332.

[18] D. A. Grant and J. Gowar, *Power mosfets: theory and applications*. Wiley, 1989.

[19] K. Lindberg-Poulsen, L. P. Petersen, Z. Ouyang, and M. A. E. Andersen, “Practical investigation of the gate bias effect on the reverse recovery behavior of the body diode in power MOSFETs,” in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, 2014, pp. 2842–2849. DOI: 10.1109/IPEC.2014.6870084.